Reference Schematics For RK3588S

RK3588S_Tablet_Demo_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x
4) ROM: eMMC5.1(Default)
5) Support: 1 x Type-C 3.0(with DP function)
6) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
7) Support: 1 x 2Lanes MIPI DPHY RX Camera
8) Support: 1 x 4Lanes MIPI D/CPHY TX
9) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
11) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
12) Support: 2 x PDM MIC Array
13) Support: Gyroscope+G-sensor+Ambient Light+Proximity

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	00.Cover Page				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	1 of 32

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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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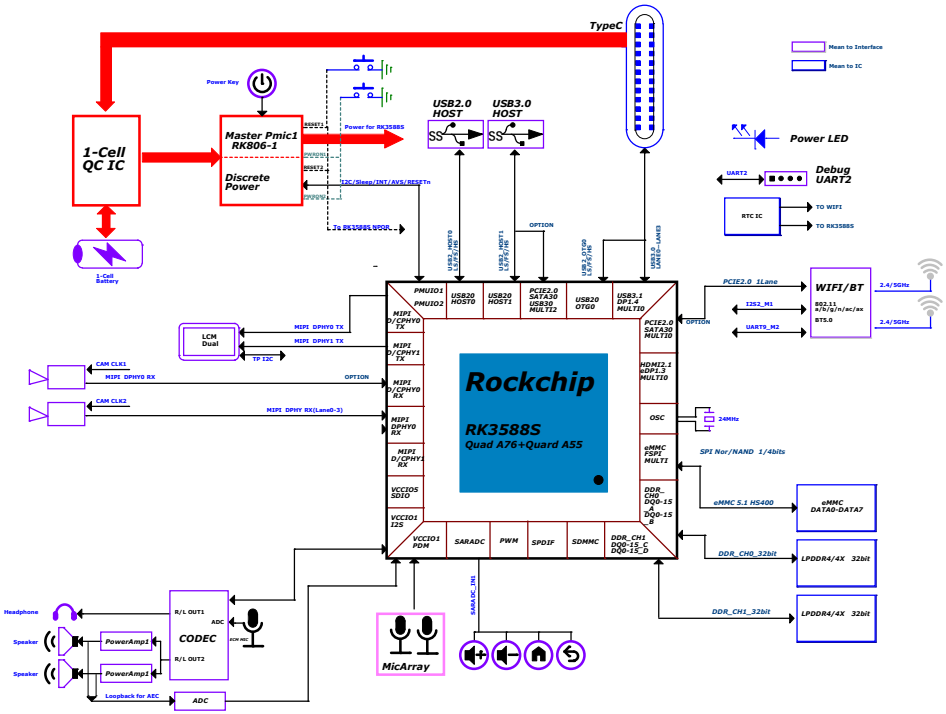
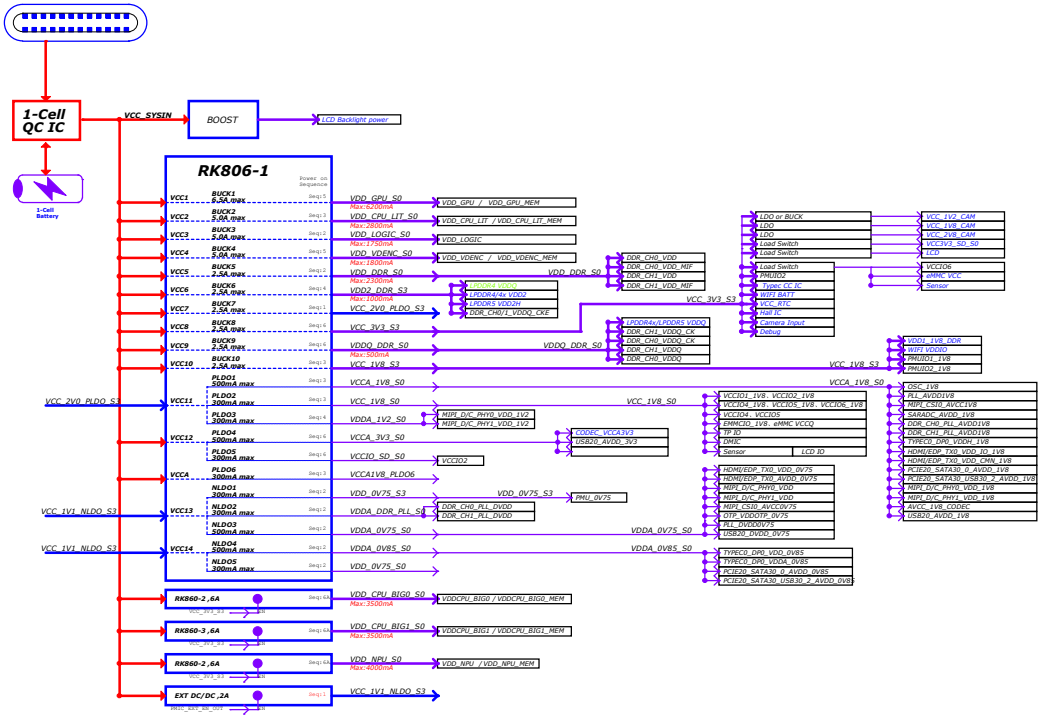
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.Wei	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203，L2205，L2207，L2300，L2301，L2302电感由0.22uH(TDK)改为0.24uH(Sunlord); L2201的电感由0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。	

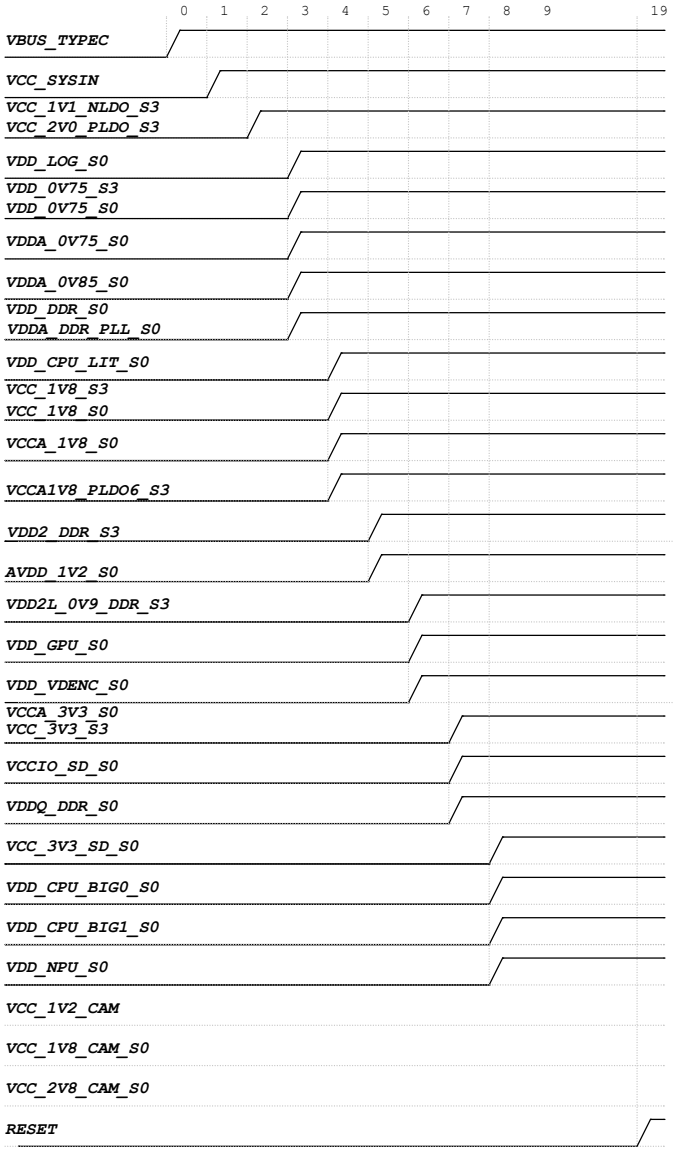
RK3588S Tablet Demo Block Diagram for 1-Cell Charger



Power tree for 1-Cell Charger



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	05.System Power Sequence				
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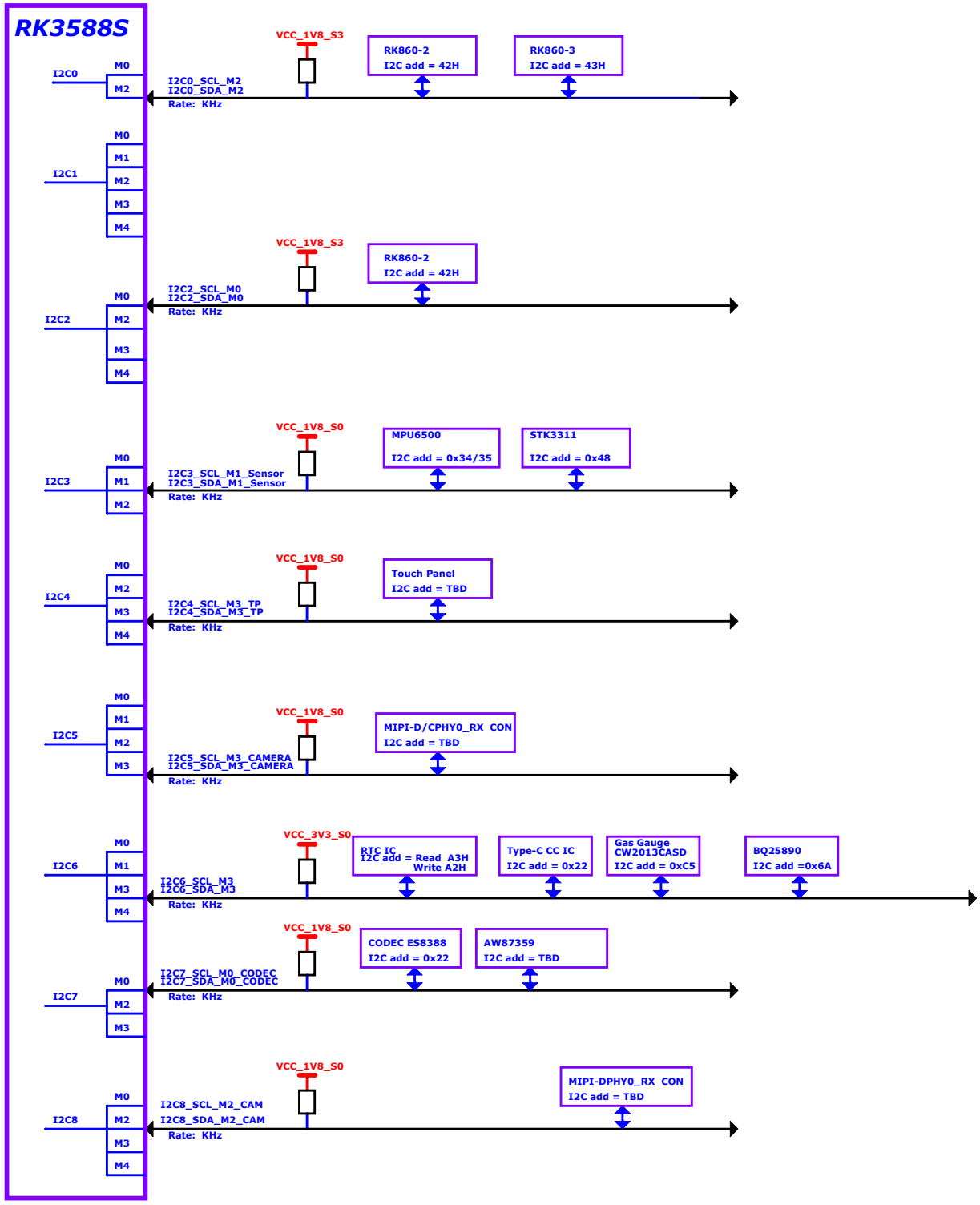
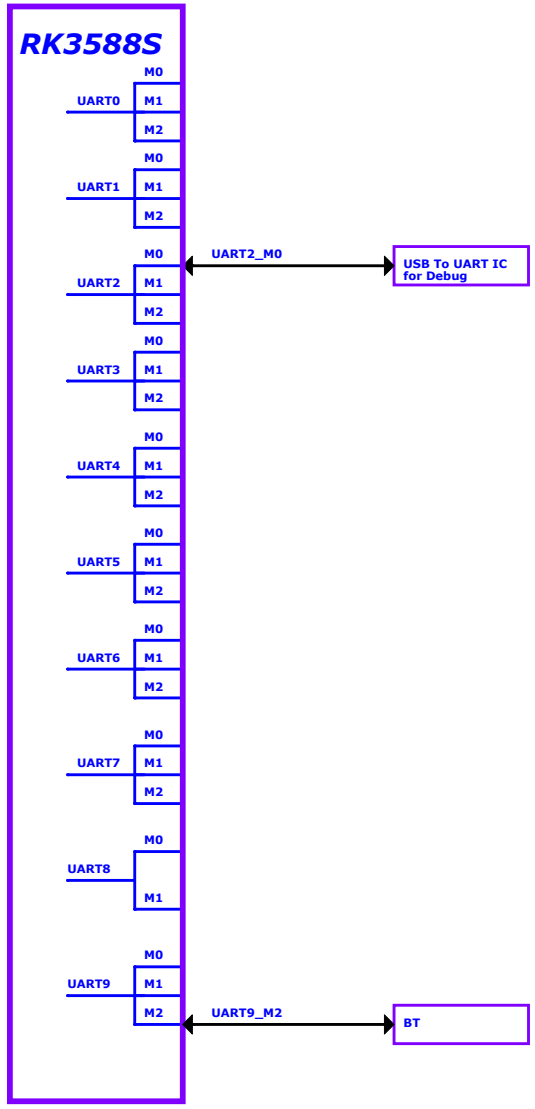
I2C MAP



UART MAP



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Demo
File:	06.Lower-Speed Bus Map
Date:	Monday, January 24, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
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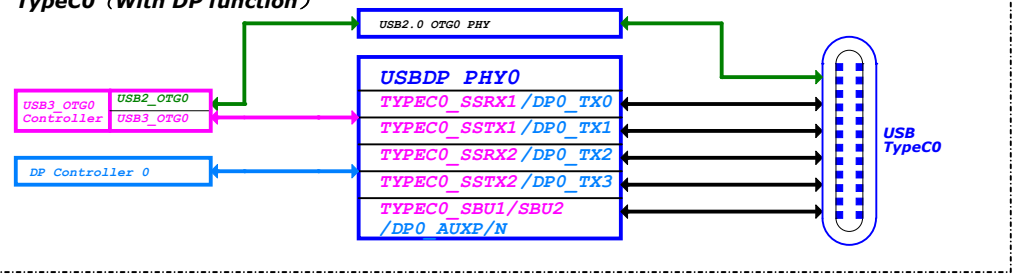
USB Controller Configure Table

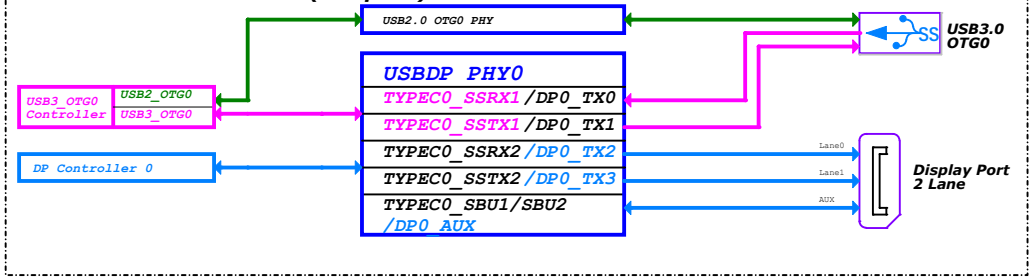
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

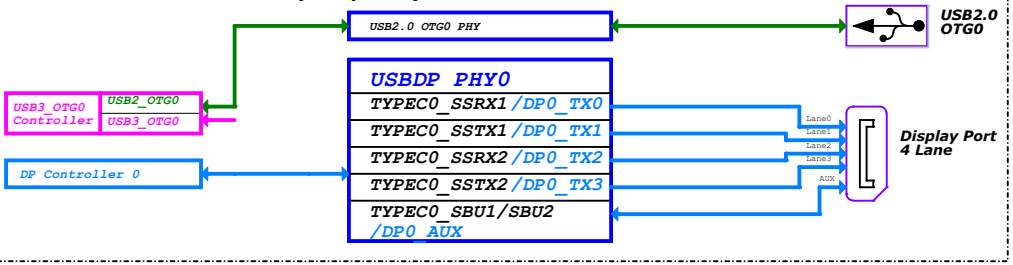
Config0:
TypeC0（With DP function）



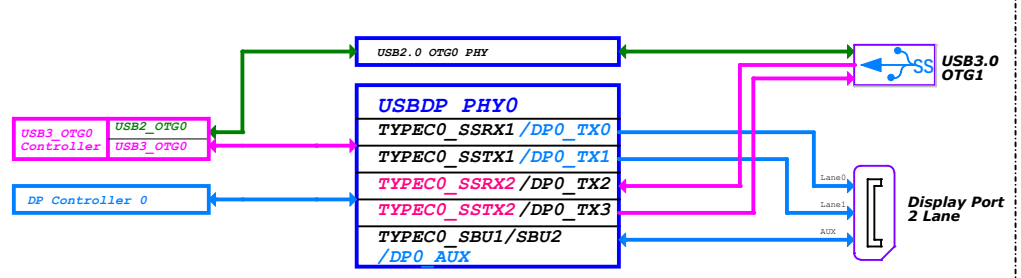
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



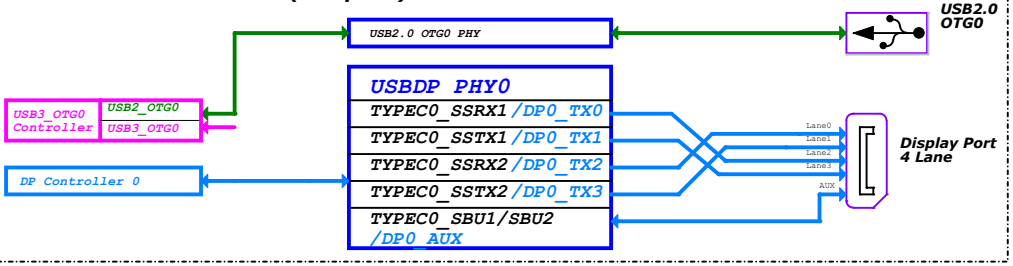
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Demo
File:	07.USB Controller Configure Tab
Date:	Friday, January 07, 2022
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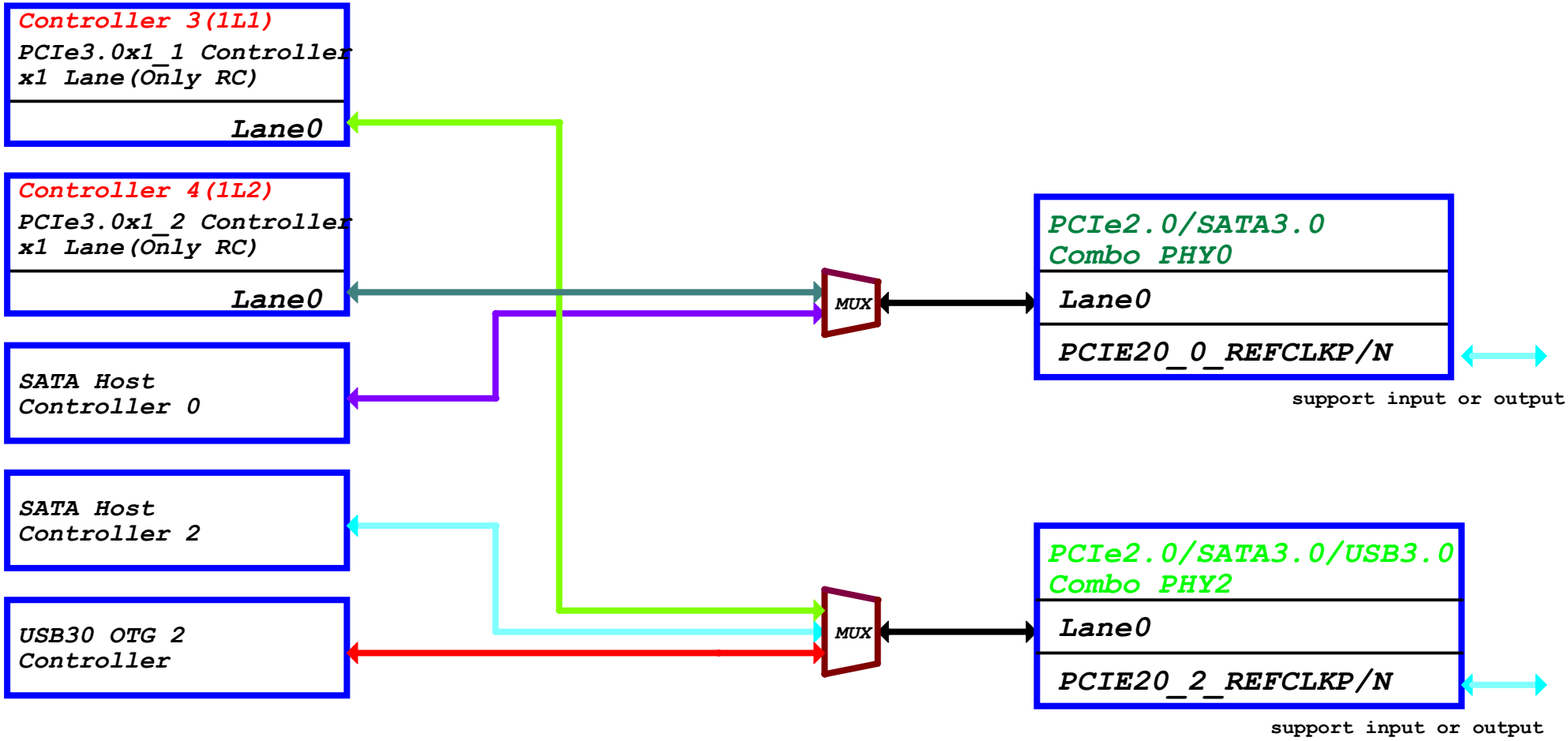
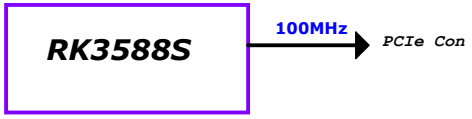
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

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Date:	Friday, January 07, 2022			Rev:	V10
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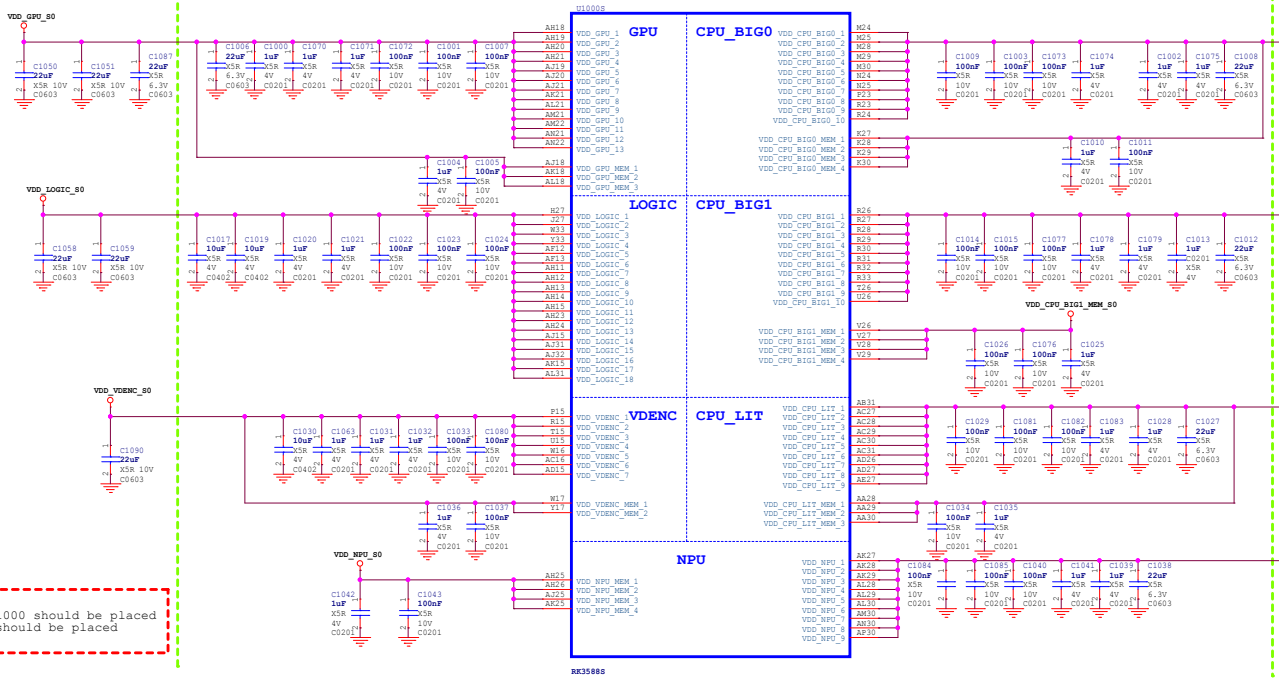
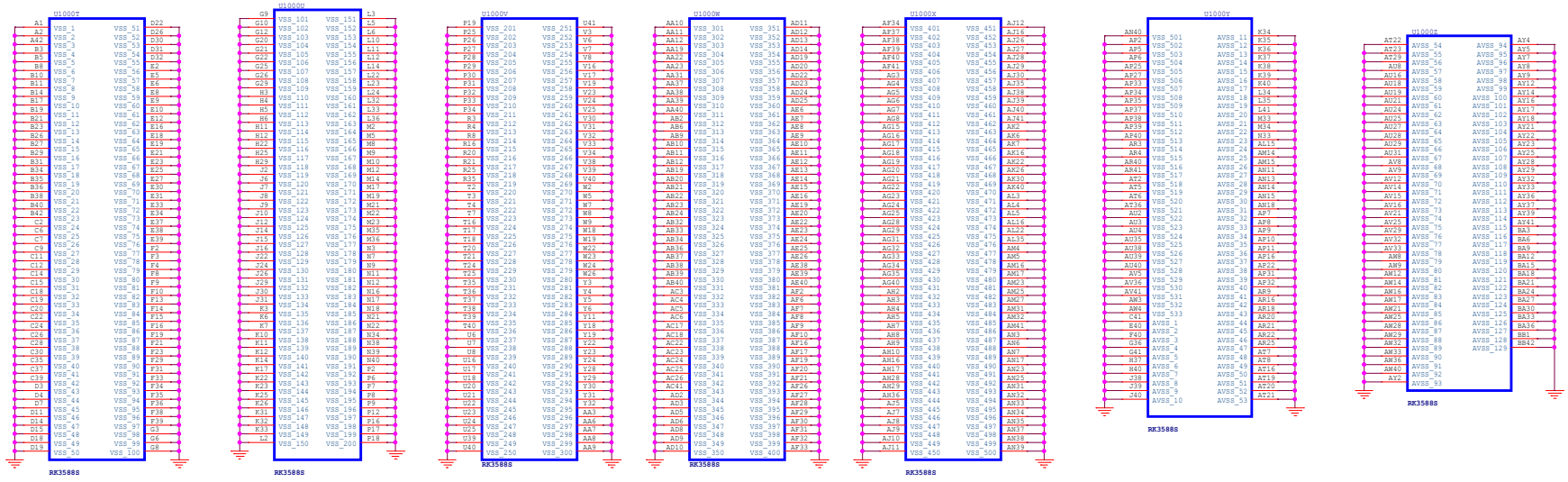
RK3588S(Power&Gnd)



Note:

The Caps between green line and yellow line should be placed under the U1000 package.Other caps should be placed close to the U1000 package



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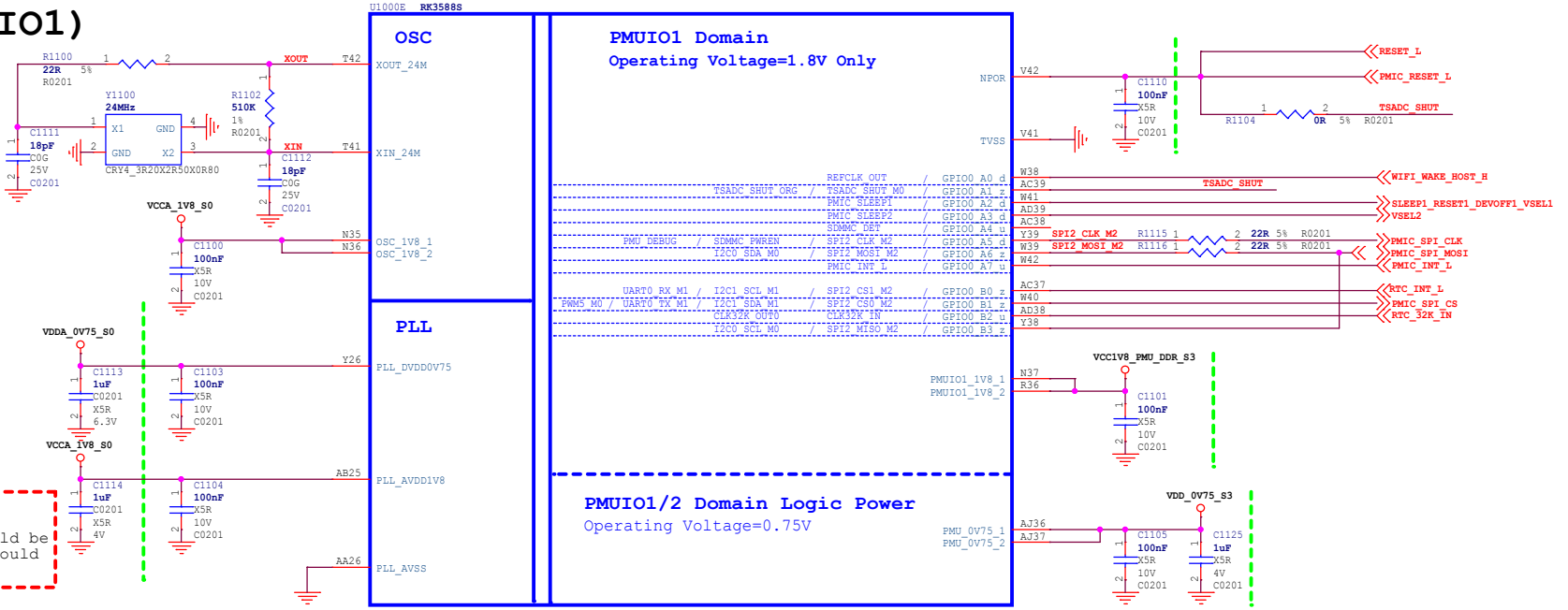
RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

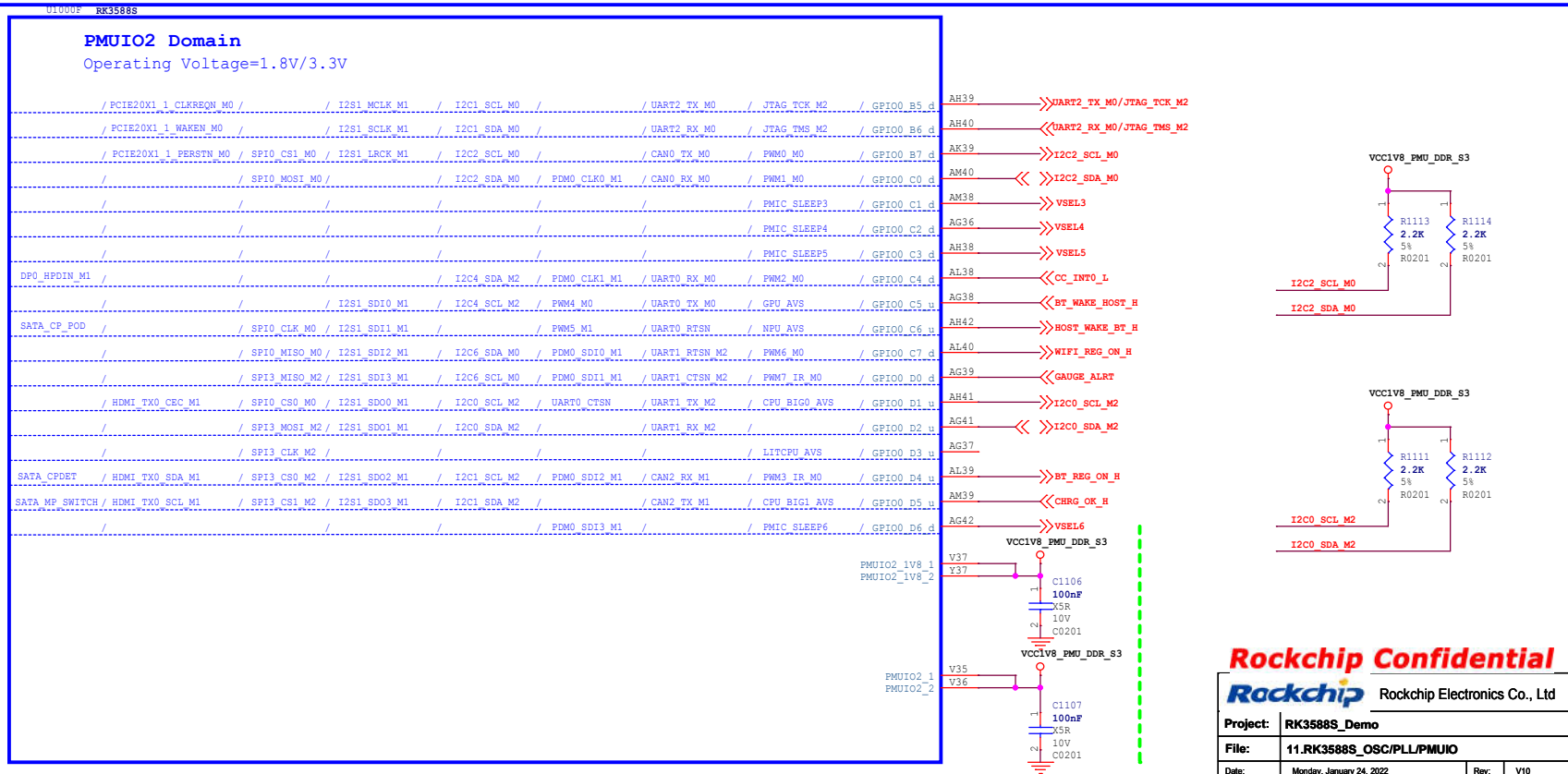
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588S(PMUIO2)



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Project:	RK3588S_Demo				
File:	11.RK3588S_OSC/PLL/PMUIO				
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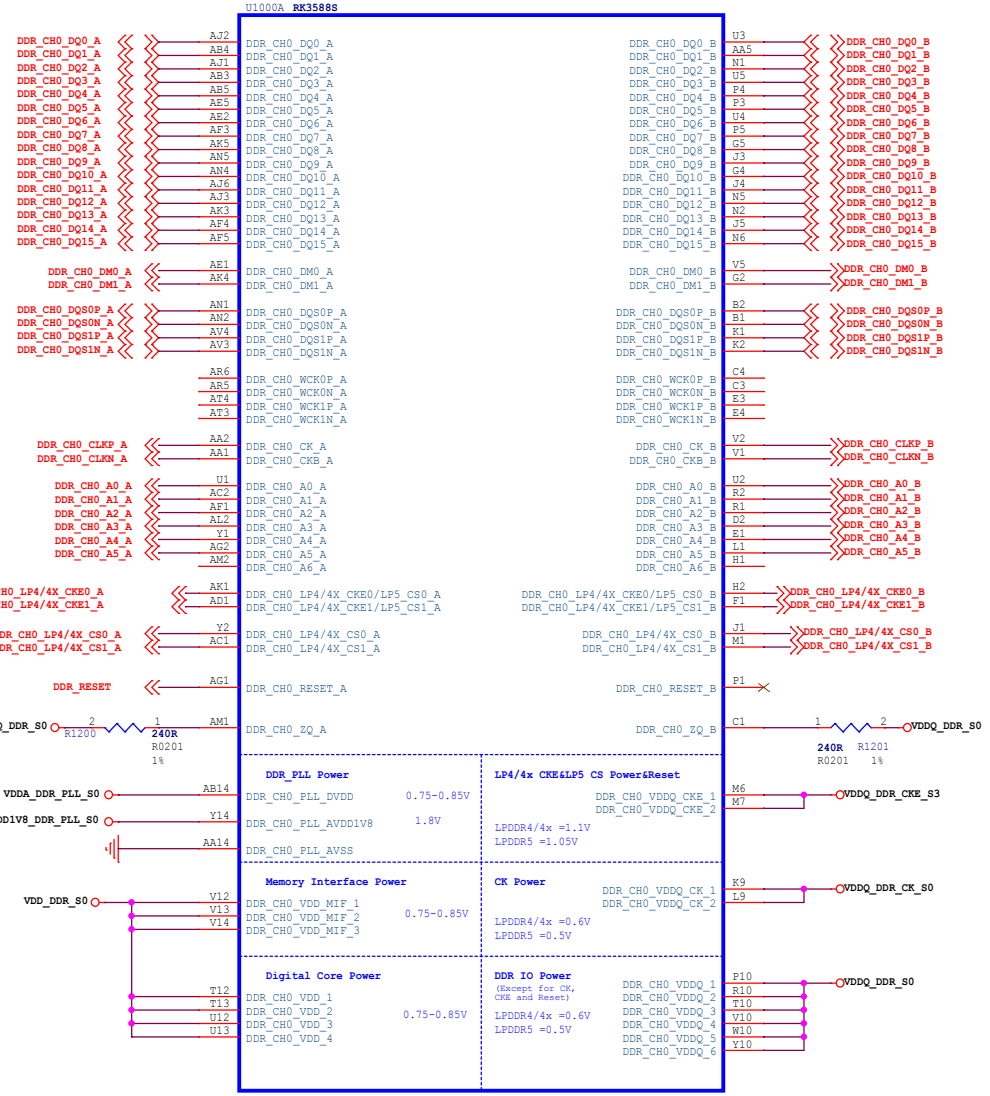
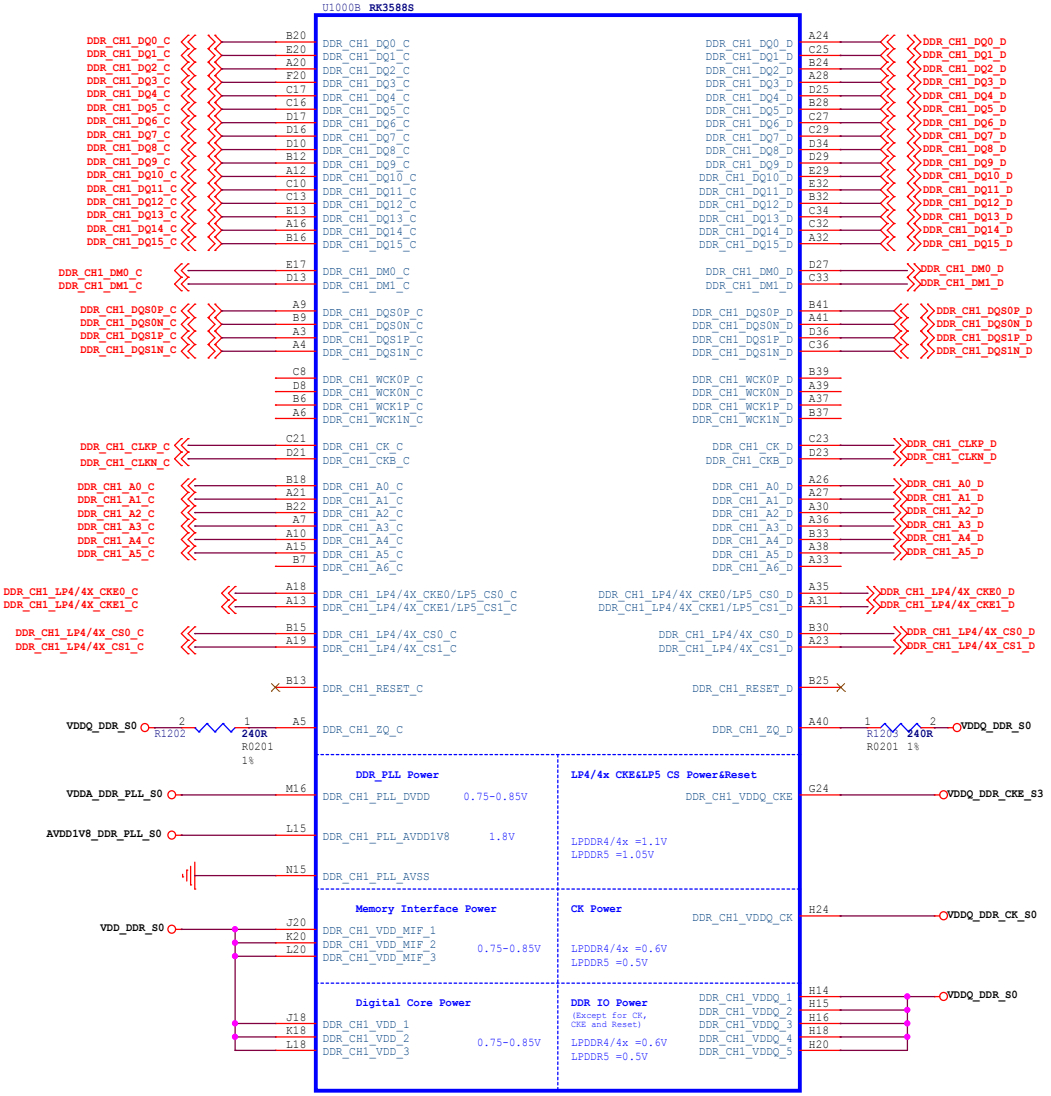
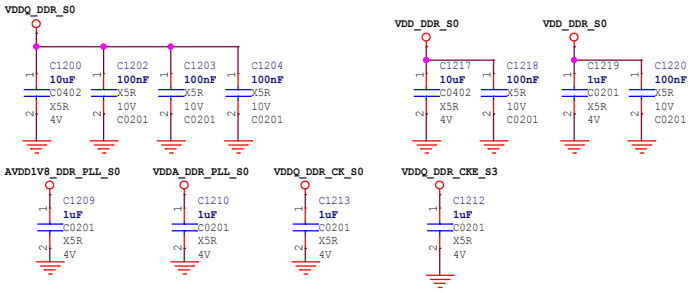
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	10 of 32

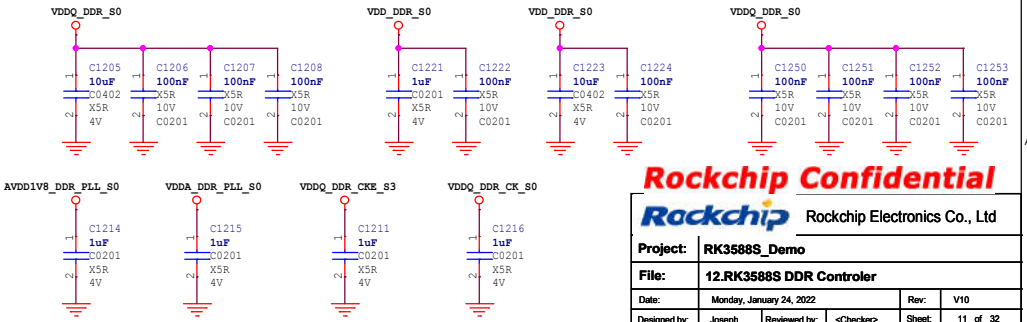
RK3588S(DDR PHY)





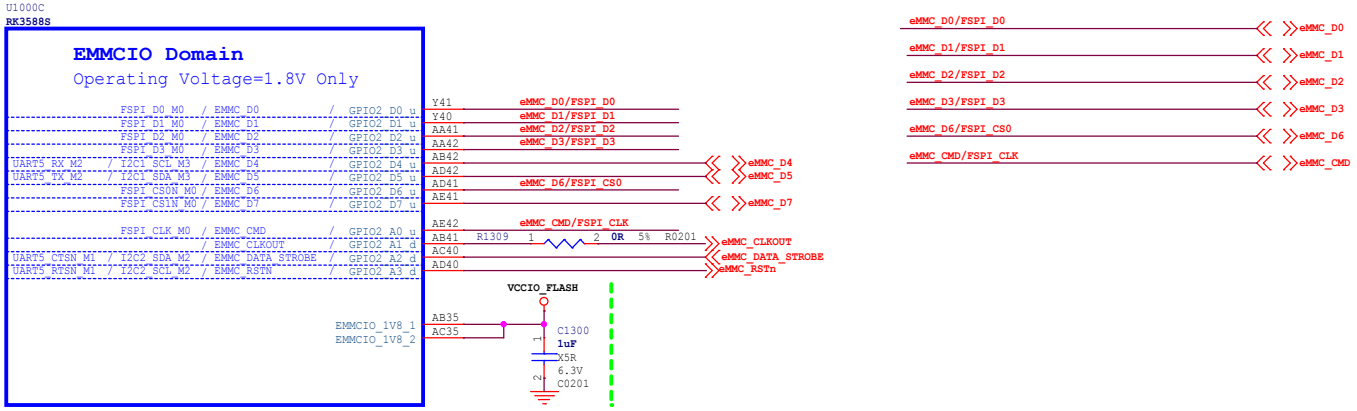
DDR FILTER



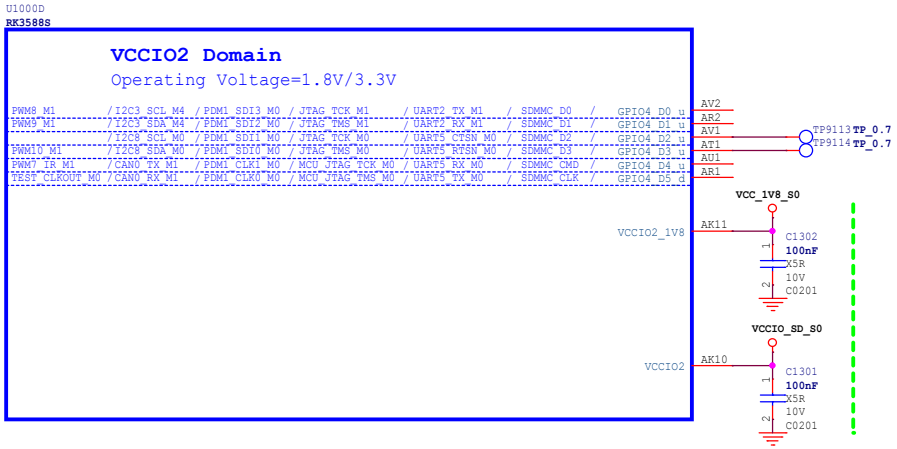


Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	12.RK3588S DDR Controler				
Date:	Monday, January 24, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	11 of 32

RK3588S(EMMCIO Domain)



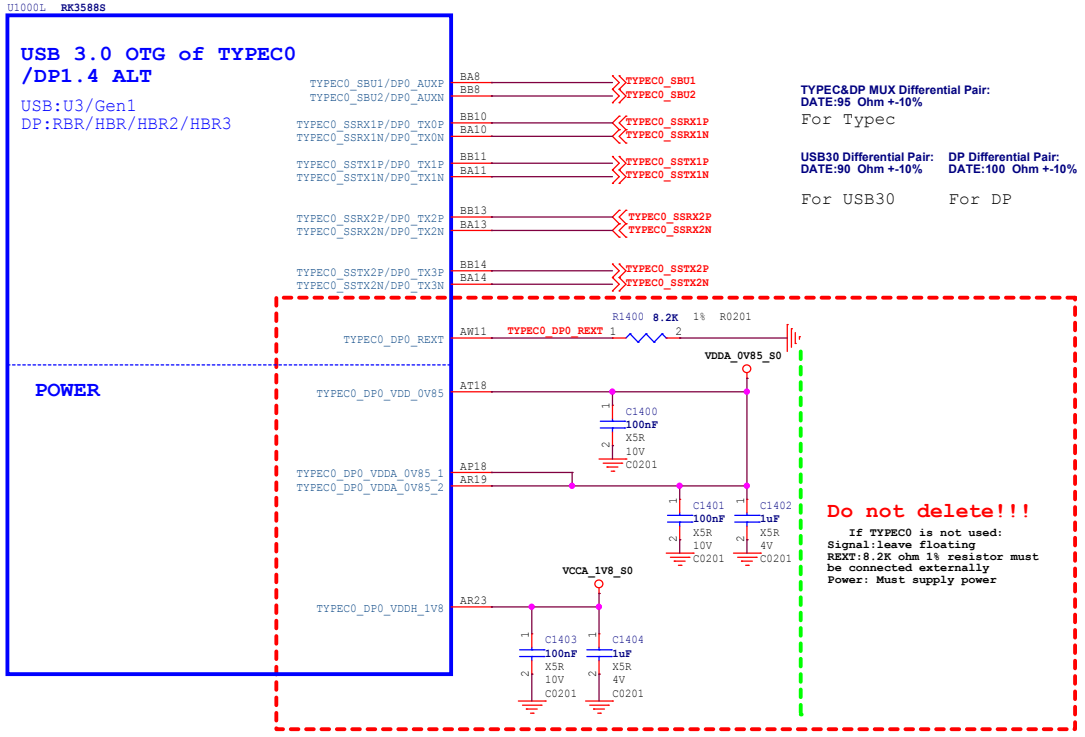
RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	13.RK3588S Flash/SD Controller				
Date:	Wednesday, January 12, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	12 of 32

RK3588S(USB3.0/DP1.4)

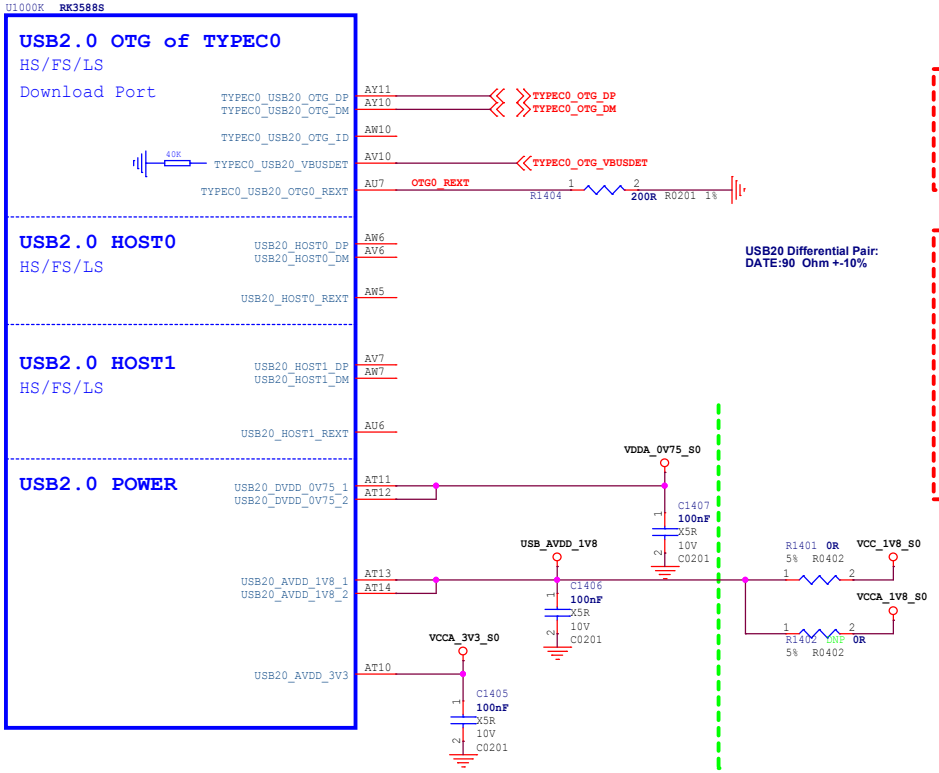


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

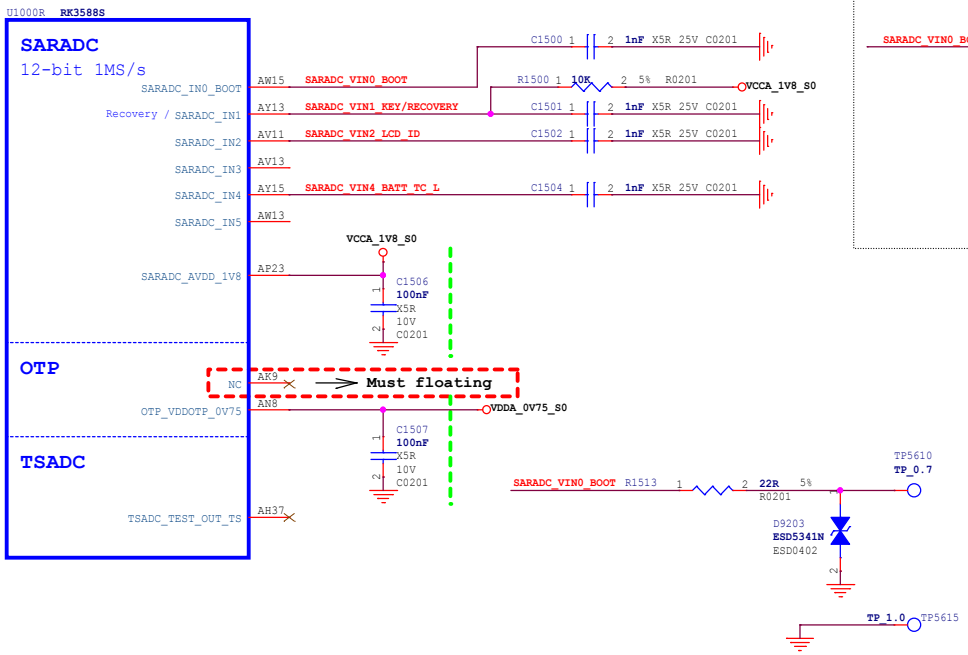
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

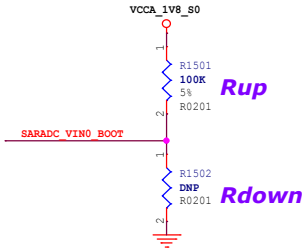
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	14.RK3588S_USB20/USB30/DP PHY				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 32

RK3588S(SARADC/OTP/TSADC)

SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_LCD_ID
SARADC_VIN4_BATT_TC_L

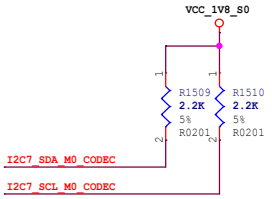


BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

RK3588S(VCCIO1 Domain)



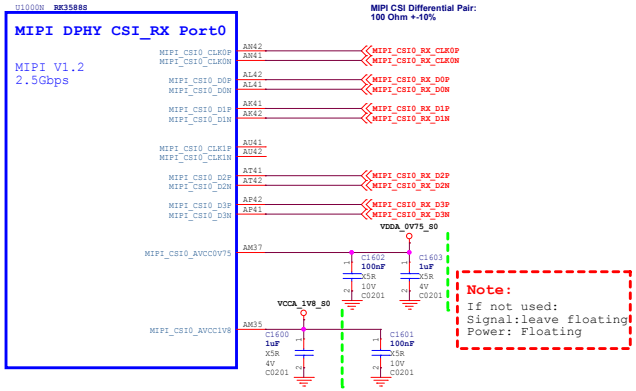
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd

Project:	RK3588S_Demo				
File:	15.RK3588S_SARADC/1.8V GPIO				
Date:	Friday, January 14, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	14 of 32

RK3588S(MIPI_DPHY CSI0 RX)

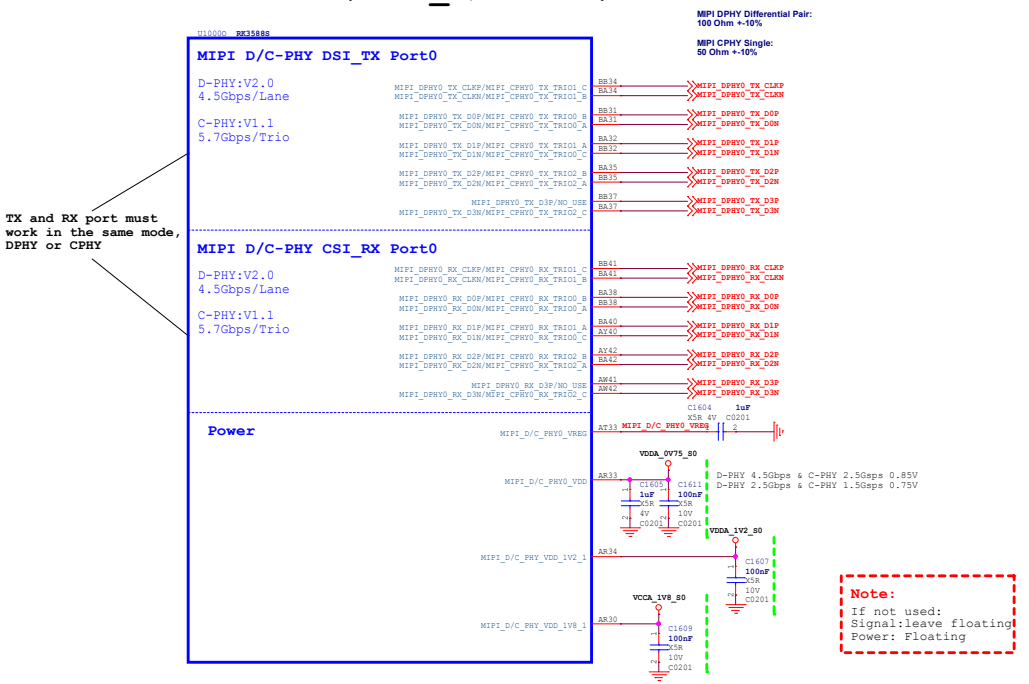


Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

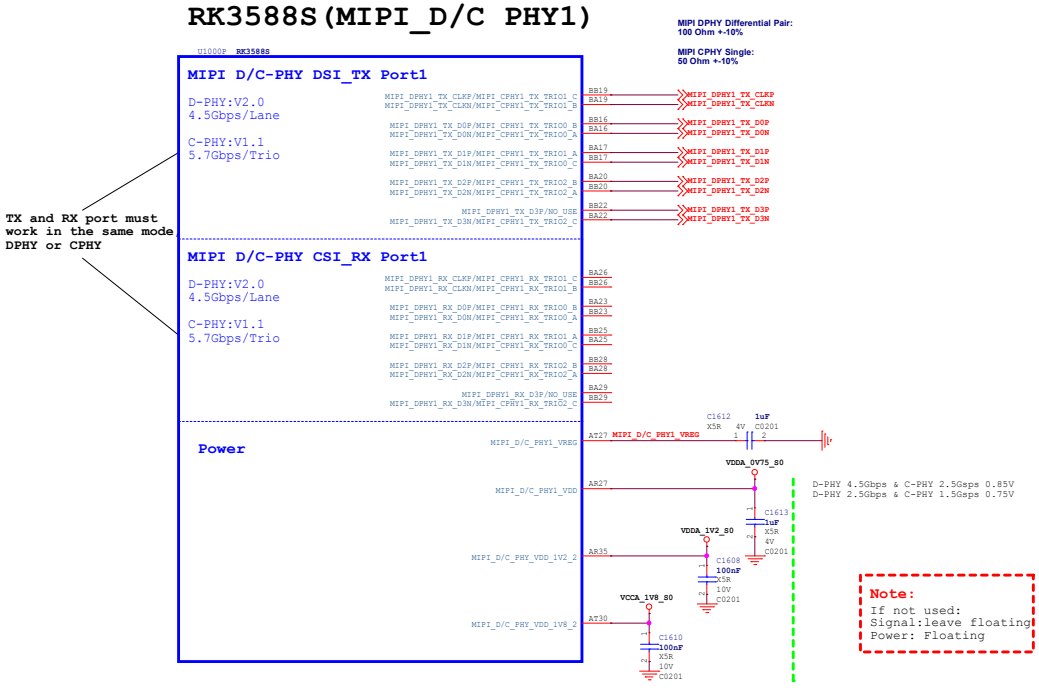
Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



RK3588S(MIPI_D/C PHY1)



Rockchip Confidential

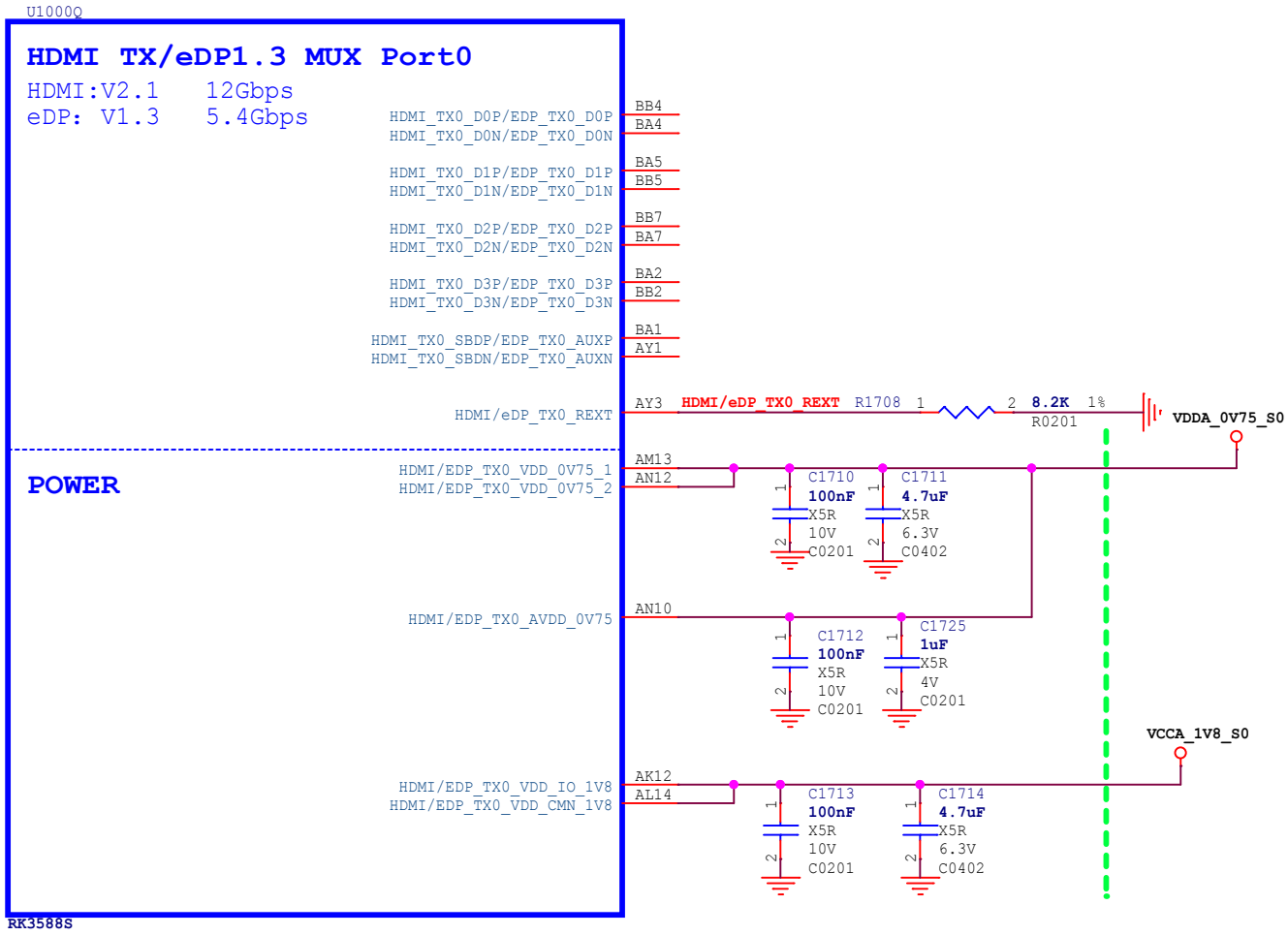
Rockchip Electronics Co., Ltd			
Project:	RK3588S_Demo		
File:	16.RK3588S_MIPI Interface		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet	15 of 32

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm ±10%

HDMI TX
100 Ohm ±10%



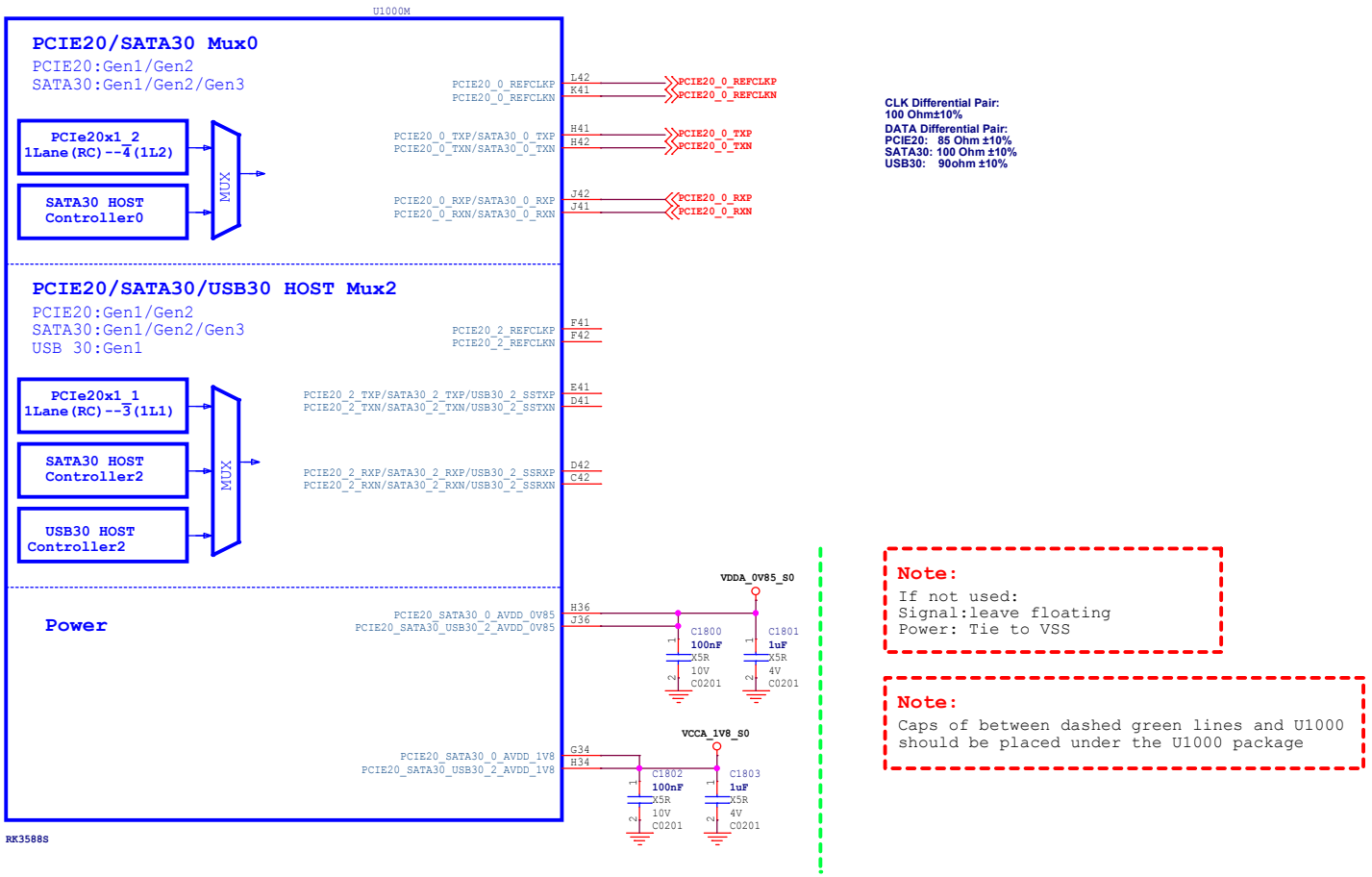
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	17.RK3588S_HDMI/eDP Interface				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	16 of 32

RK3588S(PCIE20/SATA30/USB30)



Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	18.RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 32

RK3588S(VCCIO4 Domain)

U1000H

VCCIO4 Domain
Operating Voltage=1.8V/3.3V

PCIE20X1_1_CLKREQN_M2 / SPDIF0_HPDIN_M2 / UART6_RX_M1 / SPI4_MISO_M2 / I2C2_SDA_M4 / GPIO1_A0_d
PCIE20X1_1_WAKEN_M2 / UART6_TX_M1 / SPI4_MOSI_M2 / I2C2_SCL_M4 / GPIO1_A1_d
PWM0_M2 / VOP_POST_EMPTY / UART6_RTSN_M1 / SPI4_CLK_M2 / I2C4_SDA_M3 / GPIO1_A2_d
PWM1_M2 / UART6_CTSN_M1 / SPI4_CS0_M2 / I2C4_SCL_M3 / GPIO1_A3_d
SPI2_MISO_M0 / GPIO1_A4_d
HDMI_TX0_HPD_M0 / SPI2_MOSI_M0 / GPIO1_A5_d
SPI2_CLK_M0 / GPIO1_A6_d
PWM3_IR_M3 / PCIE20X1_1_PERSTN_M2 / SPI2_CS0_M0 / PDM1_SDI0_M1 / GPIO1_A7_u
SPI2_CS1_M0 / PDM1_SDI1_M1 / GPIO1_B0_u
SPI0_MISO_M2 / PDM1_SDI2_M1 / GPIO1_B1_d
UART4_RX_M2 / SPI0_MOSI_M2 / PDM1_SDI3_M1 / GPIO1_B2_d
SATA0_ACT_LED_M1 / UART4_TX_M2 / SPI0_CLK_M2 / PDM1_CLK1_M1 / GPIO1_B3_d
UART7_RX_M2 / SPI0_CS0_M2 / PDM1_CLK0_M1 / GPIO1_B4_u
UART7_TX_M2 / SPI0_CS1_M2 / GPIO1_B5_u
PWM13_M2 / SATA2_ACT_LED_M1 / MIPI_CAMERA1_CLK_M0 / UART1_TX_M1 / SPDIF0_TX_M0 / I2C5_SCL_M3 / GPIO1_B6_u
PWM14_M2 / MIPI_CAMERA3_CLK_M0 / UART1_RTSN_M1 / I2C8_SCL_M2 / GPIO1_D6_u
PWM15_IR_M3 / MIPI_CAMERA4_CLK_M0 / UART1_CTSN_M1 / I2C8_SDA_M2 / GPIO1_D7_u

G40 L40 D38 L39 G37 M40 D39 H38 H39 G39 M38 M37 M39 D40 L38 F37 L37 G38

I2C4_SDA_M3_TP
I2C4_SCL_M3_TP
MIPI_CAM1_PWREN_H
LCD_ENN_H
LCD_RESET_L
LCD_ENP_H
MIPI_CAM1_RST_L
TP_RST_L
TP_INT_L
I2C5_SCL_M3_CAM
I2C5_SDA_M3_CAM
I2C8_SCL_M2_CAM
I2C8_SDA_M2_CAM

VCC_1V8_S0
R1911 2.2K 5% R0201
R1916 2.2K 5% R0201
R1917 2.2K 5% R0201
R1922 2.2K 5% R0201
R1910 2.2K 5% R0201

G27 G28 VCCIO4_1V8_1 VCCIO4_1V8_2
C1902 100nF X5R 10V C0201
G31 VCCIO4
C1903 100nF X5R 10V C0201

RK3588S

RK3588S(VCCIO6 Domain)

U1000J

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

BT1120_D0 / CIF_D0 / I2S1_MCLK_M0 / UART9_RTSN_M1 / SPI0_MISO_M1 / PCIE20X1_1_CLKREQN_M1 / GPIO4_A0_d
BT1120_D1 / CIF_D1 / I2S1_SCLK_M0 / UART9_CTSN_M1 / SPI0_MOSI_M1 / PCIE20X1_1_WAKEN_M1 / GPIO4_A1_d
BT1120_D2 / CIF_D2 / I2S1_LRCK_M0 / SPI0_CLK_M1 / PCIE20X1_1_PERSTN_M1 / GPIO4_A2_d
BT1120_D3 / CIF_D3 / UART0_TX_M2 / GPIO4_A3_d
BT1120_D4 / CIF_D4 / UART0_RX_M2 / SPI2_MISO_M1 / I2C3_SCL_M2 / GPIO4_A4_d
BT1120_D5 / CIF_D5 / I2S1_SDI0_M0 / UART3_TX_M2 / SPI2_MOSI_M1 / I2C3_SDA_M2 / GPIO4_A5_d
BT1120_D6 / CIF_D6 / I2S1_SDI1_M0 / UART3_RX_M2 / SPI2_CLK_M1 / I2C5_SCL_M2 / GPIO4_A6_d
BT1120_D7 / CIF_D7 / I2S1_SDI2_M0 / SPI2_CS0_M1 / I2C5_SDA_M2 / GPIO4_A7_d
BT1120_CLKOUT / CIF_CLKIN / I2S1_SDI3_M0 / UART9_TX_M0 / SPI2_CS1_M1 / I2C6_SDA_M3 / GPIO4_B0_d
SPDIF1_TX_M1 / MIPI_CAMERA0_CLK_M0 / SATA2_ACT_LED_M0 / I2S1_SDO0_M0 / UART9_RX_M0 / SPI0_CS1_M1 / I2C6_SCL_M3 / GPIO4_B1_u
CAN1_RX_M1 / BT1120_D8 / CIF_HREF / PWM14_M1 / I2S1_SDO1_M0 / UART9_RTSN_M0 / SPI0_CS0_M1 / I2C7_SCL_M3 / PCIE20X1_1_BUTTON_RSTN / GPIO4_B2_u
CAN1_TX_M1 / BT1120_D9 / CIF_VSYNC / PWM15_IR_M1 / I2S1_SDO2_M0 / UART9_CTSN_M0 / I2C7_SDA_M3 / PCIE20X1_2_BUTTON_RSTN / GPIO4_B3_u
BT1120_D10 / CIF_CLKOUT / PWM11_IR_M1 / I2S1_SDO3_M0 / UART9_TX_M1 / DP0_HPDIN_M0 / SPDIF0_TX_M1 / GPIO4_B4_u
BT1120_D11 / PWM12_M1 / UART9_RX_M1 / SPI3_MISO_M1 / GPIO4_B5_d
BT1120_D12 / PWM13_M1 / SPI3_MOSI_M1 / I2C5_SCL_M1 / SATA0_ACT_LED_M0 / GPIO4_B6_d
BT1120_D13 / HDMI_TX0_SCL_M0 / SPI3_CLK_M1 / I2C5_SDA_M1 / PCIE20X1_2_CLKREQN_M1 / GPIO4_B7_u
BT1120_D14 / HDMI_TX0_SDA_M0 / SPI3_CS0_M1 / I2C8_SCL_M3 / PCIE20X1_2_WAKEN_M1 / GPIO4_C0_u
BT1120_D15 / SPDIF1_TX_M2 / PWM6_M1 / HDMI_TX0_CEC_M0 / SPI3_CS1_M1 / I2C8_SDA_M3 / PCIE20X1_2_PERSTN_M1 / GPIO4_C1_d

AV19 AW18 AV26 AV19 AW19 AU15 AV18 AW26 AW27 AU22 AT15 AV23 AV27 AU23 AW22 AV22 AW23 AV26

TYPEC0_SBU1_DC
TYPEC0_SBU2_DC
LCD_PWREN_H
BQ_OTG_EN_H
I2C6_SDA_M3
I2C6_SCL_M3
LCD_BL_PWM14_M1

Note:
BT1120 Only Support Output

VCC_1V8_S0
VCCIO6_1V8 AJ34
C1906 100nF X5R 10V C0201
VCC_3V3_S0
VCCIO6_1 AL33 AM33
C1907 100nF X5R 10V C0201

RK3588S

RK3588S(VCCIO5 Domain)

U1000I

VCCIO5 Domain
Operating Voltage=1.8V/3.3V

PWM10_M0 / SPI4_MISO_M1 / I2C4_SDA_M4 / GMAC1_TXD2 / I2S3_MCLK / FSPI_D0_M2 / SDIO_D0_M1 / GPIO3_A0_u
AUDDSM_LN / PWM11_IR_M0 / SPI4_MOSI_M1 / I2C4_SCL_M4 / GMAC1_TXD3 / I2S3_SCLK / FSPI_D1_M2 / SDIO_D1_M1 / GPIO3_A1_u
AUDDSM_LP / UART8_TX_M1 / SPI4_CLK_M1 / GMAC1_RXD2 / I2S3_LRCK / FSPI_D2_M2 / SDIO_D2_M1 / GPIO3_A2_u
AUDDSM_RN / UART8_RX_M1 / SPI4_CS0_M1 / GMAC1_RXD3 / I2S3_SDO / FSPI_D3_M2 / SDIO_D3_M1 / GPIO3_A3_u
AUDDSM_RP / UART8_RTSN_M1 / SPI4_CS1_M1 / GMAC1_TXCLK / I2S3_SDI / SDIO_CMD_M1 / GPIO3_A4_d
UART8_CTSN_M1 / I2C4_SDA_M0 / GMAC1_RXCLK / FSPI_CLK_M2 / MIPI_CAMERA0_CLK_M1 / SDIO_CLK_M1 / GPIO3_A5_d
I2C4_SCL_M0 / ETH1_REFCLKO_25M / MIPI_CAMERA3_CLK_M1 / GPIO3_A6_d
GMAC1_RXD0 / MIPI_CAMERA2_CLK_M1 / PWM8_M0 / GPIO3_A7_u
GMAC1_RXD1 / MIPI_CAMERA3_CLK_M1 / PWM9_M0 / GPIO3_B0_u
UART2_TX_M2 / GMAC1_RXDV_CRS / MIPI_CAMERA4_CLK_M1 / PWM2_M1 / GPIO3_B1_d
UART2_RX_M2 / GMAC1_TXER / I2S2_SDI_M1 / PWM3_IR_M1 / GPIO3_B2_d
UART2_RTSN / GMAC1_TXD0 / I2S2_SDO_M1 / GPIO3_B3_u
UART2_CTSN / GMAC1_TXD1 / I2S2_MCLK_M1 / GPIO3_B4_u
UART3_TX_M1 / CAN1_RX_M0 / GMAC1_TXEN / I2S2_SCLK_M1 / PWM12_M0 / GPIO3_B5_u
UART3_RX_M1 / CAN1_TX_M0 / GMAC1_MCLKINOUT / I2S2_LRCK_M1 / PWM13_M0 / GPIO3_B6_d
SPI1_MOSI_M1 / I2C3_SCL_M1 / GMAC1_PTP_REF_CLK / GPIO3_B7_d
UART7_TX_M1 / SPI1_MISO_M1 / I2C3_SDA_M1 / GMAC1_PPSTRIG / GPIO3_C0_d
UART7_RX_M1 / SPI1_CLK_M1 / GMAC1_PPSCLK / GPIO3_C1_d
UART7_RTSN_M1 / SPI1_CS0_M1 / I2C8_SCL_M4 / GMAC1_MDC / MIPI_TE0 / PWM14_M0 / GPIO3_C2_d
UART7_CTSN_M1 / SPI1_CS1_M1 / I2C8_SDA_M4 / GMAC1_MDIO / MIPI_TE1 / PWM15_IR_M0 / GPIO3_C3_d
UART5_TX_M1 / SPI3_CS0_M3 / CAN2_RX_M0 / CIF_D8 / FSPI_CS0N_M2 / GPIO3_C4_u
UART5_RX_M1 / SPI3_CS1_M3 / CAN2_TX_M0 / CIF_D9 / FSPI_CS1N_M2 / GPIO3_C5_u
SPI3_MISO_M3 / CIF_D10 / GPIO3_C6_u
SPI3_MOSI_M3 / I2C5_SCL_M0 / CIF_D11 / PCIE20X1_2_CLKREQN_M0 / HDMI_TX0_SCL_M2 / GPIO3_C7_u
UART4_RX_M1 / SPI3_CLK_M3 / I2C5_SDA_M0 / CIF_D12 / PCIE20X1_2_WAKEN_M0 / HDMI_TX0_SDA_M2 / PWM8_M2 / GPIO3_D0_u
UART4_TX_M1 / SPI0_MISO_M3 / CIF_D13 / PCIE20X1_2_PERSTN_M0 / PWM9_M2 / GPIO3_D1_d
UART9_RTSN_M2 / SPI0_MOSI_M3 / I2C7_SCL_M2 / CIF_D14 / GPIO3_D2_d
UART9_CTSN_M2 / SPI0_CLK_M3 / I2C7_SDA_M2 / CIF_D15 / PWM10_M2 / GPIO3_D3_d
UART9_RX_M2 / SPI0_CS0_M3 / MCU_JTAG_TCK_M1 / HDMI_TX0_HPD_M1 / GPIO3_D4_d
UART9_TX_M2 / SPI0_CS1_M3 / MCU_JTAG_TMS_M1 / PWM11_IR_M3 / GPIO3_D5_d

AR38 AR37 AT38 AT40 AT39 AV38 AV37 AT37 AR39 AV39 AN34 AM35 AV35 AV35 AT37 AV34 AR36 AN38 AV40 AM39 AU34 AV34 AV30 AU30 AM31 AV27 AV30 AV31 AV31 AM30 AF35 AF36 AC33 AC34

MIPI_CAM1_CLKOUT
MIPI_CAM3_CLKOUT
FLASH_LED_EN
I2S2_SDI_M1_BT
I2S2_SDO_M1_BT
RGB_INT_L
I2S2_SCLK_M1_BT
I2S2_LRCK_M1_BT
I2C3_SCL_M1_Sensor
I2C3_SDA_M1_Sensor
MIPI_TE0
CHG_INT_L
MIPI_CAM3_RST_L
MIPI_CAM3_PWREN_H
MIPI_CAM3_PDN_L
PCIE20x1_2_CLKREQn_M0
PCIE20x1_2_WAKEn_M0
PCIE20x1_2_PERSTn_M0
UART9_RTSN_M2_BT
UART9_CTSN_M2_BT
UART9_RX_M2_BT
UART9_TX_M2_BT

RESERVED
VCCIO5_1V8
VCCIO5_1 VCCIO5_2
VCC_1V8_S0
C1904 100nF X5R 10V C0201
C1905 100nF X5R 10V C0201

VCC_1V8_S0
R1904 2.2K 5% R0201
R1905 2.2K 5% R0201
I2C3_SCL_M1_Sensor
I2C3_SDA_M1_Sensor

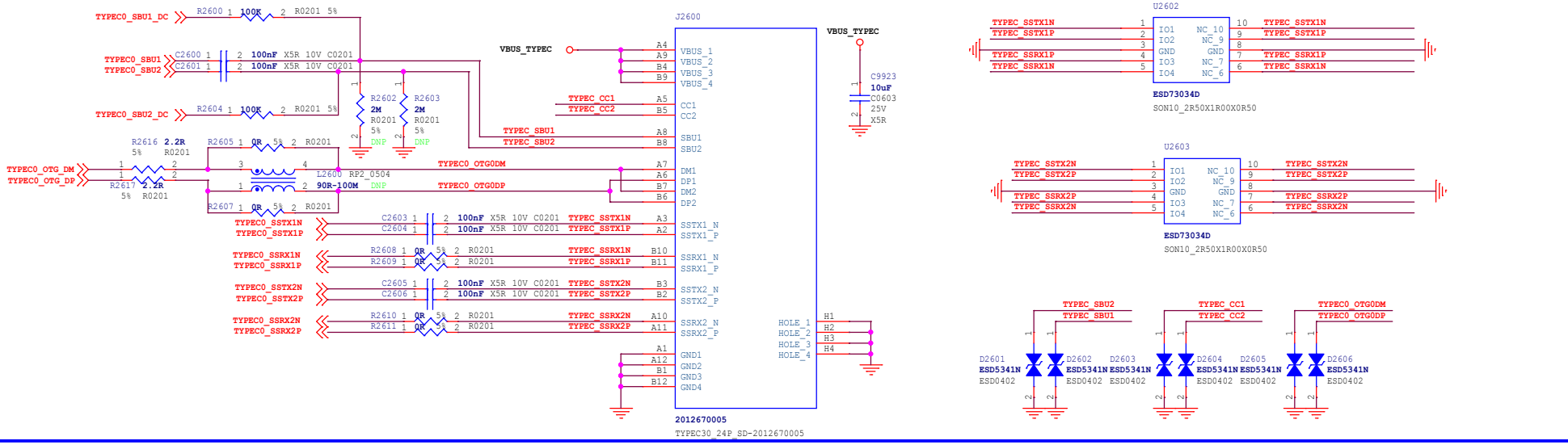
RK3588S

VCC_3V3_S0
R1914 2.2K 5% R0201
R1915 2.2K 5% R0201
I2C6_SCL_M3
I2C6_SDA_M3

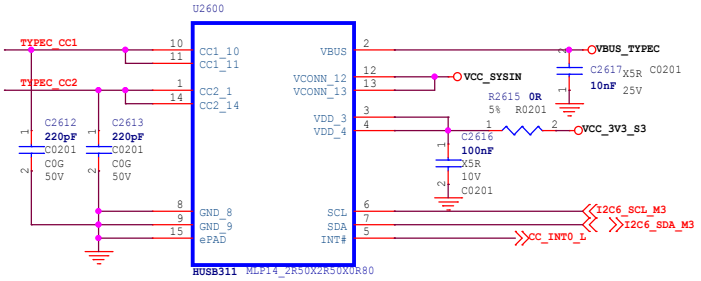
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Demo		
File:	19.RK3588S GPIO		
Date:	Friday, January 07, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet 18 of 32

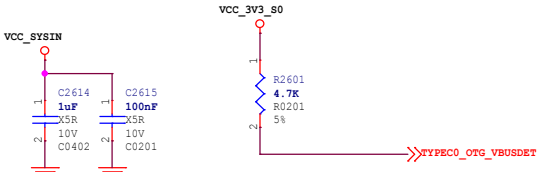
USB Type-C Port



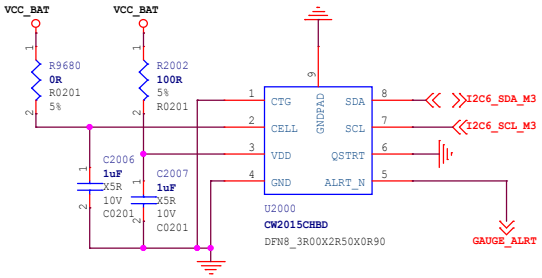
USB Type-C CC CTRL



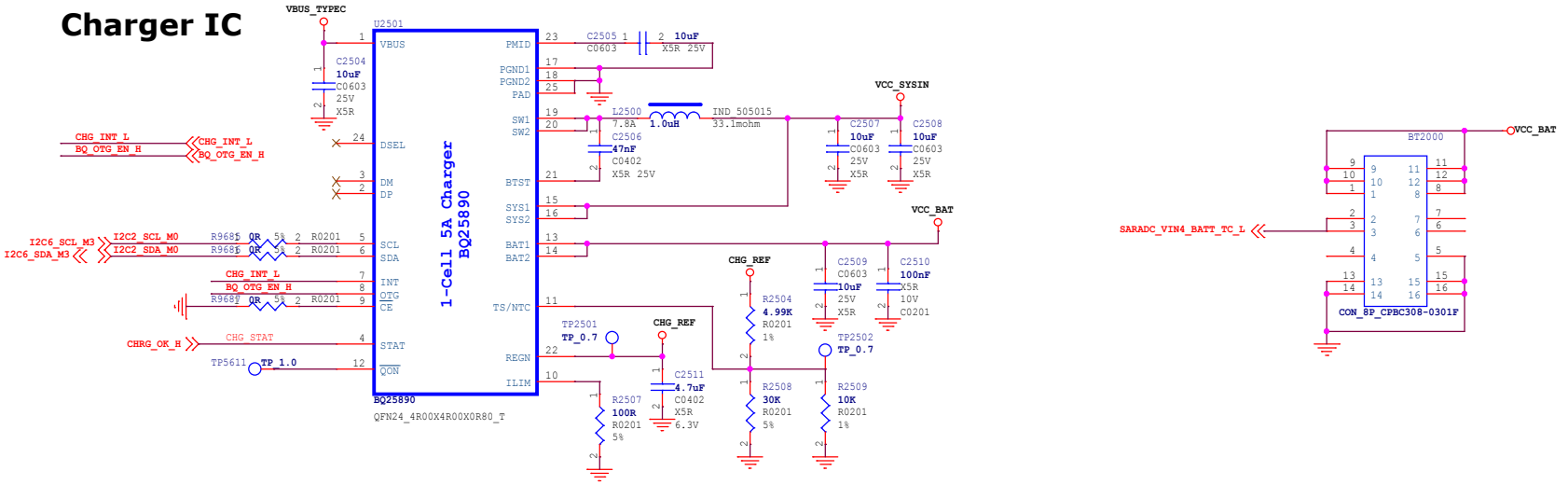
USB Detection



Gas Gauge



Charger IC



Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	20.Power_1Cell_QC				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	19 of 32

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1
VSEL4
VSEL5
PMIC_INT_L
PWRON_L
PMIC_RESET_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI

VCC_SYSIN
D2200 AZ5825-01F ESD0402

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

VSEL5 — R2242 0R — R0201 5% — PMIC_PWR_CTRL2 — R2244 DNP 120K R0201

VSEL4 — R2290 0R — R0201 5% — PMIC_PWR_CTRL3 — R2291 DNP 120K R0201

PMIC RK806-1 BUCK

U2200A

BUCK5 2.5A — BUCK1 6.5A
BUCK6 2.5A — BUCK2 5A
BUCK9 2.5A — BUCK3 5A
BUCK8 2.5A — BUCK4 5A
BUCK10 2.5A — BUCK7 2.5A

RK806-1

VDD_DDR_S0 — Default:0.85V Low frequency: 0.85V-->0.75V — C2200 22uF X5R 10V C0603 — C2202 22uF X5R 10V C0603 — C2203 22uF X5R 10V C0603 — R2200 100R 5% R0201 — C9922 1uF X5R 6.3V C0201 — L2200 0.47uH IND_201610 — PMIC_SW5 — PMIC_VOUT5 — PMIC_FB5 (FB=0.5V) — Feedback from RK3588S

VDD_GPU_S0 — C2201 22uF 10V X5R C0603 — L2201 0.22uH IND_404020 — PMIC_SW1 — PMIC_VOUT1 — C2209 1uF X5R 6.3V C0201 — R2208 100R 5% R0201 — C2210 22uF X5R 10V C0603 — C2205 22uF X5R 10V C0603 — C2280 22uF X5R 10V C0603 — Feedback from RK3588S — (FB=0.5V) FB1

VDD2_DDR_S3 — C2214 22uF X5R 10V C0603 — C2215 22uF X5R 10V C0603 — C2216 100pF X5R 25V C0201 — L2202 0.47uH IND_201610 — PMIC_SW6 — PMIC_VOUT6 — PMIC_FB6 (FB=0.5V) — R2218 120K 1% R0201 — R2227 100K 1% R0201

LPDDR4/4x=1.1V	120K	
LPDDR5=1.05V	110K	

VDD_CPU_LIT_S0 — C2213 22uF 10V X5R C0603 — L2203 0.24uH IND_252012 — PMIC_SW2 — PMIC_VOUT2 — C2221 1uF X5R 6.3V C0201 — R2219 100R 5% R0201 — C2217 22uF X5R 10V C0603 — C2218 22uF X5R 10V C0603 — C2281 22uF X5R 10V C0603 — Feedback from RK3588S — (FB=0.5V) FB2

VDDQ_DDR_S0 — C2225 10uF X5R 10V C0603 — C2228 22uF X5R 10V C0603 — C2227 22uF X5R 10V C0603 — C2229 100pF X5R 25V C0201 — L2204 0.47uH IND_201610 — PMIC_SW9 — PMIC_VOUT9 — PMIC_FB9 (FB=0.5V) — R2236 20K 1% R0201 — R2241 100K 1% R0201

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VDD_LOGIC_S0 — C2226 22uF 10V X5R C0603 — L2205 0.24uH IND_252012 — PMIC_SW3 — C2230 1uF X5R 6.3V C0201 — R2238 100R 5% R0201 — C2231 22uF X5R 10V C0603 — C2232 22uF X5R 10V C0603 — C2282 22uF X5R 10V C0603 — Feedback from RK3588S

VCC_3V3_S3 — C2238 22uF X5R 10V C0603 — C2239 22uF X5R 10V C0603 — L2206 0.47uH IND_201610 — PMIC_SW8 — PMIC_VOUT8

VDD_VDENC_S0 — C2236 22uF 10V X5R C0603 — L2207 0.24uH IND_252012 — PMIC_SW4 — C2291 1uF X5R 6.3V C0201 — R2209 100R 5% R0201 — C2240 22uF X5R 10V C0603 — C2237 22uF X5R 10V C0603 — C2283 22uF X5R 10V C0603 — Feedback from RK3588

VCC1V8_PMU_DDR_S3 — VCC_1V8_S3_PLDO6 — R2210 0R R0402 5% DNP — R2211 0R R0402 5% — Default:1.8V — VCC_1V8_S3 — C2241 22uF X5R 10V C0603 — C2242 22uF X5R 10V C0603 — C2243 22uF X5R 10V C0603 — L2208 0.47uH IND_201610 — PMIC_SW10 — PMIC_VOUT10

VCC_2V0_PLDO_S3 — C2244 22uF X5R 10V C0603 — C2245 22uF X5R 10V C0603 — L2209 0.47uH IND_201610 — PMIC_SW7 — PMIC_VOUT7

PMIC RK806-1 Managerment

VCC_1V8_S3_PLDO6 — C2248 1uF 6.3V X5R C0201 — U2200C

VCCIO — (IIC/SPI)CS — (SDA)MOSI — (SCL)CLK — (PWRCTRL3)SO — PWRCTRL2 — PWRCTRL1 — PMIC_SPI_CS — PMIC_SPI_MOSI — PMIC_SPI_CLK — PMIC_PWR_CTRL3 — PMIC_PWR_CTRL2 — SLEEP1_RESET1_DEVOFF1_VSEL1 — R2258 100K 5% R0201

VCCA — SYNC_CLK — SYNC — VDC — PWRON — (M/S)EXT_EN — INT — RESETB — ePAD — PMIC_EXT_EN_OUT — PMIC_INT_L — PMIC_RESET_L — R2261 10K 5% R0201 — R2263 10K 5% R0201 — R2262 100nF X5R 10V C0201

VCC_SYSIN — C2254 1uF X5R 10V C0402

VCC_1V8_S3

VBUS_TYPEC — R2264 39K 1% R0201 — PMIC_VDC — R2265 10K 1% R0201 — D2600 DNP BAT752C3V0 SOD_123 — C2260 1nF C0201 X5R 25V — PWRON_L — C2261 100nF X5R 10V C0201

RK806-1

RK3588S nPOR — TSADC_SHUT — RK806-1 RESETB — Reset Key

Note:

- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

VCC_2V0_PLDO_S3 — C2247 1uF X5R 6.3V C0201 — VCC11 — PLDO1 0.5A — VCC_1V8_S0 — C2246 1uF 6.3VC0201 X5R — Default:1.8V

PLDO2 0.3A — VCCA_1V8_S0 — C2249 1uF 6.3VC0201 X5R — Default:1.8V

PLDO3 0.3A — VDDA_1V2_S0 — C2250 1uF 6.3VC0201 X5R — Default:1.2V

VCC_SYSIN — C2252 1uF X5R 10V C0402 — VCC12 — PLDO4 0.5A — VCCA_3V3_S0 — C2251 1uF 6.3VC0201 X5R — Default:3.3V

PLDO5 0.3A — VCCIO_SD_S0 — C2253 1uF 6.3VC0201 X5R — Default:3.3V

PLDO

VCC_1V1_NLDO_S3 — C2257 1uF X5R 6.3V C0201 — VCC13 — NLDO1 0.3A — VDD_0V75_S3 — C2255 2.2uF 6.3VC0402 X5R — Default:0.75V

NLDO2 0.3A — VDDA_DDR_PLL_S0 — C2258 2.2uF 6.3VC0402 X5R — Default:0.85V; Low frequency:0.85V-->0.75V

NLDO3 0.5A — VDDA_0V75_S0 — C2259 2.2uF 6.3VC0402 X5R — Default:0.75V

VCC_1V1_NLDO_S3 — C2264 1uF X5R 6.3V C0201 — VCC14 — NLDO4 0.5A — VDDA_0V85_S0 — C2263 2.2uF 6.3VC0402 X5R — Default:0.85V

NLDO5 0.3A — C2265 2.2uF 6.3VC0402 X5R — Default:0.75V Reserved

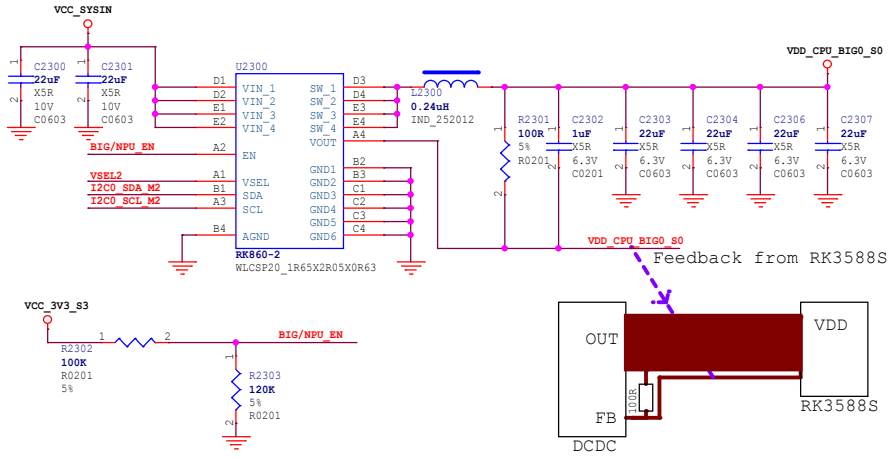
NLDO

RK806-1

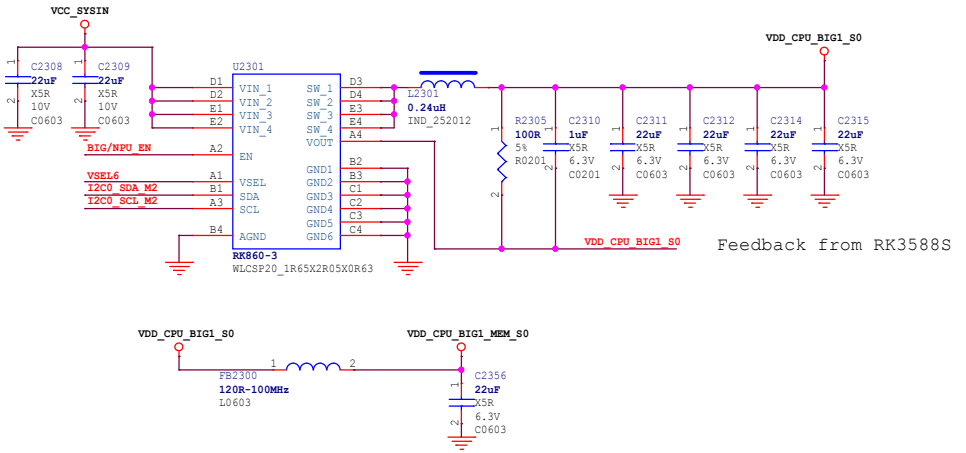
VCCA_1V8_S0 — AVDD1V8_DDR_PLL_S0 — C2290 1uF X5R 6.3V C0201

Rockchip Electronics Co., Ltd			
Project:	RK3588S_Demo		
File:	22.Power-PMIC_RK806-1		
Date:	Wednesday, February 23, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	20 of 32

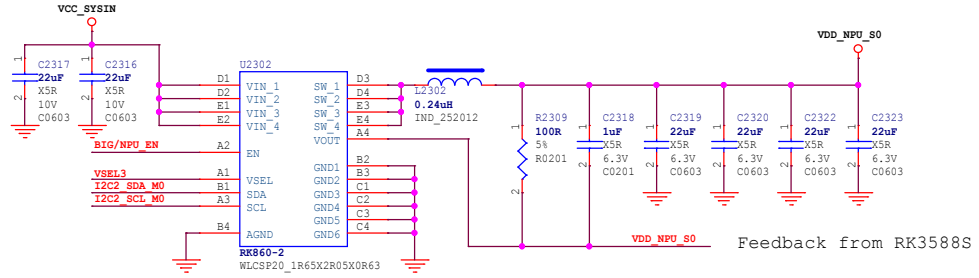
VDD_CPU_BIG0



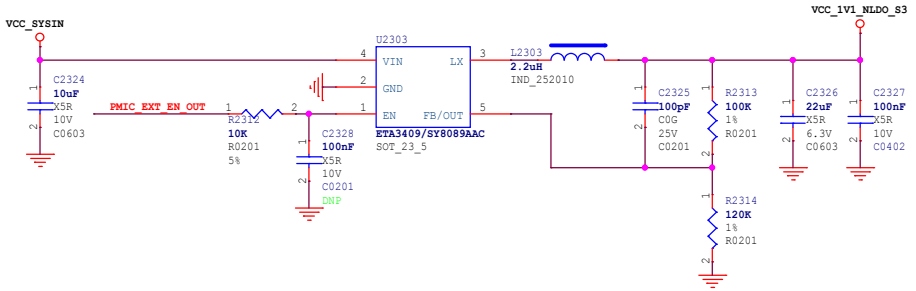
VDD_CPU_BIG1



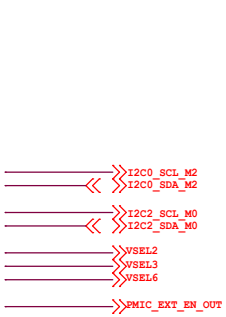
VDD_NPU

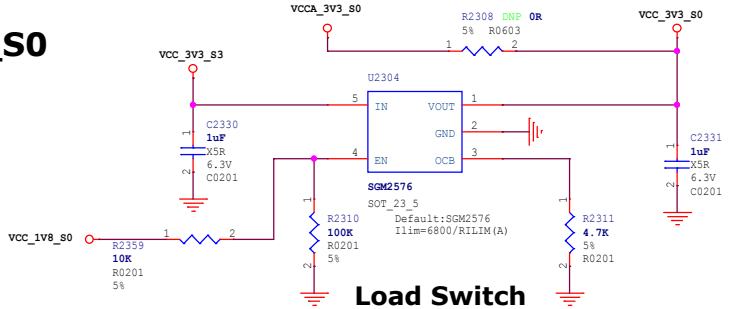


VCC_1V1_NLDO



VCC_3V3_S0





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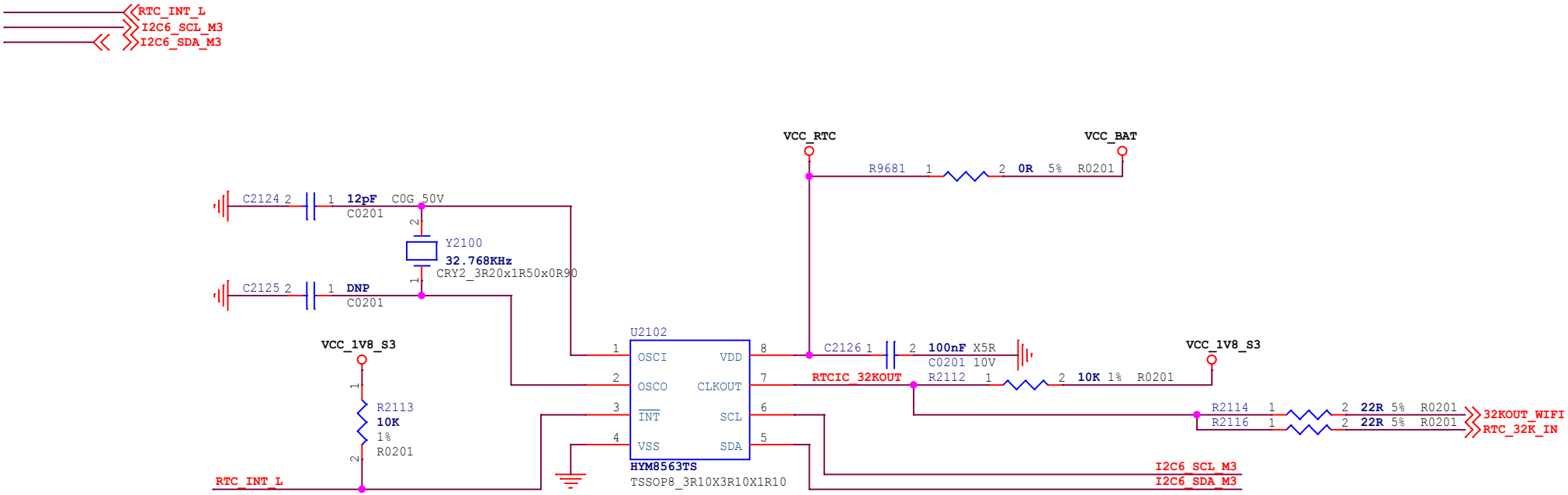
Rockchip Electronics Co., Ltd

Project:	RK3588S_Demo				
File:	23.Power_Ext Discrete				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	21 of 32

RTC IC



Address:Read A3H,Write A2H

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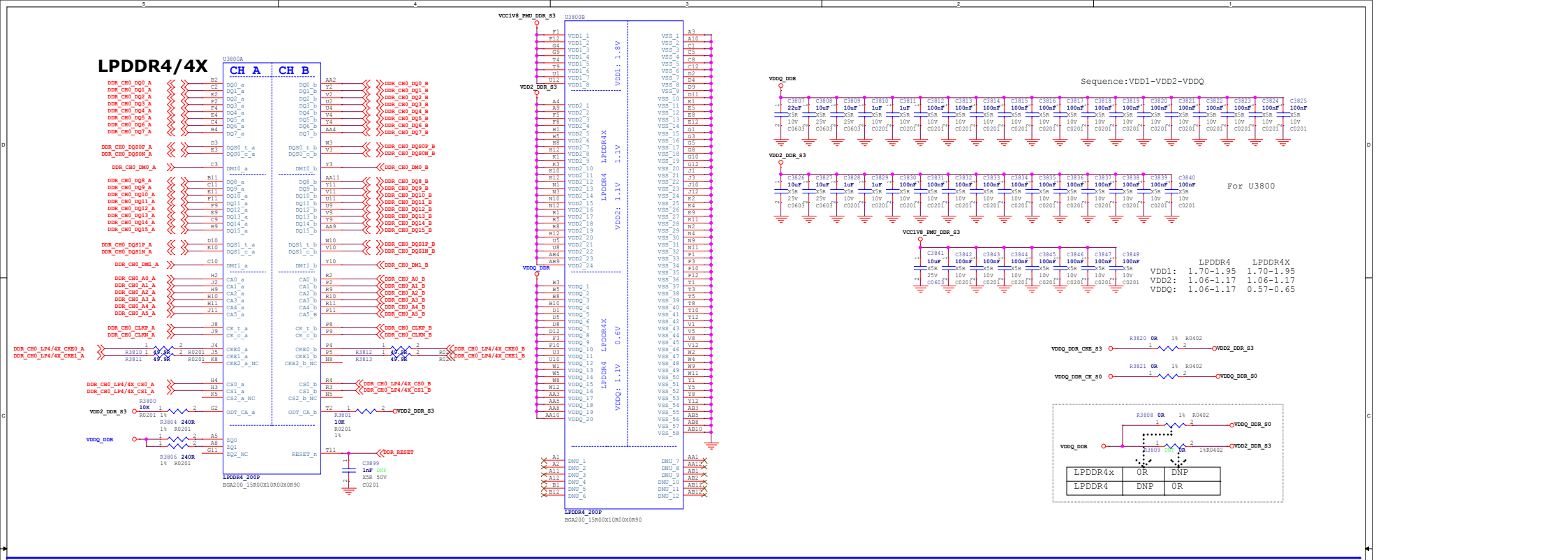
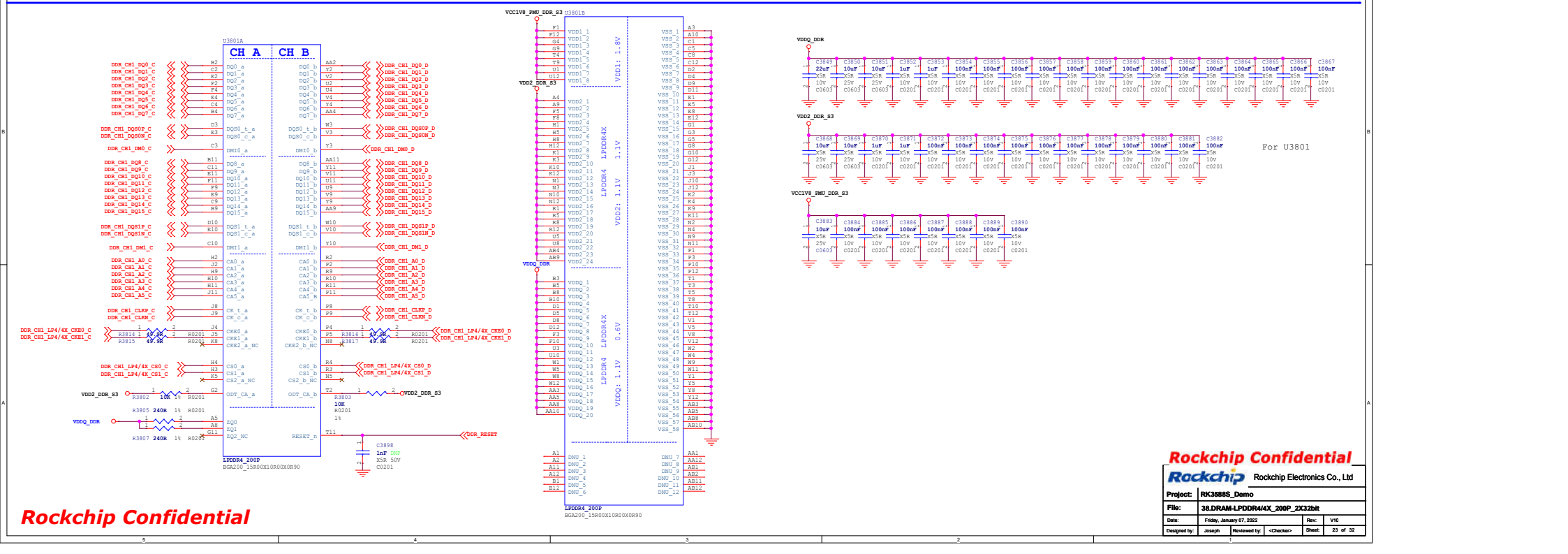
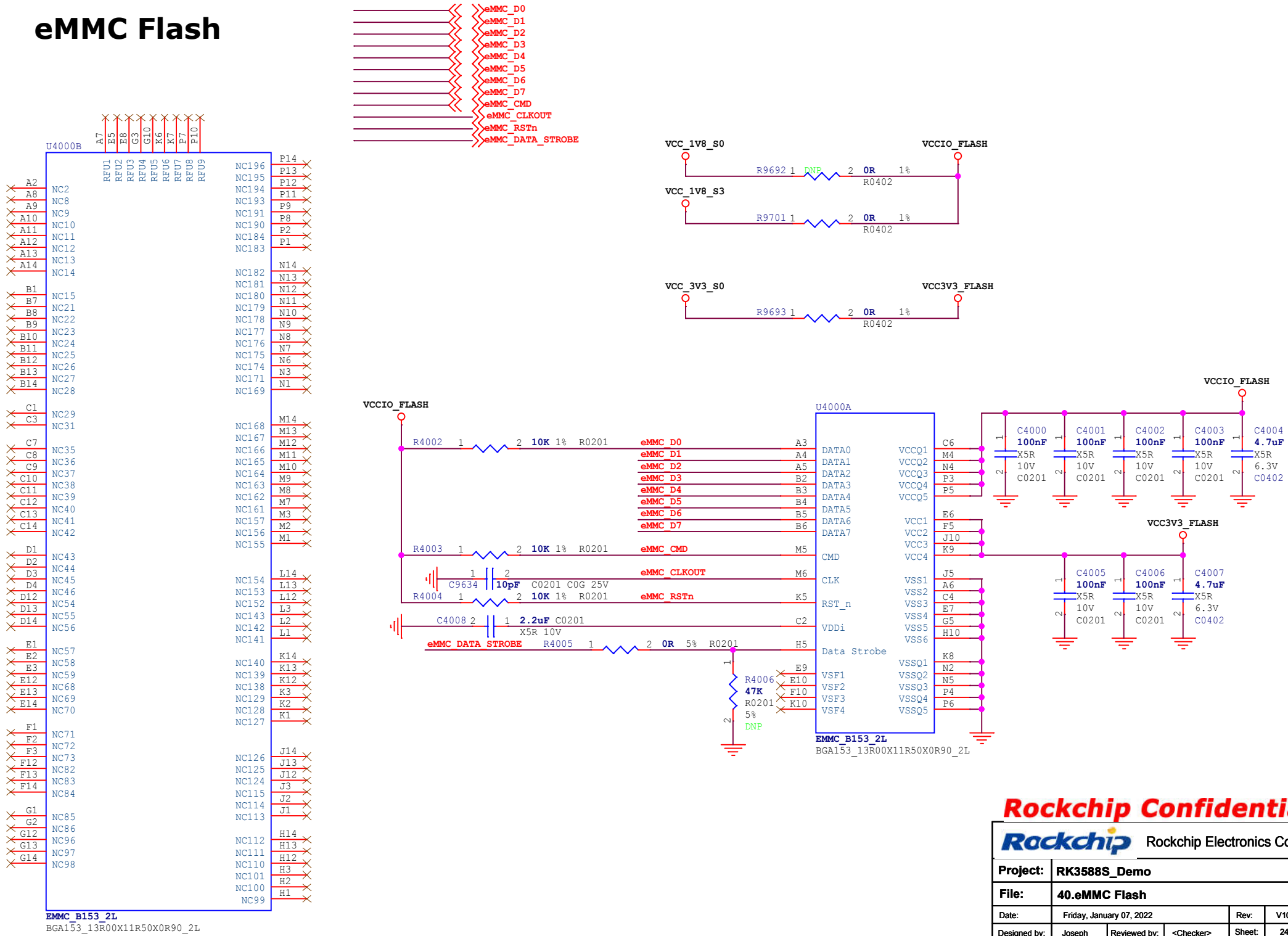
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	24.RTC				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	22 of 32





Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Demo
File:	38.DRAM-LPDDR4/4X_200P_2X32bit
Date:	Friday, January 07, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	23 of 32

eMMC Flash



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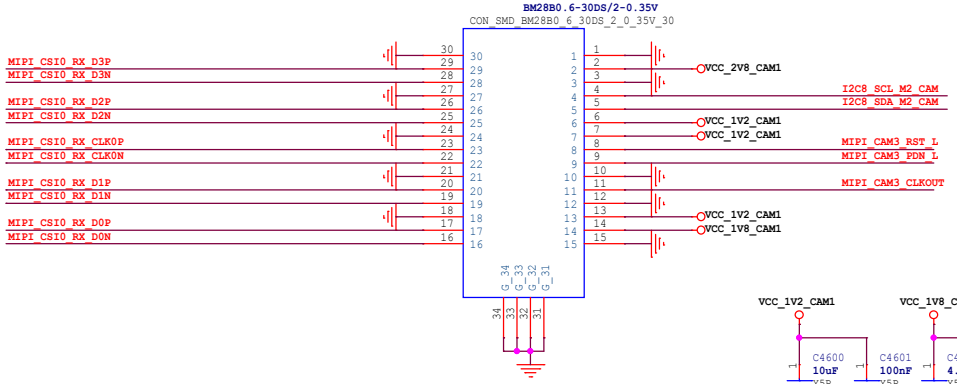
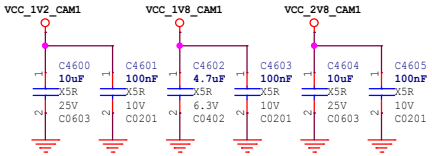
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	40.eMMC Flash				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	24 of 32

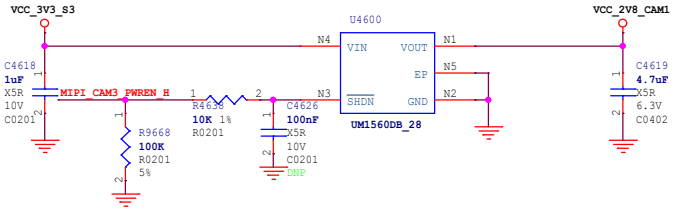
MIPI-CSI0_RX

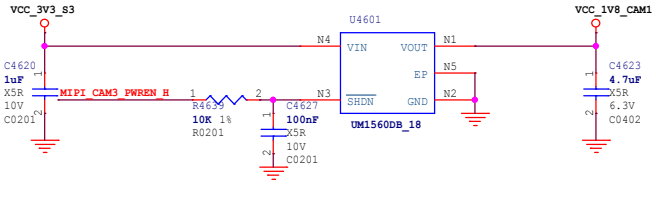
MIPI_CSI0_RX_D0P
MIPI_CSI0_RX_D0N
MIPI_CSI0_RX_D1P
MIPI_CSI0_RX_D1N
MIPI_CSI0_RX_D2P
MIPI_CSI0_RX_D2N
MIPI_CSI0_RX_D3P
MIPI_CSI0_RX_D3N
MIPI_CSI0_RX_CLK0P
MIPI_CSI0_RX_CLK0N
MIPI_CAM3_CLKOUT
MIPI_CAM3_RST_L
MIPI_CAM3_PWREN_H
MIPI_CAM3_PDN_L
I2C8_SCL_M2_CAM
I2C8_SDA_M2_CAM

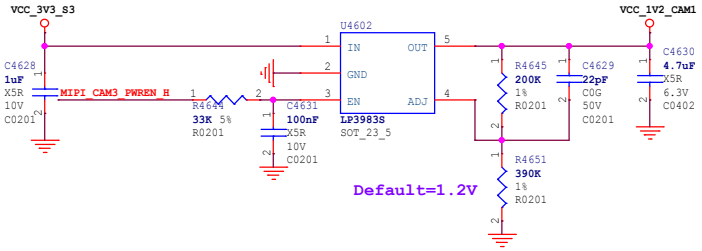
前摄：OV16A10-GA5A-Z









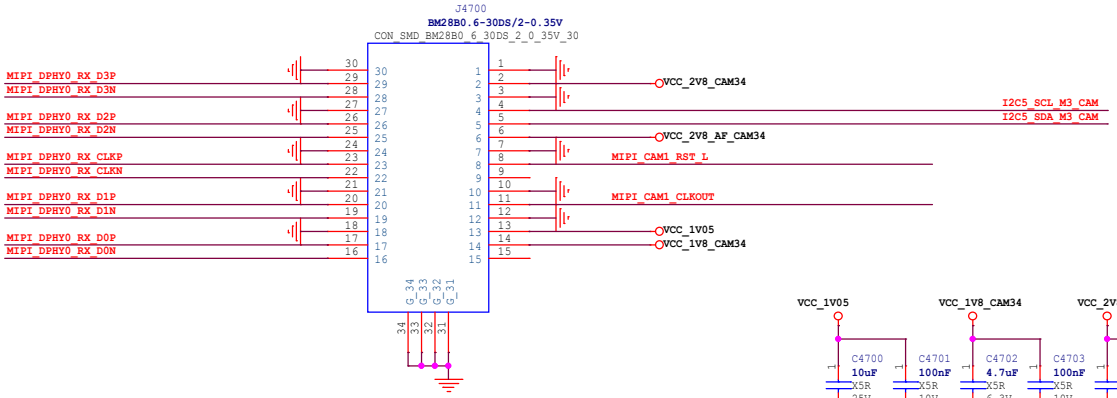


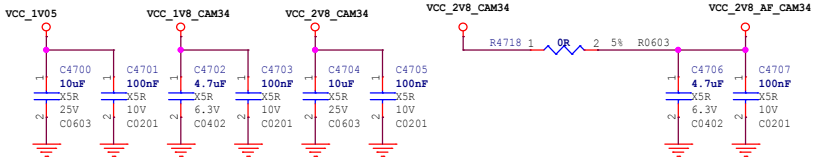
Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	46.VI-Camera MIPI CSI0-RX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	25 of 32

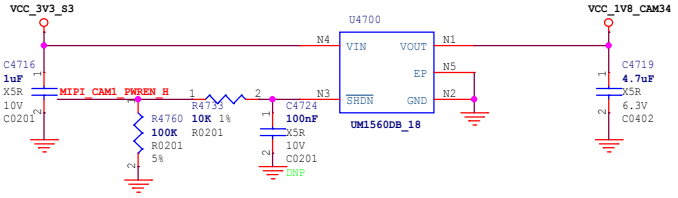
VI-Camera DPHY_RX

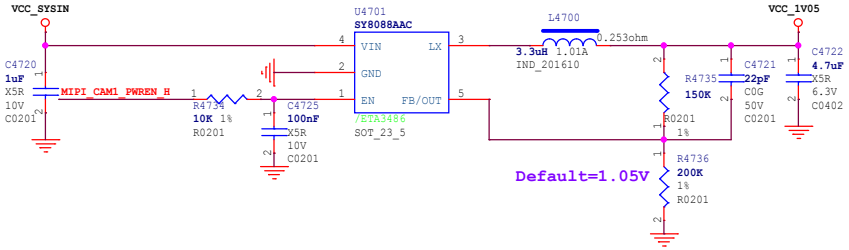
MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N
MIPI_CAM1_CLKOUT
MIPI_CAM1_PWREN_H
MIPI_CAM1_RST_L
I2C5_SCL_M3_CAM
I2C5_SDA_M3_CAM

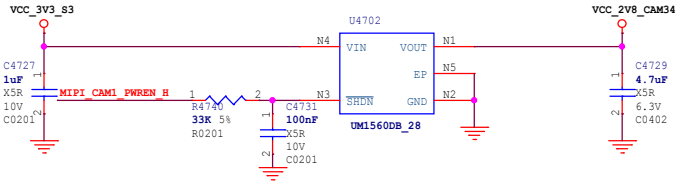
后摄：S5K3L6XX03-FGX9











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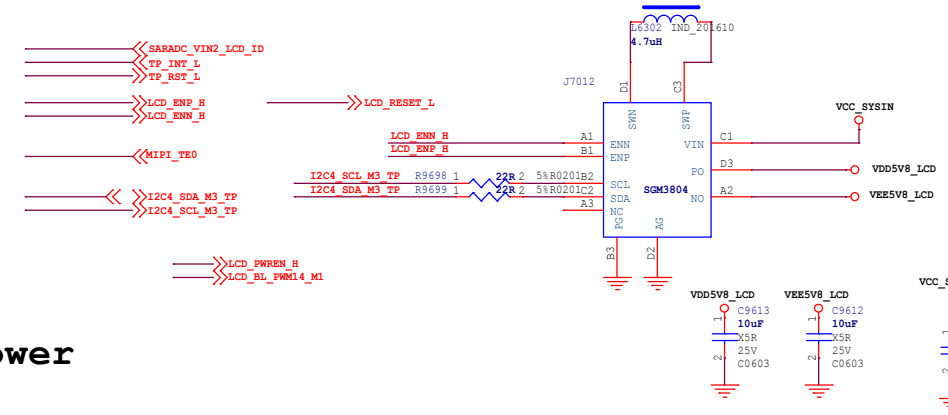
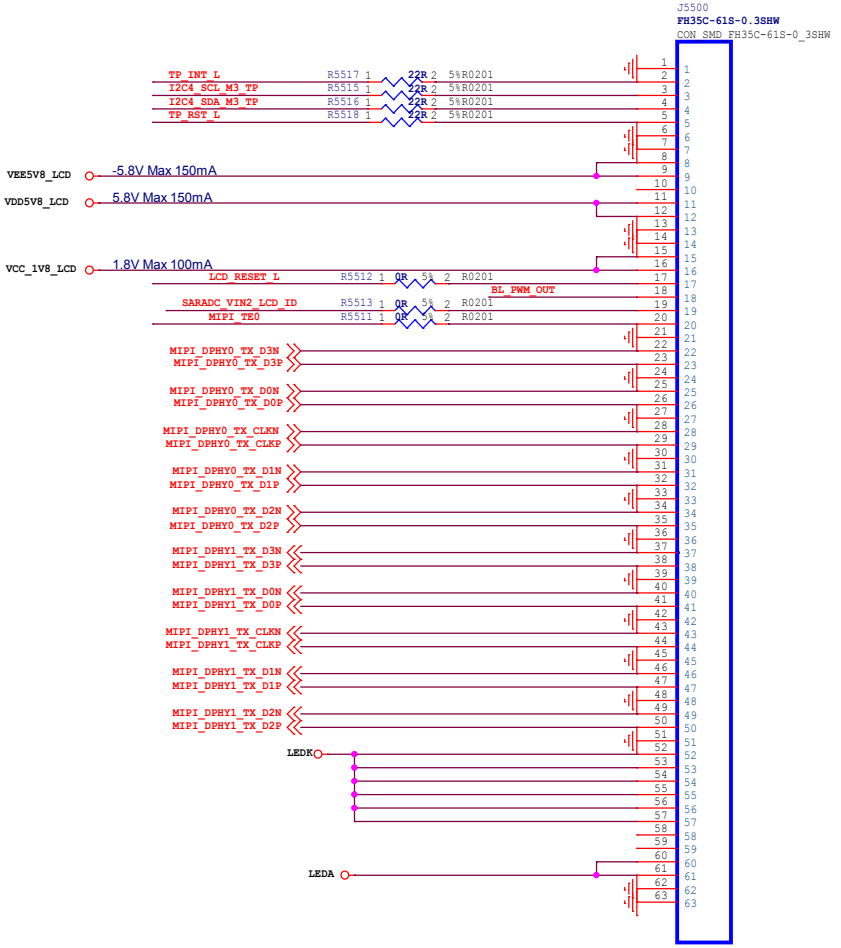
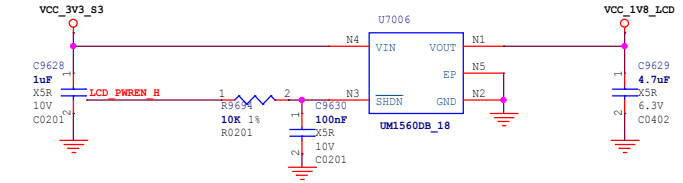
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	47.VI-Camera_MIPI-DPHY-RX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	26 of 32

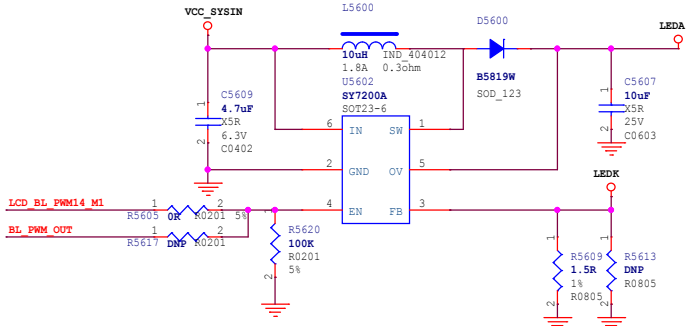
MIPI DPHY TX

Power



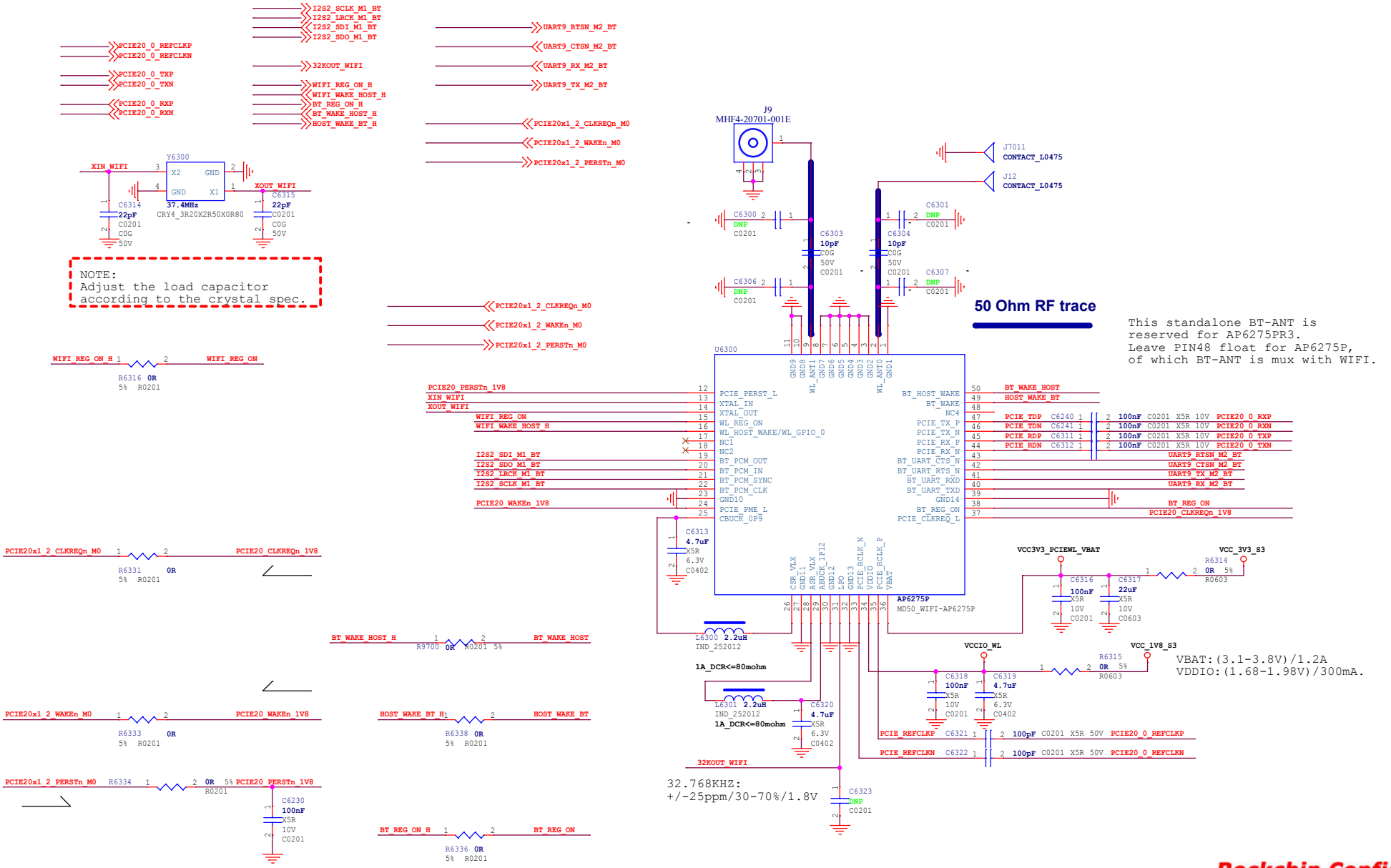






Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	55.VO-MIPI DPHY-TX				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	27 of 32

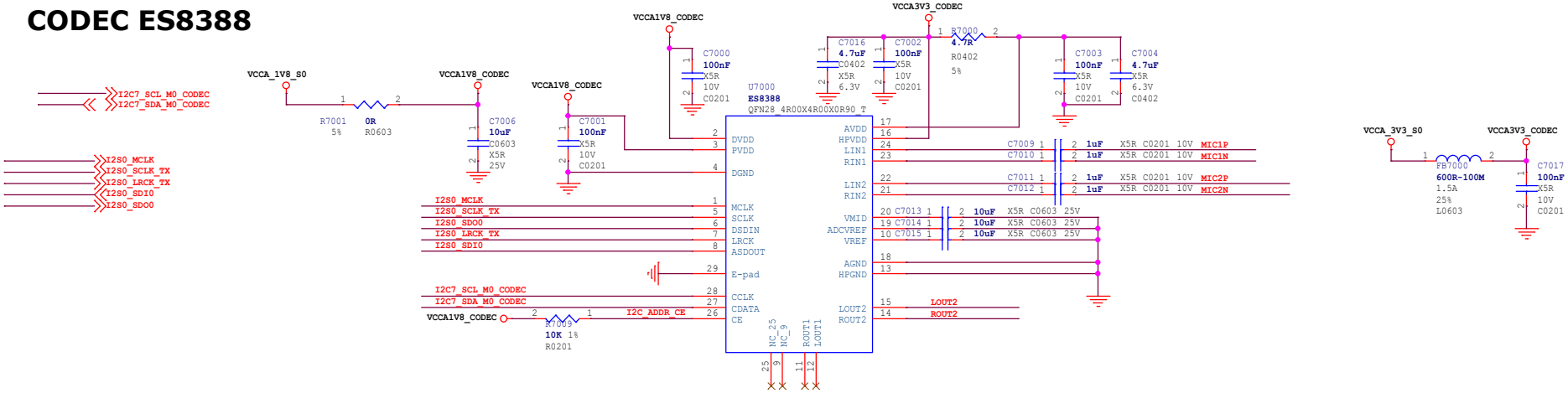
PCIe WIFI6/BT Module-2T2R



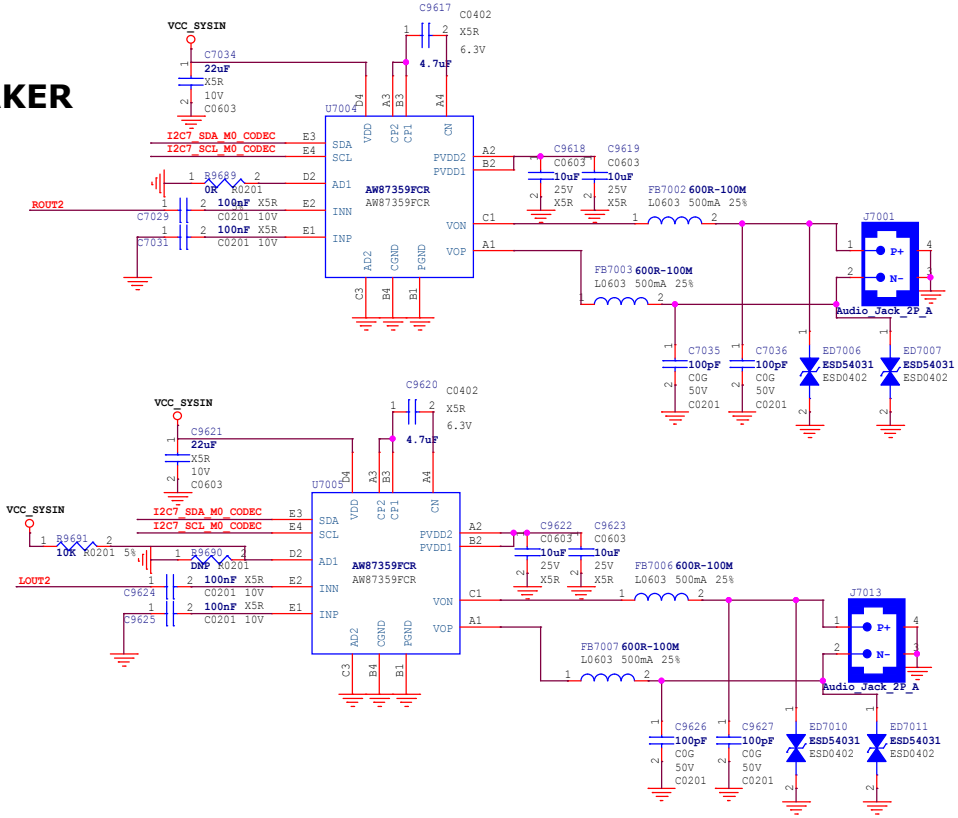
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	63.WIFI/BT-PCIe_2T2R(AP6275PR3)				
Date:	Monday, January 24, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	28 of 32

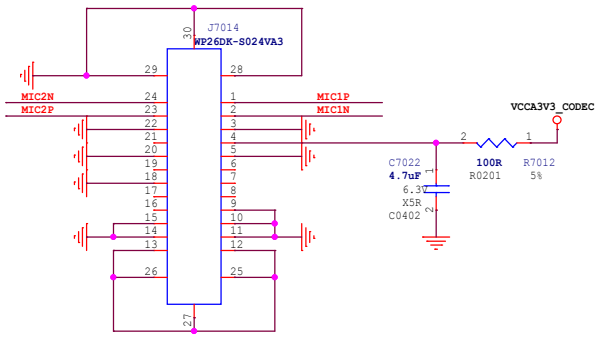
CODEC ES8388



SPEAKER



Analog MIC



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Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	70.Audio Codec-ES8388				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	29 of 32

Sensor

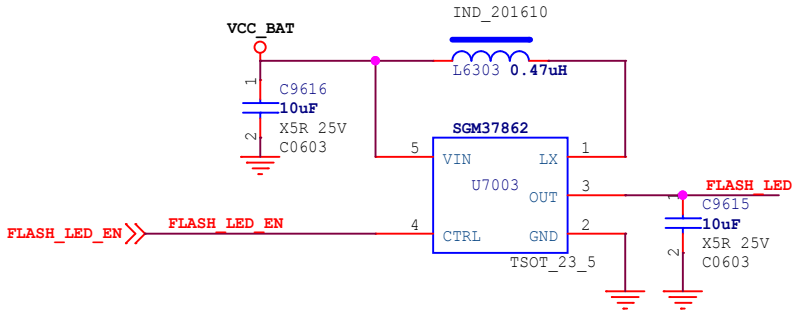
I2C3_SCL_M1_Sensor
I2C3_SDA_M1_Sensor
RGB_INT_L
ALPS_INT_L

I2C3_SCL_M1_Sensor — I2C_SCL_SENSOR

I2C3_SDA_M1_Sensor — I2C_SDA_SENSOR

VCC_1V8_S0
I2C_SCL_SENSOR
I2C_SDA_SENSOR
RGB_INT_L

J7006 CONTACT_L0475
J7007 CONTACT_L0475
J7008 CONTACT_L0475
J7009 CONTACT_L0475
J7010 CONTACT_L0475



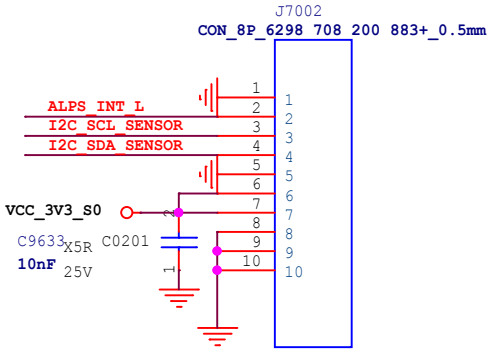
MAX:1.5A

FLASH_LED — J1 CONTACT_L0475

J3 CONTACT_L0475

Flashlight

PLS+ALS



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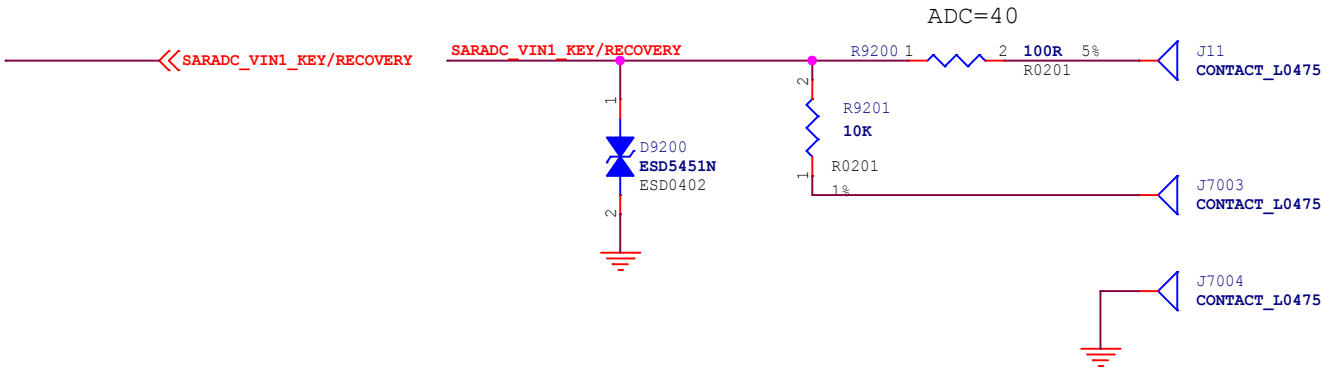
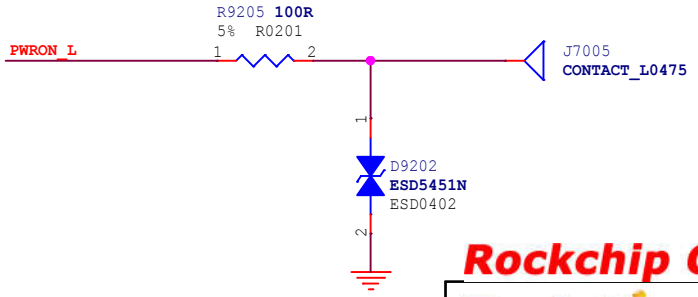
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Demo				
File:	90.Sensor				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	30 of 32

KEY Array



Reset_Key

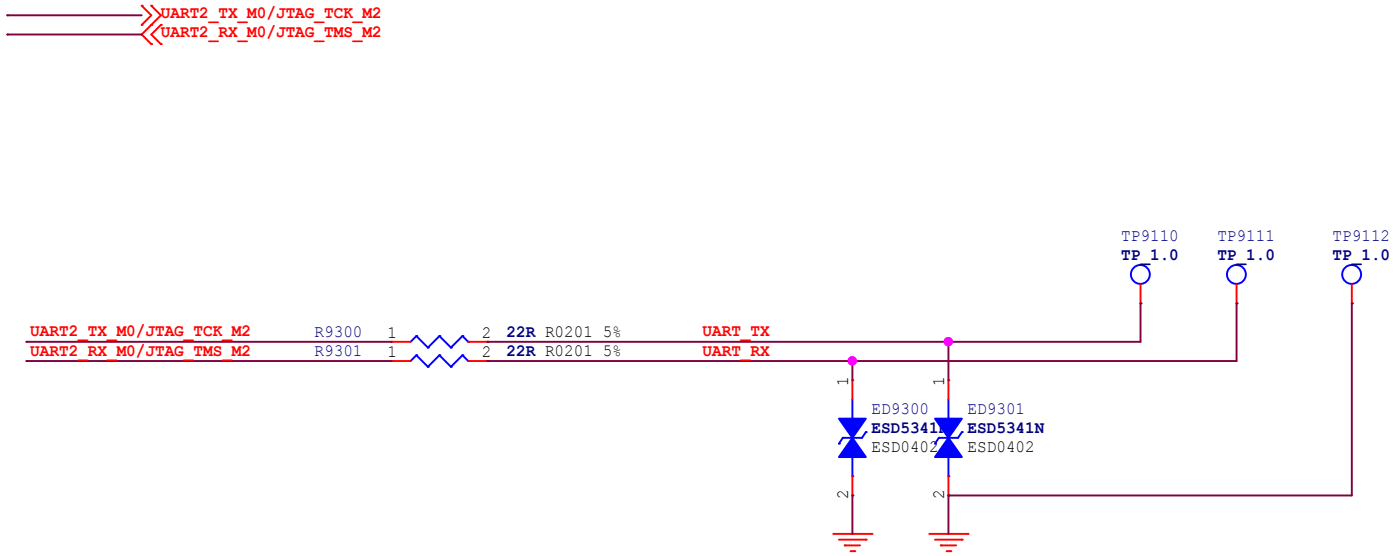
PWR_Key



Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	92.KEY Array				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	31 of 32

UART Debug

JTAG Debug



Rockchip Electronics Co., Ltd					
Project:	RK3588S_Demo				
File:	93.Debug UART/JTAG Port				
Date:	Friday, January 07, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	32 of 32