Reference Schematics For RK3588S

RK3588S_Tablet_REF_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
4) ROM: eMMC5.1(Default) or SPI Falsh
5) Support: 1 x Micro SD Card3.0
6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
8) Support: 2 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
10) Support: 2 x 4Lanes MIPI D/CPHY TX
11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
13) Support: 2 x PDM MIC Array
14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	00.Cover Page				
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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
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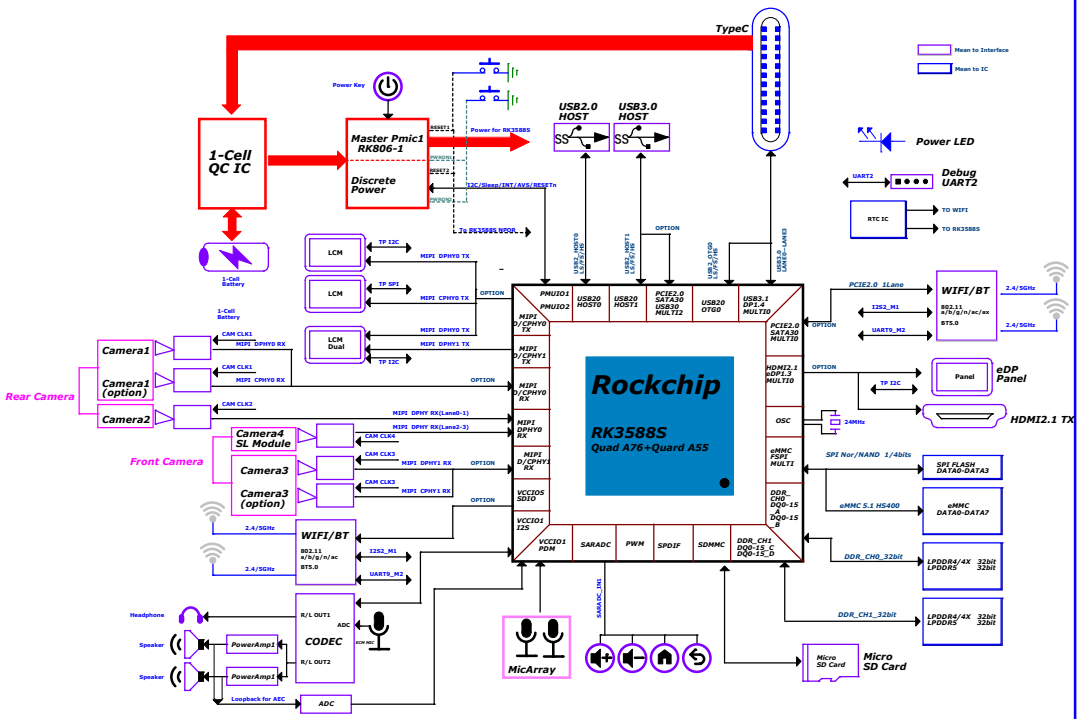
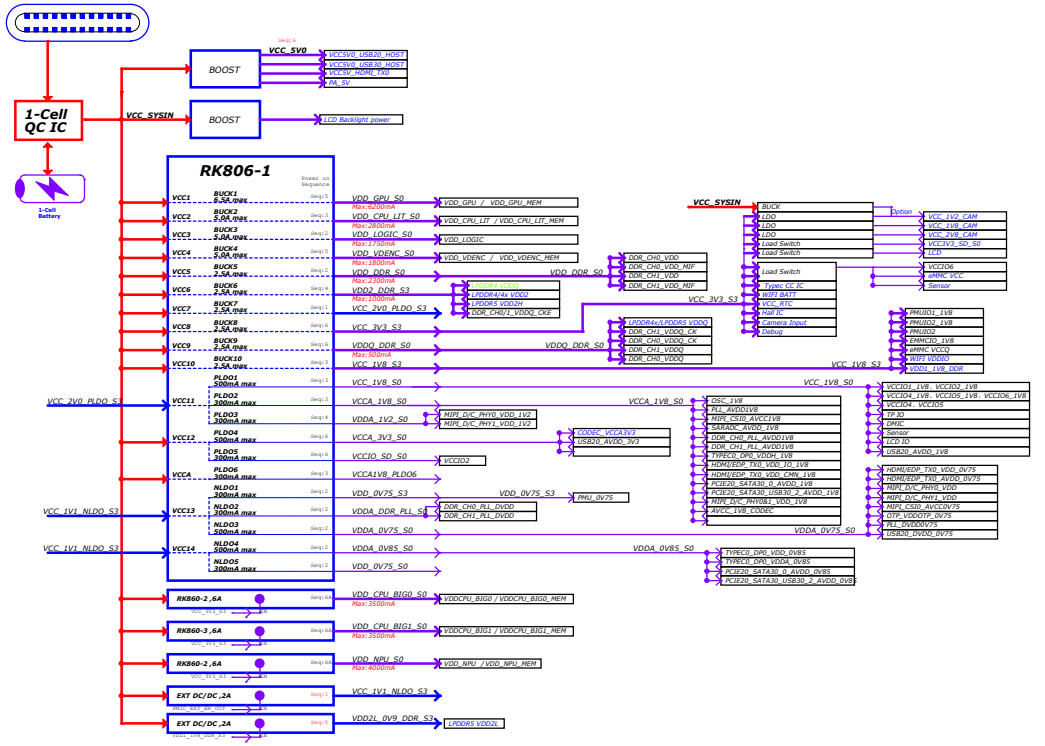
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.Wei	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203，L2205，L2207，L2300，L2301，L2302电感由0.22uH(TDK) 改为0.24uH(Sunlord); L2201的电感由0.22uH(TDK)改为0.22uH (Sunlord)，封装IND_404020。 4.HDMI eARC功能不支持，相关eARC网络改成HDMI0_TX_SBDP/N	

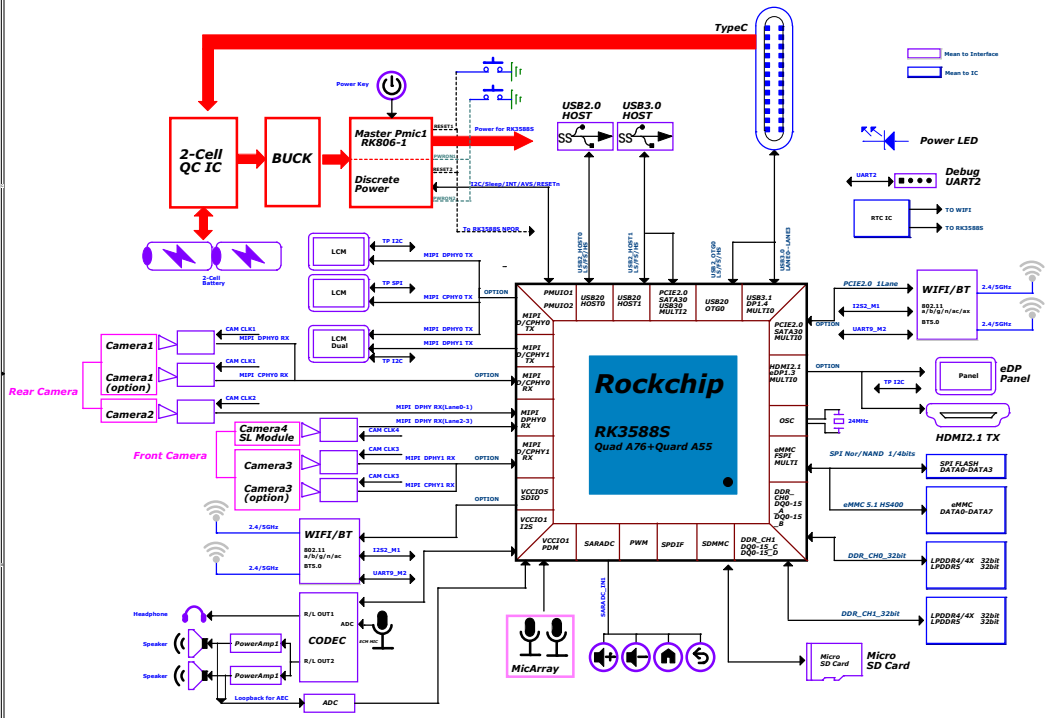
RK3588S Tablet Ref Block Diagram for 1-Cell Charger



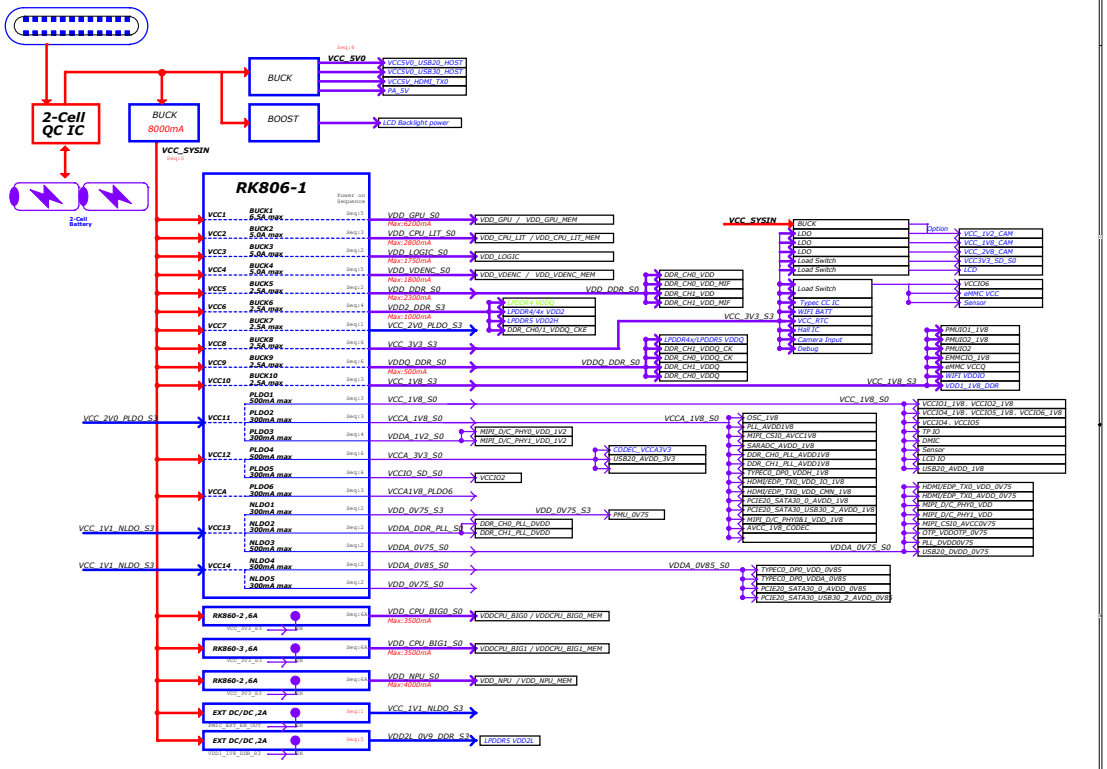
Power tree for 1-Cell Charger



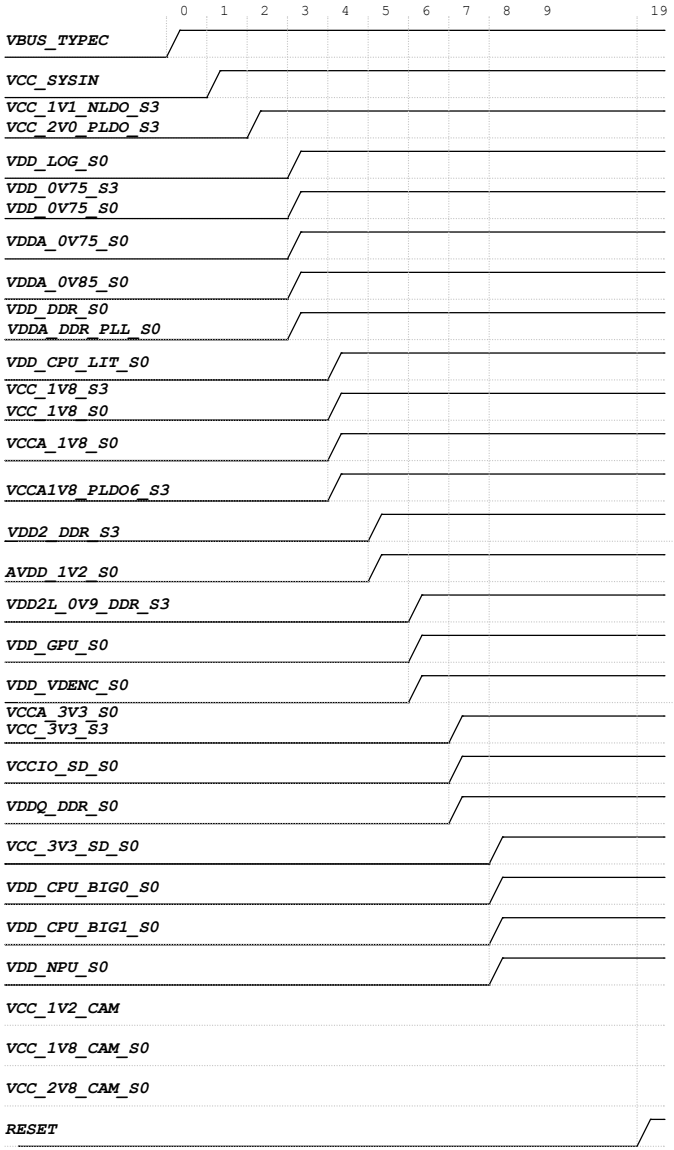
RK3588S Tablet Ref Block Diagram for 2-Cell Charger



Power tree for 2-Cell Charger



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	05.System Power Sequence				
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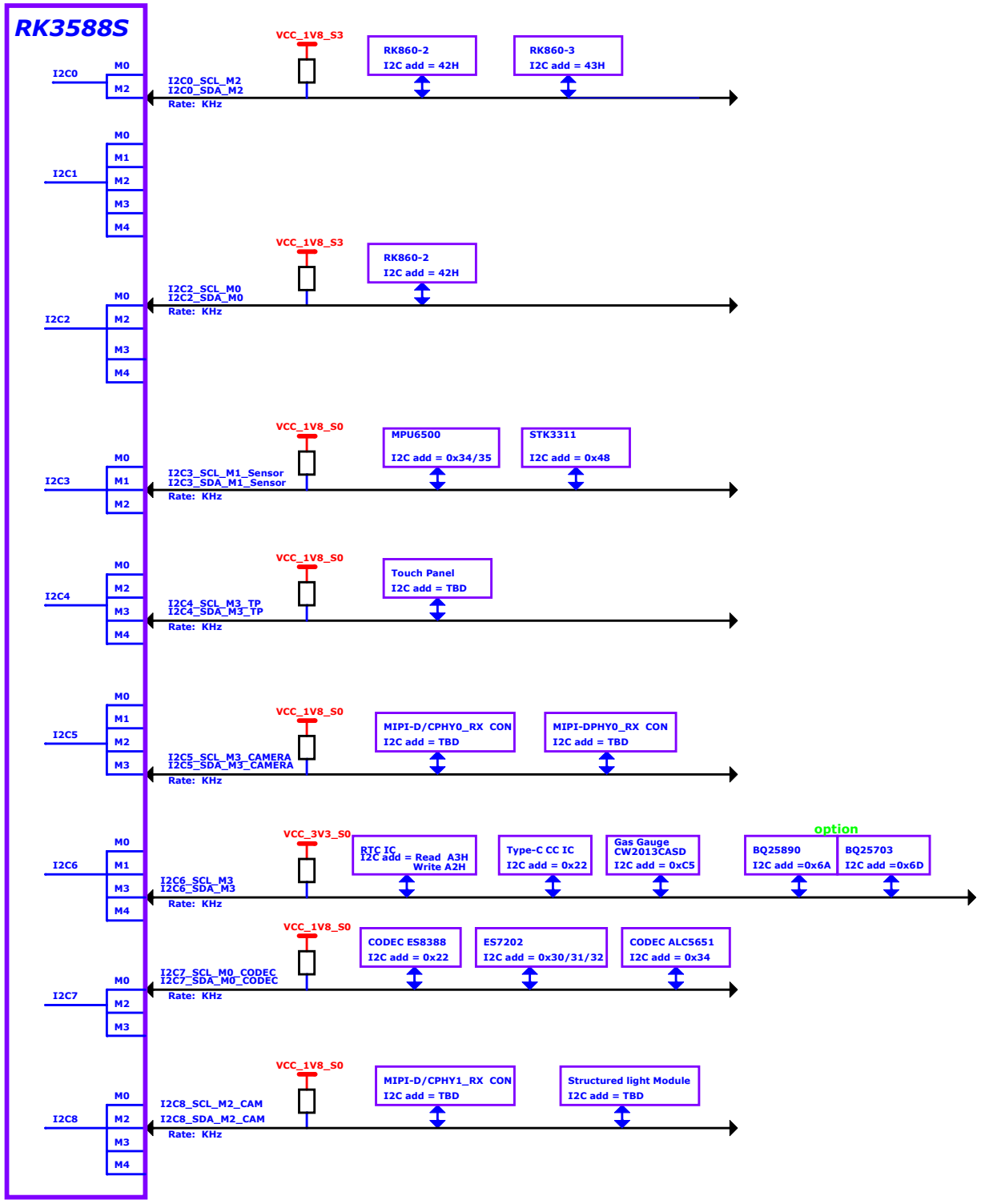
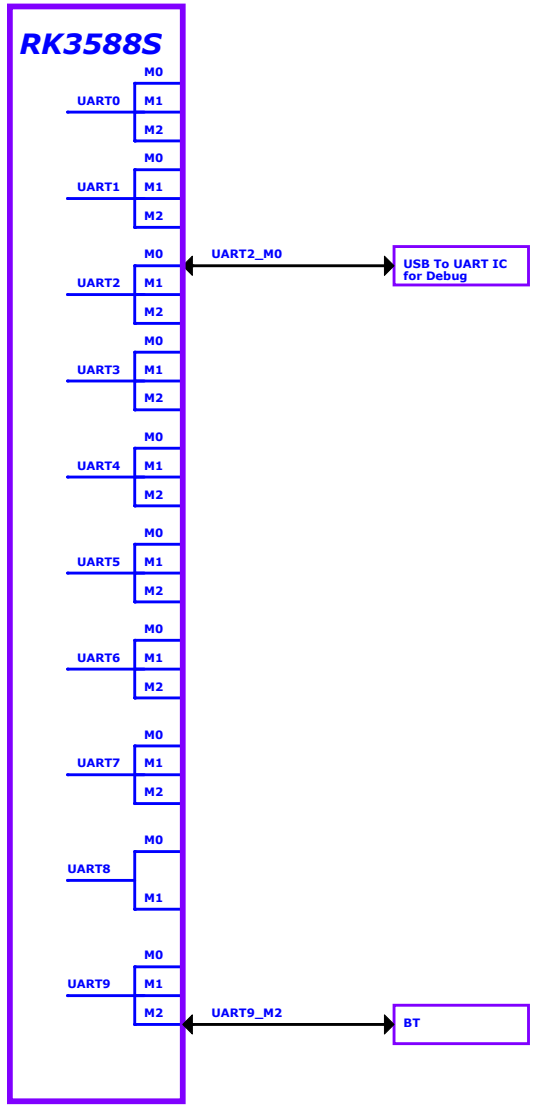
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	6 of 53

I2C MAP



UART MAP



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	06.Lower-Speed Bus Map
Date:	Monday, February 21, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
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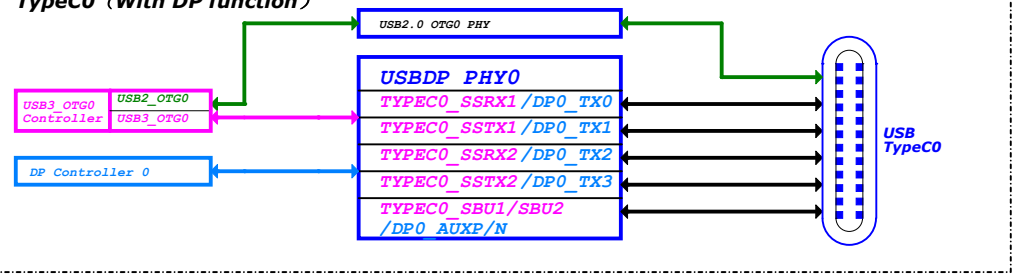
USB Controller Configure Table

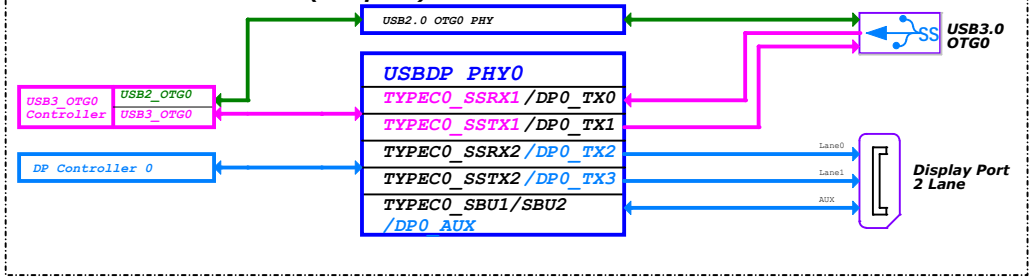
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

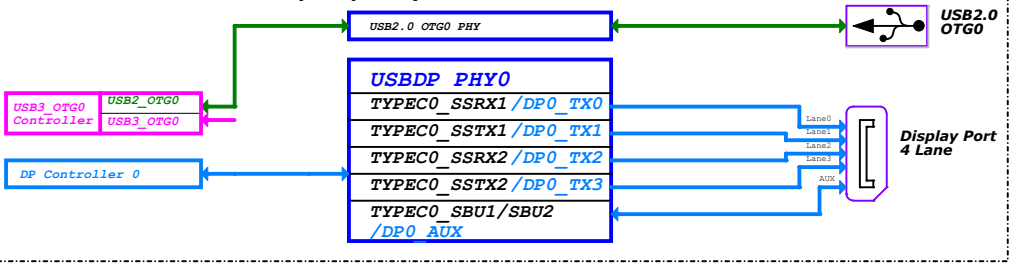
Config0:
TypeC0（With DP function）



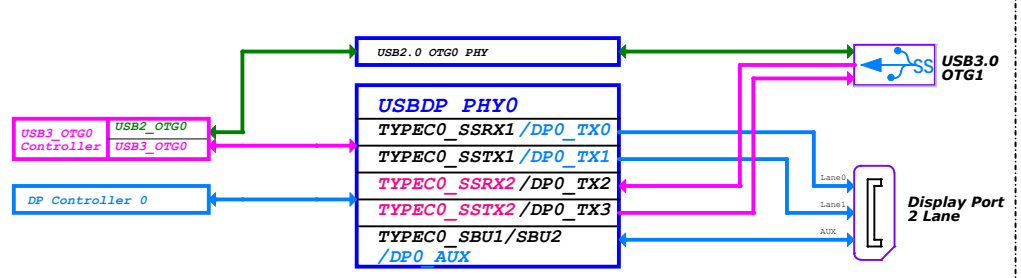
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



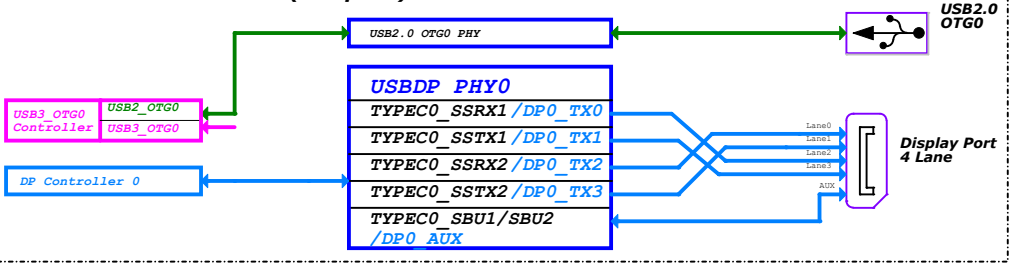
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	07.USB Controller Configure Tab
Date:	Monday, February 21, 2022
Designed by:	Joseph
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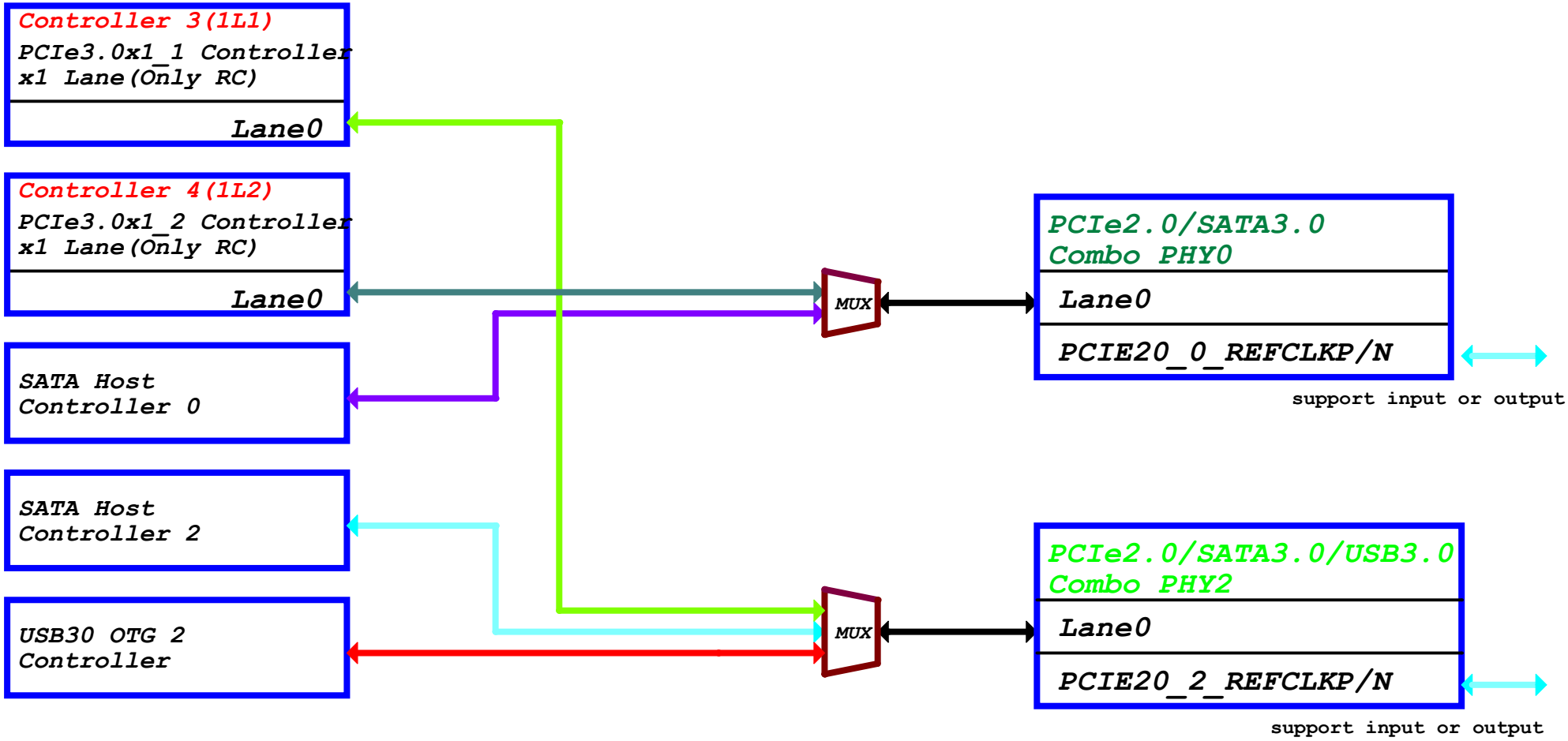
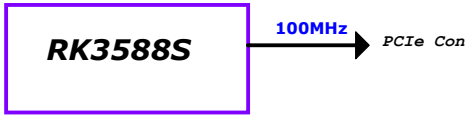
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	08.PCIE Fun Map				
Date:	Monday, February 21, 2022			Rev:	V10
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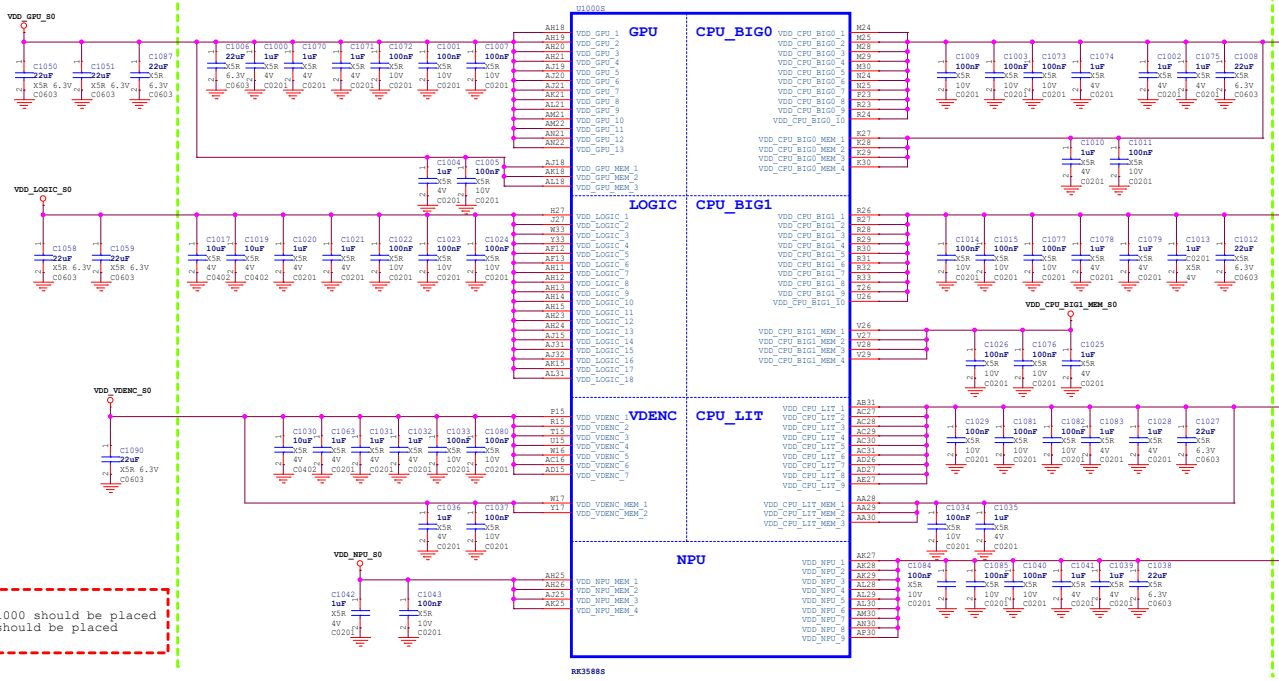
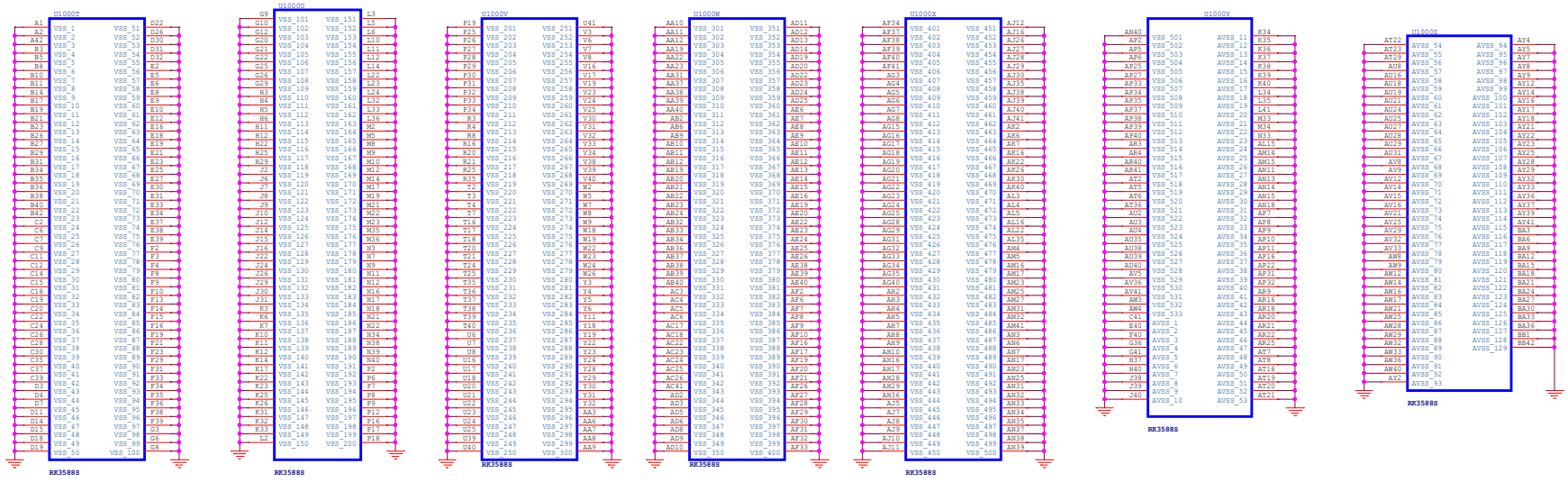
RK3588S(Power&Gnd)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



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Project:	RK3588S_Tablet_REF		
File:	10.RK3588S_Power/GND		
Date:	Monday, February 21, 2022	Rev:	V10
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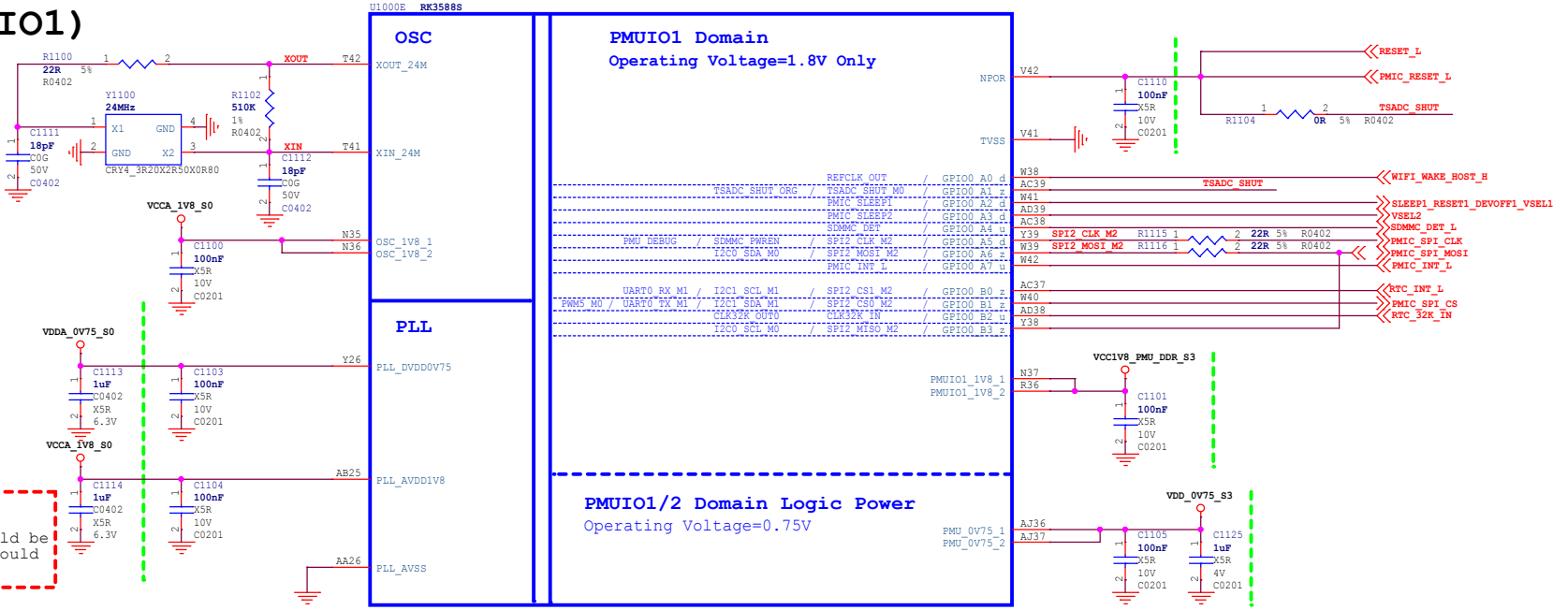
RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

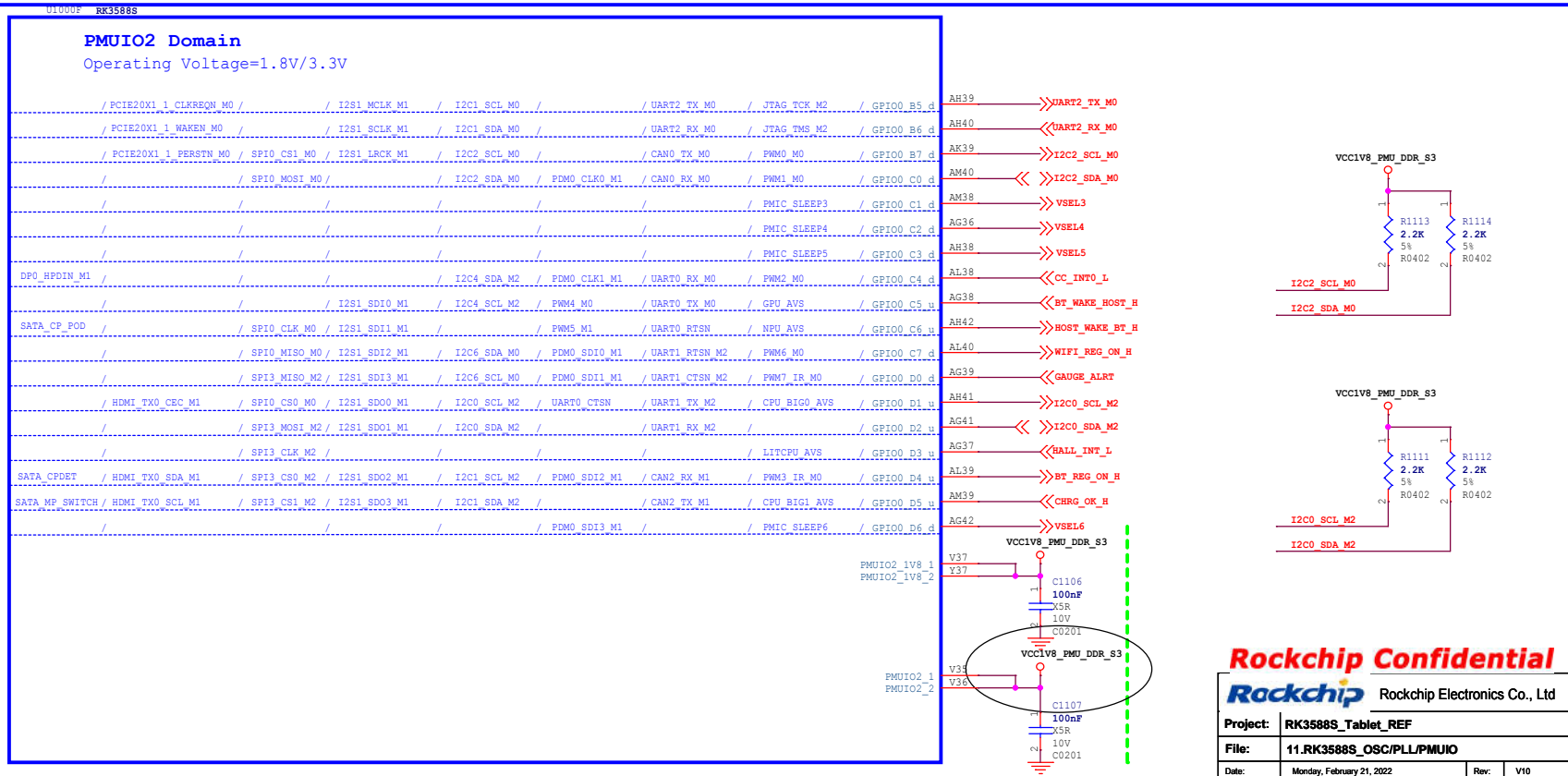
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588S(PMUIO2)



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S_Tablet_REF				
File:	11.RK3588S_OSC/PLL/PMUIO				
Date:	Monday, February 21, 2022			Rev:	V10
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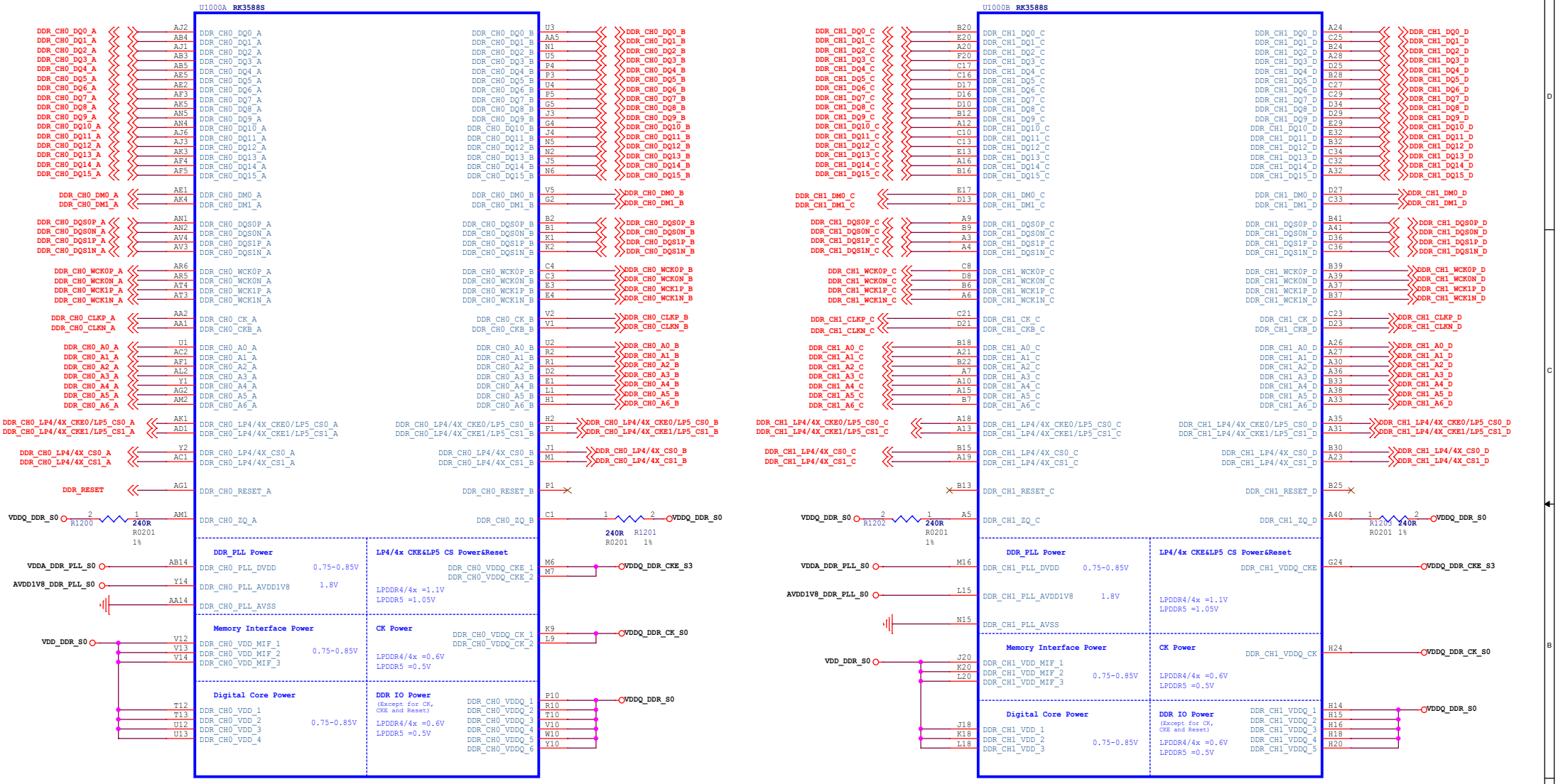
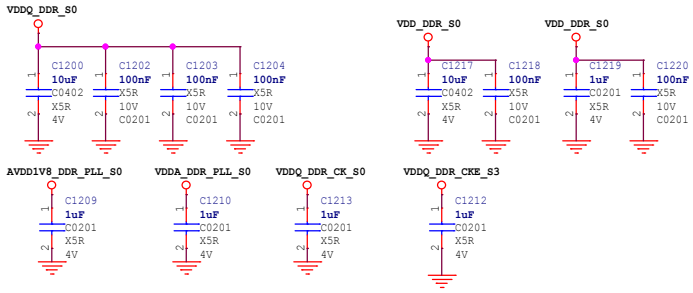
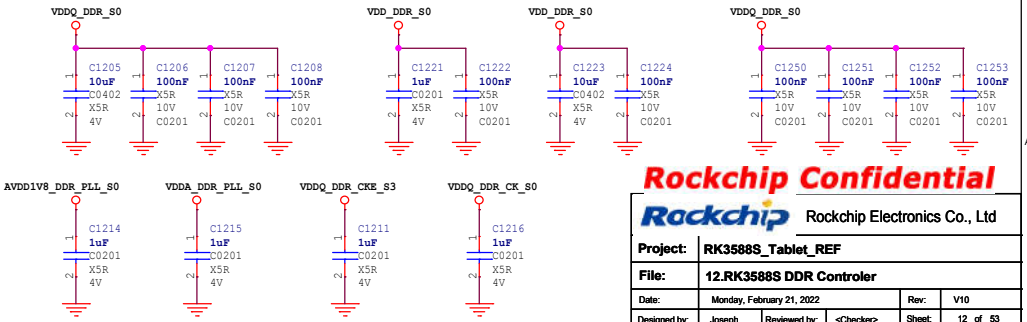
RK3588S(DDR PHY)



DDR FILTER



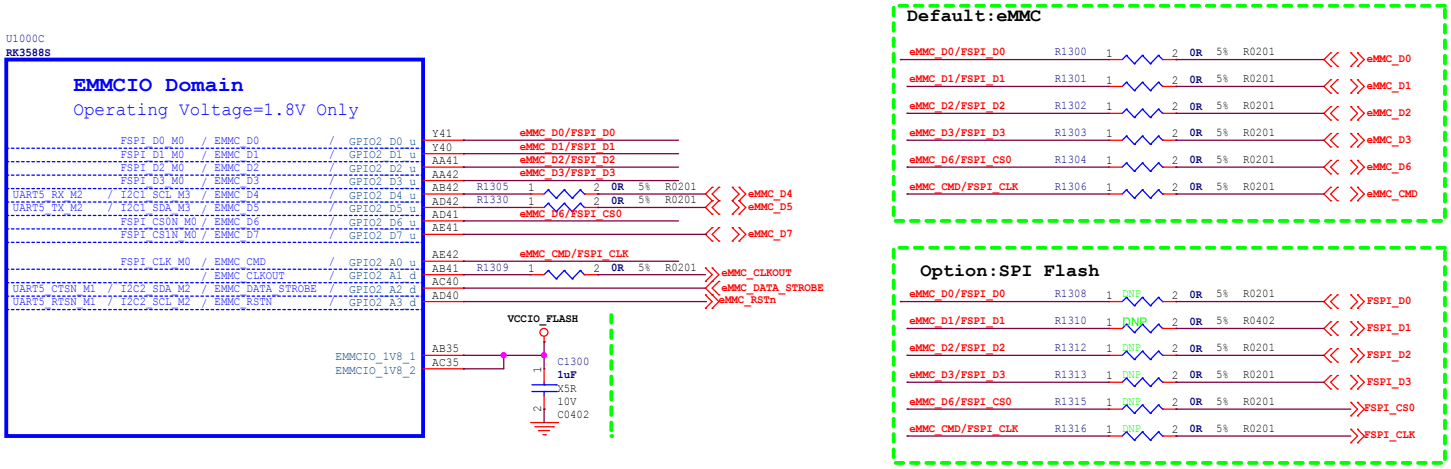


Rockchip Confidential

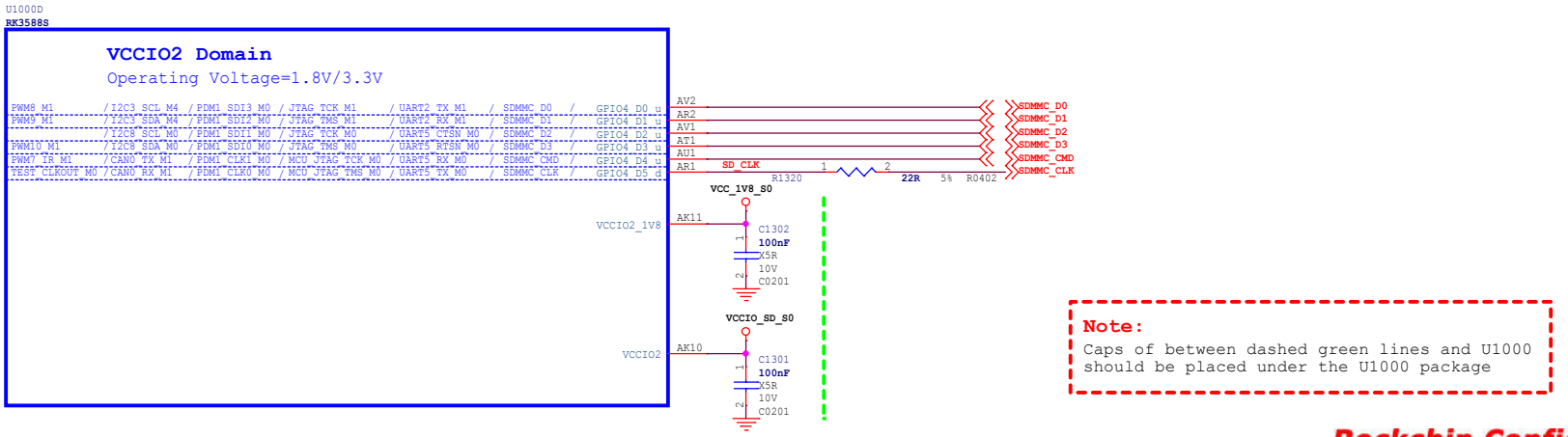
Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF				
File:	12.RK3588S DDR Controler				
Date:	Monday, February 21, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	12 of 53

RK3588S(EMMCIO Domain)



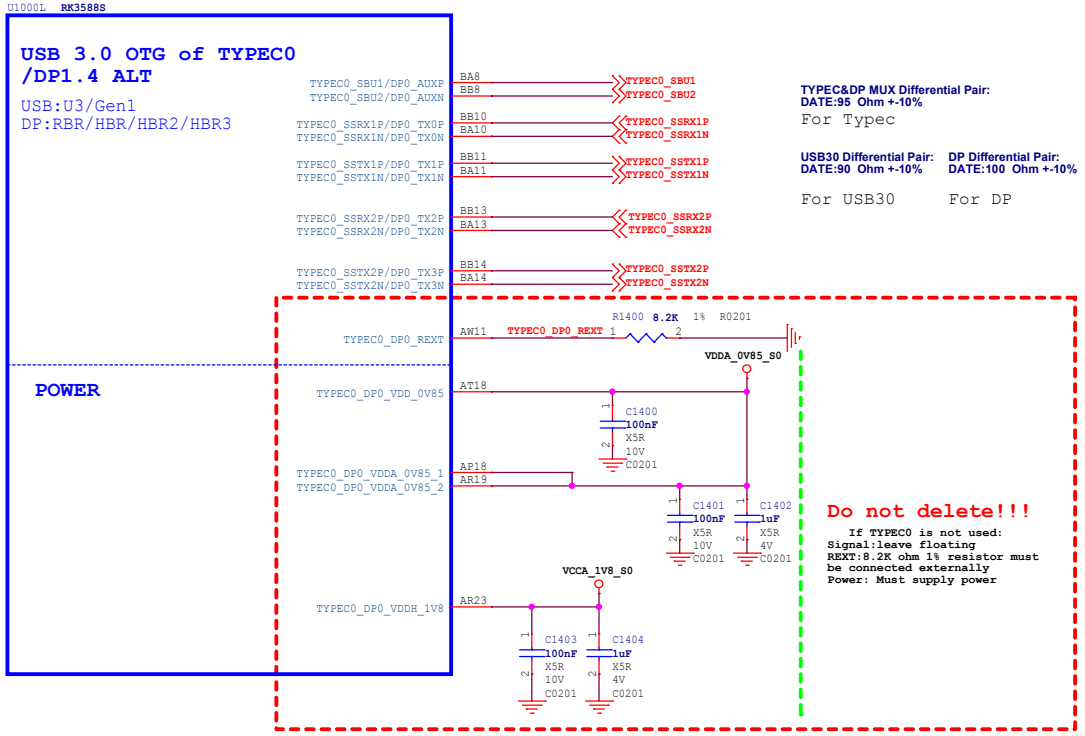
RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	13.RK3588S Flash/SD Controller				
Date:	Monday, February 21, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 53

RK3588S(USB3.0/DP1.4)

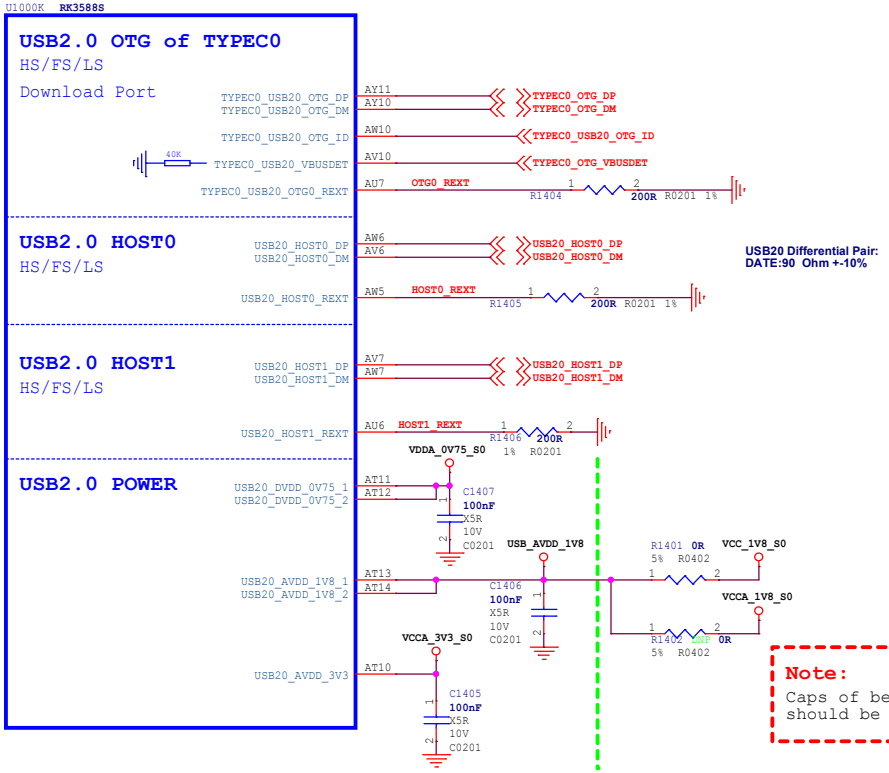


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

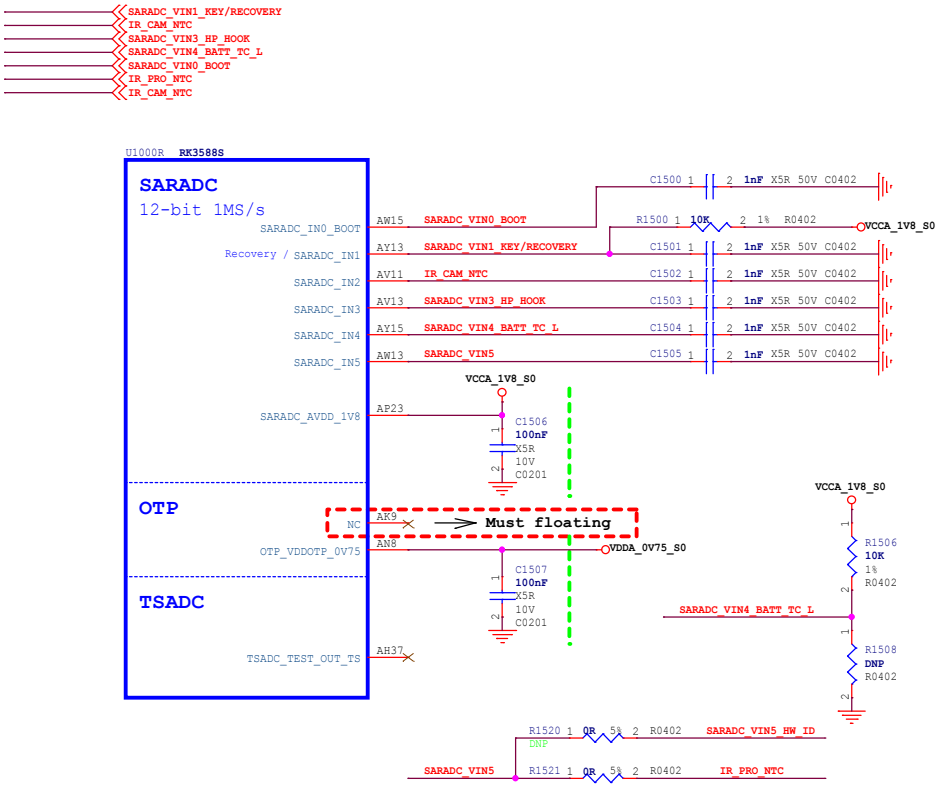
USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

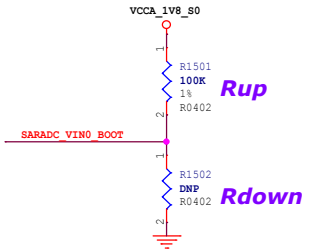
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	14.RK3588S_USB20/USB30/DP PHY				
Date:	Monday, February 21, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	14 of 53

RK3588S(SARADC/OTP/TSADC)

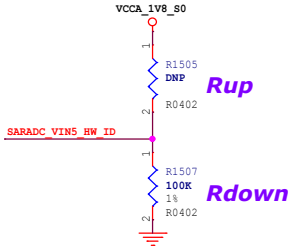


BOOT MODE CONFIG



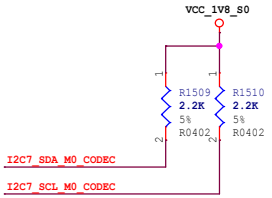
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

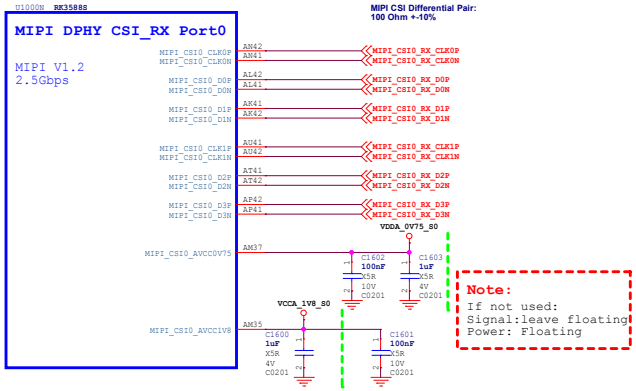
RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	15.RK3588S_SARADC/1.8V GPIO				
Date:	Monday, February 21, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	15 of 53

RK3588S(MIPI_DPHY CSI0 RX)

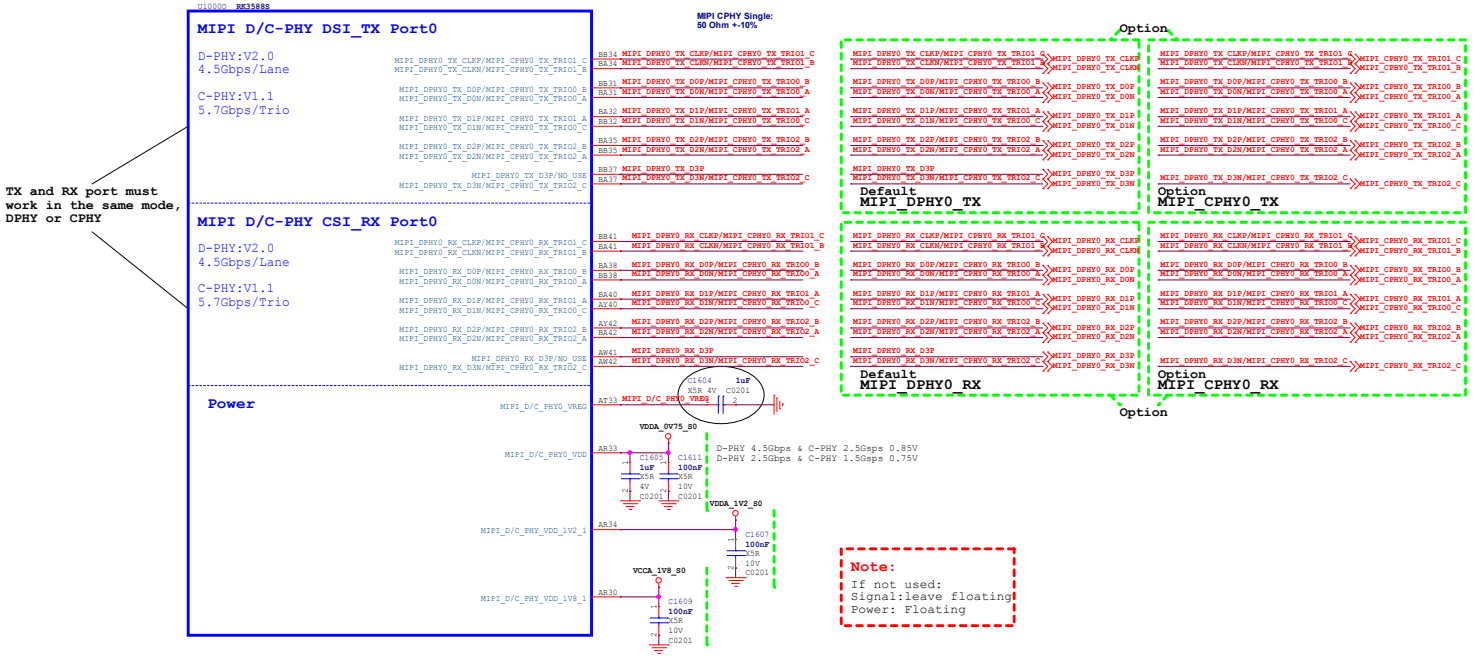


Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

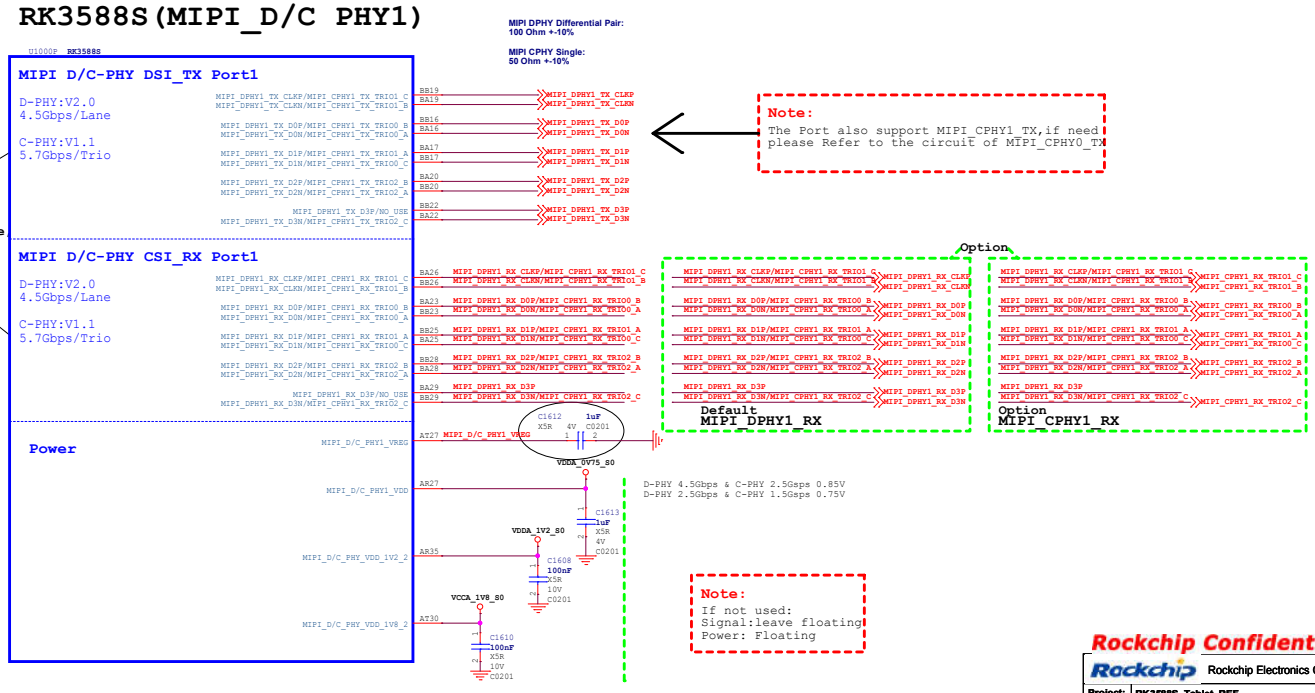
Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



RK3588S(MIPI_D/C PHY1)



Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Tablet_REF		
File:	16.RK3588S_MIPI Interface		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet	16 of 53

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm ±10%

HDMI TX
100 Ohm ±10%

U1000Q

HDMI TX/eDP1.3 MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P
HDMI_TX0_D0N/EDP_TX0_D0N
HDMI_TX0_D1P/EDP_TX0_D1P
HDMI_TX0_D1N/EDP_TX0_D1N
HDMI_TX0_D2P/EDP_TX0_D2P
HDMI_TX0_D2N/EDP_TX0_D2N
HDMI_TX0_D3P/EDP_TX0_D3P
HDMI_TX0_D3N/EDP_TX0_D3N
HDMI_TX0_SBDP/EDP_TX0_AUXP
HDMI_TX0_SBDN/EDP_TX0_AUXN
HDMI/eDP_TX0_REXT

POWER

HDMI/EDP_TX0_VDD_0V75_1
HDMI/EDP_TX0_VDD_0V75_2
HDMI/EDP_TX0_AVDD_0V75
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8

RK3588S

BB4 EDP_TX0_D0P/HDMI0_TX0P
BA4 EDP_TX0_D0N/HDMI0_TX0N
BA5 EDP_TX0_D1P/HDMI0_TX1P
BB5 EDP_TX0_D1N/HDMI0_TX1N
BB7 EDP_TX0_D2P/HDMI0_TX2P
BA7 EDP_TX0_D2N/HDMI0_TX2N
BA2 EDP_TX0_D3P/HDMI0_TX3P
BB2 EDP_TX0_D3N/HDMI0_TX3N
BA1 EDP_TX0_AUXP/HDMI0_TX_SBDP
AY1 EDP_TX0_AUXN/HDMI0_TX_SBDN
AY3 HDMI/eDP_TX0_REXT

Option

Option1:eDP_TX0

EDP_TX0_D0P/HDMI0_TX0P → EDP_TX0_D0P
EDP_TX0_D0N/HDMI0_TX0N → EDP_TX0_D0N
EDP_TX0_D1P/HDMI0_TX1P → EDP_TX0_D1P
EDP_TX0_D1N/HDMI0_TX1N → EDP_TX0_D1N
EDP_TX0_D2P/HDMI0_TX2P → EDP_TX0_D2P
EDP_TX0_D2N/HDMI0_TX2N → EDP_TX0_D2N
EDP_TX0_D3P/HDMI0_TX3P → EDP_TX0_D3P
EDP_TX0_D3N/HDMI0_TX3N → EDP_TX0_D3N
EDP_TX0_AUXP/HDMI0_TX_SBDP → EDP_TX0_AUXP
EDP_TX0_AUXN/HDMI0_TX_SBDN → EDP_TX0_AUXN

Option2:HDMI_TX0

EDP_TX0_D0P/HDMI0_TX0P → HDMI0_TX0P
EDP_TX0_D0N/HDMI0_TX0N → HDMI0_TX0N
EDP_TX0_D1P/HDMI0_TX1P → HDMI0_TX1P
EDP_TX0_D1N/HDMI0_TX1N → HDMI0_TX1N
EDP_TX0_D2P/HDMI0_TX2P → HDMI0_TX2P
EDP_TX0_D2N/HDMI0_TX2N → HDMI0_TX2N
EDP_TX0_D3P/HDMI0_TX3P → HDMI0_TX3P
EDP_TX0_D3N/HDMI0_TX3N → HDMI0_TX3N
EDP_TX0_AUXP/HDMI0_TX_SBDP → HDMI0_TX_SBDP
EDP_TX0_AUXN/HDMI0_TX_SBDN → HDMI0_TX_SBDN

R1708 1 — 2 **8.2K** 1% R0201

VDDA_0V75_S0
AM13
AN12
C1710 **100nF** X5R 10V C0201
C1711 **4.7uF** X5R 6.3V C0402
C1718 **10uF** X5R 6.3V C0603

AN10
C1712 **100nF** X5R 10V C0201
C1725 **1uF** X5R 4V C0201

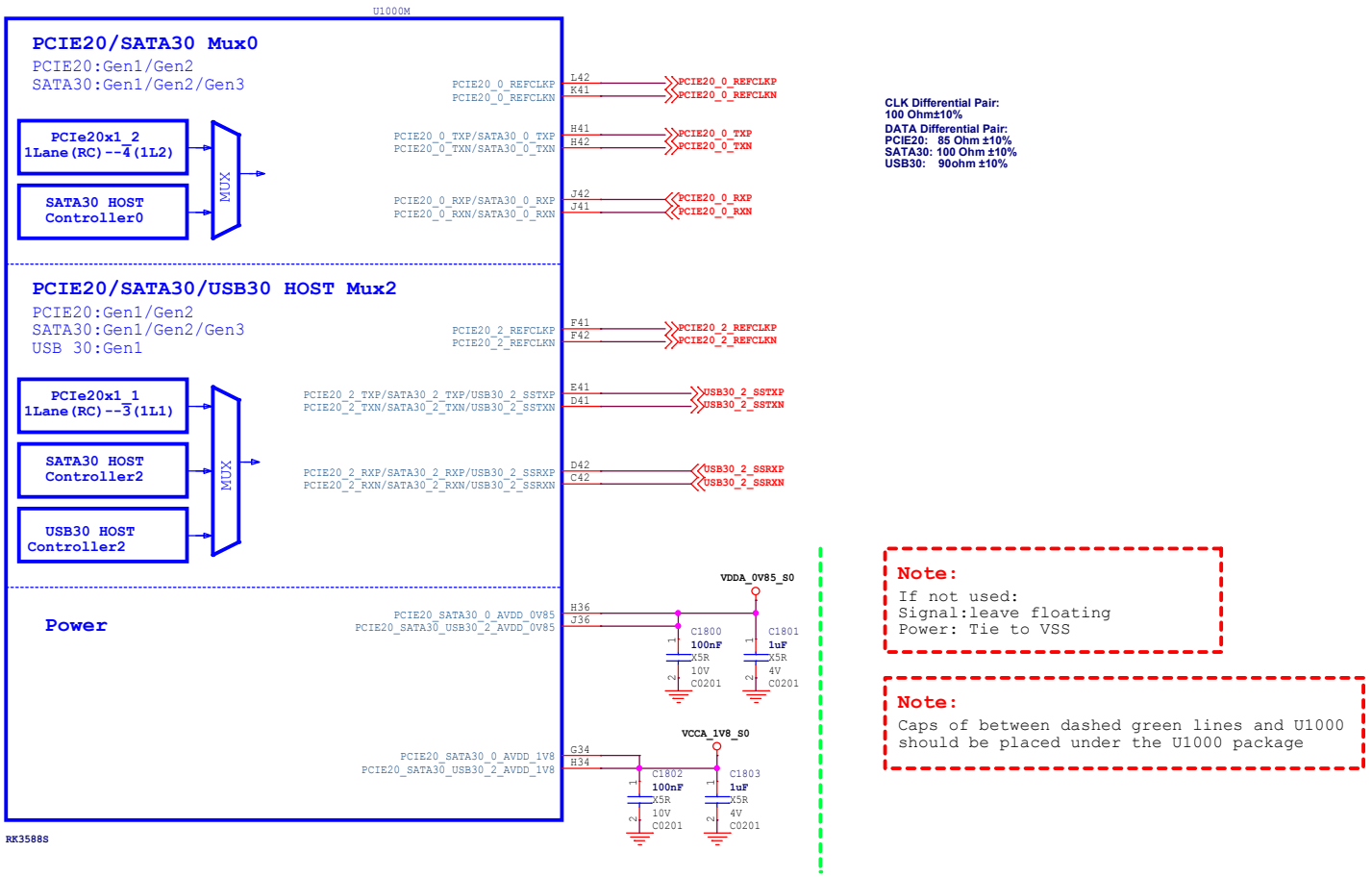
VCCA_1V8_S0
AK12
AL14
C1713 **100nF** X5R 10V C0201
C1714 **4.7uF** X5R 6.3V C0402
C1716 **4.7uF** X5R 6.3V C0402

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	17.RK3588S_HDMI/eDP Interface				
Date:	Monday, February 21, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 53

RK3588S(PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

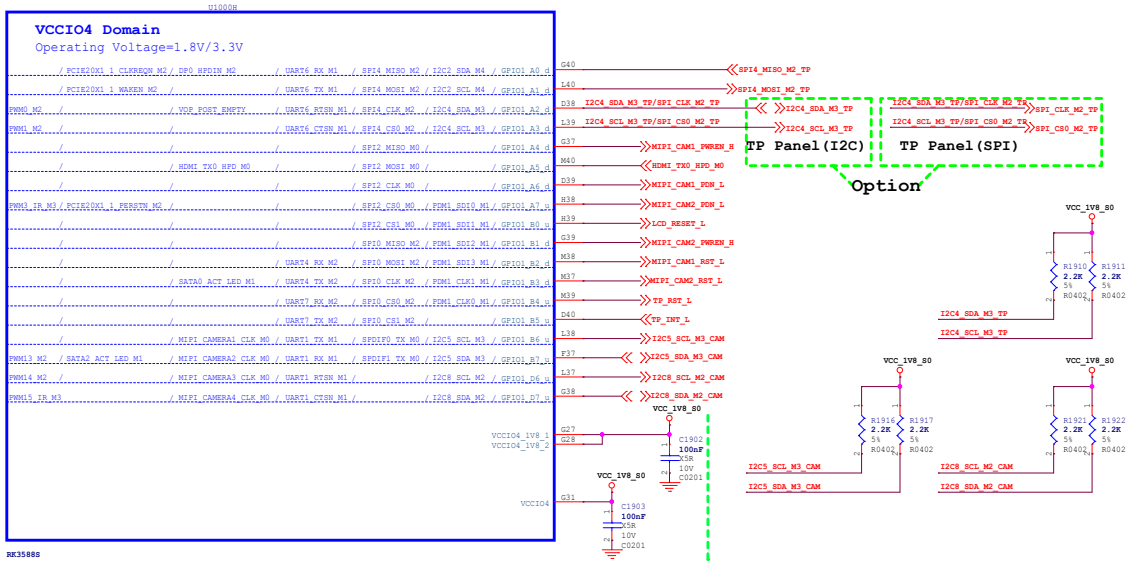
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

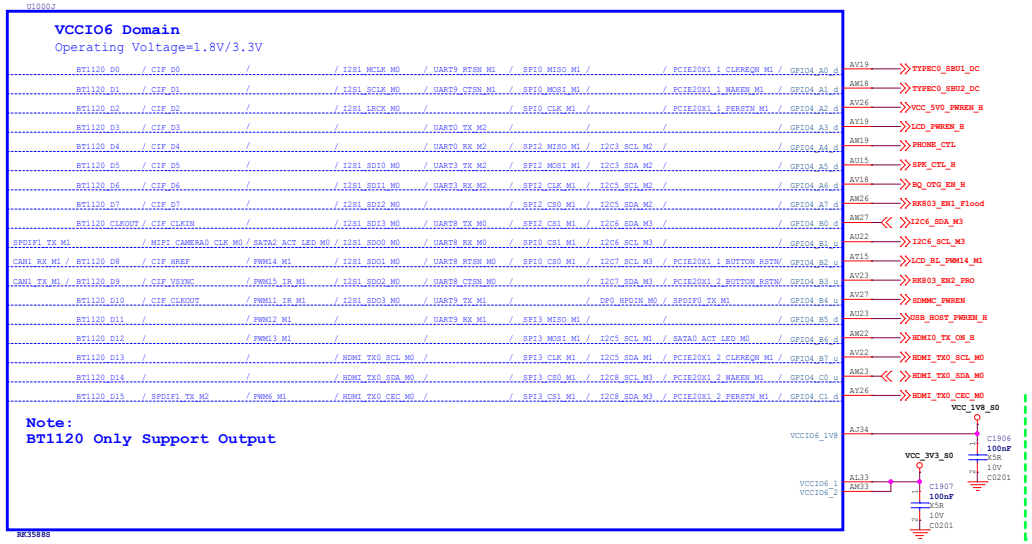
Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Rockchip Electronics Co., Ltd					
Project:	RK3588S_Tablet_REF				
File:	18.RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Tuesday, April 12, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	18 of 53

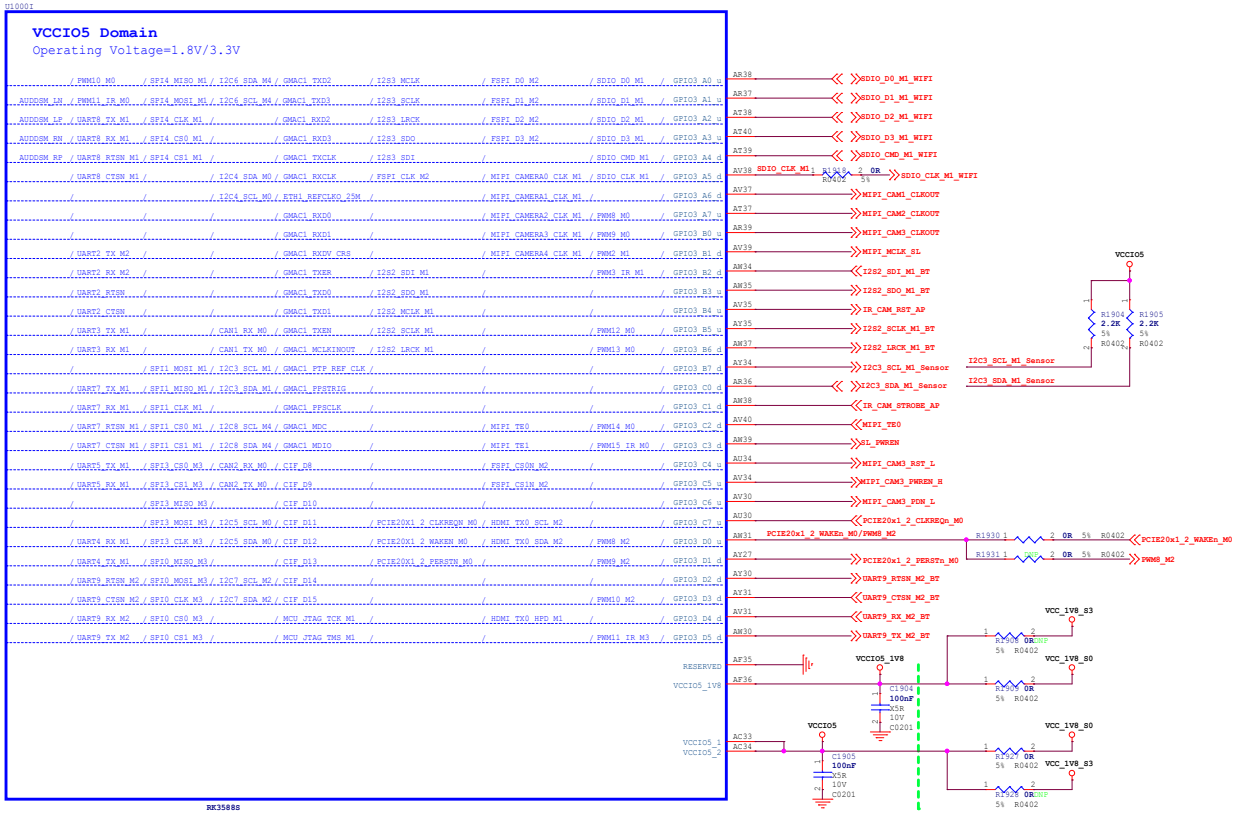
RK3588S(VCCIO4 Domain)

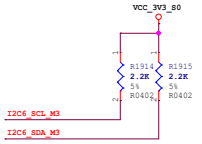


RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)



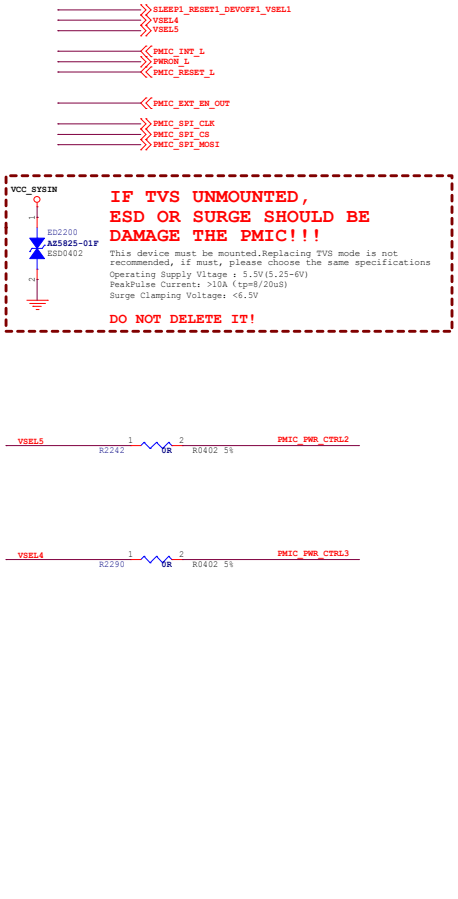


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

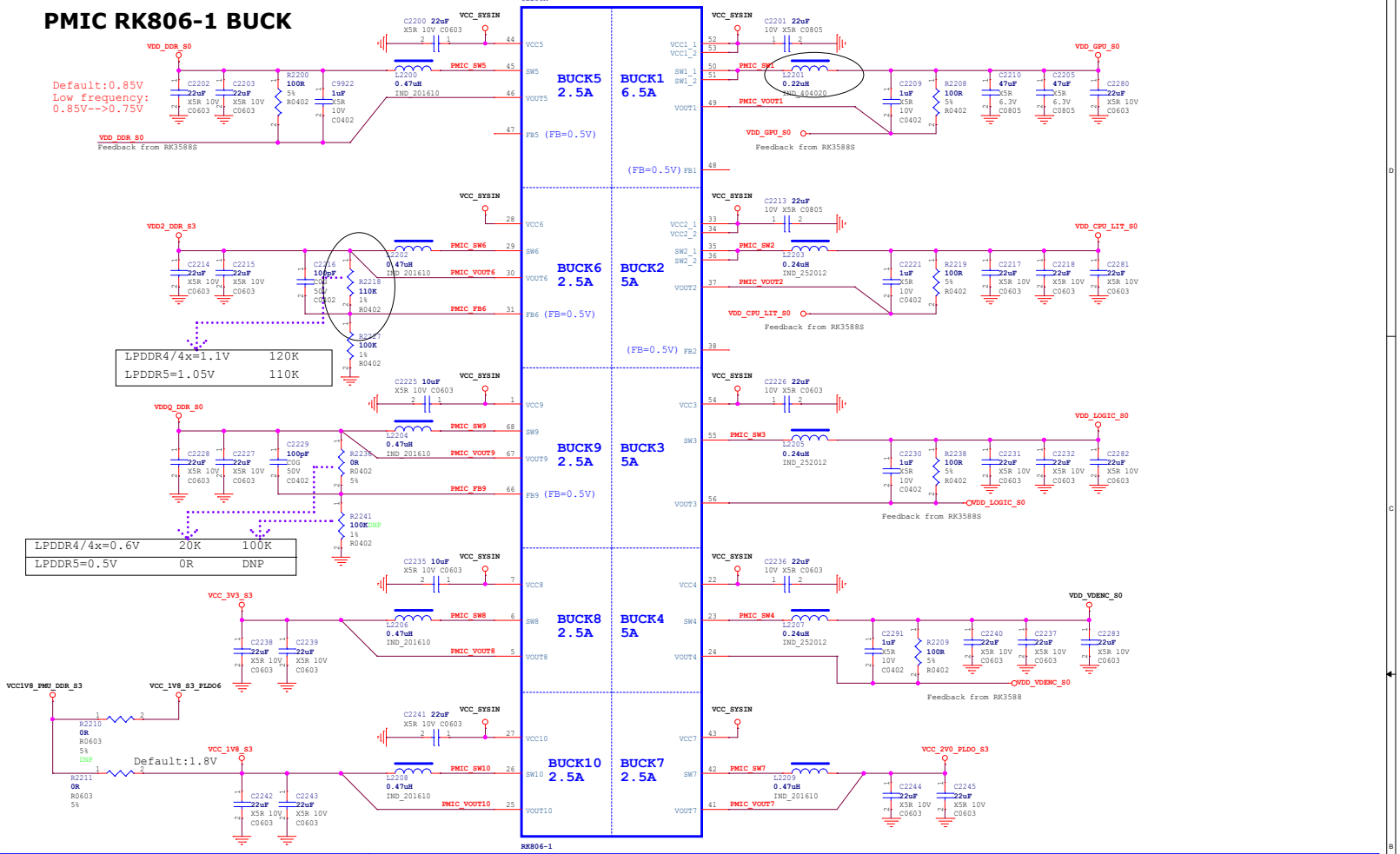
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588S_Tablet_REF		
File:	19.RK3588S GPIO		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet 19 of 53

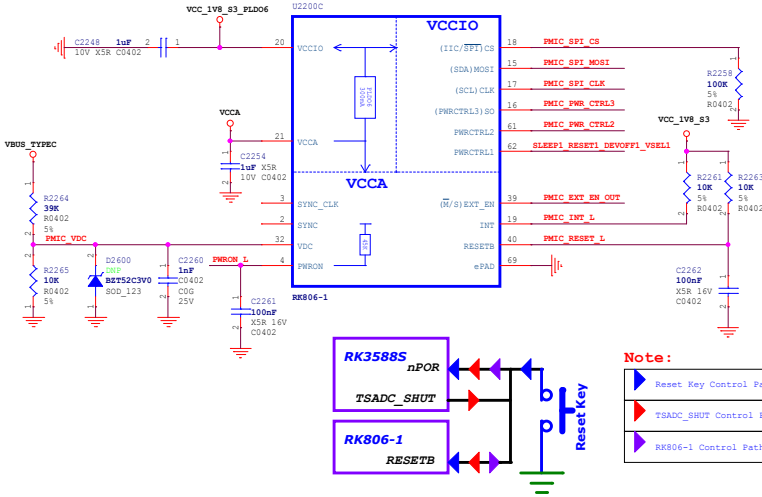
PMIC1 RK806-1



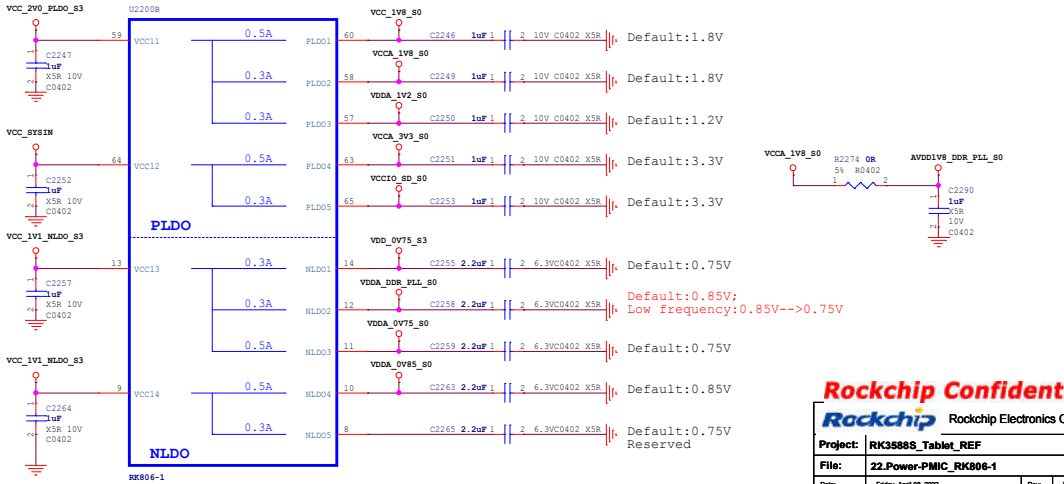
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



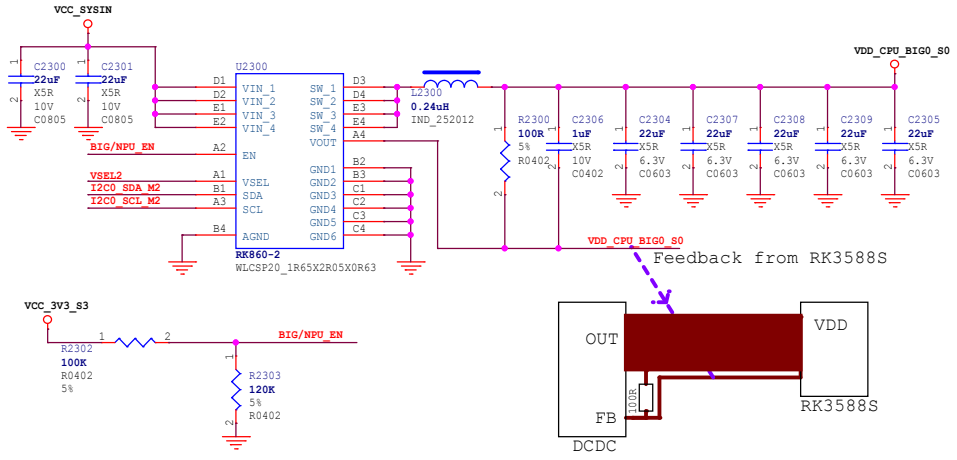
PMIC RK806-1 LDO



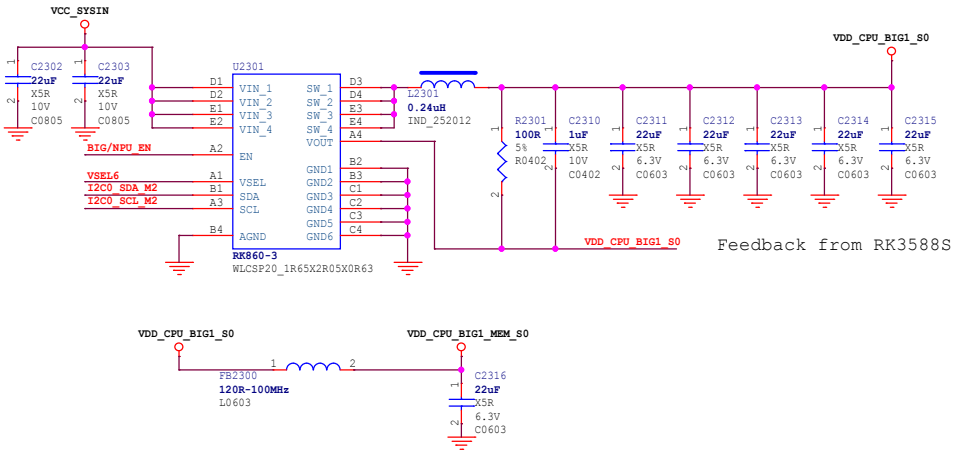
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S_Tablet_REF
File:	22.Power-PMIC_RK806-1
Date:	Friday, April 08, 2022
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	22 of 53

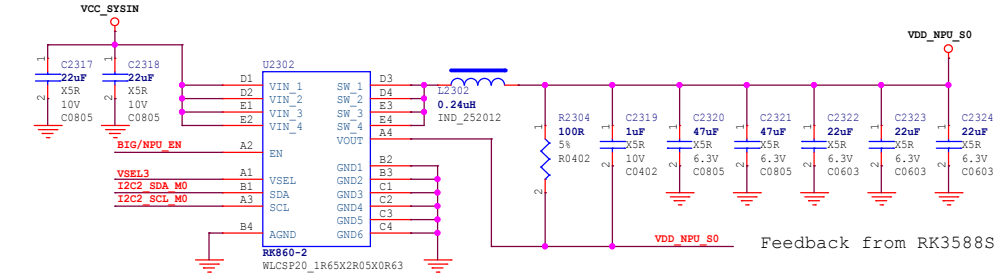
VDD_CPU_BIG0



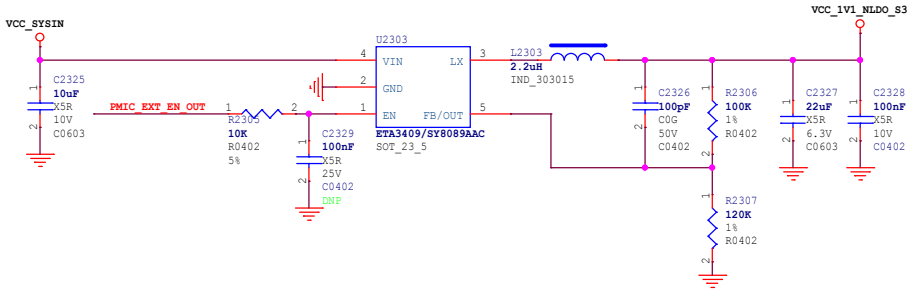
VDD_CPU_BIG1



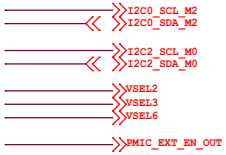
VDD_NPU

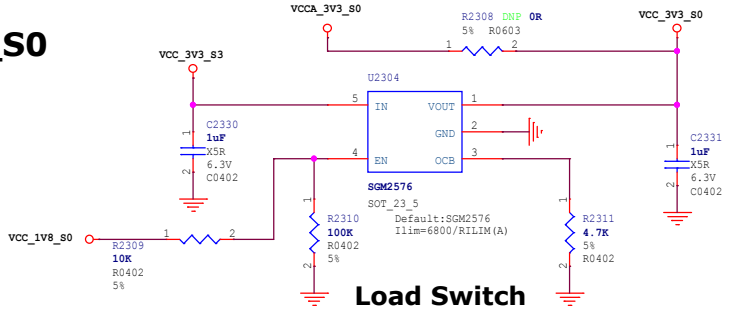


VCC_1V1_NLDO



VCC_3V3_S0





Rockchip Confidential

Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF				
File:	23.Power_Ext Discrete				
Date:	Wednesday, February 23, 2022			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	23 of 53

DRAM-LPDDR5_2X32bit