

Reference Schematics For RK3588S

RK3588S_Tablet_REF_SCH

Main Functions Introduction

- 1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
- 2) PMIC: 1 x RK806-1+DiscretePower
- 3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
- 4) ROM: eMMC5.1(Default) or SPI Falsh
- 5) Support: 1 x Micro SD Card3.0
- 6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
- 7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
- 8) Support: 2 x 2Lanes MIPI DPHY RX Camera
- 9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
- 10) Support: 2 x 4Lanes MIPI D/CPHY TX
- 11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
- 12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
- 13) Support: 2 x PDM MIC Array
- 14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

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Project:	RK3588S_Tablet_REF		
File:	00.Cover Page		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	1 of 53		

Table of Content

Page 1	00.Cover Page
Page 2	01.Index and Notes
Page 3	02.Revision History
Page 4	03.Block Diagram_PoweTree-1cell
Page 5	04.Block Diagram_PoweTree-2cell
Page 6	05.System Power Sequence
Page 7	06.Lower-Speed Bus Map
Page 8	07.USB Controller Configure Tab
Page 9	08.PCIE Fun Map
Page 10	10.RK3588S_Power/GND
Page 11	11.RK3588S_OSC/PLL/PMUIO
Page 12	12.RK3588S DDR Controler
Page 13	13.RK3588S Flash/SD Controller
Page 14	14.RK3588S_USB20/USB30/DP PHY
Page 15	15.RK3588S_SARADC/1.8V GPIO
Page 16	16.RK3588S_MIPI Interface
Page 17	17.RK3588S_HDMI/eDP Interface
Page 18	18.RK3588S_PCIE2/SATA3/USB3 PHY
Page 19	19.RK3588S GPIO
Page 20	20.Power_1Cell_QC(opt1)
Page 21	21.Power_2Cell_QC(opt2)
Page 22	22.Power-PMIC_RK806-1
Page 23	23.Power_Ext Discrete
Page 24	24.RTC
Page 25	25.USB20/USB30 HOST Port
Page 26	38.DRAM-LPDDR4/4X_200P_2X32bit
Page 27	39.DRAM-LPDDR5X_315P_2X32bit
Page 28	40.Flash Power
Page 29	41.eMMC Flash
Page 30	42.Flash-Micro-SD Card
Page 31	43.Flash-SPI FLASH(opt)
Page 32	44.VI-CAM1 MIPI_D/CPHY0-RX
Page 33	45.VI-CAM1 MIPI_D/CPHY0-RX(opt)
Page 34	46.VI-CAM2 MIPI_DPHY0-RX
Page 35	47.VI-CAM3 MIPI_D/CPHY1-RX
Page 36	48.VI-CAM3 MIPI_D/CPHY1-RX(opt)
Page 37	49.VI-CAM4 SL Module
Page 38	50.VO-HDMI2.1 TX
Page 39	51.VO-LCM_eDP1.3 TX
Page 40	52.VO-LCM_MIPI_D/CPHY0_TX
Page 41	53.VO-LCM_MIPI_D/CPHY0_TX(opt)
Page 42	54.VO-LCM_Dual MIPI_D/CPHY TX
Page 43	59.TP Connector_COF(I2C)
Page 44	62.WIFI/BT-SDIO_2T2R(opt1)
Page 45	63.WIFI/BT-PCIE_2T2R(opt2)
Page 46	70.Audio Codec
Page 47	71.Audio Codec(opt)
Page 48	72.Audio-Loopback
Page 49	77.Audio-DMIC Array
Page 50	90.Sensor
Page 51	92.KEY Array
Page 52	93.UART Debug
Page 53	99.Mark/Heatsink

Note
 The power suffix S0 or S3 means:
S3: Keep power On during sleeping
S0:Power off during sleeping

Generate Bill of Materials

Header:
 Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:
 {Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
 1. DNP stands for component not mounted temporarily
 2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
 Please use our recommended components to avoid too many changes.
 For more informations about the second source,please refer to our AVL.

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Project:	RK3588S_Tablet_REF			
File:	01.Index and Notes			
Date:	Monday, February 21, 2022	Rev:	V10	
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet: 2 of 53

Revision History

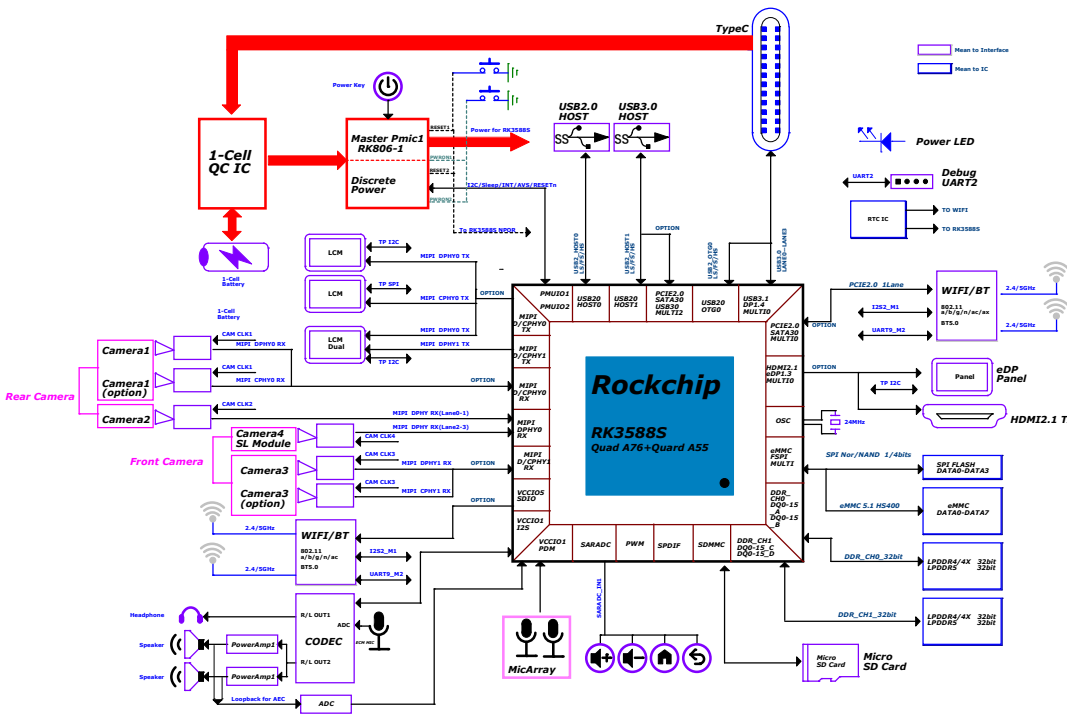
Version	Date	By	Change Description	Approved
V1.0	2022-01-05	Joseph.We	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.We	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203, L2205, L2207, L2300, L2301, L2302电感器由0.22uH(TDK)改为0.24uH(Sunlord); L2201的电感器由0.22uH(TDK)改为0.22uH (Sunlord), 封装IND_404020。 4.HDMI eARC功能不支持，相关eARC网络改成HDMI0_TX_SBDP/N	

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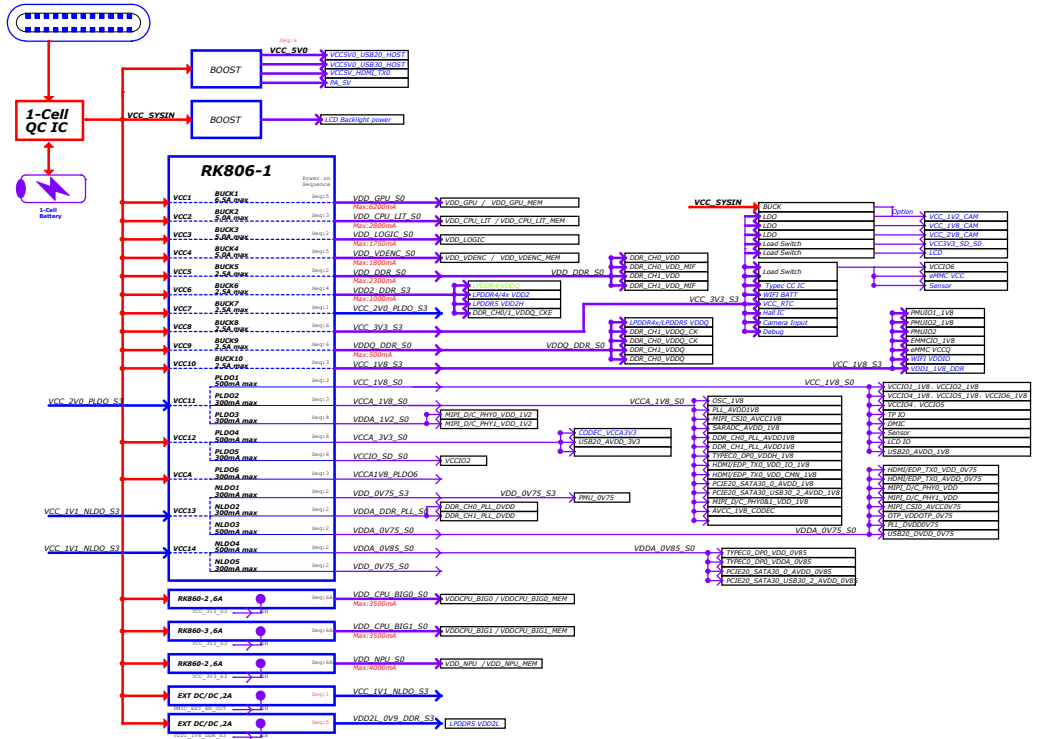
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Project:	RK3588S_Tablet_REF		
File:	02.Revision History		
Date:	Wednesday, February 23, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	3 of 53		

RK3588S Tablet Ref Block Diagram for 1-Cell Charger

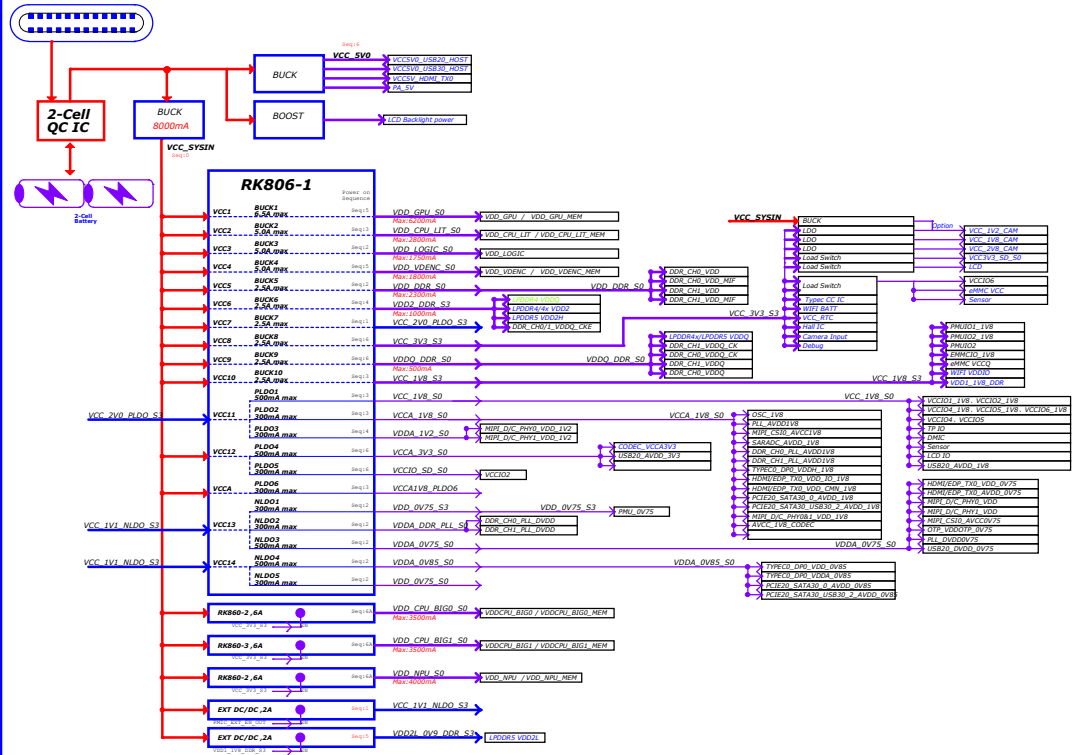
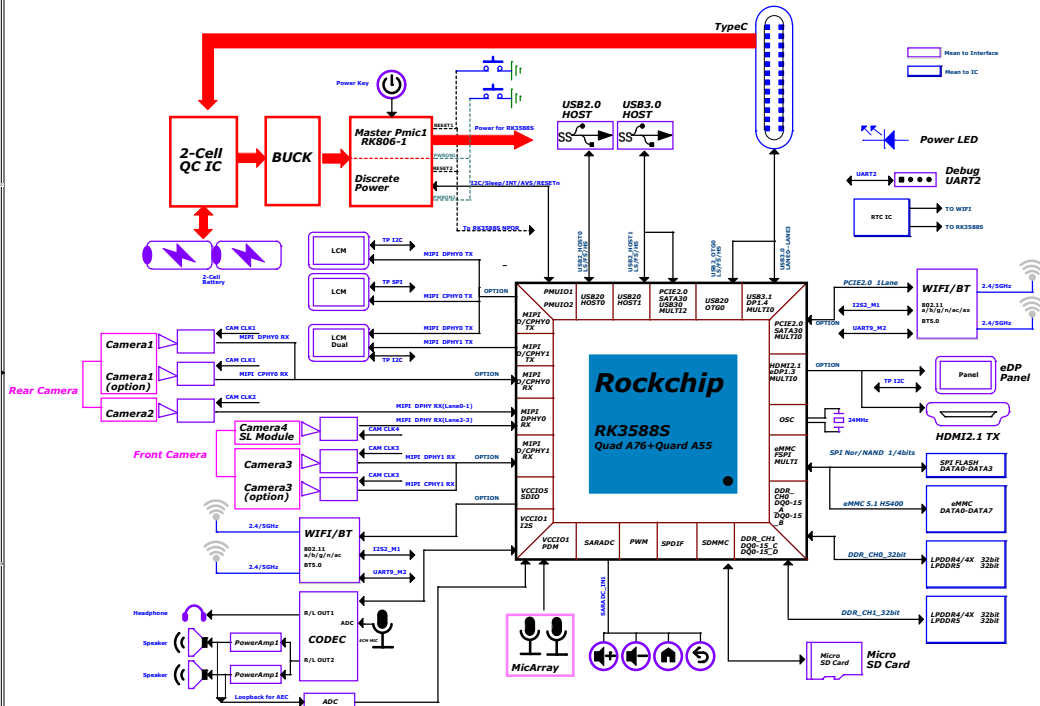


Power tree for 1-Cell Charger

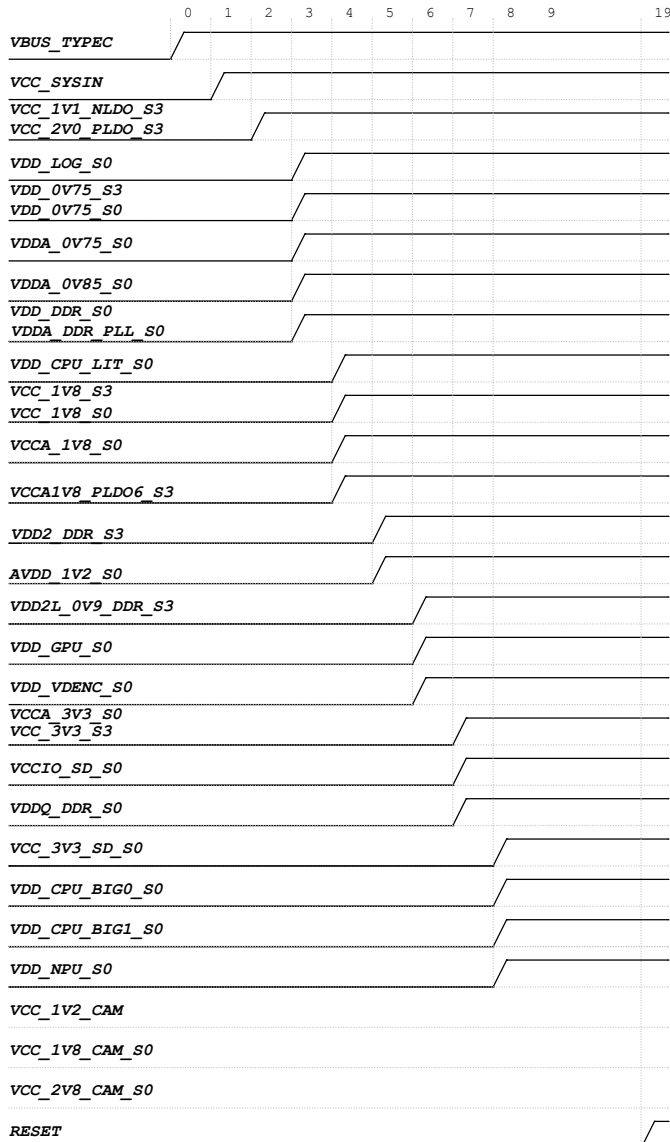


RK3588S Tablet Ref Block Diagram for 2-Cell Charger

Power tree for 2-Cell Charger



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

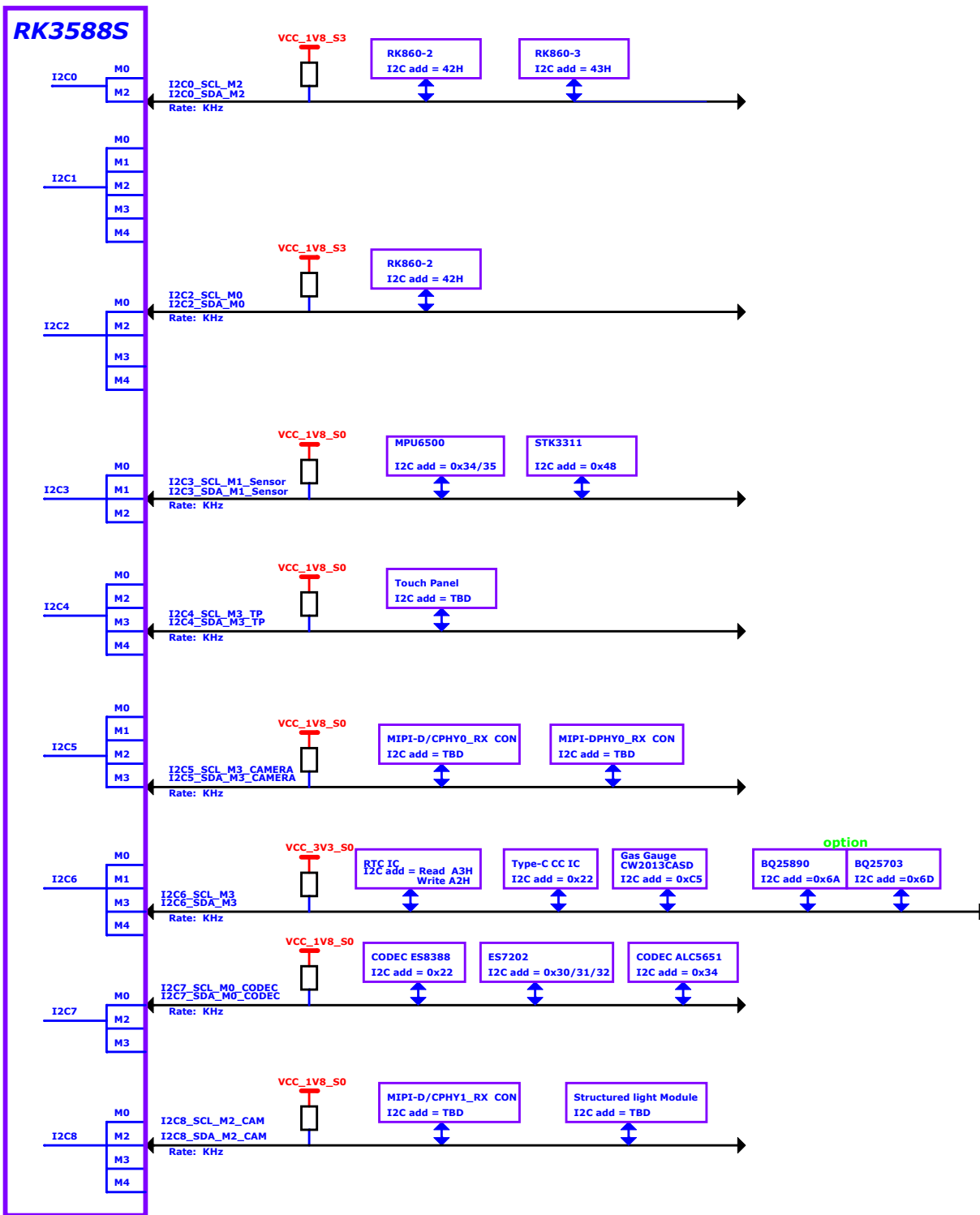
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
	Pin V35 V36		PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin AC35	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
	Pin AC36				
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_IO_SD	1.8V/3.3V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_3V3_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin A134	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin A133 AM33		VCCIO6	VCC_3V3_S0	3.3V

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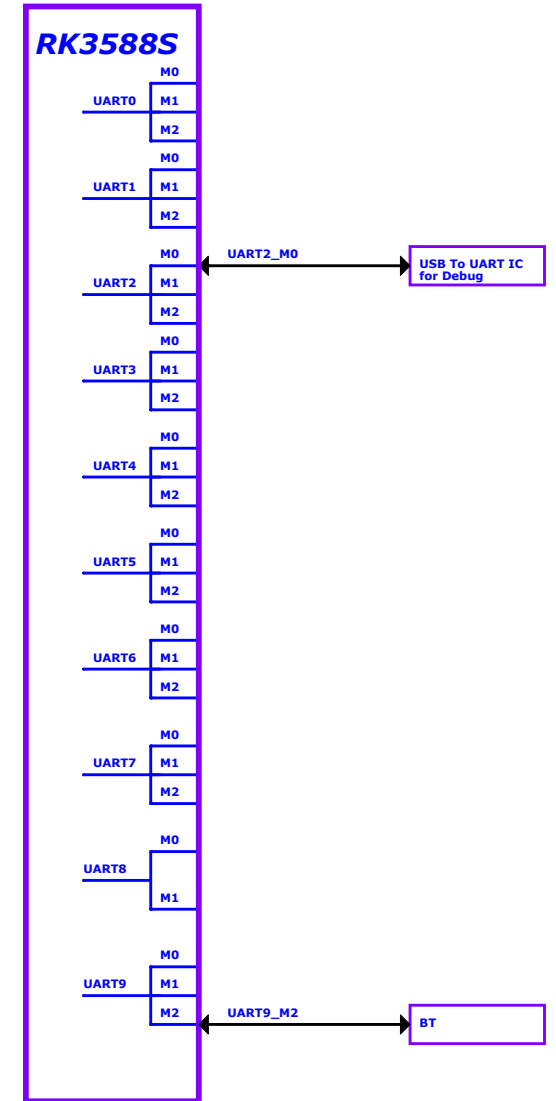
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Project:	RK3588S_Tablet_REF			
File:	05.System Power Sequence			
Date:	Monday, February 21, 2022	Rev:	V10	
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet: 6 of 53

I2C MAP



UART MAP

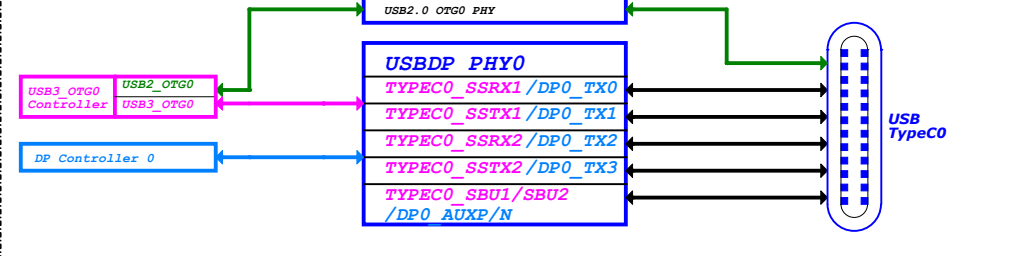


USB Controller Configure Table

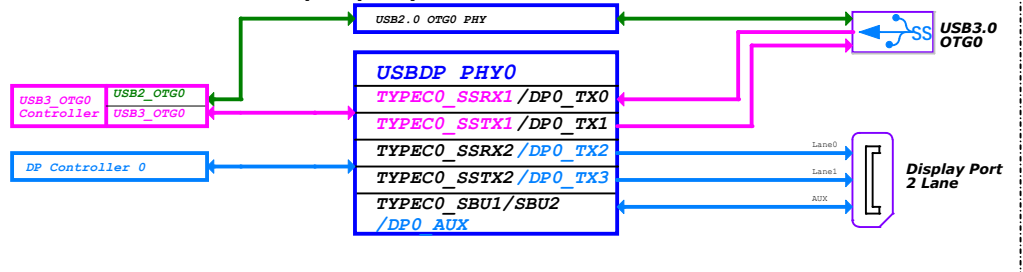
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEPC0_SSRX1/DP0_AUX0	TYPEPC0_SSRX1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEPC0_SSRX1/DP0_TX0P	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P
	TYPEPC0_SSRX1/DP0_TX0N	TYPEPC0_SSRX1N	DP0_TX0N	DP0_TX0N	TYPEPC0_SSRX1N	DP0_TX0N	DP0_TX0N	DP0_TX0N	DP0_TX0N	DP0_TX0N
	TYPEPC0_SSRX1N/DP0_TX1N	TYPEPC0_SSRX1N	DP0_TX1N	DP0_TX1N	TYPEPC0_SSRX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N
USB20 OTG0 Device or Host	TYPEPC0_SSRX2/DP0_TX2P	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSRX2/DP0_TX2N	TYPEPC0_SSRX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSRX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
	TYPEPC0_SSTX2/DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSTX2/DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
USB30 OTG2 Device or Host	PCIE20_2_RXP/SATA30_2_DP0/USB30_2_SSTXP		USB30_2_SSTXP	USB30_2_SSTXP	USB30_2_SSTXP	USB30_2_SSTXP				
	PCIE20_2_RXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXN	USB30_2_SSTXN	USB30_2_SSTXN	USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_DP0/USB30_2_SSRXP		USB30_2_SSRXP	USB30_2_SSRXP	USB30_2_SSRXP	USB30_2_SSRXP				
	PCIE20_2_RXN/SATA30_2_TXN/USB30_2_SSRXN		USB30_2_SSRXN	USB30_2_SSRXN	USB30_2_SSRXN	USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP		USB20_HOST0_DP							
	USB20_HOST0_DM		USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP			USB20_HOST1_DP						
	USB20_HOST1_DM			USB20_HOST1_DM						

Note:
 DP Lane swap enable
 0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
 1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

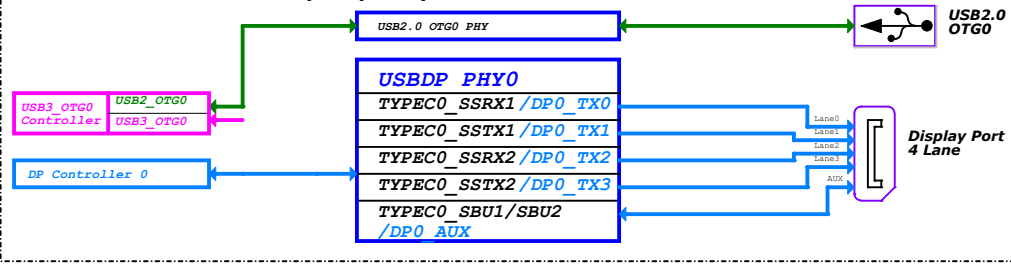
Config0: TypeC0 (With DP function)



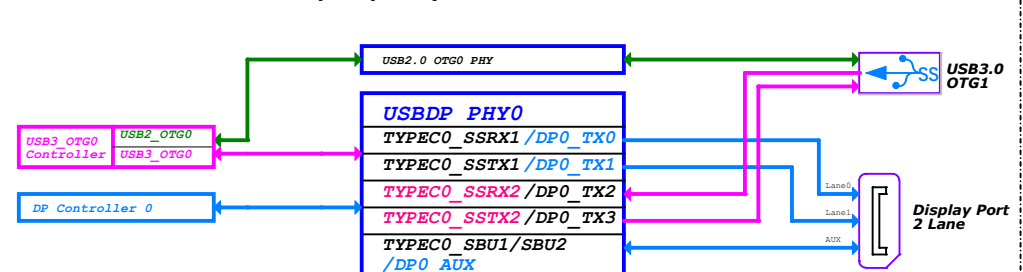
Config3:(Default) USB3.0 OTG0 + DP0 2Lane(Swap ON)



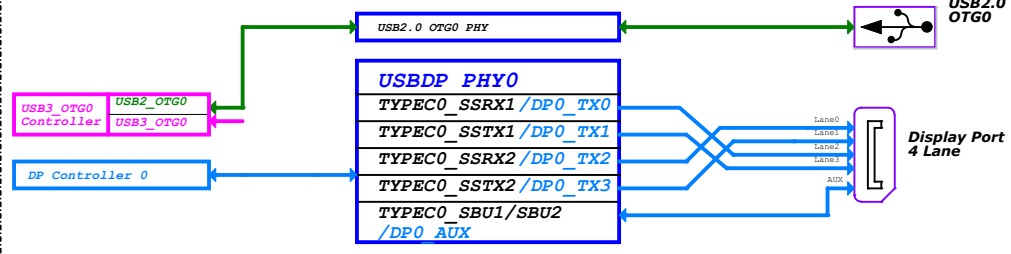
Config1: USB2.0 OTG0 + DP0 4Lane(Swap OFF)



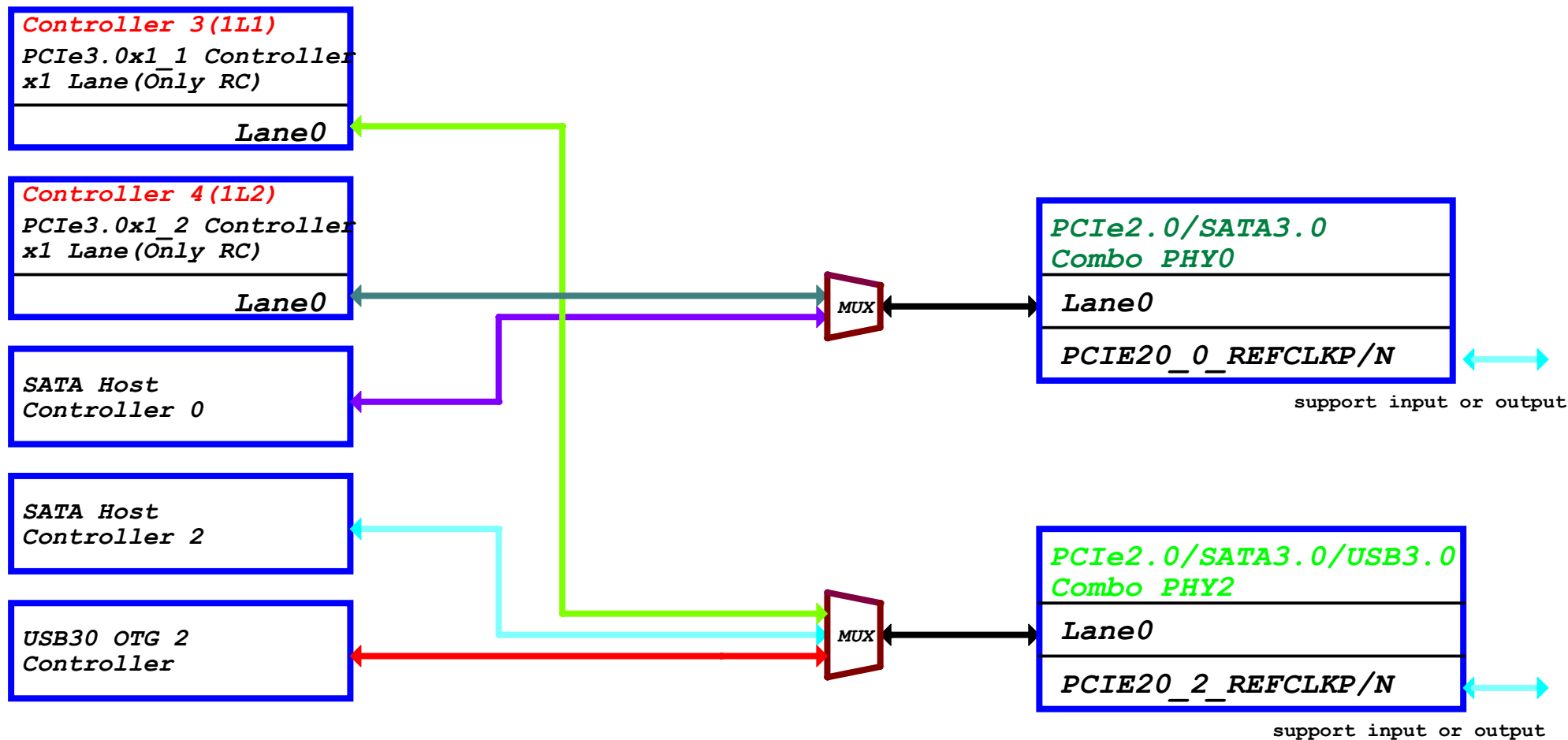
Config4: USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2: USB2.0 OTG0 + DP0 4Lane(Swap ON)



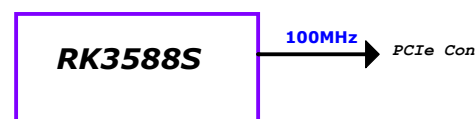
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:
 PCIE20*_REFCLKP/N is output or input gpio
 M*=Mean to M0 or M1 or M2, It's the same source, Just multiplex to M0 or M1 or M2, Only use one at the same time.

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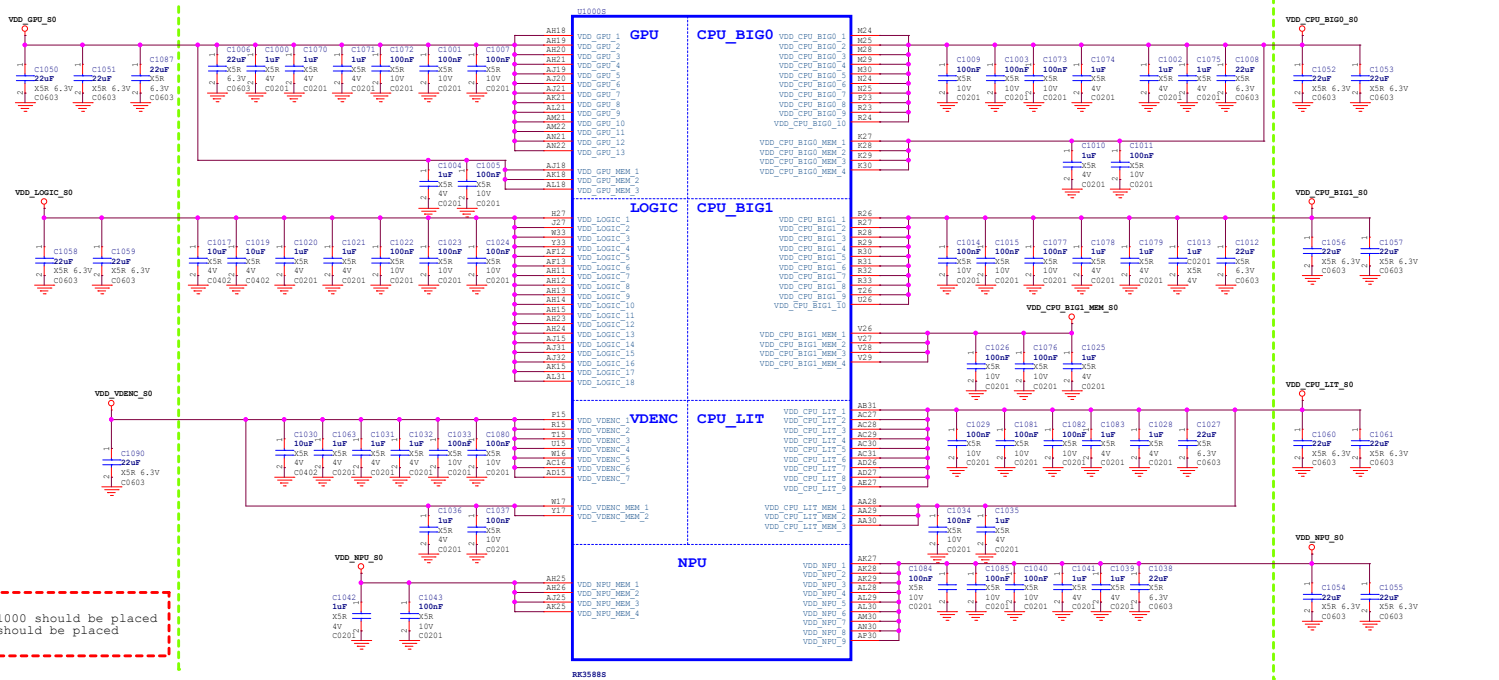
Project: RK3588S_Tablet_REF

File: 08.PCIE Fun Map

Date: Monday, February 21, 2022 Rev: V10

Designed by: Joseph Reviewed by: <Checker> Sheet: 9 of 53

RK3588S (Power&Gnd)



Note:
The Caps between green line and A1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

U1000T		U1000P		U1000V		U1000W		U1000X		U1000Y	
A1_V88_1	V88_101	A2_V88_1	V88_101	B1_V88_1	V88_101	C1_V88_1	V88_101	D1_V88_1	V88_101	E1_V88_1	V88_101
A2_V88_2	V88_102	A2_V88_2	V88_102	B1_V88_2	V88_102	C1_V88_2	V88_102	D1_V88_2	V88_102	E1_V88_2	V88_102
B1_V88_3	V88_103	B1_V88_3	V88_103	C1_V88_3	V88_103	D1_V88_3	V88_103	E1_V88_3	V88_103	F1_V88_3	V88_103
B1_V88_4	V88_104	B1_V88_4	V88_104	C1_V88_4	V88_104	D1_V88_4	V88_104	E1_V88_4	V88_104	F1_V88_4	V88_104
B1_V88_5	V88_105	B1_V88_5	V88_105	C1_V88_5	V88_105	D1_V88_5	V88_105	E1_V88_5	V88_105	F1_V88_5	V88_105
B1_V88_6	V88_106	B1_V88_6	V88_106	C1_V88_6	V88_106	D1_V88_6	V88_106	E1_V88_6	V88_106	F1_V88_6	V88_106
B1_V88_7	V88_107	B1_V88_7	V88_107	C1_V88_7	V88_107	D1_V88_7	V88_107	E1_V88_7	V88_107	F1_V88_7	V88_107
B1_V88_8	V88_108	B1_V88_8	V88_108	C1_V88_8	V88_108	D1_V88_8	V88_108	E1_V88_8	V88_108	F1_V88_8	V88_108
B1_V88_9	V88_109	B1_V88_9	V88_109	C1_V88_9	V88_109	D1_V88_9	V88_109	E1_V88_9	V88_109	F1_V88_9	V88_109
B1_V88_10	V88_110	B1_V88_10	V88_110	C1_V88_10	V88_110	D1_V88_10	V88_110	E1_V88_10	V88_110	F1_V88_10	V88_110
B2_V88_11	V88_111	B2_V88_11	V88_111	C2_V88_11	V88_111	D2_V88_11	V88_111	E2_V88_11	V88_111	F2_V88_11	V88_111
B2_V88_12	V88_112	B2_V88_12	V88_112	C2_V88_12	V88_112	D2_V88_12	V88_112	E2_V88_12	V88_112	F2_V88_12	V88_112
B2_V88_13	V88_113	B2_V88_13	V88_113	C2_V88_13	V88_113	D2_V88_13	V88_113	E2_V88_13	V88_113	F2_V88_13	V88_113
B2_V88_14	V88_114	B2_V88_14	V88_114	C2_V88_14	V88_114	D2_V88_14	V88_114	E2_V88_14	V88_114	F2_V88_14	V88_114
B2_V88_15	V88_115	B2_V88_15	V88_115	C2_V88_15	V88_115	D2_V88_15	V88_115	E2_V88_15	V88_115	F2_V88_15	V88_115
B2_V88_16	V88_116	B2_V88_16	V88_116	C2_V88_16	V88_116	D2_V88_16	V88_116	E2_V88_16	V88_116	F2_V88_16	V88_116
B3_V88_17	V88_117	B3_V88_17	V88_117	C3_V88_17	V88_117	D3_V88_17	V88_117	E3_V88_17	V88_117	F3_V88_17	V88_117
B3_V88_18	V88_118	B3_V88_18	V88_118	C3_V88_18	V88_118	D3_V88_18	V88_118	E3_V88_18	V88_118	F3_V88_18	V88_118
B3_V88_19	V88_119	B3_V88_19	V88_119	C3_V88_19	V88_119	D3_V88_19	V88_119	E3_V88_19	V88_119	F3_V88_19	V88_119
B3_V88_20	V88_120	B3_V88_20	V88_120	C3_V88_20	V88_120	D3_V88_20	V88_120	E3_V88_20	V88_120	F3_V88_20	V88_120
B4_V88_21	V88_121	B4_V88_21	V88_121	C4_V88_21	V88_121	D4_V88_21	V88_121	E4_V88_21	V88_121	F4_V88_21	V88_121
B4_V88_22	V88_122	B4_V88_22	V88_122	C4_V88_22	V88_122	D4_V88_22	V88_122	E4_V88_22	V88_122	F4_V88_22	V88_122
B4_V88_23	V88_123	B4_V88_23	V88_123	C4_V88_23	V88_123	D4_V88_23	V88_123	E4_V88_23	V88_123	F4_V88_23	V88_123
C1_V88_24	V88_124	C1_V88_24	V88_124	D1_V88_24	V88_124	E1_V88_24	V88_124	F1_V88_24	V88_124	G1_V88_24	V88_124
C1_V88_25	V88_125	C1_V88_25	V88_125	D1_V88_25	V88_125	E1_V88_25	V88_125	F1_V88_25	V88_125	G1_V88_25	V88_125
C1_V88_26	V88_126	C1_V88_26	V88_126	D1_V88_26	V88_126	E1_V88_26	V88_126	F1_V88_26	V88_126	G1_V88_26	V88_126
C1_V88_27	V88_127	C1_V88_27	V88_127	D1_V88_27	V88_127	E1_V88_27	V88_127	F1_V88_27	V88_127	G1_V88_27	V88_127
C1_V88_28	V88_128	C1_V88_28	V88_128	D1_V88_28	V88_128	E1_V88_28	V88_128	F1_V88_28	V88_128	G1_V88_28	V88_128
C1_V88_29	V88_129	C1_V88_29	V88_129	D1_V88_29	V88_129	E1_V88_29	V88_129	F1_V88_29	V88_129	G1_V88_29	V88_129
C1_V88_30	V88_130	C1_V88_30	V88_130	D1_V88_30	V88_130	E1_V88_30	V88_130	F1_V88_30	V88_130	G1_V88_30	V88_130
C1_V88_31	V88_131	C1_V88_31	V88_131	D1_V88_31	V88_131	E1_V88_31	V88_131	F1_V88_31	V88_131	G1_V88_31	V88_131
C1_V88_32	V88_132	C1_V88_32	V88_132	D1_V88_32	V88_132	E1_V88_32	V88_132	F1_V88_32	V88_132	G1_V88_32	V88_132
C2_V88_33	V88_133	C2_V88_33	V88_133	D2_V88_33	V88_133	E2_V88_33	V88_133	F2_V88_33	V88_133	G2_V88_33	V88_133
C2_V88_34	V88_134	C2_V88_34	V88_134	D2_V88_34	V88_134	E2_V88_34	V88_134	F2_V88_34	V88_134	G2_V88_34	V88_134
C2_V88_35	V88_135	C2_V88_35	V88_135	D2_V88_35	V88_135	E2_V88_35	V88_135	F2_V88_35	V88_135	G2_V88_35	V88_135
C2_V88_36	V88_136	C2_V88_36	V88_136	D2_V88_36	V88_136	E2_V88_36	V88_136	F2_V88_36	V88_136	G2_V88_36	V88_136
C2_V88_37	V88_137	C2_V88_37	V88_137	D2_V88_37	V88_137	E2_V88_37	V88_137	F2_V88_37	V88_137	G2_V88_37	V88_137
C2_V88_38	V88_138	C2_V88_38	V88_138	D2_V88_38	V88_138	E2_V88_38	V88_138	F2_V88_38	V88_138	G2_V88_38	V88_138
C2_V88_39	V88_139	C2_V88_39	V88_139	D2_V88_39	V88_139	E2_V88_39	V88_139	F2_V88_39	V88_139	G2_V88_39	V88_139
C2_V88_40	V88_140	C2_V88_40	V88_140	D2_V88_40	V88_140	E2_V88_40	V88_140	F2_V88_40	V88_140	G2_V88_40	V88_140
C3_V88_41	V88_141	C3_V88_41	V88_141	D3_V88_41	V88_141	E3_V88_41	V88_141	F3_V88_41	V88_141	G3_V88_41	V88_141
C3_V88_42	V88_142	C3_V88_42	V88_142	D3_V88_42	V88_142	E3_V88_42	V88_142	F3_V88_42	V88_142	G3_V88_42	V88_142
C3_V88_43	V88_143	C3_V88_43	V88_143	D3_V88_43	V88_143	E3_V88_43	V88_143	F3_V88_43	V88_143	G3_V88_43	V88_143
C3_V88_44	V88_144	C3_V88_44	V88_144	D3_V88_44	V88_144	E3_V88_44	V88_144	F3_V88_44	V88_144	G3_V88_44	V88_144
C3_V88_45	V88_145	C3_V88_45	V88_145	D3_V88_45	V88_145	E3_V88_45	V88_145	F3_V88_45	V88_145	G3_V88_45	V88_145
C3_V88_46	V88_146	C3_V88_46	V88_146	D3_V88_46	V88_146	E3_V88_46	V88_146	F3_V88_46	V88_146	G3_V88_46	V88_146
C3_V88_47	V88_147	C3_V88_47	V88_147	D3_V88_47	V88_147	E3_V88_47	V88_147	F3_V88_47	V88_147	G3_V88_47	V88_147
C3_V88_48	V88_148	C3_V88_48	V88_148	D3_V88_48	V88_148	E3_V88_48	V88_148	F3_V88_48	V88_148	G3_V88_48	V88_148
C3_V88_49	V88_149	C3_V88_49	V88_149	D3_V88_49	V88_149	E3_V88_49	V88_149	F3_V88_49	V88_149	G3_V88_49	V88_149
C3_V88_50	V88_150	C3_V88_50	V88_150	D3_V88_50	V88_150	E3_V88_50	V88_150	F3_V88_50	V88_150	G3_V88_50	V88_150

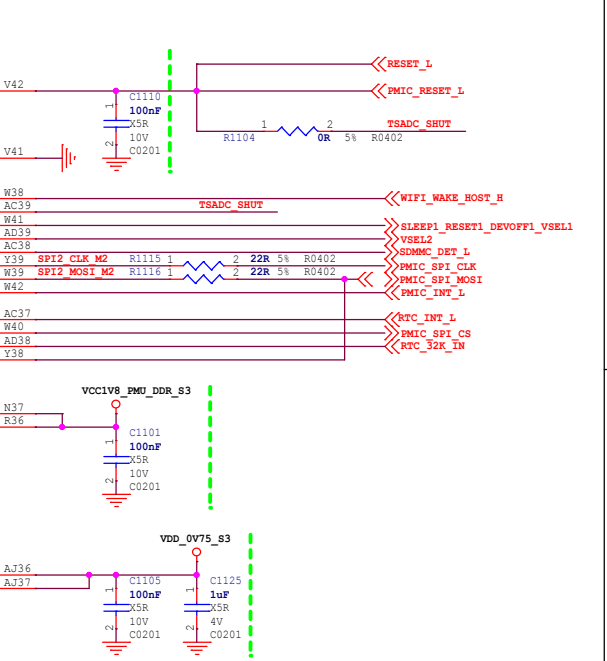
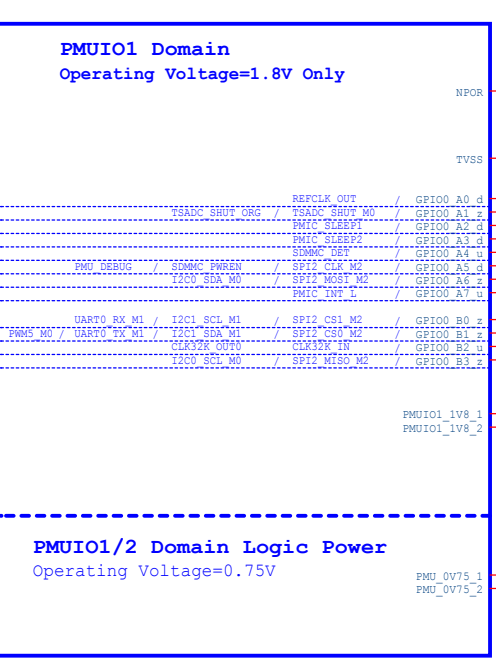
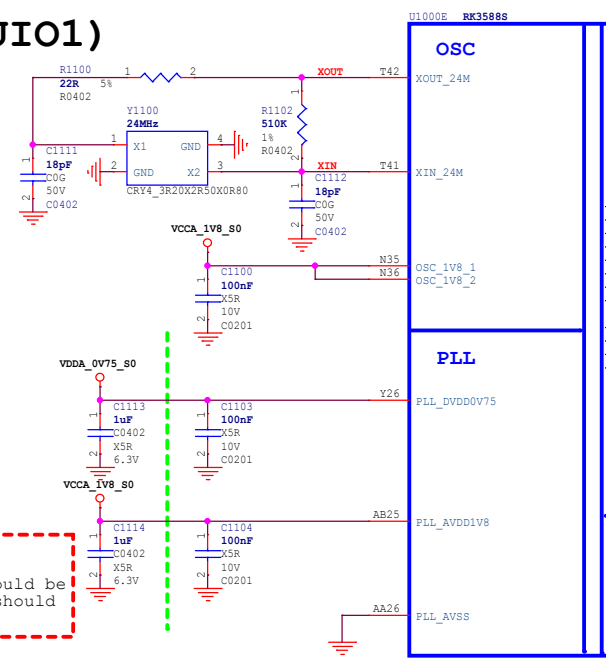
RK3588S (OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

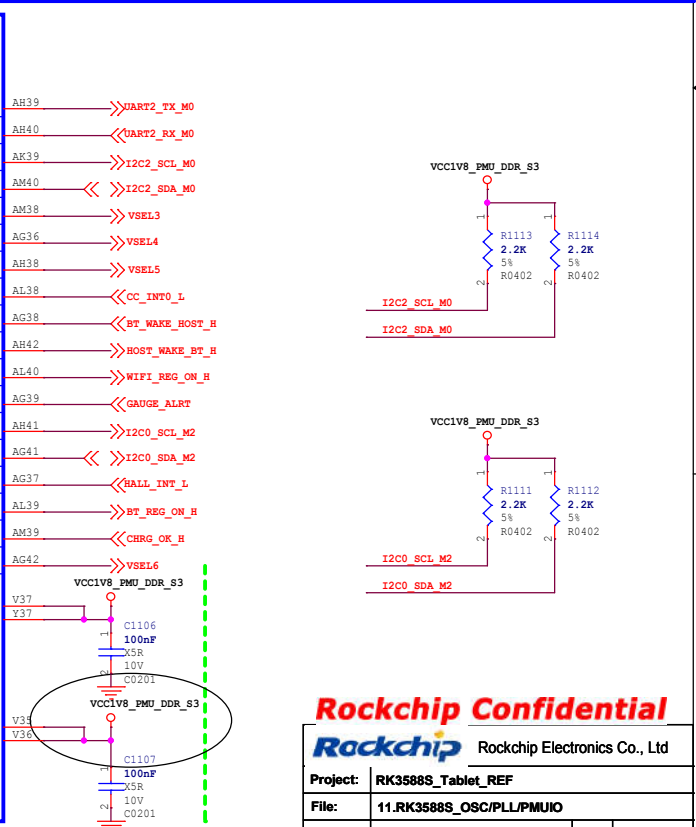
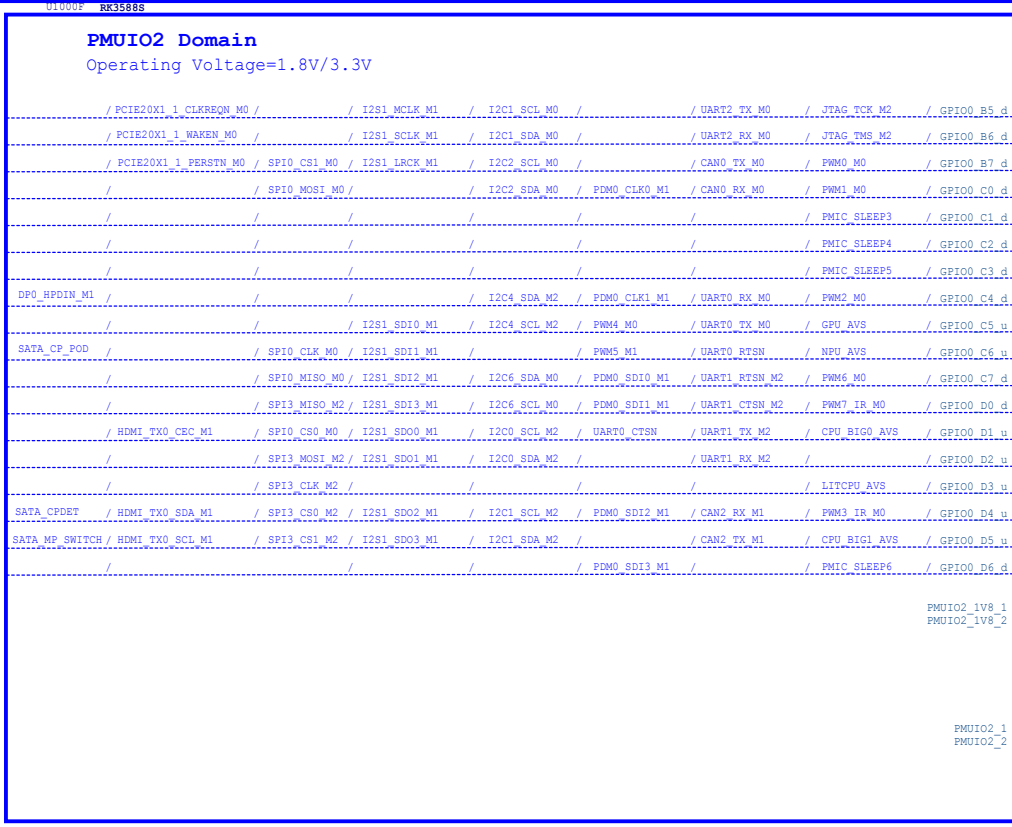
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$
Total CL=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



RK3588S (PMUIO2)

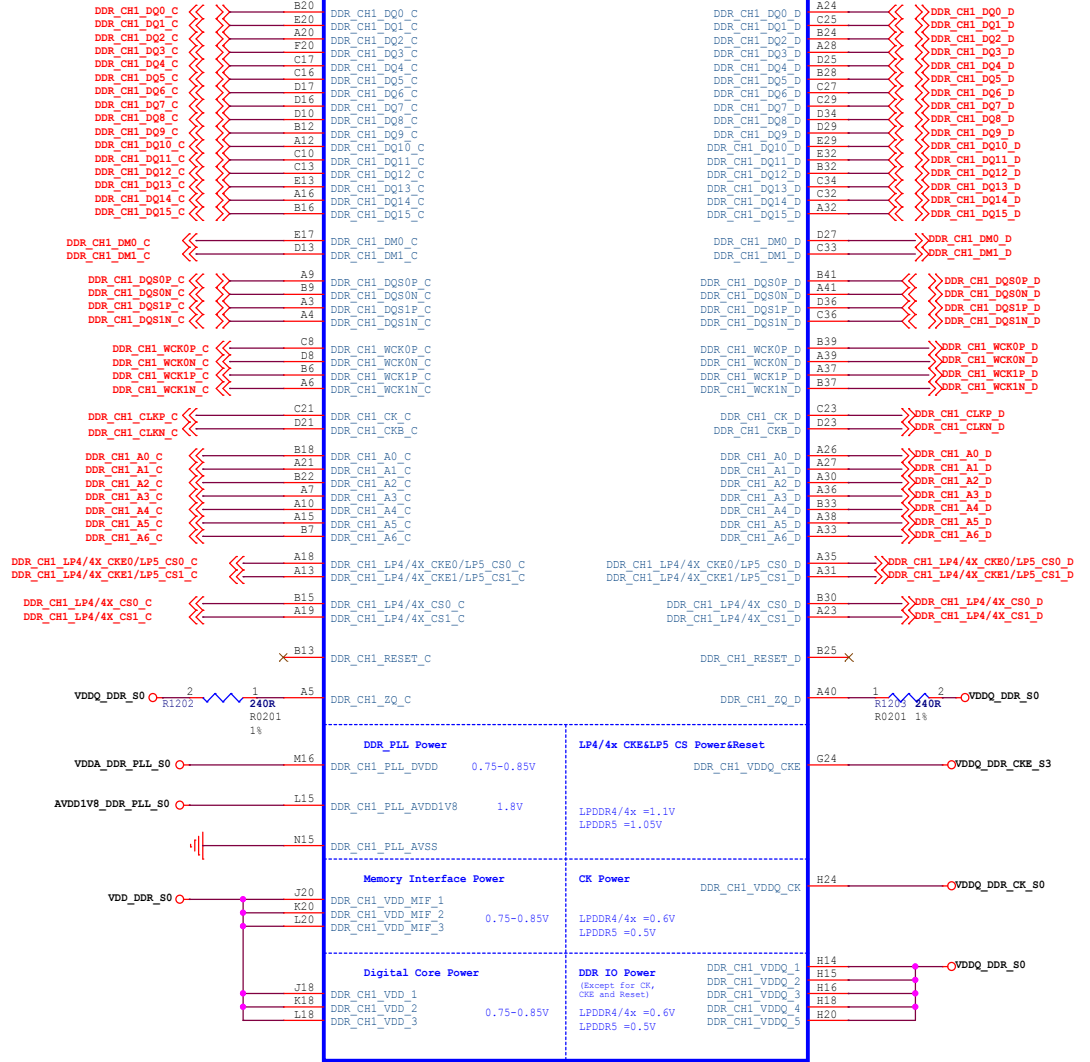


RK3588S (DDR PHY)

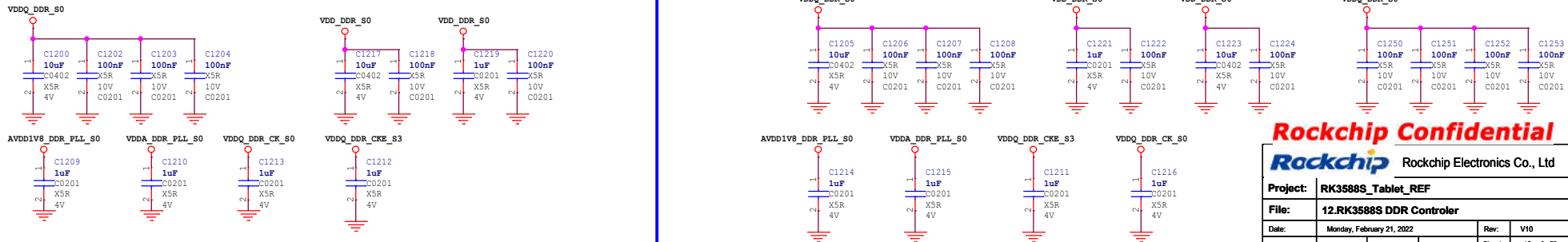
U1000A RK3588S



U1000B RK3588S



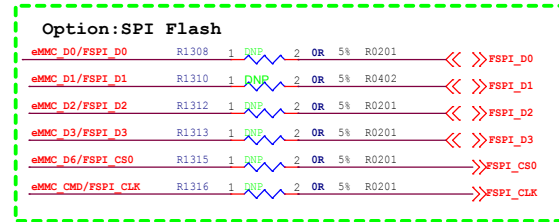
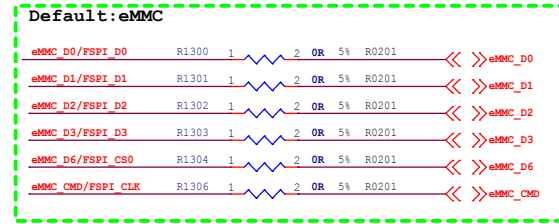
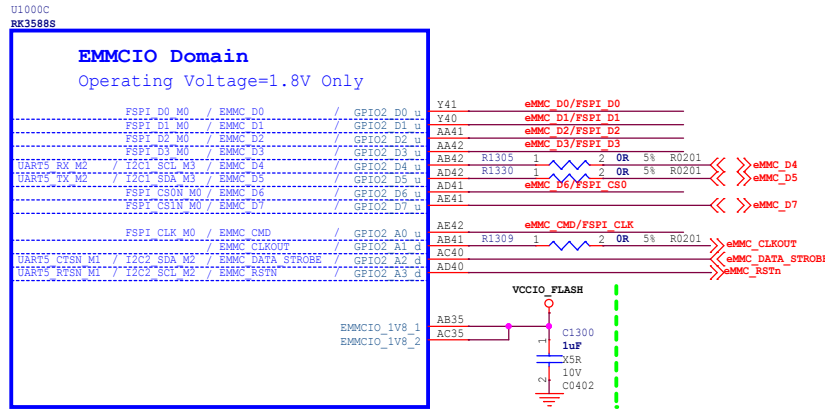
DDR FILTER



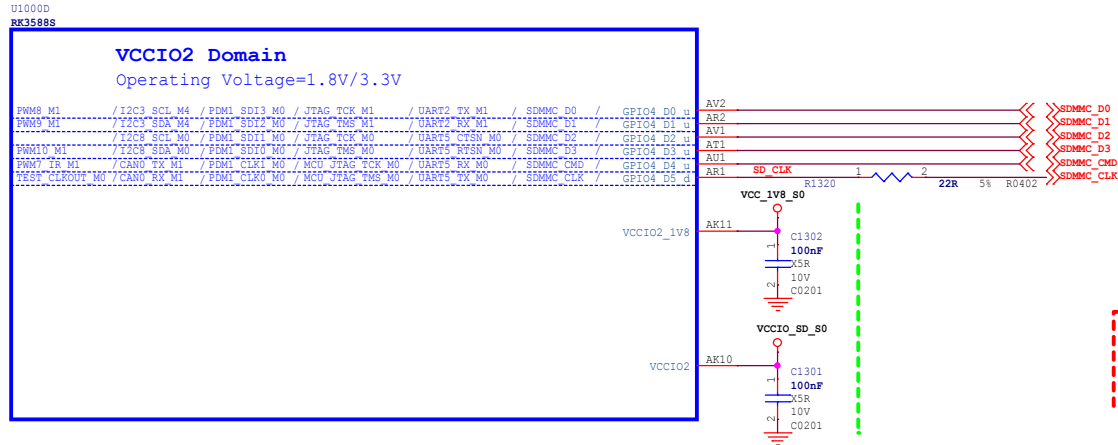
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Project:	RK3588S_Tablet_REF		
File:	12.RK3588S DDR Controller		
Date:	Monday, February 21, 2022	Sheet:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Rev:	12 of 53

RK3588S (EMMCIO Domain)



RK3588S (VCCIO2 Domain)



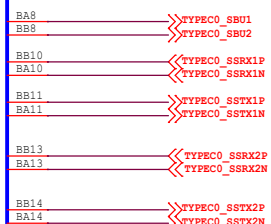
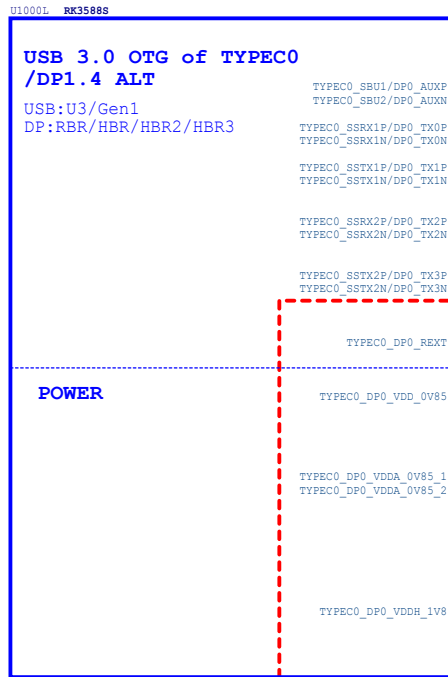
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (USB3.0/DP1.4)

USB30/DP1.4 Alt Mode Configuration

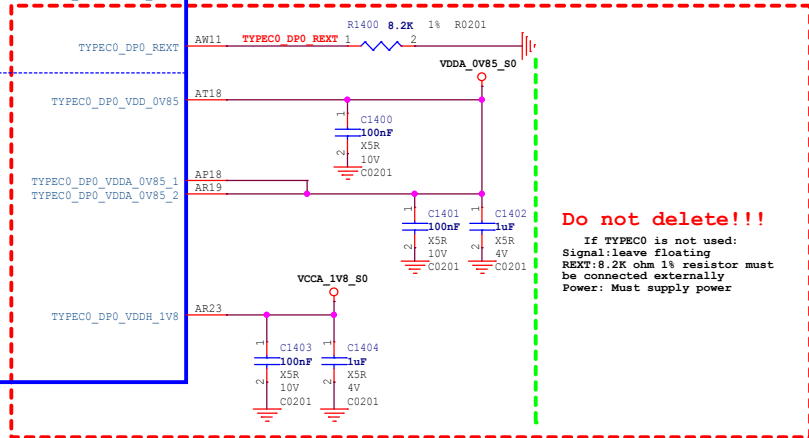
Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP: Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

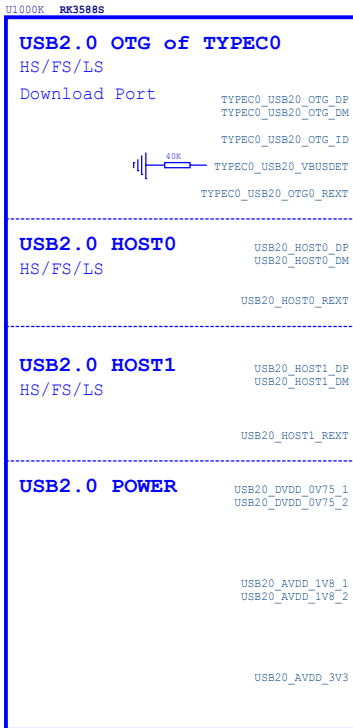


TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +/-10%
For Typec

USB30 Differential Pair: DATE:90 Ohm +/-10%
DP Differential Pair: DATE:100 Ohm +/-10%
For USB30 For DP



RK3588S (USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPECO_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

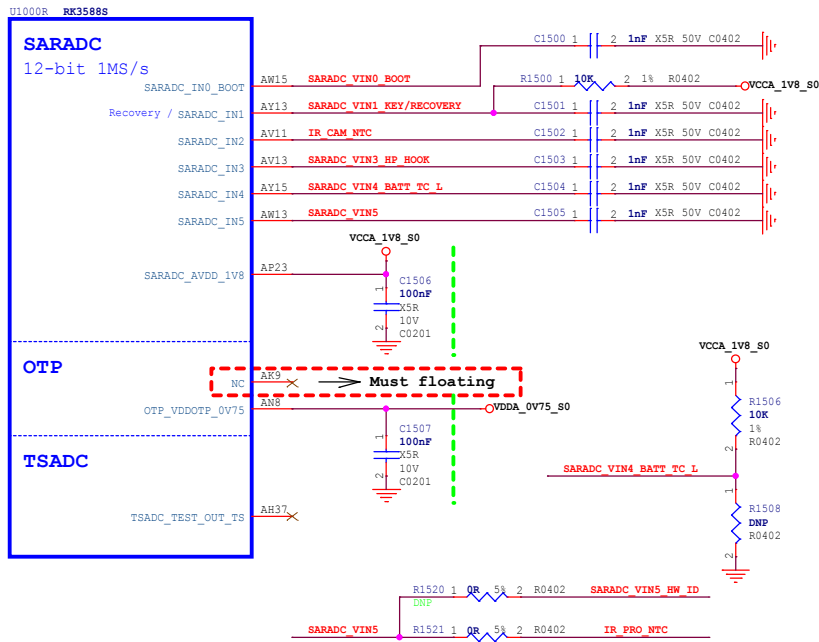
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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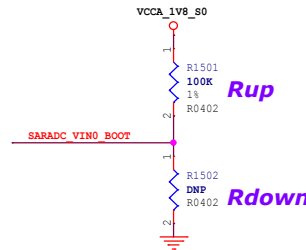
Project:	RK3588S_Tablet_REF
File:	14.RK3588S_USB20/USB30/DP_PHY
Date:	Monday, February 21, 2022
Designed by:	Joseph
Reviewed by:	<Checker>
Rev:	V10
Sheet:	14 of 53

RK3588S (SARADC/OTP/TSADC)

- < SARADC_VIN1_KEY/RECOVERY
- < IR_CAM_NTC
- < SARADC_VIN3_HP_HOOK
- < SARADC_VIN4_BATT_TC_L
- < SARADC_VIN0_BOOT
- < IR_PRO_NTC
- < IR_CAM_NTC

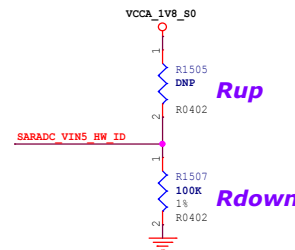


BOOT MODE CONFIG



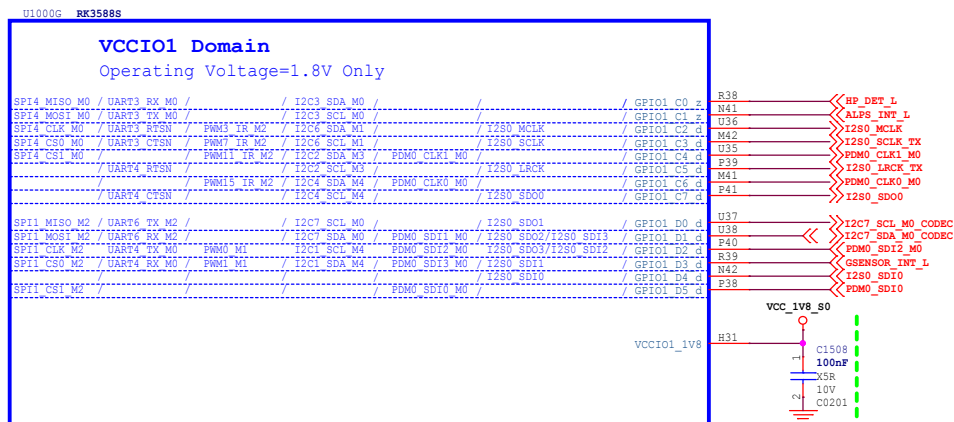
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI M2-FSPI M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S (VCCIO1 Domain)

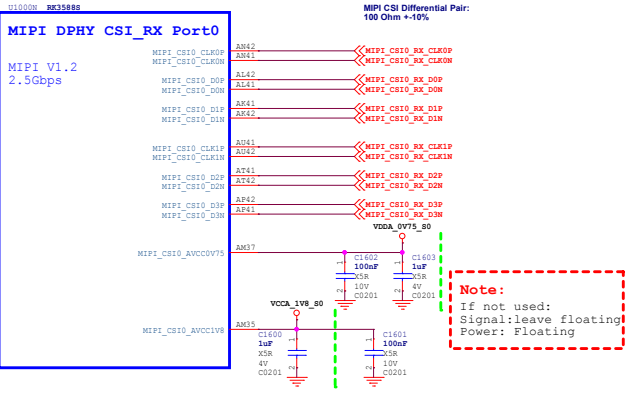


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Project: RK3588S_Tablet_REF
File: 15.RK3588S_SARADC1.8V GPIO
Date: Monday, February 21, 2022
Designed by: Joseph
Reviewed by: <Checker>
Rev: V10
Sheet: 15 of 53

RK3588S (MIPI_DPHY CSIO RX)



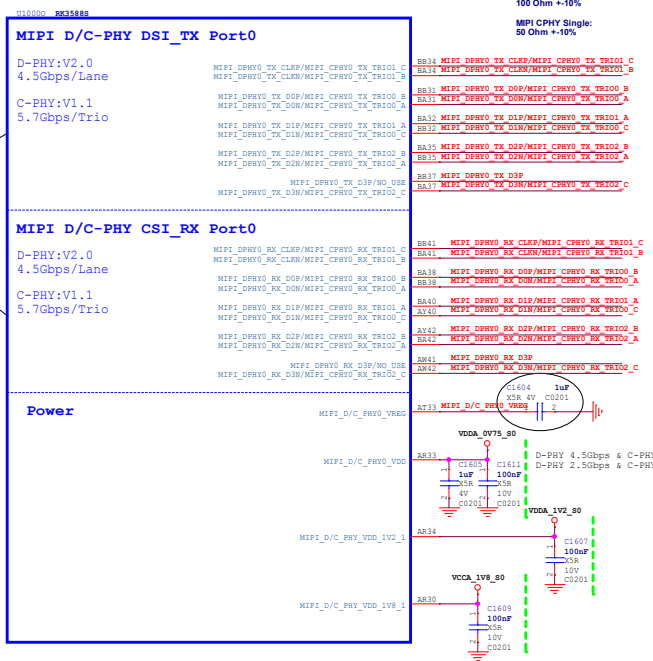
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

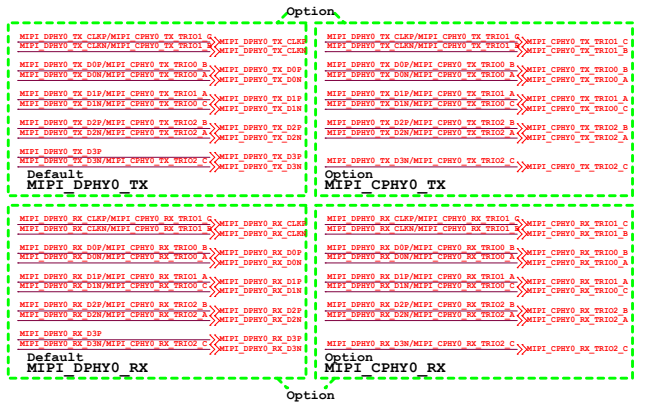
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (MIPI_D/C PHY0)



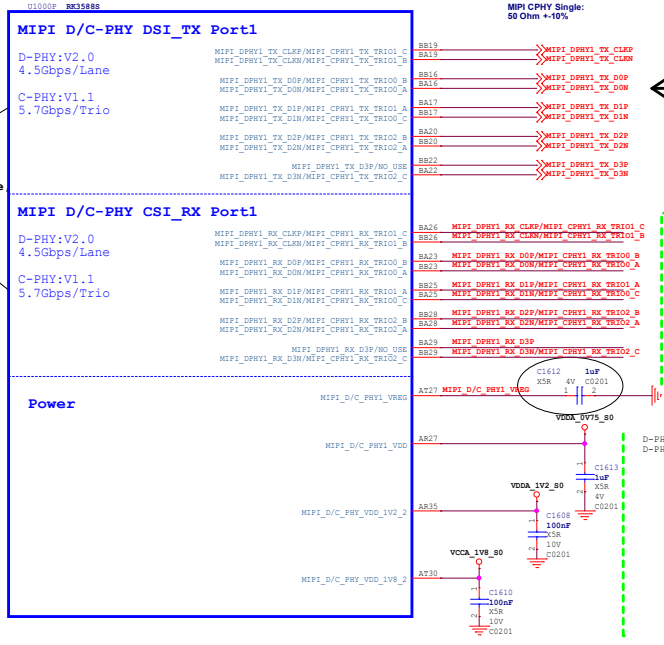
TX and RX port must work in the same mode, DPHY or CPHY

TX and RX port must work in the same mode DPHY or CPHY

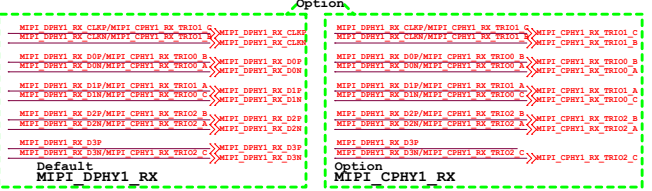


Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S (MIPI_D/C PHY1)



Note:
The Port also support MIPI CPHY1 TX, if need please Refer to the circuit of MIPI_CPHY0_TX

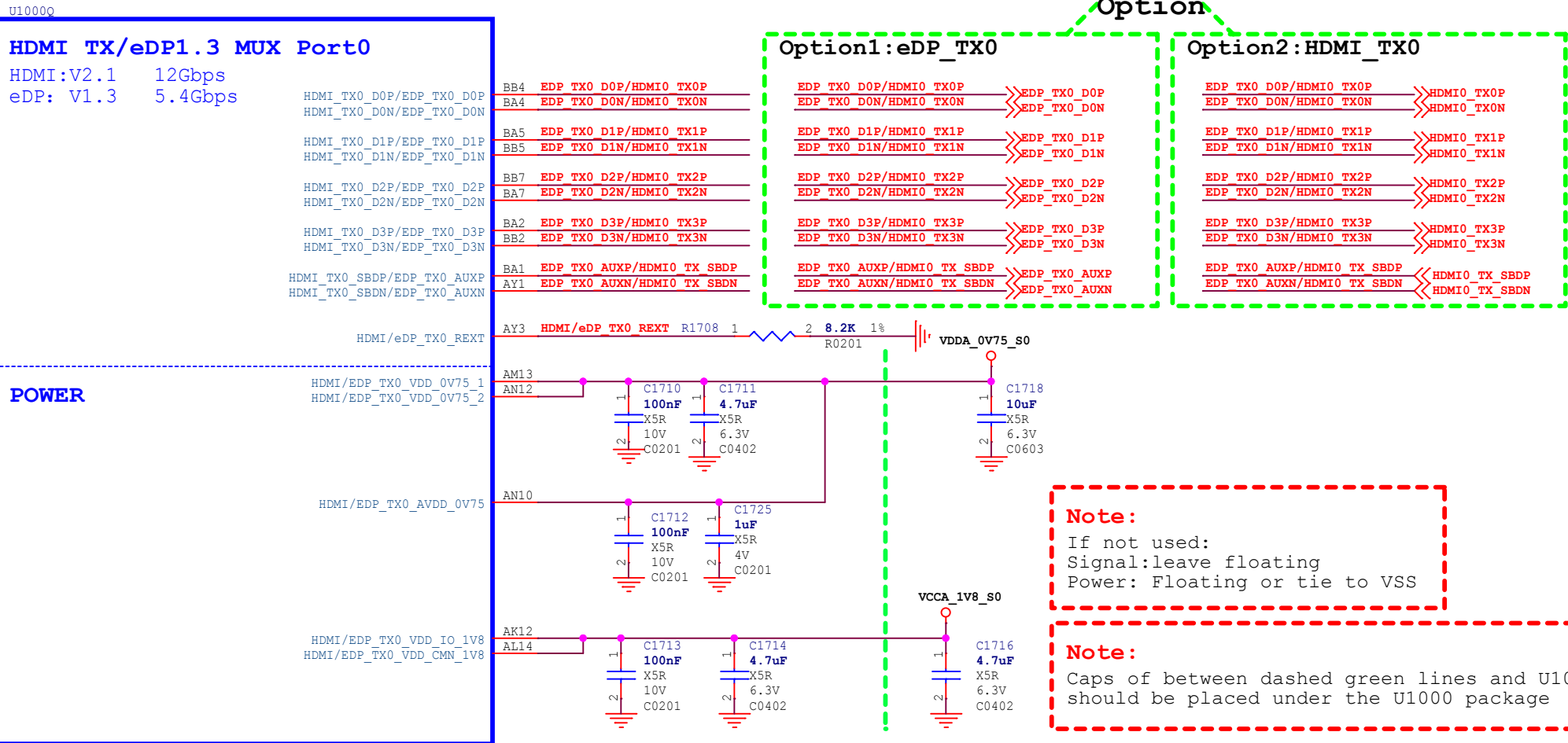


Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S (HDMI2.1 TX/eDP1.3 TX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



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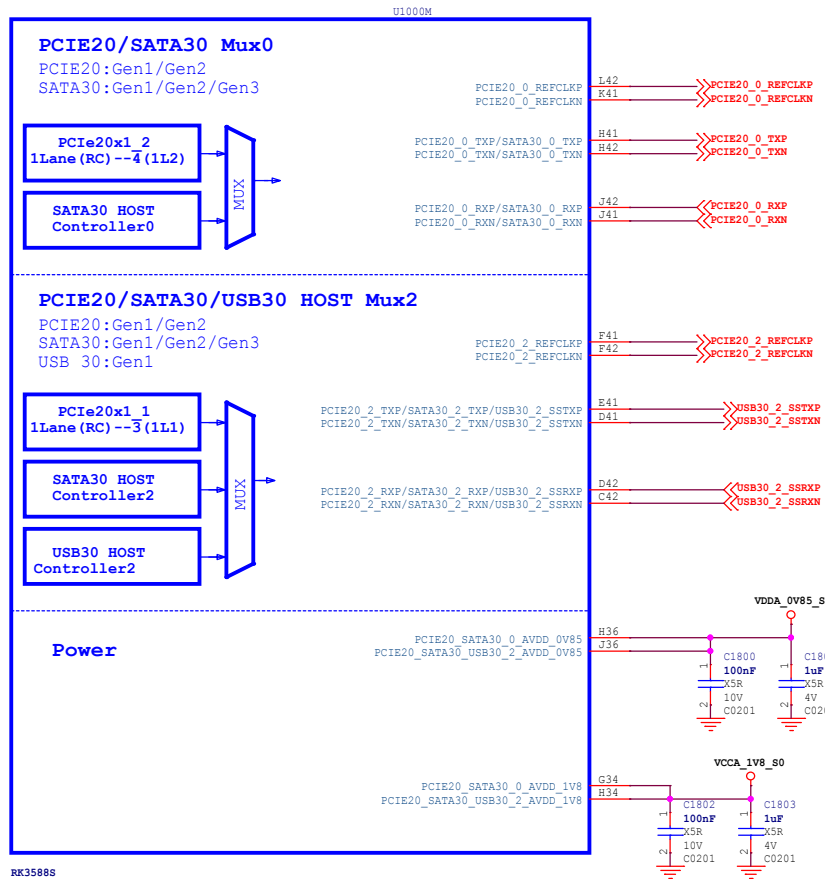
Project: RK3588S_Tablet_REF

File: 17.RK3588S_HDMI/eDP Interface

Date: Monday, February 21, 2022 **Rev:** V10

Designed by: Joseph **Reviewed by:** <Checker> **Sheet:** 17 of 53

RK3588S (PCIE20/SATA30/USB30)



CLK Differential Pair:
 100 Ohm±10%
DATA Differential Pair:
 PCIE20: 85 Ohm±10%
 SATA30: 100 Ohm±10%
 USB30: 90ohm±10%

Note:
 If not used:
 Signal:leave floating
 Power: Tie to VSS

Note:
 Caps of between dashed green lines and U1000
 should be placed under the U1000 package

PCIE2.0 PHY

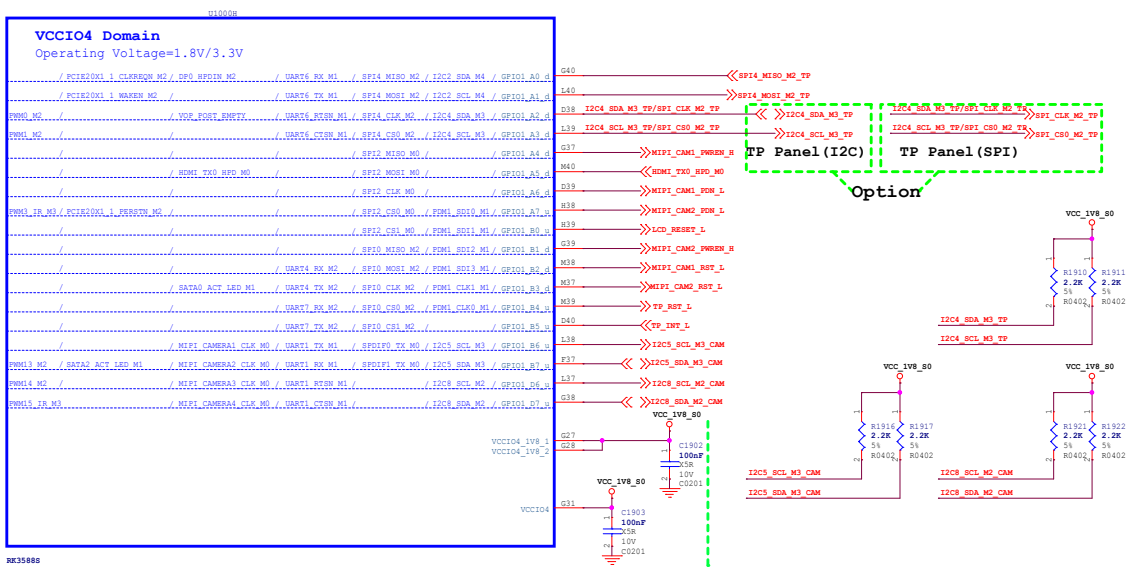
Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

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Project:	RK3588S_Tablet_REF		
File:	18.RK3588S_PCIE2/SATA3/USB3_PHY		
Date:	Tuesday, April 12, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker> Sheet: 18 of 53

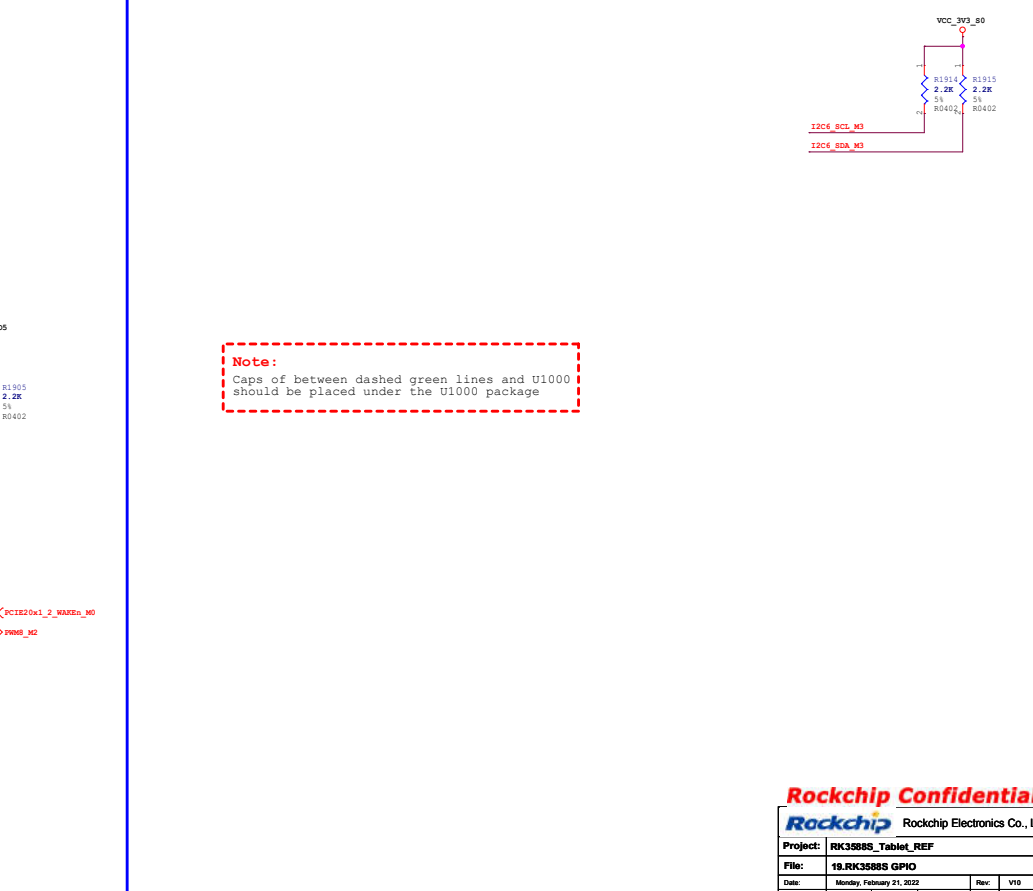
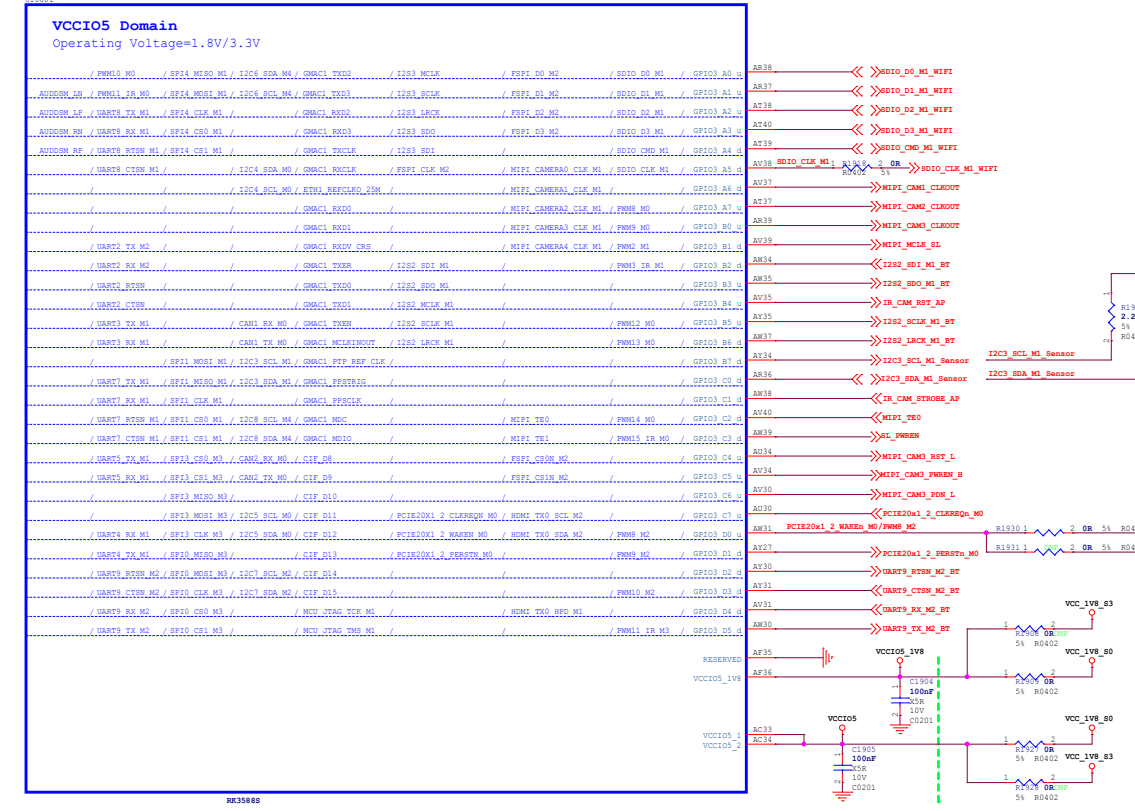
RK3588S (VCCIO4 Domain)



RK3588S (VCCIO6 Domain)



RK3588S (VCCIO5 Domain)



PMIC RK806-1



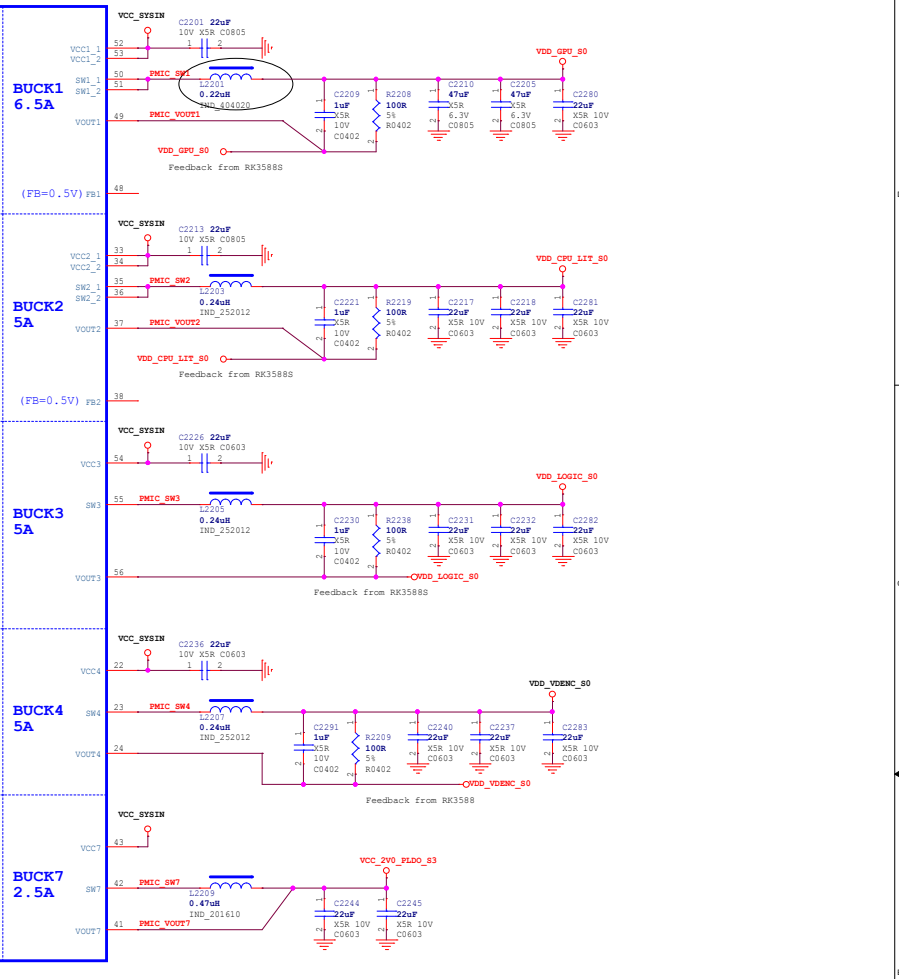
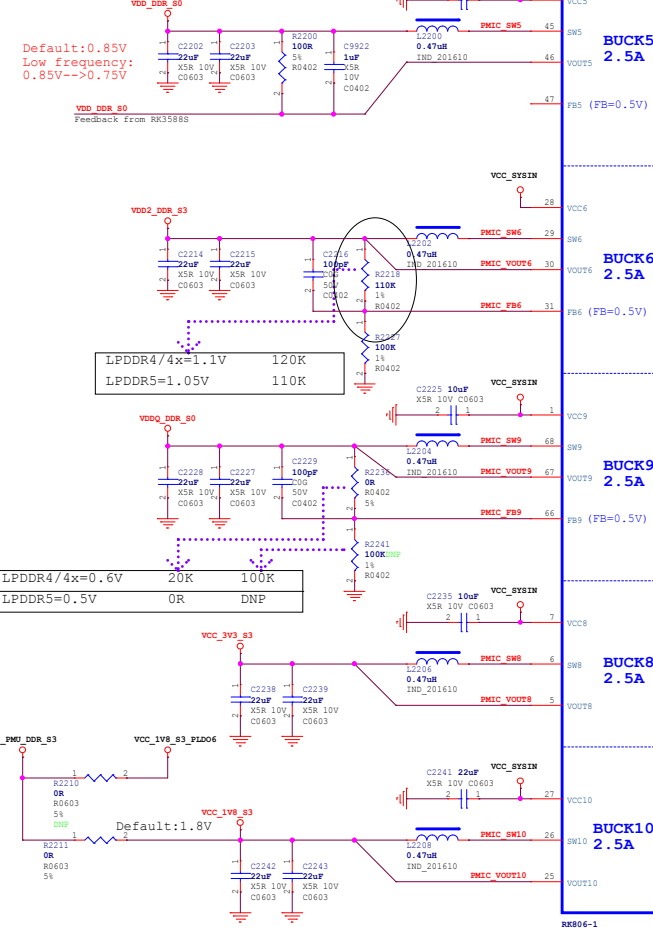
IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted. Replacing TVS mode is not recommended. If must, please choose the same specifications
 Operating Supply Voltage: ± 5V(0.25-0V)
 PeakPulse Current: >10A (tpr<20us)
 Surge Clamping Voltage: <6.5V

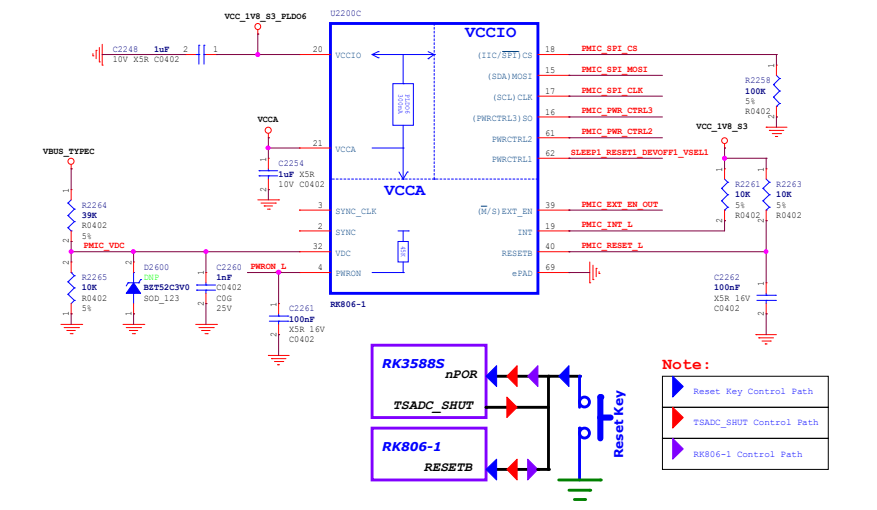
DO NOT DELETE IT!



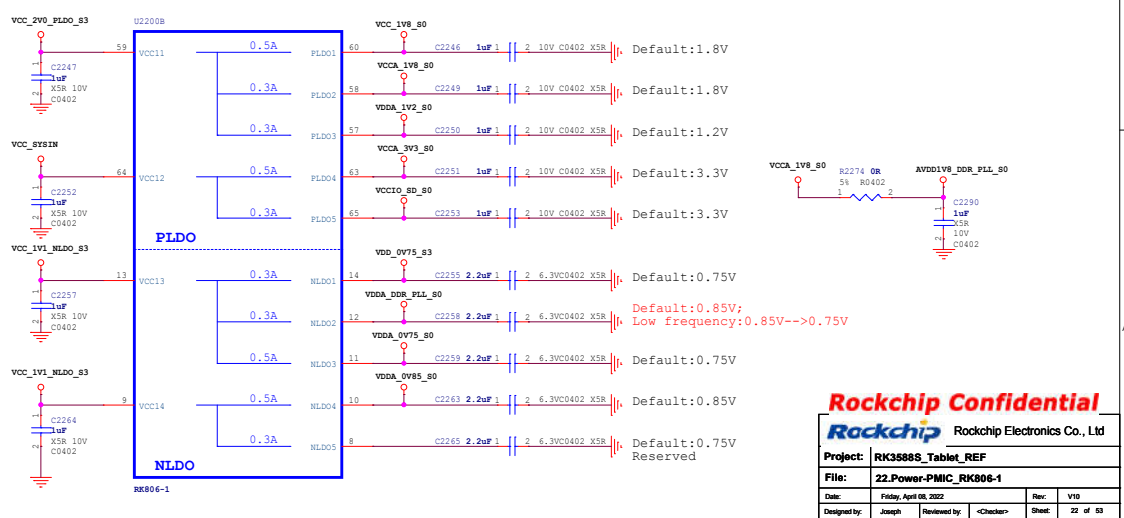
PMIC RK806-1 BUCK



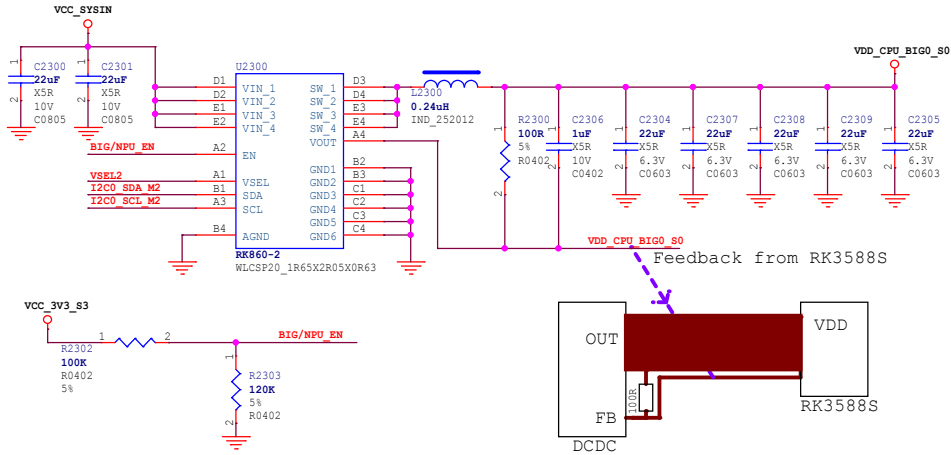
PMIC RK806-1 Management



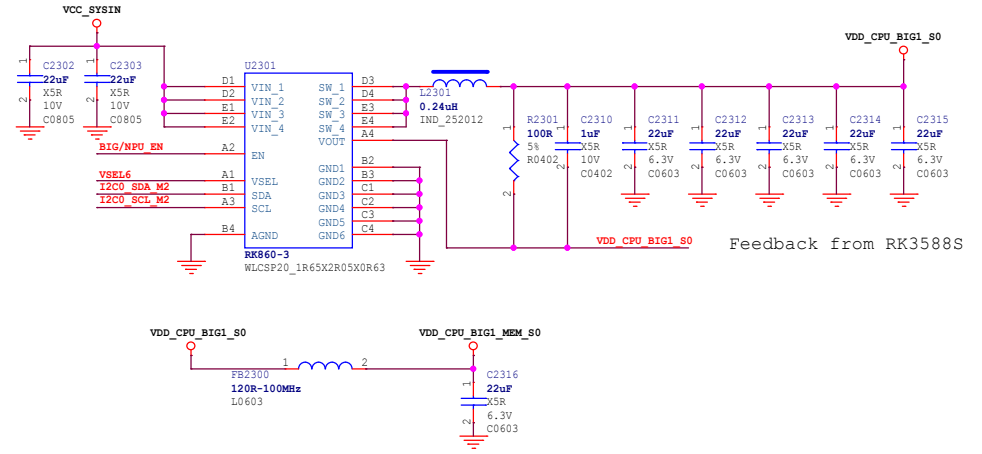
PMIC RK806-1 LDO



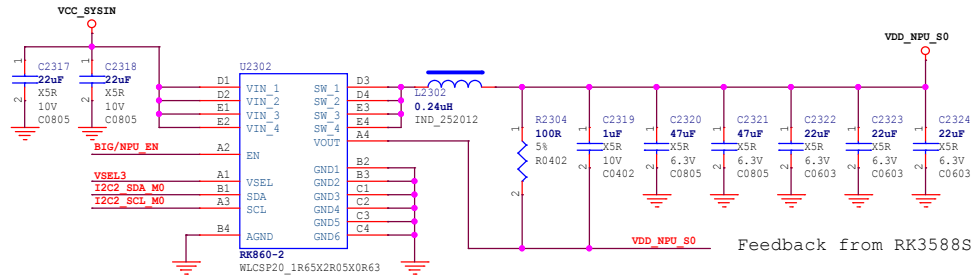
VDD_CPU_BIG0



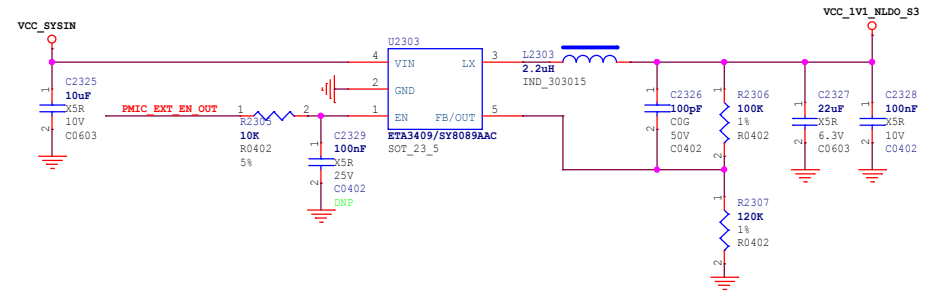
VDD_CPU_BIG1



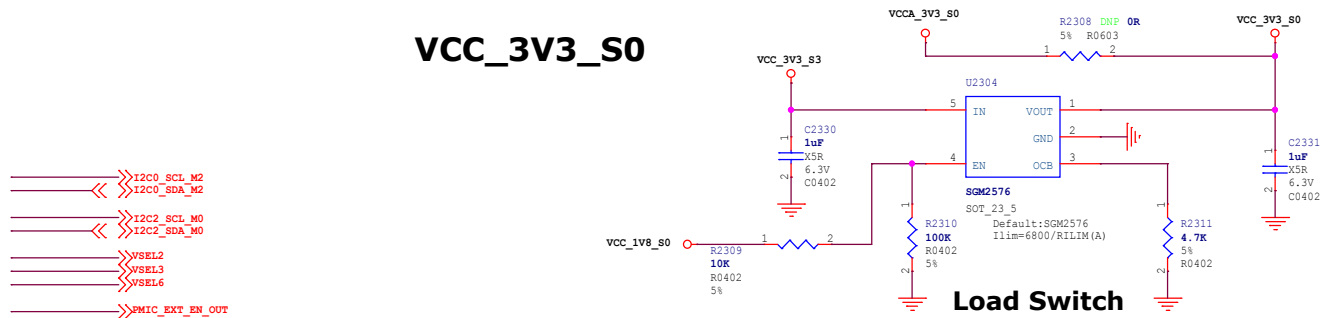
VDD_NPU



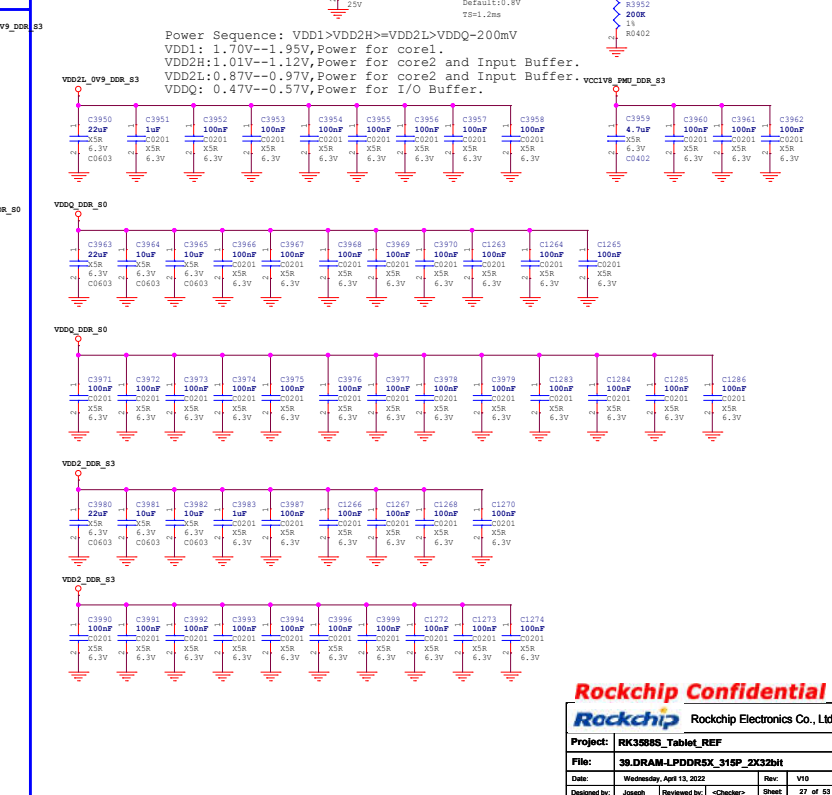
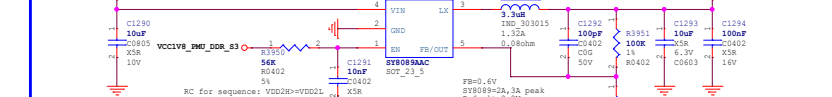
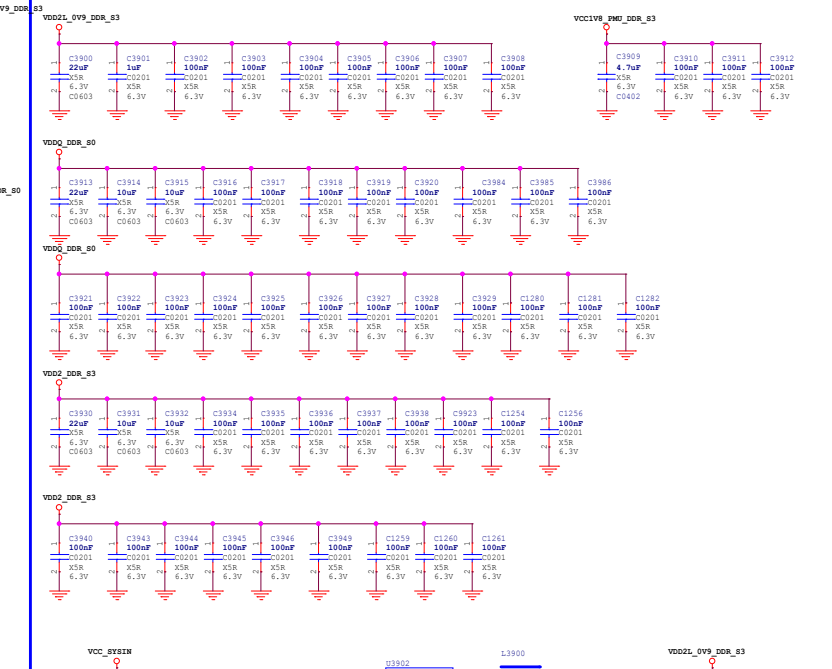
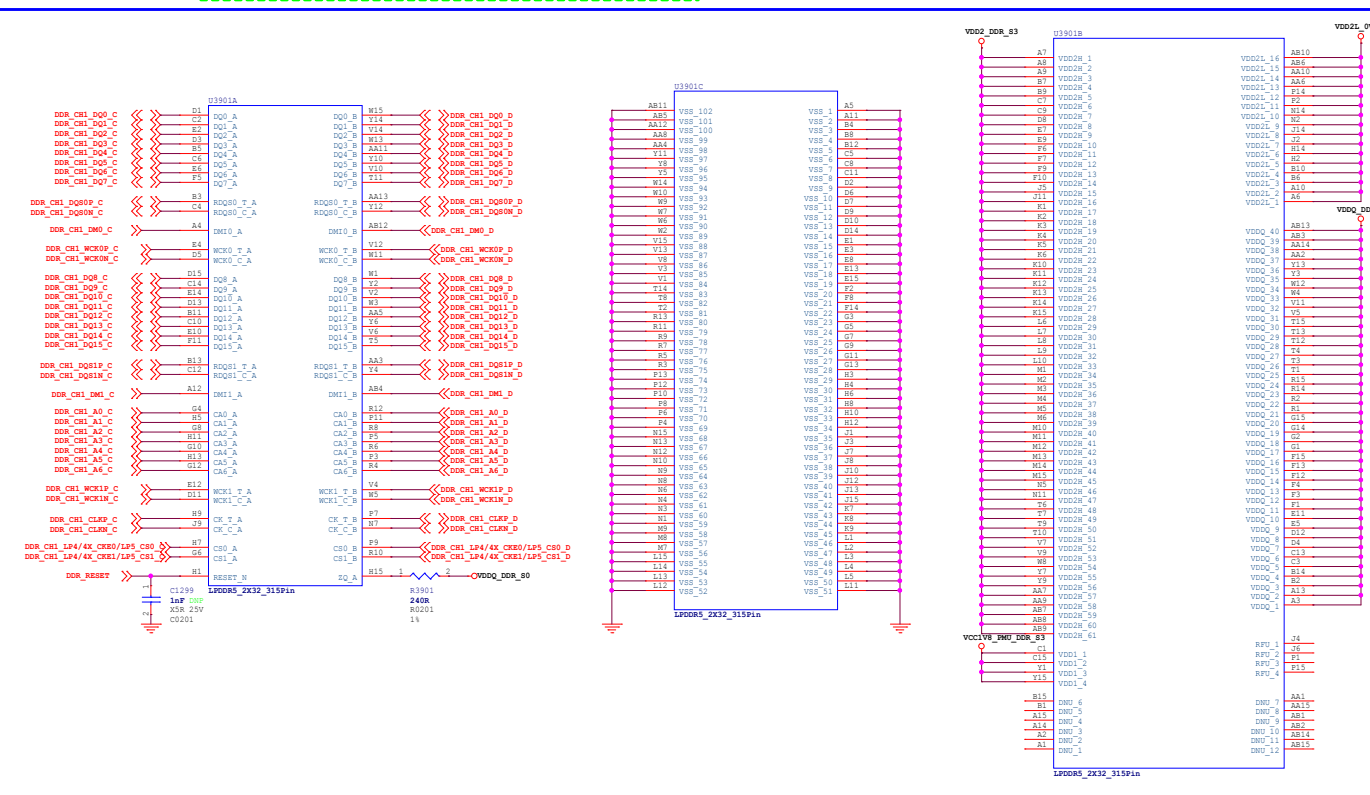
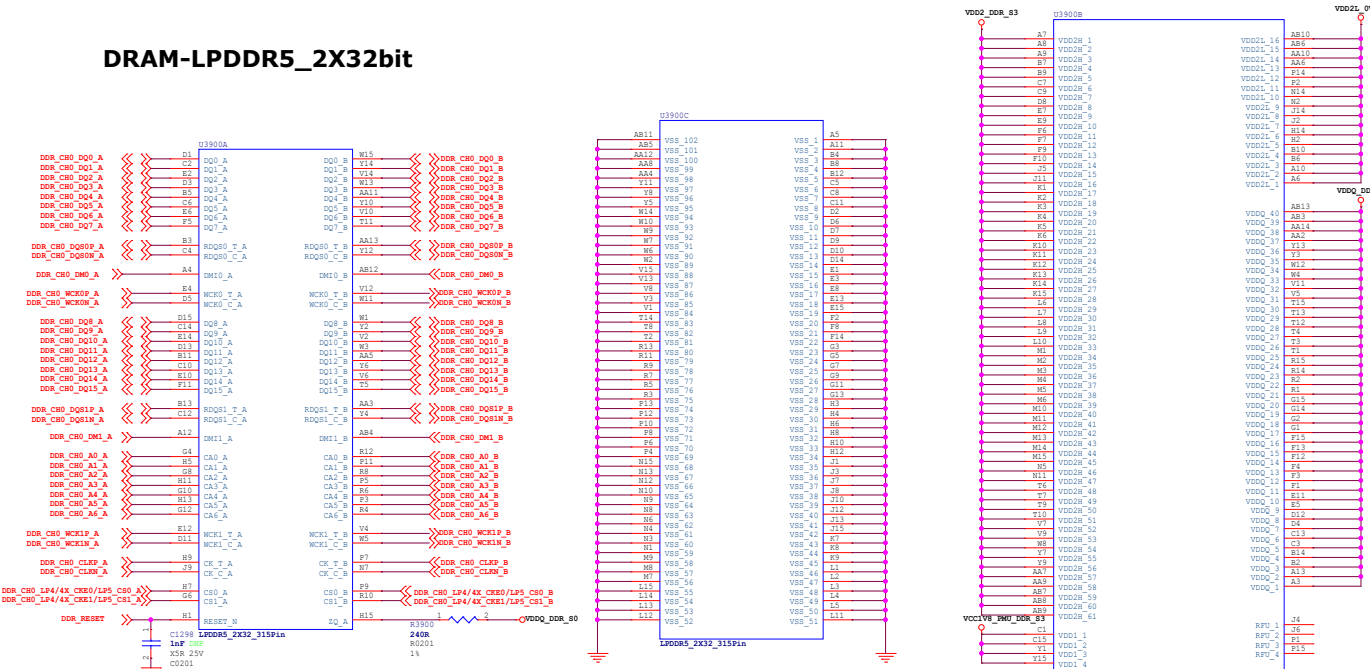
VCC_1V1_NLDO



VCC_3V3_S0



DRAM-LPDDR5_2X32bit



Power Sequence: VDD1=1.70V-1.95V, Power for Core1.
VDD2H: 1.01V-1.12V, Power for Core2 and Input Buffer.
VDDQ: 0.87V-0.97V, Power for Core2 and Input Buffer.
VDDQ: 0.47V-0.57V, Power for I/O Buffer.