



RK3588S EVB

User Guide

发布版本:V1.1

日期:2022-4-14

Disclaimer

This document is provided "status quo", Rockchip Electronics Co., Ltd. ("the company", the same below) does not make any statements, information and content of this document on the accuracy, reliability, completeness, marketability, or specific purpose and non-infringement provide any express or implied statement or guarantee. This document is only used as a reference for instructions.

Due to product version upgrades or other reasons, this document will be updated aperiodic. Unless otherwise agreed, this document is only used as a guide. All statements, information and suggestions in this document do not constitute any express or implied warranty.

Brand Statement

"Rockchip" and "瑞芯微" , "瑞芯"and other Rockchip trademarks are trademarks of Rockchip Electronics co., ltd., are exclusively owned by Rockchip Electronics Co., Ltd.

All other trademarks or registered trademarks mentioned in this document are owned by their respective owners.

Copyright © 2022 Rockchip Electronics Co., Ltd.

Without the written permission of the company, any unit or individual shall not extract or copy part or all of the content of this document, shall not disseminate it in any form.

Rockchip Electronics Co., Ltd.

Add: No.18 Building, A District, No.89, software Boulevard Fuzhou, Fujian, PRC

Web: www.rock-chips.com

Hotline: +86-591-83991906

Fax: +86-591-83951833

Email: fae@rock-chips.com



Preface

Overview

This guide mainly introduces the basic functions and hardware features, multi-function hardware configuration, and software debugging operation methods of RK3588S EVB. It aims to help debuggers use RK3588S EVB be faster and more accurately, and be familiar with RK3588S chip development and application solutions.

Product version

The product versions corresponding to this document are as follows:

Product name	Product version
RK3588S EVB	RK_EVB1_RK3588S_LP4XD200P232SD10H2_V10_20210831

Intended Audience

This guide is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Remark
V1.0	Lzx	2022-3-9	Initial release	
V1.1	Lzx	2022-4-14	Delete the 3.19	

Acronyms

Acronyms include the abbreviations of commonly used phrases in this document:

Abbreviation	English meaning	Chinese meaning
CPU	Central Processing Unit	中央处理器
NPU	Neural Network Processing Unit	神经网络处理器
VPU	Video Processing Unit	视频处理器
DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
eDP	Embedded DisplayPort	嵌入式数码音视讯传输接口
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
I2S	Inter-IC Sound	集成电路内置音频总线
PMIC	Power Management IC	电源管理芯片
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
DCDC	Direct Current to Direct Current	直流电转直流电
CAN	Controller Area Network	控制器局域网络
SARADC	Successive Approximation Register Analog to Digital Converter	逐次逼近寄存器型模数转换器
UART	Universal Asynchronous Receiver/ Transmitter	通用异步收发传输器
JTAG	Joint Test Action Group	联合测试行为组织
PWM	Pulse Width Modulation	脉冲宽度调制
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
LVDS	Low-Voltage Differential Signaling	低电压差分信号
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
RK/Rockchip	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
USB	Universal Serial Bus	通用串行总线
SATA	Serial Advanced Technology Attachment	串行高级技术附件
PCIe	Peripheral Component Interconnect Express	外围组件快速互连
RGB	Red,Green,Blue ; RGB color mode is a color standard in industry	红绿蓝，RGB 色彩模式，是工业界的一种颜色标准
VGA	Video Graphics Array	电脑显示视频图像标准接口
ADB	Android Debug Bridge	安卓调试桥
IR	Infrared Radiation	红外线
SPDIF	Sony/Philips Digital Interface	索尼/飞利浦数字音频接口
RTC	Real-time clock	实时时钟
RGMII	Reduced Gigabit Media Independent Interface	精简吉比特介质独立接口
WIFI	Wireless Fidelity	无线保真
CIF	Camera Interface	摄像头接口

Contents

Preface	III
Revision History.....	IV
Acronyms.....	V
Contents.....	VI
Figure Index	VIII
Table Index.....	IX
1 System Introduction.....	1
1.1 RK3588S Introduction	1
1.2 RK3588S Block Diagram	2
1.3 System Framework	2
1.3.1 System Block Diagram	2
1.3.2 Function Summary.....	3
1.3.3 Functional Interface	4
1.3.4 Function Module Layout.....	5
1.4 Module	6
1.5 Power on and off and Standby	6
1.6 Firmware Upgrade	6
1.6.1 USB Driver Installation	6
1.6.2 Firmware Upgrade Method.....	7
1.7 Serial Debugging	9
1.7.1 Serial Port Tool.....	9
1.7.2 ADB Debug	11
2 Hardware Introduction.....	12
2.1 The Pictures	12
2.2 I2C Address	12
2.3 Extension Connector Information	13
2.3.1 LCD /DMIC FPC Socket.....	13
2.3.2 Camera Socket	14
2.4 Reference Diagram	15
3 Module Brief	16
3.1 Power Input.....	16
3.2 Memory.....	17
3.3 RTC Circuit.....	19
3.4 Key Input	20
3.5 Fan Power Interface	20
3.6 PCIe Socket.....	21
3.7 Audio Interface	21
3.8 IR Interface	22
3.9 Sensor Chip.....	22

3.10	BT/WIFI Interface.....	23
3.11	Debug Interface.....	23
3.12	JTAG Interface.....	24
3.13	MIPI D/CPHY Input Interface	25
3.14	MIPI DPHY Input Interface	26
3.15	TYPEC Interface.....	27
3.16	TF Card Interface	27
3.17	USB2.0 Host Interface	28
3.18	MASKROM Key	28
3.19	CAN Interface.....	29
3.20	MIPI TX Interface.....	29
3.21	DMIC ARRAY Interface	30
4	Precautions.....	32

Figure Index

Figure 1-1 RK3588S Chip Block Diagram.....	2
Figure 1-2 RK3588S EVB System Block Diagram.....	3
Figure 1-3 RK3588S EVB Functional Interface Distribution Diagram (front)	5
Figure 1-4 RK3588S EVB Functional Interface Distribution Diagram (back)	5
Figure 1-5 Schematic Diagram of Successful Driver Installation	6
Figure 1-6 Schematic Diagram of Entering Loader Programming Mode.....	7
Figure 1-7 Schematic Diagram of Entering MASKROM Programming Mode	8
Figure 1-8 Get the Current Port COM Number	9
Figure 1-9 Serial Port Tool Configuration Interface.....	10
Figure 1-10 Serial Port Tool Debug Interface	11
Figure 1-11 ADB Connection is Normal.....	11
Figure 2-1 RK3588S EVB Picture	12
Figure 2-2 Pitch 0.5mm Vertical Double Row 30 PIN PCB Package.....	13
Figure 3-1 DC12V Input, Front-end Buck Converter and PMIC Chip	17
Figure 3-2 Location of LPDDR4x and eMMC.....	18
Figure 3-3 Reserve Location of SPI Flash.....	18
Figure 3-4 Key Position of EVB into MASKROM Programming.....	19
Figure 3-5 RTC Circuit.....	19
Figure 3-6 Key Position.....	20
Figure 3-7 Fan Power Interface	20
Figure 3-8 PCIe Socket.....	21
Figure 3-9 Audio Interface	21
Figure 3-10 The development board supports IR function	22
Figure 3-11 Sensor chip.....	22
Figure 3-12 BT/WIFI Antenna Interface	23
Figure 3-13 Debug Interface.....	23
Figure 3-14 JTAG Socket.....	24
Figure 3-15 DIP Switch.....	24
Figure 3-16 MIPI D/CPHY RX Input Interface	25
Figure 3-17 MIPI DPHY RX Input Interface	26
Figure 3-18 TypeC Interface	27
Figure 3-19 TF Card	27
Figure 3-20 USB2.0 Host Interface	28
Figure 3-21 MASKROM key	28
Figure 3-23 CAN Interface	29
Figure 3-24 MIPI DPHY0/DPHY1 TX interface	29
Figure 3-25 DMIC ARRAY Socket	30

Table Index

Table 1-1 PCB Functional Interface Introduction Table	4
Table 2-1 Correspondence Table of Peripheral Address and IO Level Value Mounted on I2C Channel	12
Table 3-1 MIPID/CPHY_RX Signal Definition Table.....	25
Table 3-2 MIPI DPHY_RX Signal Definition Table	26
Table 3-3 MIPI DPHY0/DPHY1 TX interface signal definition table.....	30
Table 3-4 DMIC ARRAY interface signal definition table.....	31

1 System Introduction

1.1 RK3588S Introduction

RK3588S is a high-performance, low-power application processor chip. It integrates 4 Cortex-A76, 4 Cortex-A55 and independent NEON coprocessor. Suitable for tablet, AR/VR, personal mobile Internet devices and other multimedia products.

RK3588S has built-in a variety of powerful embedded hardware engines, providing excellent performance for high-end applications. It supports 8K@60fps H.265 and VP9 decoder, 8k@30fps H.264 decoder and 4K@60fps AV1 decoder; it also supports 8K@30fps H.264 and H.265 encoder, high quality JPEG encoder/decoder, dedicated image pre-processor and post-processor.

RK3588S has a built-in 3D GPU that is fully compatible with OpenGL ES1.1/2.0/3.2, OpenCL 2.2 and Vulkan 1.2. The special 2D hardware engine with MMU will maximize the display performance and provide a smooth operating experience.

RK3588S introduces a new generation of ISP with the largest 48M pixels completely based on hardware. It implements many algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, defogging, fisheye correction, gamma correction, etc.

The NPU embedded in RK3588S supports INT4/INT8/INT16/FP16 mixed operation, and the computing power is up to 6TOP. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3588S has high-performance 4-channel external memory interfaces (LPDDR4/LPDDR4X/LPDDR5), which can support systems with high memory bandwidth requirements, and also provides a complete set of peripheral interfaces to flexibly support various Class application.

1.2 RK3588S Block Diagram

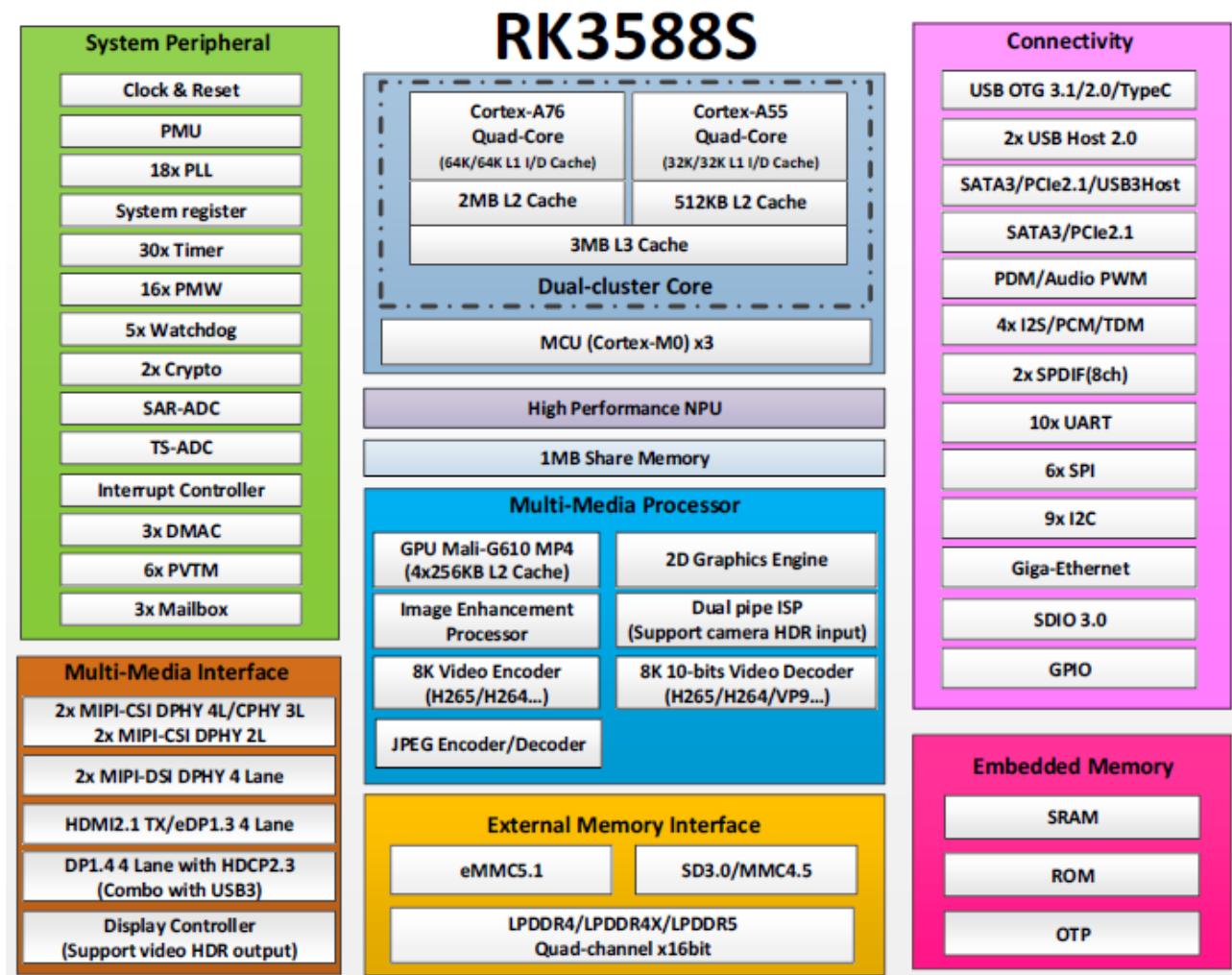


Figure 1-1 RK3588S Chip Block Diagram

1.3 System Framework

1.3.1 System Block Diagram

RK3588S EVB system uses RK3588S as the core chip of the system, and RK806-2 dual PMIC power supply scheme. Memory use LPDDR4X, eMMC; there are peripheral interfaces such as eDP, SD, MIPI RX, PCIe20, TYPEC, etc., and integrates a stable and mass-produced plan. The detailed system block diagram is as follows:

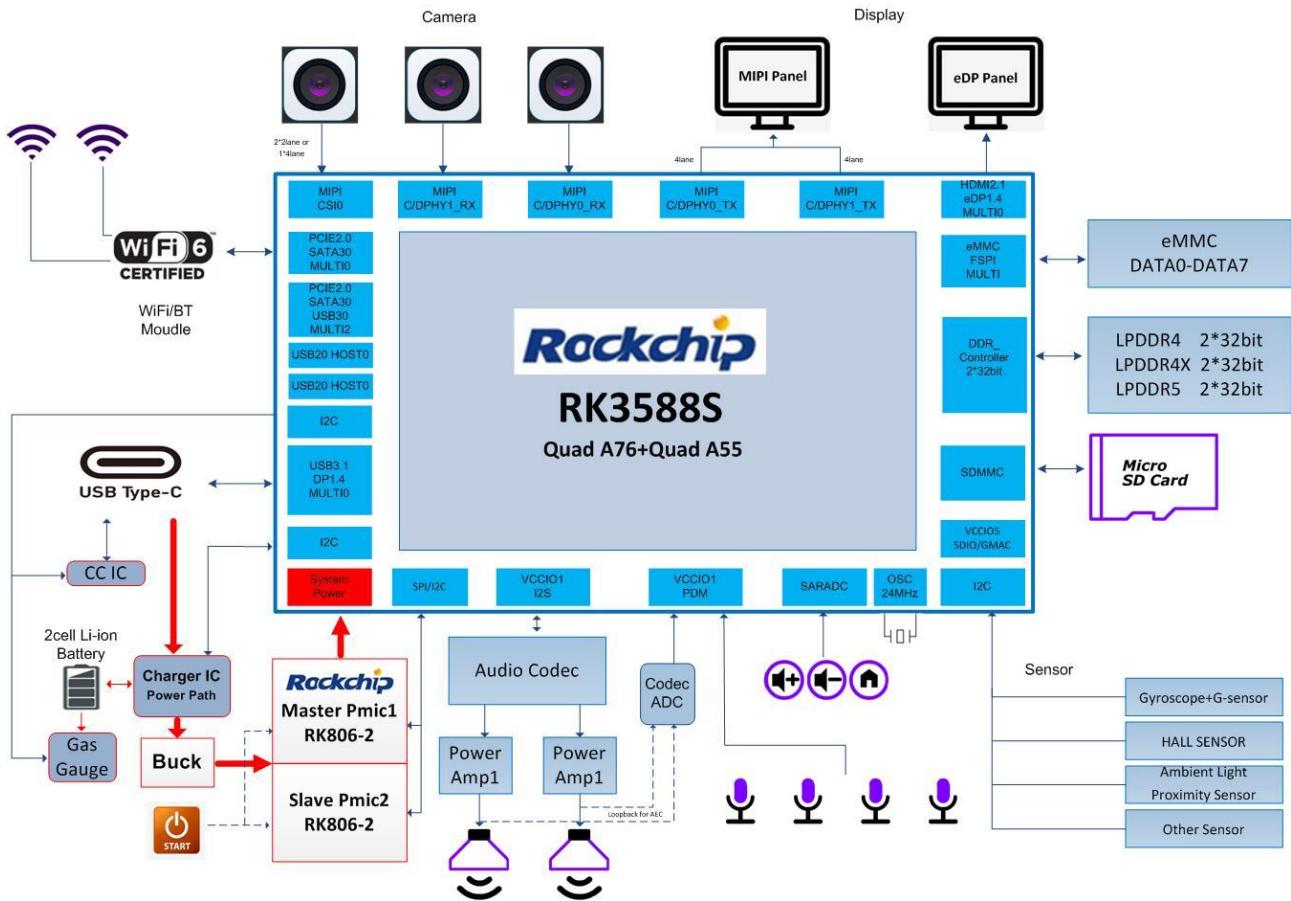


Figure 1-2 RK3588S EVB System Block Diagram

1.3.2 Function Summary

RK3588S EVB includes the following functions:

- DC Power: DC 12V adapter power supply interface;
- TYPEC: One complete TYPEC interface, compatible with system firmware upgrade channel and DP1.4 output interface;
- USB2.0 HOST0/1: Two-way USB2.0 standard-A interface, can connect to mouse, U disk, USB HUB and other equipment;
- MIPI DCPHY: Support two channels of 4lane MIPI DPHY or two channels of 3lane MIPICPHY signal input, access via 30pin AXT530124 socket;
- MIPI DPHY: Support two channels of 4lane or four channels of 2lane MIPI signal input, access via 30pin AXT530124 socket;
- MIPI DPHY0/1 TX: Support two channels of 4lane MIPI signal output, access via FPC line;
- Support eDP interface display. EVB configures the 2K screen display through this interface by default;
- PCIe Wi-Fi(2T2RWifi6&BT5.0): Wi-Fi model is AP6275P/AP6275PR3, external SMA antenna, support wireless Internet function;
- Audio Interface: Support speaker, earphone output sound, single MIC recording;

- PCIe2.0 Interface: One standard PCIe2.0x1 interface, used to expand PCIe devices;
- UART Debug: User debugging to view the LOG information; support TYPEC and MINI USB interface;
- JTAG: JTAG debug interface of system;
- System Key: Include Reset, MASKROM, PWRON, V+/Recover, V-, MENU, ESC button;
- SPDIF: Support digital audio interface;
- SD Card: Reserve SD card slot; support SD3.0, MMC ver4.51;
- DMIC: Support PDM interface DMIC ARRAY, lead out through FPC interface;
- RTC: Using HYM8563TS chip, can be powered by development board or button battery (CR1220-3V).

1.3.3 Functional Interface

Table 1-1 PCB Functional Interface Introduction Table

Function	usable or not
LPDDR4x (total capacity 8GB)	YES
eMMC (total capacity 32GB)	YES
SPI Flash	No patch by default
DC 12V Input	YES
USB2.0 Host(x2 Port)	YES
MIPI D/C PHY RX	YES
MIPI DPHY RX	YES
MIPI DPHY DSI TX1(2x4lane)	YES
BT& PCIe WIFI(2x2 WIFI&BT5.0)	YES
Audio(SPK、MIC、Earphone)	YES
DMIC ARRAY	YES
TYPEC Interface	YES
SPDIF	YES
SD Card Interface	YES
PCIe3.0 Interface(4Lane)	YES
UART Debug(TYPEC/MINI USB)	YES
JTAG Interface	YES
System Key	YES
MASKROM Key	YES

1.3.4 Function Module Layout

EVB functional interface distribution diagram:

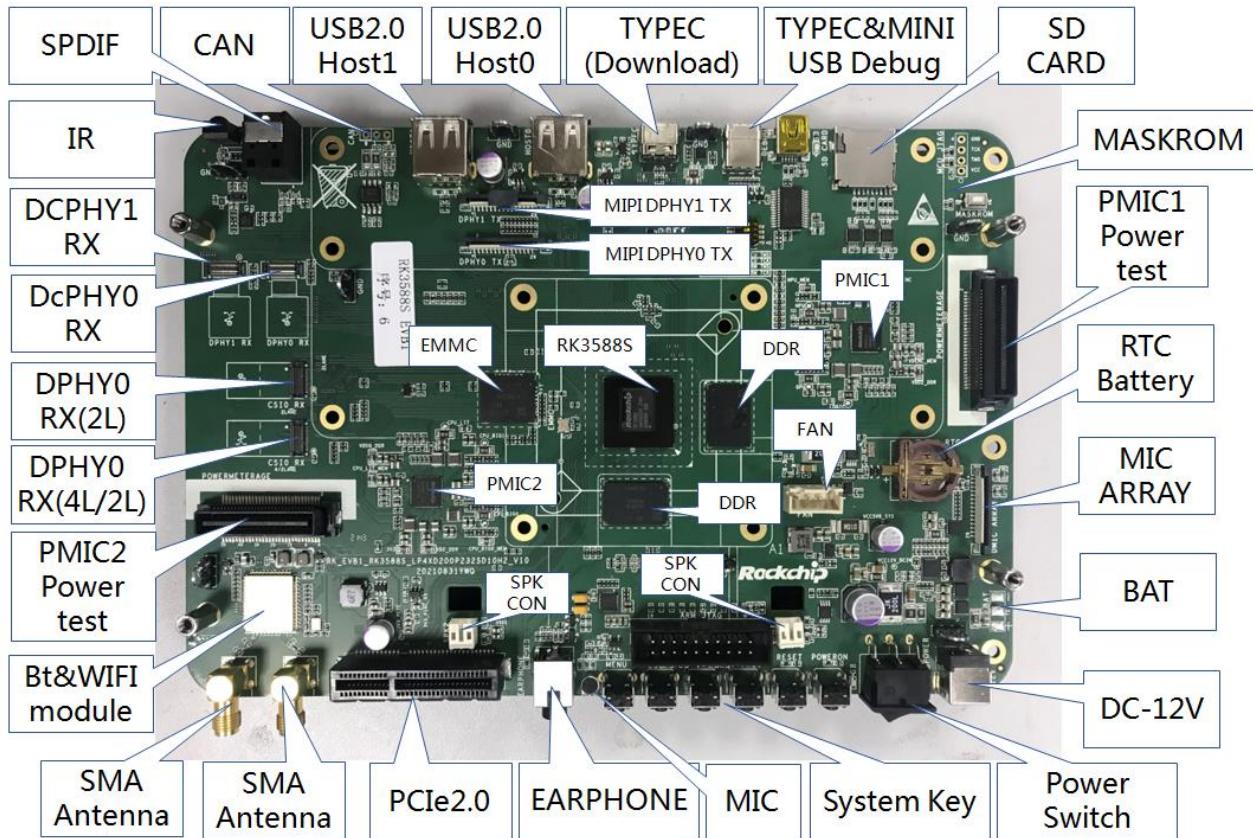


Figure 1-3 RK3588S EVB Functional Interface Distribution Diagram (front)



Figure 1-4 RK3588S EVB Functional Interface Distribution Diagram (back)

1.4 Module

The RK3588S EVB kit includes the following items:

- RK3588S EVB
- Power adapter, default specification: input 100V AC~240V AC, 50Hz; output 12V DC, 3A
- Display, specification: eDP; size: 7.85 inches/vertical screen; resolution: 2048*1536
- One 2.4G/5G dual-band SMA male connector antennas

1.5 Power on and off and Standby

The EVB power on, power off and standby methods are introduced as follows:

- Power on: Use DC 12V power supply, turn on the main power switch; wait to enter the Android interface, it means that the default firmware has been successfully started.
- Power off: Press and hold the power button for 6 seconds to shut down the system.
- Standby: Press the power button, the system will enter the first-level standby state. **When there is no USB OTG connection, and there is no other operation (such as key operation), and the software does not have a Wake_Lock source. After about 3s, it will switch from the first-level standby to the second-level standby state. Standby mode can be launched through the Power button.**

1.6 Firmware Upgrade

1.6.1 USB Driver Installation

The driver needs to be installed before the EVB driver is upgraded. The following describes the driver installation process under Windows system.

Find **DriverAssitant_v5.1.1** in the provided tool folder, and click **DriverInstall.exe** to pop up the following interface. Click "Install Driver" and wait for the prompt to install the driver successfully. If the old driver has been installed, please click "Uninstall Driver" and reinstall the driver.

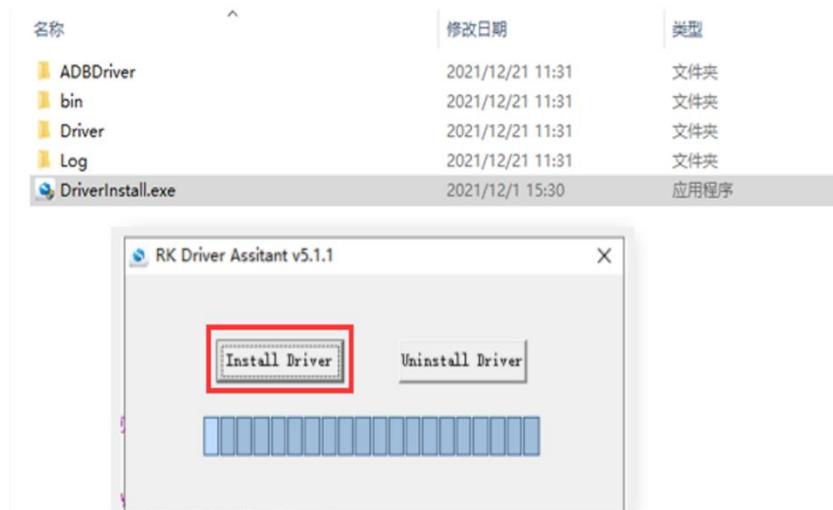


Figure 1-5 Schematic Diagram of Successful Driver Installation

1.6.2 Firmware Upgrade Method

There are two ways to upgrade RK3588S EVB firmware:

- Enter Loader upgrade mode:

Before the system is powered on, SARADC_IN1 needs to be kept low, and the system will enter the Loader state.

Specific steps are as follows:

- 1) Connect the TYPE_C port to the computer, press and hold the V+/REC button on the mainboard.
- 2) EVB is powered by 12V. If it has been powered on, press the reset button.
- 3) After the programming tool shows that “a Loader device is found”, release the V+/REC button. In the red rectangular area of the tool, right-click and choose "Import Configuration", then find the firmware path, and select the config file
- 4) The programming tool corresponds to selecting Loader, Parameter, Uboot and other files.

Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

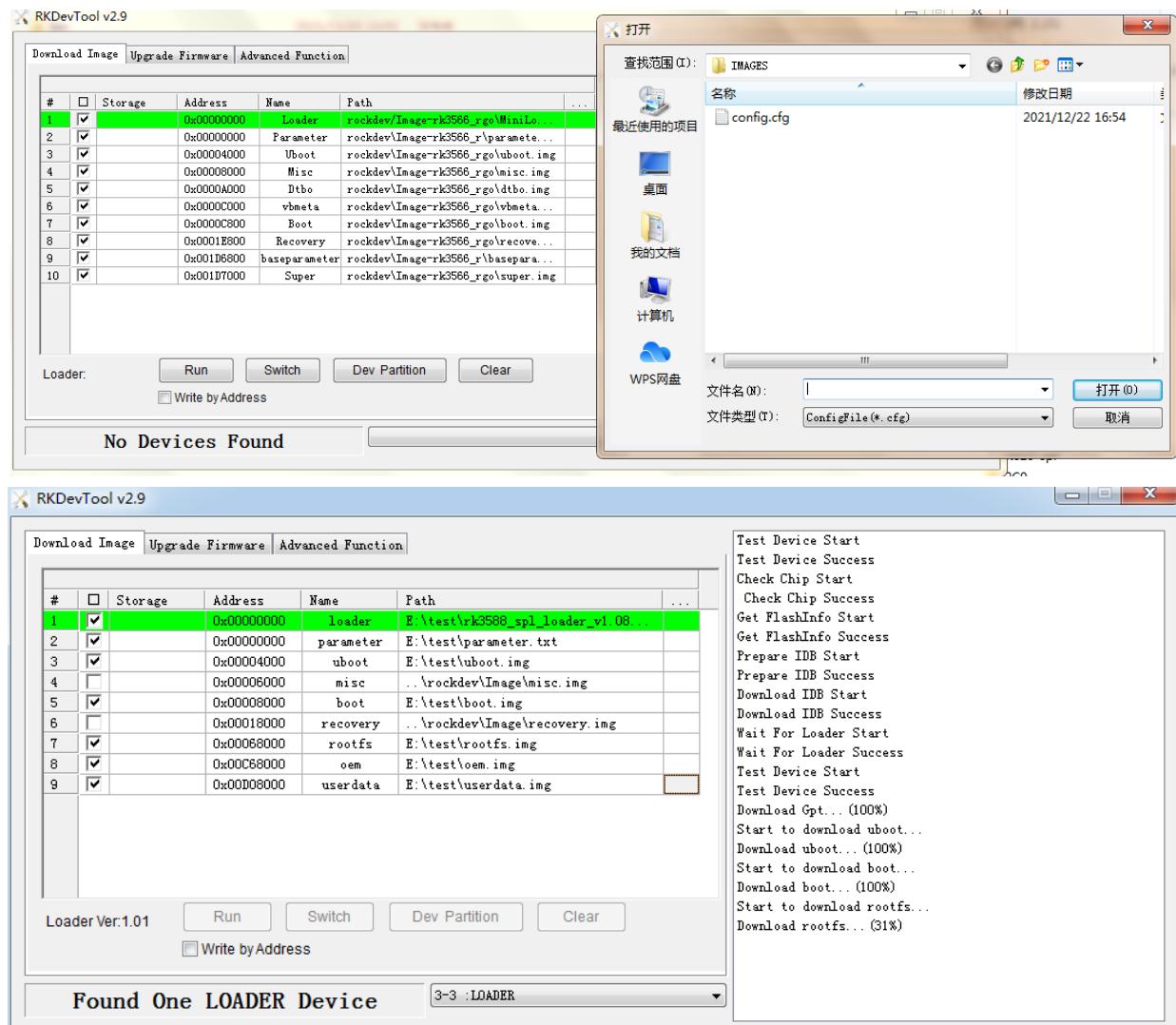


Figure 1-6 Schematic Diagram of Entering Loader Programming Mode

- Enter MASKROM upgrade mode:

Before the system is powered on, SARADC_IN0 is low and enters the MASKROM state.

Specific steps are as follows:

- 1) Connect the TYPE_C port to the computer, press and hold the MASKROM button on the board.
- 2) EVB is powered by 12V. If it has been powered on, press the reset button.
- 3) After the programming tool shows that “a MASKROM device is found”, release the MASKROM button. In the red rectangular area of the tool, right-click and choose "Import Configuration", then find the firmware path, and select the config.cfg file
- 4) The programming tool correspondingly selects Loader, Parameter, Uboot and other files.
- 5) Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

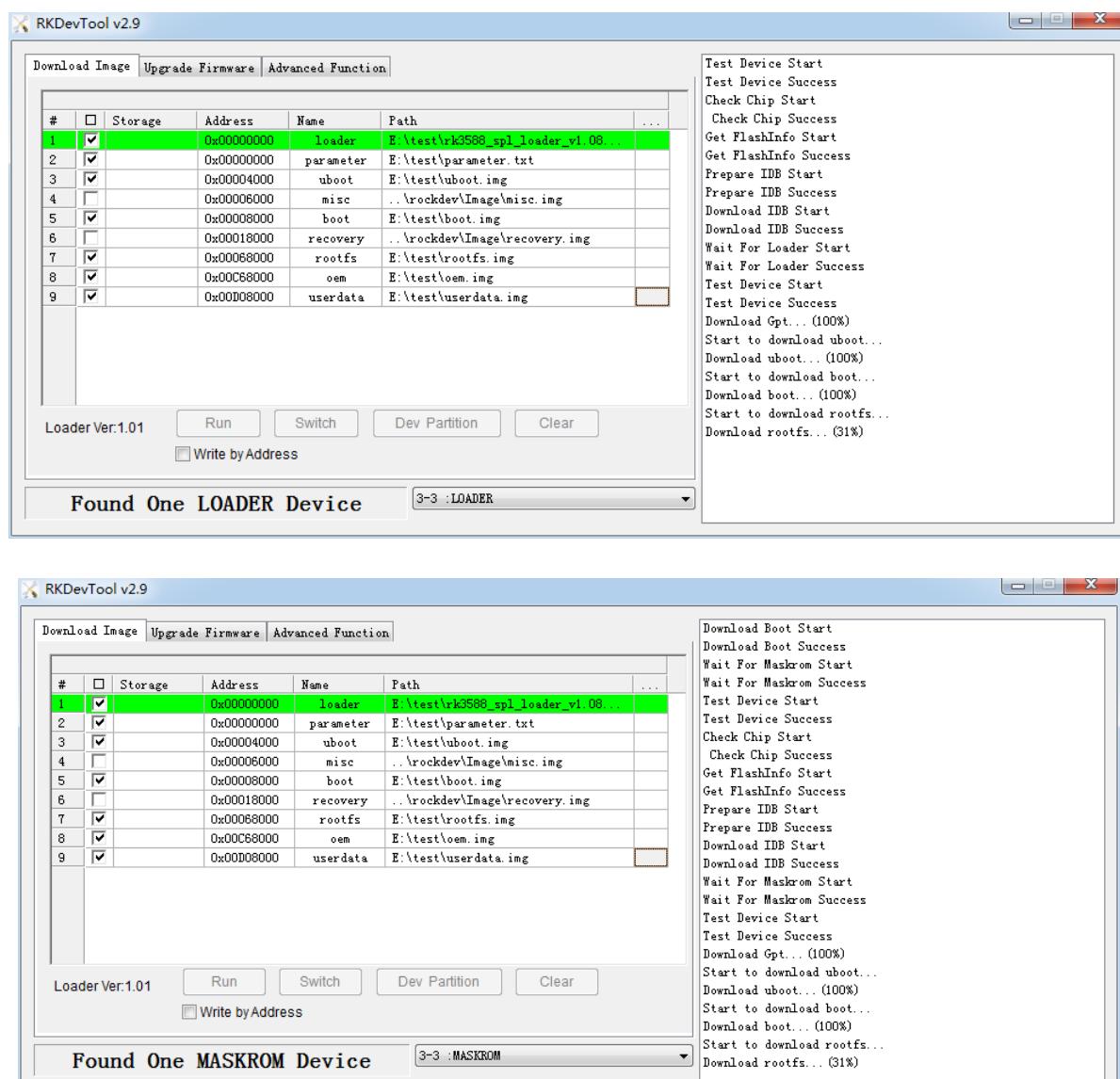


Figure 1-7 Schematic Diagram of Entering MASKROM Programming Mode

1.7 Serial Debugging

1.7.1 Serial Port Tool

Connect the MINI USB Debug debugging interface of the development board to the the computer, and get the current port COM number in the device manager of the PC end.

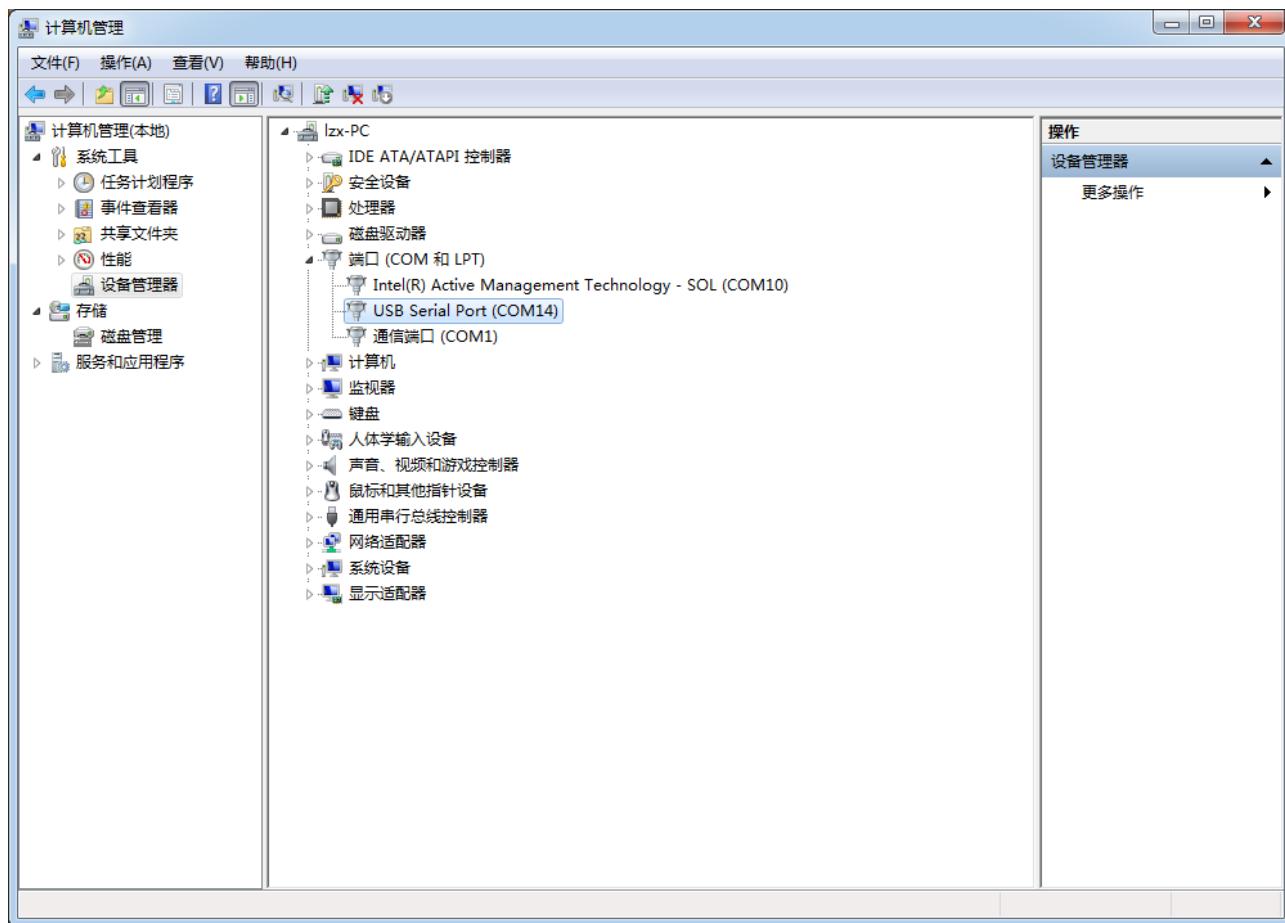


Figure 1-8 Get the Current Port COM Number

Open the serial port tool, under the "Quick Connect" interface, first select the serial port, then select the corresponding serial port number, change the baud rate to 1.5M (RK3588S supports 1.5M baud rate by default), and close the flow control at Serial, Finally, click the "Open" button to enter the serial port debugging interface.

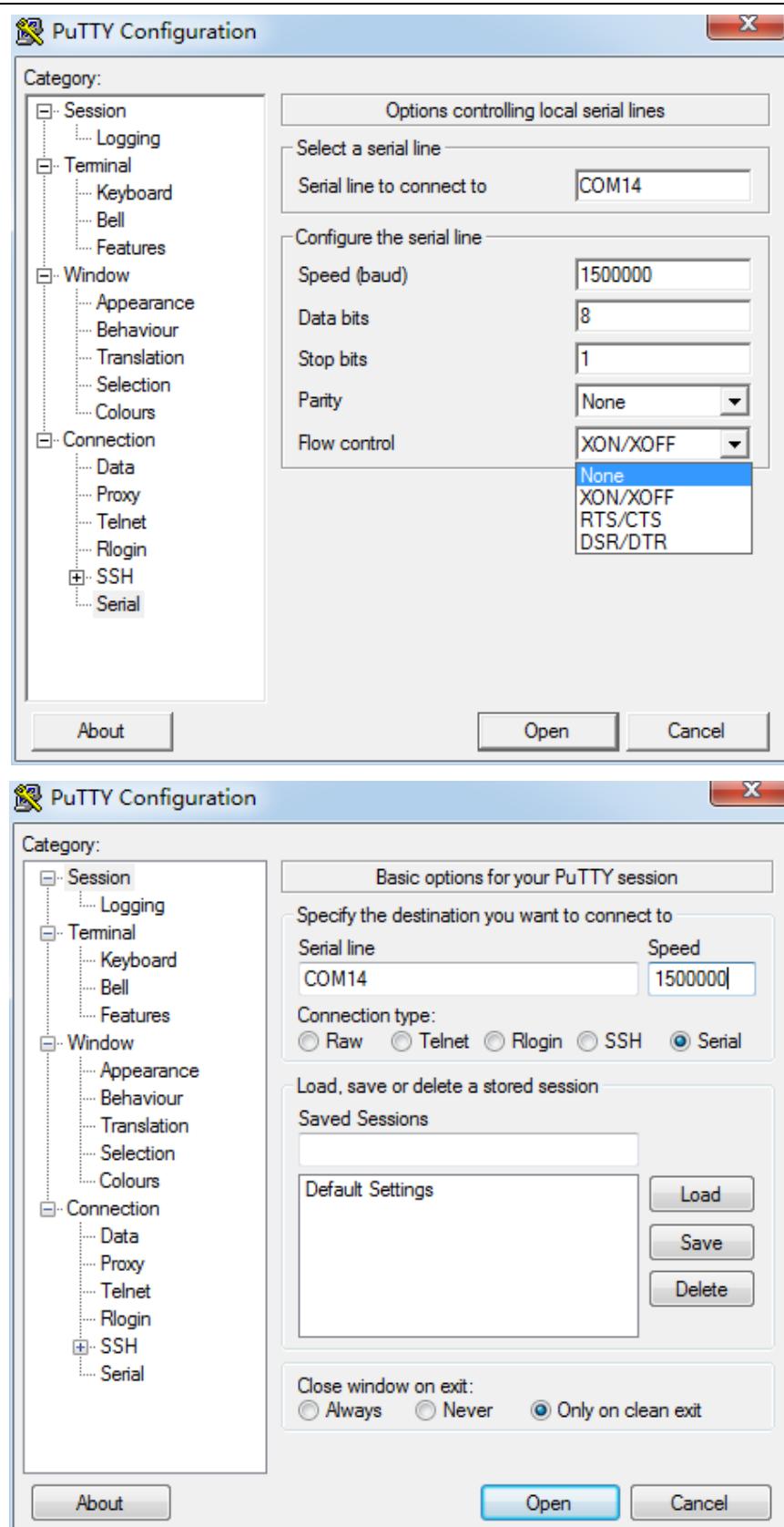


Figure 1-9 Serial Port Tool Configuration Interface

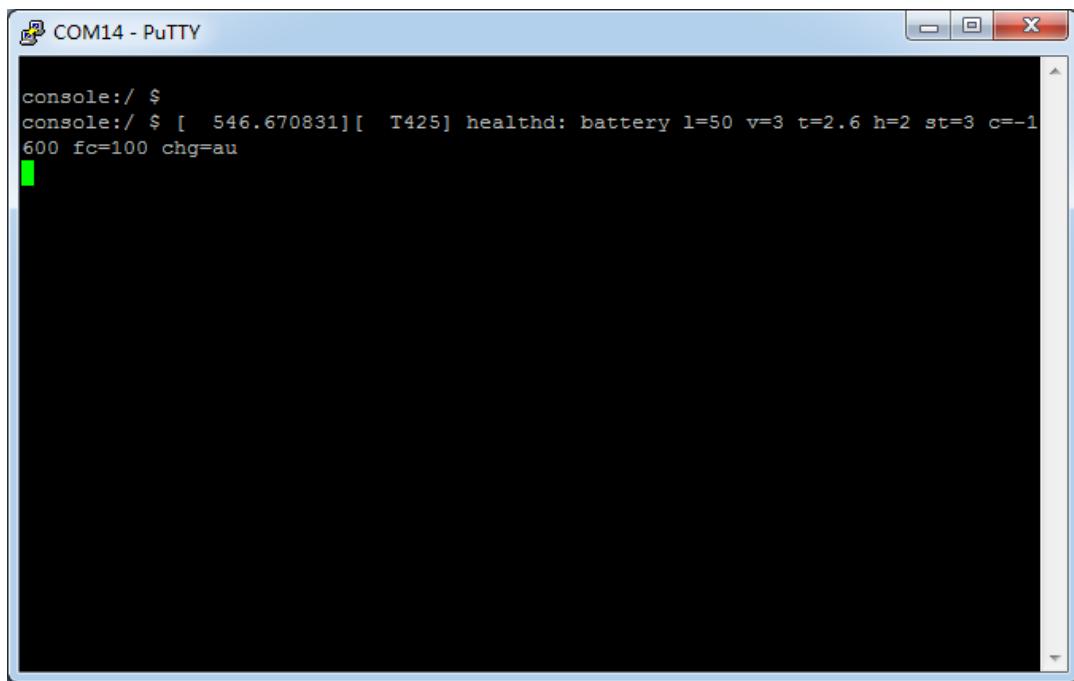


Figure 1-10 Serial Port Tool Debug Interface

1.7.2 ADB Debug

- 1) Ensure that the driver is installed successfully, and the PC is connected to the TYPE_C port on the same side as the power supply of the development board;
- 2) Power on the development board and boot into the system;
- 3) Open the adb tool on the PC side;
- 4) Type "adb shell" to enter adb debugging.

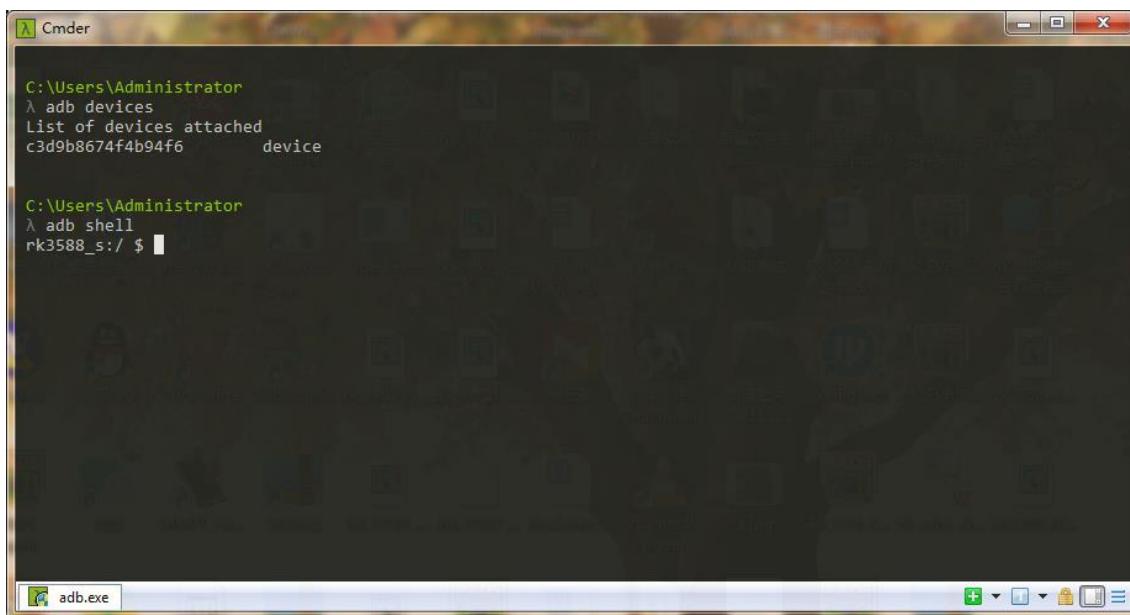


Figure 1-11 ADB Connection is Normal

2 Hardware Introduction

2.1 The Pictures



Figure 2-1 RK3588S EVB Picture

2.2 I2C Address

The development board reserves a wealth of peripheral interfaces. The user debugging I2C peripherals will involve I2C channel multiplexing. Table 2-1 shows the I2C address and level values corresponding to the existing development board devices.

Table 2-1 Correspondence Table of Peripheral Address and IO Level Value Mounted on I2C Channel

I2C 通道	设备	I2C 地址	电源域
I2C0	N/A	N/A	N/A
I2C1	N/A	N/A	N/A
I2C2	BQ25703 (Charger)	0xD6	3.3V
I2C2	CW2013CASD(Gas Gauge)	0xC5	3.3V
I2C3	ES8388	0x22	1.8V
I2C3	MIC Expand Board	TBD	1.8V
I2C3	ES7202	0x30/31/32	1.8V

I2C 通道	设备	I2C 地址	电源域
I2C4	Touch Panel	TBD	3.3V
I2C5	Gyroscope+G-sensor	TBD	3.3V
I2C5	Ambient Light+Proximity Sensor	TBD	3.3V
I2C5	HALL Sensor	TBD	3.3V
I2C5	M-Sensor	TBD	3.3V
I2C6	MIPI-CSI0_RX CON1	TBD	1.8V
I2C6	MIPI-DPHY0_RX CON	TBD	1.8V
I2C7	MIPI-CSI0_RX CON2	TBD	1.8V
I2C7	MIPI-DPHY1_RX CON	TBD	1.8V
I2C8	ET302Y/FUSB302BMPX	0xD6	3.3V
I2C8	HYM8563TS	0xA3	3.3V

Note: When using the expansion board, make sure that the I2C address on the board does not conflict with the I2C address on the development board.

2.3 Extension Connector Information

2.3.1 LCD /DMIC FPC Socket

In actual use, the user may make an expansion board. The model of the development board connector is as follows:

J5500, J5501, JP7700 are vertical double-row 30PIN card holders with 0.5mm pins and 1mm spacing, the model is FP05SL_030_V, and the dimensions are as follows:

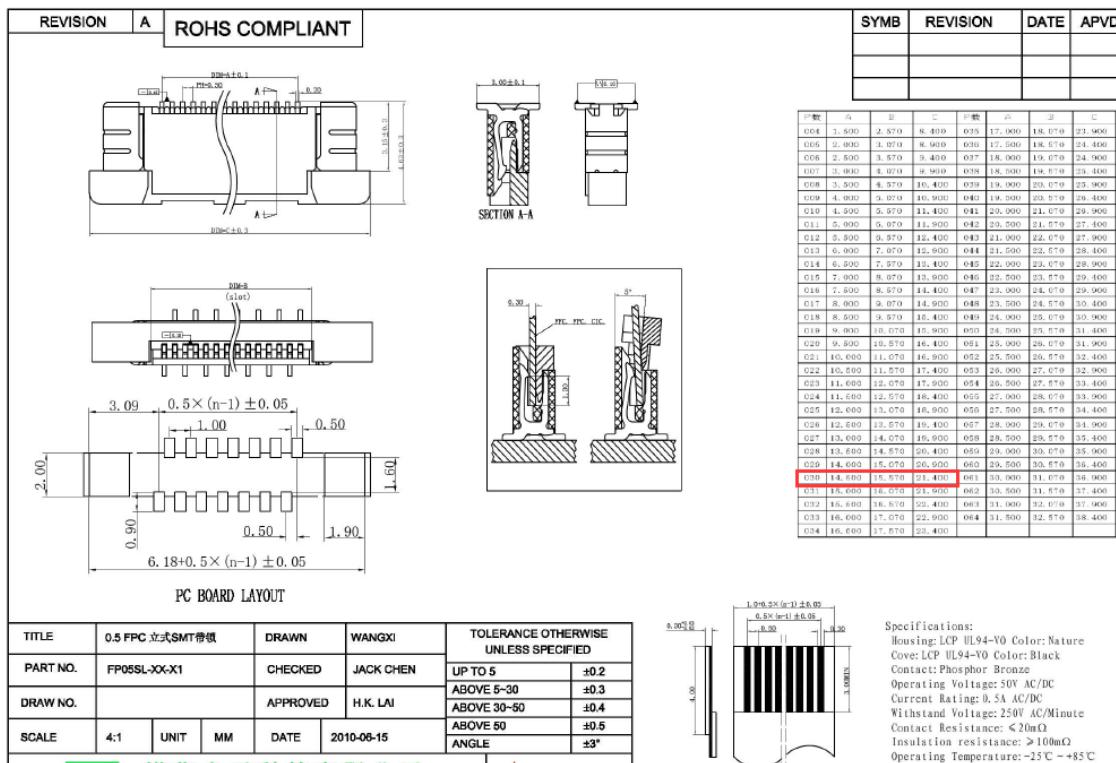


Figure 2-2 Pitch 0.5mm Vertical Double Row 30 PIN PCB Package

2.3.2 Camera Socket

J4600, J4601, J4700, J4701 sockets are 0.15mm socket sockets with a spacing of 0.4mm, and the model is AXT530124. The matching header seat model is AXT630124, and the relevant seat size is as follows:

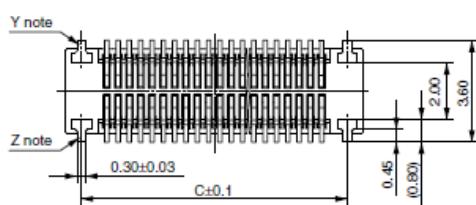
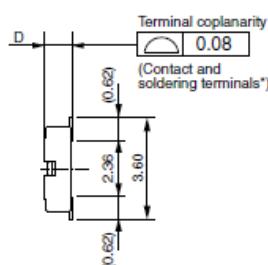
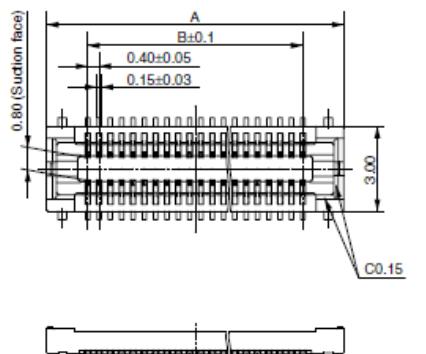
PRODUCT TYPES

Mated height	Number of pins	Part number		Packing	
		Socket	Header	Inner carton	Outer carton
1.0mm	10	AXT510124	AXT610124	3,000 pieces	6,000 pieces
	12	AXT512124	AXT612124		
	14	AXT514124	AXT614124		
	16	AXT516124	AXT616124		
	20	AXT520124	AXT620124		
	22	AXT522124	AXT622124		
	24	AXT524124	AXT624124		
	26	AXT526124	AXT626124		
	28	AXT528124	AXT628124		
	30	AXT530124	AXT630124		
	32	AXT532124	AXT632124		
	34	AXT534124	AXT634124		
	36	AXT536124	AXT636124		
	40	AXT540124	AXT640124		
	42	AXT542124	AXT642124		
	44	AXT544124	AXT644124		
	48	AXT548124	AXT648124		
	50	AXT550124	AXT650124		
	54	AXT554124	AXT654124		
	60	AXT560124	AXT660124		
	64	AXT564124	AXT664124		
	70	AXT570124	AXT670124		
	80	AXT580124	AXT680124		
1.2mm	10	AXT510224	AXT610224		
	30	AXT530224	AXT630224		
	40	AXT540224	AXT640224		
	50	AXT550224	AXT650224		
	70	AXT570224	AXT670224		
	80	AXT580224	AXT680224		

Notes: 1. Order unit: For volume production: 1-inner-box (1-reel) units
 Samples for mounting check: 50-connector units. Please contact our sales office.
 Samples: Small lot orders are possible. Please contact our sales office.

DIMENSIONS (Unit: mm)

Socket (Mated height: 1.0 mm and 1.2 mm)

CAD DataGeneral tolerance: ± 0.2

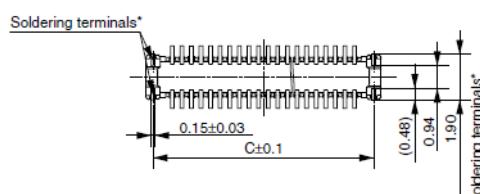
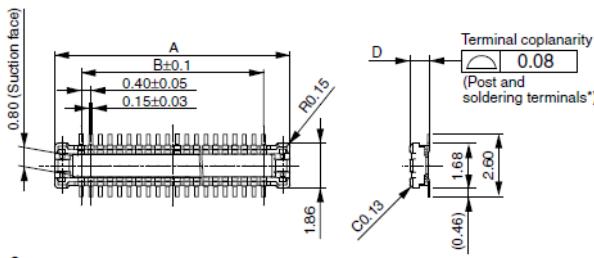
Mated height/dimension	D
1.0mm	0.97
1.2mm	1.17

Note: Since the soldering terminals* has a single-piece construction, sections Y and Z are electrically connected.

Dimension table (mm)

Number of pins/dimension	A	B	C
10	4.50	1.60	3.40
12	4.90	2.00	3.80
14	5.30	2.40	4.20
16	5.70	2.80	4.60
20	6.50	3.60	5.40
22	6.90	4.00	5.80
24	7.30	4.40	6.20
26	7.70	4.80	6.60
28	8.10	5.20	7.00
30	8.50	5.60	7.40
32	8.90	6.00	7.80
34	9.30	6.40	8.20
36	9.70	6.80	8.60
40	10.50	7.60	9.40
42	10.90	8.00	9.80
44	11.30	8.40	10.20
48	12.10	9.20	11.00
50	12.50	9.60	11.40
54	13.30	10.40	12.20
60	14.50	11.60	13.40
64	15.30	12.40	14.20
70	16.50	13.60	15.40
80	18.50	15.60	17.40

Header (Mated height: 1.0 mm and 1.2 mm)

CAD DataGeneral tolerance: ± 0.2

Mated height/dimension	D
1.0mm	0.83
1.2mm	1.01

Dimension table (mm)

Number of pins/dimension	A	B	C
10	3.80	1.60	3.20
12	4.20	2.00	3.60
14	4.60	2.40	4.00
16	5.00	2.80	4.40
20	5.80	3.60	5.20
22	6.20	4.00	5.60
24	6.60	4.40	6.00
26	7.00	4.80	6.40
28	7.40	5.20	6.80
30	7.80	5.60	7.20
32	8.20	6.00	7.60
34	8.60	6.40	8.00
36	9.00	6.80	8.40
40	9.80	7.60	9.20
42	10.20	8.00	9.60
44	10.60	8.40	10.00
48	11.40	9.20	10.80
50	11.80	9.60	11.20
54	12.60	10.40	12.00
60	13.80	11.60	13.20
64	14.60	12.40	14.00
70	15.80	13.60	15.20
80	17.80	15.60	17.20

2.4 Reference Diagram

The reference diagram and PCB design information corresponding to the EVB are as follows:

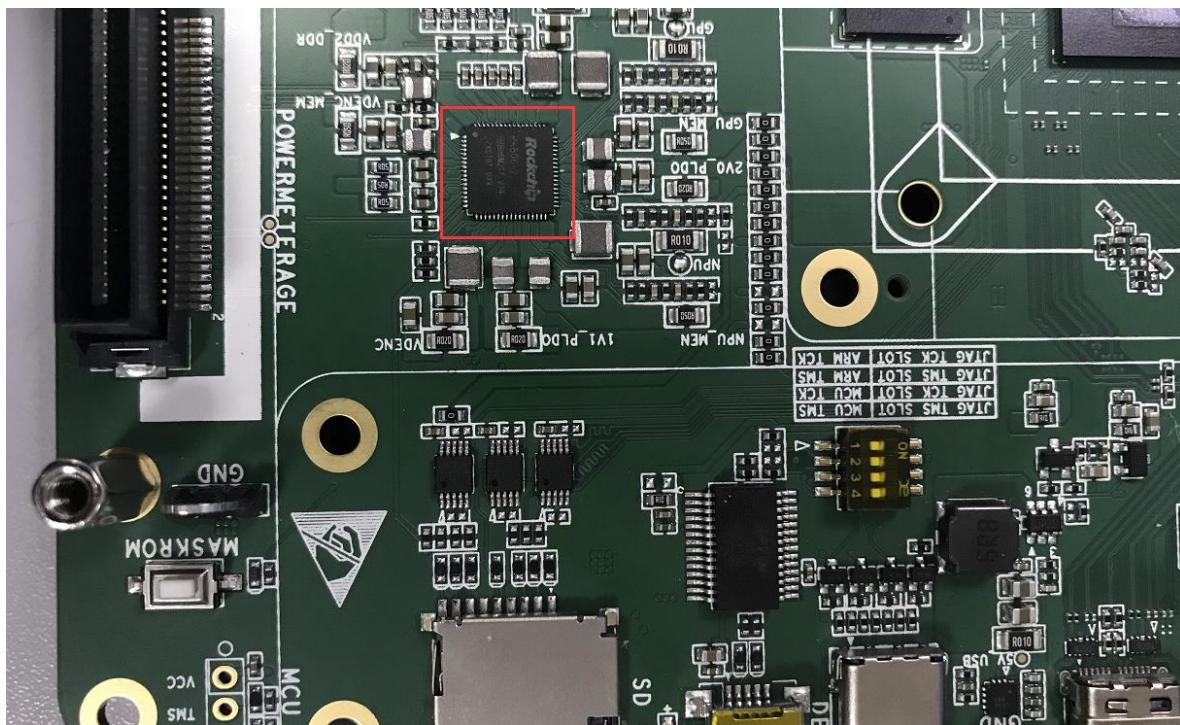
- Reference diagram: RK_EVB1_RK3588S_LP4XD200P232SD10H2_V10_20210831WF.DSN
- PCB design: RK_EVB1_RK3588S_LP4XD200P232SD10H2_V10_20210831YWQ_final.brd

3 Module Brief

3.1 Power Input

The power adapter inputs 12V/3A power, after passing the front-end buck converter power supply, the system power VCC5V0_SYS is obtained, and then the system voltage is provided to the PMIC power management chip, and different voltages are output for system use.

Power adapter input port, front-end Buck converter and PMIC chip:



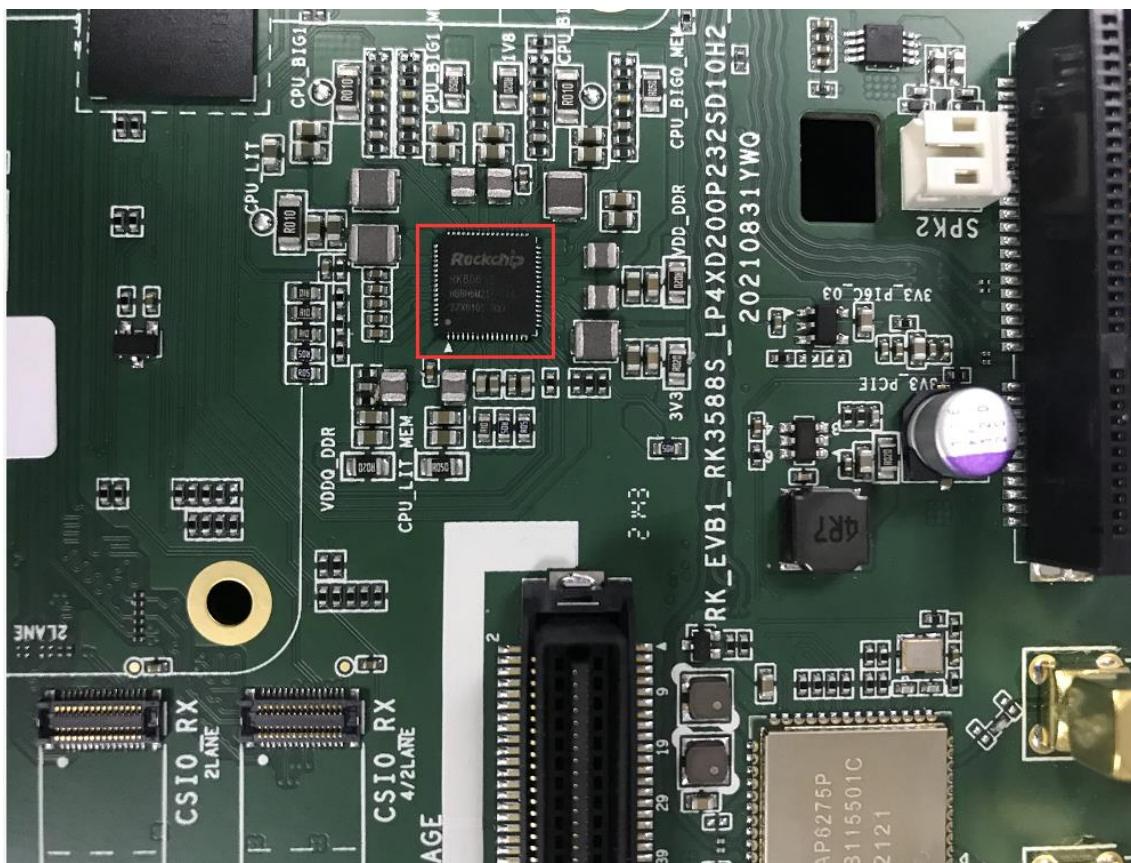


Figure 3-1 DC12V Input, Front-end Buck Converter and PMIC Chip

3.2 Memory

- eMMC: The storage type on the development board is eMMC FLASH, and the default capacity is 32GB;:
- SPI Flash: The development board reserves the location of the SPI device;
- DDR: The development board DDR adopts two pieces of 4GB LPDDR4x, with a total capacity of 8GB.

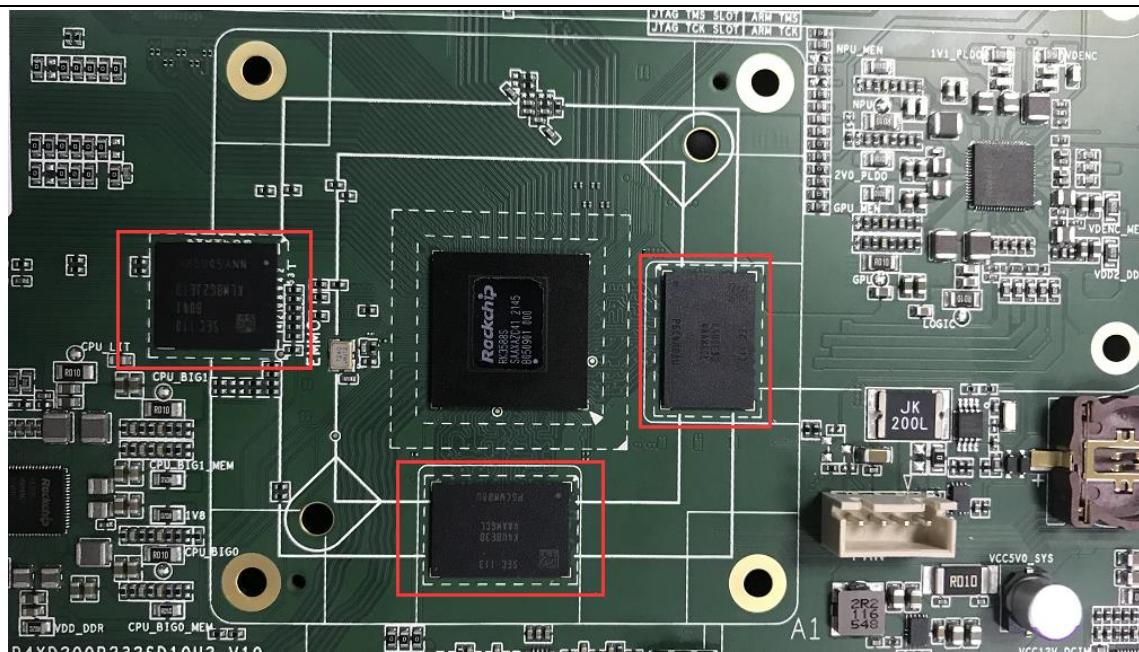


Figure 3-2 Location of LPDDR4x and eMMC

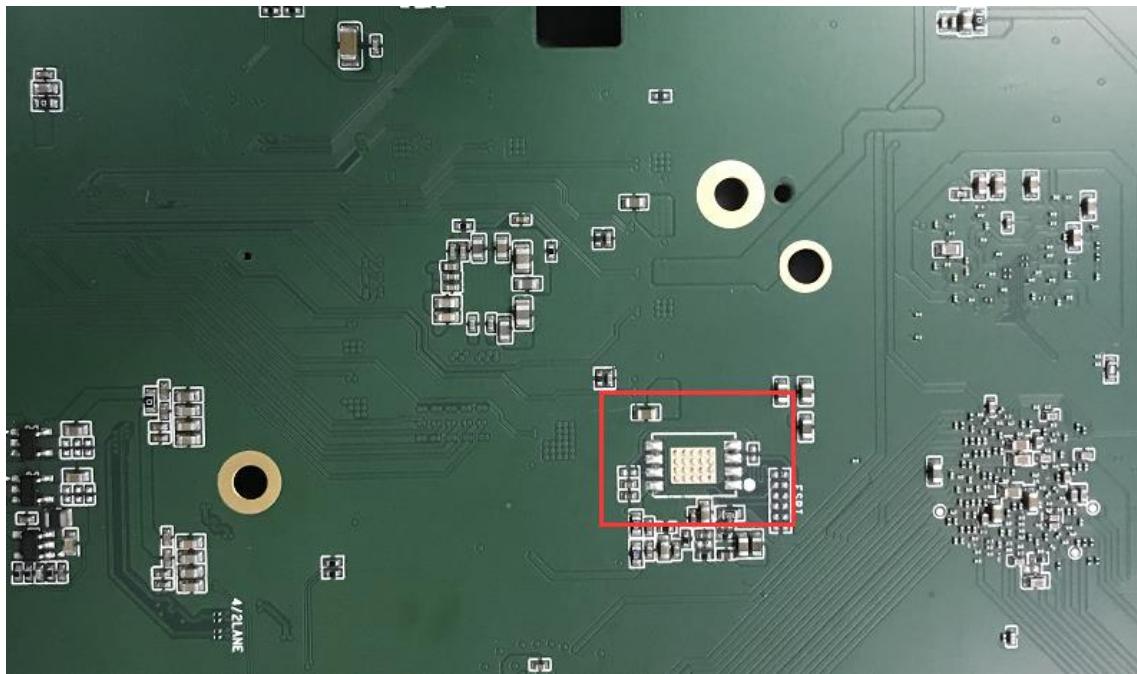


Figure 3-3 Reserve Location of SPI Flash

The key position of EVB into MASKROM programming:

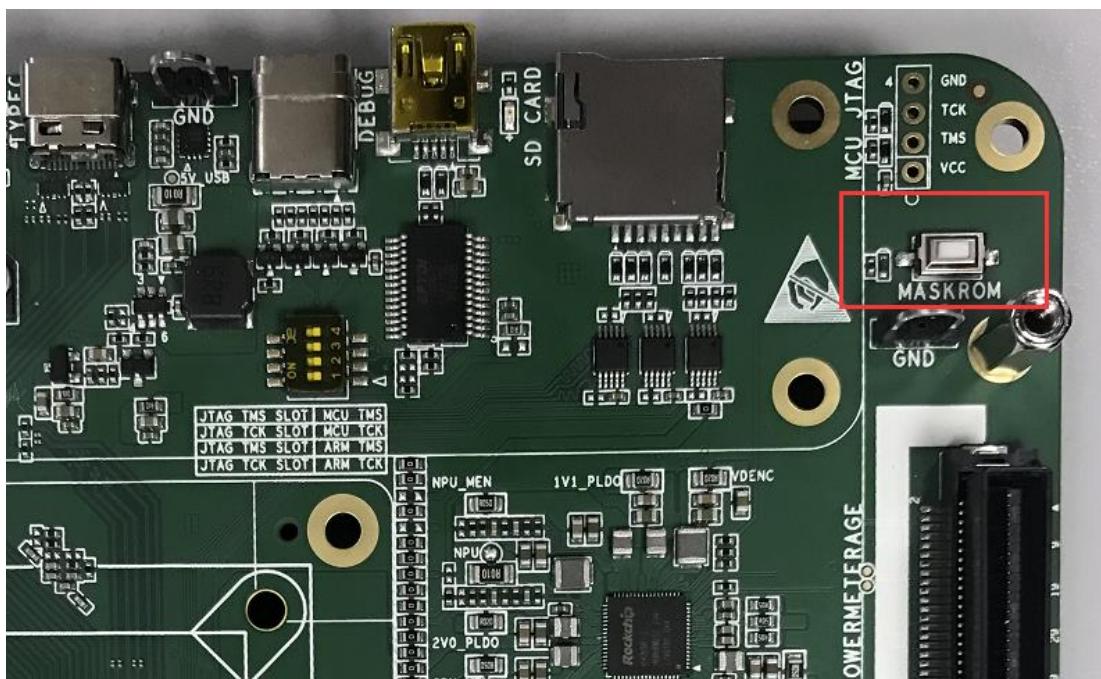


Figure 3-4 Key Position of EVB into MASKROM Programming

3.3 RTC Circuit

The RTC circuit adopts the HYM8563TS chip, which can be powered by the development board or its own button battery (not included by default, you need to purchase a CR1220-3V button battery by yourself), to ensure that it can continue to provide accurate time even when the board is powered off, and communicate with master through the I2C signal.

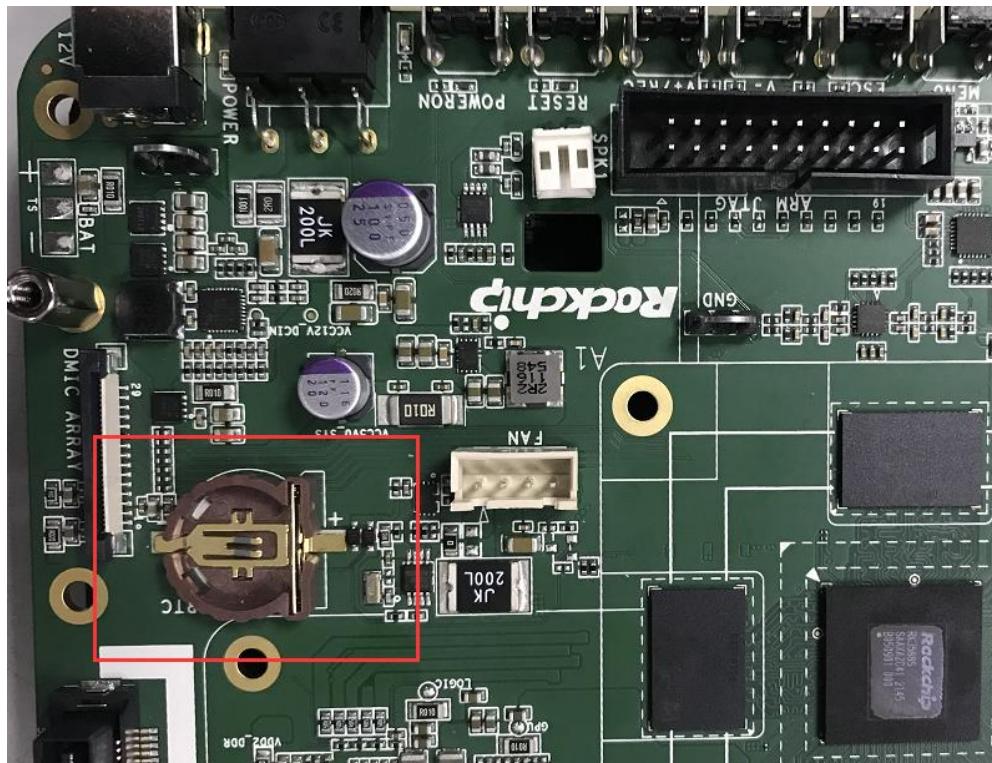


Figure 3-5 RTC Circuit

3.4 Key Input

The development board uses SARADC_IN1 as the RECOVER detection port, supports 12-bit resolution, and can enter the LOADER programming mode through the V+/REC button. In addition, the board also has a RESET button, which is convenient to reset and restart the machine through hardware; and other commonly used several Buttons: V+, V-, ESC, MENU, PWRON.

The key positions are as follows:

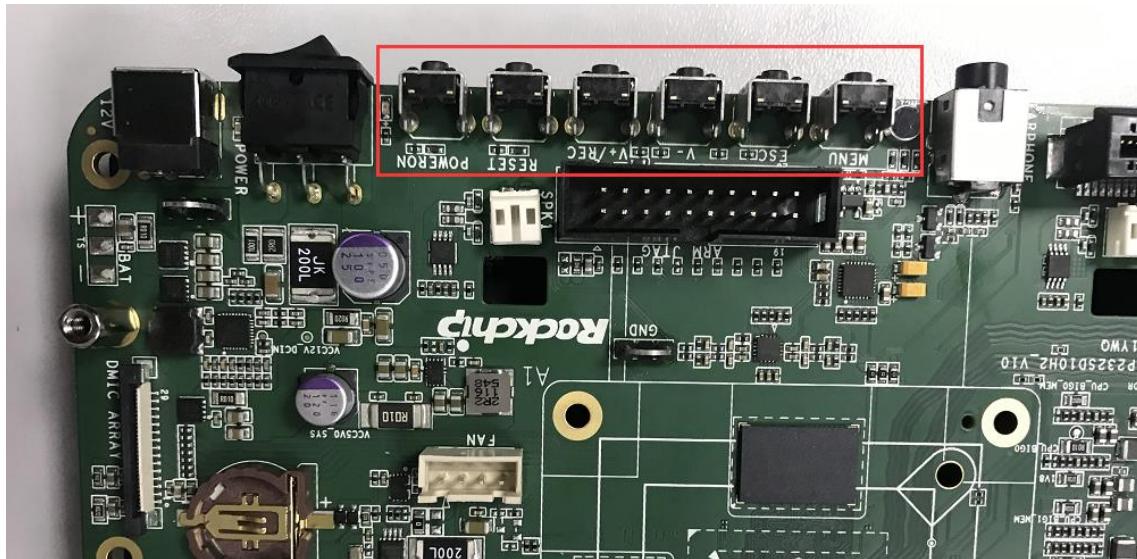


Figure 3-6 Key Position

3.5 Fan Power Interface

The development board reserves a fan interface, supports 12V/5V fans, and supports adjustable speed; the development board comes standard with a 12V fan by default.

The interface line sequence from left to right is CONTROL, SENSOR, 12V, GND.



Figure 3-7 Fan Power Interface

3.6 PCIe Socket

The development board uses a standard PCIe2.0 connector, which can be connected to an external PCIe card for communication.

- Working mode: Root Complex(RC).
- The link supports 1 lane data interfaces.

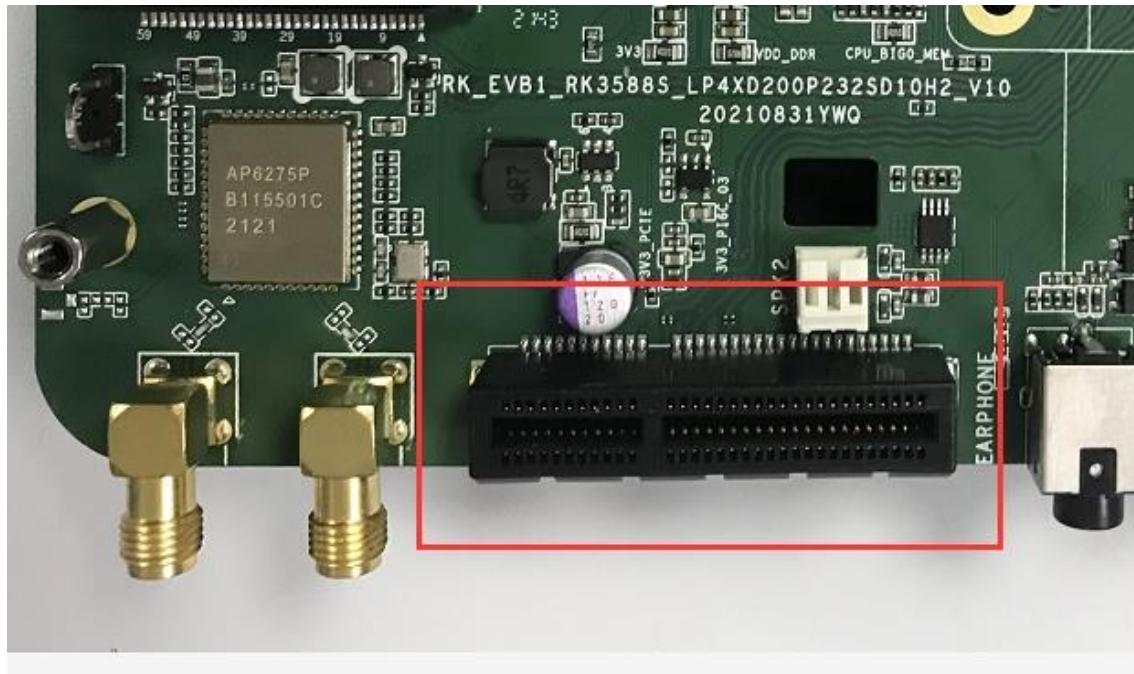


Figure 3-8 PCIe Socket

3.7 Audio Interface

The development board supports two Speaker interfaces, one Earphone interface, and one MIC interface. Can support basic network video calling function.

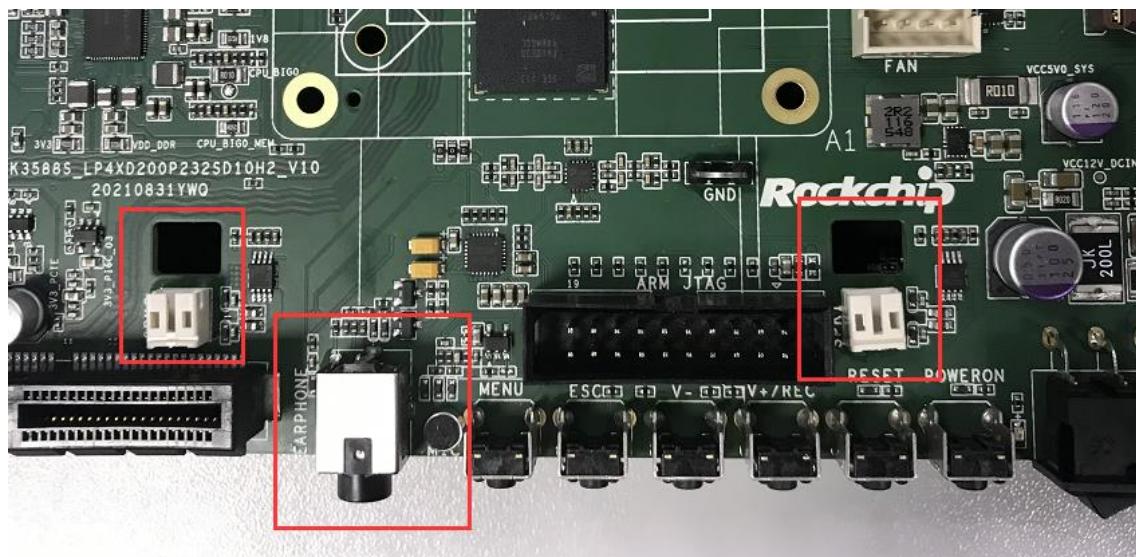


Figure 3-9 Audio Interface

3.8 IR Interface

- The development board supports IR function

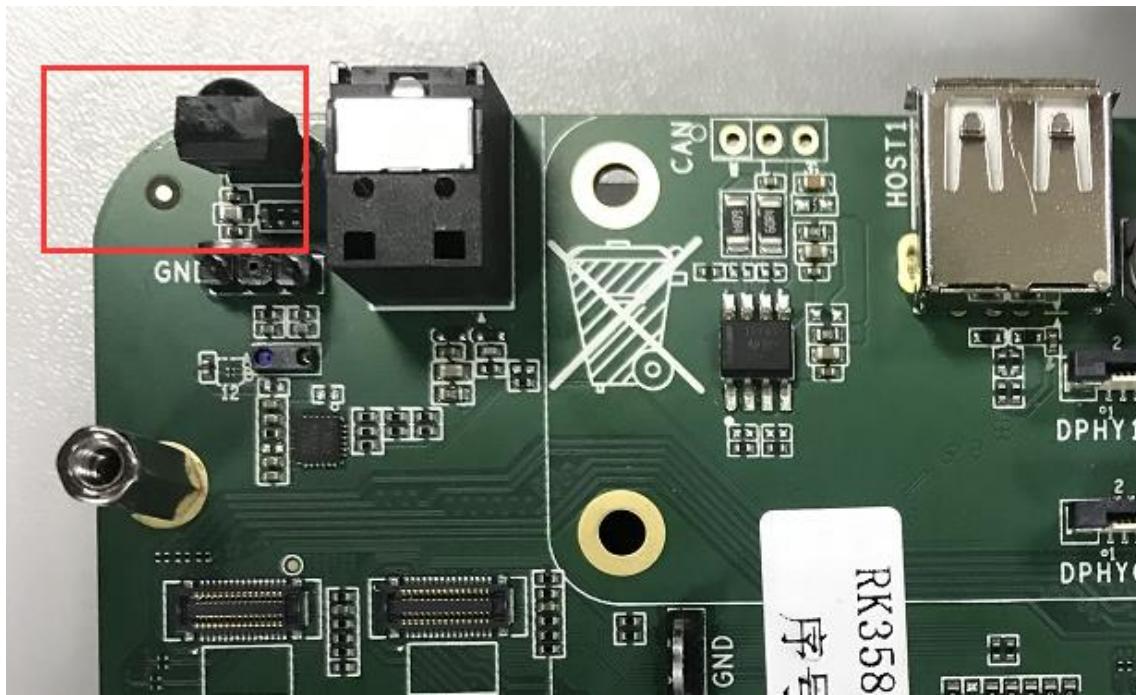


Figure 3-10 The development board supports IR function

3.9 Sensor Chip

The development board supports a variety of Sensors. The numbers in the following figure are M-Sensor, Ambient Light+Proximity Sensor, Gyroscope+G-Sensor, and Hall Sensor.

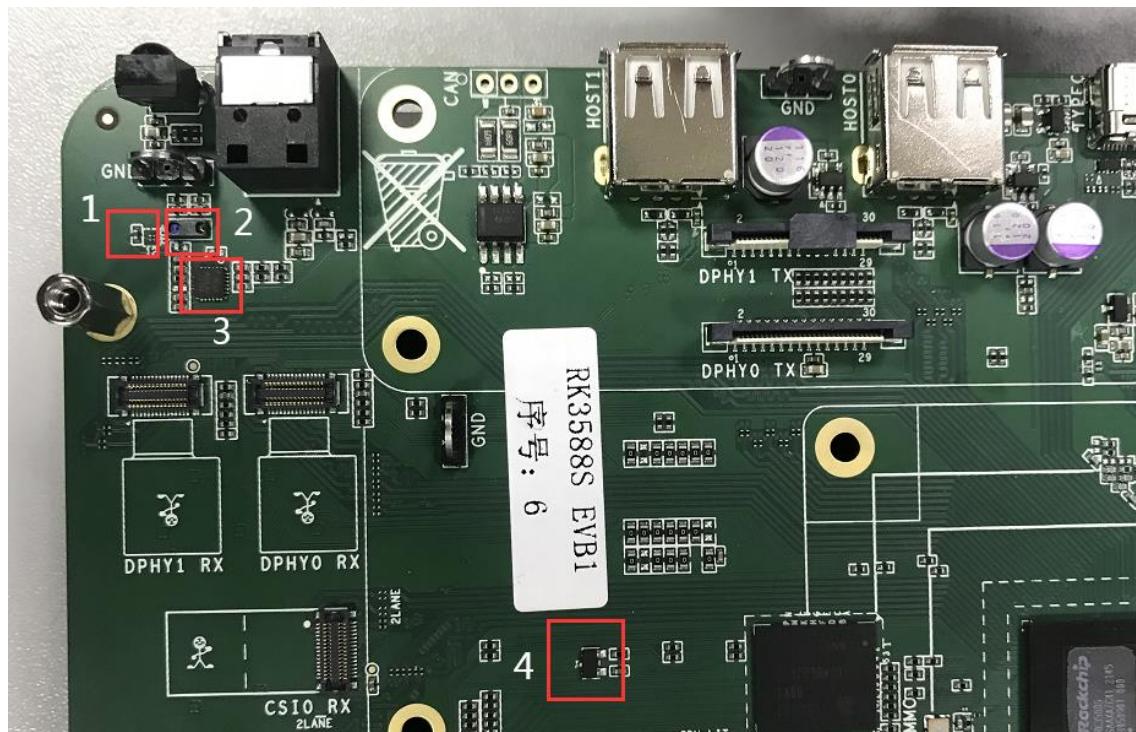


Figure 3-11 Sensor chip

3.10 BT/WIFI Interface

The WIFI+BT module on the board adopts AMPAK AP6275P, and the characteristics are as follows:

- Support 2x2WIFI (2.4G and 5G, 802.11 a/b/g/n/ac), BT5.0 function, and 2 external SMA interface antennas.
- BT data adopts UART communication mode.
- BT voice is connected to the master I2S interface.
- WIFI data adopts PCIe data bus.

RK3588S EVB is equipped with two 2.4GHz/5GHz dual-mode antennas by default.

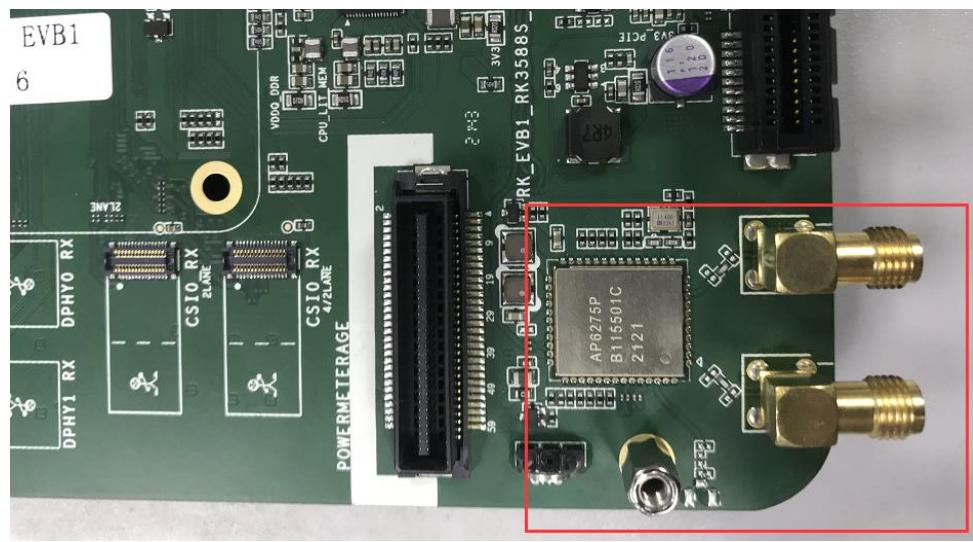


Figure 3-12 BT/WIFI Antenna Interface

3.11 Debug Interface

The development board supports TYPEC and MINI USB debugging interfaces.

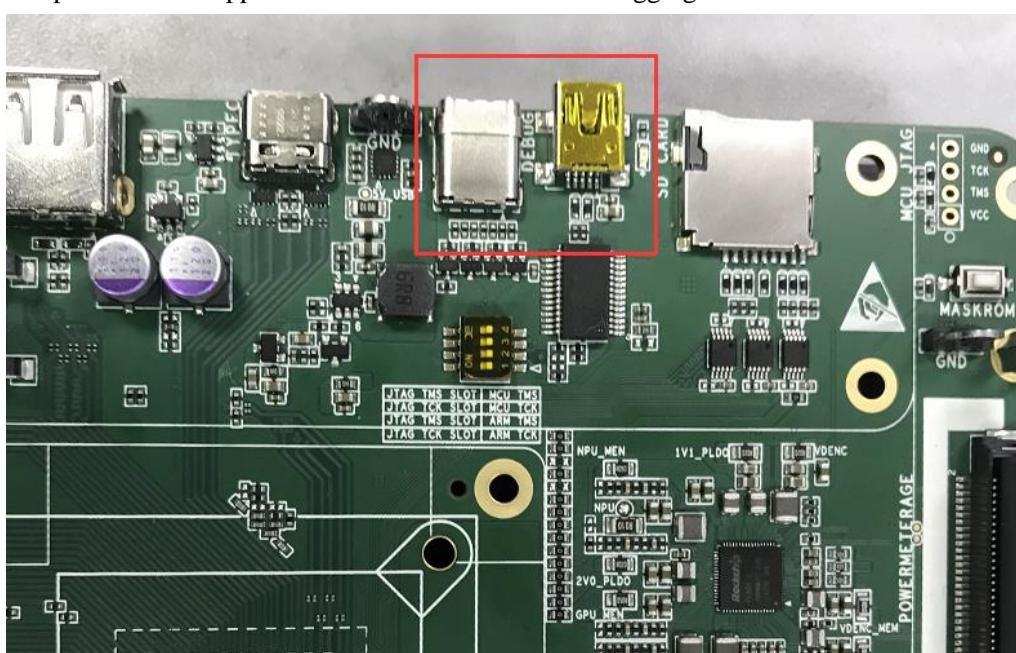


Figure 3-13 Debug Interface

3.12 JTAG Interface

The development board reserves 2xJTAG interfaces, and the reserved interface in the figure below is ARM JTAG. The standard JTAG socket supports ARM/MCU JTAG, which can be switched by the DIP switch; when the switch 1/2 is turned on and 3/4 is turned off, it supports ARM JTAG, and when the switch 1/2 is turned off and 3/4 is turned on, it supports MCU JTAG.

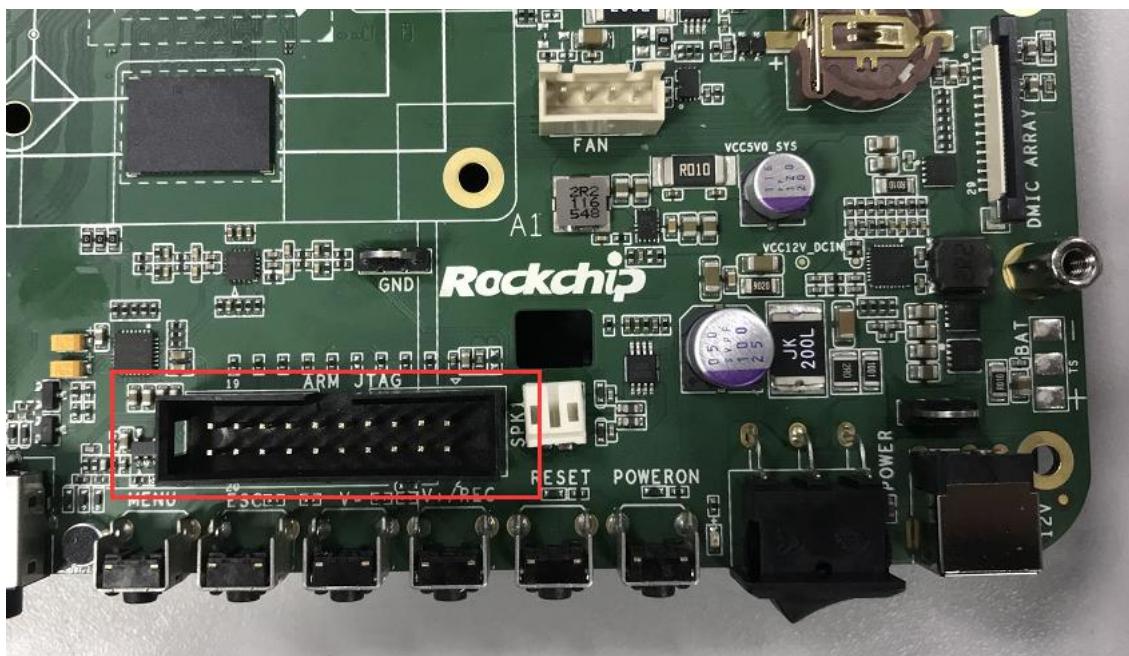


Figure 3-14 JTAG Socket

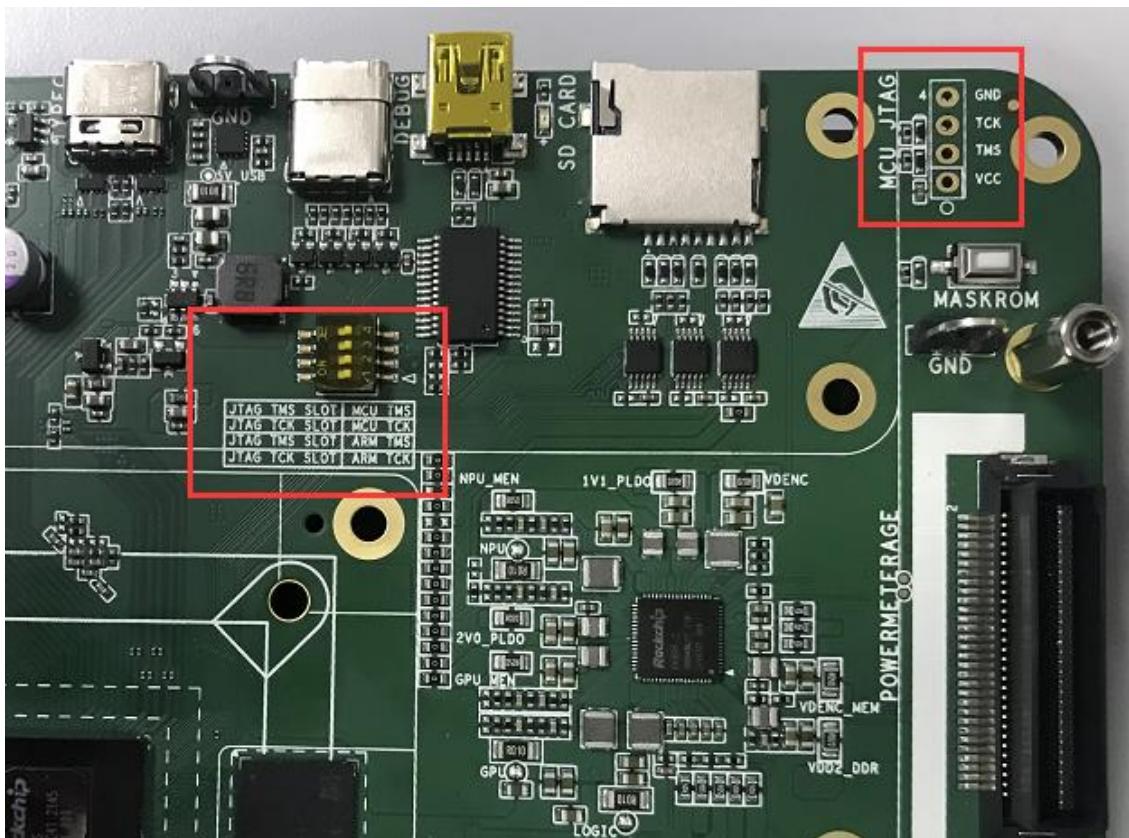


Figure 3-15 DIP Switch

3.13 MIPI D/CPHY Input Interface

The MIPI D/CPHY input interface adopts a 30pin socket (AXT530124, see section 2.3.2 for specifications) with a pitch of 0.8mm and 0.4mm, and supports dual MIPI D/CPHY interface input. It can support two-way 4Lane DPHY module input or two-way 3Lane CPHY module input. MIPI DPHY/CPHY supports up to 4.5Gbps/Lane and 5.7Gbps/Trio respectively. The socket model for this 30pin socket is AXT630124. Please refer to Chapter 2.3.2 for the package size specification. Expansion boards can be made as required.

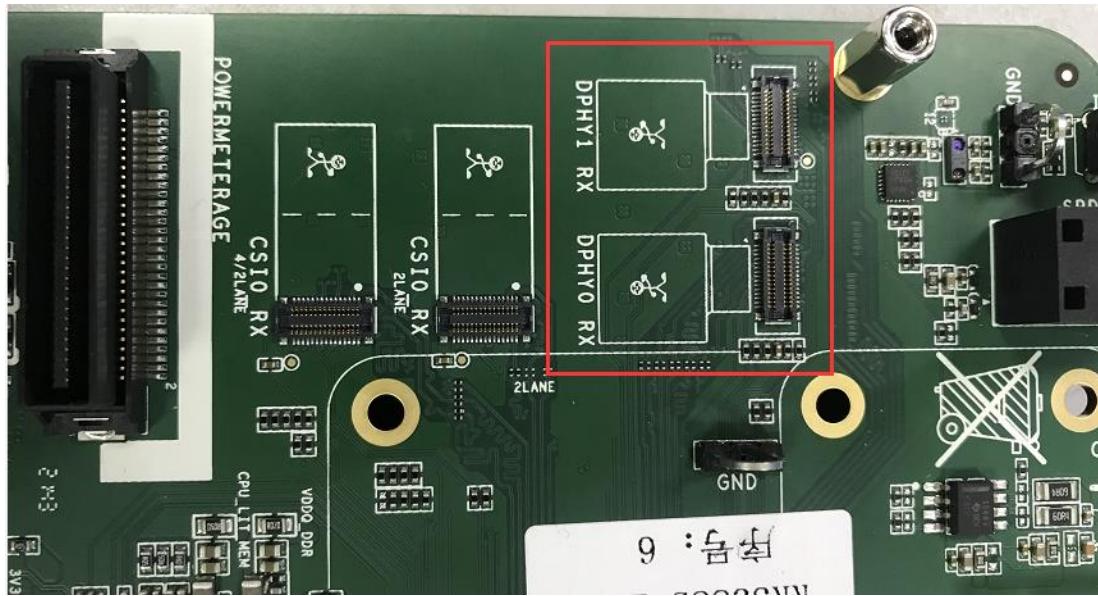


Figure 3-16 MIPI D/CPHY RX Input Interface

The MIPI D/CPHY_RX interface signal sequence is as follows:

Table 3-1 MIPID/CPHY_RX Signal Definition Table

Pin	DPHY0 (J4600)		DPHY1 (J4601)		Pin
1	GND	MIPI_DPHY0_RX_CLKN	GND	MIPI_DPHY1_RX_CLKN	30
2	MIPI_DPHY0_RX_D0P	MIPI_DPHY0_RX_CLKP	MIPI_DPHY1_RX_D0P	MIPI_DPHY1_RX_CLKP	29
3	MIPI_DPHY0_RX_D0N	GND	MIPI_DPHY1_RX_D0N	GND	28
4	GND	MIPI_DPHY0_RX_D1P	GND	MIPI_DPHY1_RX_D1P	27
5	MIPI_DPHY0_RX_D2P	MIPI_DPHY0_RX_D1P	MIPI_DPHY1_RX_D2P	MIPI_DPHY1_RX_D1P	26
6	MIPI_DPHY0_RX_D2N	GND	MIPI_DPHY1_RX_D2N	GND	25
7	GND	VCC_1V8	GND	VCC_1V8	24
8	MIPI_DPHY0_RX_D3P	VCC_1V2/GND	MIPI_DPHY1_RX_D3P	VCC_1V2/GND	23
9	MIPI_DPHY0_RX_D3N	VCC_1V2	MIPI_DPHY1_RX_D3N	VCC_1V2	22
10	GND	I2C6_SDA_M4	GND	I2C7_SDA_M2	21
11	MIPI_CAM1_CLKOUT	I2C6_SCL_M4	MIPI_CAM2_CLKOUT	I2C7_SCL_M2	20
12	MIPI_CAM1_RST_L	GND	MIPI_CAM2_RST_L	GND	19
13	XHS	VCC_2V8_AF	XHS	VCC_2V8_AF	18
14	MIPI_CAM1_PDN_L	VCC_2V8	MIPI_CAM2_PDN_L	VCC_2V8	17
15	FSIN	VSYNC	FSIN	VSYNC	16

3.14 MIPI DPHY Input Interface

The MIPI DPHY input interface adopts a 30pin socket with a pitch of 0.12mm and 0.4mm (AXT530124, see section 2.3.2 for specifications), and supports dual MIPI DPHY interface input. It can support one-way 4Lane DPHY module inputs or two-way 2Lane DPHY signal inputs. MIPI DPHY supports up to 2.5Gbps/Lane respectively. The socket model for this 30pin socket is AXT630124. Please refer to Chapter 2.3.2 for the package size specification.

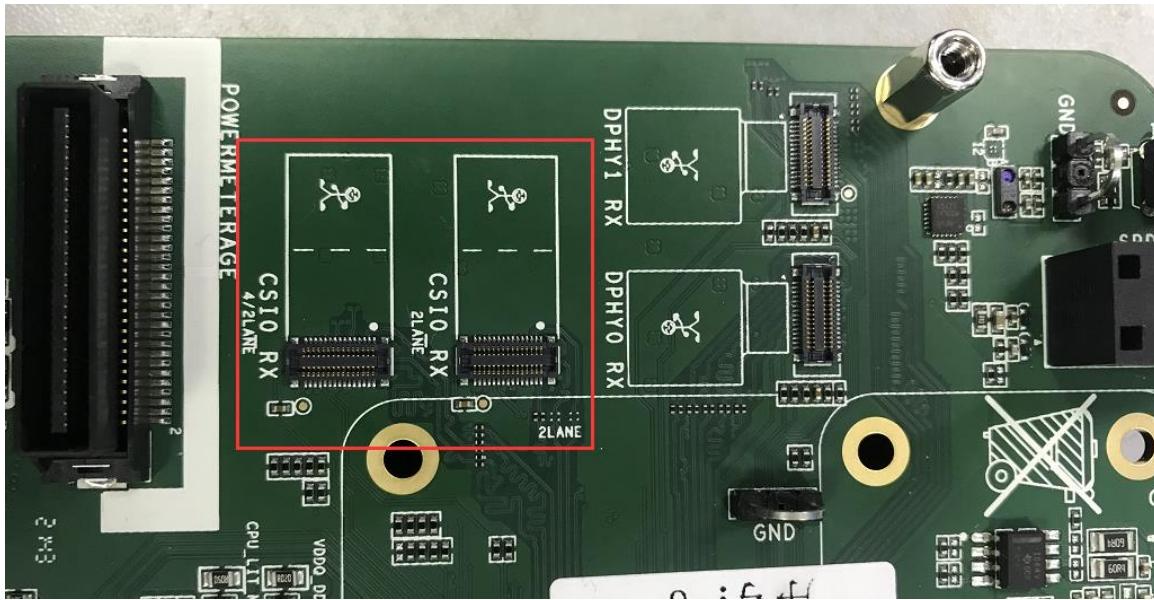


Figure 3-17 MIPI DPHY RX Input Interface

The MIPI DPHY_RX signal definition is as follows:

Table 3-2 MIPI DPHY_RX Signal Definition Table

Pin	CSI0 4Lane or 2Lane (J4700)		CSI0 2Lane (J4701)		Pin
1	GND	MIPI_CSI0_RX_CLK0N	GND	MIPI_CSI0_RX_CLK1N	30
2	MIPI_CSI0_RX_D0P	MIPI_CSI0_RX_CLK0P	MIPI_CSI0_RX_D2P	MIPI_CSI0_RX_CLK1P	29
3	MIPI_CSI0_RX_D0N	GND	MIPI_CSI0_RX_D2N	GND	28
4	GND	MIPI_CSI0_RX_D1P	GND	MIPI_CSI0_RX_D3P	27
5	MIPI_CSI0_RX_D2P	MIPI_CSI0_RX_D1N	NC	MIPI_CSI0_RX_D3N	26
6	MIPI_CSI0_RX_D2N	GND	NC	GND	25
7	GND	VCC_1V8	GND	VCC_1V8	24
8	MIPI_CSI0_RX_D3P	VCC_1V2/GND	NC	VCC_1V2/GND	23
9	MIPI_CSI0_RX_D3N	VCC_1V2	NC	VCC_1V2	22
10	GND	I2C6_SDA_M4	GND	I2C7_SDA_M2	21
11	MIPI_CAM3_CLKOUT	I2C6_SCL_M4	MIPI_CAM4_CLKOUT	I2C7_SCL_M2	20
12	MIPI_CAM3_RST_L	GND	MIPI_CAM4_RST_L	GND	19
13	XHS	VCC_2V8_AF	XHS	VCC_2V8_AF	18
14	MIPI_CAM3_PDN_L	VCC_2V8	MIPI_CAM4_PDN_L	VCC_2V8	17
15	FSIN	VSYNC	FSIN	VSYNC	16

3.15 TYPEC Interface

The development board supports a complete TYPEC interface and supports the following functions:

- TYPEC0_USB20_OTG in this interface can be used to download firmware
- Support TYPEC function
- Support DP1.4 output

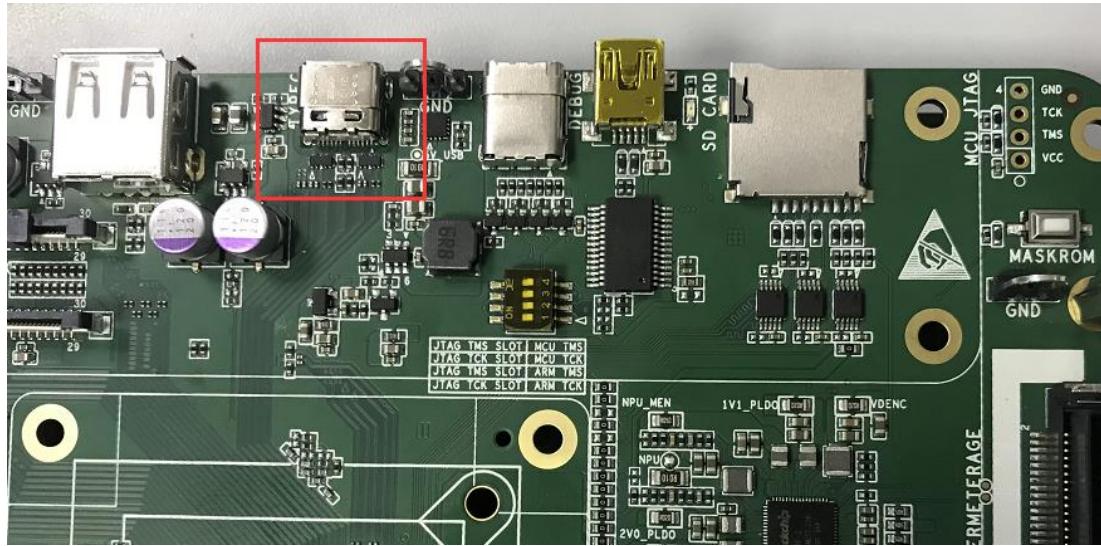


Figure 3-18 TypeC Interface

3.16 TF Card Interface

The development board supports one TF Card interface; the system memory capacity can be expanded, the data bus width is 4bits, and it supports SD3.0, MMC ver4.51.

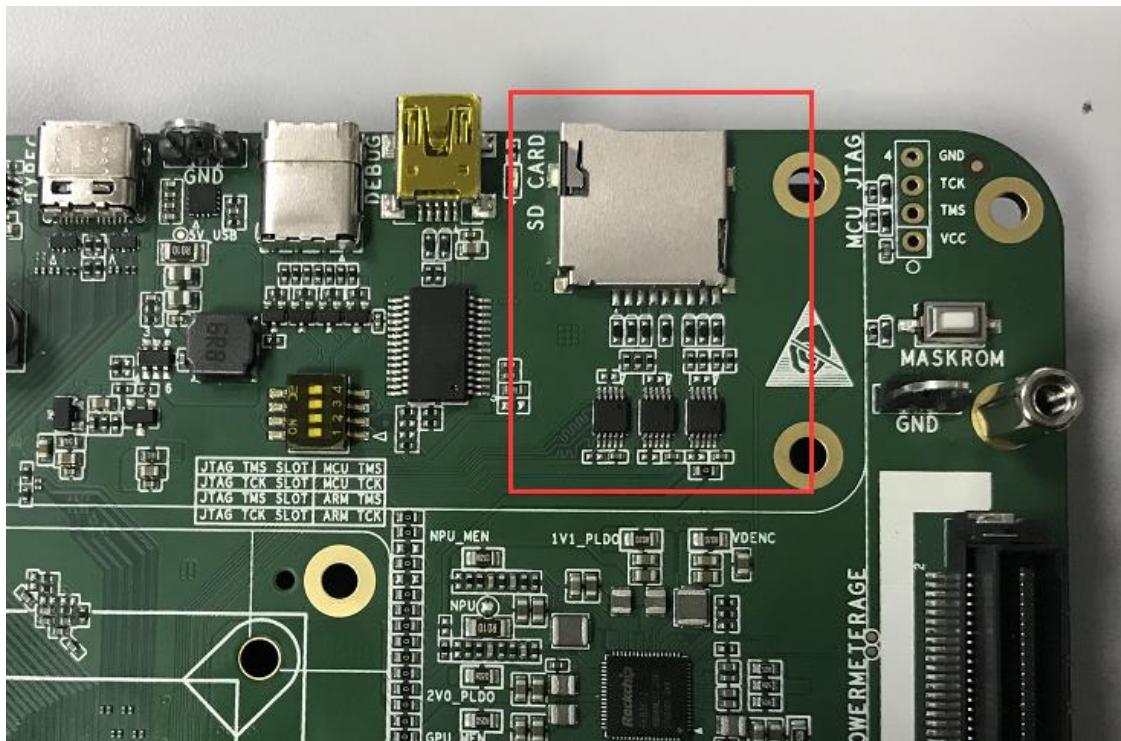


Figure 3-19 TF Card

3.17 USB2.0 Host Interface

The development board supports two channels of USB2.0, and supports the USB devices, such as mouse, U disk, and Bluetooth.

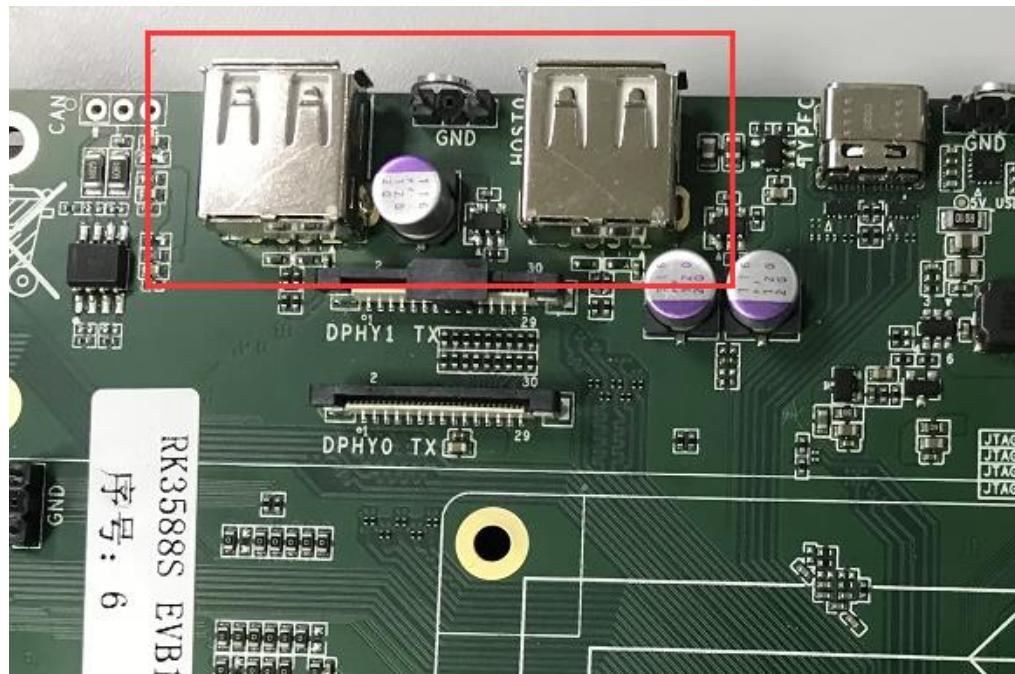


Figure 3-20 USB2.0 Host Interface

3.18 MASKROM Key

The development board can enter the MASKROM state through the MASKROM button, and upgrade the development board according to the method described in chapter 1.6.

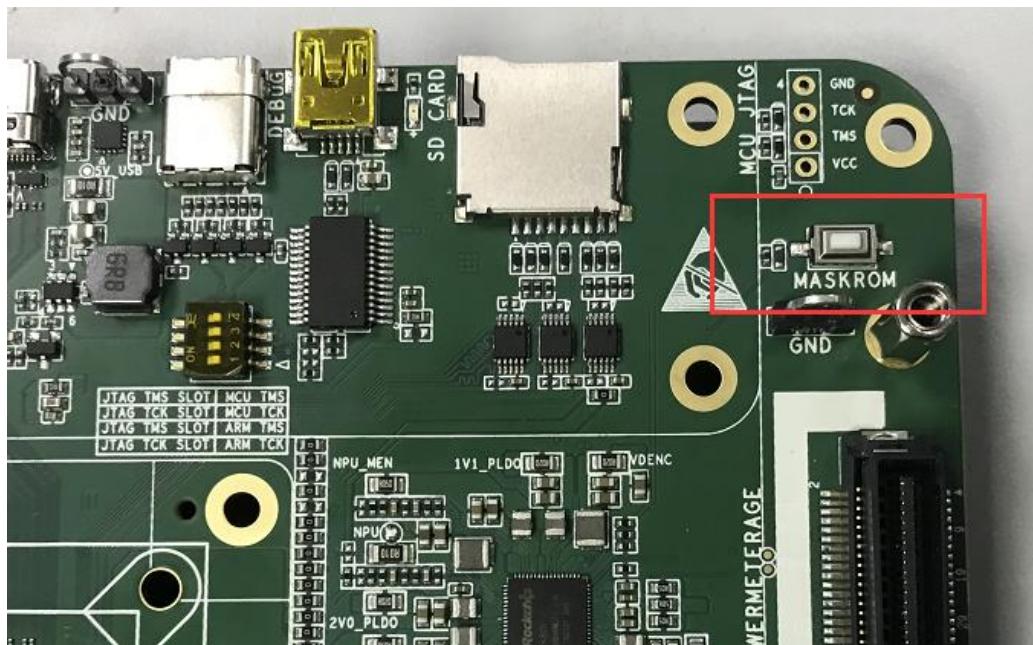


Figure 3-21 MASKROM key

3.19 CAN Interface

The development board reserves a CAN interface, and the 2.54mm interface is convenient for users to expand and use.

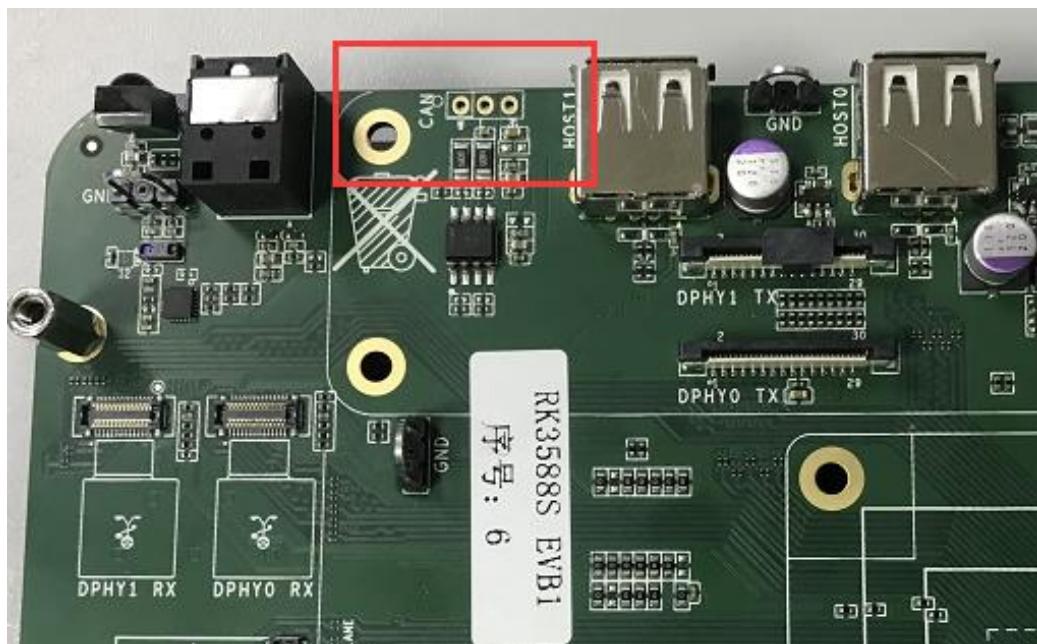


Figure 3-22 CAN Interface

3.20 MIPI TX Interface

The development board reserves 2 MIPI DPHY TX interfaces for convenience, which can support users to expand the LCD display. Please refer to Section 2.3.1 for interface encapsulation.

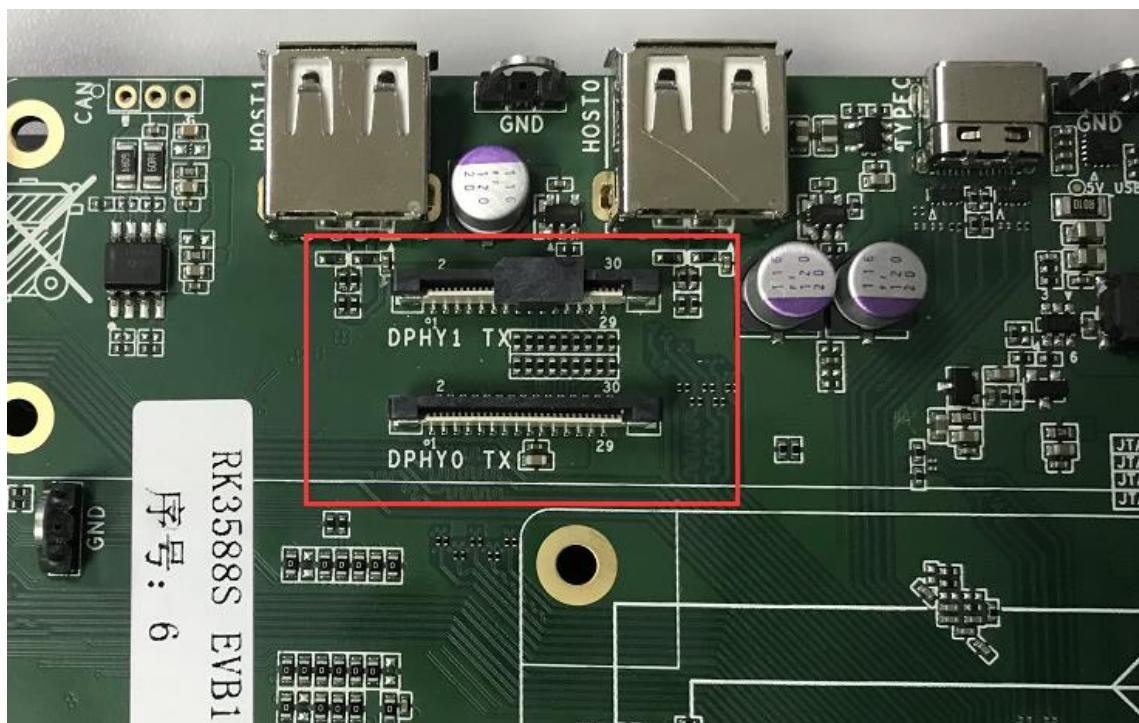


Figure 3-23 MIPI DPHY0/DPHY1 TX interface

The MIPI DPHY0/DPHY1 TX interface signal sequence is as follows:

Table 3-3 MIPI DPHY0/DPHY1 TX interface signal definition table

Pin	DPHY0 (J5500)		DPHY1 (J5501)		Pin
1	GND	MIPI_DPHY0_TX_D0N	GND	MIPI_DPHY1_TX_D0N	2
3	MIPI_DPHY0_TX_D0P	GND	MIPI_DPHY1_TX_D0P	GND	4
5	MIPI_DPHY0_TX_D1N	MIPI_DPHY0_TX_D1P	MIPI_DPHY1_TX_D1N	MIPI_DPHY1_TX_D1P	6
7	GND	MIPI_DPHY0_TX_CLKN	GND	MIPI_DPHY1_TX_CLKN	8
9	MIPI_DPHY0_TX_CLKP	GND	MIPI_DPHY1_TX_CLKP	GND	10
11	MIPI_DPHY0_TX_D2N	MIPI_DPHY0_TX_D2P	MIPI_DPHY1_TX_D2N	MIPI_DPHY1_TX_D2P	12
13	GND	MIPI_DPHY0_TX_D3N	GND	MIPI_DPHY1_TX_D3N	14
15	MIPI_DPHY0_TX_D3P	GND	MIPI_DPHY1_TX_D3P	GND	16
17	LCD_MIPI_BL_PWM12_M1	MIPI_TE0	LCD_MIPI_BL_PWM13_M1	MIPI_TE0	18
19	VCC3V3_LCD_MIPI	LCD_MIPI_RESET	VCC3V3_LCD_MIPI	LCD_MIPI_RESET	20
21	SARADC_VIN2_LCD_ID	LCD_MIPI_PWREN_H	SARADC_VIN2_LCD_ID	LCD_MIPI_PWREN_H	22
23	I2C4_SCL_M3_TP	I2C4_SDA_M3_TP	I2C4_SCL_M3_TP	I2C4_SDA_M3_TP	24
25	TP_INT_L	TP_RST_L	TP_INT_L	TP_RST_L	26
27	GND	VCC5V0_SYS	GND	VCC5V0_SYS	28
29	VCC5V0_SYS	VCC5V0_SYS	VCC5V0_SYS	VCC5V0_SYS	30

3.21 DMIC ARRAY Interface

The DMIC ARRAY interface is reserved for development, and it is led out through the 30pin FPC interface.

Please refer to chapter 2.3.1 for the interface package.

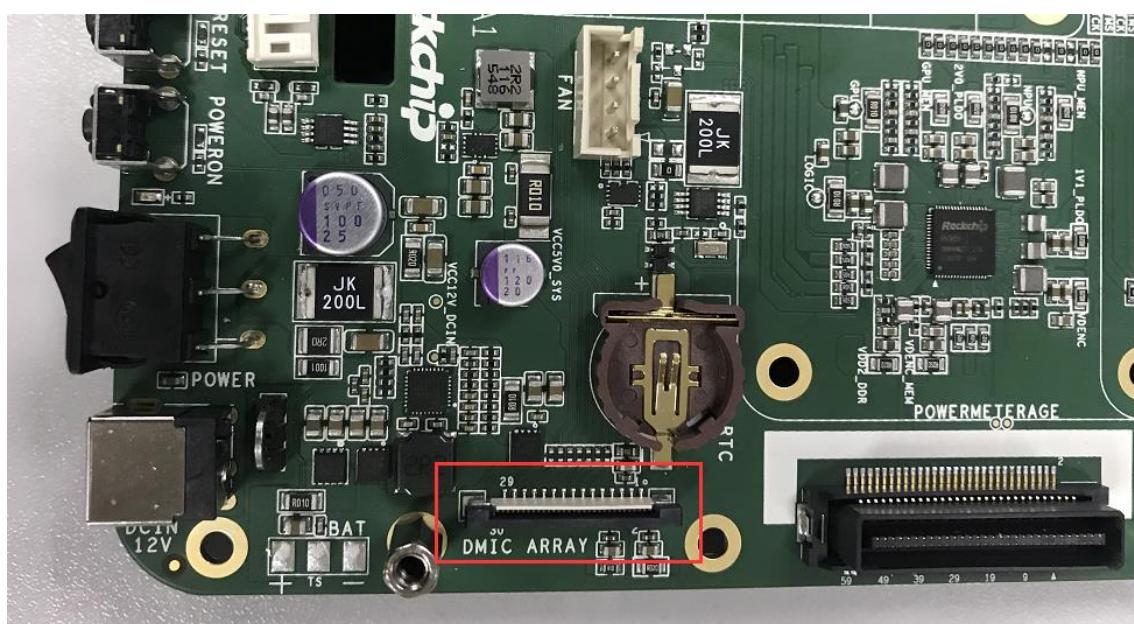


Figure 3-24 DMIC ARRAY Socket

The DMIC ARRAY interface signal sequence is as follows:

Table 3-4 DMIC ARRAY interface signal definition table

Pin	DMIC ARRAY (JP7700)		Pin
1	VCC_5V_0	VCC_5V_1	2
3	VCCIO	GND0	4
5	GND1	VCC_3V3	6
7	GND2	Codec_EN/GPIO_A_d (NC)	8
9	GND3	I2S_MCLK (NC)	10
11	GND4	I2S_SCLK_RX/PDM_CLK1	12
13	GND5	I2S_SCLK_TX (NC)	14
15	GND6	I2S_LRCK_RX/PDM_CLK0	16
17	GND7	I2S_LRCK_TX (NC)	18
19	I2S_SDO0 (NC)	I2S_SDO1 (NC)	20
21	I2S_SDO2 (NC)	I2S_SDO3 (NC)	22
23	I2S_SDI0/PDM_SDI0 (NC)	I2S_SDO1/PDM_SDI1	24
25	I2S_SDI2/PDM_SDI2	I2S_SDO3/PDM_SDI3	26
27	GND8	PA_EN/GPIO_B_d (NC)	28
29	I2C_SDA	I2C_CLK	30

4 Precautions

RK3588S EVB is suitable for laboratory or engineering environment, please read the following precautions before operation:

- Under no circumstances can the screen interface and expansion board be hot-swapped.
- Before unpacking and installing the development board, take necessary anti-static measures to avoid electrostatic discharge (ESD) damage to the development board hardware.
- When holding the development board, please hold the edge of the development board, and do not touch the exposed metal parts of the development board, so as to avoid damage to the components of the development board caused by static electricity.
- Please place the development board on a dry surface to keep them away from heat sources, electromagnetic interference sources and radiation sources, electromagnetic radiation sensitive equipment (such as medical equipment), etc.