

Reference Schematics For RK3588S

RK3588S_Tablet_REF_SCH

Main Functions Introduction

- 1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
- 2) PMIC: 1 x RK806-1+DiscretePower
- 3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
- 4) ROM: eMMC5.1(Default) or SPI Falsh
- 5) Support: 1 x Micro SD Card3.0
- 6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
- 7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
- 8) Support: 2 x 2Lanes MIPI DPHY RX Camera
- 9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
- 10) Support: 2 x 4Lanes MIPI D/CPHY TX
- 11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
- 12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
- 13) Support: 2 x PDM MIC Array
- 14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

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Project:	RK3588S_Tablet_REF		
File:	00.Cover Page		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	1 of 53		

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Note
 The power suffix S0 or S3 means:
S3: Keep power On during sleeping
S0:Power off during sleeping

Generate Bill of Materials

Header:
 Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:
 {Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
 1. DNP stands for component not mounted temporarily
 2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
 Please use our recommended components to avoid too many changes.
 For more informations about the second source,please refer to our AVL.

Revision History

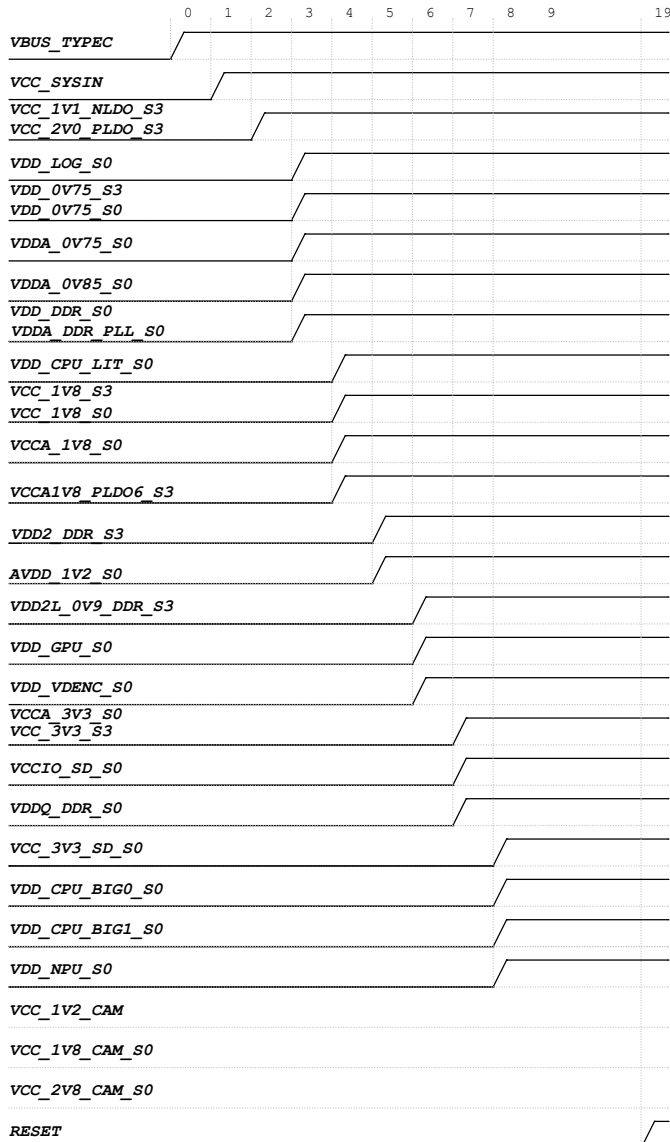
Version	Date	By	Change Description	Approved
V1.0	2022-01-05	Joseph.We	1:Revision preliminary version	
V1.1	2022-02-18	Joseph.We	1.C1604,C1612的电容改成1uF/4V。 2.为了减少待机功耗，将PMUIO2电源域改成1.8V，此IO域对应外设IO电压相应修改 3.把L2203, L2205, L2207, L2300, L2301, L2302电感器由0.22uH(TDK)改为0.24uH(Sunlord); L2201的电感器由0.22uH(TDK)改为0.22uH (Sunlord), 封装IND_404020。 4.HDMI eARC功能不支持，相关eARC网络改成HDMI0_TX_SBDP/N	

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Project:	RK3588S_Tablet_REF		
File:	02.Revision History		
Date:	Wednesday, February 23, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
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Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

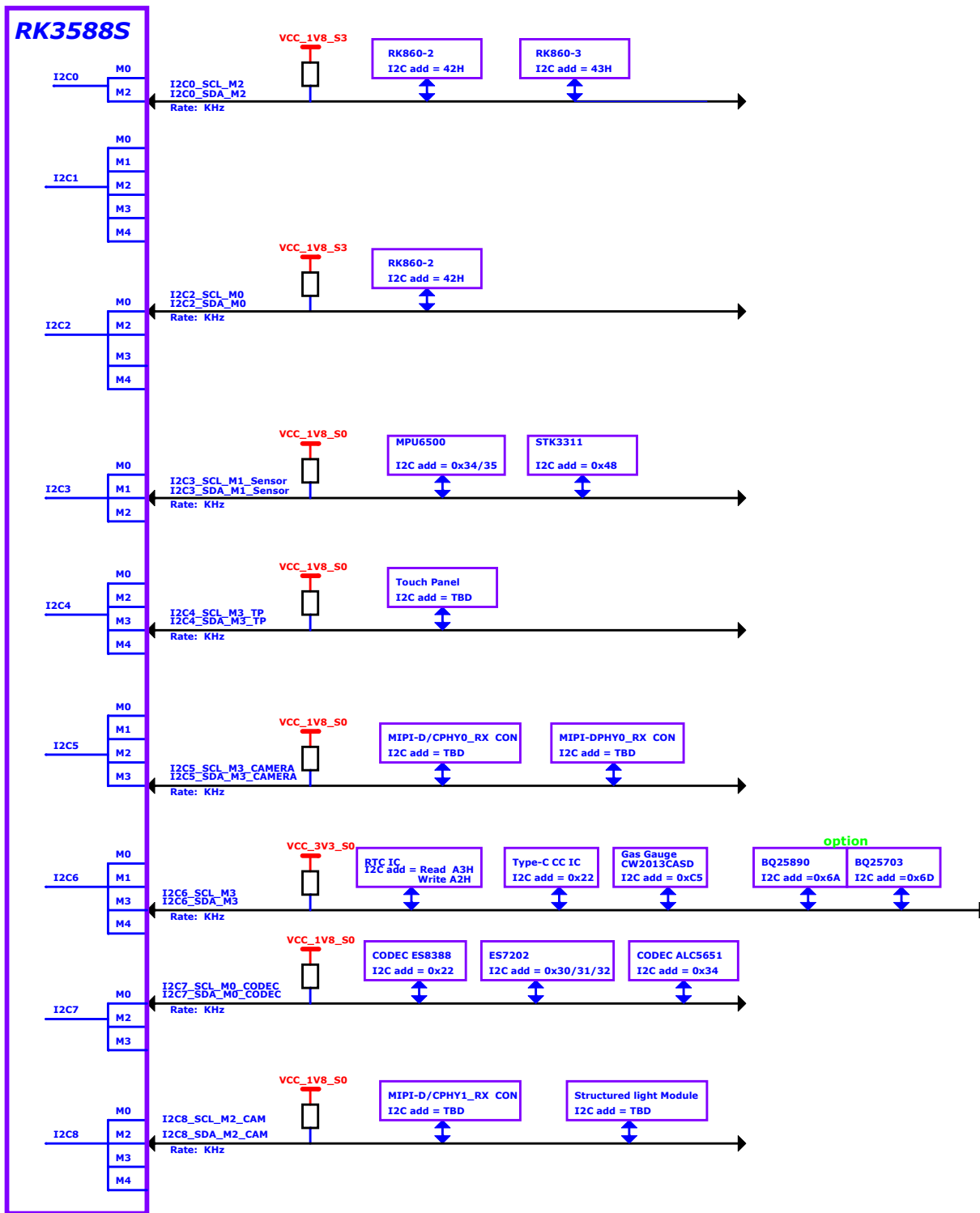
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
	Pin V35 V36		PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin AC35	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
	Pin AC36				
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_IO_SD	1.8V/3.3V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_3V3_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin A134	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin A133 AM33		VCCIO6	VCC_3V3_S0	3.3V

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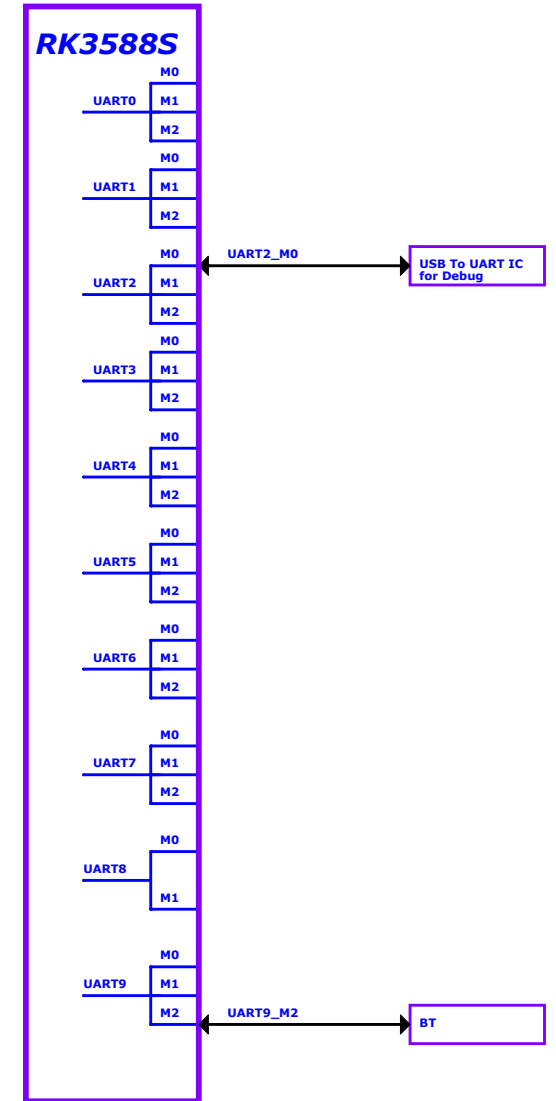
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Project:	RK3588S_Tablet_REF			
File:	05.System Power Sequence			
Date:	Monday, February 21, 2022	Rev:	V10	
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet: 6 of 53

I2C MAP



UART MAP

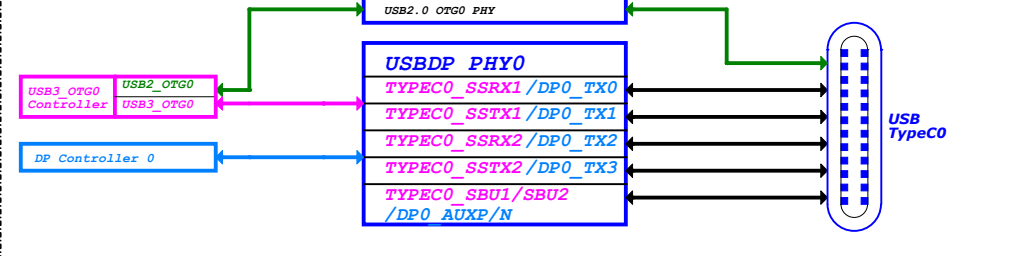


USB Controller Configure Table

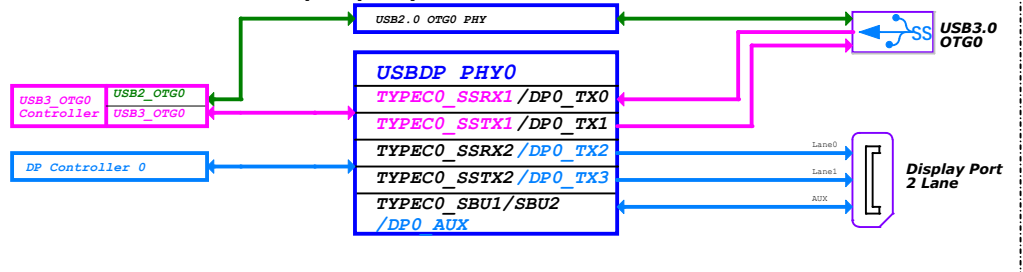
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEPC0_SSR1/DP0_AUX0	TYPEPC0_SSR1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEPC0_SSR2/DP0_AUX1	TYPEPC0_SSR2	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1	DP0_AUX1
	TYPEPC0_SSRX1/DP0_TX0	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P
	TYPEPC0_SSRX1/DP0_TX1	TYPEPC0_SSRX1N	DP0_TX1N	DP0_TX1N	TYPEPC0_SSRX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N
USB20 OTG0 Device or Host	TYPEPC0_SSRX2/DP0_TX2	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSRX2/DP0_TX3	TYPEPC0_SSRX2N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSRX2N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N
	TYPEPC0_SSTX1/DP0_TX1P	TYPEPC0_SSTX1P	DP0_TX1P	DP0_TX1P	TYPEPC0_SSTX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P
	TYPEPC0_SSTX1/DP0_TX1N	TYPEPC0_SSTX1N	DP0_TX1N	DP0_TX1N	TYPEPC0_SSTX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N
USB30 OTG2 Device or Host	TYPEPC0_SSTX2/DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSTX2/DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
	TYPEPC0_SSTX2/DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC0_SSTX2/DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N
USB20 HOST0	TYPEPC0_SSTX2P/DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC0_SSTX2N/DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N
USB20 HOST1	TYPEPC0_SSTX2P/DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	TYPEPC0_SSTX2P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC0_SSTX2N/DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSTX2N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N

Note:
 DP Lane swap enable
 0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
 1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

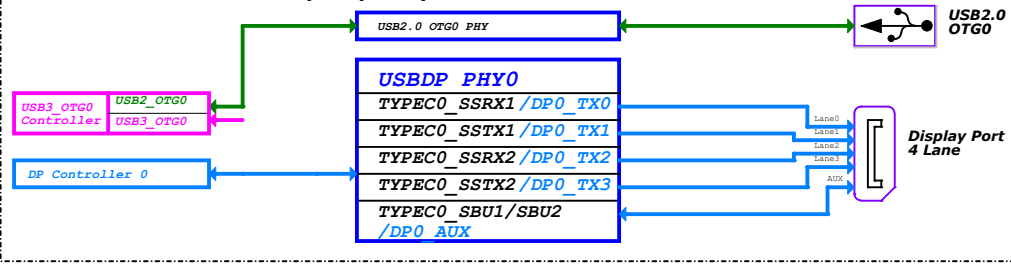
Config0: TypeC0 (With DP function)



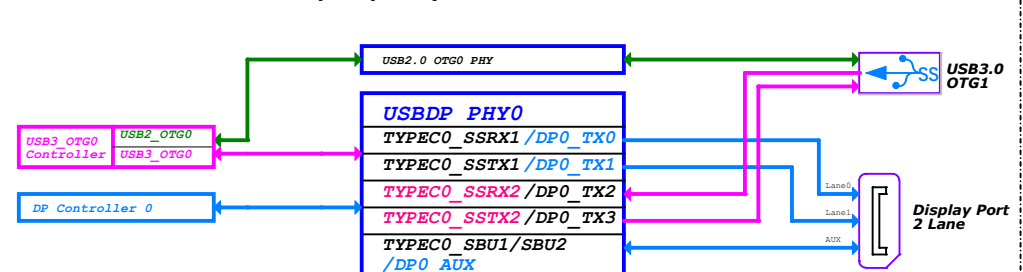
Config3:(Default) USB3.0 OTG0 + DP0 2Lane(Swap ON)



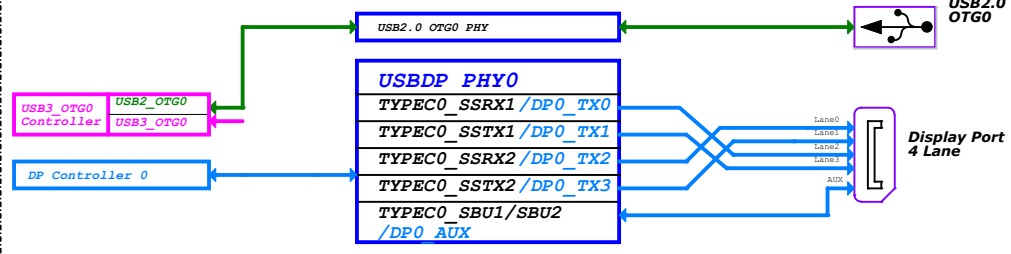
Config1: USB2.0 OTG0 + DP0 4Lane(Swap OFF)



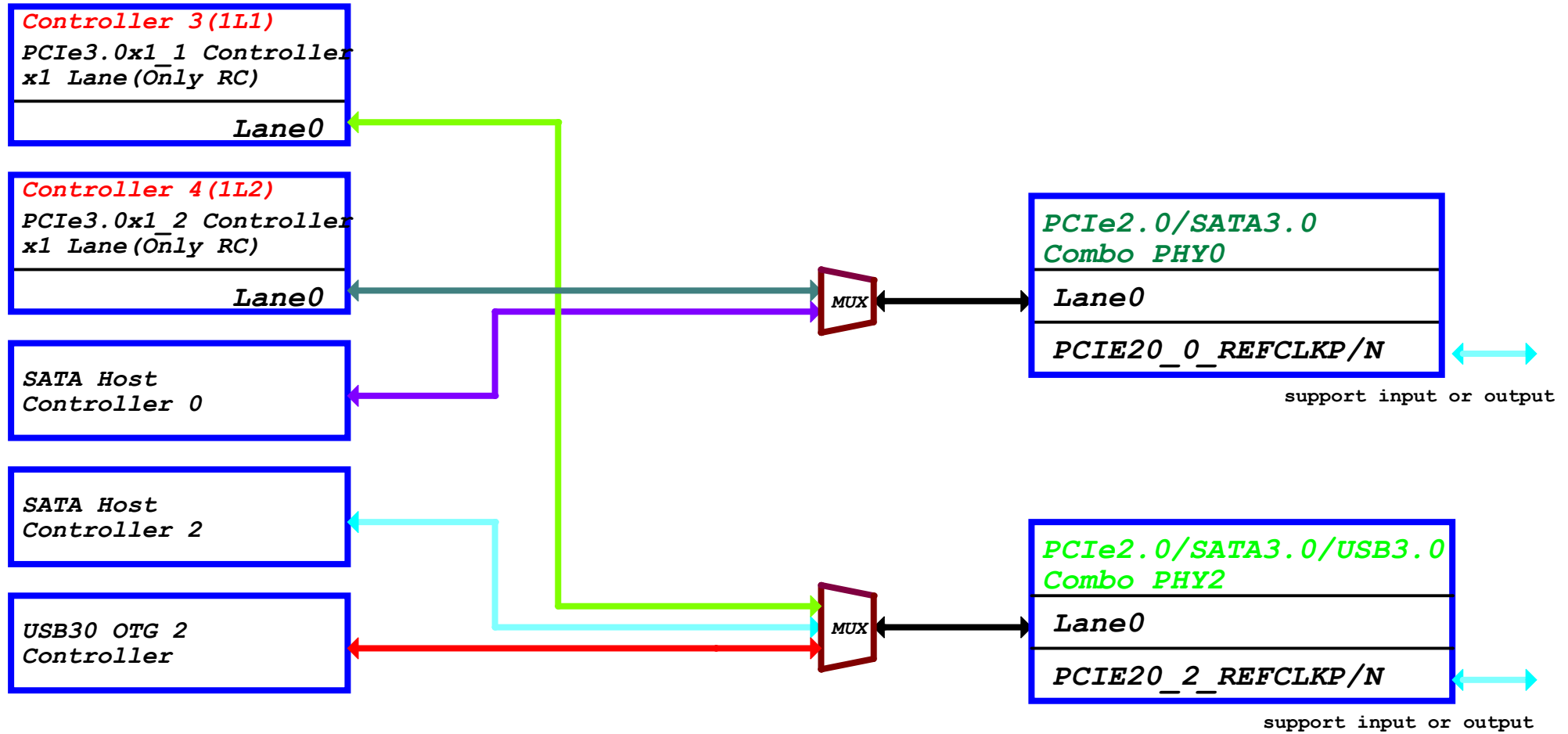
Config4: USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2: USB2.0 OTG0 + DP0 4Lane(Swap ON)



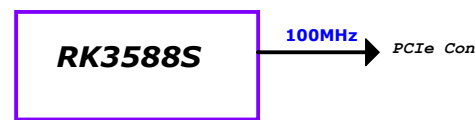
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



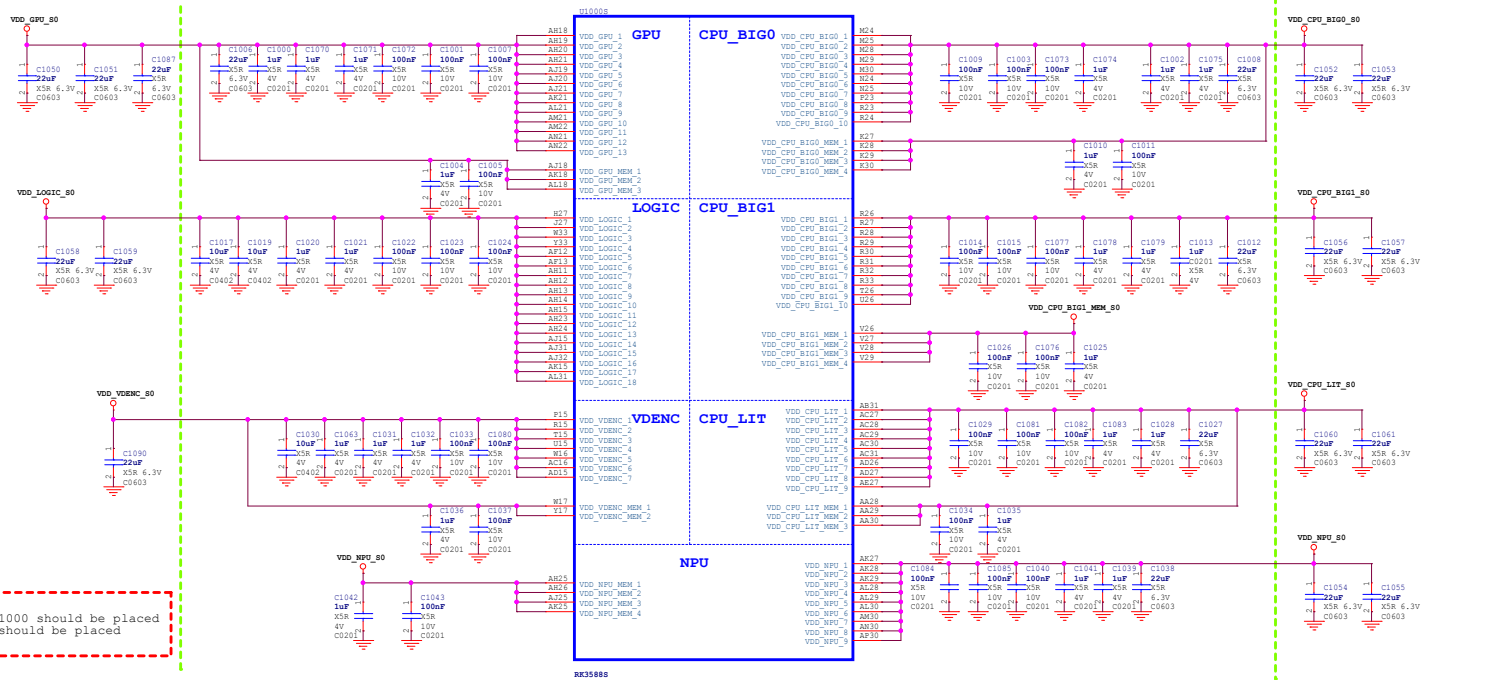
Note:
PCIE20*_REFCLKP/N is output or input gpio
M*=Mean to M0 or M1 or M2, It's the same source, Just multiplex to M0 or M1 or M2, Only use one at the same time.

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Project:	RK3588S_Tablet_REF		
File:	08.PCIE Fun Map		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	9 of 53

RK3588S (Power&Gnd)



Note:
The Caps between green line and A1000 should be placed under the U10000 package. Other caps should be placed close to the U10000 package.

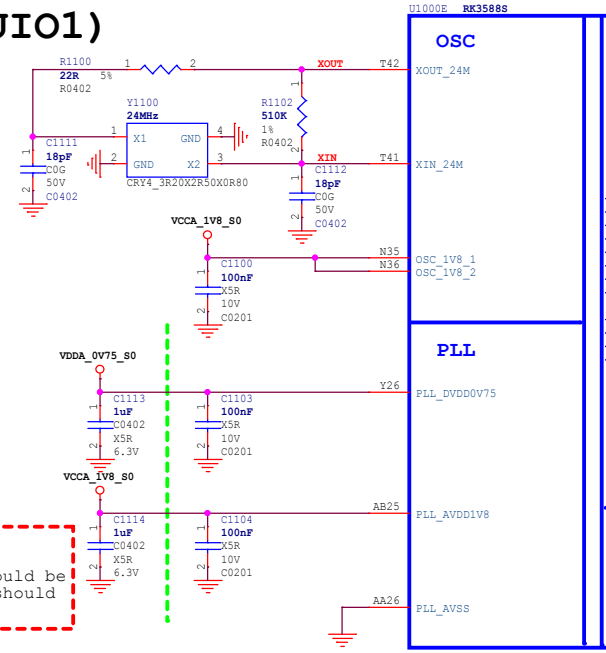
U10000		U10000		U10000		U10000		U10000		U10000		U10000		U10000	
Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value
A1	V88_1	A22	V88_10	B1	V88_101	B12	V88_102	B13	V88_103	B14	V88_104	B15	V88_105	B16	V88_106
A2	V88_2	A23	V88_11	B2	V88_107	B22	V88_108	B23	V88_109	B24	V88_110	B25	V88_111	B26	V88_112
A3	V88_3	A24	V88_12	B3	V88_113	B32	V88_114	B33	V88_115	B34	V88_116	B35	V88_117	B36	V88_118
A4	V88_4	A25	V88_13	B4	V88_119	B42	V88_120	B43	V88_121	B44	V88_122	B45	V88_123	B46	V88_124
A5	V88_5	A26	V88_14	B5	V88_125	B52	V88_126	B53	V88_127	B54	V88_128	B55	V88_129	B56	V88_130
A6	V88_6	A27	V88_15	B6	V88_131	B62	V88_132	B63	V88_133	B64	V88_134	B65	V88_135	B66	V88_136
A7	V88_7	A28	V88_16	B7	V88_137	B72	V88_138	B73	V88_139	B74	V88_140	B75	V88_141	B76	V88_142
A8	V88_8	A29	V88_17	B8	V88_143	B82	V88_144	B83	V88_145	B84	V88_146	B85	V88_147	B86	V88_148
A9	V88_9	A30	V88_18	B9	V88_149	B92	V88_150	B93	V88_151	B94	V88_152	B95	V88_153	B96	V88_154
A10	V88_10	A31	V88_19	B10	V88_155	B102	V88_156	B103	V88_157	B104	V88_158	B105	V88_159	B106	V88_160
A11	V88_11	A32	V88_20	B11	V88_161	B112	V88_162	B113	V88_163	B114	V88_164	B115	V88_165	B116	V88_166
A12	V88_12	A33	V88_21	B12	V88_167	B122	V88_168	B123	V88_169	B124	V88_170	B125	V88_171	B126	V88_172
A13	V88_13	A34	V88_22	B13	V88_173	B132	V88_174	B133	V88_175	B134	V88_176	B135	V88_177	B136	V88_178
A14	V88_14	A35	V88_23	B14	V88_179	B142	V88_180	B143	V88_181	B144	V88_182	B145	V88_183	B146	V88_184
A15	V88_15	A36	V88_24	B15	V88_185	B152	V88_186	B153	V88_187	B154	V88_188	B155	V88_189	B156	V88_190
A16	V88_16	A37	V88_25	B16	V88_191	B162	V88_192	B163	V88_193	B164	V88_194	B165	V88_195	B166	V88_196
A17	V88_17	A38	V88_26	B17	V88_197	B172	V88_198	B173	V88_199	B174	V88_200	B175	V88_201	B176	V88_202
A18	V88_18	A39	V88_27	B18	V88_203	B182	V88_204	B183	V88_205	B184	V88_206	B185	V88_207	B186	V88_208
A19	V88_19	A40	V88_28	B19	V88_209	B192	V88_210	B193	V88_211	B194	V88_212	B195	V88_213	B196	V88_214
A20	V88_20	A41	V88_29	B20	V88_215	B202	V88_216	B203	V88_217	B204	V88_218	B205	V88_219	B206	V88_220
A21	V88_21	A42	V88_30	B21	V88_221	B212	V88_222	B213	V88_223	B214	V88_224	B215	V88_225	B216	V88_226
A22	V88_22	A43	V88_31	B22	V88_227	B222	V88_228	B223	V88_229	B224	V88_230	B225	V88_231	B226	V88_232
A23	V88_23	A44	V88_32	B23	V88_233	B232	V88_234	B233	V88_235	B234	V88_236	B235	V88_237	B236	V88_238
A24	V88_24	A45	V88_33	B24	V88_239	B242	V88_240	B243	V88_241	B244	V88_242	B245	V88_243	B246	V88_244
A25	V88_25	A46	V88_34	B25	V88_245	B252	V88_246	B253	V88_247	B254	V88_248	B255	V88_249	B256	V88_250
A26	V88_26	A47	V88_35	B26	V88_251	B262	V88_252	B263	V88_253	B264	V88_254	B265	V88_255	B266	V88_256
A27	V88_27	A48	V88_36	B27	V88_257	B272	V88_258	B273	V88_259	B274	V88_260	B275	V88_261	B276	V88_262
A28	V88_28	A49	V88_37	B28	V88_263	B282	V88_264	B283	V88_265	B284	V88_266	B285	V88_267	B286	V88_268
A29	V88_29	A50	V88_38	B29	V88_269	B292	V88_270	B293	V88_271	B294	V88_272	B295	V88_273	B296	V88_274
A30	V88_30	A51	V88_39	B30	V88_275	B302	V88_276	B303	V88_277	B304	V88_278	B305	V88_279	B306	V88_280
A31	V88_31	A52	V88_40	B31	V88_281	B312	V88_282	B313	V88_283	B314	V88_284	B315	V88_285	B316	V88_286
A32	V88_32	A53	V88_41	B32	V88_287	B322	V88_288	B323	V88_289	B324	V88_290	B325	V88_291	B326	V88_292
A33	V88_33	A54	V88_42	B33	V88_293	B332	V88_294	B333	V88_295	B334	V88_296	B335	V88_297	B336	V88_298
A34	V88_34	A55	V88_43	B34	V88_299	B342	V88_300	B343	V88_301	B344	V88_302	B345	V88_303	B346	V88_304
A35	V88_35	A56	V88_44	B35	V88_305	B352	V88_306	B353	V88_307	B354	V88_308	B355	V88_309	B356	V88_310
A36	V88_36	A57	V88_45	B36	V88_311	B362	V88_312	B363	V88_313	B364	V88_314	B365	V88_315	B366	V88_316
A37	V88_37	A58	V88_46	B37	V88_317	B372	V88_318	B373	V88_319	B374	V88_320	B375	V88_321	B376	V88_322
A38	V88_38	A59	V88_47	B38	V88_323	B382	V88_324	B383	V88_325	B384	V88_326	B385	V88_327	B386	V88_328
A39	V88_39	A60	V88_48	B39	V88_329	B392	V88_330	B393	V88_331	B394	V88_332	B395	V88_333	B396	V88_334
A40	V88_40	A61	V88_49	B40	V88_335	B402	V88_336	B403	V88_337	B404	V88_338	B405	V88_339	B406	V88_340
A41	V88_41	A62	V88_50	B41	V88_341	B412	V88_342	B413	V88_343	B414	V88_344	B415	V88_345	B416	V88_346
A42	V88_42	A63	V88_51	B42	V88_347	B422	V88_348	B423	V88_349	B424	V88_350	B425	V88_351	B426	V88_352
A43	V88_43	A64	V88_52	B43	V88_353	B432	V88_354	B433	V88_355	B434	V88_356	B435	V88_357	B436	V88_358
A44	V88_44	A65	V88_53	B44	V88_359	B442	V88_360	B443	V88_361	B444	V88_362	B445	V88_363	B446	V88_364
A45	V88_45	A66	V88_54	B45	V88_365	B452	V88_366	B453	V88_367	B454	V88_368	B455	V88_369	B456	V88_370
A46	V88_46	A67	V88_55	B46	V88_371	B462	V88_372	B463	V88_373	B464	V88_374	B465	V88_375	B466	V88_376
A47	V88_47	A68	V88_56	B47	V88_377	B472	V88_378	B473	V88_379	B474	V88_380	B475	V88_381	B476	V88_382
A48	V88_48	A69	V88_57	B48	V88_383	B482	V88_384	B483	V88_385	B484	V88_386	B485	V88_387	B486	V88_388
A49	V88_49	A70	V88_58	B49	V88_389	B492	V88_390	B493	V88_391	B494	V88_392	B495	V88_393	B496	V88_394
A50	V88_50	A71	V88_59	B50	V88_395	B502	V88_396	B503	V88_397	B504	V88_398	B505	V88_399	B506	V88_400

RK3588S (OSC/PLL/PMUIO1)

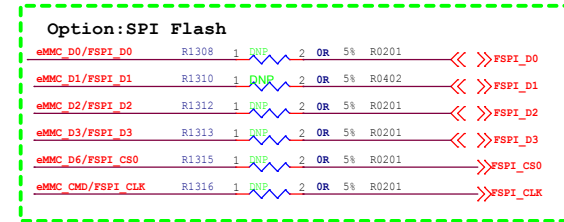
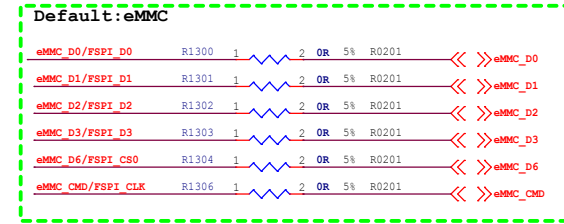
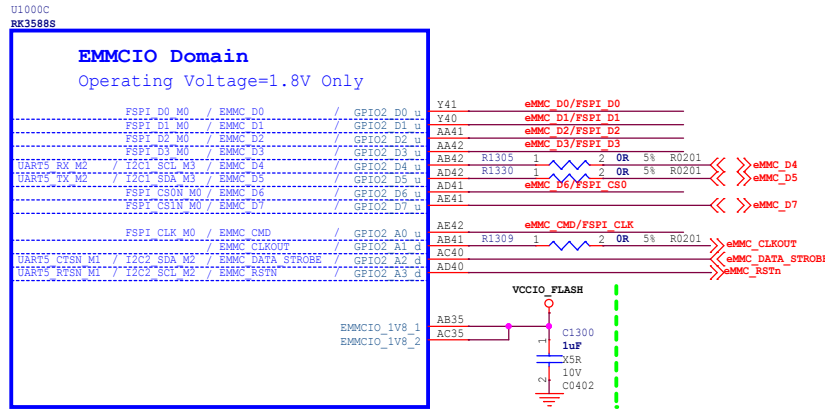
Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

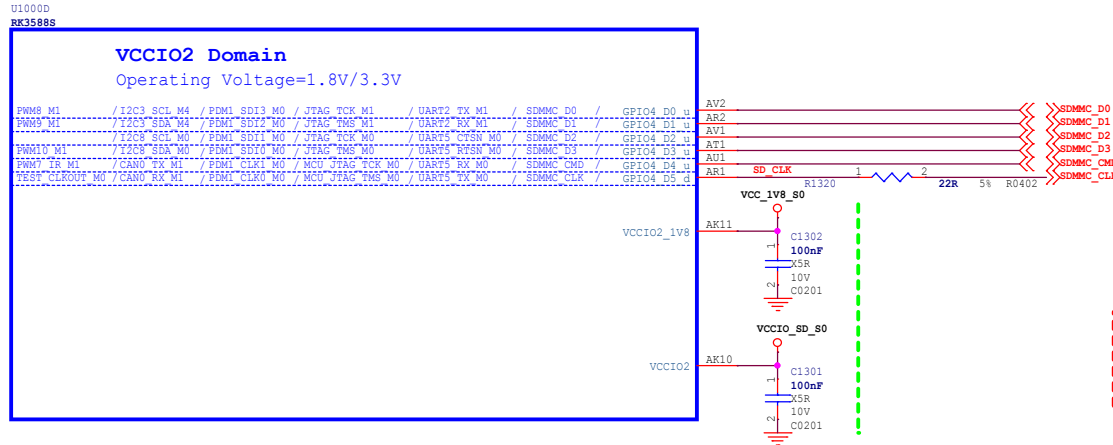
$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$
Total CL=12pF



RK3588S (EMMCIO Domain)



RK3588S (VCCIO2 Domain)



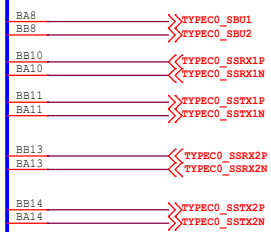
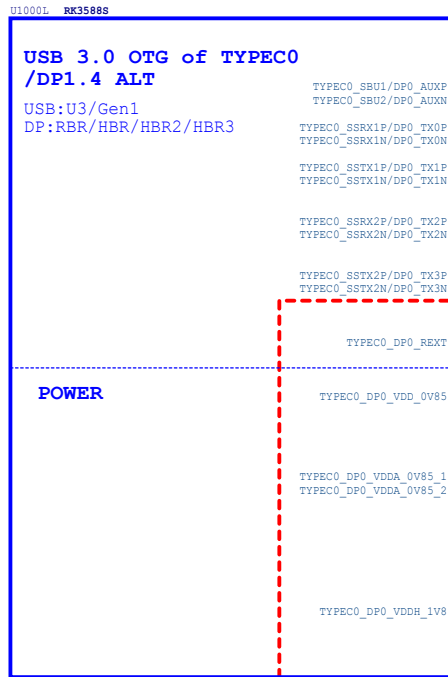
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (USB3.0/DP1.4)

USB30/DP1.4 Alt Mode Configuration

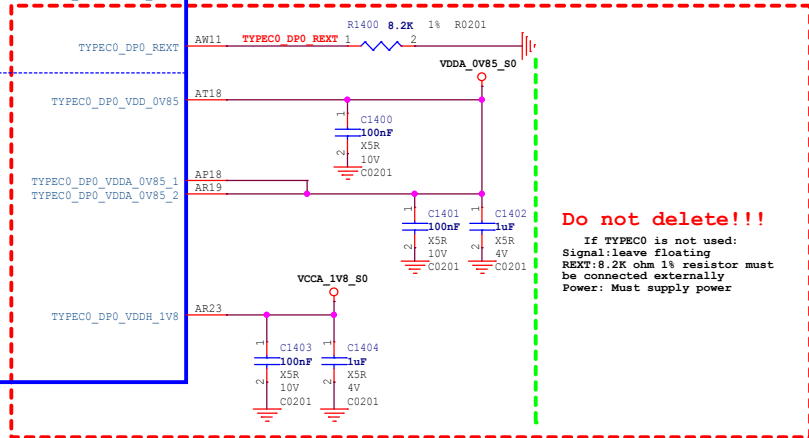
Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP: Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



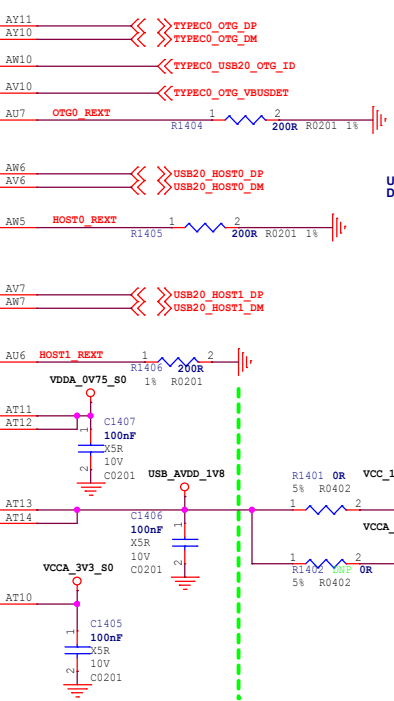
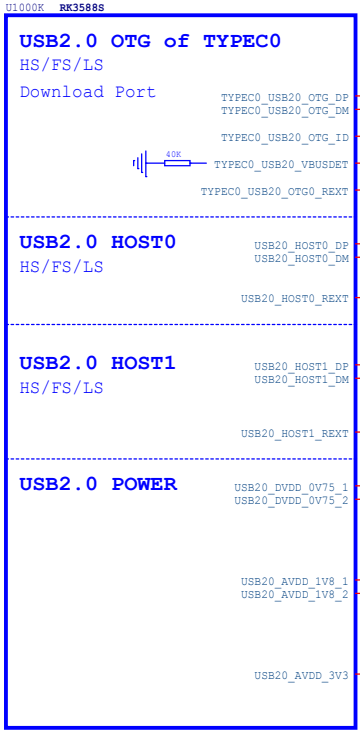
TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +/-10%
For Typec

USB30 Differential Pair: DATE:90 Ohm +/-10%
DP Differential Pair: DATE:100 Ohm +/-10%
For USB30 For DP



Do not delete!!!
If TYPECO is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

RK3588S (USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETPin voltage range <=3.3V.

Note:
TYPECO_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

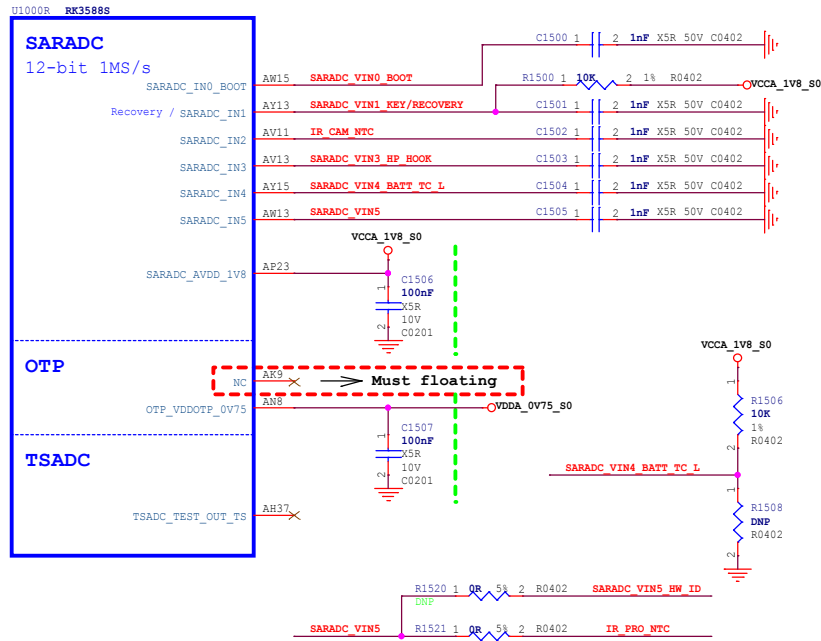
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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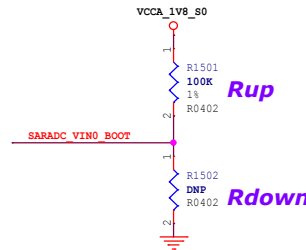
Project:	RK3588S_Tablet_REF
File:	14.RK3588S_USB20/USB30/DP_PHY
Date:	Monday, February 21, 2022
Designed by:	Joseph
Reviewed by:	<Checker>
Rev:	V10
Sheet:	14 of 53

RK3588S (SARADC/OTP/TSADC)

- < SARADC_VIN1_KEY/RECOVERY
- < IR_CAM_NTC
- < SARADC_VIN3_HP_HOOK
- < SARADC_VIN4_BATT_TC_L
- < SARADC_VIN0_BOOT
- < IR_PRO_NTC
- < IR_CAM_NTC

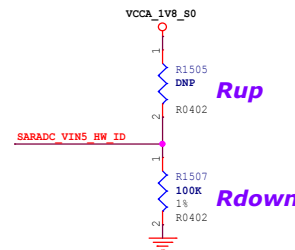


BOOT MODE CONFIG



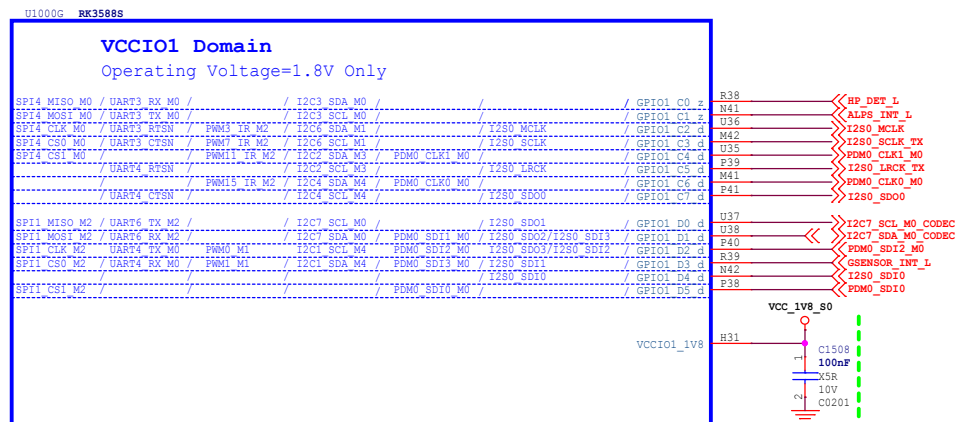
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI M2-FSPI M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S (VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

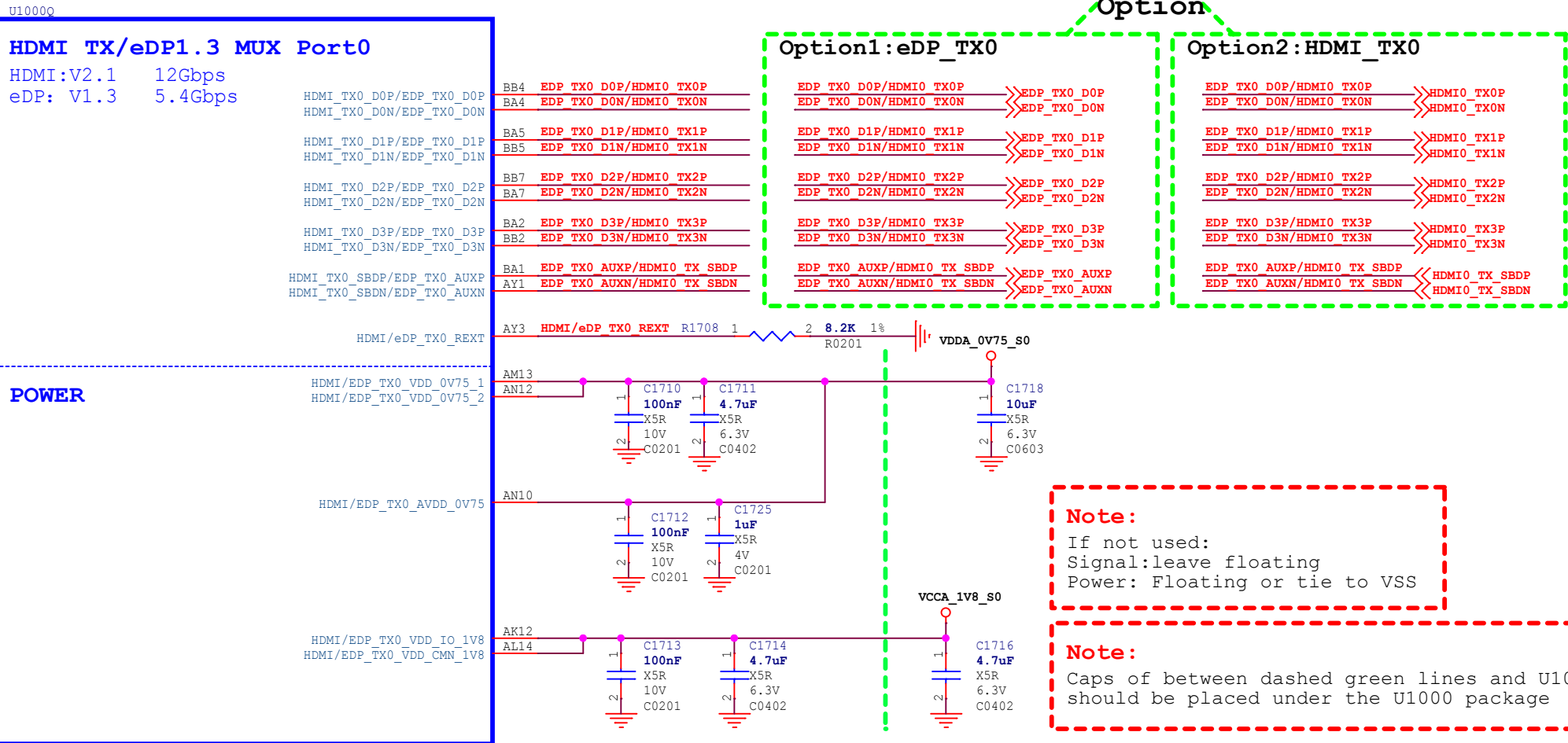
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Project: RK3588S_Tablet_REF
File: 15.RK3588S_SARADC1.8V_GPIO
Date: Monday, February 21, 2022
Designed by: Joseph
Reviewed by: <Checker>
Rev: V10
Sheet: 15 of 53

RK3588S (HDMI2.1 TX/eDP1.3 TX)

Note:

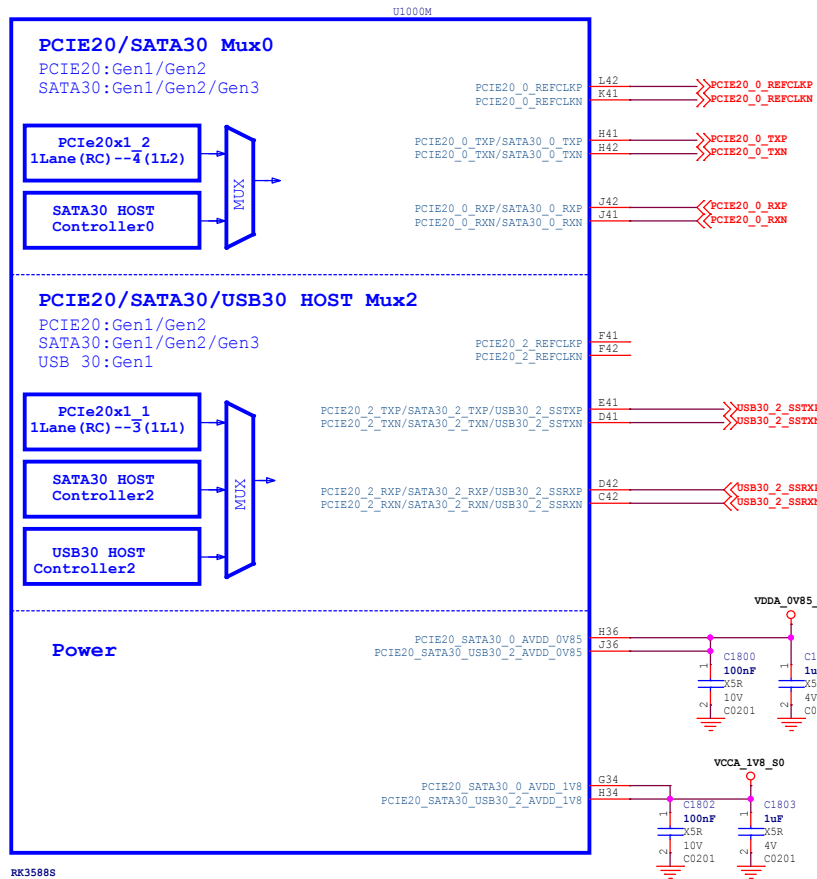
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



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Project:	RK3588S_Tablet_REF		
File:	17.RK3588S_HDMI/eDP Interface		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	17 of 53

RK3588S (PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm±10%
SATA30: 100 Ohm±10%
USB30: 90ohm±10%

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package

PCIE2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

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Project:	RK3588S_Tablet_REF		
File:	18.RK3588S_PCIE2/SATA3/USB3_PHY		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	18 of 53		

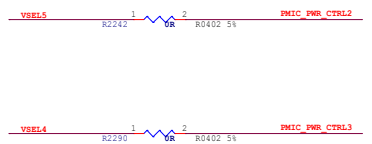
PMIC1 RK806-1



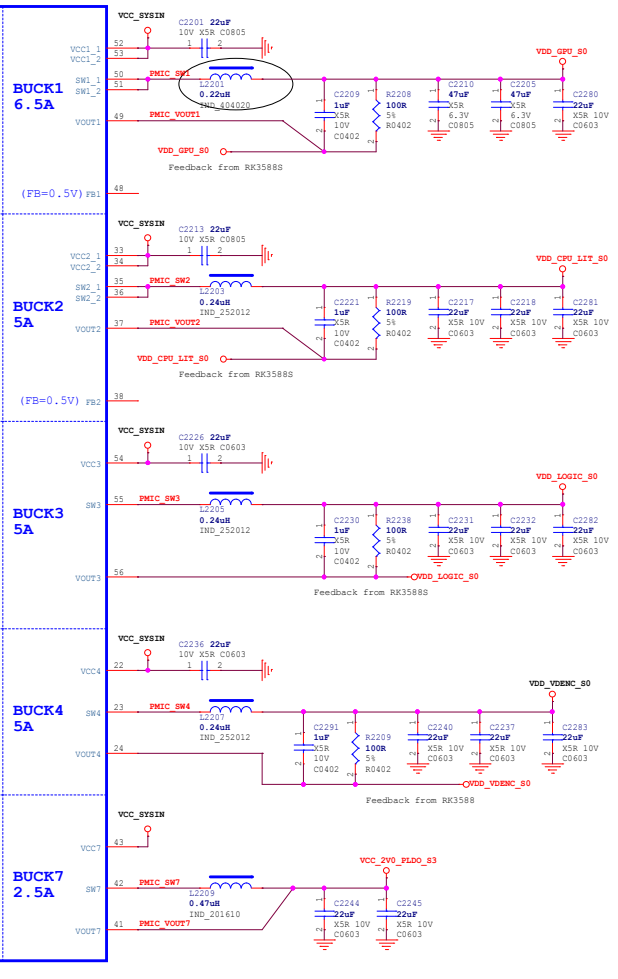
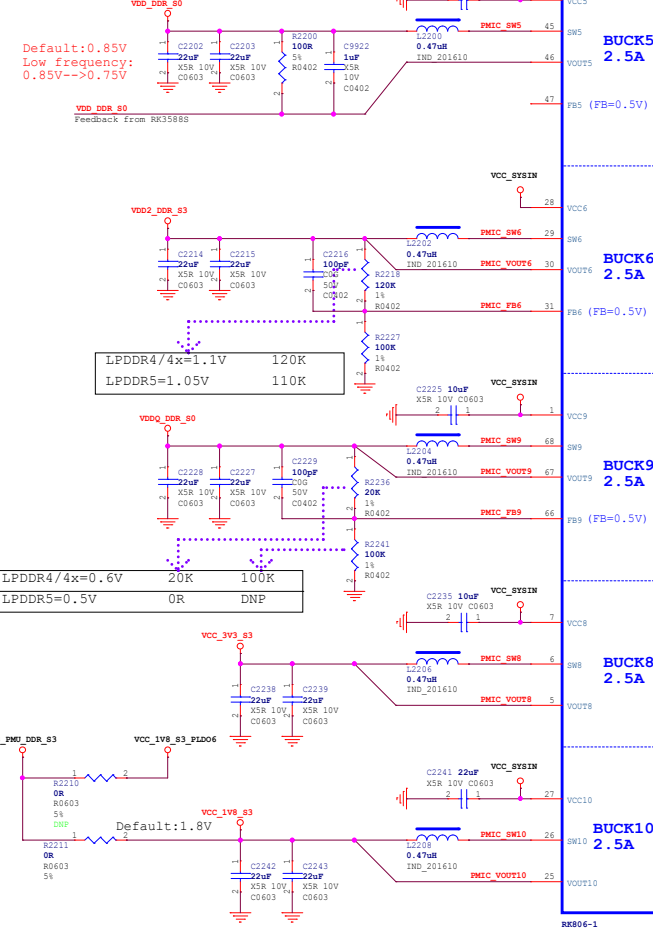
IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted. Replacing TVS mode is not recommended. If must, please choose the same specifications
 Operating Supply Voltage: ± 5V(0.5-20V)
 PeakPulse Current: >10A (tpr<20us)
 Surge Clamping Voltage: <6.5V

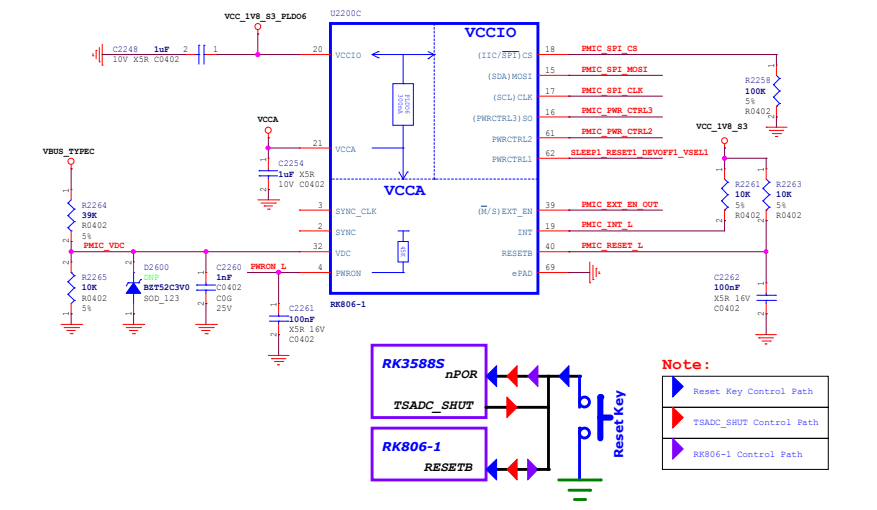
DO NOT DELETE IT!



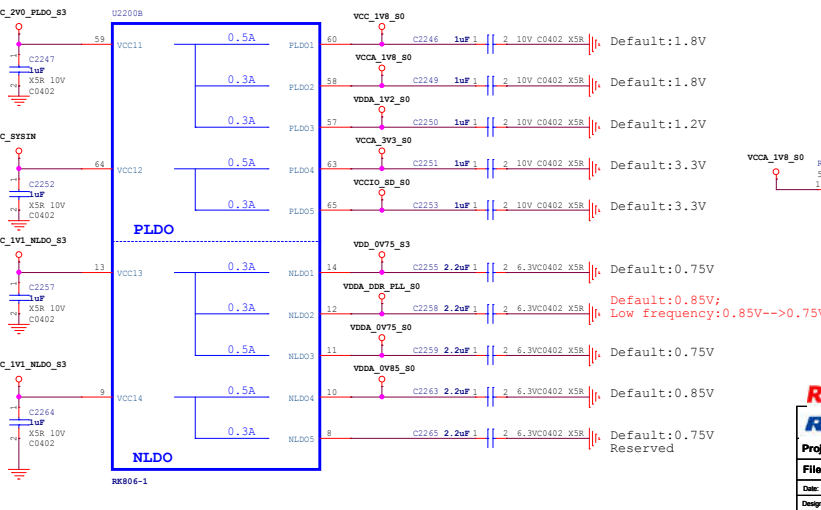
PMIC RK806-1 BUCK



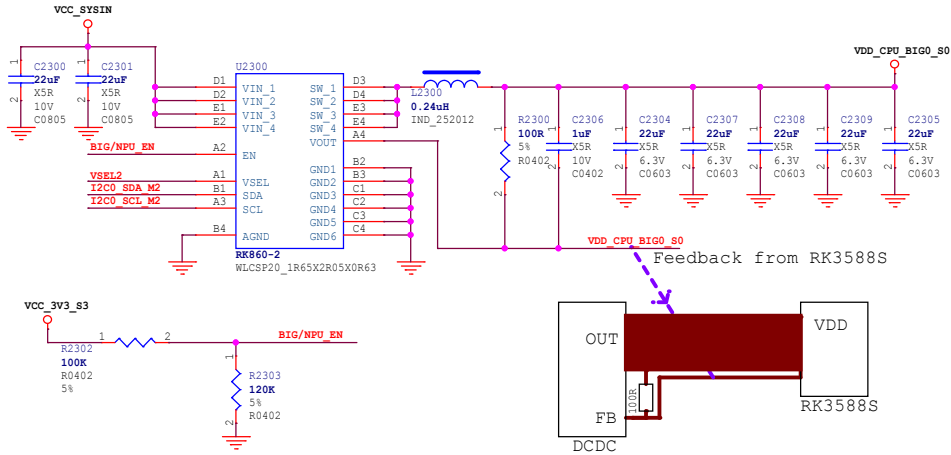
PMIC RK806-1 Management



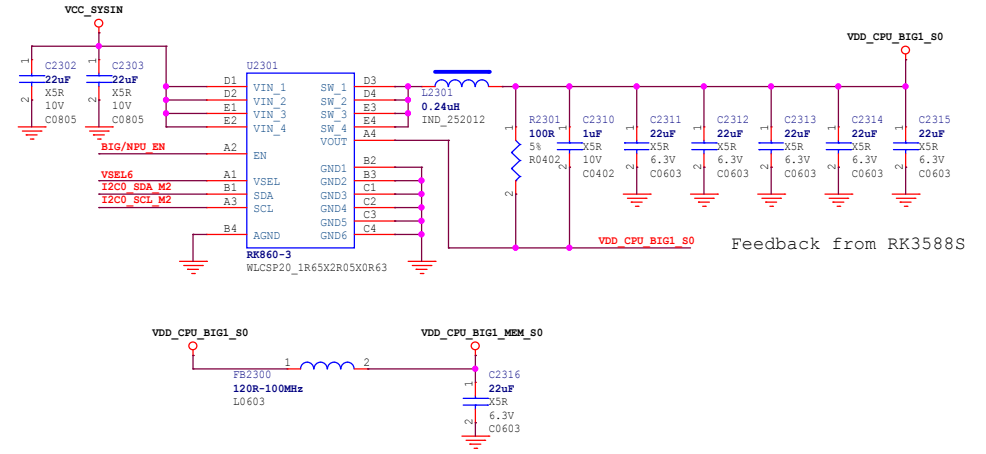
PMIC RK806-1 LDO



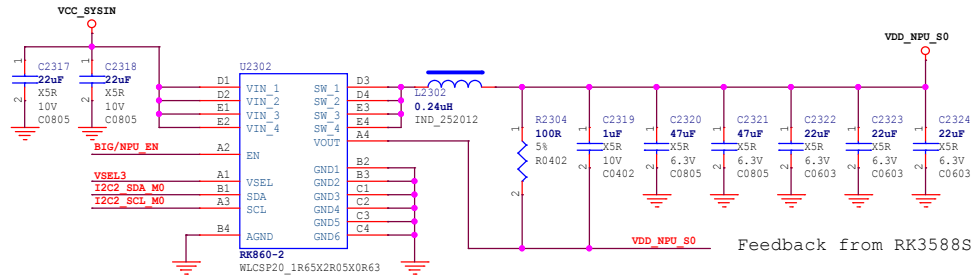
VDD_CPU_BIG0



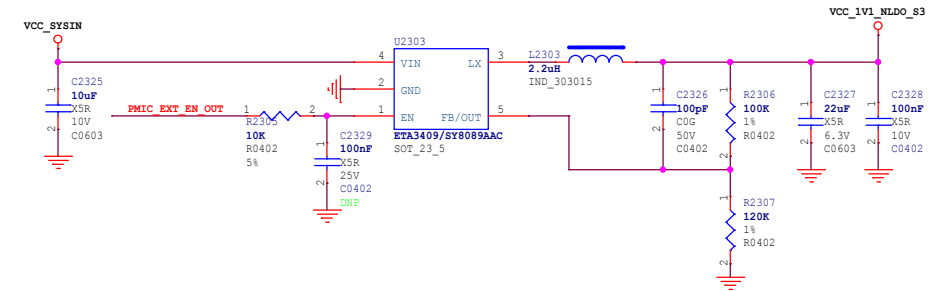
VDD_CPU_BIG1



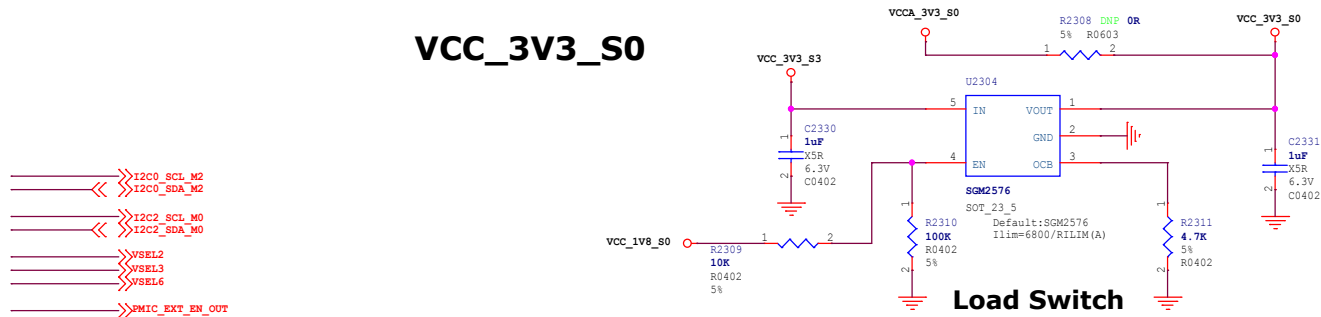
VDD_NPU



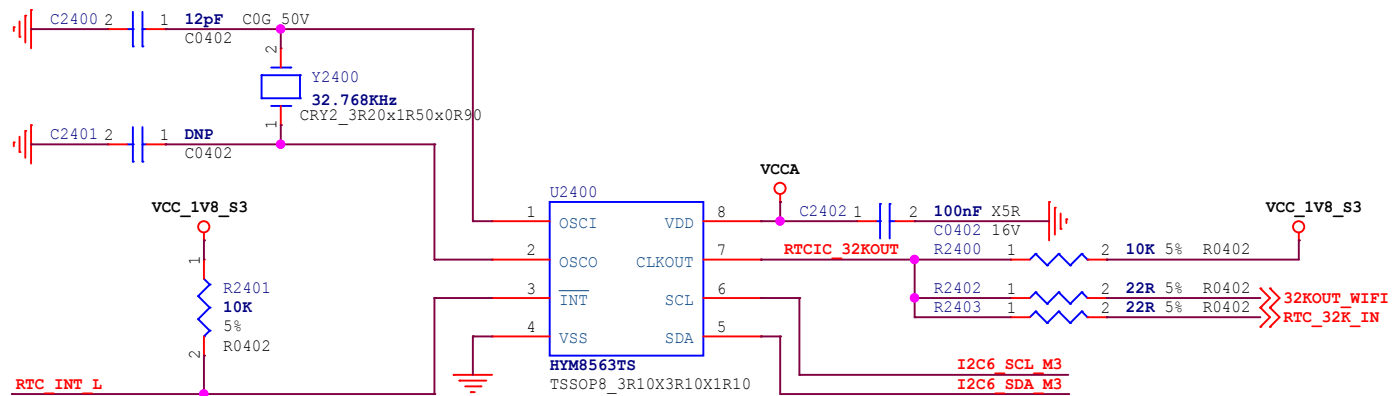
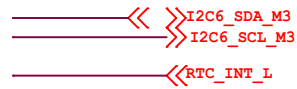
VCC_1V1_NLDO



VCC_3V3_S0



RTC IC



Address:Read A3H,Write A2H

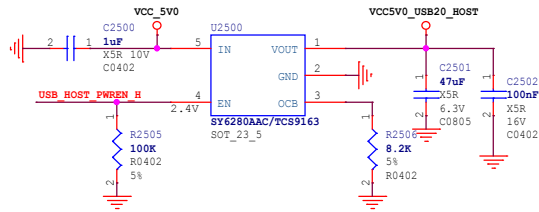
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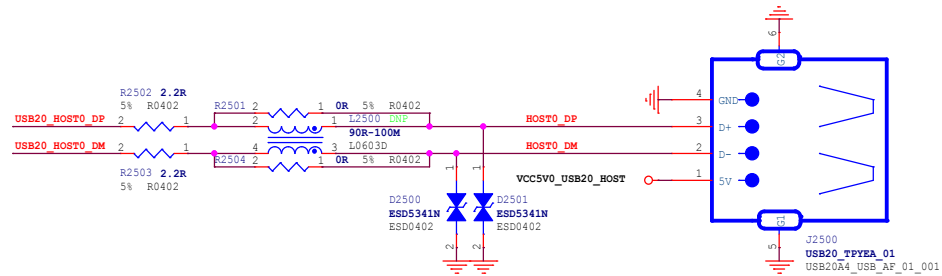
Project:	RK3588S_Tablet_REF		
File:	24.RTC		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	24 of 53

USB_HOST_PWREN_H
 USB20_HOST0_DP
 USB20_HOST0_DM

USB2.0 HOST

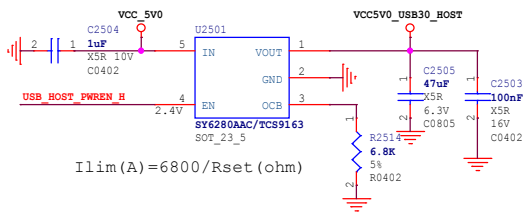


$$I_{lim}(A) = 6800 / R_{set}(\text{ohm})$$

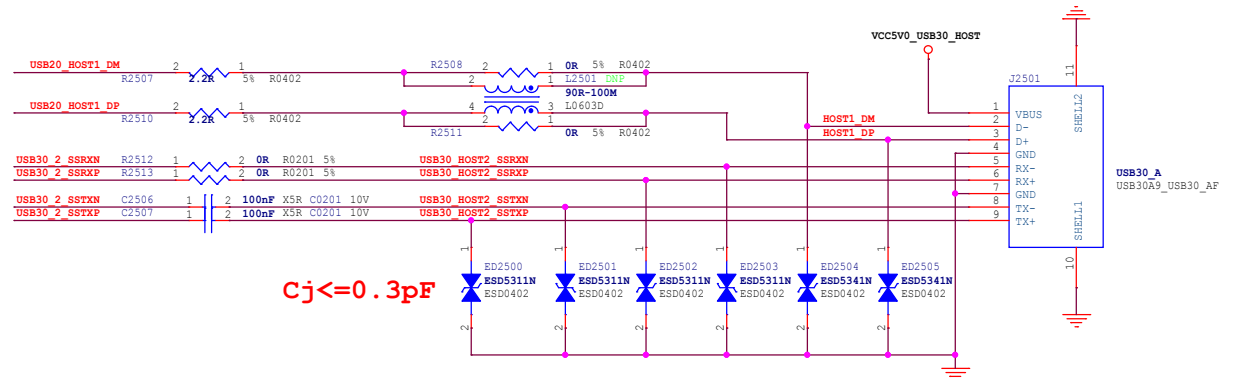


USB20_HOST1_DP
 USB20_HOST1_DM
 USB30_2_SSTXP
 USB30_2_SSTXN
 USB30_2_SSRXP
 USB30_2_SSRXN

USB3.0 HOST



$$I_{lim}(A) = 6800 / R_{set}(\text{ohm})$$



$$C_j \leq 0.3\text{pf}$$

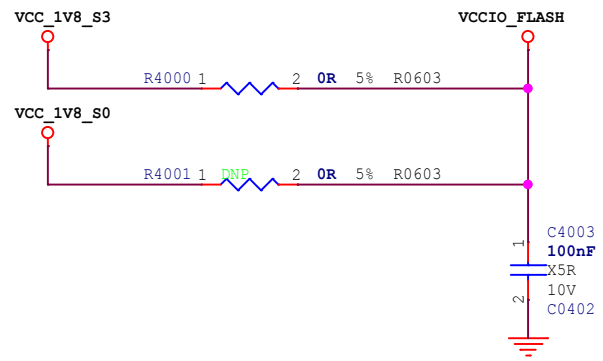
Note:
The C_j of ESD must $\leq 0.3\text{pf}$

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Project:	RK3588S_Tablet_REF		
File:	25.USB20/USB30 HOST Port		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	25	of	53

Flash Power

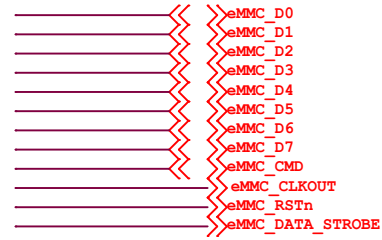
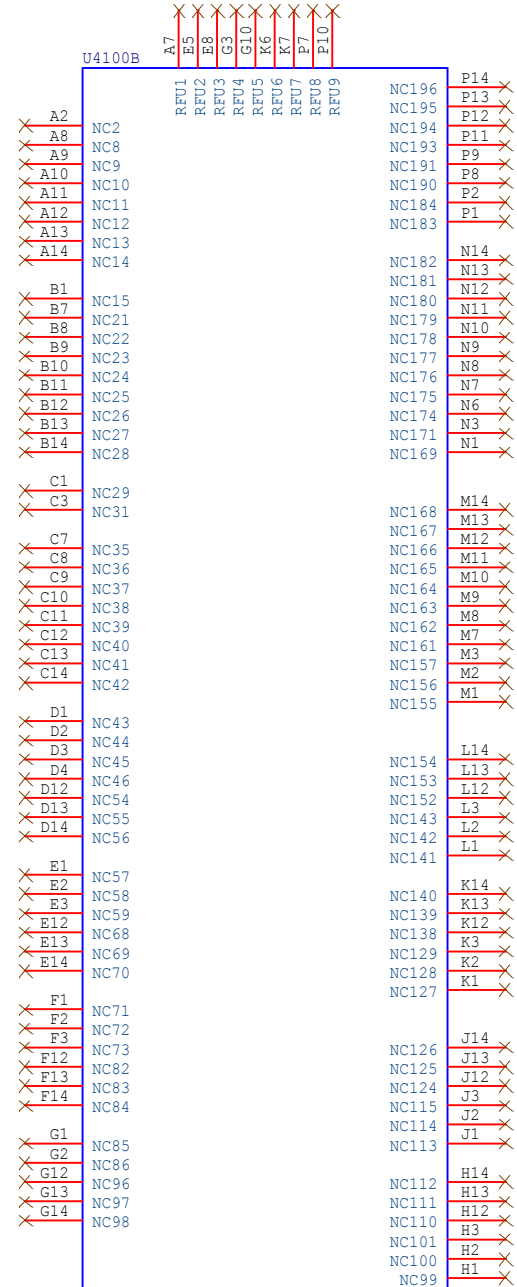


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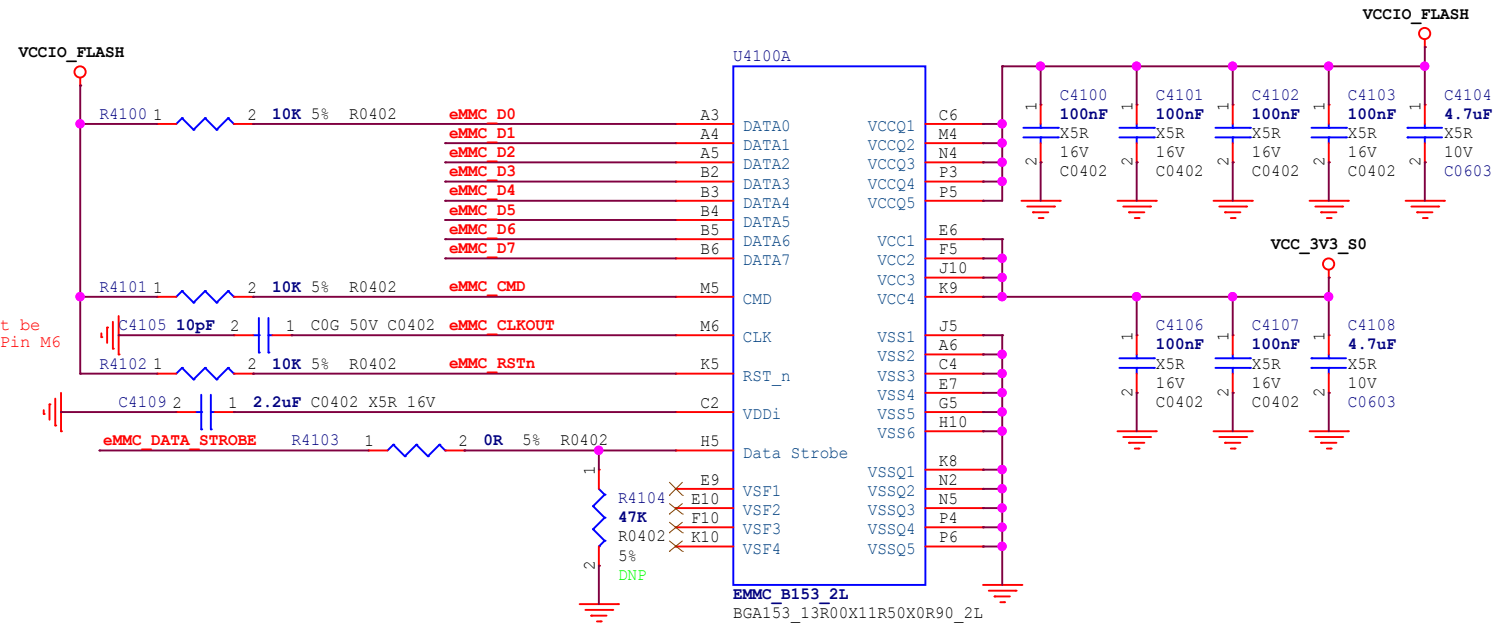
Rockchip Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF		
File:	40.Flash Power		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	28 of 53

eMMC Flash



Note:
C4010 Must be close to Pin M6



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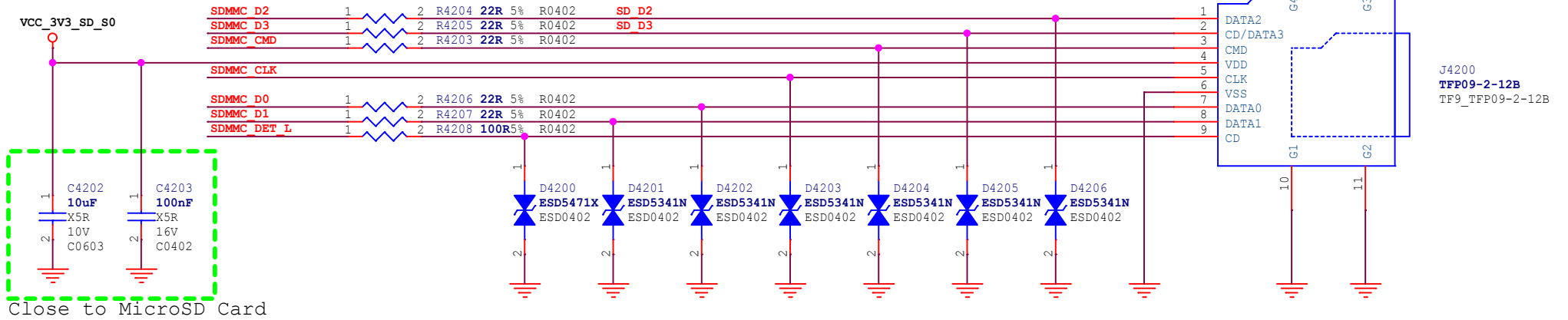
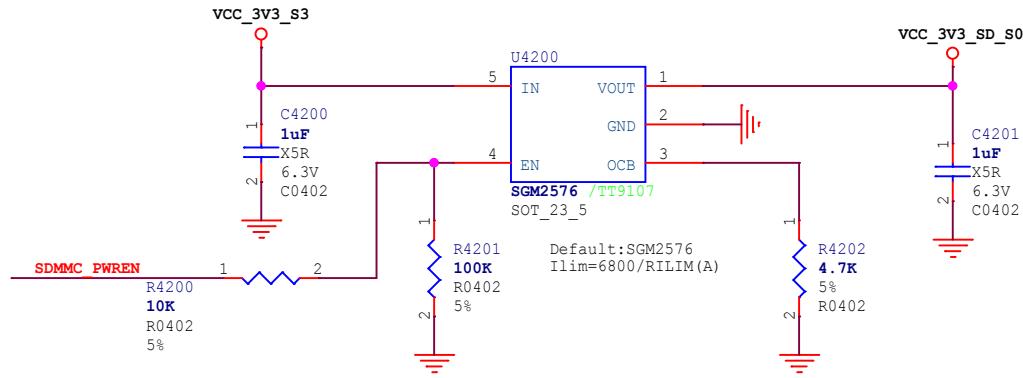
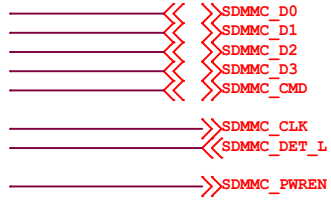
Project: RK3588S_Tablet_REF

File: 41.eMMC Flash

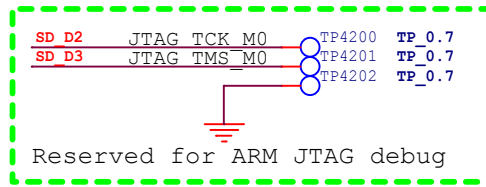
Date: Monday, February 21, 2022 Rev: V10

Designed by: Joseph Reviewed by: <Checker> Sheet: 29 of 53

MicroSD Card



Close to MicroSD Card



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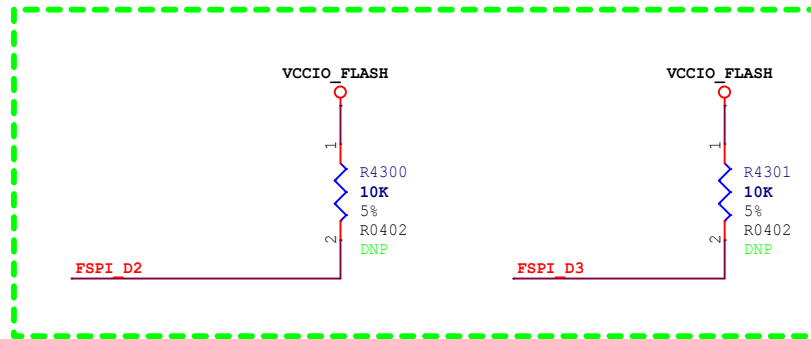
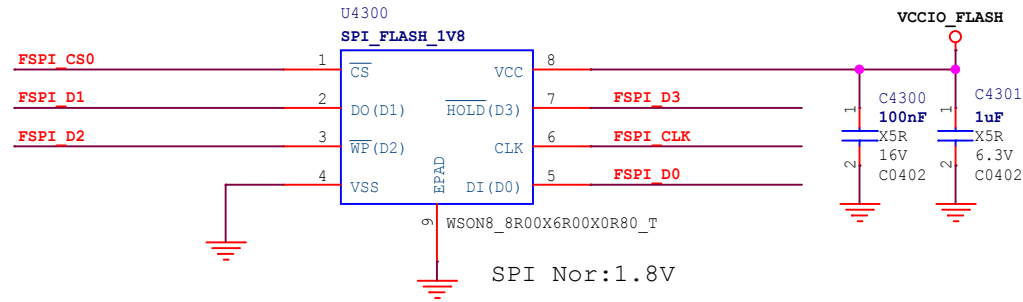
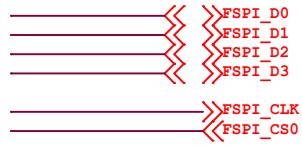
Project: RK3588S_Tablet_REF

File: 42.Flash-Micro-SD Card

Date: Monday, February 21, 2022 Rev: V10

Designed by: Joseph Reviewed by: <Checker> Sheet: 30 of 53

SPI FLASH



Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

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Project: RK3588S_Tablet_REF

File: 43.Flash-SPI FLASH(opt)

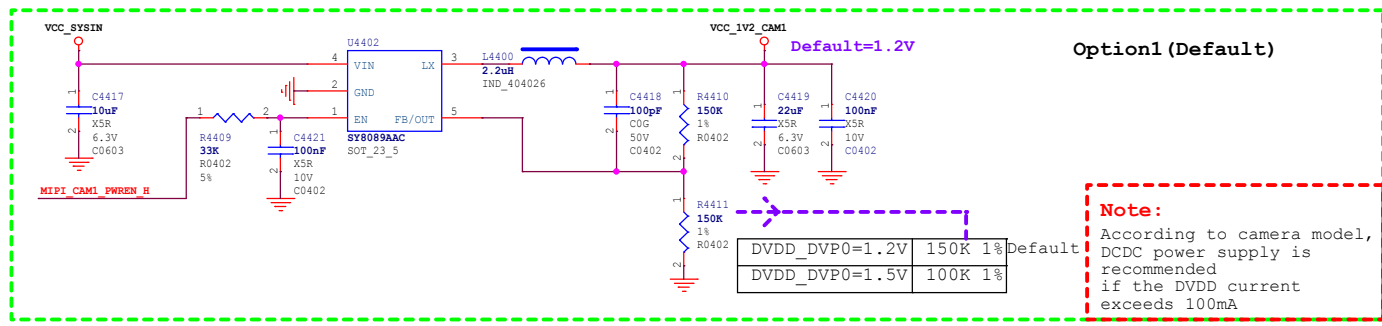
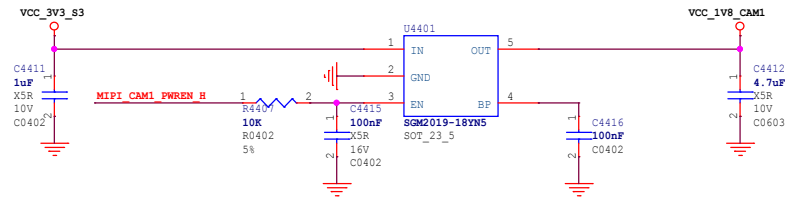
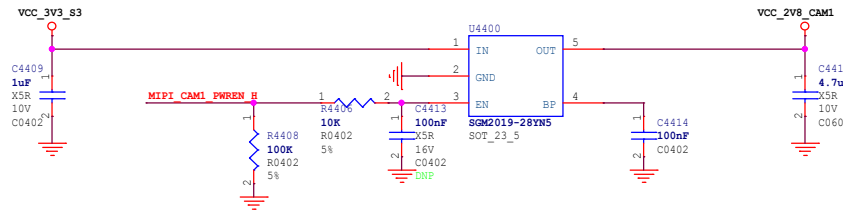
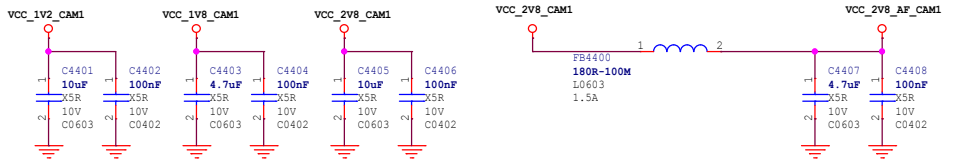
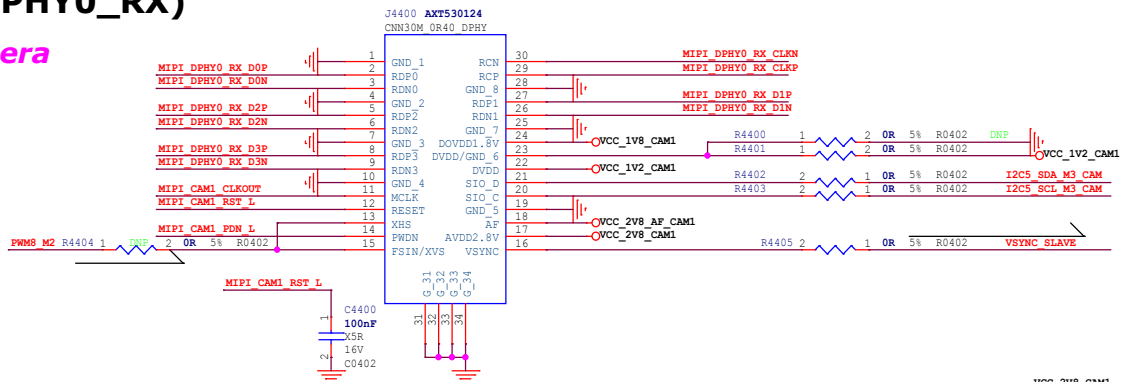
Date: Monday, February 21, 2022 **Rev:** V10

Designed by: Joseph **Reviewed by:** <Checker> **Sheet:** 31 of 53

VI-Camera D/CPHY0_RX(DPHY0_RX)

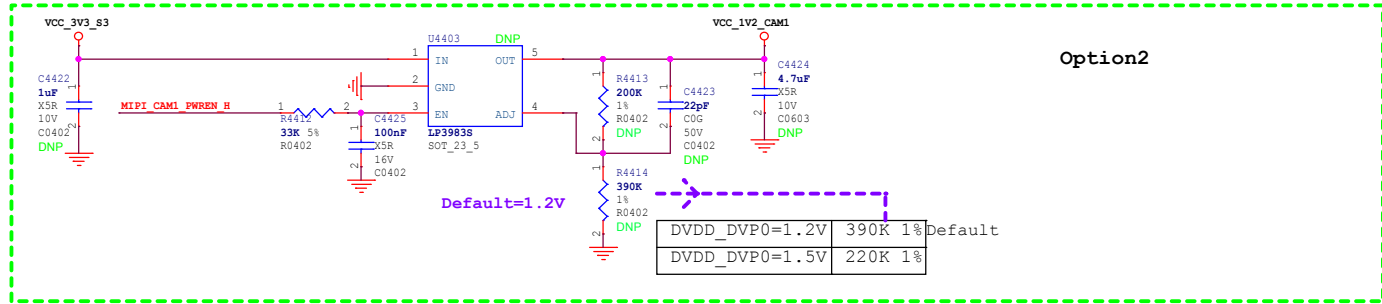
Rear Camera

- >> MIPI_DPHY0_RX_CLKP
- >> MIPI_DPHY0_RX_CLKN
- >> MIPI_DPHY0_RX_D0P
- >> MIPI_DPHY0_RX_D0N
- >> MIPI_DPHY0_RX_D1P
- >> MIPI_DPHY0_RX_D1N
- >> MIPI_DPHY0_RX_D2P
- >> MIPI_DPHY0_RX_D2N
- >> MIPI_DPHY0_RX_D3P
- >> MIPI_DPHY0_RX_D3N
- >> MIPI_CAM1_CLKOUT
- >> I2C5_SCL_M3_CAM
- >> I2C5_SDA_M3_CAM
- >> MIPI_CAM1_PWREN_H
- >> MIPI_CAM1_RST_L
- >> MIPI_CAM1_PDN_L
- >> PMW8_M2
- >> VSYNC_SLAVE



Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V-->MCLK-->PWDN-->RST

Note:
According to camera model,
DCDC power supply is
recommended
if the DVDD current
exceeds 100mA



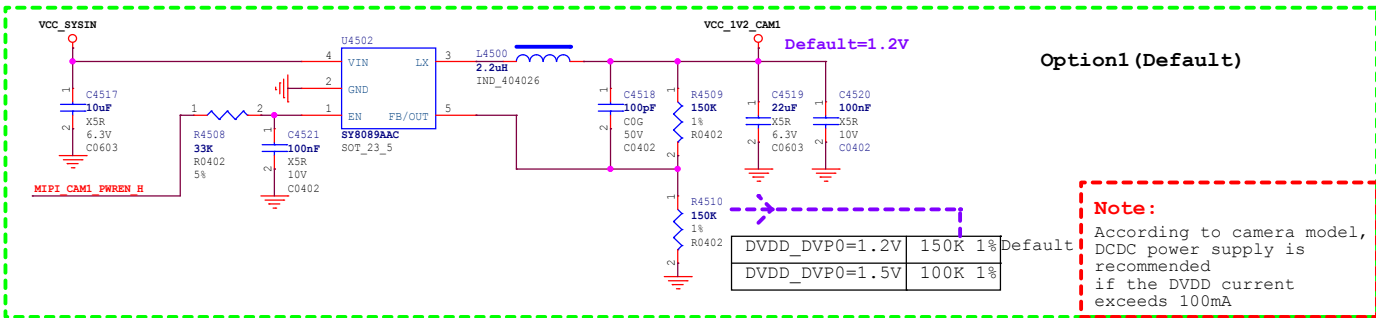
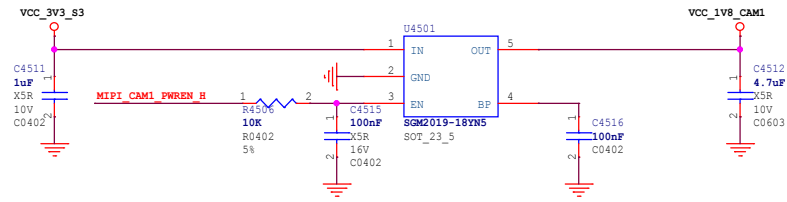
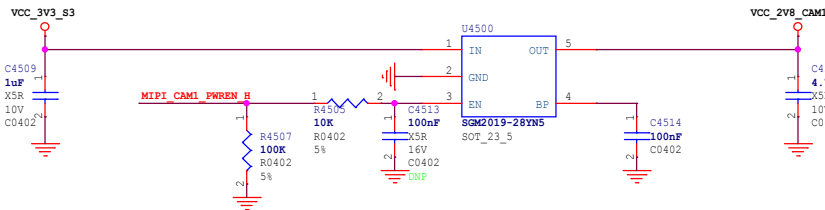
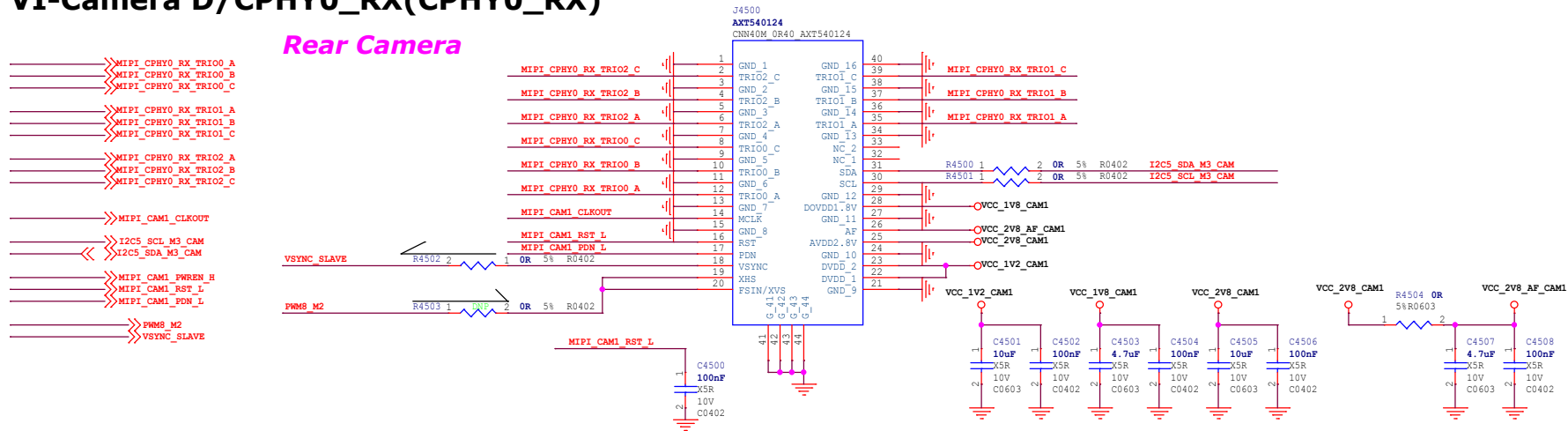
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Project:	RK3588S_Tablet_REF		
File:	44.VI-CAM1 MIPI_D/CPHY0-RX		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	32	of	53

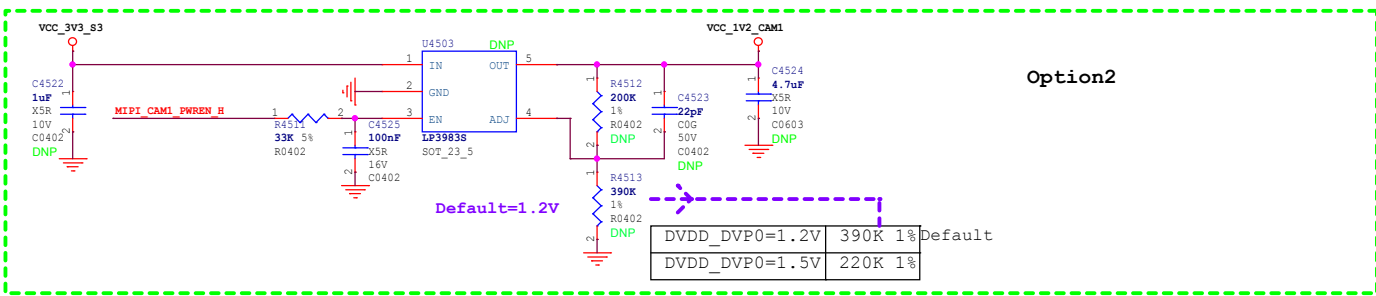
VI-Camera D/CPHY0_RX(CPHY0_RX)

Rear Camera

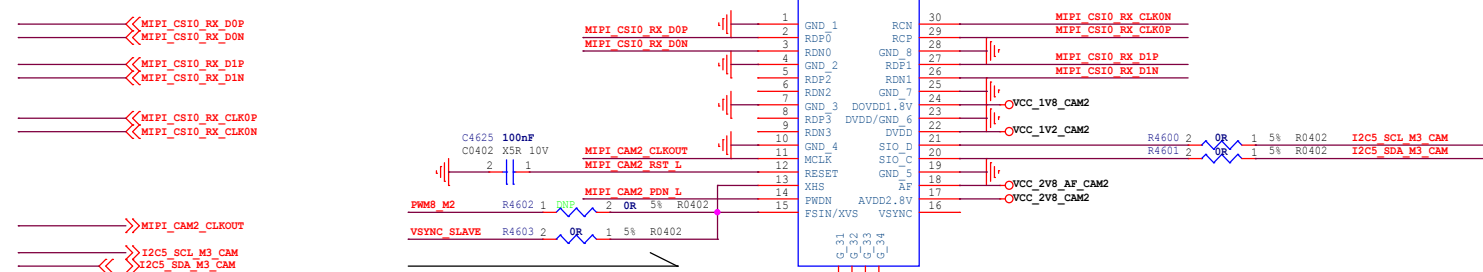


Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V---->MCLK-->PWDN--->RST

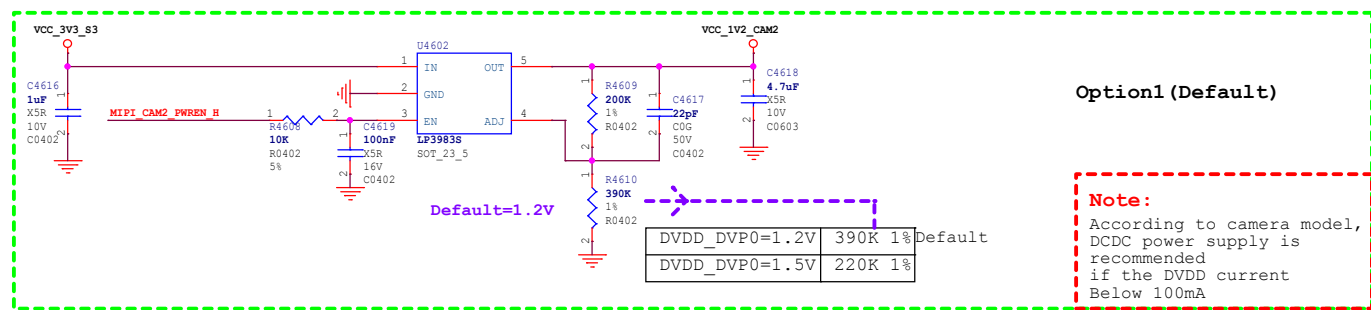
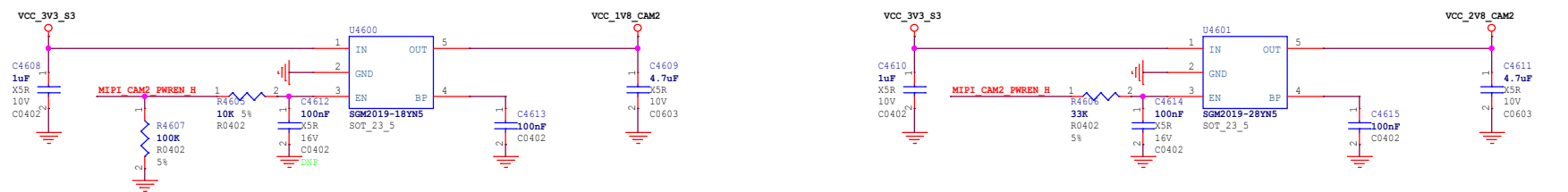
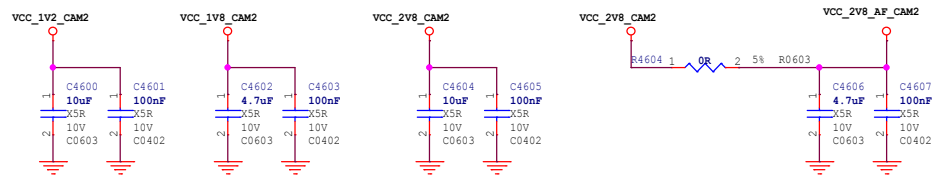
Note:
According to camera model,
DCDC power supply is
recommended
if the DVDD current
exceeds 100mA



MIPI-DPHY0_RX Rear Camera

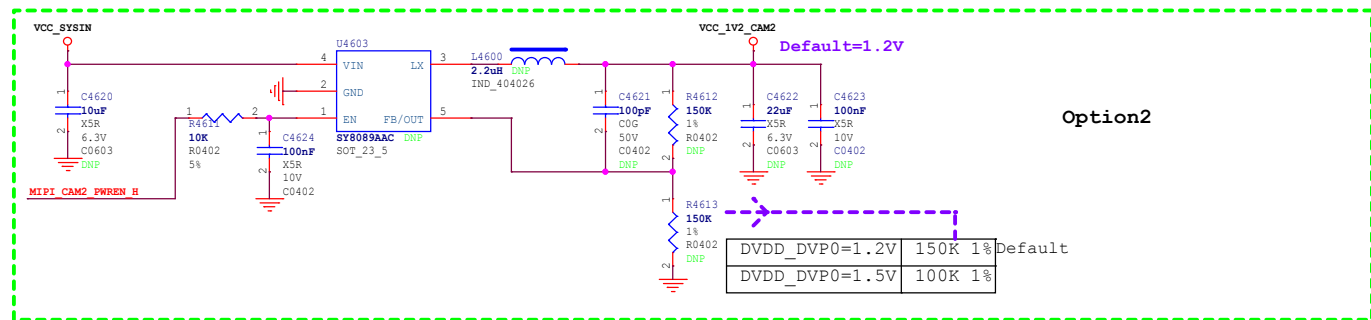


- MIPI_CSIO_RX_DOP
- MIPI_CSIO_RX_DON
- MIPI_CSIO_RX_DIP
- MIPI_CSIO_RX_DIN
- MIPI_CSIO_RX_CLKOP
- MIPI_CSIO_RX_CLKON
- MIPI_CAM2_CLKOUT
- I2C5_SCL_M3_CAM
- I2C5_SDA_M3_CAM
- MIPI_CAM2_PWREN_H
- MIPI_CAM2_RST_L
- MIPI_CAM2_PDN_L
- PMB_M2
- VSYNC_SLAVE



Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V-->MCLK-->PWDN-->RST

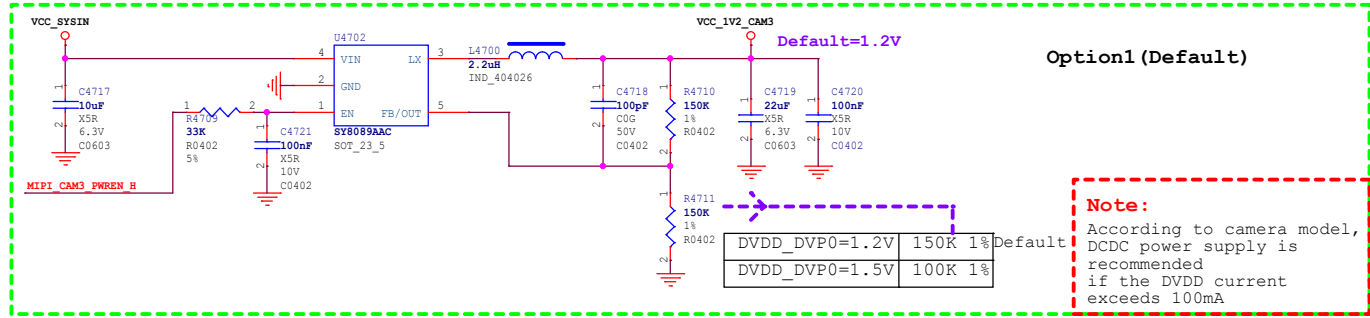
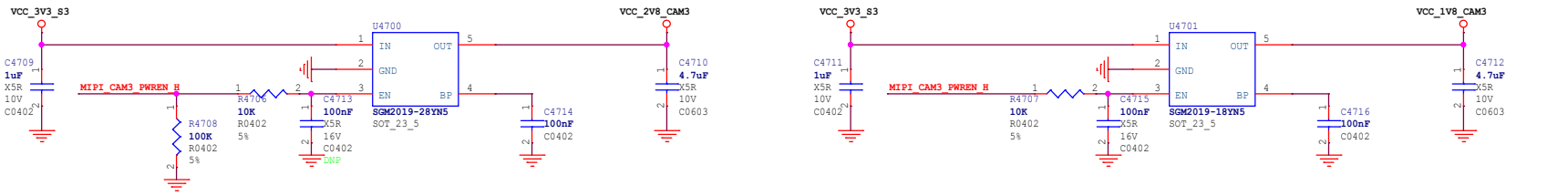
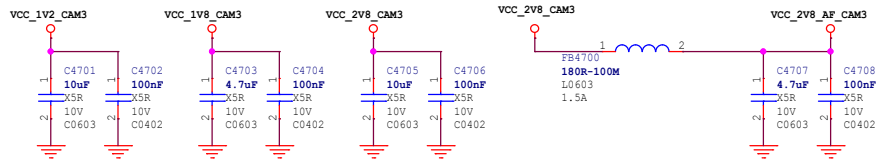
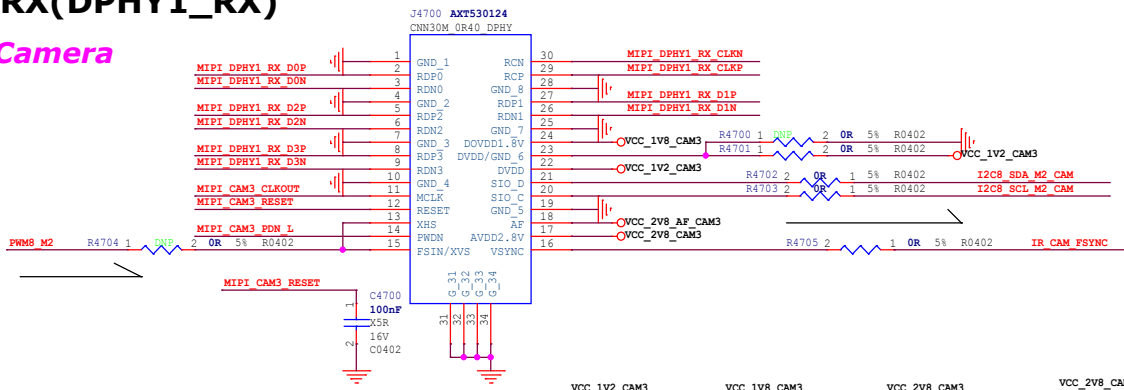
Note:
According to camera model,
DCDC power supply is
recommended
if the DVDD current
Below 100mA



VI-Camera D/CPHY1_RX(DPHY1_RX)

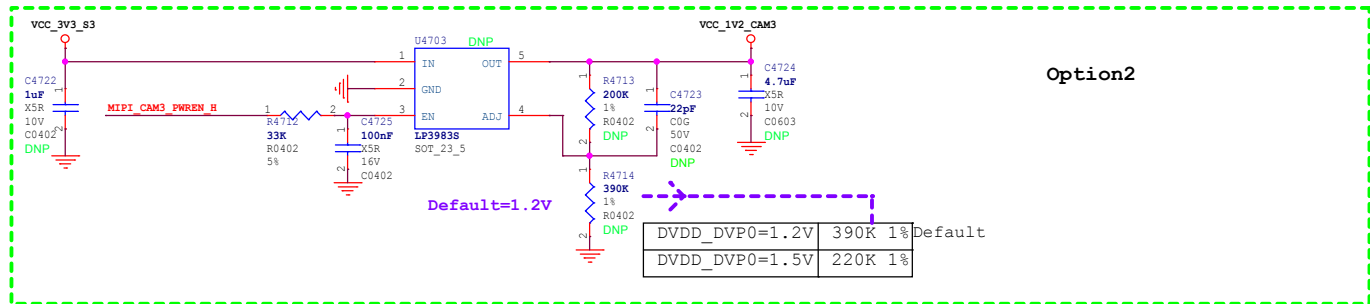
Front Camera

- >> MIPI_DPHY1_RX_CLKP
- >> MIPI_DPHY1_RX_CLKN
- >> MIPI_DPHY1_RX_D0P
- >> MIPI_DPHY1_RX_D0N
- >> MIPI_DPHY1_RX_D1P
- >> MIPI_DPHY1_RX_D1N
- >> MIPI_DPHY1_RX_D2P
- >> MIPI_DPHY1_RX_D2N
- >> MIPI_DPHY1_RX_D3P
- >> MIPI_DPHY1_RX_D3N
- >> MIPI_CAM3_CLKOUT
- >> I2C8_SCL_M2_CAM
- >> I2C8_SDA_M2_CAM
- >> MIPI_CAM3_PWREN_H
- >> MIPI_CAM3_RST_L
- >> MIPI_CAM3_PDN_L
- >> PWM8_M2
- >> IR_CAM_FSYNC



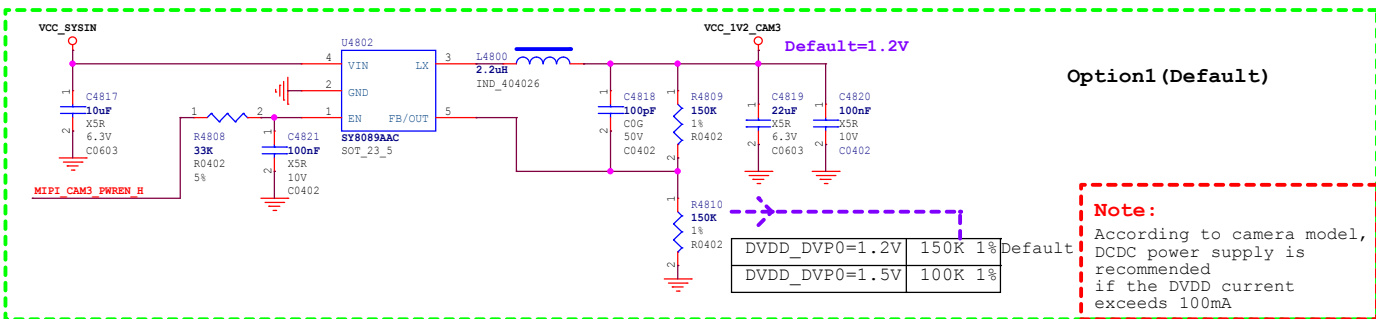
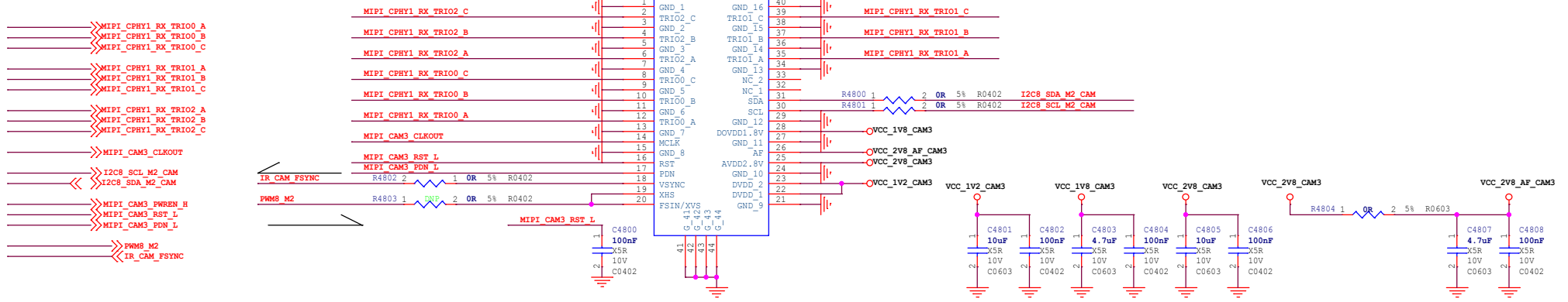
Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

Note:
According to camera model,
DCDC power supply is
recommended
if the DVDD current
exceeds 100mA



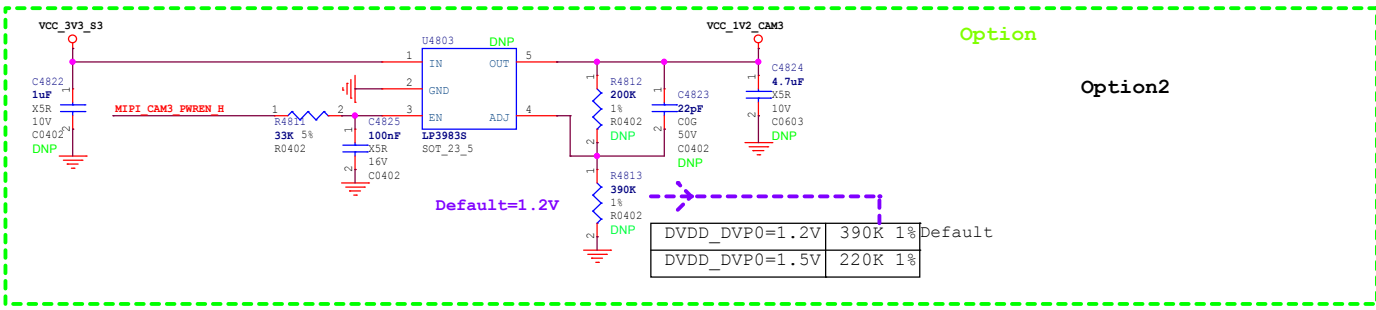
VI-Camera D/CPHY1_RX(CPHY1_RX)

Front Camera

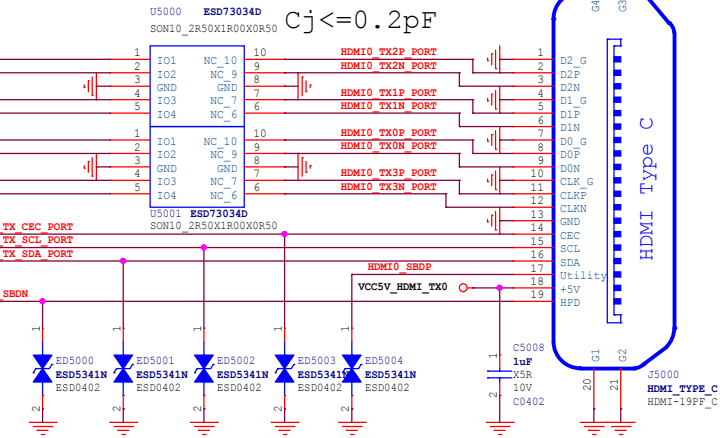
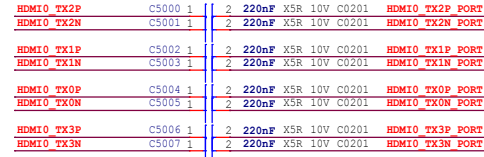
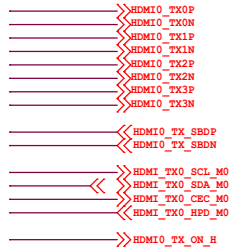


Note:
Adjust the power on sequence according to the camera model
eg:OV50C40
Power on Sequence
2.8V-->1.8V-->1.2V-->MCLK-->PWDN-->RST

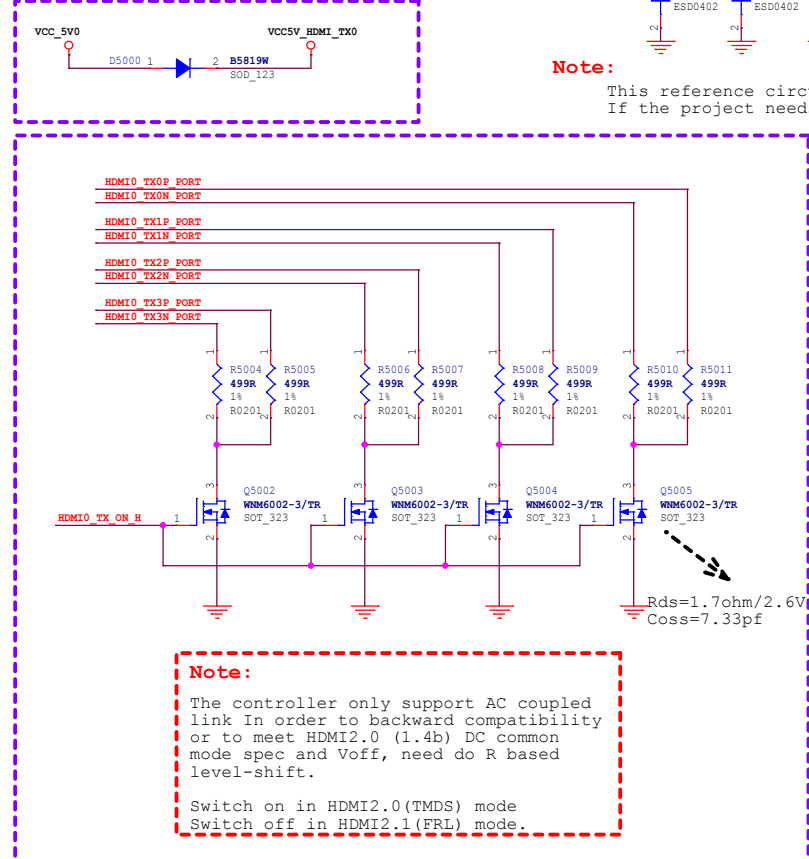
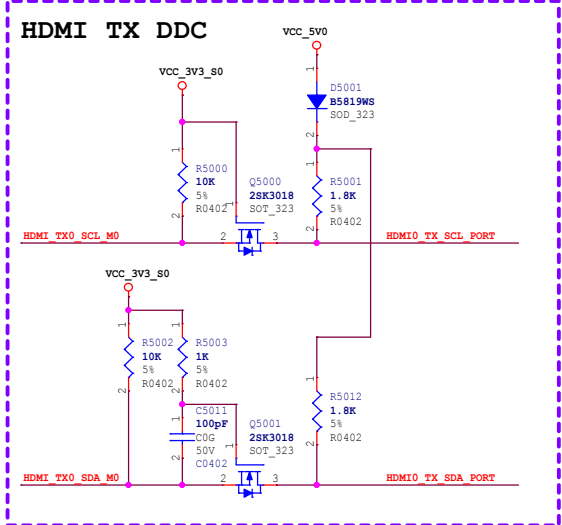
Note:
According to camera model,
DCDC power supply is
recommended
if the DVDD current
exceeds 100mA



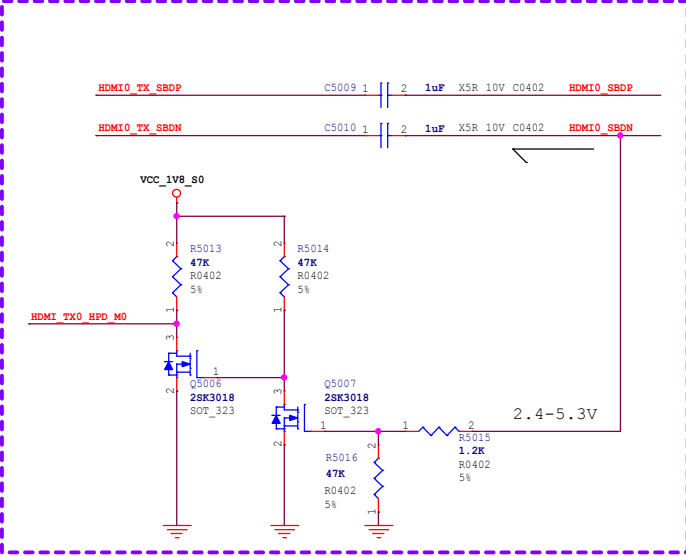
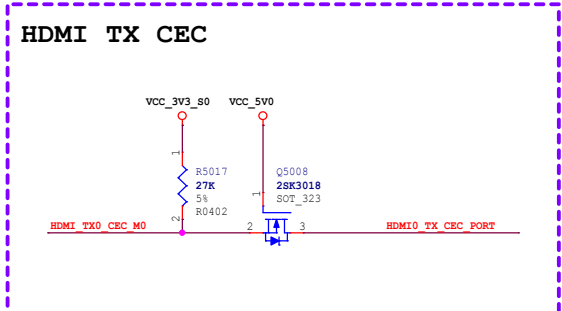
HDMI2.1 TX0



Note:
This reference circuit use TYPE C by default
If the project needs TYPE A, you must replace the library with TYPE A.

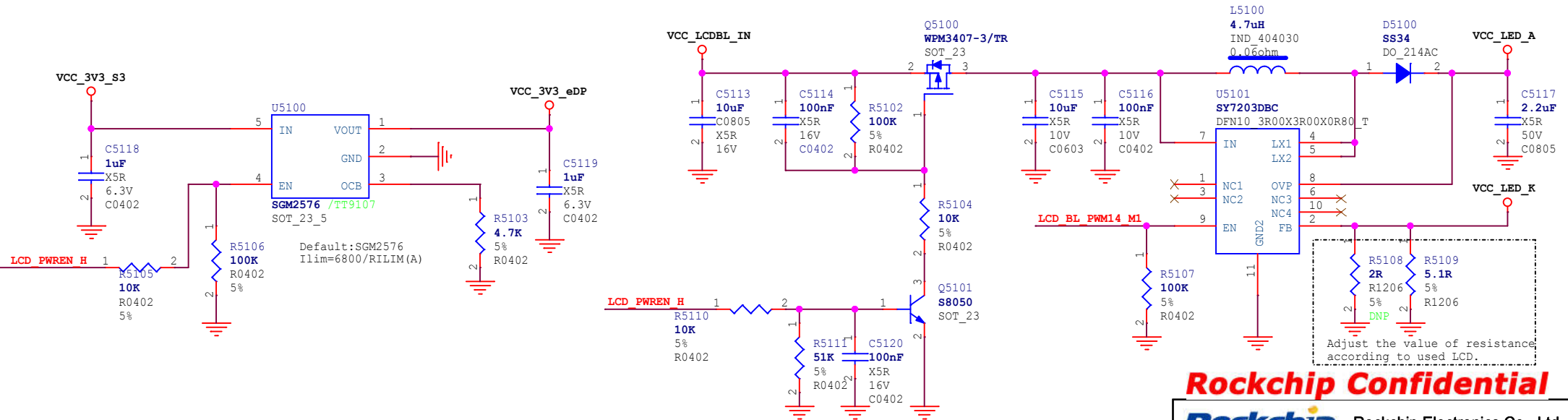
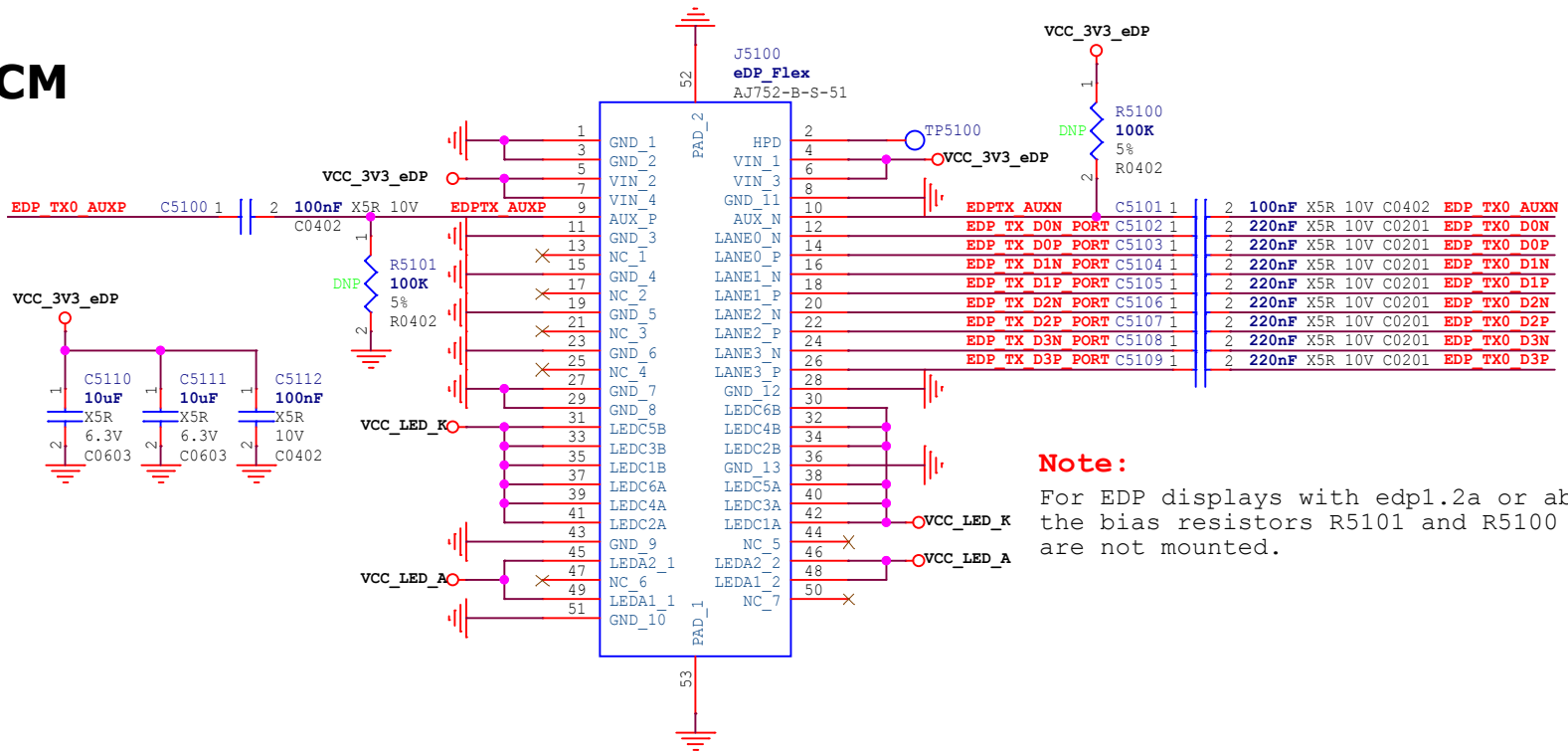


Note:
The controller only support AC coupled link in order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.
Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.



Single-eDP LCM

- >>>EDP_TX0_D0P
- >>>EDP_TX0_D0N
- >>>EDP_TX0_D1P
- >>>EDP_TX0_D1N
- >>>EDP_TX0_D2P
- >>>EDP_TX0_D2N
- >>>EDP_TX0_D3P
- >>>EDP_TX0_D3N
- >>>EDP_TX0_AUXP
- >>>EDP_TX0_AUXN
- >>>LCD_BL_PWM14_M1
- >>>LCD_PWREN_H

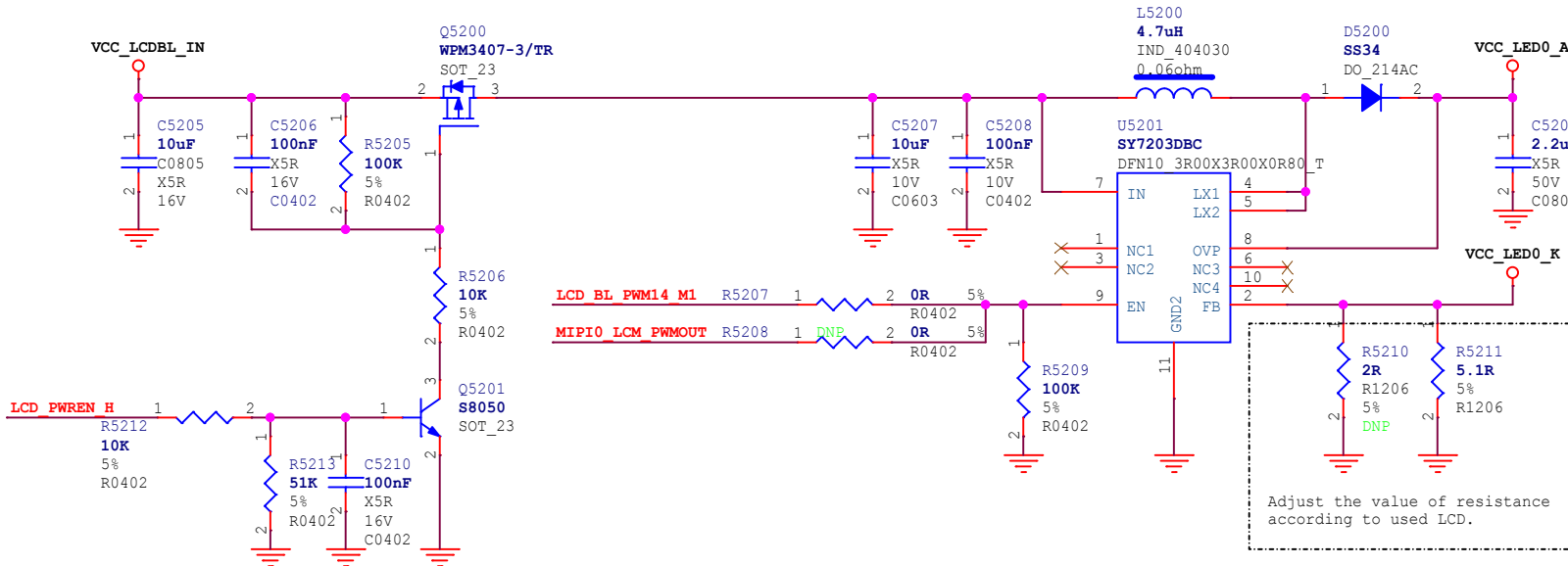
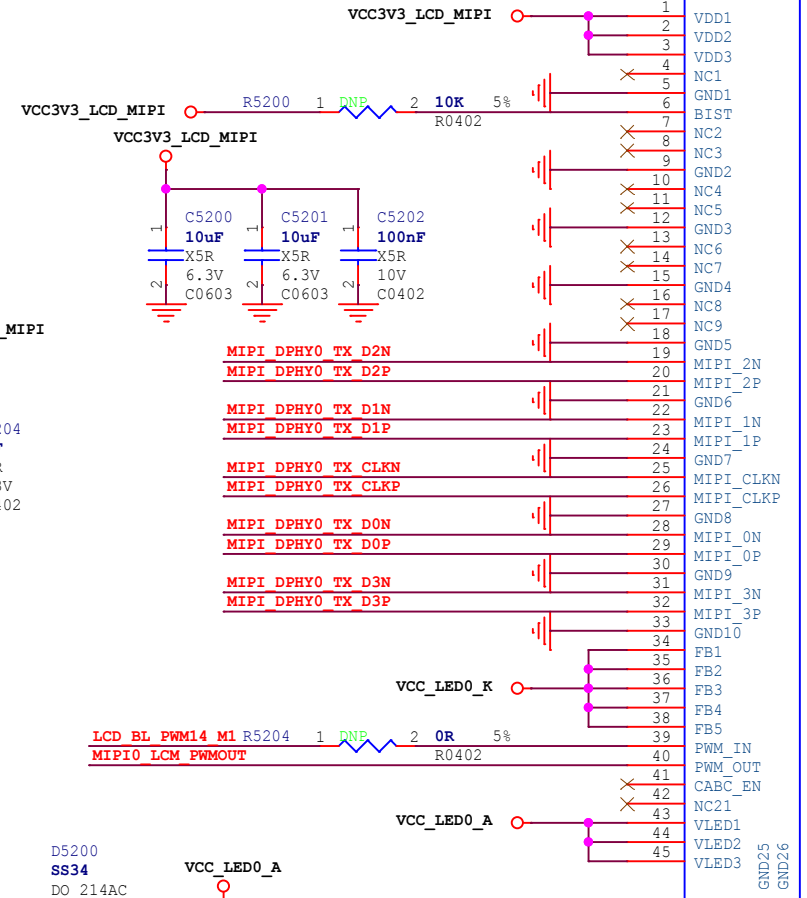
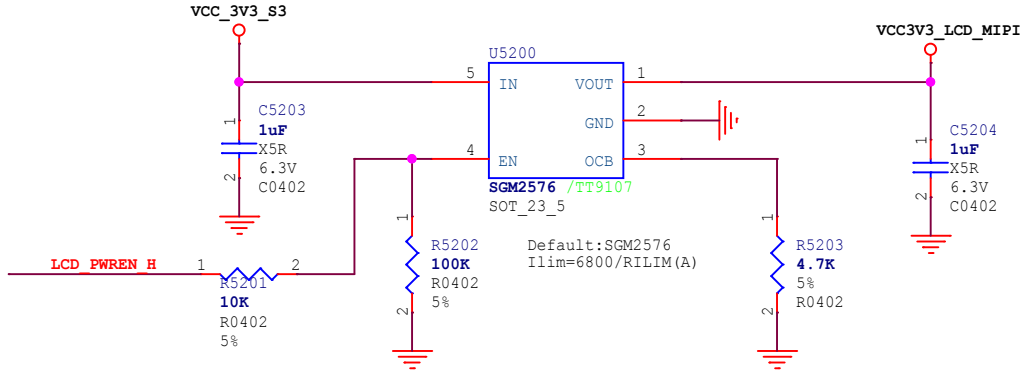


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Project:	RK3588S_Tablet_REF		
File:	51.VO-LCM_eDP1.3 TX		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	Default
		Sheet:	39 of 53

Single-MIPI LCM(MIPI DPHY0 TX)

- >>MIPI_DPHY0_TX_CLKP
- >>MIPI_DPHY0_TX_CLKN
- >>MIPI_DPHY0_TX_D0P
- >>MIPI_DPHY0_TX_D0N
- >>MIPI_DPHY0_TX_D1P
- >>MIPI_DPHY0_TX_D1N
- >>MIPI_DPHY0_TX_D2P
- >>MIPI_DPHY0_TX_D2N
- >>MIPI_DPHY0_TX_D3P
- >>MIPI_DPHY0_TX_D3N
- >>LCD_BL_PWM14_M1
- >>LCD_PWREN_H



Adjust the value of resistance according to used LCD.

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Project: RK3588S_Tablet_REF

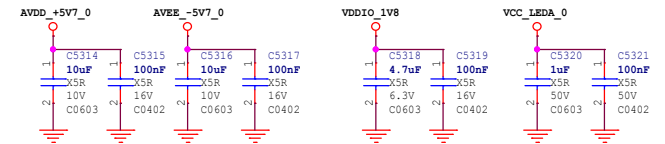
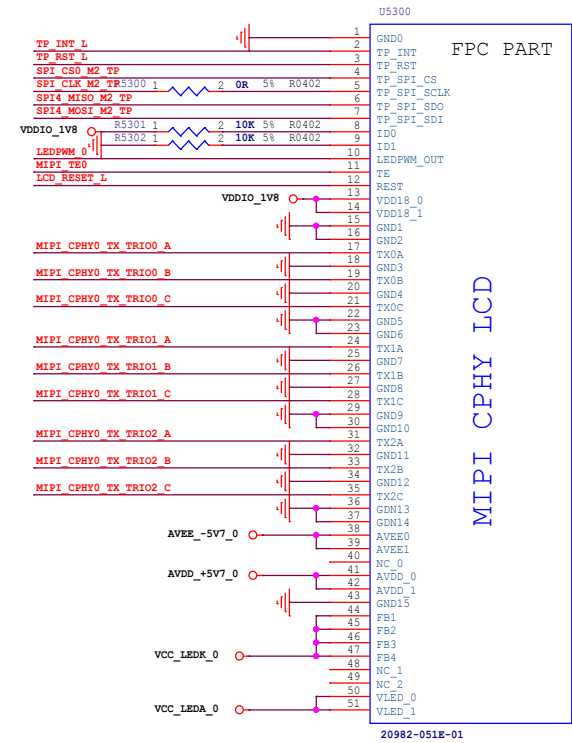
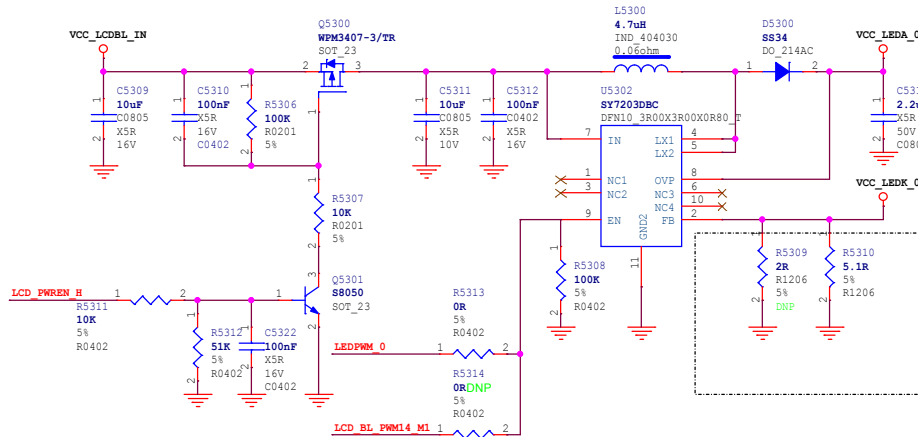
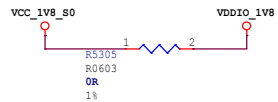
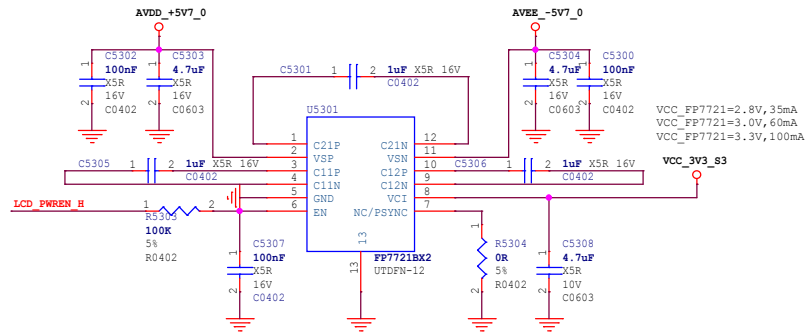
File: 52.VO-LCM_MIPI_D/CPHY0_TX

Date: Monday, February 21, 2022 Rev: V10

Designed by: Joseph Reviewed by: Default Sheet: 40 of 53

Single-MIPI LCM(MIPI CPHY0 TX)

- >>> MIPI_CPHY0_TX_TRIO0_A
- >>> MIPI_CPHY0_TX_TRIO0_B
- >>> MIPI_CPHY0_TX_TRIO0_C
- >>> MIPI_CPHY0_TX_TRIO1_A
- >>> MIPI_CPHY0_TX_TRIO1_B
- >>> MIPI_CPHY0_TX_TRIO1_C
- >>> MIPI_CPHY0_TX_TRIO2_A
- >>> MIPI_CPHY0_TX_TRIO2_B
- >>> MIPI_CPHY0_TX_TRIO2_C
- >>> SPI4_MISO_M2_TP
- >>> SPI4_MOSI_M2_TP
- >>> SPI_CLK_M2_TP
- >>> SPI_CS0_M2_TP
- >>> TP_RST_L
- >>> TP_INT_L
- >>> MIPI_TEO
- >>> LCD_BL_PWM14_M1
- >>> LCD_PWREN_H
- >>> LCD_RESET_L

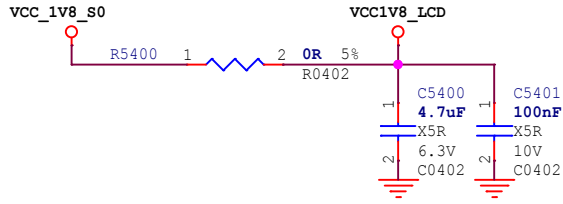


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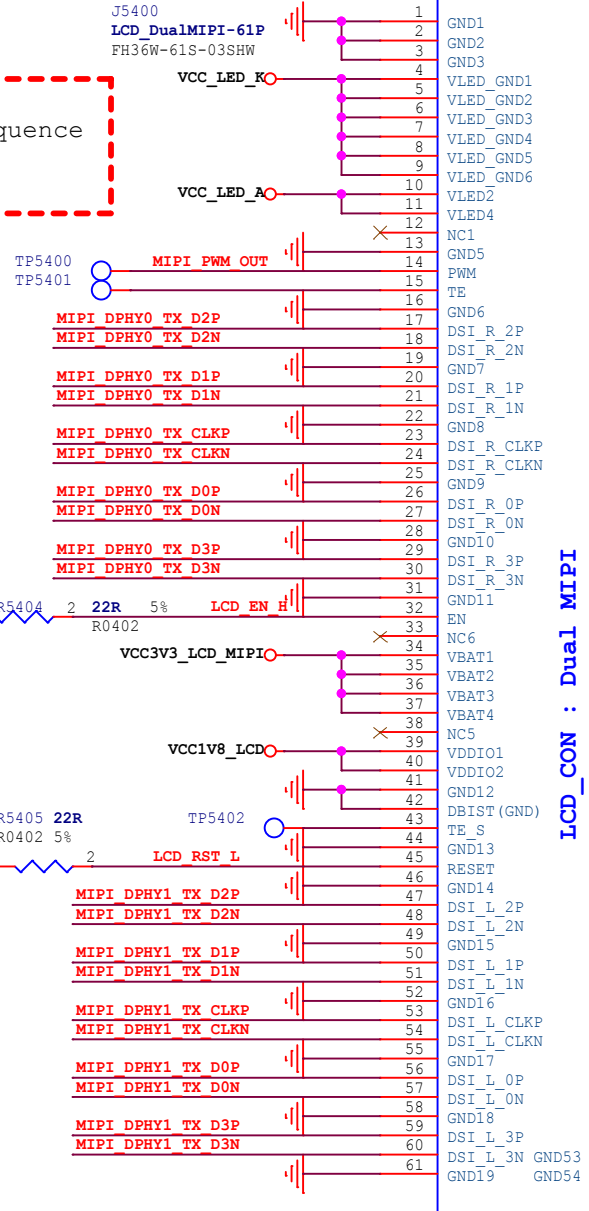
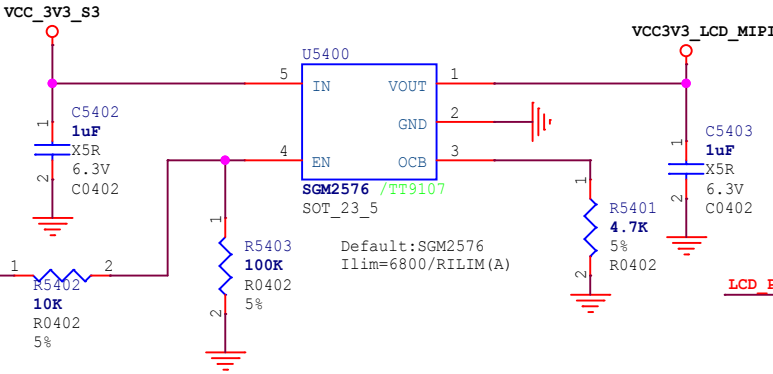
Project:	RK3588S_Tablet_REF		
File:	S3.VO-LCM_MIPI_D/CPHY0_TX(opt)		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	Default
Sheet:	41	of	53

Dual-MIPI LCM(MIPI DPHY0+DPHY1 TX)

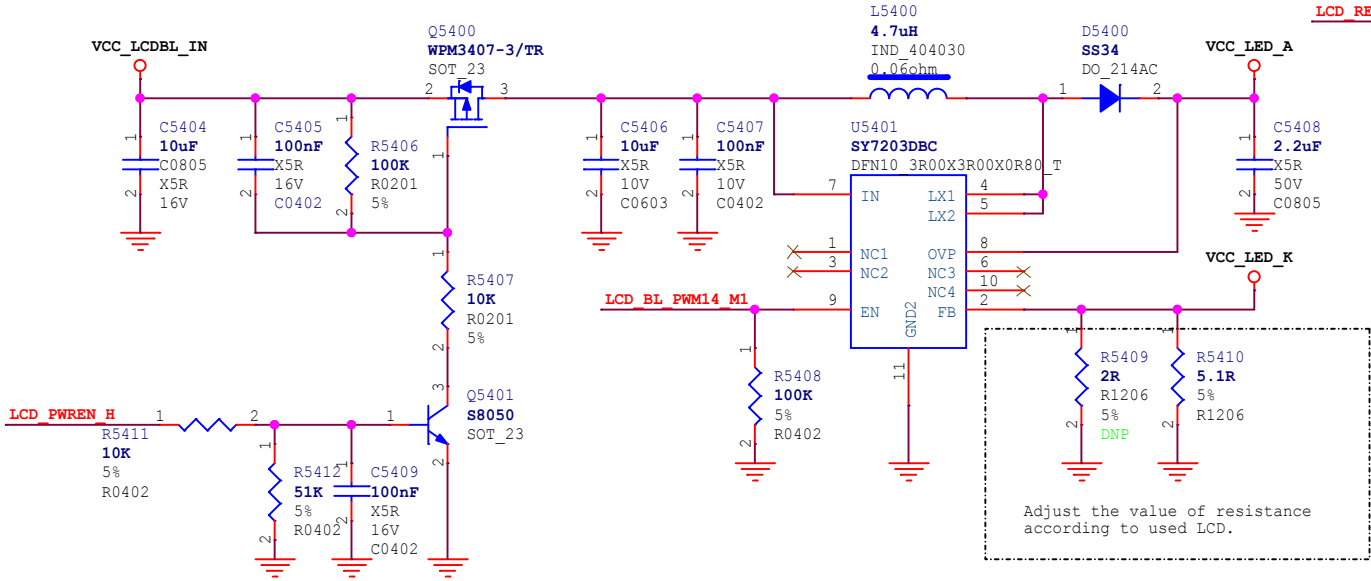
- >>MIPI_DPHY0_TX_CLKP
- >>MIPI_DPHY0_TX_CLKN
- >>MIPI_DPHY0_TX_D0P
- >>MIPI_DPHY0_TX_D0N
- >>MIPI_DPHY0_TX_D1P
- >>MIPI_DPHY0_TX_D1N
- >>MIPI_DPHY0_TX_D2P
- >>MIPI_DPHY0_TX_D2N
- >>MIPI_DPHY1_TX_CLKP
- >>MIPI_DPHY1_TX_CLKN
- >>MIPI_DPHY1_TX_D0P
- >>MIPI_DPHY1_TX_D0N
- >>MIPI_DPHY1_TX_D1P
- >>MIPI_DPHY1_TX_D1N
- >>MIPI_DPHY1_TX_D2P
- >>MIPI_DPHY1_TX_D2N
- >>MIPI_DPHY1_TX_D3P
- >>MIPI_DPHY1_TX_D3N
- >>LCD_BL_PWM14_M1
- >>LCD_PWREN_H
- >>LCD_RESET_L



Note:
Power on Sequence
1.8V-->3.3V



LCD_CON : Dual MIPI



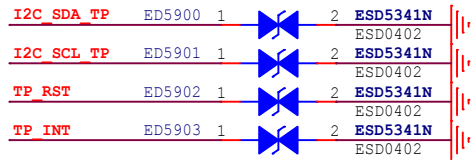
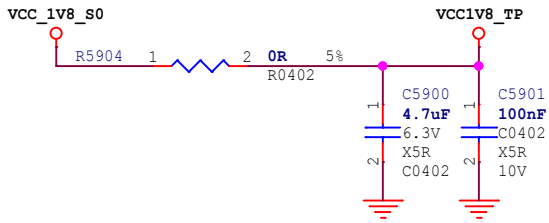
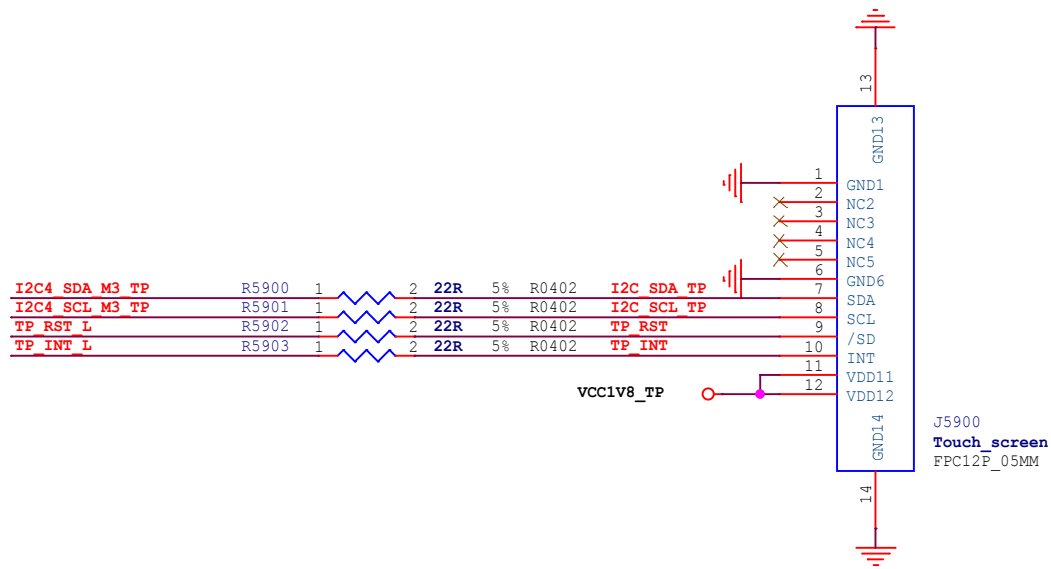
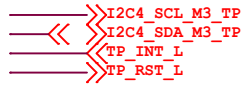
Adjust the value of resistance according to used LCD.

Left and Right support redistribution



Project:	RK3588S_Tablet_REF		
File:	54.VO-LCM_Dual MIPI_D/CPHY TX		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	Default
Sheet:	42 of 53		

Touch Panel connector



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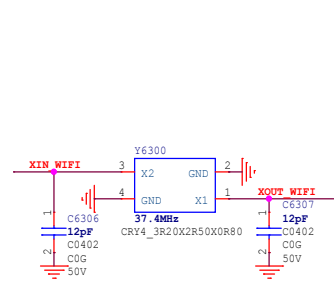
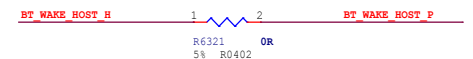
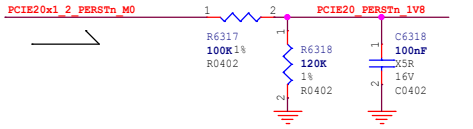
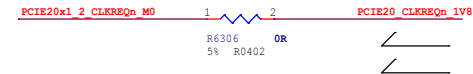
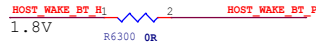
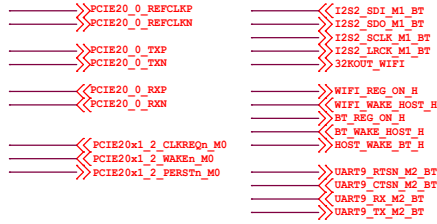
Project: RK3588S_Tablet_REF

File: 59.TP Connector_COF(I2C)

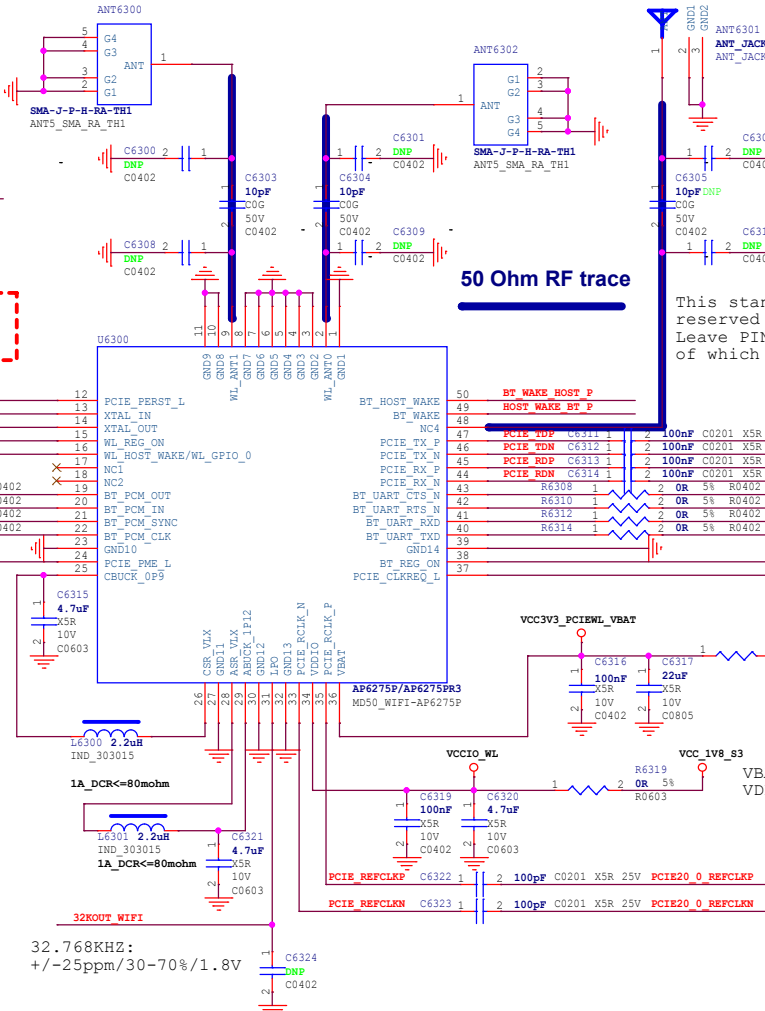
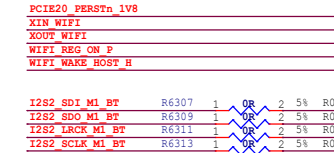
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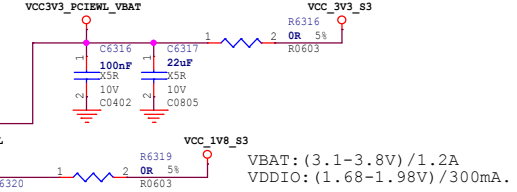
PCIe WIFI6/BT Module-2T2R



NOTE:
Adjust the load capacitor according to the crystal spec.

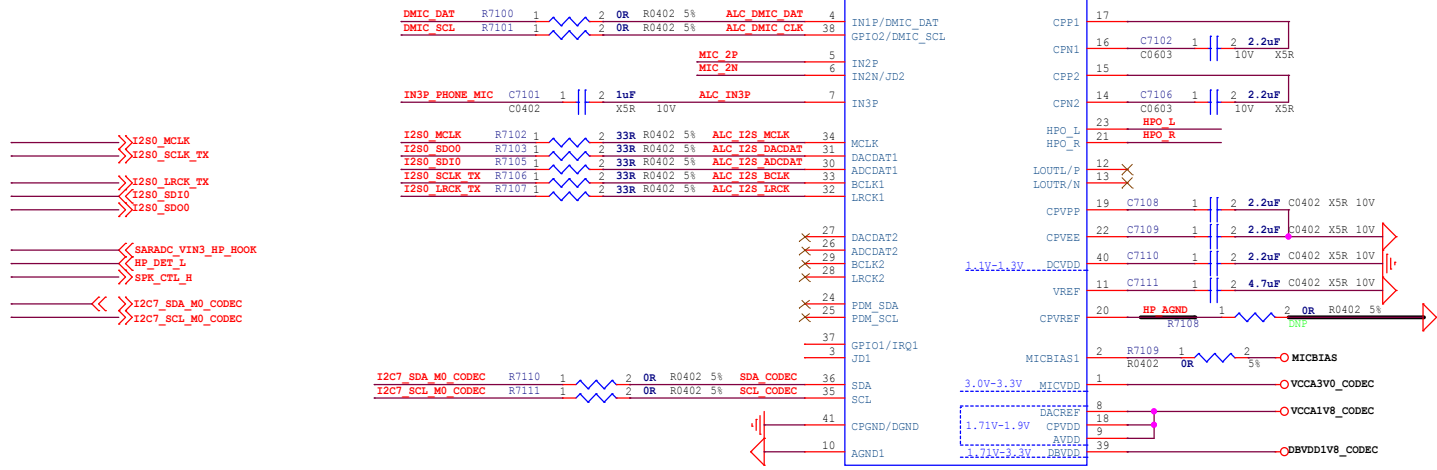


This standalone BT-ANT is reserved for AP6275PR3. Leave PIN48 float for AP6275P, of which BT-ANT is mux with WIFI.

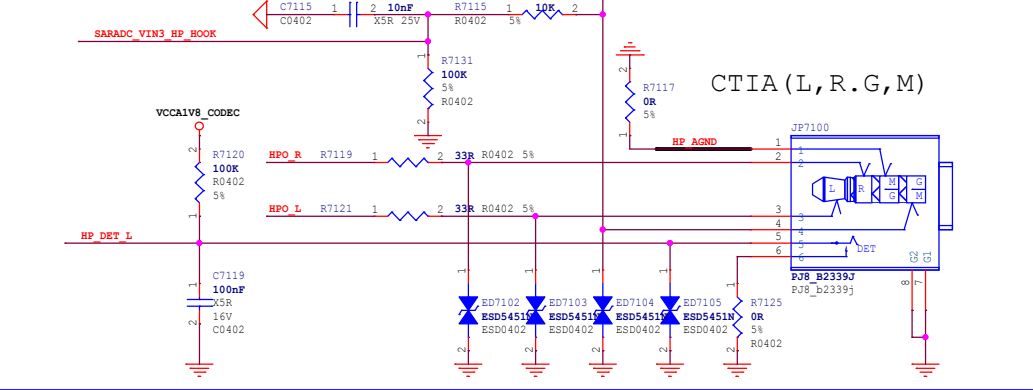


VBAT: (3.1-3.8V)/1.2A
VDDIO: (1.68-1.98V)/300mA.

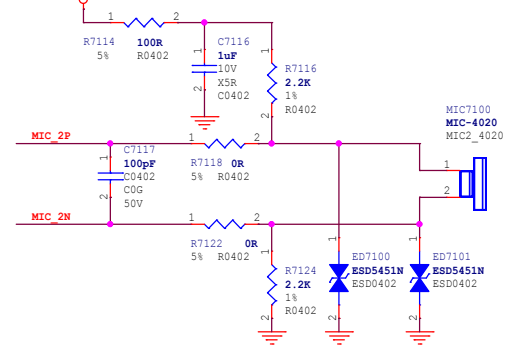
CODEC ALC5651



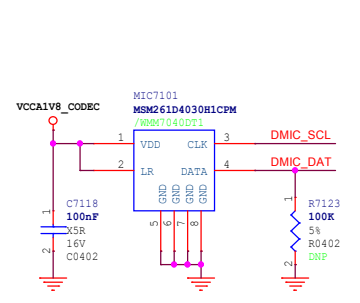
EARPHONE



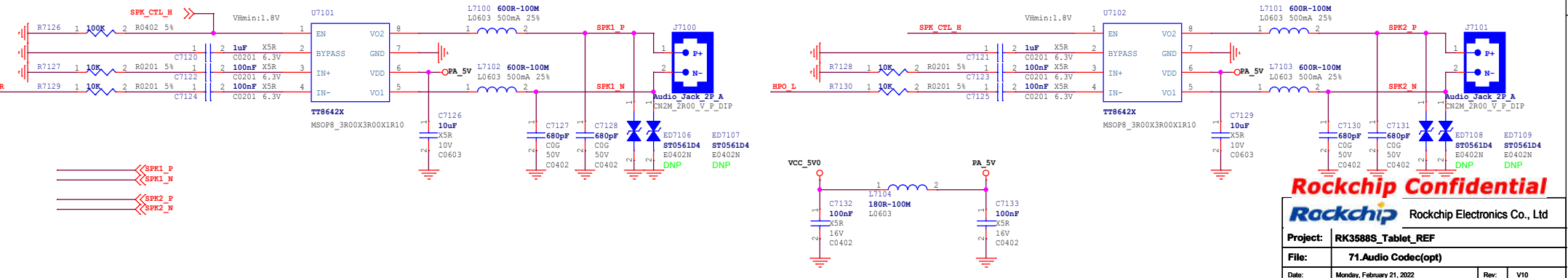
Analog MIC



DIGITAL MIC



SPEAKER



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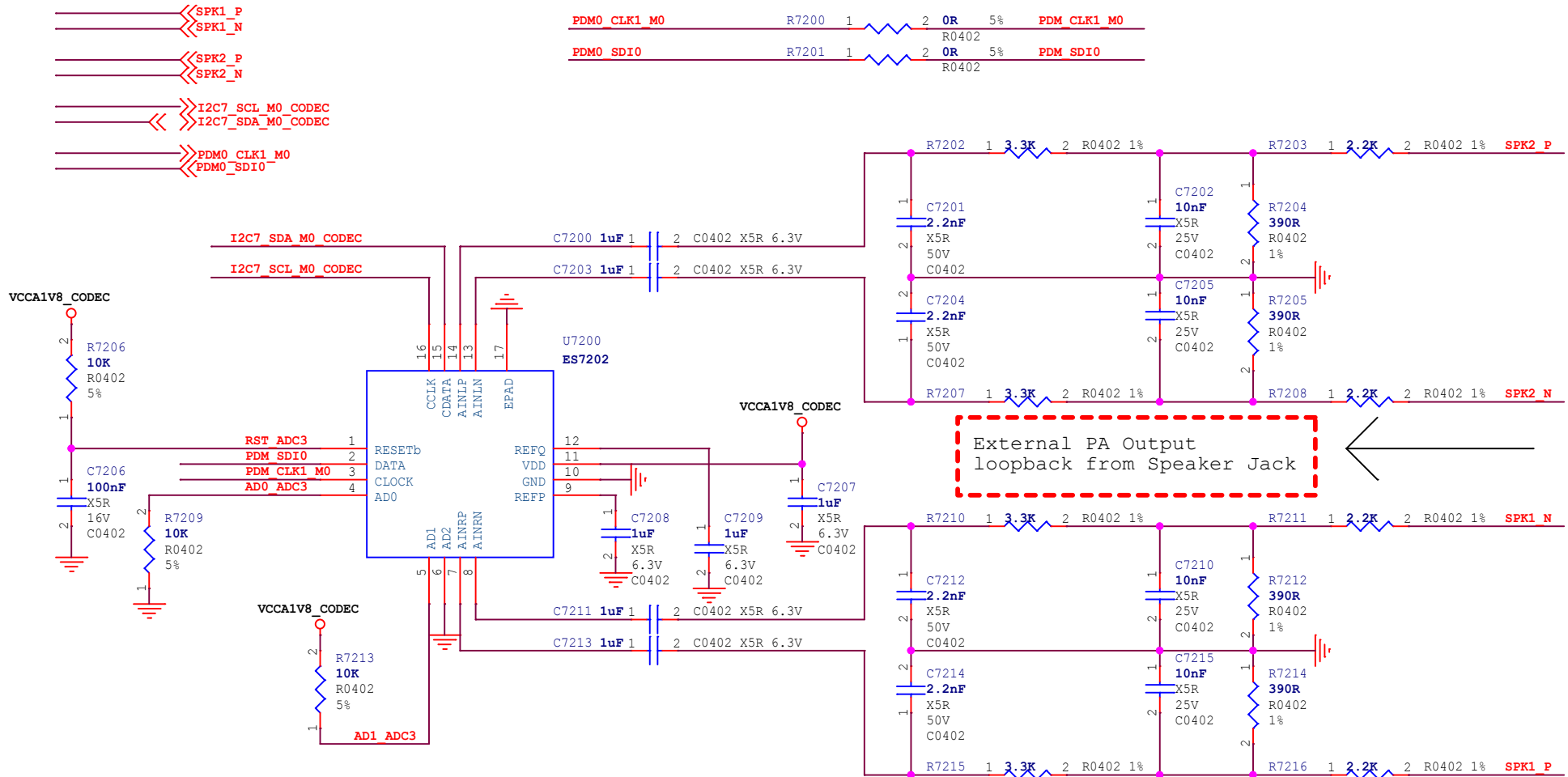
Project: RK3588S_Tablet_REF

File: 71.Audio Codec(opt)

Date: Monday, February 21, 2022 **Rev:** V10

Designed by: Joseph **Reviewed by:** Default **Sheet:** 47 of 53

Loopback



External PA Output
loopback from Speaker Jack

AD[2:0] 0 0 0 = 0x30 7bit
 AD[2:0] 0 0 1 = 0x31 7bit
 AD[2:0] 0 1 0 = 0x32 7bit (default)

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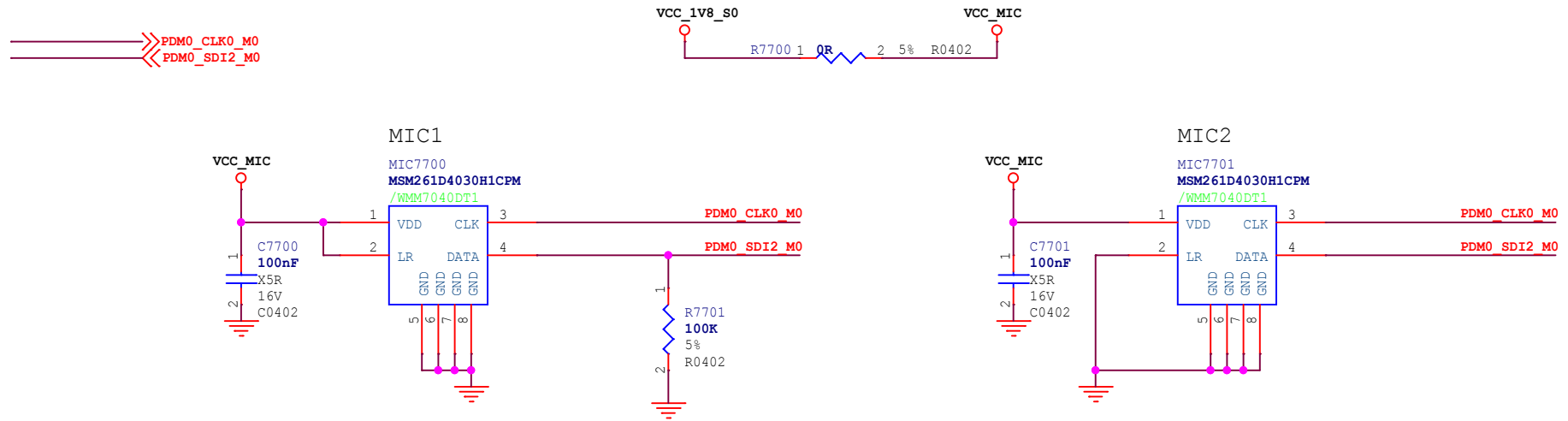
Project: RK3588S_Tablet_REF

File: 72.Audio-Loopback

Date: Monday, February 21, 2022 **Rev:** V10

Designed by: Joseph **Reviewed by:** <Checker> **Sheet:** 48 of 53

DMIC Array

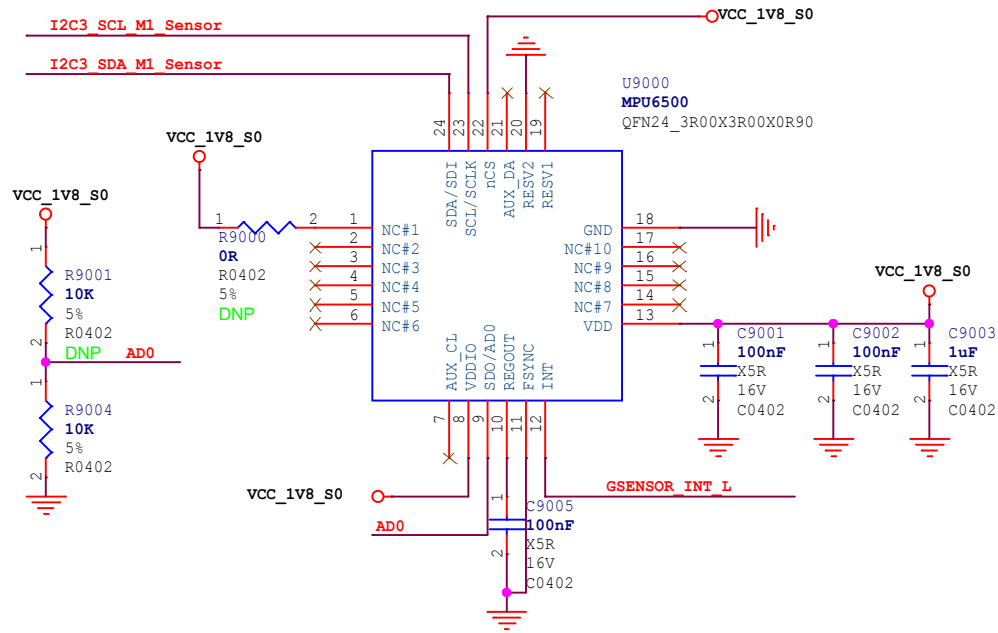


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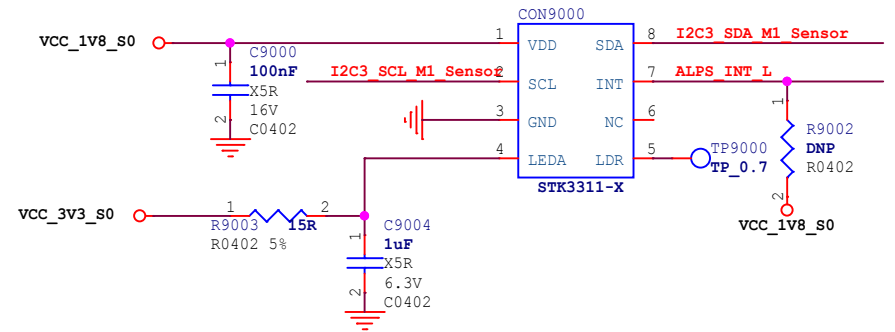
Rockchip Rockchip Electronics Co., Ltd

Project:	RK3588S_Tablet_REF		
File:	77.Audio-DMIC Array		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	49 of 53

Gyroscope+G-sensor



Ambient Light+Proximity Sensor



HALL SENSOR



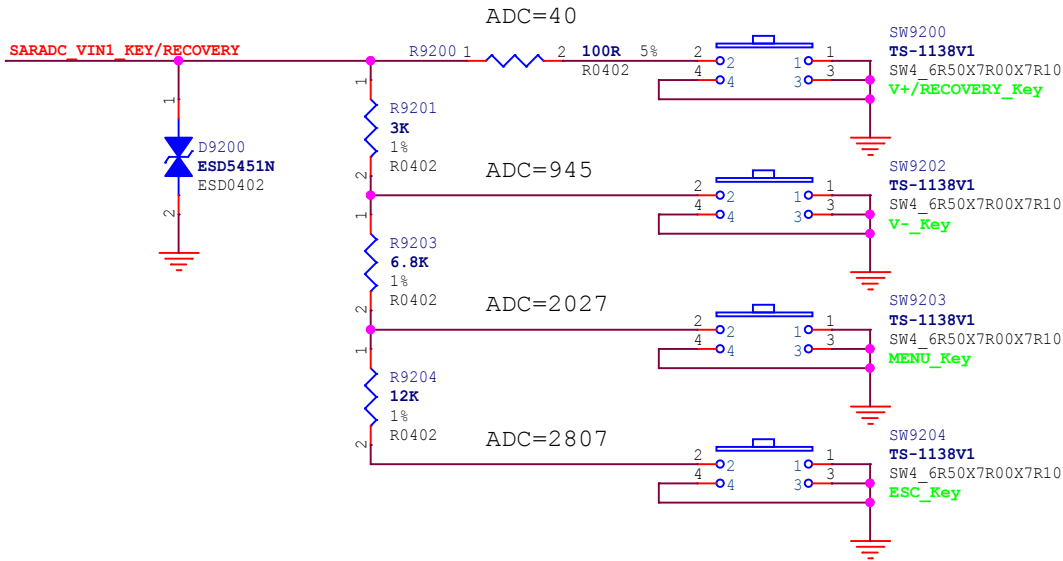
- >>> I2C3_SCL_M1_Sensor
- <<< I2C3_SDA_M1_Sensor
- >>> GSENSOR_INT_L
- <<< ALPS_INT_L
- <<< HALL_INT_L

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Project:	RK3588S_Tablet_REF		
File:	90.Sensor		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
		Sheet:	50 of 53

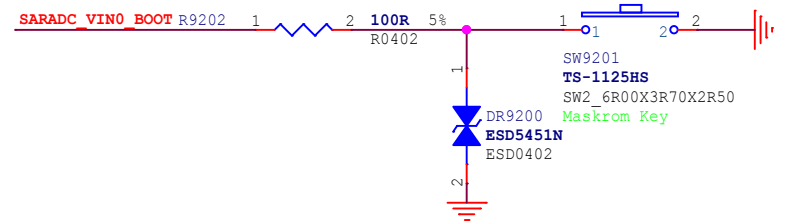
KEY Array

<< SARADC_VINI_KEY/RECOVERY



Maskrom Key

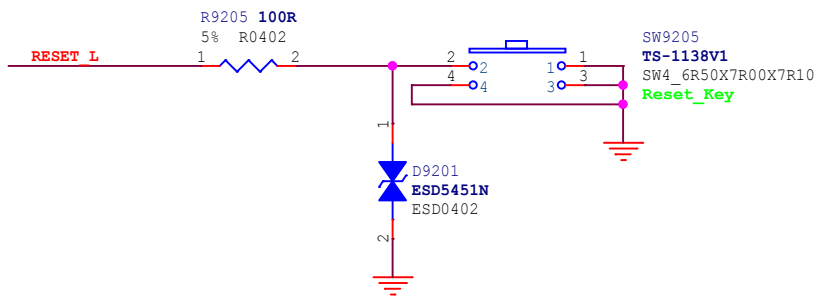
<< SARADC_VINO_BOOT



Note:
If BOOT SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

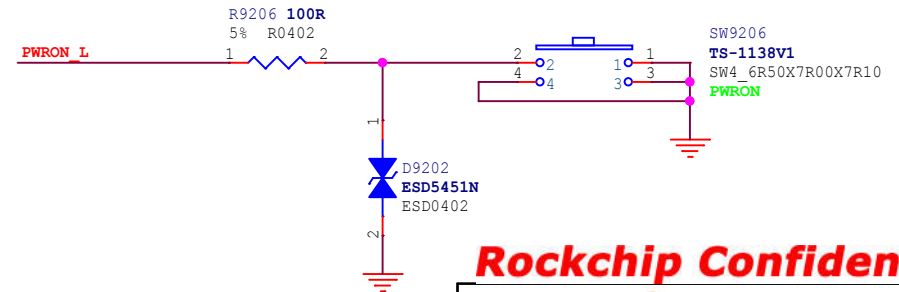
Reset_Key

<< RESET_L



PWR_Key

<< PWRON_L

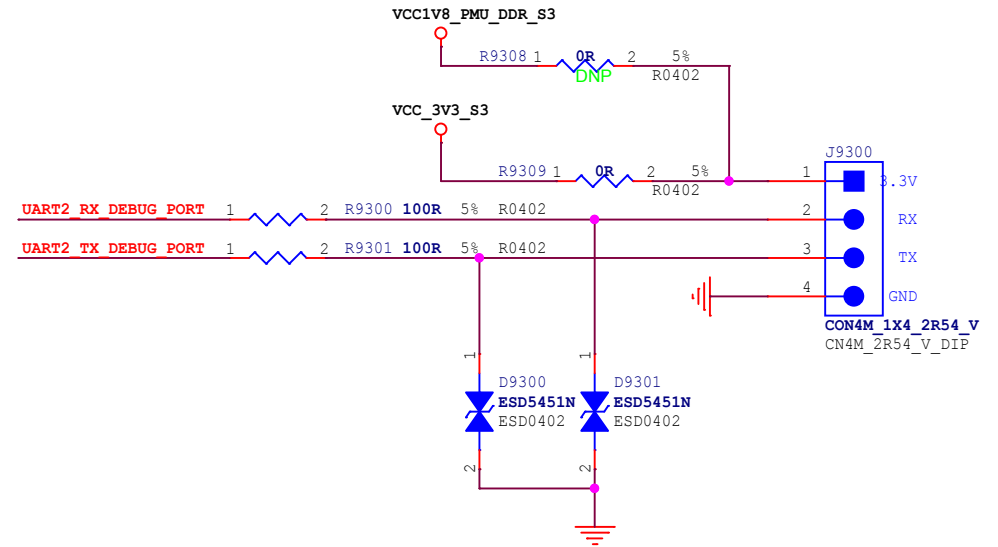
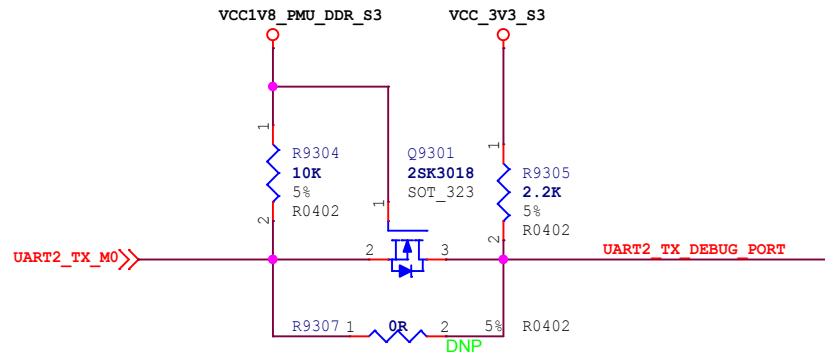
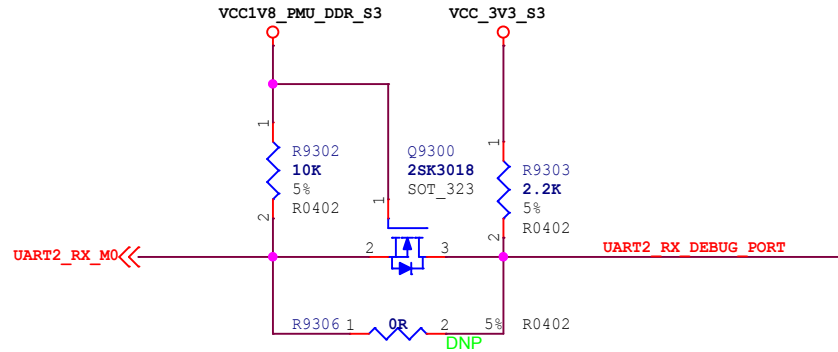


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Project:	RK3588S_Tablet_REF		
File:	92.KEY Array		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
Sheet:	51 of 53		

UART Debug

UART2_TX_M0 >>>
 UART2_RX_M0 <<<



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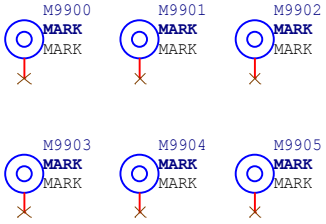
Project: RK3588S_Tablet_REF

File: 93.UART Debug

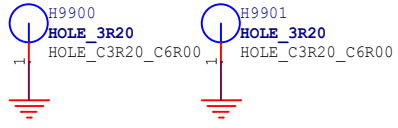
Date: Monday, February 21, 2022 Rev: V10

Designed by: Joseph Reviewed by: <Checker> Sheet: 52 of 53

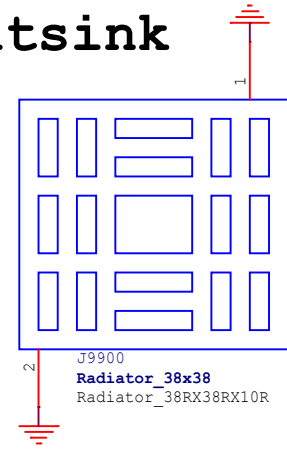
PCB Mark Point



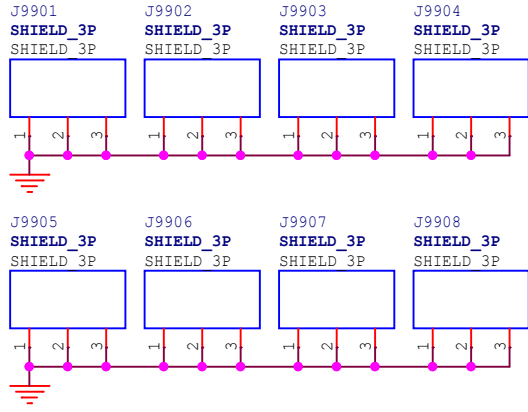
Mechanical Hole



Heatsink



Shield



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Project:	RK3588S_Tablet_REF		
File:	99.Mark/Heatsink		
Date:	Monday, February 21, 2022	Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>
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