JMB575

Port Multiplier
Data Sheet

Revision 1.2

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Revision History

Version	Date	Revision Description
1.2	2016/10/12	Correct typo
1.1	2013/09/02	1. Correct 3.13 description 2. Add 6. Flash Support list 3. Add 2.2 description
1.0	2013/05/29	Formal Release
0.9	2013/02/07	Draft Release

Table of Contents

1. Overview

JMicron JMB575 is a single chip. It integrated six independent SATA channels and a micro-processor. With proper setting, the chip can be configured as an 1 to 5-ports Serial ATA III Port Multiplier or a 5 to 1-port Serial ATA III Port Selector.

JMB575 contains 15 GPIOs which can be configured as various standard interfaces. It also has the capability to load external firmware code to extend its functionality.

JMB575 supports cascade mode which enables maximum 15 drives connected to one host.

2. Compliance, Features & Application

2.1 Compliance

- Compliant with ***Serial ATA Port Multiplier Spec. Revision 1.2***
- Compliant with ***Serial ATA Port Selector Spec. Revision 1.0***
- Compliant with ***Serial ATA PHY Electrical Spec. Revision 1.0***
- Compliant with ***Serial ATA High Speed Serialized AT Attachment Spec. Revision 3.1***

2.2 General

- Integrated 6-port SATA III PHY
- Integrated PLL for SATA III interface
- Total six independent SATA channels
- Integrated uP, PROM and SRAM for firmware programming
- 1.2V core and 3.3V I/O power supply
- Available in 64-pin QFN
- The external flash memory is mandatory for all applications

2.3 SATA

- Supports 6-port 6Gb/s SATA III interface
- Output swing control and automatic impedance calibration for SATA III PHY
- Supports asynchronous signal recovery
- Automatic speed negotiation
- Supports BIST and loopback mode
- Supports staggered spin-up (Optional)
- Supports Hot-Plug
- Supports asynchronous notification
- Supports ATAPI drives
- Supports command-based and FIS-based switching
- Supports PM aware and non-PM aware host
- Supports cascade mode
- Supports FW upgrade by HOST

2.4 GPIO

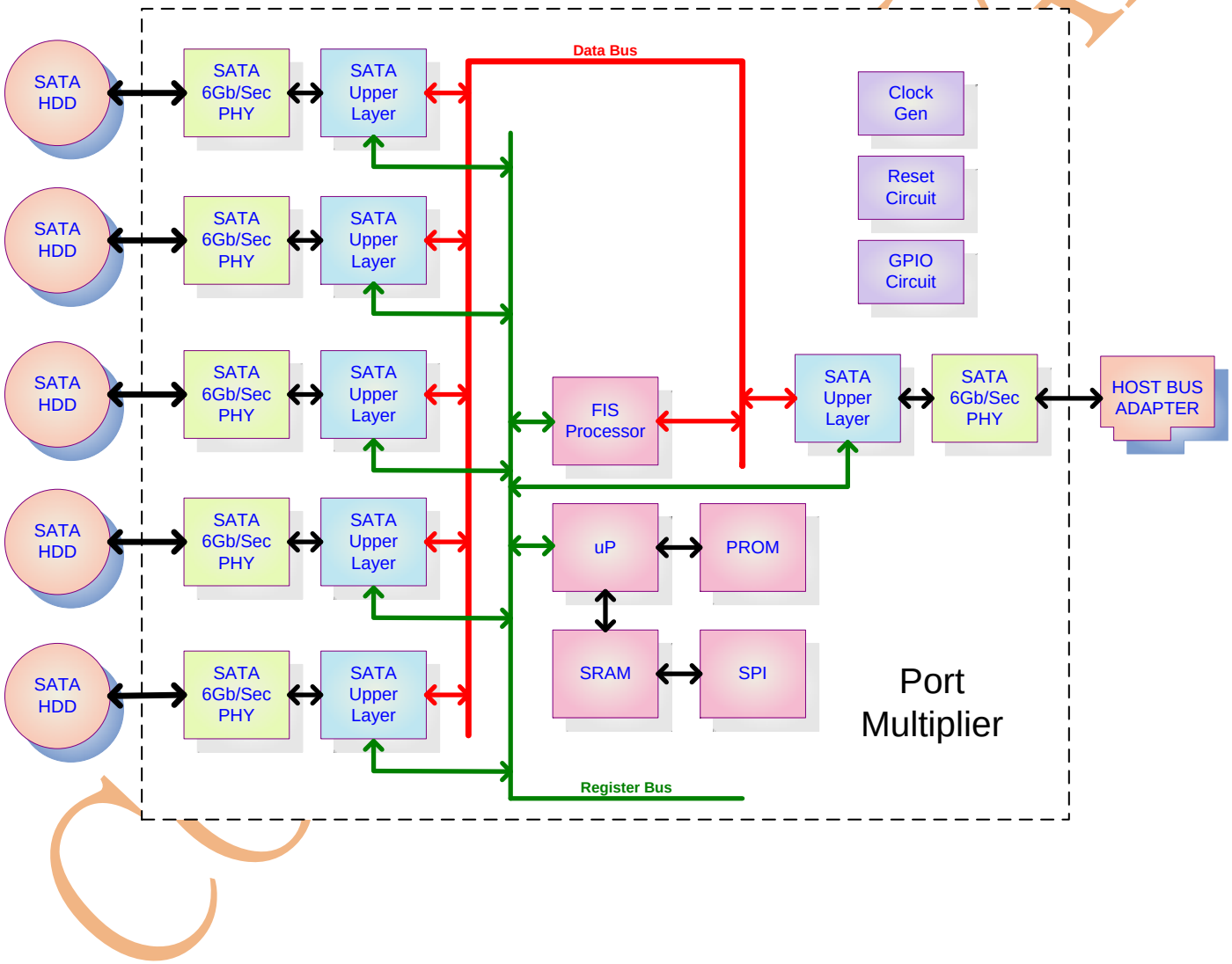
- Supports 15 GPIOs
- Supports SPI interface

3. Functional Description

JMB575 integrates six high-speed Serial I/O's, six SATA upper layers, a uP, SRAM, PROM and other control logic into the chip. JMB575 can work as a 1 to 5-ports Port Multiplier or 5 to 1-port Port Selector with internal embedded firmware without extra external flash needed. But it also can use external flash interface and with proper firmware programming to extend its capability.

3.1 Block Diagram

Figure 3.1 Function View of JMB575



3.2 Operating Mode

3.2.1 Normal Mode

When the pin XTSTN is tied to “high”, JMB575 works in normal mode. After power on sequence and reset operation, uP executes the programs stored in PROM. PROM program initializes settings of this chip and then, thru SPI bus, starts to load the external program and stores it in SRAM if the external flash is available and valid.

If the external program is loaded successfully, it will be executed by uP. Generally, the external firmware is customized program to fulfill various applications.

If JMB575 fails to load the external program, JMB575 works as a standard 1 to 5-ports Port Multiplier.

3.2.2 Test Mode

When the pin XTSTN is tied to “low”, JMB575 works in test mode.

3.3 Clock

The clock source of JMB575 is from AXIN pin. Clock rate is 25MHz. The internal PLL uses this 25MHz clock to generate various clock frequencies for different internal logic blocks of JMB575.

3.4 Reset

There are 2-level reset mechanisms in JMB575, i.e. Chip Reset and Protocol Reset.

3.4.1 Chip Reset

JMB575 uses XRSTN pin and internal Power-On Reset (POR) for Chip Reset. Chip Reset will initialize entire chip and make all circuit at default state. The micro processor will also restart to execute program from default entry point.

3.4.2 Protocol Reset

Protocol Reset is from host SATA OOB signal. It is used to reset SATA relative operation. The behavior of Protocol Reset is controlled by firmware code.

3.5 Data Bus

This high speed bus is enough to support all of the Port Multiplier or Port Selector operations.

3.6 Register Bus

Through Register Bus, uP controls and monitors all of the logic components in JMB575.

3.7 uP

uP and related data processing circuit will be in charge of

. data movement

. data comparison

. accumulate adding

Besides, several built-in timers will also help firmware control timing sequence and program flow.

3.8 FIS Processor

FIS (Frame Information Structure) processor helps uP communicate with SATA FIS protocol. The FIS Processor interprets the incoming SATA FIS and generates the outgoing SATA FIS for uP.

3.9 SATA Port

JMB575 is compliant with ***Serial ATA High Speed Serialized AT Attachment Spec. Revision 3.1***.

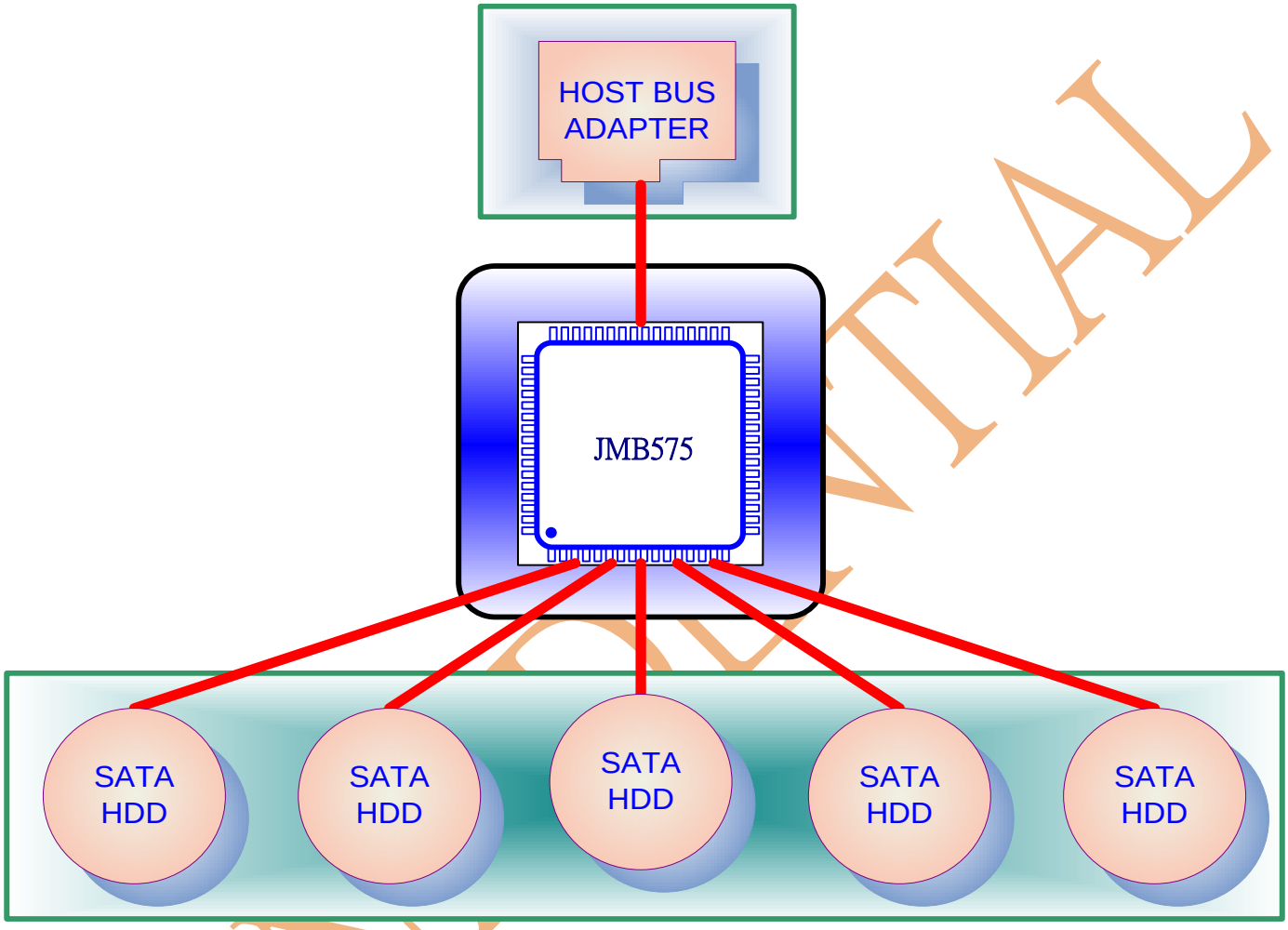
Each SATA port could be configured to be host mode (to connect to HDD) or to be device mode (to controller). Generally, users will just configure only one port to be device mode with other ports in host mode.

When a SATA port works under port multiplier condition, SATA FIS will be transferred straightly between host port and device port, without thru uP.

Built-in-self-test (BIST) circuit is implemented in each SATA port. Thru uP, each SATA port will be able to enter testing condition or to generate relevant testing patterns.

3.10 Port Multiplier Mode

A Port Multiplier is a mechanism for one active host connection to communicate with multiple devices. A Port Multiplier can be thought of as a simple multiplexer where one active host connection is multiplexed to multiple device connections, as shown below.



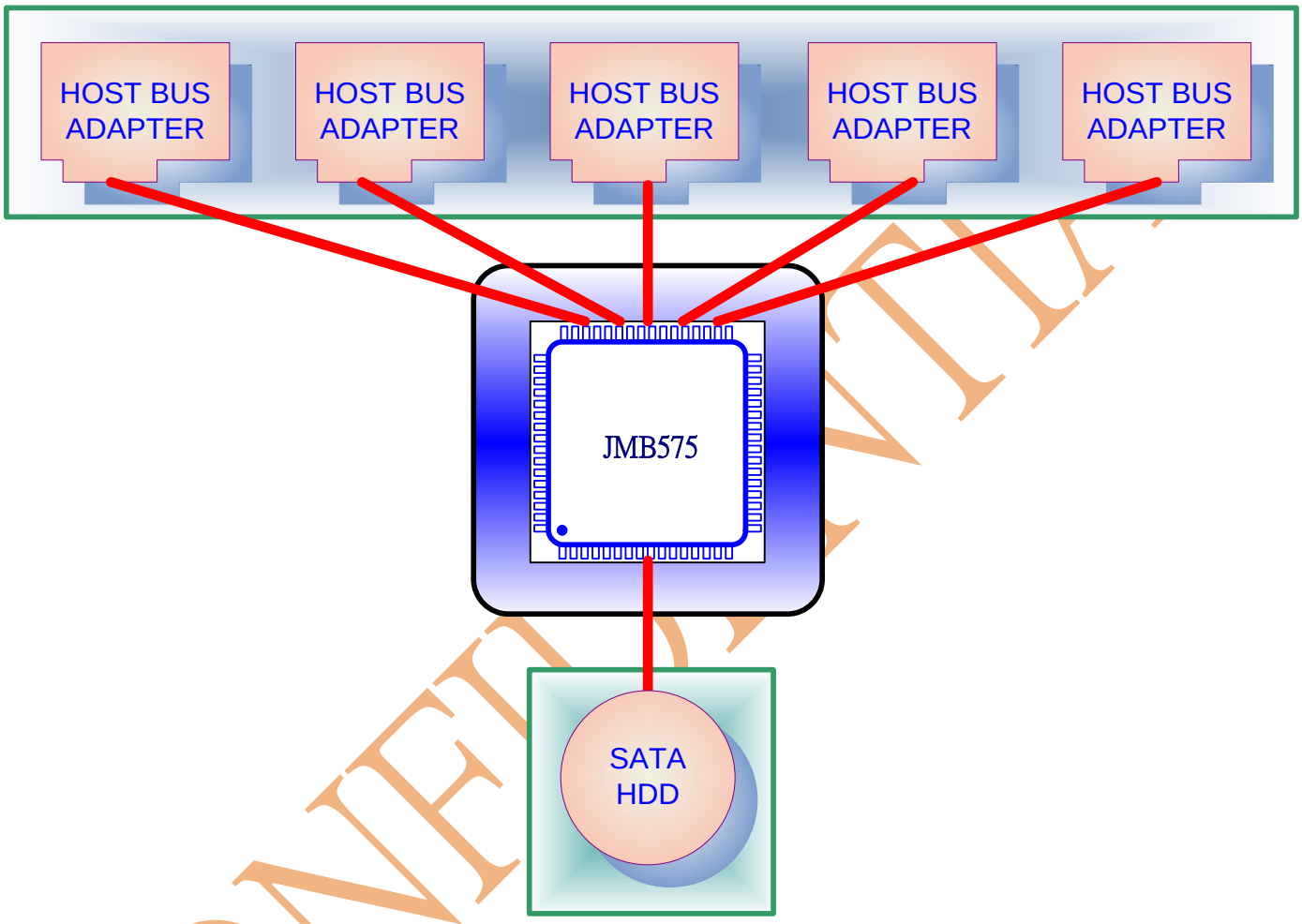
Port Multiplier can work under PM-aware or Legacy host controller. With PM-aware host controller, the Port Multiplier's operation is the same regardless of the switching type used by the host, Command-based switching or FIS-based switching.

When JMB575 is at this mode, the SATA ports are configured as:

Port 0: device port, connect to HDD 0
Port 1: device port, connect to HDD 1
Port 2: device port, connect to HDD 2
Port 3: device port, connect to HDD 3
Port 4: device port, connect to HDD 4
Port 5: host port, connect to Controller

3.11 Port Selector Mode

Port Selector is a mechanism that allows five different host ports to connect to the same device in order to create a redundant path to that device. Only one host connection to the device is active at a time. A Port Selector can be thought of as a simple multiplexer as shown below.



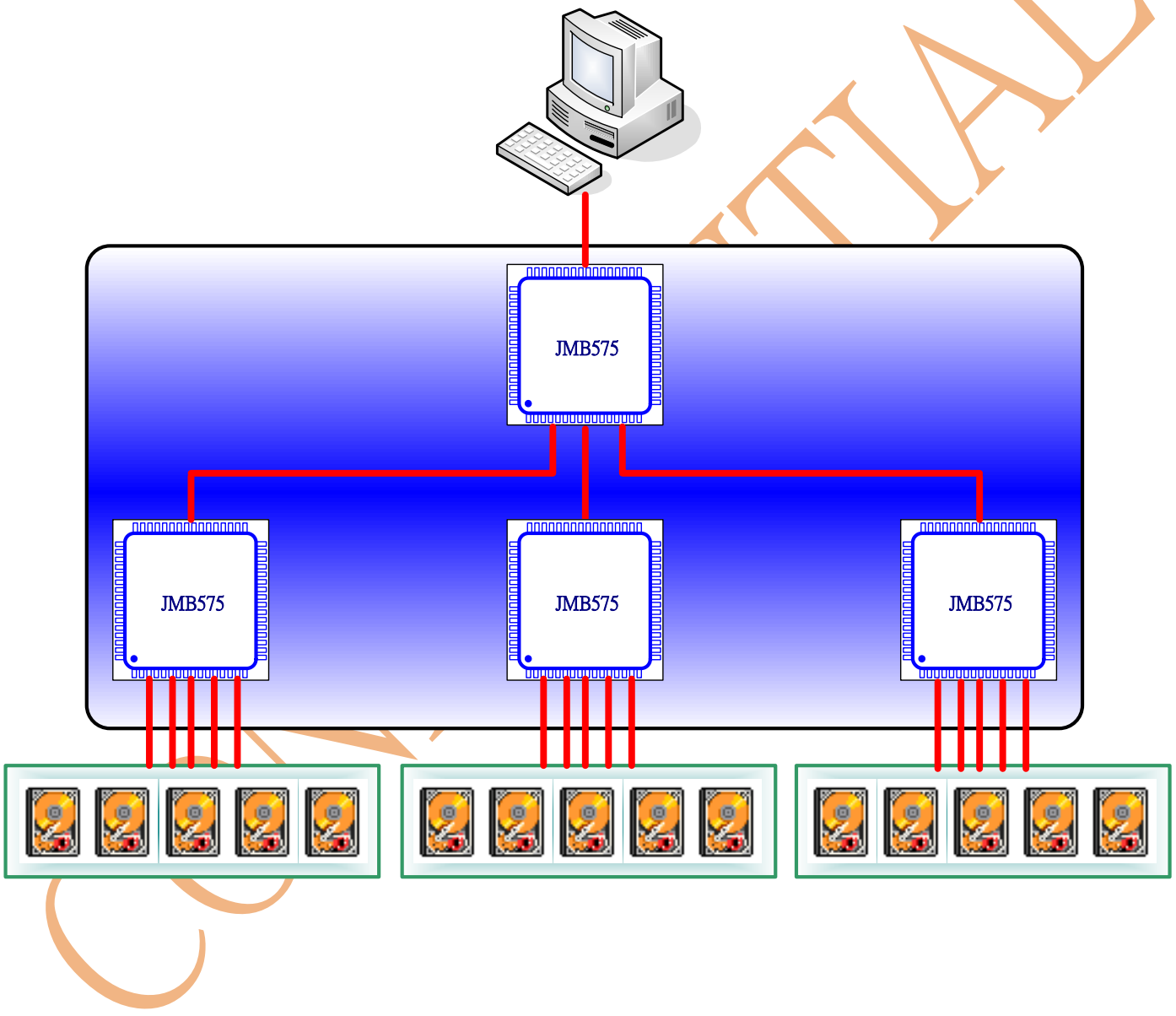
JMB575 supports only side-band port selection. The active host port is selected by the first successfully OOB linked SATA channel or by a hardware select line, GPIO pin.

When JMB575 is at this mode, the SATA ports are configured as:

Port 0: device port, connect to HDD
Port 1: host port, connect to Controller 0
Port 2: host port, connect to Controller 1
Port 3: host port, connect to Controller 2
Port 4: host port, connect to Controller 3
Port 5: host port, connect to Controller 4

3.12 Cascade Port Multiplier Mode

JMB575 supports to cascade another JMB575 to extend device number. Due to the restrictions of specification, the maximum device number extendable is 15. The requirements of specification are also maintained under this mode, for example, error propagation. The configuration of cascaded port multiplier can be treated as below:



3.13 LED Configuration

JMB575 external firmware code uses below GPIO pins to configure its LED operation mode.

Setting 1: 1 LED for 1 SATA Port as below:

GPIO00	SATA Port 0 Ready & Busy
GPIO02	SATA Port 1 Ready & Busy
GPIO04	SATA Port 2 Ready & Busy
GPIO01	SATA Port 3 Ready & Busy
GPIO03	SATA Port 4 Ready & Busy
GPIO05	SATA Port 5 Ready & Busy

Setting 2: 2 LEDs for 1 SATA Port as below:

GPIO00	SATA Port 0 Ready
GPIO01	SATA Port 0 Busy
GPIO02	SATA Port 1 Ready
GPIO03	SATA Port 1 Busy
GPIO04	SATA Port 2 Ready
GPIO05	SATA Port 2 Busy
GPIO06	SATA Port 3 Ready
GPIO07	SATA Port 3 Busy
GPIO08	SATA Port 4 Ready
GPIO09	SATA Port 4 Busy
GPIO10	SATA Port 5 Ready
GPIO11	SATA Port 5 Busy

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital 3.3V power supply	$DV33_{(ABS)}$		-0.3	3.63	V
Digital 1.2V power supply	$DV12_{(ABS)}$		-0.3	1.32	V
Analog 3.3V power supply	$AV33X_{(ABS)}$		-0.3	3.63	V
Analog 1.2V power supply	$AV12X_{(ABS)}$		-0.3	1.32	V
Digital I/O input voltage	$V_{I(D)}$		-0.3	3.63	V
Storage Temperature	$T_{STORAGE}$		-40	130	°C
Ambient operation temperature	T_A		0	70	°C
Junction Temperature	T_J			125	°C

4.2 Recommended Power Supply Operation Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	DV33		3.14	3.3	3.47	V
Digital 1.2V power supply	DV12		1.14	1.2	1.26	V
Analog 3.3V power supply	AV33X		3.14	3.3	3.47	V
Analog 1.2V power supply	AV12X		1.14	1.2	1.26	V

4.3 Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				25		MHz
Clock Duty Cycle			45	50	55	%

4.4 Power Supply DC Characteristics

4.4.1 IDLE

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	DV33			19.1		mA
Digital 1.2V power supply	DV12			195		mA
Analog 3.3V power supply	AV33X			81.4		mA
Analog 1.2V power supply	AV12X			390		mA

4.4.2 OPERATING

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	DV33			35.4		mA
Digital 1.2V power supply	DV12			203		mA
Analog 3.3V power supply	AV33X			81.4		mA
Analog 1.2V power supply	AV12X			389		mA

4.4.3 SUSPEND

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	DV33			5.5		mA
Digital 1.2V power supply	DV12			113		mA
Analog 3.3V power supply	AV33X			19.8		mA
Analog 1.2V power supply	AV12X			129		mA

4.5 I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.7	V
Input high voltage	V_{IH}		1.5			V
Output low voltage	V_{OL}				0.3	V
Output high voltage	V_{IH}		1.9			V

5. Pin Description

Pin Description for all pins described in Section 5 are under Normal mode. Once other operating modes are selected except Normal mode, all pins have different definition.

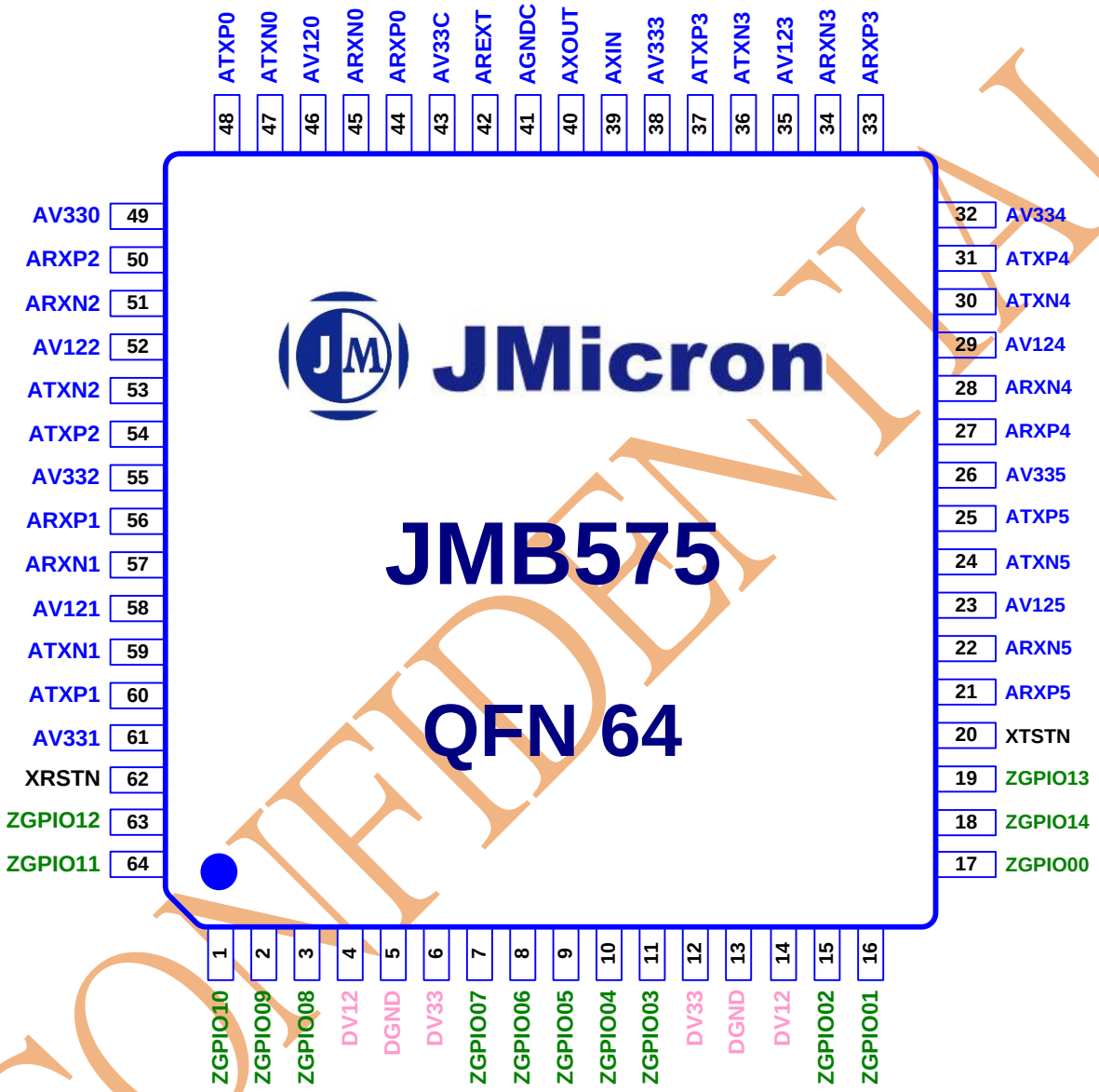
5.1 Pin List Table

Table 5-1 Pin List Table of JMB575

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	ZGPIO10	17	ZGPIO00	33	ARXP3	49	AV330
2	ZGPIO09	18	ZGPIO14	34	ARXN3	50	ARXP2
3	ZGPIO08	19	ZGPIO13	35	AV123	51	ARXN2
4	DV12	20	XTSTN	36	ATXN3	52	AV122
5	DGND	21	ARXP5	37	ATXP3	53	ATXN2
6	DV33	22	ARXN5	38	AV333	54	ATXP2
7	ZGPIO07	23	AV125	39	AXIN	55	AV332
8	ZGPIO06	24	ATXN5	40	AXOUT	56	ARXP1
9	ZGPIO05	25	ATXP5	41	AGNDC	57	ARXN1
10	ZGPIO04	26	AV335	42	AREXT	58	AV121
11	ZGPIO03	27	ARXP4	43	AV33C	59	ATXN1
12	DV33	28	ARXN4	44	ARXP0	60	ATXP1
13	DGND	29	AV124	45	ARXN0	61	AV331
14	DV12	30	ATXN4	46	AV120	62	XRSTN
15	ZGPIO02	31	ATXP4	47	ATXN0	63	ZGPIO12
16	ZGPIO01	32	AV334	48	ATXP0	64	ZGPIO11

5.2 Pin Diagram

Figure 5-1 64-Pin QFN



A: Analog, D: Digital, I: Input, O: Output, Z: I/O, L: Internal pull-low, H: Internal pull-high, S: Smittch Trigger Input, PWR: Power, GND: Ground

5.3 System Control Pin

Table 5-2 System Control Pin

Signal	Location	Type	Description
XTSTN	20	DIH	**Test Mode Enable.** Low-active signal to enable testing and debug modes.
XRSTN	62	DIH	**Whole Chip Reset#** Low-active signal used to reset whole chip except PLL.

5.4 General Purpose Input/Output Pin

Table 5-3 General Purpose Input/Output Pin

Signal	Location	Type	Description
ZGPIO00	17	DZ	**GPIO Pin 0.** General Purpose Input/Output.
ZGPIO01	16	DZ	**GPIO Pin 1.** General Purpose Input/Output.
ZGPIO02	15	DZ	**GPIO Pin 2.** General Purpose Input/Output.
ZGPIO03	11	DZ	**GPIO Pin 3.** General Purpose Input/Output.
ZGPIO04	10	DZ	**GPIO Pin 4.** General Purpose Input/Output.
ZGPIO05	9	DZ	**GPIO Pin 5.** General Purpose Input/Output.
ZGPIO06	8	DZ	**GPIO Pin 6.** General Purpose Input/Output.
ZGPIO07	7	DZ	**GPIO Pin 7.** General Purpose Input/Output.
ZGPIO08	3	DZ	**GPIO Pin 8.** General Purpose Input/Output.
ZGPIO09	2	DZ	**GPIO Pin 9.** General Purpose Input/Output.
ZGPIO10	1	DZ	**GPIO Pin 10.** General Purpose Input/Output
ZGPIO11	64	DZ	**GPIO Pin 11.** General Purpose Input/Output
ZGPIO12	63	DZ	**GPIO Pin 12.** General Purpose Input/Output.
ZGPIO13	19	DZ	**GPIO Pin 13.** General Purpose Input/Output.
ZGPIO14	18	DZ	**GPIO Pin 14.** General Purpose Input/Output.

5.5 SATA III Analog Pin

Table 5-4 SATA III Analog Pin

Signal	Location	Type	Description
AREXT	42	AI	**External Reference Resistor.** An external 12KΩ resistor should be connected and bypass to the AGNDC.

AXIN	39	AI	**Crystal/Oscillator Input.** Connect to an external crystal/oscillator. The clock rate is 25Mhz.
AXOUT	40	AO	**Crystal Output.** Connect to an external crystal.
ATXP0	48	AO	**Port 0 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN0	47	AO	**Port 0 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP0	44	AI	**Port 0 Serial Data Receiver.** It receives positive input of differential signal.
ARXN0	45	AI	**Port 0 Serial Data Receiver.** It receives negative input of differential signal.
ATXP1	60	AO	**Port 1 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN1	59	AO	**Port 1 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP1	56	AI	**Port 1 Serial Data Receiver.** It receives positive input of differential signal.
ARXN1	57	AI	**Port 1 Serial Data Receiver.** It receives negative input of differential signal.
ATXP2	54	AO	**Port 2 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN2	53	AO	**Port 2 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP2	50	AI	**Port 2 Serial Data Receiver.** It receives positive input of differential signal.
ARXN2	51	AI	**Port 2 Serial Data Receiver.** It receives negative input of differential signal.
ATXP3	37	AO	**Port 3 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN3	36	AO	**Port 3 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP3	33	AI	**Port 3 Serial Data Receiver.** It receives positive input of differential signal.
ARXN3	34	AI	**Port 3 Serial Data Receiver.** It receives negative input of differential signal.

ATXP4	31	AO	**Port 4 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN4	30	AO	**Port 4 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP4	27	AI	**Port 4 Serial Data Receiver.** It receives positive input of differential signal.
ARXN4	28	AI	**Port 4 Serial Data Receiver.** It receives negative input of differential signal.
ATXP5	25	AO	**Port 5 Serial Data Transmitter.** It transmits positive output of differential signal.
ATXN5	24	AO	**Port 5 Serial Data Transmitter.** It transmits negative output of differential signal.
ARXP5	21	AI	**Port 5 Serial Data Receiver.** It receives positive input of differential signal.
ARXN5	22	AI	**Port 5 Serial Data Receiver.** It receives negative input of differential signal.

5.6 Power/Ground Pin

Table 5-5 Power and Ground Pin

Signal	Location	Type	Description
AVDDC	43	PWR	**Analog SATA III PLL Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AGNDC	41	GND	**Analog SATA III PLL Ground.** It is ground for AVDD0.
AV120	46	PWR	**Analog SATA III Port 0 PHY Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV121	58	PWR	**Analog SATA III Port 1 PHY Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV122	52	PWR	**Analog SATA III Port 2 PHY Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV123	35	PWR	**Analog SATA III Port 3 PHY Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV124	29	PWR	**Analog SATA III Port 4 PHY Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV125	23	PWR	**Analog SATA III Port 5 PHY Power.**

			It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
AV330	49	PWR	**Analog SATA III Port 0 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AV331	61	PWR	**Analog SATA III Port 1 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AV332	55	PWR	**Analog SATA III Port 2 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AV333	38	PWR	**Analog SATA III Port 3 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AV334	32	PWR	**Analog SATA III Port 4 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
AV335	26	PWR	**Analog SATA III Port 5 PHY Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
DV33	6/12	PWR	**I/O Pad Power.** It is 3.3V and should be bypassed to ground by a 0.1uF capacitance.
DV12	4/14	PWR	**Digital Core Power.** It is 1.2V and should be bypassed to ground by a 0.1uF capacitance.
DGND	5/13	GND	**I/O Pad and Digital Core Ground.** It is ground for I/O pad and digital core.

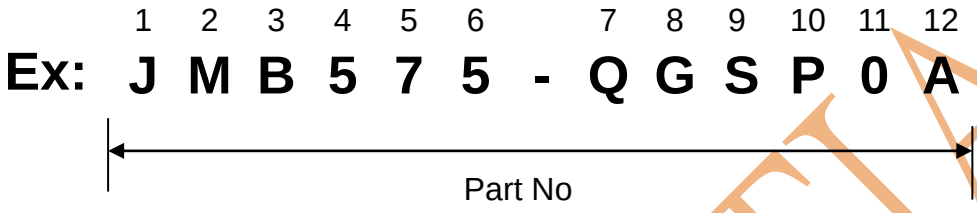
6. Flash Support List

Vendor Name	Model Name	Model Name	Model Name
PMC	25LV512	25LD010 CE1001	25LV010 AE1008
	25LD512 CE1007	PM25LV010 1M	25LD512 AE0935
	25LD512 CE0953	PM25LV020 2M	
MXIC	25L512 MC	25L4006E	25L512E
	25L512 CM1	25L8006E	25L1006E
	25L2005 MC	25L1606E	25L2006E
	25L4005 AMC	25L3206E	25L8035E
	25L1605 DM2I	25L6406E	25L6445E
	25L8005 MC	25L1633E	25V4006E
AMIC	A25L5120-F	A25L016M-F	A25L032M-F
	A25L040M-F		
Winbond	W25X10 AING	W25X10CLSNIG(2.5V)	W25X40BLSNIG
	25X10AVNIG	W25X20CLSNIG(2.5V)	W25X05CLSNIG(2.5V)
	25X10BVNIG	W25X20BVSNGT	25Q16CVSIG
	W25X20BLSNIG(2.5V)	25X40CLNIG	25X40CLVIG
	W25X10BLSNIG	25Q80BLNIG	
EON	P05-50GCP	F16-100 HIP	F10-100 GIP
	EN25F05-100GIP	F80-100 HCP	F40-100 GCP
	F20-100 GCP	Q64-104 HIP	LF10-75GIP
	F32-100 H1P	Q80A-100HIP	LF40-75GIP
ATMEL	25FS010	AT25F-512B	
PFlash	PM25LD020-SCE(2.5V)	PM25LD040	
Sanyo	LE25FU206AMB(2.5V)		
ESMT	F25L01PA	F25L04PAG1SM	F25L02PA
	F25L05PA		
Giga Device	25Q512T	25Q20T	25Q40T
	25Q10T		
SHANGHAI FUDAN	FM25F02	FM25F04	

7. Package Information

JMB575 is fabricated with CMOS Standard Logic Process with 1.2V core and 3.3V I/O voltages and is available with 64-pin QFN package. JMicron uses 12 digits number for part number shown below. Figure 6-1 shows the physical dimension.

QFN64



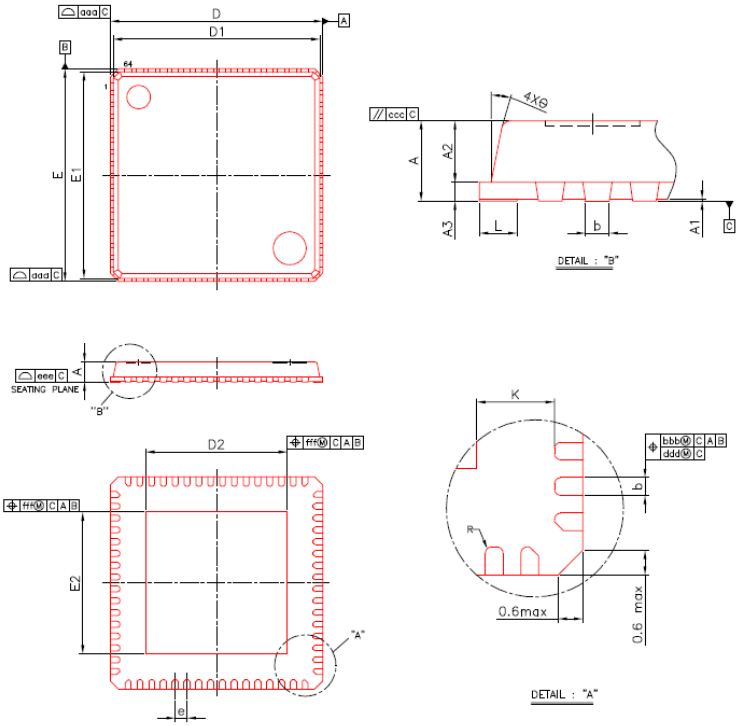
The comparison table of numbering

Digit	Classification	Numbering	Definition
1~2	Brand Name	JM	JMicron
3	Product Index	B,C,P…	B: Bridge C: Communication P: PHY Chip S: SOC V: Video E: EVB (Evaluation Board)
4~6	Product Serial Number	001~999	A serial no, it's up to the real situation
7	Assembly Type	T, L, S…	See the comparison table of assembly type
8	Environment Indicate	S, G	S: Standard Package G: Green Package
9	Bonding Type	A~Z	Same product has a different bonding, from A~Z
10~11	Code Mask	A0~Z9	Same product has a code mask change, from A0~Z9, ROM-free default is Z0
12	Version Code	A~Z	Dice Revision (From A to Z)

The comparison table of package type

Numbering	Assembly Type
T	TQFP
L	LQFP
Q	QFN
S	SOP
N	TSSOP
R	SSOP
B	BGA

Figure 6-1 Physical Dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		9.00 BSC			0.354 BSC	
D1/E1		8.75 BSC			0.344 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

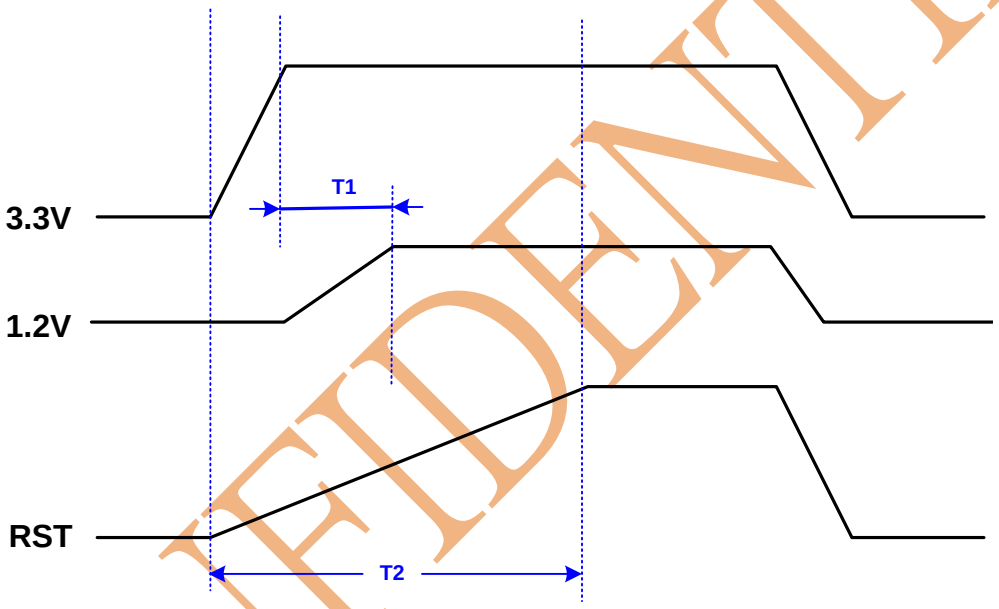
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

L/F	Exposed Pad Size					
	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
①	5.85	6.00	6.15	0.230	0.236	0.242
②	3.64	3.79	3.94	0.143	0.149	0.155
③	5.49	5.64	5.79	0.216	0.222	0.228
④	6.75	6.90	7.05	0.266	0.272	0.278
⑤	5.05	5.20	5.35	0.199	0.205	0.211
⑥	5.05/6.09	5.20/6.24	5.35/6.39	0.199/0.240	0.205/0.246	0.211/0.252

8. Power Sequence and Reset Timing

If external power design is applied, designers should make sure that the 3.3V power rail ramps prior to the 1.2V power rail to prevent excessive current leakage onto the 3.3V power rail. It is not acceptable if 1.2V power rail ramps prior to 3.3V power rail. Except for 1.2V power rail, reset signal should be also taken into consideration. Designers should make sure that the 3.3V power rail ramps prior to the reset signal for system normal operating purpose. It is not acceptable if reset signal ramps prior to 3.3V power rail. To sum up, there are two necessary requirements for external power design.

1. T1: The minimum timing requirement from 3.3V power rail reaching high state (3.3V) to 1.2V power rail reaching high state (1.2V) is 200us.
2. T2: The minimum timing requirement from 0V to reset rail reaching high state (3.3V) is 12ms.



Time	Min.	Max.
T1	200us	10ms
T2	12ms	500ms

Figure 7.1 Power Sequence and Reset Timing