ITE 聯陽半導體 ITE Tech. Inc.

IT6161

MIPI to HDMI Converter

Preliminary Specification V0.8.8

ITE TECH. INC.

To find out more about ITE, visit our World Wide Web at:
http://www.ite.com.tw

Or e-mail itesupport@ite.com.tw for more product information/services

Revision History

Section	Revision	Page No.
0.5.0	Release first version	
0.6.0	Add Power consumption data	
0.7.0	Add SMD resistor	
0.8.0	Add IDDQ Standby Power	
0.8.5	Change package pin pitch from 0.4mm to 0.5mm	
0.8.6		
0.8.7	REXT Description	
0.8.8	QFN56 T1(8x8)	

CONTENTS

FIGURES

TABLES

1. Features

- **4-lane MIPI RX with total 4Gbps bandwidth**
- **Flexible MIPI Rx lane swap and P/N swap configuration**
- **Compliant with MIPI D-PHY 1.1 and DSI 1.1 specifications**
- **Single HDMI transmitter**
- **Compliant with HDMI 1.4b, HDCP 1.4 and DVI 1.0 specifications**
- **Supporting pixel rates from 25MHz to 165MHz:**
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i up to 1080p
  - PC resolutions: VGA, SVGA, XGA, SXGA up to UXGA
- **Support output channel swap and P/N swap**
- **Supporting the following 24-bit RGB 4:4:4 progressive video formats:**
  - DTV resolutions: 480p, 576p, 720p,up to 1080p
  - PC resolutions: VGA, SVGA, XGA, up to SXGA
- **Various Packed Pixel Stream of DSI are supported, such as:**
  - 18/24 bit RGB 4:4:4
  - 18-bit RGB 4:4:4 (Loosely)
- **Support HDMI1.4 3D feature**
  - Frame packing mode up to 1080P@23.98/24Hz and 720P@59.94/60Hz
  - Top and bottom up to 1080P@59.94/60Hz
  - Side-by-side (half) up to 1080P@59.94/60Hz
  - Side-by-side (full) up to 720P@59.94/60Hz
- **Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.**
- **Support digital audio input interface**
  - sample size: 16~24 bits
  - four I^2S interfaces supporting 8-channel audio
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio transmission at up to 192kHz
  - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I^2S interface or the S/PDIF interface, with frame rates as high as 768kHz
  - Compatible with IEC 60958 and IEC 61937
- **Software programmable HDMI output current, enabling users to optimize performance for fixed-cable systems or those with pre-defined cable length**
- **MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK.**
- **Integrated pre-programmed HDCP keys**
- **Purely hardware HDCP engine increasing robustness and security of HDCP operation**
- **Monitor detection through Hot Plug Detection and Receiver Termination Detection**
- **Embedded full-function pattern generator**
- **Intelligent, programmable power management**

- **Embedded hardware controlled CEC PHY**
- **56-pin (8x8 mm) QFN package**

2. General Description

The IT6161 is a high-performance and low-power MIPI to HDMI converter, fully compliant with MIPI D-PHY 1.1, DSI 1.1 and HDMI 1.4b, HDCP 1.4 and backward compatible to DVI 1.0 specifications. The IT6161 supports four lanes MIPI RX and HDMI TX interface. The data transfer rate of MIPI RX is up to 1Gbps per lane.

IT6161 support MIPI DSI packed pixel stream 24-bit RGB888 ,loosely packed pixel stream 18-bit RGB666 and packed pixel stream 18-bit RGB666 mode, the sync even short packets can be received and generate HSync and VSync by firmware setting. A Pattern Generator is embedded in the IT6161 and thus the video data and timing can be easily switched from external MIPI RX to internal pattern generator for testing.

MIPI input 1/2/4-lane swap and HDMI output channel swap and PN swap can be controlled separately for flexible circuit layout.

Aside from the various video output formats supported, the IT6161 also supports 8 channels of I^2S digital audio, with sampling rate up to 192kHz and sample size up to 24 bits. IT6161 also support S/PDIF input of up to 192kHz sampling rate.

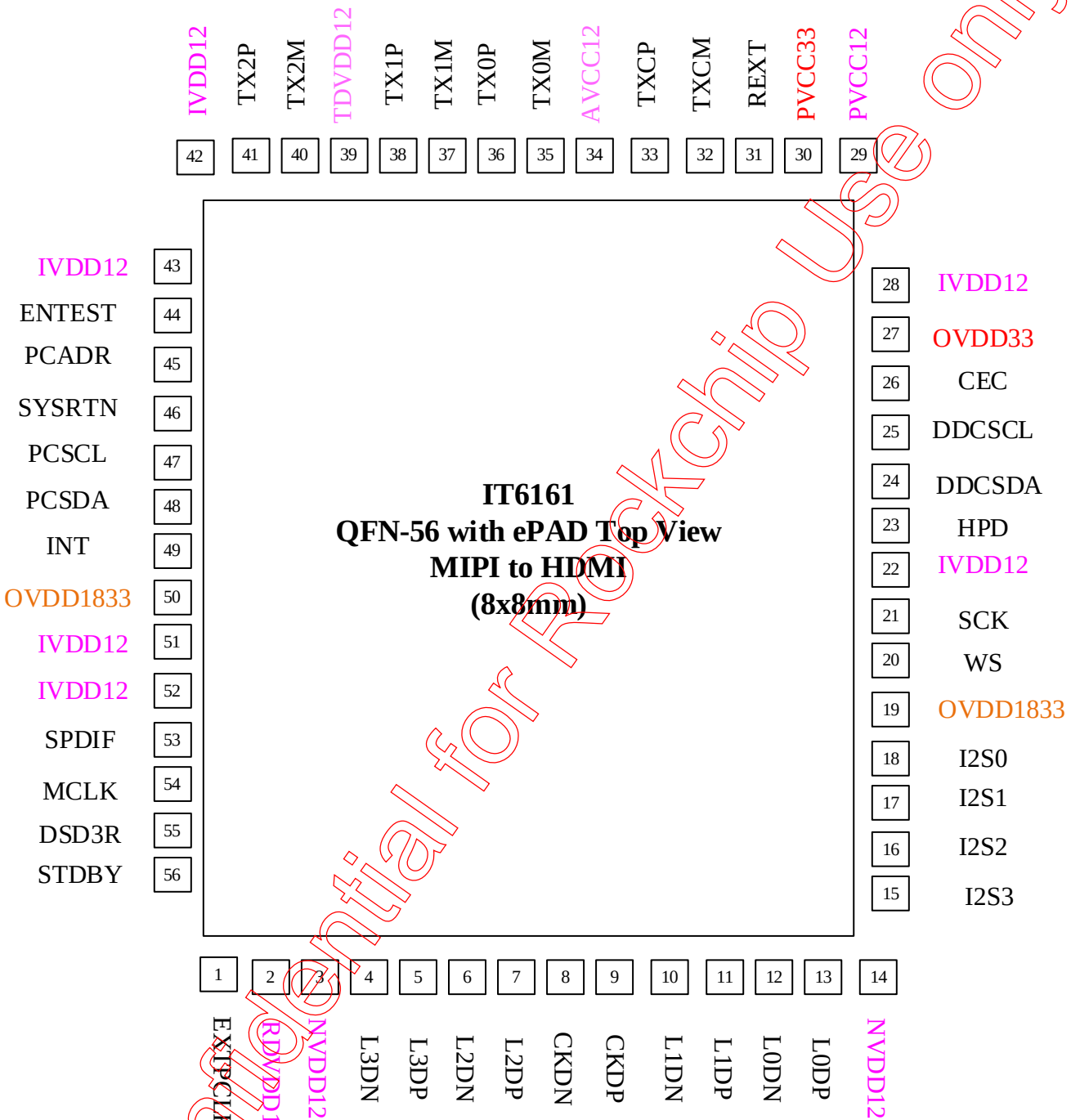
The newly supported High-Bit Rate (HBR) audio by HDMI Specifications v1.4b is provided by the IT6161 in two interfaces: with the four I^2S input ports or the S/PDIF input port. With both interfaces the highest possible HBR frame rate is supported at up to 768kHz

By default the IT6161 comes with integrated HDCP ROMs which are pre-programmed with HDCP keys that ensures secure digital content transmission. Users need not worry about the procurement and maintenance of the HDCP keys.

The IT6161 also provides a complete solution of Consumer Electronics Control (CEC) function. This optional CEC feature of HDMI specification allows the user to control two or more CEC-enabled devices through HDMI network. With IT6161 embedded CEC PHY, user can use high-level software API to easily implement all the necessary remote control commands. The CEC bus related protocol is handled by the CEC PHY which eliminates extra loading of the MCU.

IT6161 provide I2C interface for firmware setting . Please refer to the IT6161 Programming Guide if necessary.

3. Pin Configuration



4. Pin Description

Table 4-1. Digital Video input Pins

Pin Name	Direction	Description	Type	Pin No.
L0DP	Analog	***MIPI RX lane 0 positive signal***	MIPI	13
L0DN	Analog	***MIPI RX lane 0 negative signal***	MIPI	12
L1DP	Analog	***MIPI RX lane 1 positive signal***	MIPI	11
L1DN	Analog	***MIPI RX lane 1 negative signal***	MIPI	10
CKDP	Analog	***MIPI RX clock lane positive signal***	MIPI	9
CKDN	Analog	***MIPI RX clock lane negative signal***	MIPI	8
L2DP	Analog	***MIPI RX lane 2 positive signal***	MIPI	7
L2DN	Analog	***MIPI RX lane 2 negative signal***	MIPI	6
L3DP	Analog	***MIPI RX lane 3 positive signal***	MIPI	5
L3DN	Analog	***MIPI RX lane 3 negative signal***	MIPI	4

Table 4-2. Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
SCK	Input	***I2S mode: I2S serial clock input***	LVTTL	21
WS_DSD0L	Input	***I2S word select input*** ***DSD mode: DSD 0 serial Left data input***	LVTTL	20
I2S0_ DSD0R	Input	***I2S mode: I2S 0 serial data input*** ***DSD mode: DSD 0 serial Right data input***	LVTTL	18
I2S1_ DSD1L	Input	***I2S mode: I2S 1 serial data input*** ***DSD mode: DSD 1 serial Left data input***	LVTTL	17
I2S2_ DSD1R	Input	***I2S mode: I2S 2 serial data input*** ***DSD mode: DSD 1 serial Right data input***	LVTTL	16
I2S3_ DSD2L	Input	***I2S mode: I2S 3 serial data input*** ***DSD mode: DSD 2 serial Left data input***	LVTTL	15
SPDIF_DSD2R	Input	***S/PDIF mode: S/PDIF audio input*** ***DSD mode: DSD 2 serial Right data input***	LVTTL	53
MCLK_DSD3L	Input	***S/PDIF mode: S/PDIF master clock input*** ***DSD mode: DSD 3 serial Left data input***	LVTTL	54
DSD3R	Input	***DSD mode: DSD 3 serial Right data input***	LVTTL	55

Table 4-3. HDMI Interface Pins

Pin Name	Direction	Description	Type	Pin No.
CEC	I/O	***CEC signal (5V-tolerant)***	Schmitt 5V-TOL	26
DDCSCL	I/O	***I2C Clock for DDC (5V-tolerant)***	Schmitt 5V-TOL	25
DDCSDA	I/O	***I2C Data for DDC (5V-tolerant)***	Schmitt 5V-TOL	24
HPD	Input	***Hot Plug Detection (5V-tolerant)***	LVTTL 5V-TOL	23

Table 4-4. TMDS Front-End Interface Pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Analog	***HDMI channel 2 positive output***	TMDS	41
TX2M	Analog	***HDMI channel 2 negative output***	TMDS	40
TX1P	Analog	***HDMI channel 1 positive output***	TMDS	38
TX1M	Analog	***HDMI channel 1 negative output***	TMDS	37
TX0P	Analog	***HDMI channel 0 positive output***	TMDS	36
TX0M	Analog	***HDMI channel 0 negative output***	TMDS	35
TXCP	Analog	***HDMI clock channel positive output***	TMDS	33
TXCM	Analog	***HDMI clock channel negative output***	TMDS	32
REXT	Analog	***External resistor for setting TMDS output level. Default tied to AGND via a 5.6k-Ohm SMD resistor***	Analog	31

Table 4-5. Programming Pins

Pin Name	Direction	Description	Type	Pin No.
PCSCL	Input	***Serial programming clock for chip programming***	Schmitt	47
PCSDA	I/O	***Serial programming data for chip programming***	Schmitt	48
PCADR	Input	***Serial programming device address select Default pull-down low internally for slave address 0x98 Tied to OVDD1833 via a 4.7K ohm resistor for slave address 0x9A***	LVTTL	45
INT	Output	***Interrupt output, default active low***	LVTTL	49

Table 4-6. System Control Pins

Pin Name	Direction	Description	Type	Pin No.
ENTEST	Input	***Must be tied low via a resistor***	LVTTL	44
SYSRSTN	Input	***Hardware reset pin, active low***	Schmitt	46
EXTPCLK	Input	***External pixel clock input***	LVTTL	1
STDBY	Input	***External standby function control signal***	LVTTL	56

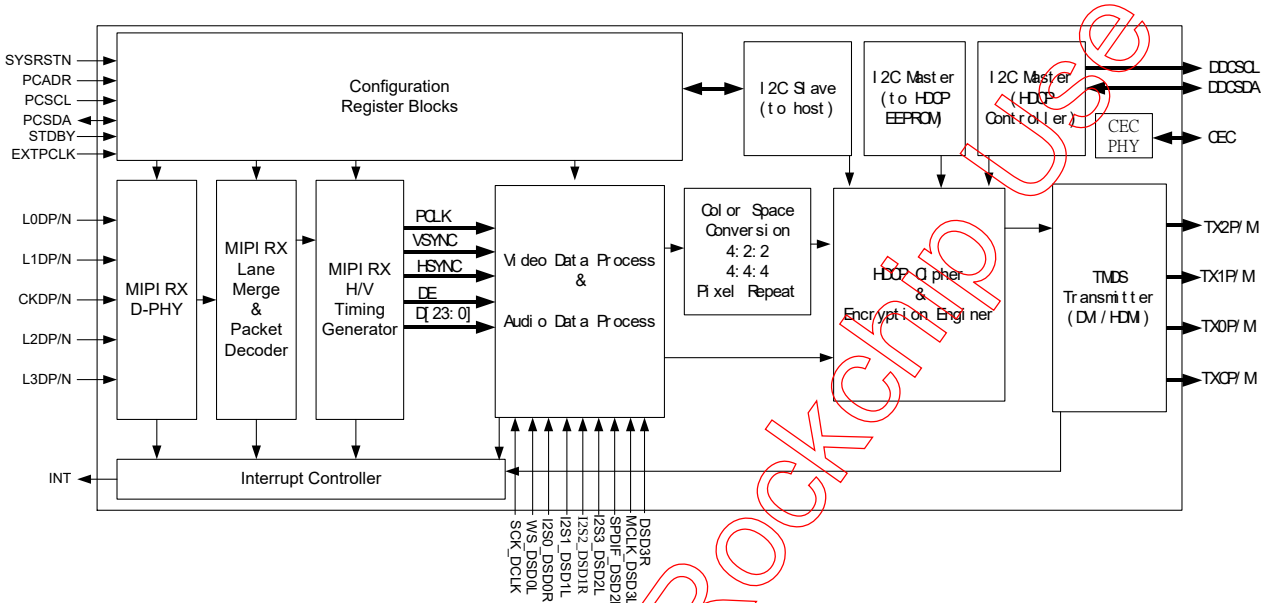
Table 4-7. Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD12	***Digital logic power (1.2V)***	Power	22,28,42,43,51,52
OVDD1833	***I/O Pin power (1.8V to 3.3V)***	Power	19,50
OVDD33	***5V-tolerant I/O power (3.3V)***	Power	27
PVCC33	***HDMI core PLL power (3.3V)***	Power	30
PVCC12	***HDMI core PLL power (1.2V)***	Power	29
AVCC12	***HDMI analog frontend power (1.2V)***	Power	34
TDVDD12	***HDMI digital frontend power (1.2V)***	Power	39
NVDD12	***MIPI analog frontend power (1.2V)***	Power	3,14
RDVDD12	***MIPI digital frontend power (1.2V)***	Power	2
GND	***Common ground***	Ground	0

5. Functional Description

IT6161 is a MIPI RX to HDMI TX converter and provides complete solutions for HDMI 1.4 Source systems by implementing all the required HDMI functions
. The following picture is the functional block diagram of IT6161, which describes clearly the data flow.

Figure 5-1. Functional Block Diagram of IT6161



5.1 Video Data Processing Flow

- MIPI RX D-PHY

MIPI RX D-PHY implements four unidirectional data lanes and one clock lane. The operating mode of data lane could be Control or High-Speed mode. However, the clock lane can only support continuous clock because the pixel clock for HDMI is generated from this differential DDR clock. An internal PLL is used to generate the HDMI pixel clock. Please refer to the IT6161 Programming Guide for the PLL setting.

- MIPI RX Lane Merge and Packet Decoder

Base on the video bandwidth, MIPI RX D-PHY can be configured as 1/2/3/4-lane and Lane Merge function combines input data to a uniform 32-bit internal bus for further processing. Packet Decoder is used to check the ECC and CRC error. One-bit error in the Packet Header can be automatically corrected by the ECC function.

- MIPI RX H/V Timing Generator

The H/V Timing Generator uses Sync Event to generate video HSync and VSync timing. Both Sync Pulse and Sync Event mode are supported by the IT6161. The generated video timing parameters can be over-written by firmware if necessary.

- Video Processor and Pattern Generator

Figure 5-2 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enabling and path bypassing are controlled through register programming. Please refer to IT6161 Programming Guide for detailed and precise descriptions.

As can be seen from Figure 5-2, the first step of video data processing is to prepare the video data (Data), data enable signal (DE), video clock (Clock), horizontal sync and vertical sync signals (H/VSYNC). While the video data and video clock are always readily available from input pins, the preparation of the data enable and sync signals require special extraction process (Pattern & Timing Generator) depending on the format of input video data.

All the data then undergo a series of video processing including color-space conversion and YCbCr

down-sampling. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected input-output format combination and the corresponding video processing block selection. Please refer to the IT6161 Programming Guide for suggested register setting.

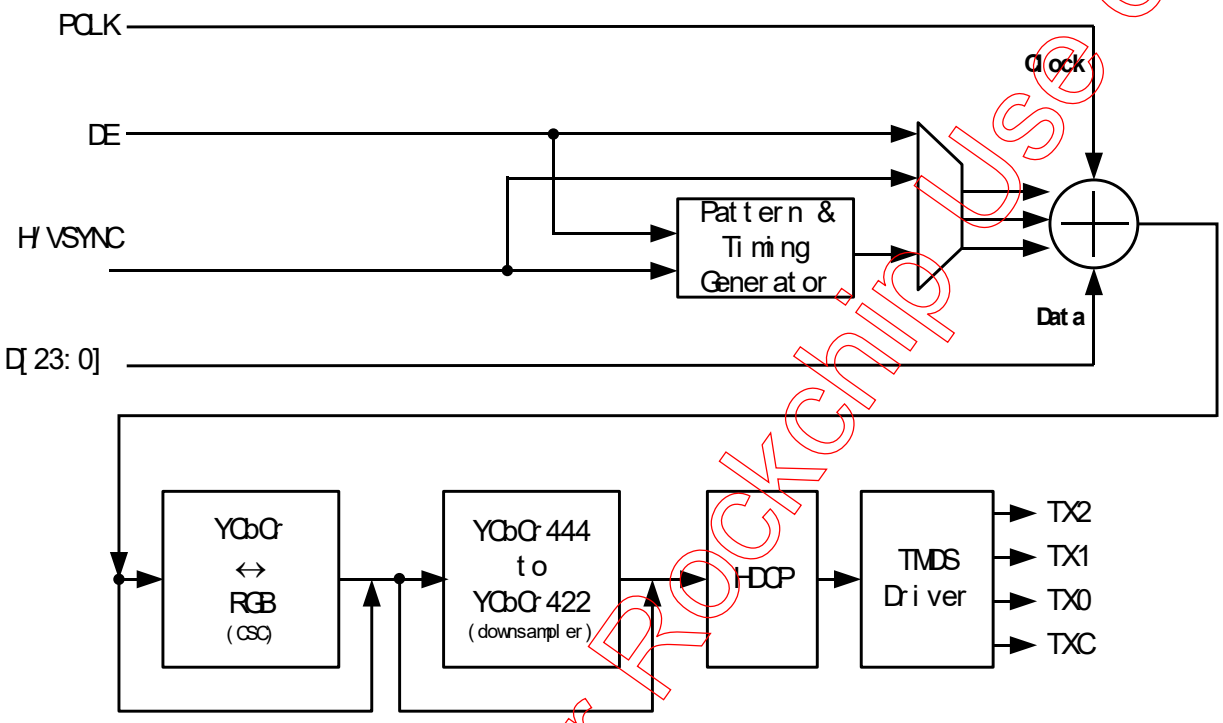


Figure 5-2. Video Data Processing Flow of IT6161

Designated as D[23:0], the input video data could take on bus width of 8 bits to 24 bits.

Although not explicitly depicted in Figure 5-2, input video clock (PCLK) can be configured to be multiplied by 1, 2 or 4, so as to support special formats such as pixel-repeating. This is also enabled by software programming.

General description of block functions is as follows:

Timing & Pattern Generator
A pattern and timing generator embedded in the IT6161 can be programmed to generate user-defined video data and timing, which are processed from TTL single pixel inputs . All the data then undergo a series of video processing including color-space conversion and YCbCr down-sampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)
Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in IT6161 are fully programmable. Users of IT6161 could elect to employ their preferred conversion formula.

Downsampling (YCbCr444 to YCbCr422)
In cases where input signals are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling.

HDCP engine (HDCP)
The HDCP engine in IT6161 handles all the processing required by HDCP mechanism in hardware. Software intervention is not necessary except checking for revocation. Preprogrammed HDCP keys are also embedded in IT6161. Users need not worry about the purchasing and management of the HDCP keys.

TMDS driver (TMDS Driver)
The final stop of the data processing flow is TMDS serializer. The TMDS driver serializes the input parallel data and drive out the proper electrical signals to the HDMI cable. The output current level is controlled through connecting a precision resistor of proper value to Pin 31 (REXT).

5.2 Supported Packed Pixel Steam

Figure 5-3. 18-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x1E

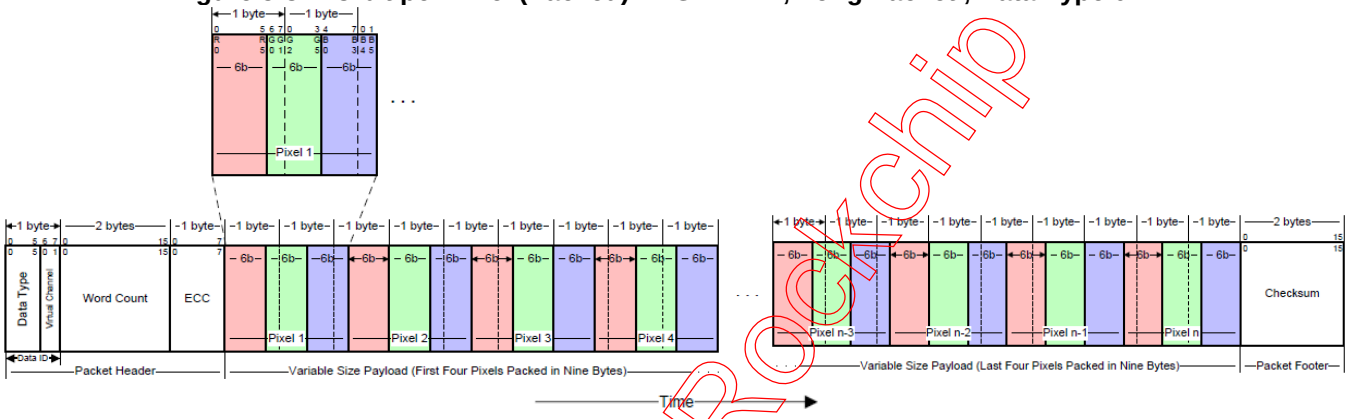


Figure 5-4. 18-bit per Pixel (Loosely) - RGB 4:4:4, Long Packet , Data Type 0x2E

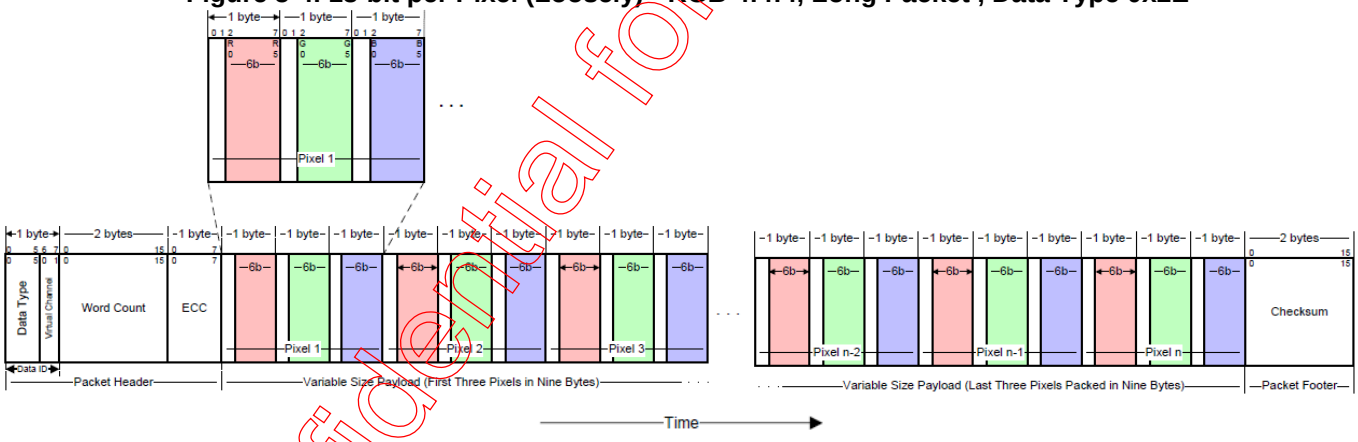
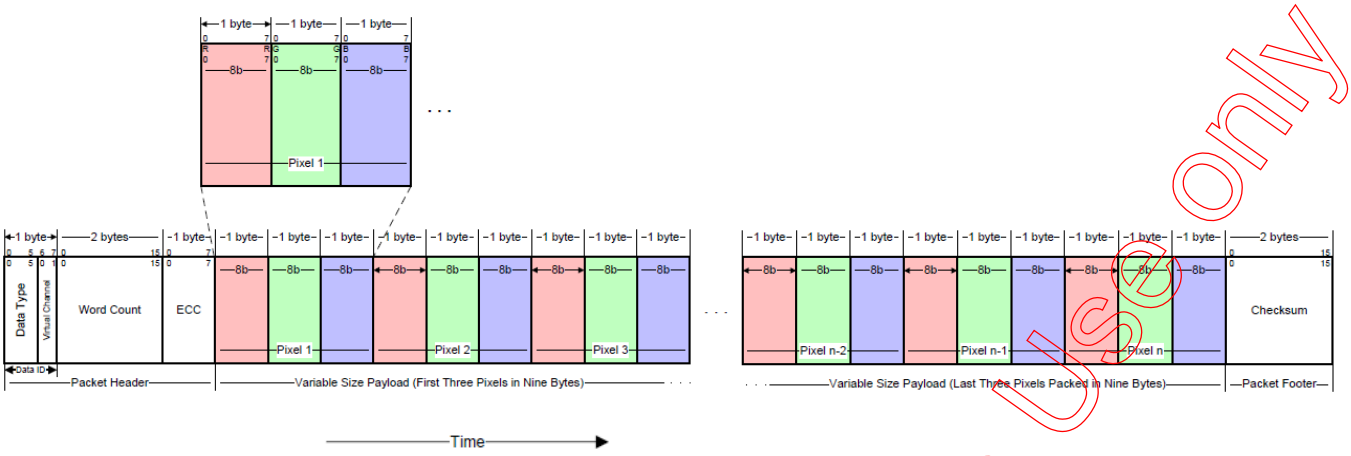


Figure 5-5. 24-bit per Pixel (Packed) - RGB 4:4:4, Long Packet , Data Type 0x3E



5.3 Audio Data Capture and Processing

The IT6161 supports various audio formats and interfaces specified by the HDMI Specification through I²S, S/PDIF and optional 8 channels one-bit audio inputs.

Note that MCLK input is necessary when the audio format is HRB through S/PDIF and is optional for other audio formats. By default IT6161 generates the MCLK internally to process the audio. Neither I²S nor S/PDIF inputs requires external MCLK signal. However, if the jitter or the duty cycle of the input S/PDIF is considerable, coherent external MCLK input is recommended and such configuration could be enabled through register setting. Refer to IT6161 Programming Guide for such setting.

I²S

Four I²S inputs are provided to support 8-channel uncompressed audio data at up to 192kHz sample rate. Not all video formats can carry multi-channel audio data at 192kHz in the blank interval. Users may set the proper pixel repeating value to increase the available bandwidth.

S/PDIF

The S/PDIF input supports 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the data stream itself via coding.

One-Bit Audio (DSD/SACD)

Direct stream digital (DSD) audio is a one-bit audio format, which is prescribed by Super Audio CD (SACD) to provide superior audio hearing experiences. The IT6161 uses multi-function input pins for DSD audio. A total of 8 data inputs are provided for right channels and left channels.

High-Bit-Rate Audio (HBR)

High-Bit-Rate Audio is first introduced in the HDMI 1.4 standard. It is called upon by high-end audio system such as DTS-HD and Dolby TrueHD. No specific interface is defined by the HBR standard. The IT6161 supports HBR audio in two ways. One is to employ the four I²S inputs simultaneously, where the original streaming HBR audio is broken into four parallel data streams before entering the IT6161. The other is to use the S/PDIF input port. The maximum frame rate supported by SPDIF interface is 768K. Since the data rate here is as high as 98.304Mbps, a coherent MCLK is required in this application.

5.4 Configuration and Function Contronl

IT6161 includes two serial programming ports by default (i.e. with embedded HDCP keys): one for interfacing with micro-controller, the other for accessing the DDC channels of HDMI link.

The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 47) and PCSDA (Pin 48). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 45). If PCADR is pulled high by the user, the device address is **0x9A**. If pulled low, **0x98**.

The I²C interface for accessing the DDC channels of the HDMI link is a master interface, comprising DDCSCL (Pin 25) and DDCSDA (Pin 24). IT6161 uses this interface to read the EDID data and perform HDCP authentication protocol with the sink device over the HDMI cable.

For temporarily storing the acquired EDID data, IT6161 includes a 32 bytes dedicated FIFO. The micro-controller may command IT6161 to acquire 32 bytes of EDID information, read it back and then continue to read the next 32 bytes until getting all necessary EDID information.

The HDCP protocol of IT6161 is completely implemented in hardware. No software intervention is needed except for revocation list checking. Various HDCP-related statuses are stored in HDCP registers for the reference of micro-controller. Refer to IT6161 Programming Guide for detailed register descriptions. The HDCP Standard also specifies a special message read protocol other than the standard I²C protocol. See Figure 5-6 for checking HDCP port link integrity.

S=Start; R=Read; A=Ack; NA=No Ack; P=Stop

Figure 5-6. HDCP port link integrity message read

All serial programming interfaces conform to standard I²C transactions and operate at up to 100kHz

5.5 Interrupt Generation

The system micro-controller should take in the interrupt signal output by IT6161 at PIN 49 (INT). INT pin can be configured as Push-pull or Tristate mode depending on user's application. IT6161 generates an interrupt signal with events involving the following signals or situations:

1. Hot-plug detection (Pin 23, HPD) experiences state changes.
2. Receiver detection circuit reports the presence or absence of an active termination at the TMDS Clock Channel (RxSENDetect)
3. DDC bus is hanged for any reasons
4. Audio FIFO overflows
5. HDCP authentication fails
6. Audio/Video data is stable or not

A typical initialization of HDMI link should be based on interrupt signal and appropriate register probing. Recommended flow is detailed in IT6161 Programming Guide. Simply put, the microcontroller should monitor the HPD status first. Upon valid HPD event, move on to check RxSENDetect register to see if the receiver chip is ready for further handshaking. When RxSENDetect is asserted, start reading EDID data through DDC channels and carry on the rest of the handshaking subsequently.

If the micro-controller makes no use of the interrupt signal as well as the above-mentioned status registers, the link establishment might fail. Please do follow the suggested initialization flow recommended in IT6161 Programming Guide.

6. Operation Supply Current Specification

- Active(Operation) Mode:
  - Normal Case (Color Bar)

Voltage	Name	Videoformat	VIC	HDCP	BUS	Audio	measurement
1.2v Total Current (mA)		480P60hz	2	1.4	8b MIPI1L	2ch192Khz	34.43
		720P60hz	4	1.4	8b MIPI4L	8ch192Khz	58.15
		1080P60hz	16	1.4	8b MIPI4L	8ch192Khz	88.46
3.3v Total Current (mA)		480P60hz	2	1.4	8b MIPI1L	2ch192Khz	3.44
		720P60hz	4	1.4	8b MIPI4L	8ch192Khz	7.23
		1080P60hz	16	1.4	8b MIPI4L	8ch192Khz	4.57
P Total (mW)		480P60hz	2	1.4	8b MIPI1L	2ch192Khz	52.67
		720P60hz	4	1.4	8b MIPI4L	8ch192Khz	93.64
		1080P60hz	16	1.4	8b MIPI4L	8ch192Khz	121.23

■ Standby Mode

Testing Configurations:

	Total 1.2V (uA)	Total 3.3V (uA)	Total Power (mW)
Standby Mode (Audio Disabled)	531.36	266.69	1.52

■ IDDQ Mode

Testing Configurations:

	Total 1.2V (uA)	Total 3.3V (uA)	Total Power (mW)
IDDQ Mode (Audio Disabled)	531.94	223.69	1.38

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
IVDD12	Core logic supply voltage	-0.5		1.5	V
OVDD33	5V-tolerant I/O pins supply voltage	-0.3		4.0	V
OVDD1833	1.8V I/O pins supply voltage (OVDD1833=1.8V)	-0.3		2.5	V
	2.5V I/O pins supply voltage (OVDD1833=2.5V)	-0.3		3.2	V
	3.3V I/O pins supply voltage (OVDD1833=3.3V)	-0.3		4.0	V
PVCC33	HDMI core PLL power	-0.3		4.0	V
PVCC12	HDMI core PLL power	-0.5		1.5	V
AVCC12	HDMI analog frontend power	-0.5		1.5	V
TDVDD12	HDMI digital frontend power	-0.5		1.5	V
NVDD12	MIPI analog frontend power	-0.5		1.5	V
RDVDD12	MIPI digital frontend power	-0.5		1.5	V
V_I	Input voltage	-0.3		I/O supply voltage + 0.3 5.5 (5V-tolerant I/O)	V
V_O	Output voltage	-0.3		I/O supply voltage + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:

1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

7.2 Functional Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
IVDD12	Core logic supply voltage	1.14	1.2	1.26	V
OVDD33	5V-tolerant I/O pins supply voltage	3.0	3.3	3.6	V
OVDD1833	1.8V I/O pins supply voltage	1.62	1.8	1.98	V
	2.5V I/O pins supply voltage	2.25	2.5	2.75	V
	3.3V I/O pins supply voltage	3.0	3.3	3.6	V
PVCC33	HDMI core PLL power	3.0	3.3	3.6	V
PVCC12	HDMI core PLL power	1.14	1.2	1.26	V
AVCC12	HDMI analog frontend power	1.14	1.2	1.26	V
TDVDD12	HDMI digital frontend power	1.14	1.2	1.26	V
NVDD12	MIPI analog frontend power	1.14	1.2	1.26	V
RDVDD12	MIPI digital frontend power	1.14	1.2	1.26	V

$V_{CCNOISE}$	Supply noise			80	mV_{pp}
T_A	Ambient temperature	-20	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance			30	°C/W

Notes:
1. PVCC33, PVCC12, AVCC12, NVDD12 should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

7.3 DC Electrical Specification

Under Functional Operation Conditions

Symbol	Parameter	Pin Type	OVDD33=3.3V			Unit
			Min.	Typ.	Max.	
V_{IL}	Input low voltage[1]	5V-TOL	GND		0.8	V
V_{IH}	Input high voltage[1]	5V-TOL	2.5		5.5	V

Symbol	Parameter	Pin Type	OVDD1833=1.8V			OVDD1833=2.5V			OVDD1833=3.3V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IL}	Input low voltage[1]	LVTTL	GND		0.6	GND		0.7	GND		0.8	V
V_{IH}	Input high voltage[1]	LVTTL	1.2			1.7			2.0			V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt	0.63	0.75		0.94	1.06		1.22	1.39		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt		1.05	1.14		1.35	1.48		1.7	1.92	V
V_{OL}	Output low voltage[1]	LVTTL			0.4			0.4			0.4	V
V_{OH}	Output high voltage[1]	LVTTL	1.4			2.1			29			V
I_{IN}	Input leakage current[1]	all	-10		+10	-10		+10	-10		+10	μA
I_{OZ}	Output leakage current[1]	all	-10		+10	-10		+10	-10		+10	μA
I_{OL}	Serial programming output sink current[2]	Schmitt							2.5		10	mA
V_{swing}	TMDS output single-ended swing[3]single-ended swing[3]	TMDS	400		600	400		600	400		600	mV

I_{OFF}	Single-ended standby output current[3]	TMDS			10			10			10	μA

Notes:

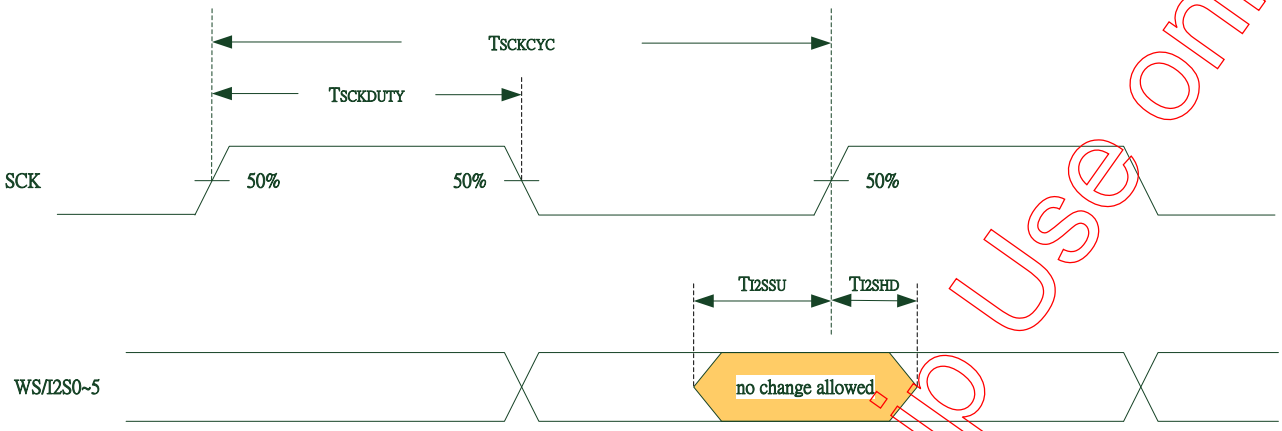
1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I²C Standard. When set at maximum current, the serial programming output ports of IT6161 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I²C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6161 Programming Guide for proper register setting.
3. Limits defined by HDMI standard

7.4 Audio AC Timing Specification

Under Functional Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{S_I2S}	I²S sample rate	Up to 8 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		768	kHz

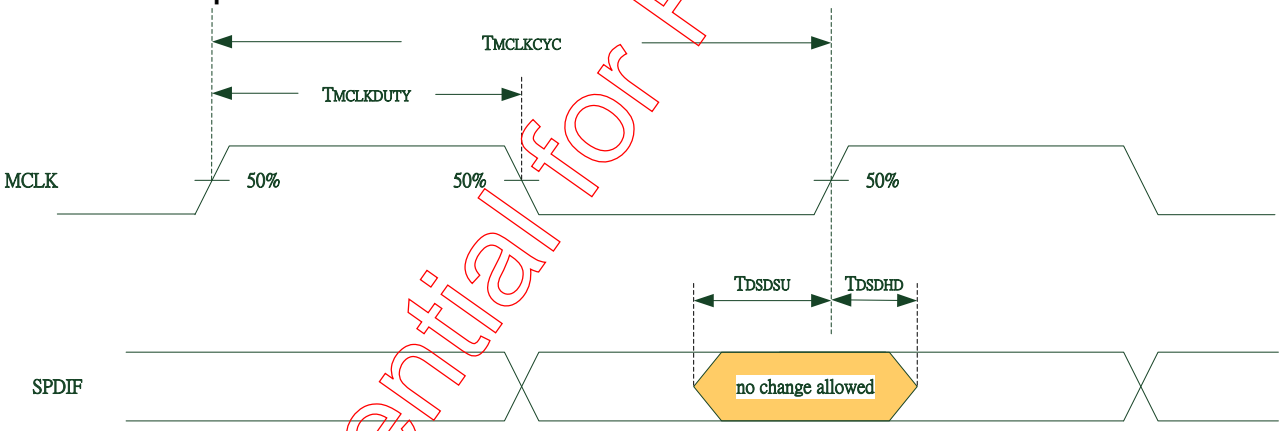
7.4.1 I2S input



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{SCKCYC}	SCK cycle time	40.69		488.28	ns
$T_{SCKDUTY}$	SCK duty cycle	45%		55%	UI
T_{I2SSU}	I2S setup time	10			ns
T_{I2SHD}	I2S hold time	5			ns

Note: SCK could be programmed to latch WS/I2S0~3 using falling edge.

7.4.2 SPDIF input with 128FS MCLK



Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{MCLKCYC}$	MCLK cycle time	10.172		244.14	ns
$T_{MCLKDUTY}$	MCLK duty cycle	45%		55%	UI
$T_{SPDIFSU}$	SPDIF setup time	5			ns
$T_{SPDIFHD}$	SPDIF hold time	3			ns

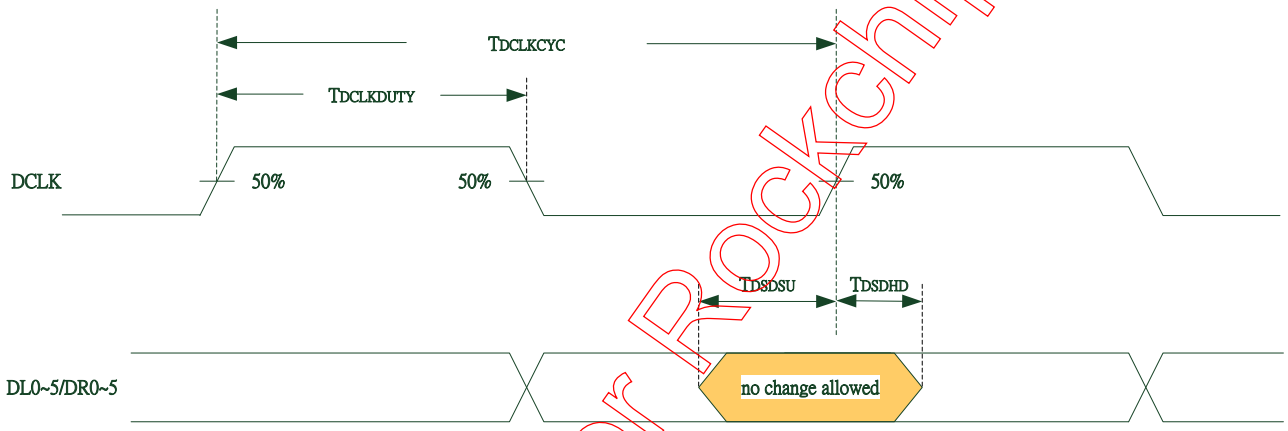
Note: MCLK could be programmed to latch SPDIF using falling edge.

7.4.3 SPDIF input without MCLK

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{SPDIFCYC}$	SPDIF cycle time	81.38		488.28	ns
$T_{SPDIFDUTY}$	SPDIF duty cycle	45%		55%	UI

Note: the SPDIF timing is based on Logic '1' bi-phase encoding

7.4.4 DSD input



Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{DCLKCYC}$	DCLK cycle time	81.38		488.28	ns
$T_{DCLKDUTY}$	DCLK duty cycle	45%		55%	UI
T_{DSDSU}	DSD setup time	10			ns
T_{DSDHD}	DSD hold time	5			ns

Note: DCLK could be programmed to latch DL0~5/DR0~5 using falling edge.

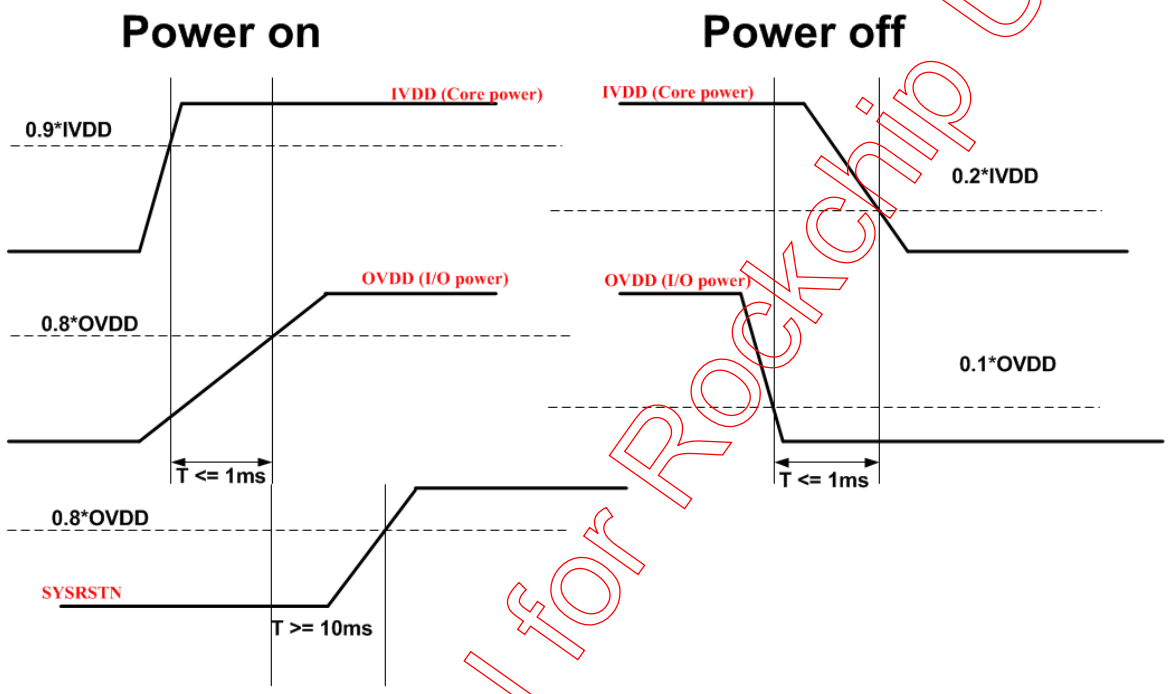
8. System Design Consideration

As a high-performance receiver/transmitter, ITE's RX/TX is capable of receiving/transmitting those signals that are attenuated and degraded by the HDMI cables. These signals are usually very small in amplitudes in addition to the distortion that the cable inflicts on them. The analog front-end of ITE's RX/TX is designed to combat environment noises as well as interference to some degree. However, to get the optimum performance, the system designers should follow the guideline below when designing the application circuits and PCB layout.

Please refer the "IT6161 HW Design Guidelines" document for detail description.

8.1 power supply sequence

The recommended power sequence for IT6161 is shown as Figure 8-1.

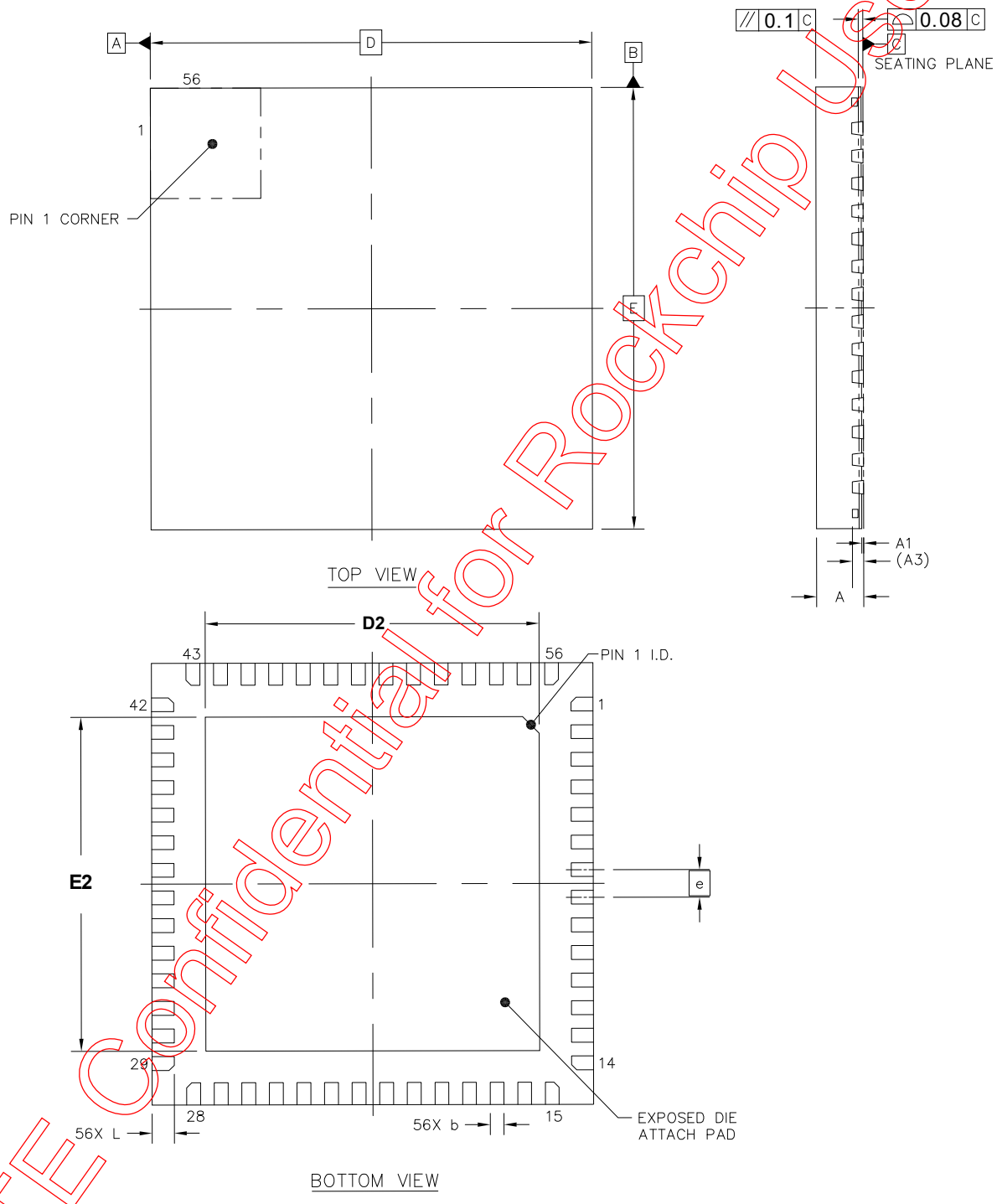


When power on, please keep IVDD go 0.9*IVDD before OVDD go 0.8*OVDD (IVDD must supply earlier than or equal to OVDD).
And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

Figure 8-1. Power Sequence

9. Package Information

QFN 56(8*8) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	--	0.002	0.00	--	0.05
A3	0.20 REF			0.203 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.311	0.315	0.319	7.90	8.00	8.10
D2	0.219	--	0.244	5.55	--	6.20
E	0.311	0.315	0.319	7.90	8.00	8.10
E2	0.219	--	0.244	5.55	--	6.20
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50

Notes:
1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-220
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

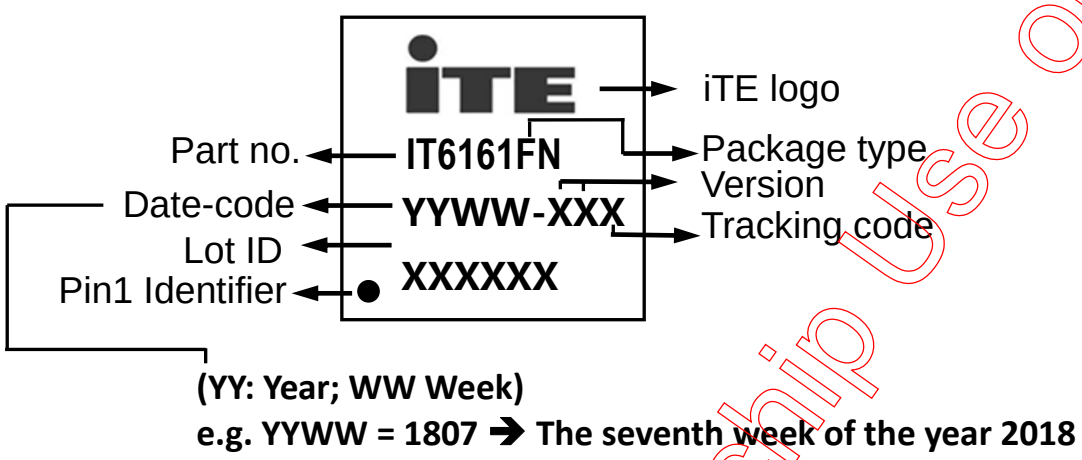
DI-SAW-QFN56 T1(8*8)v2

10. Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6161	-20~70	56-pin QFN	Green

All green components provided are in compliance with RoHS, and Halogen-Free.

11. Top Marking Information



(YY: Year; WW Week)

e.g. YYWW = 1807 ➔ The seventh week of the year 2018

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorney's fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.