IT6516BFN

Single Chip DisplayPort to VGA Converter with Embedded MCU

ITE TECH. INC.

General Description

The IT6516BFN is a high-performance single-chip DisplayPort to VGA converter. Combined with DisplayPort receiver and triple DACs, the IT6516BFN supports DisplayPort input and VGA output by conversion function. The build-in DisplayPort receiver is fully compliant with DisplayPort 1.1a specification. With 2-lane HBR (High-Bit-Rate) DisplayPort receiver, the IT6516BFN can support VESA resolution up to WUXGA and UXGA. Also the build-in triple DACs can support up to 8 bit deep colors.

The single chip IT6516BFN provides high performance, cost effective, DP2VGA conversion function, and it can help modern NB or MB to be compatible with traditional VGA only projectors, monitors, and TVs.

With embedded MCU and Flash, IT6516BFN is easy to program thru the ISP interface. Customers need no external Flash and MCU, can save the BOM cost and board size.

With embedded 3.3V to 1.8V Power Regulator, IT6516BFN can optional use single 3.3V power supply for PCB design, customers need no external power regulator to save the BOM cost and board size. And when the system provides both 1.8V and 3.3V supply, the IT6516BFN's embedded regulator can be disabled to save power consumption.

With embedded Crystal, customers need no external crystal and related application circuits to save the BOM cost and board size.

Features (DisplayPort RX)

- Compliance with DisplayPort Specification **V1.1a** at **1.62/2.7 Gbps** data rate (Low bit rate/High bit rate)
- Support flexible **1/2** lanes configurations; **5.4 Gbps** data rate support (2 lanes at 2.7Gbps)
- Support DPCD **Rev.1.1**
- Support **Spread Spectrum Clocking** up to **0.5%** down-spread to reduce EMI
- Support Source Connection Detection through AUX channel DC levels
- Automatic loss of signal detection for Link management
- Intelligent, programmable power management

- Embedded Block0 EDID RAM to saving BOM cost
- Compliance with “DP only” or “DP++” Source device

Features (VGA DACs)

- Tripe **8-Bit** DAC Converters
- **230 MSPS** Throughput Rate
- Embedded Compensated Circuits.
- Complementary Outputs
- DAC Output Current Range 2mA to 18.5mA
- VESA VSIS V1r2 Compliant

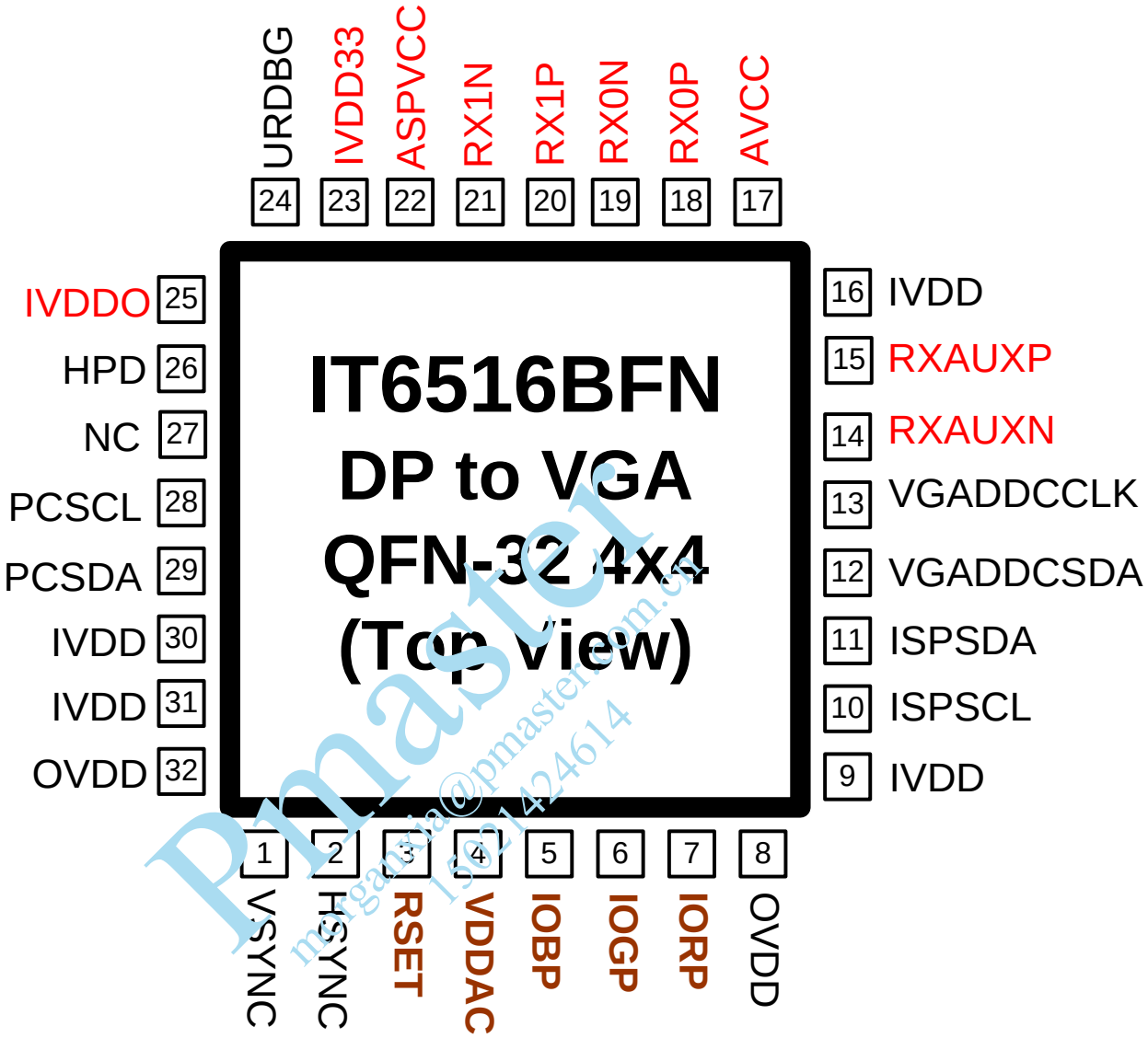
Features (Combined)

- Support up to **QXGA(2048x1536), QWXGA(2048x1280 RB), WUXGA(1920X1200 RB) and UXGA(1600x1200)** VESA display format
- Support DP Input deep color depth up to **12bit**, and support VGA output color depth to **8bit**
- Embedded MCU and Flash
- 8KV ESD Protection (Human Body Mode) on VGA pins
- Embedded 3.3V to 1.8V power regulator
- Embedded Crystal
- Active mode current consumption at 162 Mhz UXGA resolution is ~245mA.
- 32-pin QFN (4mm x 4mm) package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6516BFN/BX-0062	0~70	32-pin QFN	Green

Pin Diagram



Red: DP AFE pin
Brown: DAC AFE pin
Others: TTL pin

Figure 1. IT6516BFN Pin Diagram

Pin Description

DP Analog front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
RX0P	Analog	DP Lane 0 positive input	DP	18
RX0N	Analog	DP Lane 0 negative input	DP	19
RX1P	Analog	DP Lane 1 positive input	DP	20
RX1N	Analog	DP Lane 1 negative input	DP	21
RXAUXP	Analog	DP AUX channel positive input	DP	15
RXAUXN	Analog	DP AUX channel negative input	DP	14

VGA output interface pins

Pin Name	Direction	Description	Type	Pin No.
IORP	Analog	Red Current Output	Analog	7
IOGP	Analog	Green Current Output	Analog	6
IOBP	Analog	Blue Current Output	Analog	5
RSET	Analog	Voltage Reference Input	Analog	3
VGADDCCLK	Output	DDC/EDID clock interface to VGA (5V tolerant)	LVTTL	13
VGADDCSDA	I/O	DDC/EDID data interface to VGA (5V tolerant)	LVTTL	12

Digital Output Pins

Pin Name	Direction	Description	Type	Pin No.
HSYNC	Output	Horizontal sync. signal	LVTTL	2
VSYNC	Output	Vertical sync. signal	LVTTL	1

MCU Pins

Pin Name	Direction	Description	Type	Pin No.
ISPSDA	I/O	ISP programming data pin	LVTTL	11
ISPSCL	Input	ISP programming clock pin	LVTTL	10

System control/Programming Pins

Pin Name	Direction	Description	Type	Pin No.
URDBG	I/O	UR interface for S/W debugging	Schmitt	24

HPD	Output	DisplayPort HPD/IRQ pin	LVTTL	26
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	28
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	29
NC	I/O	Shall be left unconnected	LVTTL	27

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD33	Regulator power input (3.3V)	Power	23
IVDDO	Regulator power output (1.7V~1.8V)	Power	25
IVDD	Digital logic power (1.7V~1.8V)	Power	9, 16, 30, 31
OVDD	I/O Pin power (3.3V)	Power	8, 32
AVCC	DP analog front-end power (1.7V~1.8V)	Power	17
ASPVCC	Power for oscillator and PLL	Power	22
VDDAC	DAC/ Voltage reference circuit analog power (1.7V~1.8V)	Power	4
GND	**Exposed GND pad**	**Ground**	**33**

Block Diagram

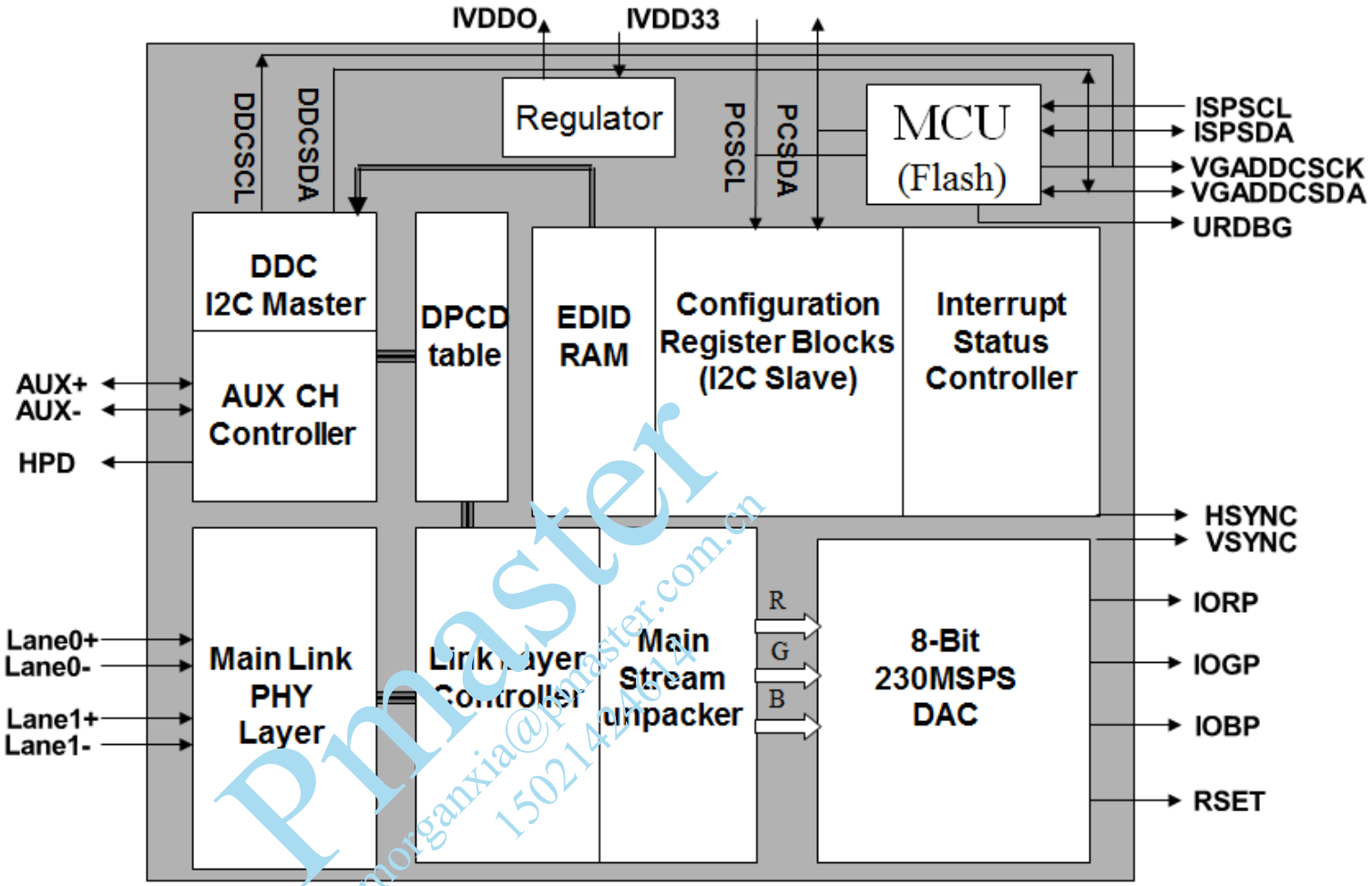


Figure 2. The IT6516BFN DP2VGA Block Diagram

Electrical Specifications

1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD33	Digital logic power 3.3V input	-0.3		4.0	V
IVDD	Digital logic power	-0.3		2.5	V
OVDD	I/O Pin power	-0.3		4.0	V
AVCC	DP analog front-end power	-0.3		2.5	V
ASPVCC	Power for crystal oscillator	-0.3		2.5	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity, **VGA pins**	**8000**			V
ESD_HB	Human body mode ESD sensitivity, others pins	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.

2. Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
VDDAC	DAC/ Voltage reference circuit analog power	1.62	1.8	2.0	V
$V_{DAC,NOISE}$	Allowable DAC power's supply noise			50	mVpp
IVDD33	Digital logic power 3.3V input	3.15	3.3	3.5	V
IVDDO	Digital logic LDO power output	1.62	1.8	2.0	V
IVDD	Digital logic power input	1.62	1.8	2.0	V
OVDD	I/O Pin power	2.97	3.3	3.63	V
AVCC	DP analog front-end power	1.62	1.8	2.0	V
ASPVCC	Power for crystal oscillator	1.62	1.8	2.0	V
$V_{CCNOISE}$	Supply noise			80	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance		32		°C/W

Notes:
1. AVCC and ASPVCC should be regulated.

3. Operation Supply Current Specification

3.1. Normal Active Mode with Internal LDO:

Symbol	Video Timing	PCLK	HBR/2Line	HBR/1Line	LBR/2Line	LBR/1Line	Unit
I_{OVDD}	640x480P60	25.2MHz	1.622	1.622	1.622	1.622	mA
	800x600P60	40.0MHz	1.622	1.622	1.622	1.622	mA
	1024x768P60	65.0MHz	1.622	1.622	1.622	-	mA
	1280x1024P60	108.0MHz	1.622	-	-	-	mA
	1080P600	148.5MHz	1.622	-	-	-	mA
	1600x1200P60	162.0MHz	1.622	-	-	-	mA
	1920x1200P60	193.2MHz	1.622	-	-	-	mA
I_{IVDD33}	640x480P60	25.2MHz	233.58	194.15	183.82	160.22	mA
	800x600P60	40.0MHz	236.47	196.03	185.67	163.23	mA
	1024x768P60	65.0MHz	239.65	200.64	188.67	-	mA
	1280x1024P60	108.0MHz	244.09	-	-	-	mA
	1080P60	148.5MHz	252.65	-	-	-	mA
	1600x1200P60	162.0MHz	271.91	-	-	-	mA
	1920x1200P60	193.2MHz	254.07	-	-	-	mA
$P_{IC-total}$	640x480P60	25.2MHz	**752.809**	**626.633**	**593.577**	**518.057**	mW
	800x600P60	40.0MHz	**762.057**	**632.649**	**599.497**	**527.689**	mW
	1024x768P60	65.0MHz	**772.233**	**647.401**	**609.097**	-	mW
	1280x1024P60	108.0MHz	**786.441**	-	-	-	mW
	1080P60	148.5MHz	**807.433**	-	-	-	mW
	1600x1200P60	162.0MHz	**811.465**	-	-	-	mW
	1920x1200P60	193.2MHz	**818.377**	-	-	-	mW

3.2. Deep Standby mode, MCU active to monitor VGA plug/unplug detection:

Symbol	Deep Standby	Unit	Item	Deep Standby	Unit
I_{Total}	2.45	mA	P_{Total}	**8.085**	mW

3.3. Normal Active Mode with External LDO:

Symbol	Video Timing	PCLK	HBR/2Line	HBR/1Line	LBR/2Line	LBR/1Line	Unit
I_{OVDD}	640x480P60	25.2MHz	1.622	1.622	1.622	1.622	mA
	800x600P60	40.0MHz	1.622	1.622	1.622	1.622	mA
	1024x768P60	65.0MHz	1.622	1.622	1.622	-	mA
	1280x1024P60	108.0MHz	1.622	-	-	-	mA
	1080P60	148.5MHz	1.622	-	-	-	mA
	1600x1200P60	162.0MHz	1.622	-	-	-	mA
	1920x1200P60	193.2MHz	1.622	-	-	-	mA
I_{IVDD}	640x480P60	25.2MHz	87.67	71.65	56.85	46.45	mA
	800x600P60	40.0MHz	89.38	73.71	58.59	49.34	mA
	1024x768P60	65.0MHz	92.95	77.18	61.72	-	mA
	1280x1024P60	108.0MHz	97.83	-	-	-	mA
	1080P60	148.5MHz	103.52	-	-	-	mA
	1600x1200P60	162.0MHz	104.48	-	-	-	mA
	1920x1200P60	193.2MHz	107.79	-	-	-	mA
I_{AVCC}	640x480P60	25.2MHz	38.06	30.48	31.91	27.47	mA
	800x600P60	40.0MHz	38.06	30.48	31.91	27.47	mA
	1024x768P60	65.0MHz	38.06	30.48	31.91	-	mA
	1280x1024P60	108.0MHz	38.06	-	-	-	mA
	1080P60	148.5MHz	38.06	-	-	-	mA
	1600x1200P60	162.0MHz	38.06	-	-	-	mA
	1920x1200P60	193.2MHz	38.06	-	-	-	mA
I_{ASPVCC}	640x480P60	25.2MHz	36.81	20.81	22.96	13.87	mA
	800x600P60	40.0MHz	36.81	20.81	22.96	13.87	mA
	1024x768P60	65.0MHz	36.81	20.81	22.96	-	mA
	1280x1024P60	108.0MHz	36.81	-	-	-	mA
	1080P60	148.5MHz	36.81	-	-	-	mA
	1600x1200P60	162.0MHz	36.81	-	-	-	mA
	1920x1200P60	193.2MHz	36.81	-	-	-	mA
I_{DAC_VDDA}	640x480P60	25.2MHz	0.29	0.29	0.29	0.29	mA
	800x600P60	40.0MHz	0.29	0.29	0.29	0.29	mA
	1024x768P60	65.0MHz	0.29	0.29	0.29	-	mA
	1280x1024P60	108.0MHz	0.29	-	-	-	mA
	1080P60	148.5MHz	0.29	-	-	-	mA
	1600x1200P60	162.0MHz	0.29	-	-	-	mA
	1920x1200P60	193.2MHz	0.29	-	-	-	mA

I_{DAC_VDDC}	640x480P60	25.2MHz	60.83	60.83	60.83	60.83	mA
	800x600P60	40.0MHz	60.83	60.83	60.83	60.83	mA
	1024x768P60	65.0MHz	60.83	60.83	60.83	-	mA
	1280x1024P60	108.0MHz	60.83	-	-	-	mA
	1080P60	148.5MHz	60.83	-	-	-	mA
	1600x1200P60	162.0MHz	60.83	-	-	-	mA
	1920x1200P60	193.2MHz	60.83	-	-	-	mA
P_{Total}	640x480P60	25.2MHz	**385.575**	**318.255**	**299.181**	**258.500**	mW
	800x600P60	40.0MHz	**388.482**	**321.757**	**302.139**	**263.413**	mW
	1024x768P60	65.0MHz	**394.551**	**327.656**	**307.460**	-	mW
	1280x1024P60	108.0MHz	**402.847**	-	-	-	mW
	1080P60	148.5MHz	**412.520**	-	-	-	mW
	1600x1200P60	162.0MHz	**414.152**	-	-	-	mW
	1920x1200P60	193.2MHz	**419.779**	-	-	-	mW

4. Display Resolution

IT6516 support the following popular resolution modes, **and the support mode also can be customized via IT6516 flexible EDID parsing algorithm.**

IT6516BFN Video Format:

Name	Active video		Total Frame		Bit Per Pixel	Vertical Frequency (Hz)	PCLK (MHz)	Data Rate (Gbits / Sec)
	Horizontal	Vertical	Horizontal	Vertical				
640x480@60Hz	640	480	800	525	24	60	25.17	0.75
640x480@60Hz	640	480	800	525	24	60	25.17	0.75
640x480@72Hz	640	480	832	520	24	72	31.50	0.94
640x480@75Hz	640	480	840	500	24	75	31.50	0.94
640x480@85Hz	640	480	832	509	24	85	36.00	1.08
720x480@60Hz	720	480	858	525	24	60	27.00	0.81
720x576@50Hz	720	576	864	625	24	50	27.00	0.81
800x600@56Hz	800	600	1024	625	24	56	36.00	1.08
800x600@60Hz	800	600	1056	628	24	60	40.00	1.20
800x600@72Hz	800	600	1040	666	24	72	50.00	1.50
800x600@75Hz	800	600	1056	625	24	75	49.50	1.48
800x600@85Hz	800	600	1048	631	24	85	56.25	1.68
832x624@75Hz	832	624	1152	667	24	75	57.28	1.71
848x480@60Hz	848	480	1088	517	24	60	33.75	1.01
1024x768@60Hz	1024	768	1344	806	24	60	65.00	1.95
1024x768@70Hz	1024	768	1328	806	24	70	75.00	2.25
1024x768@75Hz	1024	768	1312	800	24	75	78.75	2.36
1024x768@85Hz	1024	768	1376	808	24	85	94.50	2.83
1152x864@75Hz	1152	864	1600	900	24	75	108.00	3.24
1280x720@50Hz	1280	720	1980	750	24	50	74.25	2.22
1280x720@60Hz	1280	720	1650	750	24	60	74.25	2.22
1280x768@60Hz	1280	768	1440	790	24	60	68.25	2.04
1280x768@60Hz	1280	768	1664	798	24	60	79.50	2.38
1280x768@75Hz	1280	768	1696	805	24	75	102.25	3.06
1280x768@85Hz	1280	768	1712	809	24	85	117.50	3.52
1280x800@60Hz	1280	800	1440	823	24	60	71.00	2.13
1280x800@60Hz	1280	800	1680	831	24	60	83.50	2.50
1280x960@60Hz	1280	960	1800	1000	24	60	108.00	3.24
1280x960@85Hz	1280	960	1728	1011	24	85	148.50	4.45
1280x1024@60Hz	1280	1024	1688	1066	24	60	108.00	3.24
1280x1024@75Hz	1280	1024	1688	1066	24	75	135.00	4.05
1280x1024@85Hz	1280	1024	1728	1072	24	85	157.50	4.72
1360x768@60Hz	1360	768	1792	795	24	60	85.50	2.56
1366x768@60Hz	1366	768	1500	800	24	60	72.00	2.16
1366x768@60Hz	1366	768	1792	798	24	60	85.50	2.56
1400x1050@60Hz	1400	1050	1560	1080	24	60	101.00	3.03
1400x1050@60Hz	1400	1050	1864	1089	24	60	121.75	3.65
1400x1050@75Hz	1400	1050	1896	1099	24	75	156.00	4.68
1440x480@60Hz	1440	480	1716	525	24	60	54.00	1.62
1440x576@50Hz	1440	576	1728	625	24	50	54.00	1.62
1440x900@60Hz	1440	900	1600	926	24	60	88.75	2.66
1440x900@60Hz	1440	900	1904	934	24	60	106.50	3.19
1440x900@75Hz	1440	900	1936	942	24	75	136.75	4.10
1440x900@85Hz	1440	900	1952	948	24	85	157.00	4.71
1600x1200@60Hz	1600	1200	2160	1250	24	60	162.00	4.86
1680x1050@60Hz	1680	1050	1840	1080	24	60	119.00	3.57
1680x1050@60Hz	1680	1050	2240	1089	24	60	146.25	4.38
1920x1080@50(I)Hz	1920	540	2640	562	24	50	74.25	2.22
1920x1080@60(I)Hz	1920	540	2200	562	24	60	74.25	2.22
1920x1080@24Hz	1920	1080	2750	1125	24	24	74.25	2.22
1920x1080@25Hz	1920	1080	2640	1125	24	25	74.25	2.22
1920x1080@30Hz	1920	1080	2200	1125	24	30	74.25	2.22
1920x1080@50Hz	1920	1080	2640	1125	24	50	148.50	4.45
1920x1080@60Hz	1920	1080	2200	1125	24	60	148.50	4.45
1920x1200@60Hz(RB)	1920	1200	2080	1235	24	60	154.00	4.62
1920x1200@60Hz	1920	1200	2592	1245	18	60	193.25	4.35
1920x1440@60Hz(RB)	1920	1440	2080	1480	18	60	184.75	4.87
2048x1152@50Hz	2048	1152	2720	1188	24	50	161.5	4.84

2048x1152@60Hz(RB)	2048	1152	2250	1185	24	60	156.75	4.71
2048x1280@60Hz(RB)	2048	1280	2208	1317	24	60	174.25	5.22
2048x1536@50Hz	2048	1536	2144	1555	24	50	164.25	4.92

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		µA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		µA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
V_{AUX_diff}	AUX Channel differential swing[3]	Differential		0.32		1.38	V
V_{Rx_diff}	Main Link differential swing[3]	Differential		40			mV

Notes:

1. Guaranteed by I/O design
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real I^2C environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6516 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6516 Programming Guide for proper register setting.
3. Limits defined by DisplayPort 1.1a standard

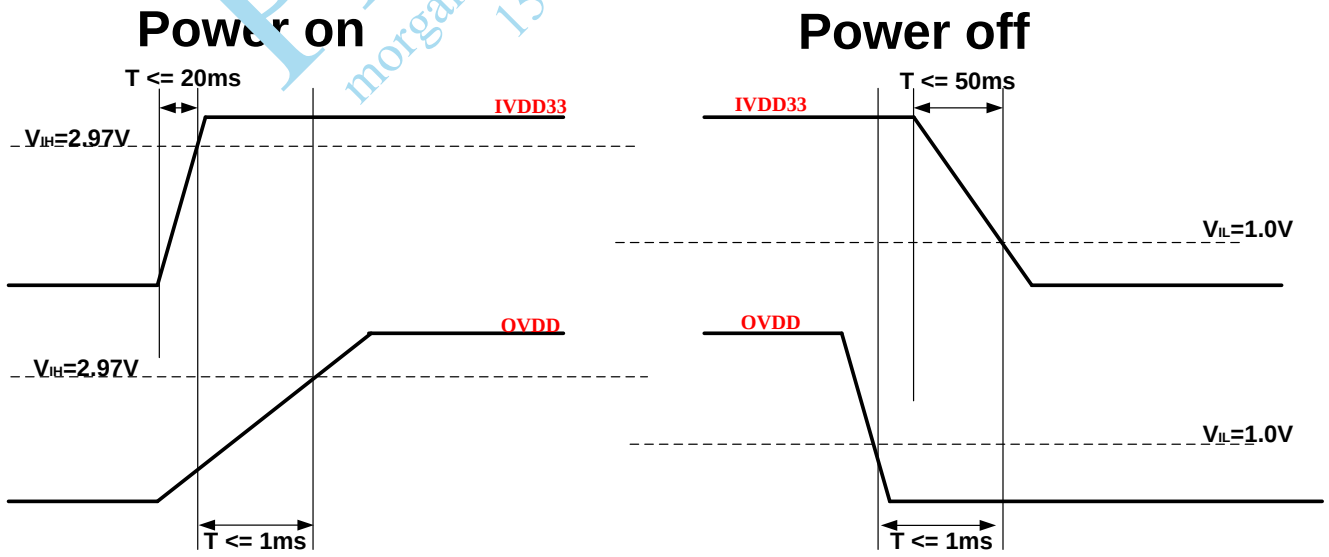
DAC Specification

(VDDAC=1.8V±5%, R_{SET}=200Ω, R_L=37.5Ω. All specification are T_A=25°C, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
MAX Luminance Voltage	0.665	0.7	0.77	Volts	Input Data=(3FFh)
MIN Luminance Voltage		0		Volts	Input Data=(000h)
Resolution (Each DAC)			8	Bits	
Offset Error		0	0	LSB	
Gain Error		0		LSB	
Integral Linearity Error	-1		+1	LSB	

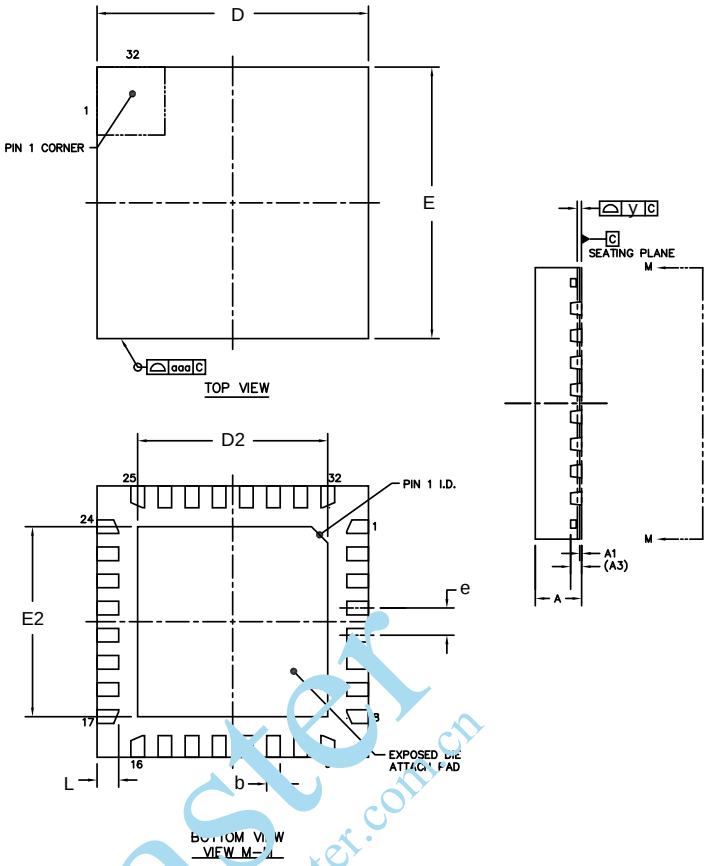
Differential Linearity Error	-1		+1	LSB	
Monotonic		Yes			
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			Volts	
Input Low Voltage, V_{IL}		0.8		Volts	
ANALOG OUTPUTS					
Output Current	2		18.5	mA	R_{SET}=2kΩ ~ 200Ω
Video Channel to Video Channel Mismatch		2	6	%	% of Max Luminance Voltage
Video Channel to Video Channel Output Skew		1		ns	
Video Noise Injection Ratio	-2.5	1	2.5	%	% of Max Luminance Voltage
Overshoot/Undershoot	-12	1	12	%	
Video Channel Rise/Fall Time		0.7	3	ns	
Maximum Settling Time After Overshoot/Undershoot		1	3	ns	
POWER DISSIPATION					
RGB Channels Supply Current	0.5	64.5		mA	Min. current is measured in power-down mode.
Voltage Reference Supply Current	50	280		uA	
Digital Supply Current	0.3	3.8		mA	

Power Sequence for Power on and Power off.



When power on, please keep IVDD33 go VIH before OVDD go VIH. And please keep the time interval between IVDD33 and OVDD shorter than 1ms when power on or power off.

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	-	0.002	0.00	-	0.05
A3		0.008 REF			0.203 REF	
b	0.006	0.008	0.01	0.15	0.20	0.25
D		0.157 BSC			4.00 BSC	
D2	0.102	0.106	0.110	2.60	2.70	2.80
E		0.157 BSC			4.00BSC	
E2	0.102	0.106	0.110	2.60	2.70	2.80
e		0.016 BSC			0.40 BSC	
L	0.010	0.012	0.014	0.25	0.30	0.35
y	-	-	0.003	-	-	0.08

Notes:

1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-248
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

Figure 3. 32-pin QFN Package Dimensions

Top Marking Information