Rockchip
RK3568
Technical Reference Manual

Revision 1.1
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Revision History

Date	Revision	Description
2021-3-1	1.1	Add VOP infomration
2021-01-11	1.0	Initial Release

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Chapter 1 DMC (Dynamic Memory Interface)

1.1 Overview

The DMC includes DDR enhanced memory controller(UMCTL2) and DDRPHY which are a complete memory interface solution for DDR memory subsystems.

The UMCTL2 SoC application bus interface supports AXI interface, with flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.

The DDR PHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, write leveling training and programmable configuration controls.

The DMC supports the following features:

- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4
- Support up to 4 ranks and up to 8GB capacity
- Support 32-bit, 16-bit DDR data bus width
- Support up to 16-type address mapping
- Support up to 32-bank (including bank group)
- Support DDR burst8 for DDR3/DDR3L/DDR4/LPDDR3 and burst16 for LPDDR4
- Support different CL/WL latency
- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SW frequency change
- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 HW frequency change
- Support auto gated clock through DDRC and AXI low power interface
- Support auto put DDR PHYentry or exit self-refresh by DFI lower power interface
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep power-down/max power saving mode
- Support SW or PMU auto control DDR PHY entry or exit retention/self-refresh
- Support open, close, intelligent precharge paging policy
- Support advance refresh control
- Support APB interface for UMCTL2 and PHY software-accessible registers
- Support automatic RX DQS gate training and automatic write leveling training
- Support DDR monitor for debug:
  - AMBA 32-bit APB slave interface
  - Support to monitor DDR read or write address
  - Support to observe whether DDR access address within a specified range
  - Support to do the statistics about DDR read number, write number and active number
    - Hardware mode
    - Software mode
  - Support monitor interrupt

1.2 Block Diagram

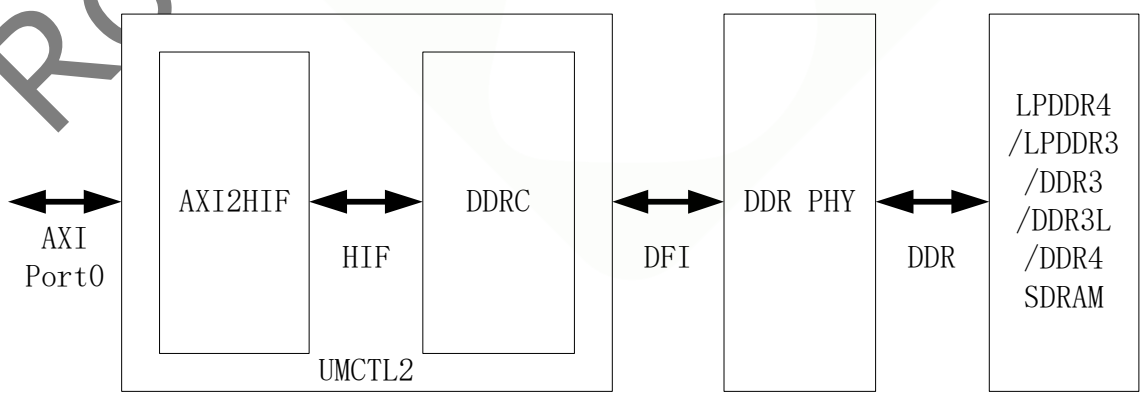


Fig.1-1 DMC Block Diagram

1.3 Function Description

1.3.1 UMCTL2

UMCTL2 supports only one AXI Port0, it receives AXI transactions from memory schedule of interconnect. These transactions are queued internally and scheduled for access in order to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn issues commands on the DFI interface to the DDR PHY block which launches and captures data to and from the SDRAM. UMCTL2 contains the following main components:

- AXI2HIF block: This block provides the AXI interface to system level and HIF interface to DDRC block. It provides bus protocol handing, data buffering, data bus size conversion and memory burst alignment. Read is stored in a SRAM, read re-order buffer and return in order to the AXI Port.
- DDRC block: This block issues the read/write commands in order, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned in order on the HIF.

1.3.2 DDR PHY

DDR PHY supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM and provides turnkey physical interface solutions for ICs requiring access to JEDEC compatible SDRAM devices.It is optimized for low power and high speed (up to 1866Mbps for DDR3/DDR3L/LPDDR3 and up to2133Mbps for DDR4/LPDDR4) applications with robust timing and small silicon area in14nm process. It supports all JEDEC DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM components in themarket. The PHY components contain DDR specialized functional and utility SSTL I/Osup to 2133MHz in SMIC 14nm, critical timing synchronization module (TSM) and a low power/jitterDLLs with programmable fine-grain control for any SDRAM interface.

1.3.3 DDR Monitor

The DDR Monitor Module has three functions, the first function is used when debug, it will monitor the DDR read or write address. The second function is also used when debug, it will observe whether DDR access address within a specified range. The third function is used to do the statistics about DDR bandwidth and utilization.

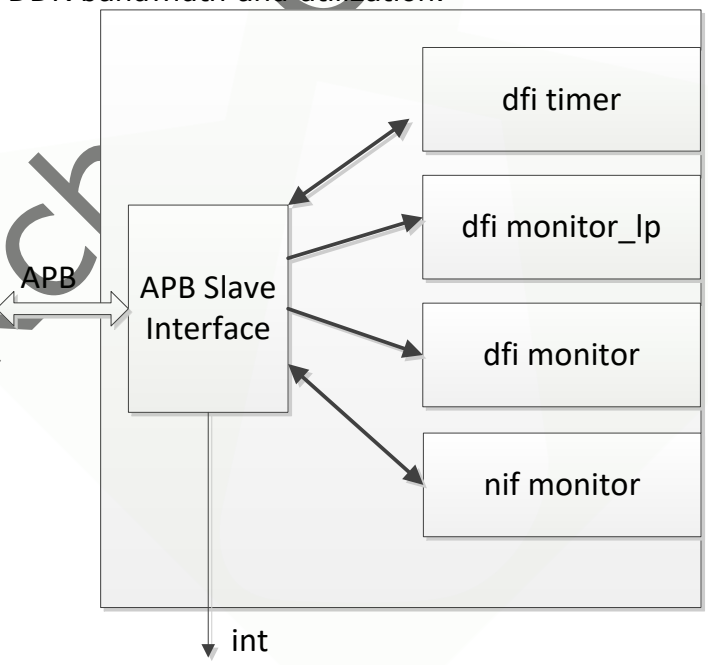


Fig.1-2 DDR Monitor Block Diagram

The host processor gets access to DDR Monitor Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt.
DDR Monitor does the monitor and statistics by dfi monitor module, nif monitor module and dfi monitor_lp module.

1.3.4 HWFFC BLOCK

To support hardware fast frequency protocol, a hardware block which is name HWFFC is

implemented in RK3368. The HWFFC is fully compatible with DDRC low-power interface which is send HWFFC request through.

During the HWFFC, a timing procedure is request as follows:
1. The system requests frequency change by de-asserting csysreq_ddrc. csysmode_ddrc = 1, csysfrequency_ddrc and csysdiscamdrain_ddrc must remain at constant values while csysreq_ddrc
= 0. csysreq_ddrc must be held de-asserted until csysack_ddrc is de-asserted.
2. The DDRC issues SRE to put SDRAMs into self-refresh (without power down), and then sends several MRW commands to update timing parameters for opposite side of current FSP, and lastly it switches FSP-OP to the opposite side.
3. The DDRC de-asserts dfi_cke to put SDRAMs into SR-Powerdown.
4. The DDRC requests frequency change to the PHY by asserting dfi_init_start dfi_frequency is set to the frequency value indicated by csysfrequency_ddrc (and holds it during dfi_init_start = 1).
5. The PHY responds to the frequency change request by de-asserting dfi_init_complete.
6. The DDRC de-asserts cactive_ddrc and then de-asserts csysack_ddrc (Frequency change request is accepted).
7. The system changes clock frequency.
8. The system asserts csysreq_ddrc (stable clock is required here).
9. The DDRC de-asserts dfi_init_start.
10. The PHY acknowledges dfi_init_start by asserting dfi_init_complete.
11. The DDRC asserts cactive_ddrc.
12. The DDRC asserts dfi_cke to exit SR-Powerdown, and sends an MRW command to program MR13.VRCG = 0 if required.
13. The DDRC asserts csysack_ddrc. cactive_ddrc starts to behave again as described in other
sections.
14. The DDRC issues SRX to exit self-refresh.
And all csys*_ddrc signals is controlled by HWFFC during frequency change and clock frequency can be controlled by HWFFC block or under software control.

1.4 Register Description

Slave address can be divided into different length for different usage, which is shown as follows.

1.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDRC_MSTR	0x0000	W	0x03040001	Master Register 0
DDRC_STAT	0x0004	W	0x00000000	Operating Mode Status Register
DDRC_MRCTRL0	0x0010	W	0x00000000	Mode Register Read/Write Control Register 0
DDRC_MRCTRL1	0x0014	W	0x00000000	Mode Register Read/Write Control Register 1
DDRC_MRSTAT	0x0018	W	0x00000000	Mode Retgister Read/Write Status Register
DDRC_MRCTRL2	0x001c	W	0x00000000	Mode Register Read/Write Control Register 2
DDRC_DERATEEN	0x0020	W	0x00000000	Temperature Derate Enable Register

Name	Offset	Size	Reset Value	Description
DDRC_DERATEINT	0x0024	W	0x00800000	Temperature Derate Interval Registesr
DDRC_PWRCTL	0x0030	W	0x00000000	Lower Power Control Register
DDRC_PWRTMG	0x0034	W	0x00402010	Lower Power Timing Register
DDRC_HWLUMCTL2	0x0038	W	0x00000003	Hardware Lower Power Control Register
DDRC_HWFFCCTL	0x003c	W	0x00000010	Hardware Fast Frequency Change Control Register
DDRC_HWFFCSTAT	0x0040	W	0x00000000	Hardware Fast Frequency Change Status Register
DDRC_RFSHCTL0	0x0050	W	0x00210000	Refresh Control Register
DDRC_RFSHCTL1	0x0054	W	0x00000000	Refresh Control Register 1
DDRC_RFSHCTL3	0x0060	W	0x00000000	Refresh Control Register 3
DDRC_RFSHTMG	0x0064	W	0x0062008c	Refresh Timing Register
DDRC_CRCPARCTL0	0x00c0	W	0x00000000	CRC Parity Control Register 0
DDRC_CRCPARCTL1	0x00c4	W	0x00001000	CRC Parity Control Register 1
DDRC_CRCPARSTAT	0x00cc	W	0x00000000	CRC Parity Status Register
DDRC_INIT0	0x00d0	W	0x0002004e	SDRAM Initilization Register 0
DDRC_INIT1	0x00d4	W	0x00000000	SDRAM Initialization Register 1
DDRC_INIT2	0x00d8	W	0x00000d05	SDRAM Initialization Register 2
DDRC_INIT3	0x00dc	W	0x00000510	SDRAM Initialization Register 3
DDRC_INIT4	0x00e0	W	0x00000000	SDRAM Initialization Register 4
DDRC_INIT5	0x00e4	W	0x00100004	SDRAM Initialization Register 5
DDRC_INIT6	0x00e8	W	0x00000000	SDRAM Initialization Register 6
DDRC_INIT7	0x00ec	W	0x00000000	SDRAM Initialization Register 7
DDRC_DIMMCTL	0x00f0	W	0x00000000	DIMM Control Register
DDRC_RANKCTL	0x00f4	W	0x0000066f	Rank Control Register
DDRC_DRAMTMG0	0x0100	W	0x0f101b0f	SDRAM Timing Register 0
DDRC_DRAMTMG1	0x0104	W	0x00080414	SDRAM Timing Register 1
DDRC_DRAMTMG2	0x0108	W	0x0305060d	SDRAM Timing Register 2
DDRC_DRAMTMG3	0x010c	W	0x0050400c	SDRAM Timing Register 3
DDRC_DRAMTMG4	0x0110	W	0x05040405	SDRAM Timing Register 4
DDRC_DRAMTMG5	0x0114	W	0x05050403	SDRAM Timing Register 5
DDRC_DRAMTMG6	0x0118	W	0x02020005	SDRAM Timing Register 6
DDRC_DRAMTMG7	0x011c	W	0x00000202	SDRAM Timing Register 7
DDRC_DRAMTMG8	0x0120	W	0x03034405	SDRAM Timing Register 8
DDRC_DRAMTMG9	0x0124	W	0x0004040d	SDRAM Timing Register 9
DDRC_DRAMTMG10	0x0128	W	0x001c180a	SDRAM Timing Register 10
DDRC_DRAMTMG11	0x012c	W	0x440c021c	SDRAM Timing Register 11
DDRC_DRAMTMG12	0x0130	W	0x00020010	SDRAM Timing Register 12
DDRC_DRAMTMG13	0x0134	W	0x1c200004	SDRAM Timing Register 13
DDRC_DRAMTMG14	0x0138	W	0x000000a0	SDRAM Timing Register 14
DDRC_DRAMTMG15	0x013c	W	0x00000000	SDRAM Timing Register 15
DDRC_DRAMTMG17	0x0144	W	0x00000000	SDRAM Timing Register 17
DDRC_ZQCTL0	0x0180	W	0x02000040	ZQ Control Register 0
DDRC_ZQCTL1	0x0184	W	0x02000100	ZQ Control Register 1
DDRC_ZQCTL2	0x0188	W	0x00000000	ZQ Control Register 2
DDRC_ZQSTAT	0x018c	W	0x00000000	ZQ Status Register
DDRC_DFITMG0	0x0190	W	0x07020002	DFI Timing Register 0
DDRC_DFITMG1	0x0194	W	0x00000404	DFI Timing Register 1
DDRC_DFILPCFG0	0x0198	W	0x07000000	DFI Lower Power Configuration Register 0

Name	Offset	Size	Reset Value	Description
DDRC_DFILPCFG1	0x019c	W	0x00000000	DFI Lower Power Configuration Register 1
DDRC_DFIUPD0	0x01a0	W	0x00400003	DFI Update Register 0
DDRC_DFIUPD1	0x01a4	W	0x00000001	DFI Update Register 1
DDRC_DFIUPD2	0x01a8	W	0x00000001	DFI Update Register 2
DDRC_DFIMISC	0x01b0	W	0x00000001	DFI Miscellaneous Control Register
DDRC_DFITMG2	0x01b4	W	0x00000202	DFI Timing Register 2
DDRC_DFITMG3	0x01b8	W	0x00000000	DFI Timing Register 3
DDRC_DFISTAT	0x01bc	W	0x00000000	DFI Status Register
DDRC_DBICTL	0x01c0	W	0x00000001	DM/DBI Control Register
DDRC_DFIPHYMSTR	0x01c4	W	0x00000001	DFI PHY Master
DDRC_ADDRMAP0	0x0200	W	0x00000000	Address Map Register 0
DDRC_ADDRMAP1	0x0204	W	0x00000000	Address Map Register 1
DDRC_ADDRMAP2	0x0208	W	0x00000000	Address Map Register 2
DDRC_ADDRMAP3	0x020c	W	0x00000000	Address Map Register 3
DDRC_ADDRMAP4	0x0210	W	0x00000000	Address Map Register 4
DDRC_ADDRMAP5	0x0214	W	0x00000000	Address Map Register 5
DDRC_ADDRMAP6	0x0218	W	0x00000000	Address Map Register 6
DDRC_ADDRMAP7	0x021c	W	0x00000000	Address Map Register 7
DDRC_ADDRMAP8	0x0220	W	0x00000000	Address Map Register 8
DDRC_ADDRMAP9	0x0224	W	0x00000000	Address Map Register 9
DDRC_ADDRMAP10	0x0228	W	0x00000000	Address Map Register 10
DDRC_ADDRMAP11	0x022c	W	0x00000000	Address Map Register 11
DDRC_ODTCFG	0x0240	W	0x04000400	ODT Configuration Register
DDRC_ODTMAP	0x0244	W	0x00002211	ODT/Rank Map Register
DDRC_SCHED	0x0250	W	0x00000804	Scheduler Control Register
DDRC_SCHED1	0x0254	W	0x00000000	Scheduler Control Register 1
DDRC_PERFLPR1	0x0264	W	0x0f00007f	Low Priority Read CAM Register 1
DDRC_PERFWR1	0x026c	W	0x0f00007f	Write CAM Register 1
DDRC_DBG0	0x0300	W	0x00000000	Debug Register 0
DDRC_DBG1	0x0304	W	0x00000000	Debug Register 1
DDRC_DBGCAM	0x0308	W	0x00000000	CAM Debug Register
DDRC_DBGCMD	0x030c	W	0x00000000	Command Debug Register
DDRC_DBGSTAT	0x0310	W	0x00000000	Status Debug Register
DDRC_SWCTL	0x0320	W	0x00000001	Software Register Programming Control Enable
DDRC_SWSTAT	0x0324	W	0x00000001	Software Register Programming Control Status
DDRC_POISONCFG	0x036c	W	0x00110011	AXI Poison Configuration Register
DDRC_POISONSTAT	0x0370	W	0x00000000	AXI Poison Status Register
DDRC_PSTAT	0x03fc	W	0x00000000	Port Status Register
DDRC_PCCFG	0x0400	W	0x00000000	Port Common Configuration Register
DDRC_PCFGR_0	0x0404	W	0x00000000	Port 0 Configuration Read Register
DDRC_PCFGW_0	0x0408	W	0x00004000	Port 0 Configuration Write Register
DDRC_PCTRL_0	0x0490	W	0x00000000	Port 0 Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Name	Offset	Size	Reset Value	Description
DDRPHY_REG0	0x0000	W	0x00000087	REG0
DDRPHY_REG1	0x0004	W	0x00000E00	REG1
DDRPHY_REG2	0x0008	W	0x00000000	REG2
DDRPHY_REG3	0x000C	W	0x00000000	REG3
DDRPHY_REG4	0x0010	W	0x00000000	REG4
DDRPHY_REG5	0x0014	W	0x00000000	REG5
DDRPHY_REG6	0x0018	W	0xFFFFFFFF	REG6
DDRPHY_REG7	0x001C	W	0x00C20023	REG7
DDRPHY_REG8	0x0020	W	0x0000E000	REG8
DDRPHY_REG9	0x0024	W	0x08F205FC	REG9
DDRPHY_REG10	0x0028	W	0x00280F1F	REG10
DDRPHY_REGA	0x002C	W	0x00000000	REGA
DDRPHY_REGB	0x0030	W	0x00000000	REGB
DDRPHY_REGC	0x0034	W	0x3F000000	REGC
DDRPHY_REGD	0x0038	W	0x88881140	REGD
DDRPHY_REGE	0x003C	W	0x00FF1506	REGE
DDRPHY_REGF	0x0040	W	0x06061515	REGF
DDRPHY_REG10	0x0044	W	0x00000000	REG10
DDRPHY_REG11	0x0048	W	0x0000003F	REG11
DDRPHY_REG12	0x004C	W	0x00401000	REG12
DDRPHY_REG13	0x0050	W	0x00000401	REG13
DDRPHY_REG14	0x0054	W	0x00010203	REG14
DDRPHY_REG15	0x0058	W	0x04000607	REG15
DDRPHY_REG16	0x005C	W	0x08090A0B	REG16
DDRPHY_REG17	0x0060	W	0x0C0D0E0F	REG17
DDRPHY_REG18	0x0064	W	0x10111213	REG18
DDRPHY_REG19	0x0068	W	0x14151617	REG19
DDRPHY_REG1A	0x006C	W	0x18000000	REG1A
DDRPHY_REG1D	0x0078	W	0x00008101	REG1D
DDRPHY_REG1E	0x007C	W	0x00000000	REG1E
DDRPHY_REG1F	0x0080	W	0x00000003	REG1F
DDRPHY_REG20	0x0084	W	0x0007597F	REG20
DDRPHY_REG21	0x0088	W	0x00161388	REG21
DDRPHY_REG22	0x008C	W	0x1FF0FC08	REG22
DDRPHY_REG23	0x0090	W	0x0E0E0707	REG23
DDRPHY_REG24	0x0094	W	0x00000000	REG24
DDRPHY_REG25	0x0098	W	0x55555A3C	REG25
DDRPHY_REG26	0x009C	W	0x00000000	REG26
DDRPHY_REG27	0x00A0	W	0x01000000	REG27
DDRPHY_REG28	0x00A4	W	0x00000001	REG28
DDRPHY_REG29	0x00A8	W	0x25808C80	REG29
DDRPHY_REG2A	0x00AC	W	0x00000000	REG2A
DDRPHY_REG2B	0x00B0	W	0x00005555	REG2B
DDRPHY_REG2C	0x00B4	W	0x00005555	REG2C
DDRPHY_REG2D	0x00B8	W	0x00005555	REG2D
DDRPHY_REG2E	0x00BC	W	0x00005555	REG2E
DDRPHY_REG2F	0x00C0	W	0x1800607E	REG2F
DDRPHY_REG31	0x00C8	W	0x641F1F1F	REG31
DDRPHY_REG32	0x00CC	W	0x0000005F	REG32
DDRPHY_REG33	0x00D0	W	0x00000000	REG33
DDRPHY_REG34	0x00D4	W	0x00000008	REG34
DDRPHY_REG36	0x00DC	W	0x00000080	REG36

Name	Offset	Size	Reset Value	Description
DDRPHY_REG37	0x00F0	W	0x00002000	REG37
DDRPHY_REG38	0x00F4	W	0x00000E0E	REG38
DDRPHY_REG3B	0x0104	W	0x00008080	REG3B
DDRPHY_REG3C	0x0108	W	0x00008080	REG3C
DDRPHY_REG3D	0x010C	W	0x00008080	REG3D
DDRPHY_REG3E	0x0110	W	0x00008080	REG3E
DDRPHY_REG3F	0x0114	W	0x00008080	REG3F
DDRPHY_REG40	0x0118	W	0x00005080	REG40
DDRPHY_REG41	0x011C	W	0x00005080	REG41
DDRPHY_REG42	0x0120	W	0x00005080	REG42
DDRPHY_REG54	0x0150	W	0x00A5C33C	REG54
DDRPHY_REG55	0x0154	W	0xFF5500AA	REG55
DDRPHY_REG56	0x0158	W	0x0000F00F	REG56
DDRPHY_REG57	0x015C	W	0x00A5C33C	REG57
DDRPHY_REG58	0x0160	W	0xFF5500AA	REG58
DDRPHY_REG59	0x0164	W	0x0000F00F	REG56
DDRPHY_REG6C	0x01B0	W	0x14285140	REG6C
DDRPHY_REG6E	0x01B8	W	0x0000003F	REG6E
DDRPHY_REG7C	0x01F0	W	0x00000000	REG7C
DDRPHY_REG7D	0x01F4	W	0x00000000	REG7D
DDRPHY_REG7E	0x01F8	W	0x00000000	REG7E
DDRPHY_REG7F	0x01FC	W	0x00000000	REG7F
DDRPHY_REG83	0x020C	W	0x00000000	REG83
DDRPHY_REG84	0x0210	W	0x00000000	REG84
DDRPHY_REG85	0x0214	W	0x00000000	REG85
DDRPHY_REGAD	0x02B4	W	0x00000000	REGAD

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

1.4.2 Detail Register Description

DDRC_MSTR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	device_config Configuration of device used 2'b00: x4 device 2'b01: x8 device 2'b10: x16 device 2'b11: x32 device Programming Mode: Static
29	RW	0x0	frequency_mode Choose wich register are used. 1'b0: Original registers 1'b1: FREQ1 registers Programming Mode: Quasi-dynamic Group 2
28:26	RO	0x0	reserved
25:24	RW	0x3	active_ranks 2'b01: One Rank 2'b11: Two Ranks Others: Reserved Programming Mode: Static
23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22	RW	0x0	frequency_ratio selects the frequency ratio 1'b0: 1:2 mode 1'b1: 1:1 mode Programming Mode: Static
21:20	RW	0x0	active_logical_ranks Number of logical ranks for DDR4 3DS 2'b00: Monolithic (no stack) 2'b01: 2H stack 2'b10: 4H stack 2'b11: 8H stack Programming Mode: Static
19:16	RW	0x4	burst_rdwr SDRAM burst length used: 4'b0001: Burst length of 2 4'b0010: Burst length of 4 4'b0100: Burst length of 8 4'b1000: Burst length of 16 Programming Mode: Static
15	RW	0x0	dll_off_mode 1'b1: Dll-off mode for lower frequency operation 1'b0: Dll-on mode for normal frequency operation Programming Mode: Quasi-dynamic Group 2
14	RO	0x0	reserved
13:12	RW	0x0	data_bus_width 2'b00: Full DQ bus width to SDRAM 2'b01: Half DQ bus width to SDRAM Others: Reserved Programming Mode: Static
11	RW	0x0	geardown_mode 1'b1: Enable geardow mode 1'b0: Normal mode Programming Mode: Quasi-dynamic Group 2
10	RW	0x0	en_2t_timing_mode 1'b1: Use 2T timing 1'b0: Use 1T timing Programming Mode: Static
9	RW	0x0	burstchop 1'b1: Enable burst-chop 1'b0: Disable burst-chop Programming Mode: Static
8	RW	0x0	burst_mode 1'b0: Sequential burst mode 1'b1: Interleaved burst mode Programming Mode: Static
7:6	RO	0x0	reserved
5	RW	0x0	lpddr4 1'b1: LPDDR4 1'b0: Non-LPDDR4 Programming Mode: Static
4	RW	0x0	ddr4 1'b1: DDR4 1'b0: Non-DDR4 Programming Mode: Static

Bit	Attr	Reset Value	Description
3	RW	0x0	lpddr3 1'b1: LPDDR3 1'b0: Non-LPDDR3 Programming Mode: Static
2	RW	0x0	lpddr2 1'b1: LPDDR2 1'b0: Non-LPDDR2 Programming Mode: Static
1	RW	0x0	mobile 1'b1: Mobile/LPDDR 1'b0: Non-Mobile Programming Mode: Static
0	RW	0x1	ddr3 1'b1: DDR3 1'b0: Non-DDR3 Programming Mode: Static

DDRC_STAT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	selfref_cam_not_empty Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh. Programming Mode: Dynamic
11:10	RO	0x0	reserved
9:8	RO	0x0	selfref_state Self refresh state. This indicates self refresh or self refresh power down state for LPDDR4. This register is used for frequency change and MRR/MRW access during self refresh. 2'b00: SDRAM is not in Self Refresh. 2'b01: Self refresh 1 2'b10: Self refresh power down 2'b11: Self refresh 2 Programming Mode: Dynamic
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RO	0x0	selfref_type Flags if Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4) is entered and if it was under Automatic Self Refresh control only or not. 2'b00: SDRAM is not in Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4). If retry is enabled by CRCPARCTRL1.crc_parity_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. 2'b11: SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b10: SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. 2'b01: SDRAM is in Self Refresh, which was caused by PHY Master Request. Programming Mode: Dynamic
3	RO	0x0	reserved
2:0	RO	0x0	operating_mode Operating mode. This is 3-bits wide in configurations with mDDR/LPDDR2/LPDDR3/LPDDR4/DDR4 support and 2-bits in all other configurations. non-mDDR/LPDDR2/LPDDR3/LPDDR4 and non-DDR4 designs: 2'b00: Init 2'b01: Normal 2'b10: Power-down 2'b11: Self refresh mDDR/LPDDR2/LPDDR3 or DDR4 designs: 3'b000: Init 3'b001: Normal 3'b010: Power-down 3'b011: Self refresh 3'b1xx: Deep power-down/Maximum Power Saving Mode LPDDR4 designs: 3'b000: Init 3'b001: Normal 3'b010: Power-down 3'b011: Self refresh/Self refresh power-down Programming Mode: Dynamic

DDRC_MRCTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	mr_wr Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the uMCTL2 automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
30	RW	0x0	pba_mode Indicates whether PBA access is executed. When setting this bit to 1 along with setting pda_en to 1, uMCTL2 initiates PBA access instead of PDA access. 1'b0: Per DRAM Addressability mode 1'b1: Per Buffer Addressability mode The completion of PBA access is confirmed by MRSTAT.pda_done in the same way as PDA. Programming Mode: Dynamic
29:16	RO	0x0000	reserved
15:12	RW	0x0	mr_addr Address of the mode register that is to be written to. 4'b0000: MR0 4'b0001: MR1 4'b0010: MR2 4'b0011: MR3 4'b0100: MR4 4'b0101: MR5 4'b0110: MR6 4'b0111: MR7 Don't Care for LPDDR2/LPDDR3/LPDDR4 (see MRCTRL1.mr_data for mode register addressing in LPDDR2/LPDDR3/LPDDR4). In case of DDR4, the bit[3:2] corresponds to the bank group bits. Programming Mode: Dynamic
11:6	RO	0x00	reserved
5:4	RW	0x0	mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits should be set to 1. 2'b01: select rank 0 only 2'b10: select rank 1 only 2'b11: select rank 0 and 1 Programming Mode: Dynamic
3	RW	0x0	sw_init_int Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. 1'b0: Software intervention is not allowed. 1'b1: Software intervention is allowed. Programming Mode: Dynamic
2	RW	0x0	pda_en Indicates whether the mode register operation is MRS in PDA mode or not 1'b0: MRS 1'b1: MRS in Per DRAM Addressability mode Note that when pba_mode=1, PBA access is initiated instead of PDA access. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
1	RW	0x0	mpr_en Indicates whether the mode register operation is MRS or WR/RD for MPR (only supported for DDR4) 1'b0: MRS 1'b1: WR/RD for MPR Programming Mode: Dynamic
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. Only used for LPDDR2/LPDDR3/LPDDR4/DDR4. 1'b0: Write 1'b1: Read Programming Mode: Dynamic

DDRC_MRCTRL1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	mr_data Mode register write data for all non-LPDDR2/non-LPDDR3/non-LPDDR4 modes. For LPDDR2/LPDDR3/LPDDR4, MRCTRL1[15:0] are interpreted as [15:8] MR Address [7:0] MR data for writes, don't care for reads. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Programming Mode: Dynamic

DDRC_MRSTAT

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	pda_done The SoC core may initiate a MR write operation in PDA/PBA mode only if this signal is low. This signal goes high when three consecutive MRS commands related to the PDA/PBA mode are issued to the SDRAM. This signal goes low when MRCTRL0.pda_en becomes 0. Therefore, it is recommended to write MRCTRL0.pda_en to 0 after this signal goes high in order to prepare to perform PDA operation next time. 1'b0: Indicates that mode register write operation related to PDA/PBA is in progress or has not started yet. 1'b1: Indicates that mode register write operation related to PDA/PBA has competed. Programming Mode: Dynamic
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	mr_wr_busy The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when MRSTAT.mr_wr_busy is high. 1'b0: Indicates that the SoC core can initiate a mode register write operation 1'b1: Indicates that mode register write operation is in progress Programming Mode: Dynamic

DDRC_MRCTRL2

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mr_device_sel Indicates the device(s) to be selected during the MRS that happens in PDA mode. Each bit is associated with one device. For example, bit[0] corresponds to Device 0, bit[1] to Device 1 etc. A '1' should be programmed to indicate that the MRS command should be applied to that device. A '0' indicates that the MRS commands should be skipped for that device. Programming Mode: Dynamic

DDRC_DERATEEN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4 3'b000: Derating uses +1. 3'b001: Derating uses +2. 3'b010: Derating uses +3. 3'b011: Derating uses +4. Present only in designs configured to support LPDDR4. The required number of cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding up the next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RW	0x0	derate_byte Derate byte Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Indicates which byte of the MRR data is used for derating. Programming Mode: Static
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	derate_value Derate value 1'b0: Derating uses +1. 1'b1: Derating uses +2. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4 Set to 0 for all LPDDR2 speed grades as derating value of +1.875 ns is less than a core_ddrc_core_clk period. For LPDDR3/4, if the period of core_ddrc_core_clk is less than 1.875ns, this register field should be set to 1; otherwise it should be set to 0. Programming Mode: Quasi-dynamic Group 2 and Group 4
0	RW	0x0	derate_enable Enables derating 1'b0: Timing parameter derating is disabled 1'b1: Timing parameter derating is enabled using MR4 read value. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4 This field must be set to 0 for non-LPDDR2/LPDDR3/LPDDR4 mode. Programming Mode: Dynamic

DDRC_DERATEINT

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycle. Programming Mode: Static

DDRC_PWRCTL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while PWRCTL.selfref_sw==1. 1'b0: SR-PD -> SR -> SR-PD not allowed 1'b1: SR-PD -> SR -> SR-PD allowed Programming Mode: Dynamic
7	RW	0x0	dis_cam_drain_selfref Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. 1'b0: CAMs must be empty before entering SR. 1'b1: CAMs are not emptied before entering SR. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
6	RW	0x0	stay_in_selfref Self refresh state is an intermediate state to enter to Selfrefresh power down state or exit Self refresh power down state for LPDDR4. This register controls transition from the Self refresh state. 1'b1: Prohibit transition from Self refresh state 1'b0: Allow transition from Self refresh state Programming Mode: Dynamic
5	RW	0x0	selfref_sw A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating_mode. This is referred to as Software Entry/Exit to Self Refresh. 1'b1: Software Entry to Self Refresh 1'b0: Software Exit from Self Refresh Programming Mode: Dynamic
4	RW	0x0	mpsm_en When this is 1, the uMCTL2 puts the SDRAM into maximum power saving mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of maximum power saving mode. Present only in designs configured to support DDR4. For non-DDR4, this register should not be set to 1. Programming Mode: Dynamic
3	RW	0x0	en_dfi_dram_clk_disable Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR2/DDR3, can only be asserted in Self Refresh. In DDR4, can be asserted in the Self Refresh and Maximum Power Saving Mode In mDDR/LPDDR2/LPDDR3, can be asserted in the Self Refresh, Power Down, Deep Power Down and Normal operation (Clock Stop) In LPDDR4, can be asserted in the Self Refresh Power Down, Power Down and Normal operation (Clock Stop) Programming Mode: Dynamic
2	RW	0x0	deeppowerdown_en When this is 1, uMCTL2 puts the SDRAM into deep powerdown mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of deep power-down mode. Controller performs automatic SDRAM initialization on deep power-down exit. Present only in designs configured to support mDDR or LPDDR2 or LPDDR3. For non-mDDR/non-LPDDR2/nonLPDDR3, this register should not be set to 1. Programming Mode: Dynamic
1	RW	0x0	powerdown_en If true then the uMCTL2 goes into power-down after a programmable number of cycles "maximum idle clocks before power down" PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	selfref_en If true then the uMCTL2 puts the SDRAM into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic

DDRC_PWRTMG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. Unit: Multiples of 32 DFI clocks. Programming Mode: Static
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Unit: Multiples of 4096 DFI clocks. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into powerdown. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. Unit: Multiples of 32 DFI clocks Programming Mode: Static

DDRC_HWLUMCTL2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. Unit: Multiples of 32 DFI clocks. Programming Mode: Static
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x1	hw_lp_exit_idle_en When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). Programming Mode: Static
0	RW	0x1	hw_lp_en Enable for Hardware Low Power Interface. Programming Mode: Quasi-dynamic Group 3

DDRC_HWFFCCTL

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	target_vrcg Set target value of VRCG (MR13 OP[3]). This field value is used when HWFFC request has been issued. Programming Mode: Static
5	RW	0x0	init_vrcg Set initial value of VRCG (MR13 OP[3]). This field value is used when HWFFCCTL.hwffc_en has been changed to 2'b11. Programming Mode: Static
4	RW	0x1	init_fsp Set initial value of FSP-OP (MR13 OP[7]). This field value is used when HWFFCCTL.hwffc_en has been changed to 2'b11. Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x0	hwffc_en Enable HWFFC through Hardware Low Power Interface. The other fields of this register are used only when changing this field to 11. 2'b00: Disable HWFFC 2'b10: Intermediate, set only when disabling HWFFC 2'b11: Enable HWFFC 2'b01: Not allowed Programming Mode: Dynamic

DDRC_HWFFCSTAT

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	current_vrcg Indicates current value of VRCG (MR13 OP[3]). Programming Mode: Dynamic
8	RO	0x0	current_fsp Indicates current value of FSP-OP (MR13 OP[7]). Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RO	0x0	current_frequency Indicates the current frequency. 1'b0: Frequency 0/Normal 1'b1: Frequency 1/FREQ1 Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	RO	0x0	hwffc_operating_mode Operating mode of HWFFC. 1'b0: Normal 1'b1: Self Refresh or SR-Powerdown Programming Mode: Dynamic
0	RO	0x0	hwffc_in_progress Indicates HWFFC is in progress. Programming Mode: Dynamic

DDRC_RFSHCTL0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom_x32 may be equal to RFSHTMG.t_rfc_nom_x32>>2 if derating is enabled (DERATEEN.derate_enable=1). Otherwise, internally used t_rfc_nom_x32 will be equal to RFSHTMG.t_rfc_nom_x32. Unit: Multiples of 32 DFI clocks. Programming Mode: Dynamic - Refresh Related
19:17	RO	0x0	reserved
16:12	RW	0x10	refresh_to_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, but it has not expired (RFSHCTL0.refresh_burst+1) times yet, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful, but before it is absolutely required. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. Unit: Multiples of 32 DFI clocks. Programming Mode: Dynamic - Refresh Related
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worstcase latency associated with refreshes. 5'h0: Single refresh 5'h1: Burst-of-2 refresh 5'h7: Burst-of-8 refresh For DDR2/3, the refresh is always per-rank and not perbank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until the PHYinitiated update is complete. Programming Mode: Dynamic - Refresh Related
3	RO	0x0	reserved
2	RW	0x0	per_bank_refresh 1'b1: Per bank refresh 1'b0: All bank refresh Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but should be supported by all LPDDR3/LPDDR4 devices. Programming Mode: Static

DDRC_RFSHCTL1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related

DDRC_RFSHCTL3

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	refresh_mode Fine Granularity Refresh Mode 3'b000: Fixed 1x (Normal mode) 3'b001: Fixed 2x 3'b010: Fixed 4x 3'b101: Enable on the fly 2x (not supported) 3'b110: Enable on the fly 4x (not supported) Everything else - reserved Note: Only Fixed 1x mode is supported if RFSHCTL3.dis_auto_refresh = 1. Note: The on-the-fly modes are not supported in this version of the uMCTL2. Note: This must be set up while the Controller is in reset or while the Controller is in self-refresh mode. Changing this during normal operation is not allowed. Making this a dynamic register will be supported in future version of the uMCTL2. Note: This register field has effect only if a DDR4 SDRAM device is in use (MSTR.ddr4 = 1). Programming Mode: Quasi-dynamic Group 2
3:2	RO	0x0	reserved
1	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). The refresh register(s) are automatically updated when exiting reset. Programming Mode: Dynamic
0	RW	0x0	dis_auto_refresh When '1', disable auto-refresh generated by the uMCTL2. When auto-refresh is disabled, the SoC core must generate refreshes using the registers DBGCMD.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the uMCTL2. If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), disable autorefresh is not supported, and this bit must be set to '0'. (DDR4 only) If FGR mode is enabled (RFSHCTL3.refresh_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly. Programming Mode: Dynamic - Refresh Related

DDRC_RFSHTMG

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the t_rfc_nom_x1_x32 register value is x1 or x32.
30:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x062	t_rfc_nom_x1_x32 tREFI: Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). For LPDDR2/LPDDR3/LPDDR4: if using all-bank refreshes (RFSHCTL0.per_bank_refresh= 0), this register should be set to tREFIab if using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), this register should be set to tREFIpb When the controller is operating in 1:2 frequency ratio mode, program this to (tREFI/2), no rounding up. In DDR4 mode, tREFI value is different depending on the refresh mode. The user should program the appropriate value from the spec based on the value programmed in the refresh mode register. Note that if RFSHTMG.t_rfc_nom_x1_sel==1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min; if RFSHTMG.t_rfc_nom_x1_sel==0, RFSHTMG.t_rfc_nom_x1_x32*32 must be greater than RFSHTMG.t_rfc_min; RFSHTMG.t_rfc_nom_x32 must be greater than 0x1. Non-DDR4 or DDR4 Fixed 1x mode:RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE. DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF. DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF. Unit: Clocks or multiples of 32 clocks, depending on RFSHTMG.t_rfc_nom_x1_sel. Programming Mode: Dynamic - Refresh Related
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Should only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not. 1'b0: tREFBW parameter not used 1'b1: tREFBW parameter used Programming Mode: Static
14:10	RO	0x00	reserved
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min should be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user should program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI Clocks. Programming Mode: Dynamic - Refresh Related

DDRC_CRCPARCTL0

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	dfi_alert_err_cnt_clr DFI alert error count clear. Clear bit for DFI alert error counter. Asserting this bit will clear the DFI alert error counter, CRCPARSTAT.dfi_alert_err_cnt. When the clear operation is complete, the uMCTL2 automatically clears this bit. Programming Mode: Dynamic
1	WO	0x0	dfi_alert_err_int_clr Interrupt clear bit for DFI alert error. If this bit is set, the alert error interrupt on CRCPARSTAT.dfi_alert_err_int will be cleared. When the clear operation is complete, the uMCTL2 automatically clears this bit. Programming Mode: Dynamic
0	RW	0x0	dfi_alert_err_int_en Interrupt enable bit for DFI alert error. If this bit is set, any parity/CRC error detected on the dfi_alert_n input will result in an interrupt being set on CRCPARSTAT.dfi_alert_err_int. Programming Mode: Dynamic

DDRC_CRCPARCTL1

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	retry_add_rd_lat Retry additional read latency value. Delay value used is retry_add_rd_lat+1. Only used if CRCPARCTL1.retry_add_rd_lat_en is enabled. Selects the number of pipeline stages to dfi_rddata_valid/dfi_rddata/dfi_rddata_dbi before rest of internal uMCTL2 logic observes it. Required to compensate for fact delay in PHY/PCB for generating dfi_alert_n for retry may be more than the delay in PHY/PCB on read data path. Recommended settings (in terms of core_ddrc_core_clk): (Maximum Alert delay through PHY/PCB from erroneous read command including tPAR_UNKNOWN) - (Minimum Read data delay through PHY/PCB from erroneous read command) + (PHY's max granularity of dfi_rddata beats that may be corrupted before erroneous Read) Note: This calculation depends on various items such as RL, tPAR_ALERT_ON/tPAR_UNKNOWN/RCD/PHY/PCB behavior. Unit: DFI clock cycles. Programming Mode: Static
15	RW	0x0	retry_add_rd_lat_en Retry additional read latency enable. Number of pipeline stages selected is defined as CRCPARCTL1.retry_add_lat+1. Only set if CRCPARCTL1.crc_parity_retry_enable = 1 Programming Mode: Static
14:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x1	caparity_disable_before_sr If DDR4-SDRAM's CA parity is enabled by INIT6.mr5[2:0]!=0 and this register is set to 1, CA parity is automatically disabled before Self-Refresh entry and enabled after SelfRefresh exit by issuing MR5. 1'b1: CA parity is disabled before Self-Refresh entry 1'b0: CA parity is not disabled before Self-Refresh entry If Geardown is used by MSTR.geardown_mode=1, this register must be set to 1. If this register set to 0, DRAMTMG5.t_ckesr and DRAMTMG5.t_cksre must be increased by PL(Parity latency) Programming Mode: Static
11:8	RO	0x0	reserved
7	RW	0x0	crc_inc_dm CRC Calculation setting register 1'b1: CRC includes DM signal 1'b0: CRC not includes DM signal Present only in designs configured to support DDR4. Programming Mode: Static
6:5	RO	0x0	reserved
4	RW	0x0	crc_enable CRC enable Register 1'b1: Enable generation of CRC 1'b0: Disable generation of CRC The setting of this register should match the CRC mode register setting in the DRAM. Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	parity_enable C/A Parity enable register 1'b1: Enable generation of C/A parity and detection of C/A parity error 1'b0: Disable generation of C/A parity and disable detection of C/A parity error If RCD's parity error detection or SDRAM's parity detection is enabled, this register should be 1. Programming Mode: Static

DDRC_CRCPARSTAT

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	dfi_alert_err_fatl_int Fatal parity error interrupt. One or more these situation below happens, this interrupt bit is set:MPSMX caused parity error. (RCD's parity error detection only)Parity error happens again during software intervention time MRS was in retry_fifo_max_hold_timer_x4 window from alert_n=0 or STAT.operating_mode is Init. It remains set until cleared by CRCPARCTL0.dfi_alert_err_fatl_clr. If this interrupt is asserted, system reset is strongly recommended. Programming Mode: Static

Bit	Attr	Reset Value	Description
16	RO	0x0	dfi_alert_err_int DFI alert error interrupt. If a parity/CRC error is detected on dfi_alert_n, and the interrupt is enabled by CRCPARCTL0.dfi_alert_err_int_en, this interrupt bit will be set. It will remain set until cleared by CRCPARCTL0.dfi_alert_err_int_clr Programming Mode: Static
15:0	RO	0x0000	dfi_alert_err_cnt DFI alert error count. If a parity/CRC error is detected on dfi_alert_n, this counter be incremented. This is independent of the setting of CRCPARCTL0.dfi_alert_err_int_en. It will saturate at 0xFFFF, and can be cleared by asserting CRCPARCTL0.dfi_alert_err_cnt_clr. Programming Mode: Static

DDRC_INIT0

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	skip_dram_init If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed 2'b00: SDRAM Intialization routine is run after power-up 2'b01: SDRAM Intialization routine is skipped after powerup. Controller starts up in Normal Mode 2'b11: SDRAM Intialization routine is skipped after powerup. Controller starts up in Self-refresh Mode 2'b10: SDRAM Intialization routine is run after power-up. Programming Mode: Quasi-dynamic Group 2
29:26	RO	0x0	reserved
25:16	RW	0x002	post_cke_x1024 Cycles to wait after driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 typically requires a 400 ns delay, requiring this value to be programmed to 2 at all clock speeds. LPDDR2/LPDDR3 typically requires this to be programmed for a delay of 200 us. LPDDR4 typically requires this to be programmed for a delay of 2 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x04e	pre_cke_x1024 Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 specifications typically require this to be programmed for a delay of >= 200 us. LPDDR2/LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static

DDRC_INIT1

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	dram_rstn_x1024 Number of cycles to assert SDRAM reset signal during init sequence.This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices.When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 1024 DFI clock cycles. Programming Mode: Static
15:4	RO	0x000	reserved
3:0	RW	0x0	pre_ocd_x32 Wait period before driving the OCD complete command to SDRAM. Unit: Counts of a global timer that pulses every 32 DFI clock cycles.There is no known specific requirement for this; it may be set to zero. Programming Mode: Static

DDRC_INIT2

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0d	idle_after_reset_x32 Idle time after the reset command, tINIT4. Present only in designs configured to support LPDDR2. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x5	min_stable_clock_x1 Time to wait after the first CKE high, tINIT2. Present only in designs configured to support LPDDR2/LPDDR3. LPDDR2/LPDDR3 typically requires 5 x tCK delay. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Static

DDRC_INIT3

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2: Value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Programming Mode: Quasi-dynamic Group 1 and Group 4
15:0	RW	0x0510	emr DDR2: Value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. If PHY-evaluation mode training is enabled, this bit is set appropriately by the uMCTL2 during write leveling. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register Programming Mode: Quasi-dynamic Group 4

DDRC_INIT4

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register mDDR: Unused Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register mDDR/LPDDR2/LPDDR3: Unused LPDDR4: Value to write to MR13 register Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_INIT5

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x10	dev_zqinit_x32 ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR2/LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR2/LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
15:10	RO	0x00	reserved
9:0	RW	0x004	max_auto_init_x1024 Maximum duration of the auto initialization, tINIT5. Present only in designs configured to support LPDDR2/LPDDR3.LPDDR2/LPDDR3 typically requires 10 us. Unit: 1024 DFI clock cycles. Programming Mode: Static

DDRC_INIT6

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4- Value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:0	RW	0x0000	mr5 DDR4- Value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Programming Mode: Quasi-dynamic Group 1 and Group 4

DDRC_INIT7

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr6 DDR4- Value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	mr22 LPDDR4- Value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Programming Mode: Quasi-dynamic Group 4

DDRC_DIMMCTL

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	mrs_bg1_en Enable for BG1 bit of MRS command. BG1 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have BG1 are attached and both the CA parity and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include BG1 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. If address mirroring is enabled, this is applied to BG1 of even ranks and BG0 of odd ranks. 1'b1: Enabled 1'b0: Disabled Programming Mode: Static
3	RW	0x0	mrs_a17_en Enable for A17 bit of MRS command. A17 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have A17 are attached and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include A17 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. 1'b1: Enabled 1'b0: Disabled Programming Mode: Static

DDRC_RANKCTL

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value should consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, should be increased by 1. If write preamble is set to 2tCK(DDR4 only), should be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, the requirement is ODTLoff - ODTLon - BL/2 + 1 When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. Programming Mode: Quasi-dynamic Group 2

Bit	Attr	Reset Value	Description
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value should consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) If read preamble is set to 2tCK(DDR4 only), should be increased by 1. If read postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads. When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. Programming Mode: Static
3:0	RW	0xf	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. Programming Mode: Static

DDRC_DRAMTMG0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Unit: DFI Clocks Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x10	t_faw tFAW Valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15	RO	0x0	reserved
14:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:2 frequency ratio mode, program this to (tRAS(max)-1)/2. No rounding up. Unit: Multiples of 1024 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:6	RO	0x0	reserved
5:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. When the controller is operating in 1:2 frequency mode, 1T mode, program this to tRAS(min)/2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, program this to (tRAS(min)/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. For DDR3, this should be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR2: tAL + BL/2 + max(tRTP, 2) - 2 DDR3: tAL + max (tRTP, 4) DDR4: Max of following two equations: tAL + max (tRTP, 4) or, RL + BL/2 - tRP (*). mDDR: BL/2 LPDDR2: Depends on if it's LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + tRTP - 1. LPDDR2-S4: BL/2 + max(tRTP,2) - 2. LPDDR3: BL/2 + max(tRTP,4) - 4 LPDDR4: BL/2 + max(tRTP,8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
7	RO	0x0	reserved
6:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set to WL. Time from write command to write data on SDRAM interface. For mDDR, it should normally be set to 1. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols Unit: DFI clocks Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x05	read_latency Set to RL. Time from read command to read data on SDRAM interface. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols Unit: DFI clocks Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what should be included here. Unit: DFI Clocks. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = write preamble. This is unique to DDR4 and LPDDR4. RD_POSTAMBLE = read postamble. This is unique to LPDDR4. For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax should be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
7:6	RO	0x0	reserved
5:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Unit: DFI Clocks. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

DDRC_DRAMTMG3

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x005	t_mrw Time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the above values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Programming Mode: Quasi-dynamic Group 2 and Group 4
19:18	RO	0x0	reserved
17:12	RW	0x04	t_mrd tMRD: Cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. Programming Mode: Quasi-dynamic Group 2 and Group 4
11:10	RO	0x0	reserved
9:0	RW	0x00c	t_mod tMOD: Parameter used only in DDR3 and DDR4. Cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If MPR writes for DDR4 are used, set to tMOD + AL (or tMPD_PAR + AL if C/A parity is also used). Set to tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:12	RO	0x0	reserved
11:8	RW	0x4	t_rrd DDR4: tRRD_L: Minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b". When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved
4:0	RW	0x05	t_rp tRP: Minimum time from precharge to activate of same bank. When the controller is operating in 1:2 frequency ratio mode, t_rp should be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp should be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x5	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKCKEH DDR2: 1 DDR3: tCKSRX DDR4: tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x5	t_cksre This is the time after Self Refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKELCK DDR2: 1 DDR3: max (10 ns, 5 tCK) DDR4: max (10 ns, 5 tCK) (+ PL(parity latency)(*)) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:14	RO	0x0	reserved
13:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR: tRFC LPDDR2: tCKESR LPDDR3: tCKESR LPDDR4: max(tCKE, tSR) DDR2: tCKE DDR3: tCKE + 1 DDR4: tCKE + 1 (+ PL(parity latency)(*)) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	t_cke Minimum number of cycles of CKE HIGH/LOW during power-down and self refresh. LPDDR2/LPDDR3 mode: Set this to the larger of tCKE or tCKESR LPDDR4 mode: Set this to the larger of tCKE or tSR. Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs: Set this to tCKE value. When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x2	t_ckdpde This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKCKEH DDR2: 1 DDR3: tCKSRX DDR4: tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:4	RO	0x000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR: 1 LPDDR2: tXP + 2 LPDDR3: tXP + 2 LPDDR4: tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG7

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKELCK When using DDR2/3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RO	0x0	reserved
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: 2 When using DDR2/3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit Self Refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4
23	RO	0x0	reserved
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit Self Refresh to commands not requiring a locked DLL in Self Refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4
15	RO	0x0	reserved
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG9

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode 1'b0: 1tCK preamble 1'b1: 2tCK preamble Programming Mode: Quasi-dynamic Group 2 and Group 4
29:19	RO	0x000	reserved

Bit	Attr	Reset Value	Description
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:12	RO	0x0	reserved
11:8	RW	0x4	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:6	RO	0x0	reserved
5:0	RW	0x0d	wr2rd_s CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Present only in designs configured to support DDR4. Unit: DFI Clocks. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

DDRC_DRAMTMG10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns/0.625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15:13	RO	0x0	reserved
12:8	RW	0x18	t_cmd_gear Sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min). tMOD(min) is greater of 24nCK or 15ns 15ns/0.625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RO	0x0	reserved
3:2	RW	0x2	t_gear_setup Geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks. When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
1:0	RW	0x2	t_gear_hold Geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks. When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI Clocks Value After Reset: 0x2 Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG11

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:21	RO	0x0	reserved
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:10	RO	0x00	reserved
9:8	RW	0x2	t_mpx_s tMPX_S: Minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved
4:0	RW	0x1c	t_ckmpe tCKMPE: Minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. Unit: DFI Clocks. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG12

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE. When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:5	RO	0x000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: tODTLoff: This is the latency from CAS-2 command to tODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (tODTLoff/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:3	RO	0x0000	reserved
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG15

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1'b1: Enable using tSTAB when exiting DFI LP. Needs to be set when the PHY is stopping the clock during DFI LP to save maximum power. 1'b0: Disable using tSTAB when exiting DFI LP. Programming Mode: Quasi-dynamic Group 2 and Group 4
30:8	RO	0x000000	reserved
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM : when exiting power saving mode, if the clock was stopped, after re-enabling it the clock must be stable for a time specified by tSTAB in the case of input clock frequency change (DDR4)after issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4)When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_vrcg_enable LPDDR4: tVRCG_ENABLE: VREF high current mode enable time.When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_ENABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x000	reserved
6:0	RW	0x00	t_vrcg_disable LPDDR4: tVRCG_ENABLE: VREF high current mode disable time.When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_DISABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4

DDRC_ZQCTL0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1'b1: Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. 1'b0: Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
30	RW	0x0	dis_srx_zqcl 1'b1: Disable issuing of ZQCL/MPC(ZQ calibration)command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode. 1'b0: Enable issuing of ZQCL/MPC(ZQ calibration)command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4
29	RW	0x0	zq_resistor_shared 1'b1: Denotes that ZQ resistor is shared between ranks.Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap. 1'b0: ZQ resistor is not shared. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
28	RW	0x0	dis_mpsmx_zqcl 1'b1: Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode. 1'b0: Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode. This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Programming Mode: Static
27	RO	0x0	reserved
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM.When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value.This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static

DDRC_ZQCTL1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DFI clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM.When the controller is operating in 1:2 frequency ratio mode, program this to tZQReset/2 and round it up to the next integer value.This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR3/DDR4/LPDDR2/LPDDR3/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: 1024 DFI clock cycles. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static

DDRC_ZQCTL2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	zq_reset Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the uMCTL2 automatically clears this bit. It is recommended NOT to set this signal if in Init, Self-Refresh(except LPDDR4) or SRPowerdown(LPDDR4) or Deep power-down operating modes. This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Dynamic

DDRC_ZQSTAT

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	zq_reset_busy SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. 1'b0: Indicates that the SoC core can initiate a ZQ Reset operation. 1'b1: Indicates that ZQ Reset operation is in progress. Programming Mode: Dynamic

DDRC_DFITMG0

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. 1'b0: In terms of HDR (DFI clock) cycles, Only support HDR DFI clock. 1'b1: In terms of SDR (DFI PHY clock) cycles Programming Mode: Static
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DFI clock cycles Programming Mode: Quasi-dynamic Group 1 and Group 4
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles 1'b0: In terms of HDR (DFI clock) cycles, Only support HDR DFI clock. 1'b1: In terms of SDR (DFI PHY clock) cycles Programming Mode: Static
14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles Programming Mode: Quasi-dynamic Group 1 and Group 4

DDRC_DFITMG1

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, should be set to '0' or the value which matches the CAL mode register setting in the DRAM. If the PHY can add the latency for CAL mode, this should be set to '0'. Valid Range: 0, 3, 4, 5, 6, and 8 Programming Mode: Quasi-dynamic Group 2 and Group 4
27:26	RO	0x0	reserved
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Programming Mode: Quasi-dynamic Group 4
23:21	RO	0x0	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. Refer to PHY specification for correct value. Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the deassertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4

DDRC_DFILPCFG0

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_tlp_resp Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Power Down and Maximum Power Saving modes. DFI 2.1 specification onwards, recommends using a fixed value of 7 always. Programming Mode: Static
23:20	RW	0x0	dfi_lp_wakeup_dpd Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered. Determines the DFI's tlp_wakeup time. 4'h0: 16 cycles 4'h1: 32 cycles 4'h2: 64 cycles 4'h3: 128 cycles 4'h4: 256 cycles 4'h5: 512 cycles 4'h6: 1024 cycles 4'h7: 2048 cycles 4'h8: 4096 cycles 4'h9: 8192 cycles 4'hA: 16384 cycles 4'hB: 32768 cycles 4'hC: 65536 cycles 4'hD: 131072 cycles 4'hE: 262144 cycles 4'hF: Unlimited This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Programming Mode: Static
19:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	dfi_lp_en_dpd Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit. 1'b0: Disabled 1'b1: Enabled This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Programming Mode: Static
15:12	RW	0x0	dfi_lp_wakeup_sr Value in DFI clpck cycles to drive on dfi_lp_wakeup signal when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time. 4'h0: 16 cycles 4'h1: 32 cycles 4'h2: 64 cycles 4'h3: 128 cycles 4'h4: 256 cycles 4'h5: 512 cycles 4'h6: 1024 cycles 4'h7: 2048 cycles 4'h8: 4096 cycles 4'h9: 8192 cycles 4'hA: 16384 cycles 4'hB: 32768 cycles 4'hC: 65536 cycles 4'hD: 131072 cycles 4'hE: 262144 cycles 4'hF: Unlimited Programming Mode: Static
11:9	RO	0x0	reserved
8	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit. 1'b0: Disabled 1'b1: Enabled Programming Mode: Static

Bit	Attr	Reset Value	Description
7:4	RW	0x0	dfi_lp_wakeup_pd Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time. 4'h0: 16 cycles 4'h1: 32 cycles 4'h2: 64 cycles 4'h3: 128 cycles 4'h4: 256 cycles 4'h5: 512 cycles 4'h6: 1024 cycles 4'h7: 2048 cycles 4'h8: 4096 cycles 4'h9: 8192 cycles 4'hA: 16384 cycles 4'hB: 32768 cycles 4'hC: 65536 cycles 4'hD: 131072 cycles 4'hE: 262144 cycles 4'hF: Unlimited Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 1'b0: Disabled 1'b1: Enabled Programming Mode: Static

DDRC_DFILPCFG1

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	dfi_lp_wakeup_mpsm Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Maximum Power Saving Mode is entered. Determines the DFI's tlp_wakeup time. 4'h0: 16 cycles 4'h1: 32 cycles 4'h2: 64 cycles 4'h3: 128 cycles 4'h4: 256 cycles 4'h5: 512 cycles 4'h6: 1024 cycles 4'h7: 2048 cycles 4'h8: 4096 cycles 4'h9: 8192 cycles 4'hA: 16384 cycles 4'hB: 32768 cycles 4'hC: 65536 cycles 4'hD: 131072 cycles 4'hE: 262144 cycles 4'hF: Unlimited This is only present for designs supporting DDR4 devices. Programming Mode: Static

Bit	Attr	Reset Value	Description
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_mpsm Enables DFI Low Power interface handshaking during Maximum Power Saving Mode Entry/Exit. 1'b0: Disabled 1'b1: Enabled This is only present for designs supporting DDR4 devices. Programming Mode: Static

DDRC_DFIUPD0

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_ctrlupd When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2. The core must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd. When '0', uMCTL2 issues dfi_ctrlupd_req periodically. Programming Mode: Quasi-dynamic Group 3
30	RW	0x0	dis_auto_ctrlupd_srx When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2 at self-refresh exit. When '0', uMCTL2 issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. Programming Mode: Static
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX. 1'b0: Send ctrlupd after SRX 1'b1: Send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. Programming Mode: Static
28:26	RO	0x0	reserved
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Programming Mode: Static
15:10	RO	0x00	reserved
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x3. Programming Mode: Static

DDRC_DFIUPD1

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between uMCTL2 initiated DFI update requests (which is executed whenever the uMCTL2 is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the uMCTL2 is idle. Minimum allowed value for this field is 1. Unit: 1024 DFI clock cycles Programming Mode: Static
15:8	RO	0x00	reserved
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between uMCTL2 initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: 1024 DFI clock cycles Programming Mode: Static

DDRC_DFIUPD2

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 1'b0: Disabled 1'b1: Enabled Programming Mode: Static

DDRC_DFIMISC

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	dfi_frequency Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Programming Mode: Quasi-dynamic Group 1
7:6	RO	0x0	reserved
5	RW	0x0	dfi_init_start PHY init start request signal.When asserted it triggers the PHY init start request. Programming Mode: Quasi-dynamic Group 3
4	RW	0x0	ctl_idle_en Enables support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. See signal description of ctl_idle signal for further details of ctl_idle functionality. Programming Mode: Static

Bit	Attr	Reset Value	Description
3	RW	0x0	share_dfi_dram_clk_disable Indicate dfi_dram_clk_disable is shared for two channels or not. 1'b1: Share mode 1'b0: Not share In Shared mode, Controller does not request PHY stop clock while any rank of any channel has not disable clock. Note: when dfi_dram_clk_disable is shared by two channels, an additional DFF is inserted, that will cause dram clock enable is delay one cycle. Suggest set dfi_t_dram_clk_enable value to Tdram_clk_enable+1. Tdram_clk_enable value is from PHY, which indicate how many cycles from dfi_dram_clk_disable de-assert to dram clock output. Programming Mode: Static
2	RW	0x0	dfi_data_cs_polarity Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. 1'b0: Signals are active low. 1'b1: Signals are active high. Programming Mode: Static
1	RW	0x0	phy_dbi_mode DBI implemented in DDRC or PHY. 1'b0: DDRC implements DBI functionality. 1'b1: PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4. Programming Mode: Static
0	RW	0x1	dfi_init_complete_en PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation. Programming Mode: Quasi-dynamic Group 3

DDRC_DFITMG2

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DFITMG3

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Static

DDRC_DFISTAT

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dfi_lp_ack Stores the value of the dfi_lp_ack input to the controller. Programming Mode: Dynamic
0	RO	0x0	dfi_init_complete The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. Programming Mode: Dynamic

DDRC_DBICTL

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 1'b0: Read DBI is disabled. 1'b1: Read DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[6] Programming Mode: Quasi-dynamic Group 1
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 1'b0: Write DBI is disabled. 1'b1: Write DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[7] Programming Mode: Quasi-dynamic Group 1

Bit	Attr	Reset Value	Description
0	RW	0x1	dm_en DM enable signal in DDRC. 1'b0: DM is disabled. 1'b1: DM is enabled. This signal must be set the same logical value as DRAM's mode register. DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. LPDDR4: Set this to inverted value of MR13[5] which is opposite polarity from this signal. Programming Mode: Quasi-dynamic Group 3

DDRC_DFIPHYMSTR

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface. 1'b0: Disabled 1'b1: Enabled Programming Mode: Dynamic

DDRC_ADDRMAP0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	addrmap_dch_bit0 Selects the HIF address bit used as data channel address bit 0. Valid Range: 0 to 30, and 31 (Traffic constraints apply based on the register value when UMCTL2_EXCL_ACCESS>0. See Exclusive Access section for details.) Internal Base: 2 The selected address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then channel bit is set to 0. Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_cs_bit1 Selects the HIF address bit used as rank address bit 1. Valid Range: 0 to 28, and 31 Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 1 is set to 0. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 29, and 31 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31 and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Programming Mode: Static
15:14	RO	0x0	reserved
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32 and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_col_b5 Full bus width mode: Selects the HIF address bit used as column address bit 5. Half bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	addrmap_col_b4 Full bus width mode: Selects the HIF address bit used as column address bit 4. Half bus width mode: Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_col_b3 Full bus width mode: Selects the HIF address bit used as column address bit 3. Half bus width mode: Selects the HIF address bit used as column address bit 4. Valid Range: 0 to 7 Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0. Programming Mode: Static
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	addrmap_col_b2 Full bus width mode: Selects the HIF address bit used as column address bit 2. Half bus width mode: Selects the HIF address bit used as column address bit 3. Valid Range: 0 to 7 Internal Base: 2 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless: in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and either In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0 If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless: in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and In DDR4 and ADDRMAP8.addrmap_bg_b0==0 Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3. Programming Mode: Static

DDRC_ADDRMAP3

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	addrmap_col_b9 Full bus width mode: Selects the HIF address bit used as column address bit 9. Half bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, and 31. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_col_b8 Full bus width mode: Selects the HIF address bit used as column address bit 8. Half bus width mode: Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, and 31. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_col_b7 Full bus width mode: Selects the HIF address bit used as column address bit 7. Half bus width mode: Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, and 31. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_col_b6 Full bus width mode: Selects the HIF address bit used as column address bit 6. Half bus width mode: Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, and 15 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

DDRC_ADDRMAP4

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x00	addrmap_col_b11 Full bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). Half bus width mode: Unused. To make it unused, this should be tied to 4'hF. Valid Range: 0 to 7, and 31. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_col_b10 Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, and 31. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static

DDRC_ADDRMAP5

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b11 Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 11, and 15 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 11 is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	addrmap_row_b2_10 Selects the HIF address bits used as row address bits 2 to 10. Valid Range: 0 to 11, and 15 Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) etc increasing to 16 (for row address bit 10) The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When value 15 is used the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 11 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 11 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static

DDRC_ADDRMAP6

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31	RW	0x0	lpddr3_6gb_12gb Set this to 1 if there is an LPDDR3 SDRAM 6Gb or 12Gb device in use. 1'b1: LPDDR3 SDRAM 6Gb/12Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid. 1'b0: Non-LPDDR3 6Gb/12Gb device in use. All addresses are valid. Present only in designs configured to support LPDDR3. Programming Mode: Static
30:29	RW	0x0	lpddr4_6gb_12gb_24gb Indicates what type of LPDDR4 SDRAM device is in use. 2'b00: No LPDDR4 SDRAM 6Gb/12Gb/24Gb device in use. All addresses are valid. 2'b01: LPDDR4 SDRAM 6Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid. 2'b10: LPDDR4 SDRAM 12Gb device in use. Every address having row[15:14]==2'b11 is considered as invalid. 2'b11: LPDDR4 SDRAM 24Gb device in use. Unsupported. Present only in designs configured to support LPDDR4. Programming Mode: Static
28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 11, and 15 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 15 is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 11, and 15 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 14 is set to 0. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 11, and 15 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 13 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 11, and 15 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 12 is set to 0. Programming Mode: Static

DDRC_ADDRMAP7

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 11, and 15 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 16 is set to 0. Programming Mode: Static

DDRC_ADDRMAP8

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP9

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 11 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x0	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 11 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 11 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 11 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ADDRMAP10

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 11 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 11 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 11 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 11 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ADDRMAP11

Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	addrmap_row_b10 Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 11 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ODTCFG

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8: 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7(DDR2-1066); BL4: 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8: 0x6 DDR4: BL8: 5 + WR_PREAMBLE + CRC_MODE. WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8: 7 + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	wr_odt_delay The delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066). If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Programming Mode: Quasi-dynamic Group 1 and Group 4
15:12	RO	0x0	reserved
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8: 0x6 (not DDR2-1066), 0x7 (DDR2-1066); BL4: 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8: 5 + RD_PREAMBLE. RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCKwrite preamble) LPDDR3: BL8: 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
7	RO	0x0	reserved
6:2	RW	0x00	rd_odt_delay The delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066). If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode). WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). If (CL - CWL - RD_PREAMBLE + WR_PREAMBLE) < 0, uMCTL2 does not support ODT for read operation. LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4

DDRC_ODTMAP

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
11:10	RO	0x0	reserved
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
7:6	RO	0x0	reserved
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static

DDRC_SCHED

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. Programming Mode: Static
23:12	RO	0x000	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x8	lpr_num_entries Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. Programming Mode: Static
7:3	RO	0x00	reserved
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if SCHED1.pageclose_timer=0. Even if this register set to 1 and SCHED1.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The pageclose feature provids a midway between Open and Close page policies. Programming Mode: Quasi-dynamic Group 3

DDRC_SCHED1

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Programming Mode: Static

DDRC_PERFLPR1

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	lpr_max_starve Number of DFI clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies. Programming Mode: Quasi-dynamic Group 3

DDRC_PERFWR1

Address: Operational Base + offset (0x026c)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x00	reserved
15:0	RW	0x007f	w_max_starve Number of DFI clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies. Programming Mode: Quasi-dynamic Group 3

DDRC_DBG0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with DBG0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). Programming Mode: Static

DDRC_DBG1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	dis_hif When 1, uMCTL2 asserts the HIF command signal hif_cmd_stall. uMCTL2 will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Programming Mode: Dynamic
0	RW	0x0	dis_dq When 1, uMCTL2 will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the uMCTL2, which makes it safe to modify certain register fields associated with reads and writes (see User Guide for details). After setting this bit, it is strongly recommended to poll DBGCAM.wr_data_pipeline_empty and DBGCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Programming Mode: Dynamic

DDRC_DBGCAM

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	wr_data_pipeline_empty When 1, indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Programming Mode: Dynamic
28	RO	0x0	rd_data_pipeline_empty When 1indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Programming Mode: Dynamic
27	RO	0x0	reserved
26	RO	0x0	dbg_wr_q_empty When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time. Programming Mode: Dynamic
25	RO	0x0	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
24	RO	0x0	dbg_stall Stall Programming Mode: Dynamic
23:20	RO	0x0	reserved
19:16	RO	0x0	dbg_w_q_depth Write queue depth The last entry of WR queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic
15:12	RO	0x0	reserved
11:8	RO	0x0	dbg_lpr_q_depth Low priority read queue depth. The last entry of Lpr queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic

DDRC_DBGCMD

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the uMCTL2 to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Programming Mode: Dynamic
4	RW	0x0	zq_calib_short Setting this register bit to 1 indicates to the uMCTL2 to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init operating mode. This register bit is ignored when in SelfRefresh(except LPDDR4) and SR-Powerdown(LPDDR4) and Deep power-down operating modes and Maximum Power Saving Mode. Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RW	0x0	rank1_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 1. Writing to this bit causes DBGSTAT.rank1_refresh_busy to be set. When DBGSTAT.rank1_refresh_busy is cleared, the command has been stored in uMCTL2. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
0	RW	0x0	rank0_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 0. Writing to this bit causes DBGSTAT.rank0_refresh_busy to be set. When DBGSTAT.rank0_refresh_busy is cleared, the command has been stored in uMCTL2. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Programming Mode: Dynamic

DDRC_DBGSTAT

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ctrlupd_busy SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the uMCTL2. It is recommended not to perform ctrlupd operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a ctrlupd operation. 1'b1: Indicates that ctrlupd operation has not been initiated yet in the uMCTL2. Programming Mode: Dynamic
4	RO	0x0	zq_calib_short_busy SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the uMCTL2. It is recommended not to perform ZQCS operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a ZQCS operation. 1'b1: Indicates that ZQCS operation has not been initiated yet in the uMCTL2. Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RO	0x0	rank1_refresh_busy SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after DBGCMD.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the uMCTL2. It is recommended not to perform rank1_refresh operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a rank1_refresh operation. 1'b1: Indicates that rank1_refresh operation has not been stored yet in the uMCTL2. Programming Mode: Dynamic

Bit	Attr	Reset Value	Description
0	RO	0x0	rank0_refresh_busy SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after DBGCMD.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the uMCTL2. It is recommended not to perform rank0_refresh operations when this signal is high. 1'b0: Indicates that the SoC core can initiate a rank0_refresh operation. 1'b1: Indicates that rank0_refresh operation has not been stored yet in the uMCTL2. Programming Mode: Dynamic

DDRC_SWCTL

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	sw_done Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Programming Mode: Dynamic

DDRC_SWSTAT

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Programming Mode: Static

DDRC_POISONCFG

Address: Operational Base + offset (0x036c)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
23:21	RO	0x0	reserved
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning. Programming Mode: Dynamic
19:17	RO	0x0	reserved
16	RW	0x1	rd_poison_slverr_en If set to 1, enables SLVERR response for read transaction poisoning. Programming Mode: Dynamic
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	WO	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning. Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x1	wr_poison_slverr_en If set to 1, enables SLVERR response for write transaction poisoning. Programming Mode: Dynamic

DDRC_POISONSTAT

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic
15:1	RO	0x0000	reserved
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic

DDRC_PSTAT

Address: Operational Base + offset (0x03fc)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI port 0. Programming Mode: Dynamic
15:1	RO	0x0000	reserved
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI port 0. Programming Mode: Dynamic

DDRC_PCCFG

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	bl_exp_mode Burst length expansion mode. By default (i.e. bl_exp_mode==0) XPI expands every AXI burst into multiple HIF commands, using the memory burst length as a unit. If set to 1, then XPI will use half of the memory burst length as a unit. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in cases where Partial Writes is enabled (UMCTL2_PARTIAL_WR=1), in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: UMCTL2_PARTIAL_WR=0 UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Programming Mode: Static
7:5	RO	0x0	reserved
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	go2critical_en If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. Programming Mode: Static

DDRC_PCFGR_0

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Programming Mode: Static

Bit	Attr	Reset Value	Description
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Programming Mode: Static
12	RW	0x0	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x000	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition -Priority0). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Programming Mode: Static

DDRC_PCFGW_0

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Programming Mode: Static

Bit	Attr	Reset Value	Description
12	RW	0x0	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Programming Mode: Static
11:10	RO	0x0	reserved
9:0	RW	0x000	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Programming Mode: Static

DDRC_PCTRL_0

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	port_en Enables AXI port 0. Programming Mode: Dynamic

DDRPHY_REG0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	reg_rank4_en enable the 4 rank of lpddr3 and lpddr4
19:13	RO	0x00	reserved
12:8	RW	0x00	reg_channel_en The byte enable signal of the PHY. High is valid. The defautl mode will open the four bytes at the same time. [0]: The byte0 enable signal, corresponding to A_DQ0~A_DQ7. [1]: The byte1 enable signal, corresponding to A_DQ8~A_DQ15. [2]: The byte2 enable signal, corresponding to B_DQ0~B_DQ7. [3]: The byte3 enable signal, corresponding to B_DQ8~B_DQ15. [4]: The byte4 enable signal, corresponding to C_DQ0~C_DQ7 If the user only wants to use two bytes, we suggest to choose the byte0 and byte1.
7	RW	0x1	reg_burst_sel According to the SDRAM type to choose the burst type that the PHY needs to support. 1: Support the BL8/BL16 0: Reserved.

Bit	Attr	Reset Value	Description
6:4	RW	0x0	mem_select_t Reset digital core, active low.
3	RO	0x0	reserved
2	RW	0x1	soft_reset1 The reset signal of digital core, Active low.
1	RW	0x1	soft_reset0 The reset signal of analog logic, Active low.
0	RW	0x1	soft_reset The reset signal of digital core and analog logic. Active low.

DDRPHY_REG1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_wl_loadmode [23:16]Write leveling load mode [7:0]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register should keep the same value with the MR1[7:0]. For LPDDR3/LPDDR4, this register should keep the same value with the MR2[7:0]. Please reference to the section 4.5.2 to get more information. [31:24]"Write leveling load mode [15:8]. Relate to the register 10'h002 [2]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register [13:8] should keep the same value with the MR1[13:8] and this register[15:14] should set 2'b01. For LPDDR3/LPDDR4, this register should set to 8'h0. Please reference to the section 4.5.2 to get more information.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0xe	reg_wlcs_sel The rank select signal of the write-leveling fuction. Low is valid. 4'b0000: The write-leveling result will auto switch between the RANK0 ,RANK1,RANK2,RANK3 according to the DFI interface command after the write-leveling training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the write-leveling training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the write-leveling training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the write-leveling training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the write-leveling training. 4'b1111: Reserved. Note: Can't set to 4'b0000 when enable the write-levleing training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the write-leveling training
7	RW	0x0	reg_wl_bypass The tx perbit-skew bypass function enable signal. High is valid. 1’b0: Use the write-leveling training result to control the tx perbit-skew delay.The A_DQ0~A_DQ7/A_DM0 will use the A_DQS0 training result.The A_DQ8~A_DQ15/A_DM1 will use the A_DQS1 training result.INNOSILICON INNO DDR PHY For TSMC 22-nm 239 INNOSILICON TECHNOLOGY CO LTD.The B_DQ0~A_DQ7/A_DM0 will use the B_DQS0 training result.The B_DQ8~A_DQ15/A_DM0 will use the B_DQS1 training result. 1’b1: Use the register to control the tx perbit-skew delay. Each data pad has an independet controller register.
6	RW	0x0	reg_wl_enable The write-leveling training enable signal. High is valid. 1’b0: Keep current state or exit the write-leveling training state. 1’b1: Eanble the write-leveling training function.
5:2	RW	0x0	reg_calcs_sel The rank select signal of the rx-dqs calibration fuction. Low is valid. 4'b0000: The rx-dqs calibration result will auto switch between the RANK0, RANK1,RANK2,RANK3 according to the DFI interface command after the rx-dqs calibration training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the auto rx-dqs calibration training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the auto rx-dqs calibration training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the auto rx-dqs calibration training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the auto rx-dqs calibration training. 4'b11: Reserved. Note: Can't set to 2'b00 when enable the rx-dqs calibration training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the rx-dqs calibration training.
1	RW	0x0	reg_calib_bypass Reserved.

Bit	Attr	Reset Value	Description
0	RW	0x0	reg_start_calib The auto rx-dqs calibration training enable signal. High is valid. 1'b0: Keep current state or exit the auto rx-dqs calibration training. 1'b1: Enable the auto rx-dqs calibration training function.

DDRPHY_REG2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	AL_FRE_OP0 Setting the AL vlaue of the PHY for frequency point 0. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP0 as the AL setting of the PHY when the freq== 2'b00. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
23:22	RO	0x0	reserved
21:16	RW	0x00	AL_FRE_OP1 Setting the AL vlaue of the PHY for frequency point 1. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP1 as the AL setting of the PHY when the freq == 2'b01.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
15:14	RO	0x0	reserved
13:8	RW	0x00	AL_FRE_OP2 Setting the AL vlaue of the PHY for frequency point 2. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP2 as the AL setting of the PHY when the freq == 2'b10.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
7:6	RO	0x0	reserved
5:0	RW	0x00	AL_FRE_OP3 Setting the AL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP3 as the AL setting of the PHY when the freq == 2'b11.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.

DDRPHY_REG3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x00	CL_FRE_OP0 Setting the CL/RL vlaue of the PHY for frequency point 0.When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b00. For LPDDRn,this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
23:22	RO	0x0	reserved
21:16	RW	0x00	CL_FRE_OP1 Setting the CL/RL vlaue of the PHY for frequency point 1.When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b01. For LPDDRn,this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
15:14	RO	0x0	reserved
13:8	RW	0x00	CL_FRE_OP2 Setting the CL/RL vlaue of the PHY for frequency point 2.When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b10. For LPDDRn,this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
7:6	RO	0x0	reserved
5:0	RW	0x00	CL_FRE_OP3 Setting the CL/RL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b11. For LPDDRn,this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.

DDRPHY_REG4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	CWL_FRE_OP0 Setting the CWL/WL vlaue of the PHY for frequency point 0. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn,this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.
23:22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	CWL_FRE_OP1 Setting the CWL/WL vlaue of the PHY for frequency point 1. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn,this register should keep the same WL setting with the SDRAM.For DDRn, this register should keep the same CWL setting with the SDRAM.
15:14	RO	0x0	reserved
13:8	RW	0x00	CWL_FRE_OP2 Setting the CWL/WL vlaue of the PHY for frequency point 2. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn,this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.
7:6	RO	0x0	reserved
5:0	RW	0x00	CWL_FRE_OP3 Setting the CWL/WL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn,this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.

DDRPHY_REG5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	reg_fb1xclk_invdela Used to adjust the hold timing of the digital to analog interface.When increase this register, it will increase the hold time of the digital to analog interface.
23:0	RO	0x000000	reserved

DDRPHY_REG6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	reg_cmd_ph90en_b The command 90 degree control signal. High means eanble the command 90 degree conrol and low means the disalbe the command 90 degree control. [0]:A0 [1]:A1 [2]:A2 [3]:A3 [4]:A4 [5]:A5 [6]:A6 [7]:A7 [8]:A8 [9]:A9 [10]:A10 [11]:A11 [12]:A12 [13]:A13 [14]:A14 [15]:A15 [16]:A16 [17]:A17 [18]:ACTN [19]:BA0 [20]:BA1 [21]:BG0 [22]:BG1 [23]:CK [24]:CKB [25]:CKE0 [26]:CSB0 [27]:CSB1 [28]:ODT0 [29]:ODT1 [30]:CKE1 [31]:RESETN [7]:RESETN

DDRPHY_REG7

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	reg_rx_lock_code_bp_en The rx dll lock value bypass. Active High. 1'b1: use the dll lock value from the register reg_rx_lock_code_bp_value[7:0]. 1'b0: use the dll lock value from dll module automatically.
26	RW	0x0	reg_tx_lock_code_bp_en The tx dll lock value bypass. Active High. 1'b1: use the dll lock value from the register reg_tx_lock_code_bp_value[7:0]. 1'b0: use the dll lock value from dll module automatically.
25:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23	RW	0x1	reg_vt_comp_bp The rx vt compensation disable signal. Active High. 1'b1: Disable the rx vt compensation function. 1'b0: Enable the rx vt compensation funciton.
22	RW	0x1	reg_cmdout_mux The timing control of the command path between the digital part and analog part. 1'b1: The command signal from the digital part to the analog part is align to the posedge of the dfi_clk1x. 1'b0: The command signal from the ditial part to the analog part is align to the negedge of the dfi_clk1x.
21	RW	0x0	ph90en_bp The 90 degree control bypass enable signal of the command path. In the normal mode, the 90 degree control of the command path is setting automatically based on the sdram type. The user also can use this register to choose the bypass mode, then use the register reg_cmd_ph90en_bp to control the 90 degree of each command pad. 1'b1: Choose the bypass mode. 1'b0: Choose the auto mode.
20	RW	0x0	ph90en_bp_dq The 90 degree control bypass enable signal of the data path.In the normal mode, the 90 degree control of the data path is setting automatically based on the sdram type. The user also can use this register to choose the bypass mode, then use the register reg_a/b/c_l/h_dq_ph90en_bp ,reg_a/b/c_l/h_dqs_ph90en_bp to control the 90 degree of each dq pad. 1'b1: Choose the bypass mode. 1'b0: Choose the auto mode.
19	RW	0x0	reg_rden_bypass Then enable signal of the rx fifo read control bypass mode.High is valid. 1'b0: Disable the bypass mode. 1'b1: Enable the bypass mode and use the reg_rden_delay to control the rx fifo read timing.

Bit	Attr	Reset Value	Description
18:16	RW	0x2	reg_rden_delay This register is used to control read timing of the rx fifo when enable the rx fifo read control bypass mode. When the dfi_rddata_en change to high, the phy will read out the rxdata from the rx fifo afther the following delay. 0:9+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 1:10+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 2:11+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 3:12+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 4:13+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 5:14+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 6:15+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 7:16+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) For auto mode, the delay =11+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel).
15	RO	0x0	reserved
14	RW	0x0	reg_rdodt_bypass The bypass enable signal of the rx odt bypass function. When enable this function, the user can use the register reg_a/b/c_l/h_rdodt0/1/2/3_delay[2:0](eg reg_a_l_rdodt0_delay[2:0]),reg_a/b/c_l/h_rdodt0/1/2/3_ophsel[2:0],reg_a/b/c_l/h_rdodt0/1/2/3_dllsel[4:0] to adjust the timing of the rx odt .
13	RW	0x0	reg_rxodt_st_bypass The enable signal of the rx odt start point bypass mode, when enable this function , using the register reg_rxodt_stdelay to control the start point of the rx odt. High is valid.
12	RO	0x0	reserved
11:8	RW	0x0	reg_rxodt_stdelay Using to control the rx odt start point when enable the rx odt start point bypass mode(reg_rxodt_st_bypass).Decrease this value will left shift the rx odt window, increase this value will right shift the rx odt window. Unit:dfi_clk1x.For auto mode, the start_point = (RL-1)>>1.
7:4	RW	0x2	reg_rxodt_length Used to control the length of the RX ODT. The step is 1x clock cycle.When the value +1, the length of RX ODT will increase 1x clock cycle.Related register 0x00f.It combines with the register reg_rxodt_start_point to decide the range of the RX ODT.The default RX ODT length is 4*dfi_clk1x cycles.

Bit	Attr	Reset Value	Description
3:0	RW	0x3	reg_rxodt_start_poi Used to control the start point of the RX ODT. When the value +1, the start point of RX ODT will increase 1x clock cycle. If the user wants to keep the length of the RX ODT unchanged, the users need to increase 1x clock cycle of the length of the RX ODT using the register reg_rxodt_length. The default RX ODT start point is RL-2 in regard to the read command.

DDRPHY_REG8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:15	RW	0x1	reg_cat_rank_num Define the rank number of the command bus train should support. 2'b00: Two ranks. 2'b10: rank 0. 2'b01: rank 1. Others: Not support
14:13	RW	0x3	reg_cat_channel_nu The command channel enable signal of command bus train.High is valid. 2'b11: Enable Channel A and Channel B. 2'b01: Only enable Channel A. 2'b10: Only enable Channel B
12:8	RW	0x00	reg_clk_div_cnt This register is used to control the divider of the dfi_clk1x which used for the initialization of the SDRAM and command bus training.The dfi_clk1x will be clock divided to the low speed based on this register. Tclkinit = Tdfi_clk1x/(2*reg_clk_div_cnt).
7:6	RW	0x0	reg_cat_bp_rank_s Used to choose the rank when enable the bypass command bus train or only enable one rank of auto command bus train. 2'b10: Choose the Rank0 to do the command bus train. 2'b01: Choose the Rank1 to do the command bus train.
5	RW	0x0	reg_cat_bp_cmd_send Used to send the command bus train command when enable the command bus training bpass mode. Posedge is valid.When this signal change from low to high, it will send the command bus train command to the SDRAM. The command bus value depends on the reg_cat_bp_mode, reg_cat_cs_train_value and reg_ca_train_value
4	RW	0x0	reg_cat_bp_mode Choose the command bus train stage for the byass mode. 1'b0: Current is CS bypass command bus train. 1'b1: Current is CA bypass command bus train.
3	RW	0x0	reg_cat_bp_en The Bypass command bus train enable signal. High is valid.When this bit set to high, the command path will choose the command bus train module and the tx delay line of command will be controlled by the register directly through the logic in the command bus training logic.

Bit	Attr	Reset Value	Description
2	RW	0x0	reg_cat_bp_start The Bypass command bus train start signal. High is valid.When this bit set to high, the command bus module will go into the bypass command bus train flow.
1	RW	0x0	reg_cat_start The Auto command bus train start signal. High is valid.When this signal enable, it will begin the command bus train.
0	RW	0x0	reg_cat_enable The Auto command bus train enable signal. High is valid.When this signal enable, the command path will switch to the command bus train module.

DDRPHY_REG9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x04	reg_txcbt Used to control the timing parameter tcs_VREF/tCKCKEH/tMRZ. The delay should >= MAX(1.5ns,2nCK)
24:20	RW	0x0f	reg_tadr Used to control the check time of the read back data from the DQ. The delay should >= 20ns
19:15	RW	0x04	reg_tckelck Used to control the clock and command valid after CKE low(tCKELCK). The delay should >= max(7.5ns,3nCK)
14:10	RW	0x01	reg_tdstrain Data Setup/Hold for Vref(CA) Training Mode.
9:5	RW	0x0f	reg_tmrw Used to control the delay between the MRW command and valid clock/CS requirement after CKE input LOW after MRW command. The delay >= MAX(14ns, 10nCK).
4:0	RW	0x1c	reg_tcacd Used to control the CA Bus Training Command to CA Bus Training Command Delay(tCACD). The delay should >= RU(20ns/tCK).

DDRPHY_REG10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x28	reg_tvrefca_long Used to control the Vref(CA) step time
15:8	RW	0x0f	reg_tcaent Used to control the first CA Bus Training Command following CKE Low(tCAENT). The delay should >= 25
7:0	RW	0x1f	reg_tfc Used to control the frequency set point switching time(tFC). The delay should >= 250ns.

DDRPHY_REGA

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	reg_mr1 Used to control the LPDDR4 load mode value of MR1 when command bus train.
23:16	RW	0x00	reg_mr2 Used to control the LPDDR4 load mode value of MR2 when command bus train.
15:8	RW	0x00	reg_mr3 Used to control the LPDDR4 load mode value of MR3 when command bus train
7:0	RW	0x00	reg_mr11 Used to control the LPDDR4 load mode value of MR11 when command bus train.

DDRPHY_REGB

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	reg_mr13 Used to control the LPDDR4 load mode value of MR13 when command bus train.
15:8	RW	0x00	reg_mr14 Used to control the LPDDR4 load mode value of MR14 when command bus train.
7:0	RW	0x00	reg_mr22 Used to control the LPDDR4 load mode value of MR22 when command bus train.

DDRPHY_REGC

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	reg_cat_vref_scan_ Disable the CA_VREF train when do the Auto command but train. High is valid . 1'b1: Only scan the timing window of the CA and CS based on the current CA_VREF setting. 1'b0: Will scan the CA_VREF to find the best point.
29:24	RW	0x3f	reg_cat_vref_scan_ Set the max value that the Vref train. When the Vref scan arrive to the reg_cat_vref_scan_max, it will stop the Vref scan.
23:22	RO	0x0	reserved
21:16	RW	0x00	reg_cat_vref_scan_min Set the min value that the perbit skew train. The tx delay line scan will start from this delay point
15:0	RO	0x0000	reserved

DDRPHY_REGD

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RW	0x8	reg_cs_perbit_skew_offset_fsp0 The FSP[0] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
27:24	RW	0x8	reg_cs_perbit_skew_offset_fsp1 The FSP[1] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
23:20	RW	0x8	reg_cs_perbit_skew_offset_fsp2 The FSP[2] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
19:16	RW	0x8	reg_cs_perbit_skew_offset_fsp3 The FSP[3] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI
15:12	RW	0x1	reg_lpddr4_ca_odt When enable the register control mode of CA ODT, the PHY will use this register to control the CA_ODT.
11	RW	0x0	reg_lpddr4_ca_odt_sel Choose the CA ODT control mode in LPDDR4 mode. 1'b1: Use the register reg_lpddr4_ca_odt[1:0] to control. 1'b0: Use the dfi_odt to control.
10:8	RW	0x1	reg_cat_vref_scan_steps Used to control the CA_VREF scan steps. When the reg_cat_vref_scan_disable is set to 1'b0 to open the CA_VREF scan mode, the use can use this register to control the scan steps to decrease the scan time.
7	RW	0x0	reg_cs_pwc_disable The disable signal of pulse width control of CS. High is valid. For command bus train, when the PHY do the command bus train of CS, if enable the pulse width control function, the pulse width will decrease 25% for command bus train. Before enter command bus train and after exit command bus train, the pulse width of CS will keep the normal pulse width.

Bit	Attr	Reset Value	Description
6	RW	0x1	reg_cat_skip_fspy For the command bus train, the user can choose to set the FSP[Y](assume that the current is FSP[X]) at the low speed based on the setting in the register (reg_mr1~regmr22). This register is used to control to enable this function or not. 1'b1: Enable the function to set the FSP[Y] before the command bus train. 1'b0: Disable the function to set the FSP[Y]] before the command bus train. When the user chooses this mode, the user need to set the FSP[Y] before to enable the command bus trian. Note: For the first time of high speed command bus training, the phy will complete the sdram initialization and skip this operation automatically.
5:4	RW	0x0	reg_cat_fspy_rank If the user chooses to set the FSP[Y] in the command bus train flow by set tingthe reg_cat_ske_fspy = 1'b0, the use can use this register to choose the RANK which need to be set. 2'b00: Choose RANK0 and RANK1. 2'b01: Choose Rank1. 2'b10: Choose Rank0. 2'b11: Disable the setting.
3	RO	0x0	reserved
2	RW	0x0	reg_cat_skip_cs_train The disable signal to skip the cs train flow of the auto command bus train. 1'b1: Skip the CS train and go to the ca training directly. 1'b0: Begin the CS train firstly and go to the ca training.
1	RW	0x0	reg_cmd_perbit_skew_bp The tx delay line of the command pad bypass enable signal. 1'b1: For LPDDR4 mode, it can use the register to control the tx delay line of the command pad. 1'b0: For LPDDR4 mode, it will use the command bus training module to control the tx delay line of the command pad. Note: For other sdram types, the tx delay line is always control by the register directly. This register is unsed.
0	RW	0x0	reg_ca_perbit_skew Used to update the perbit skew of the command in the command bus train module through the registers. Posedge is valid. When this signal change from low to high, it will update the perbit skew value setting by the register to the command bus train module according to the current frequency point.

DDRPHY_REGE

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0xff	reg_cat_ca_scan_max Set the max value that the perbit skew train. When the perbit skew scan arrive to the reg_cat_ca_scan_max, it will stop the tx delay line scan of the command.
15:14	RO	0x0	reserved
13:8	RW	0x15	reg_cat_ca_train_value The signal is used to control the CA command bus train pattern. The user can use this register to control the training patter for CA command bus train.

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:0	RW	0x06	reg_cat_cs_train_value The signal is used to control the CS command bus train pattern. The user can use this register to control the command bus train patter for cs train stage.

DDRPHY_REGF

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x06	reg_cha_cat_cs_check_value The check pattern of cs train mode for channel A
23:22	RO	0x0	reserved
21:16	RW	0x06	reg_chb_cat_cs_check_value The check pattern of cs train mode for channel B.
15:14	RO	0x0	reserved
13:8	RW	0x15	reg_cha_cat_ca_check_value The check pattern of ca train mode for channel A.
7:6	RO	0x0	reserved
5:0	RW	0x15	reg_chb_cat_ca_check_value The check pattern of ca train mode for channel B.

DDRPHY_REG10

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	reg_freq_choose_t Used for Fast Frequency Changing. Valid only when reg_freq_choose_bypass is high. 2'b00: Freq Point 0. 2'b01: Freq Point 1. 2'b10: Freq Point 2. 2'b11: Freq Point 3. In the normal mode, the current frequency point is set by the dfi_frequency[4:0] at the initialization and frequency change. If the user want to change the current working frequency or update the registers which used to control other frequency points. The user can use this register to set the frequency point firstly. After choose the freq point using this register, the user can switch the training result belong to this freq point fastly
29	RW	0x0	reg_lpddr4_rd_prea Choose the read preamble mode when PHY is in LPDDR4 mode. 1'b0: Static. 1'b1: Toggle

Bit	Attr	Reset Value	Description
28	RW	0x0	reg_wl_freq_update The data tx delay line control value update signal. Active high. In the default mode, the tx delay line is controlled by the write-levevling/write training result according to the frequency point. If the user wants to change the value to adjust the delay line, the user can use the bypass registers (invdelay_t) that show in the Table "Data Perbit De-skew Control Registers For TX And RX" to set the value and set this signal i°1i±. Then the bypass register value will be updated to the control register of the tx perbit skew base on the current frequency point.Please reference the section "4.4.3 Data Per-bit phase tuning Control" to get more information. Note: Please recover to i°0i± after the setting
27	RW	0x0	reg_calib_freq_upd The RX DQS Gating control value update signal. Active high.In the default mode, after the RX DQS Gating, the training value will control the RX DQS Gating delay. If the user wants to change the value to adjust the RX DQS Gating window,the user can use the bypass registers that show in the "Table the related register of bypass-mode DQS gating calibration to set the control value". If this bit set to i°1i±, then the setting value will be update to the control register of the RX DQS Gating base on the current frequency point.Please reference the section "4.5.2.2 Bypass RX DQS"gating trainto get more information. Note: Please recover to i°0i± after the setting
26:25	RO	0x0	reserved
24	RW	0x0	reg_calib_mode_sel The DQS-Gating model sel. 1’b1: Use the Read Preamble Training mode (Only used for DDR4). 1’b0: Use the Normal Read mode (Can used for DDR2/3/4 and LPDDR2/3).When the DQS Gating mode chooses the Normal Read mode for DDR4, the Read DQS will be pulling down to 1i¯b0. So the register reg_a/b/c_l/h_weakpub_reg[1:0] should set to 2’b00 to pull down the Read DQS when it is in i°high zi± state.
23:13	RO	0x000	reserved
12	RW	0x0	bist_ck_select The register used to choose the clk which used to sample the bist command when enable the phy noraml bist. 1’b1: Choose the feedback signal from the CK pad as the clock. 1’b0: Choose the feedback signal from the CKB pad as the clock
11:0	RO	0x000	reserved

DDRPHY_REG11

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	reg_ram_vref1_pd The power down signal of RAM VREF. 1’b1: Power Down. 1’b0: Open. Not used in this design
11:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x3f	reg_mpr_cnt Used to control the timing of the MPR command for DDR4 rx dqs calibration.Timing interval between MPR = reg_mpr_cnt * dficlk1x.

DDRPHY_REG12

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x40	reg_max_rdvalue Use to set the max number of the read command when do the DQS Gating. When the read commands are more than the max number, it is the DQS Gating Error and this state can be read from the register 0x91[5]
15:0	RW	0x1000	reg_calib_timeout The bit[15:0] of the timer used for DQS Gating. When the clock cycle exceed the bits[15:0] of the timer, it is the DQS Gating Error and this state can be read from the register calib_error.

DDRPHY_REG13

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x1	reg_rrankdly_4x_dec The delay control signal of the read rank switch. Unit: dfi_clk4x. 1'b1: Decrease 1 dfi_clk4x delay for the read rank switch 1'b0: Keep current state.
9:8	RO	0x0	reserved
7	RW	0x0	reg_rdrank_delay_bp The bypass mode of read rank switch point at 4x clock cycle precision. The user can use the register 0xa6 and 0xd6 to adjust the read rank switch point
6:3	RO	0x0	reserved
2:0	RW	0x1	reg_wrrank_1xdly The delay control signal of the write rank witch. Unit:dfi_clk1x.

DDRPHY_REG14

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_cmd0_wrap_sel The pin wrap sel of pad A0 for DDRn/LPDDRn
23:21	RO	0x0	reserved
20:16	RW	0x01	reg_cmd1_wrap_sel The pin wrap sel of pad A1 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x02	reg_cmd2_wrap_sel The pin wrap sel of pad A2 for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x03	reg_cmd3_wrap_sel The pin wrap sel of pad A3 for DDRn/LPDDRn

DDRPHY_REG15

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	reg_cmd4_wrap_sel The pin wrap sel of pad A4 for DDRn/LPDDRn
23:21	RO	0x0	reserved
20:16	RW	0x00	reg_cmd5_wrap_sel The pin wrap sel of pad A5 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x06	reg_cmd6_wrap_sel The pin wrap sel of pad A6 for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x07	reg_cmd7_wrap_sel The pin wrap sel of pad A7 for DDRn/LPDDRn

DDRPHY_REG16

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x08	reg_cmd8_wrap_sel The pin wrap sel of pad A8 for DDRn/LPDDRn
23:21	RO	0x0	reserved
20:16	RW	0x09	reg_cmd9_wrap_sel The pin wrap sel of pad A9 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x0a	reg_cmd10_wrap_sel The pin wrap sel of pad A10 for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x0b	reg_cmd11_wrap_sel The pin wrap sel of pad A11 for DDRn/LPDDRn

DDRPHY_REG17

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0c	reg_cmd12_wrap_s The pin wrap sel of pad A12 for DDRn/LPDDRn
23:21	RO	0x0	reserved
20:16	RW	0x0d	reg_cmd13_wrap_s The pin wrap sel of pad A13 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x0e	reg_cmd14_wrap_sel The pin wrap sel of pad A14 for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x0f	reg_cmd15_wrap_s The pin wrap sel of pad A15 for DDRn/LPDDRn

DDRPHY_REG18

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x10	reg_cmd16_wrap_s The pin wrap sel of pad A16 for DDRn/LPDDRn
23:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x11	reg_cmd17_wrap_s The pin wrap sel of pad 170 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x12	reg_cmd18_wrap_s The pin wrap sel of pad ACTN for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x13	reg_cmd19_wrap_s The pin wrap sel of pad BA0 for DDRn/LPDDRn

DDRPHY_REG19

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x14	reg_cmd20_wrap_s The pin wrap sel of pad BA1 for DDRn/LPDDRn
23:21	RO	0x0	reserved
20:16	RW	0x15	reg_cmd21_wrap_s The pin wrap sel of pad BG0 for DDRn/LPDDRn
15:13	RO	0x0	reserved
12:8	RW	0x16	reg_cmd22_wrap_s The pin wrap sel of pad BG1 for DDRn/LPDDRn
7:5	RO	0x0	reserved
4:0	RW	0x17	reg_cmd23_wrap_s The pin wrap sel of pad CK for DDRn/LPDDRn

DDRPHY_REG1A

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x18	reg_cmd24_wrap_s The pin wrap sel of pad CKB for DDRn/LPDDRn
23:0	RO	0x000000	reserved

DDRPHY_REG1D

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00008101	reg_cke_ck_cmd_p Because the phy supports the command reamp, so the ck/cke may remap to the other pads, so the user need to use this register to tell the phy which pad is ck/cke. For the ck/cke output pad, the bits should set to 1'b1. [0]:A0 [1]:A1 [2]:A2 [3]:A3 [4]:A4 [5]:A5 [6]:A6 [7]:A7 [8]:A8 [9]:A9 [10]:A10 [11]:A11 [12]:A12 [13]:A13 [14]:A14 [15]:A15 [16]:A16 [17]:A17 [18]:ACTN [19]:BA0 [20]:BA1 [21]:BG0 [22]:BG1 [23]:CK [24]:CKB [25]:CKE0 [26]:CSB0 [27]:CSB1 [28]:ODT0 [29]:ODT1 [30]:CKE1 [31]:RESETN

DDRPHY_REG1E

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	reg_pllfbdiv_dqcmd The control signal of feedback div signal
15:9	RO	0x00	reserved
8:4	RW	0x00	reg_pllprediv_dqcmd Internal PLL charge bump work frequency adjusts, it can be used to adjust PLL band width, 5i¯h1 has maximum band width. Please reference the section 4.8 to get more information of PLL.
3:0	RO	0x0	reserved

DDRPHY_REG1F

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	reg_lockenb_dqcmd The power down enable signal of the pll. Active low. 1'b0: Enable the pll. 1'b1: Disalbe the pll
5:2	RO	0x0	reserved
1	RW	0x1	reg_pllclkouten_dqcmd_t The clock output enable signal of pll. Active high
0	RW	0x1	reg_pllpd_dqcmd_t Internal PLL power down. Set to i°0i± to enable the PLL.

DDRPHY_REG20

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x1	reg_train_reg_update_en Disable the clock gate of the train logic. Active high. 1'b1: It will enable the clock of the train logic. 1'b0: Automatically gate the clock when the train logic is in idle state. If the users wants to use the register to update the training result through the bypass mode. This register should set to 1'b1 to enable the clock of the training control logic, then the bypass value can be updated to the lock register
17	RW	0x1	reg_dqclken_t The enable signal of clock for DQ path in the analog circuit.This signal will be used to disable the clk of the DQ module to save the power when the DDR2/3/4 SDRAM goes to power down mode. 1'b1: Keep the clock of the DQ path in the analog circuit. 1'b0: Gate the clock of the DQ path in the analog circuit
16	RW	0x1	reg_outclken The gating control signal of 1x clock of PHY. Active Low. 1'b0: It will gate the 1x clock of the PHY. 1'b1: The 1x clock of the PHY will be gate automatically in dfi low power mode.
15	RW	0x0	reg_lp_bypass The dfi low power disable signal. When set to high, it will ignore the signals of dfi low power interface.
14	RW	0x1	reg_deep_lp_en The deep low power mode enable signal. 1'b1: Enable the deep low power. 1'b0: Disable the deep low power
13	RO	0x0	reserved
12	RW	0x1	reg_lp_vref_ctrl_en Disable the bypass mode of the VREF control. 1'b1: Using auto mode the disable VREF at dfi low power mode. 1'b0: Using the register 0x114[4]/0x124[4]/0x134[4]/0x144[4] to disable the VREF.
11:8	RW	0x9	reg_lp_wakeup_threhold Configure the low power mode threshold.When the dfi_lp_wakeup<= threshold, it will go into the normal low power mode; when dfi_lp_wakeup> threshold, it will go into the deep low power mode.

Bit	Attr	Reset Value	Description
7:6	RW	0x1	reg_lp_io_dis_ctrl Adjust the timing from disable the IO to disable the clock when begin the low power flow.
5	RW	0x1	reg_lp_dq_clk_ctrl_ Choose the control mode of the DQ clock path when in low power mode. 1'b1: Auto mode. 1'b0: Bypass mode. Use the register 0x00[1] to control.
4	RW	0x1	reg_lp_dig_rst_ctrl_en Choose the control mode of the reset of the digital core. 1'b1: Auto mode. 1'b0: Not reset.
3	RW	0x1	reg_lp_spll_clktree_
2	RW	0x1	reg_lp_dig_clk_ctrl_en Choose the control mode of the clock of the digital core. 1'b1: Auto mode. 1'b0: Not close.
1	RW	0x1	reg_lp_io_ctrl_en Choose the control mode of the IO. 1'b1: Auto mode. 1'b0: Not close.
0	RW	0x1	reg_lp_pllpd_ctrl_en Choose the power down mode of the PLL. 1'b1: Auto mode. 1'b0: Not power down.

DDRPHY_REG21

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x1	reg_lp_stvalue The response timing when high the dfi_lp_ack. Unit: dfi_clk1x.
19:16	RW	0x6	reg_lp_ackvalue The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x.
15:0	RW	0x1388	reg_wait_cnt The bit[7:0] of pll lock wait signal. There are two ways to generate the pll lock. The first way is using the pll_lock from the pll module directly, the second way is using the counter to calcuate the cycle after enable the pll.For the second way, after enable the pll, the phy will start to count until the counter equal the reg_wait_cnt[15:0], the high the pll lock.The bit[15:8] of pll lock wait signal. There are two ways to generate the pll lock. The first way is using the pll_lock from the pll module directly, the second way is using the counter to calcuate the cycle after enable the pll.For the second way, after enable the pll, the phy will start to count until the counter equal the reg_wait_cnt[15:0], the high the pll lock.

DDRPHY_REG22

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:20	RW	0x1ff	reg_zq_chg_interval The timing interval of the zqcalib training value changing when we do the zq calibration.Unit: dfi_clk1x
19	RO	0x0	reserved
18:10	RW	0x03f	reg_pu_interval The timing interaval of the zqcalib between the pull down training state to pull up training state. Unit:dfi_clk1x.
9:4	RO	0x00	reserved
3	RW	0x1	reg_pd_zqcali The power down signal of zqcalib module when enable the zqcalib function. 1'b1: Power down mode. 1'b0: Normal work mode.
2	RW	0x0	reg_zqcali_clear The clean signal of zqcalib module. High is valid.
1	RW	0x0	reg_zqcali_bypass The bypass enable of zqcalib function. Active high. 1'b1: The phy will use the register reg_drvlegn_zqcali/reg_drvlegpb_zqcali/reg_odtlegn_zqcali/reg_odtlegpb_zqcali to control zqcalib. 1'b0: It will use the zqcali module to control
0	RW	0x0	reg_zqcali_en The enable signal of zqcalib function.

DDRPHY_REG23

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0e	reg_drvlegpd_zqcali The drivier pull-down value when reg_zqcali_bypass set to 1'b1 to enable the zqcalib bypass function.
23:21	RO	0x0	reserved
20:16	RW	0x0e	reg_drvlegpu_zqcali The drivier pull-up value when reg_zqcali_bypass set to 1'b1 to enable the zqcalib bypass function.
15:13	RO	0x0	reserved
12:8	RW	0x07	reg_odtlegpd_zqcali The odt pull-up value when reg_zqcali_bypass set to 1'b1 to enable the zqcalib bypass function.
7:5	RO	0x0	reserved
4:0	RW	0x07	reg_odtlegpu_zqcali The odt pull up value when reg_zqcali_bypass set to 1'b1 to enable the zqcalib bypass function.

DDRPHY_REG24

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	reg_rd_train_perdef_en The enable signal of the read predef training, predefine Mode. 1'b1: Enable the predef train of the read train. 1'b0: Exit the predef train of the read train

Bit	Attr	Reset Value	Description
13	RW	0x0	reg_train_vref_en The enable signal of the vref training. 1'b1: Enable the vref train of the read train(predefine mode)/write train. 1'b0: Exit the vref train of the read train(predefine mode)/write train.reuse for rd perdef training and wr training
12	RW	0x0	reg_ddr4_dbi
11:8	RW	0x0	reg_rdtrain_cs_sel Choose the rank of the read train. 4'b0111: Choose Rank3. 4'b1011: Choose Rank2. 4'b1101: Choose Rank1. 4'b1110: Choose Rank0
7	RW	0x0	reg_rx_vref_value_update
6	RW	0x0	reg_rd_train_dqs_ra
5	RW	0x0	reg_bypass_rd_train_cmd_start_en Generate the read train command wh training mode. High pulse valid. en enable bypass read
4	RW	0x0	reg_bypass_rd_train_en Enable the bypass read train function. 1'b1: Enable the read train bypass mode. 1'b0: Disable the read train bypass mode.
3	RW	0x0	reg_rd_train_check_value_en Choose the check value of the read train. 1'b0: Use the fix mode. DDR3 = 8i_b10101010 LPDDR3 = 16i_hcc55 LPDDR4 = MR#40,MR#32 DDR4 = 8i_haa/8i_hcc/8i_hf0/8i_h00 1'b1: Use the register to configure
2	RW	0x0	reg_rd_train_freq_update
1	RW	0x0	reg_dqs_rd_train_en
0	RW	0x0	reg_dq_rd_train_en The enable signal of the read training Auto Mode. 1'b1: Enable the auto train of the read train. 1'b0: Exit the auto train of the read train.

DDRPHY_REG25

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	reg_lpddr4_mr15_value The load mode value of MR15 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rdtraining
23:16	RW	0x55	reg_lpddr4_mr20_value The load mode value of MR20 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.

Bit	Attr	Reset Value	Description
15:8	RW	0x5a	reg_lpddr4_mr32_value The load mode value of MR32 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.
7:0	RW	0x3c	reg_lpddr4_mr40_value The load mode value of MR40 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.

DDRPHY_REG26

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_ddr4_mr4_value Used to control the DDR4 load mode value of MR4 when the register reg_calib_mode_sel = 1'b1, when ddr4 calib, set this register as current SDRAM MR4(A15~A0) value. The calib operation will write new data to the MR4, so we should keep the other bits the same with the current MR4
15:8	RO	0x00	reserved
7:0	RW	0x00	reg_ddr4_mr3 Used to control the DDR4 load mode value of MR3 when read training(MPR), when ddr4 read training, set this register as current SDRAM MR3(A10~A3) value. The read training operation will write new data to the MR3, so we should keep the other bits the same with the current MR3.

DDRPHY_REG27

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x1	reg_wrtrain_lpddr4_vref_range Choose the adjust range of SDRAM's vref,reference to JESD-LPDDR4
23:16	RW	0x00	reg_pbit_deskew_offset_for_lpddr4 The tx delay line adjust signal of the DQS/DQSB after the write-leveling.The tx delay line value will equal the write-leveing result+reg_pbit_deskew_offset_for_lpddr4 and apply to the DQ/DM
15:12	RO	0x0	reserved
11	RW	0x0	reg_dqs_wr_train_en The enable signal of the DQS Scan. When this bit set to i°1i±, it will enable adjust the DQS to find the best window of the DQ. Only used for debug, because it will change the write-leveling result if the user enable the write leveling function.
10	RW	0x0	reg_wrtrain_check_data_value_random_gen 1'b1: PHY generate random data and write to SDRAM during write training. 1'b0: the user config dq0-7_train_check_data_value0-9 and PHY write it (10*BL8) to SDRAM during write training.
9:6	RW	0x0	reg_wrtrain_cs_sel Choose the rank of the write train. 4'b0111: Choose Rank3. 4'b1011: Choose Rank2. 4'b1101: Choose Rank1. 4'b1110: Choose Rank0

Bit	Attr	Reset Value	Description
5	RW	0x0	reg_wr_train_rst The wr train fsm clear signal. 1'b1: Reset the write train fsm. 1'b0: Keep the current state.
4	RO	0x0	reserved
3	RW	0x0	reg_wr_train_dqs_range_bypass The enable signal to setting the DQS scan range using the register.(wr training) 1'b1: Enable to use the register to set the DQS scan range. 1'b0: Use the default DQS scan range[0~6'h3f].
2	RO	0x0	reserved
1	RW	0x0	reg_dq_wr_train_en The enable signal of the write training Auto Mode. 1'b1: Enable the auto train of the read train. 1'b0: Exit the auto train of the read train.
0	RW	0x0	reg_dq_wr_train_auto Choose the mode of the write train. 1: Choose the write train auto mode,you should set it to 1'b1 before write train

DDRPHY_REG28

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	reg_wr_train_ba_addr The bit[2:0] of bank address for write/read operation in DDR3/4 and LPDDR3 write training mode.](reuse for rd perdef training and wr training)
27:26	RO	0x0	reserved
25:16	RW	0x000	reg_wr_train_col_addr The bit[7:0] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.](reuse for rd perdef training and wr training)The bit[9:8] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training)
15:0	RW	0x0001	reg_wr_train_row_addr The bit[7:0] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training)The bit[15:8] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training)

DDRPHY_REG29

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:18	RW	0x0960	reg_phy_trefi The value is Trefi/dfi_clk1x
17:8	RW	0x08c	reg_phy_trfc he register is used to control the auto-refresh interval when the phy do the training. The reg_phy_trfc[9:0] = reg0x4e[7:6],reg0x57[7:0]. The auto-refresh interval = reg_phy_trfc *Tdfi_clk1x.The bit9 and bit 8 of the reg_phy_trfc. The reg_phy_trfc is used to control the interval of the auto-refresh.The PHY will send the auto-refresh when it is in the training mode. Auto-refresh interval = reg_phy_trfc* Tdfi_clk1x

Bit	Attr	Reset Value	Description
7:4	RW	0x8	reg_max_refi_cnt this register used in wr/rd training,if you set reg_phy_refresh_en to 1'b1. this register means how many auto refresh cmd can be accumulated at one time.the maximum is 8,and the larger the value ,the less time training takes.
3:1	RO	0x0	reserved
0	RW	0x0	reg_phy_refresh_en When you want to enable phy auto refresh function in training, you should set this reg to 1 at frist.

DDRPHY_REG2A

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	reg_freq_choose_b The bypass signal of the freq point choose. Active High. 1'b1: It will use the reg_freq_choose_t to choose the freq point. 1'b0: The phy will choose the freq point based on the dfi_freqeuncy at the phy initialization and fast frequency change.
3	RO	0x0	reserved
2	RW	0x0	reg_pll_lock_bypass Choose the way to wait for the pll lock after the pll enable. 1'b0: Wait the pll lock from the pll module. 1'b1: Wait the pll lock by enable the pll lock counter after the pll enable
1	RW	0x0	reg_pllpd_bypass Choose the way to control the pll pd signal of the pll module. 1'b1: Only can use the register to control. 1'b0: Automatically control in the dfi low power mode.
0	RW	0x0	reg_lpddr4_write_postamble_sel The write postamble control signal of the LPDDR4 mode.Please keep the same setting with the LPDDR4 MR1[7]. 1'b1:1.5*tCK. 1'b0:0.5*tCK

DDRPHY_REG2B

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_a7_lp4x_en when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_a7_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_a6_lp4x_en when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_a6_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_a5_lp4x_en when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_a5_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_a4_lp4x_en when use lpddr4x ,this register should be set to 1.
8	RW	0x1	reg_a4_pvt_comp_en enable the pvt compensation function

Bit	Attr	Reset Value	Description
7	RW	0x0	reg_a3_lp4x_en when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_a3_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_a2_lp4x_en when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_a2_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a1_lp4x_en when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_a1_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a0_lp4x_en when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_a0_pvt_comp_en enable the pvt compensation function

DDRPHY_REG2C

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_a15_lp4x_en when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_a15_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_a14_lp4x_en when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_a14_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_a13_lp4x_en when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_a13_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_a12_lp4x_en when use lpddr4x ,this register should be set to 1.
8	RW	0x1	reg_a12_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_a11_lp4x_en when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_a11_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_a10_lp4x_en when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_a10_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a9_lp4x_en when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_a9_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a8_lp4x_en when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_a8_pvt_comp_en enable the pvt compensation function

DDRPHY_REG2D

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_resetn_lp4x_en when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_resetn_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_bg1_lp4x_en when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_bg1_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_bg0_lp4x_en when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_bg0_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_ba1_lp4x_en when use lpddr4x ,this register should be set to 1.
8	RW	0x1	reg_ba1_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_ba0_lp4x_en when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_ba0_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_actn_lp4x_en when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_actn_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a17_lp4x_en when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_a17_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a16_lp4x_en when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_a16_pvt_comp_en enable the pvt compensation function

DDRPHY_REG2E

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_odt1_lp4x_en when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_odt1_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_odt0_lp4x_en when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_odt0_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_csb1_lp4x_en when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_csb1_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_csb0_lp4x_en when use lpddr4x ,this register should be set to 1.

Bit	Attr	Reset Value	Description
8	RW	0x1	reg_csb0_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_cke1_lp4x_en when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_cke1_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_cke0_lp4x_en when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_cke0_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_ckb_lp4x_en when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_ckb_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_ck_lp4x_en when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_ck_pvt_comp_en enable the pvt compensation function

DDRPHY_REG2F

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x1	reg_pllpostdiv_ls The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
27	RW	0x1	reg_pllpostdiven_ls The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
26:19	RO	0x00	reserved
18	RW	0x0	reg_cmd_delay_one_ui delay the cmd for one ui,base on the cmd 2t mode(reg_cmd_2t_mode=1).
17	RW	0x0	reg_cmd_2t_mode enable cmd 2t mode
16	RW	0x0	reg_phy_sdram_initial initial the sdram through phy. When lpddr4 ca training, register should be set to 1'b1, phy will initial the sdram itself
15:8	RW	0x60	reg_wl_dqs_start_point write leveling's dqs tx delay start point
7:1	RW	0x3f	reg_rd_train_dqs_scan_max the max rx dqs delay when do rd training dqs scan.
0	RW	0x0	reg_pvt_comp_dis disable pvt compensation fuction

DDRPHY_REG31

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:24	RW	0x64	reg_ddrc_treset_h_x1024 when lpddr4 initial , reset need keep high 2ms, so this register's value = 2ms/(1024*dfi1xclk)
23:16	RW	0x1f	reg_ddrc_treset_l_x1024 when lpddr4 initial , phy need to wait 2us, so this register's value = 2us/(1024*dfi1xclk)
15:8	RW	0x1f	reg_ddrc_tckeh when lpddr4 initial , this register's value = tckeh/(32*dfi1xclk)
7:0	RW	0x1f	reg_ddrc_tzqlat when lpddr4 initial , this register's value = tzqlat/(dfi1xclk)

DDRPHY_REG32

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5f	reg_ddrc_tzqinit when lpddr4 initial , this register's value = tzqinit/(dfi1xclk)

DDRPHY_REG33

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	reg_pllpostdiv_fsp3 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
27	RW	0x0	reg_pllpostdiven_fsp3 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
26:23	RO	0x0	reserved
22:20	RW	0x0	reg_pllpostdiv_fsp2 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.

Bit	Attr	Reset Value	Description
19	RW	0x0	reg_pllpostdiven_fsp2 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
18:15	RO	0x0	reserved
14:12	RW	0x0	reg_pllpostdiv_fsp1 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
11	RW	0x0	reg_pllpostdiven_fsp1 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
10:7	RO	0x0	reserved
6:4	RW	0x0	reg_pllpostdiv_fsp0 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
3	RW	0x0	reg_pllpostdiven_fsp0 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
2:0	RO	0x0	reserved

DDRPHY_REG34

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	reg_rx_lock_code_bp_value when reg_rx_lock_code_bp_en=1 , the value of register reg_rx_lock_code_bp_value is dll lock value
15:8	RW	0x00	reg_tx_lock_code_bp_value when reg_tx_lock_code_bp_en=1 , the value of register reg_tx_lock_code_bp_value is dll lock value

Bit	Attr	Reset Value	Description
7:0	RW	0x08	reg_pvt_comp_req_wait_cnt when phy send a pvt req(dfi_phymstr_req),it need get a pvt ack(dfi_phymstr_ack) from ctrl, this register is used to change the time of timeout

DDRPHY_REG36

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	reg_osc_sel The osc select signal. 1'b0: transform reg_invdelaysel_osc_reg with dll decode 1'b1: Choose the register reg_invdelaysel_osc_reg directly
9:8	RO	0x0	reserved
7:0	RW	0x80	reg_invdelaysel_osc_reg used to measure the delay capability of invdealysel

DDRPHY_REG37

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	reg_cmd_drv_zqcalib_en The comand driver control signal. 1'b1: Choose the zqcalibration result as the control signal. 1'b0: Choose the register as the conrol signal.
15	RW	0x0	reg_cmd_fbsel_reg The phy bist command path seletc signal. 1'b1: Choose to arrive the pad. 1'b0: Choose the interal as the end.
14	RW	0x0	reg_cmd_fben_reg The phy bist cmmand feebback enable signal. Active high. Just used for debug.
13	RW	0x1	reg_cmd_abutweak_pub_reg The enable signal of CMD PAD weak pull up. Active Low.
12:8	RW	0x00	reg_cmd_abutslewpu_reg CMD/CK rising edge slew rate control, larger value means larger risign slew rate.
7:6	RO	0x0	reserved
5	RW	0x0	reg_cmd_abutweakpd_reg The enable signal of CMD PAD weak pull down. Active high.
4:0	RW	0x00	reg_cmd_abutslewpd_reg CMD/CK falling edge slew rate control, larger value means larger falling slew rate.

DDRPHY_REG38

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	reg_cmd_abutnrco The pull-down resistance of CK and CKB.The resistance relation with the configuration show in the table "CMD driver strength table

Bit	Attr	Reset Value	Description
11	RW	0x1	reg_cmd_abutnrcomp3_ck0_reg The pull-down resistance of CK and CKB.The resistance relation with the configuration show in the table "CMD driver strength table"
10	RW	0x1	reg_cmd_abutnrcomp2_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in the table "CMD driver strength table"
9	RW	0x1	reg_cmd_abutnrcomp1_ck0_reg The pull The resistance relation with the configuration show in the -down resistance of CK and CKB. table "CMD driver strength table"
8	RW	0x0	reg_cmd_abutnrcomp0_ck0_reg The pull The resistance relation with the configuration show in the -down resistance of CK and CKB.table "CMD driver strength table"
7:5	RO	0x0	reserved
4	RW	0x0	reg_cmd_abutprcomp4_ck0_reg The pull The resistance relation with the configuration show in the -up resistance of CK and CKB. table "CMD driver strength table"
3	RW	0x1	reg_cmd_abutprcomp3_ck0_reg The pull The resistance relation with the configuration show in the -up resistance of CK and CKB.table "CMD driver strength table
2	RW	0x1	reg_cmd_abutprcomp2_ck0_reg The pull The resistance relation with the configuration -up resistance of CK and CKB. show in the table "CMD driver strength table"
1	RW	0x1	reg_cmd_abutprcomp1_ck0_reg The pull The resistance relation with the configuration show in the -up resistance of CK and CKB.table "CMD driver strength table"
0	RW	0x0	reg_cmd_abutprcomp0_ck0_reg The pull The resistance relation with the configuration show in the -up resistance of CK and CKB. table "CMD driver strength table"

DDRPHY_REG3B

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_a0_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_a1_invdelayse_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x80	reg_a2_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_a3_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG3C

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_a4_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_a5_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x80	reg_a6_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_a7_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG3D

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_a8_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_a9_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x80	reg_a10_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_a11_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG3E

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_a12_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_a13_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x80	reg_a14_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_a15_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG3F

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_a16_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_a17_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x80	reg_ba0_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_ba1_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG40

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_bg0_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_bg1_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x50	reg_cke0_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_cke1_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG41

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_ckb_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_ck_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x50	reg_odt0_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_odt1_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG42

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	reg_csb0_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:17	RO	0x00	reserved
16	RW	0x0	reg_csb1_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256
15:8	RW	0x50	reg_resetn_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256
7:0	RW	0x80	reg_actn_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256

DDRPHY_REG54

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq0_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
23:16	RW	0xa5	dq0_train_check_dada_value1 For the write training of DDR4, it is the data pattern of the second burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

Bit	Attr	Reset Value	Description
15:8	RW	0xc3	dq0_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8
7:0	RW	0x3c	dq0_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

DDRPHY_REG55

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq0_train_check_data_value4 For the write training of DDR4, it is the data pattern of the first burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

Bit	Attr	Reset Value	Description
23:16	RW	0x55	dq0_train_check_dada_value5 For the write training of DDR4, it is the data pattern of the second burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
15:8	RW	0x00	dq0_train_check_data_value6 For the write training of DDR4, it is the data pattern of the third burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8
7:0	RW	0xaa	dq0_train_check_data_value7 For the write training of DDR4, it is the data pattern of the fourth burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

DDRPHY_REG56

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0xf0	dq0_train_check_data_value8 For the write training of DDR4, it is the data pattern of the third burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8
7:0	RW	0x0f	dq0_train_check_data_value9 For the write training of DDR4, it is the data pattern of the fourth burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

DDRPHY_REG57

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq1_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

Bit	Attr	Reset Value	Description
23:16	RW	0xa5	dq1_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
15:8	RW	0xc3	dq1_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0x3c	dq1_train_check_data_value3 For the write training of DDR4, it is the data pattern of the second burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read traiing of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

DDRPHY_REG58

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq1_train_check_data_value4 For the write training of DDR4, it is the data pattern of the eighth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

Bit	Attr	Reset Value	Description
23:16	RW	0x55	dq1_train_check_data_value5 For the write training of DDR4, it is the data pattern of the eighth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
15:8	RW	0x00	dq1_train_check_data_value6 For the write training of DDR4, it is the data pattern of the eighth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0xaa	dq1_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

DDRPHY_REG59

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	dq1_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0x0f	dq1_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which wiil be writen to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

DDRPHY_REG6C

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x14	reg_wrtrain_vref_wait_vref_cnt_50ns the register is used in write train, if you enable tx vref scan function, you need to configure this register.When set a new tx vref value to sdram , we should wait 100-250ns ,then it works, you should set this register tell PHY how long is 50ns,then the phy have a reference.So the regi_s value = 50ns/dfi_1xclk
23:21	RW	0x1	reg_train_vref_step_min the register is used in read predef train or write train, if you enable vref scan function, you can configure this register.this register means How many step at a time, when doing A fine vref scanning.

Bit	Attr	Reset Value	Description
20:16	RW	0x08	reg_train_vref_step_max the register is used in read predef train or write train, if you enable vref scan function, you can configure this register.this register means How many step at a time, when doing A rough vref scanning
15:10	RW	0x14	reg_cmd_invdelaysel_sel The command tx delay line value obs signal. The user can use this register to get the current control value of each command pad. 1'b0:A0 1'b1:A1
9:0	RW	0x140	reg_rdtrain_wait_vref_valid_cnt the register is used in read predef train,if you enable rx vref scan function,you need to configure this register. When set a new rx vref value,we should wait 800ns,then it works.So the reg's value = 800ns/dfi_1xclk

DDRPHY_REG6E

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x3f	reg_rd_train_dq_scan_max control the scan range of dq's rd training

DDRPHY_REG7C

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	train_all_step_done The complete signal of the write training/rd perdef training.Active high.The user need to wait this bit change to high after enable the write training. (reuse for rd perdef training and wr training)
6	RO	0x0	train_step1_delay_done The compelte signal of the delay scan before the vref scan when write training/rd perdef training. Active high.(reuse for rd perdef training and wr training)
5	RO	0x0	train_step2_vref_doone The compelte signal of the vref scan when write training/rd perdef training. Active high. (reuse for rd perdef training and wr training)
4	RO	0x0	train_step3_delay_done The compelte signal of the delay scan after the vref scan when write training/rd perdef training. Active high. (reuse for rd perdef training and wr training)
3	RO	0x0	train_step1_error
2	RO	0x0	train_step2_error when train done,you need to check this register.this reg's value equal to 1'b1 means step2 have error in rd perdef training or write training.(reuse for rd perdef training and wr training)
1	RO	0x0	train_step3_error

Bit	Attr	Reset Value	Description
0	RO	0x0	train_true_done The complete signal of the read training(mpr/mpc mode).Active high.

DDRPHY_REG7D

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	halfui_lock_code_to_reg dll lock value
23:1	RO	0x000000	reserved
0	RO	0x0	lock_pll_dqcmd The lock signal of the pll. Active high. The pll will be locked in 5000 reference clock cycles after the pd operation.

DDRPHY_REG7E

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	drvlegpd_zqcali_2reg The zqclibration result of driver pull down after the zqcalib training.
23:21	RO	0x0	reserved
20:16	RO	0x00	drvlegpu_zqcali_2reg The zqclibration result of driver pull up after the zqcalib training.
15:13	RO	0x0	reserved
12:8	RO	0x00	odtlegpd_zqcali_2reg The zqclibration result of odt pull down after the zqcalib training.
7:5	RO	0x0	reserved
4:0	RO	0x00	odtlegpu_zqcali_2reg The zqclibration result of odt pull up after the zqcalib training.

DDRPHY_REG7F

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	reg_zqcali_done The complete signal of the zacalib training. Active high.
3	RO	0x0	reg_drvpd_overflow The fail flag of driver pull down zacalib trraining. Active high.
2	RO	0x0	reg_drvpu_overflow The fail flag of driver pull up zacalib trraining. Active high.
1	RO	0x0	reg_odtpd_overflow The fail flag of odt pull down zacalib trraining. Active high.
0	RO	0x0	reg_odtpu_overflow The fail flag of odt pull up zacalib trraining. Active high.

DDRPHY_REG83

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12:8	RO	0x00	wl_done_byte The write leveling complete signal of each channel. Active high. [0]: The write leveling complete of byte0. [1]: The write leveling complete of byte1. [2]: The write leveling complete of byte2. [3]: The write leveling compelte of byte3. [4]: The write leveling compelte of byte4
7	RO	0x0	reserved
6	RO	0x0	calib_end The rx dqs calib complete signal. Active high. Only change to 1'b1 when all open channel have compelte the rx dqs calibration.
5	RO	0x0	calib_error The error flag of the rx dqs calib. Active high.
4:0	RO	0x00	calib_done_byte The rx dqs calib complete signal of each channel. Active high. [0]: The rx dqs calib complete of byte0. [1]: The rx dqs calib complete of byte1. [2]: The rx dqs calib complete of byte2. [3]: The rx dqs calib compelte of byte3. [4]: The rx dqs calib compelte of byte4.

DDRPHY_REG84

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RO	0x0	cha_rank_cat_bp_cmd_send_rdy [0]:The reay signal of the command bus training bypass mode of channel b RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode. [1]:The reay signal of the command bus training bypass mode of channel a RANK1. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode.

Bit	Attr	Reset Value	Description
17:16	RO	0x0	chb_rank_cat_bp_cmd_send_rdy [0]:The reay signal of the command bus training bypass mode of channel b RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode. [1]:The reay signal of the command bus training bypass mode of channel a RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode.
15:14	RO	0x0	cha_rank_cat_bp_done [0]:The command bus training bypass mode compelte signal of channel b RANK1. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to "1". Then the user can set the reg_cat_bp_en to exit the command bust train mod [1]:The command bus training bypass mode compelte signal of channel a RANK1. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to "1". Then the user can set the reg_cat_bp_en to exit the command bust train mode.
13:12	RO	0x0	chb_rank_cat_bp_d [0]:The command bus training bypass mode compelte signal of channel b RANK0. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to "1". Then the user can set the reg_cat_bp_en to exit the command bust train mod [1]:The command bus training bypass mode compelte signal of channel a RANK0. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to "1". Then the user can set the reg_cat_bp_en to exit the command bust train mode.

Bit	Attr	Reset Value	Description
11:0	RO	0x000	ca_check_value [5:0]:The command bus train read back data from the dq[5:0] of channel a when enable the command bus train bypass mode. When enable the command bus train bypass mode and go into the comand bus train mode, if the phy send the CBT command, the dq will read back the data on the command bus through, the read back data will be stored in this register. The user can use this register to get the read back data and judge the curren tx delay line is right or not. [6:11]:The command bus train read back data from the dq[5:0] of channel b when enable the command bus train bypass mode. When enable the command bus train bypass mode and go into the comand bus train mode, if the phy send the CBT command, the dq will read back the data on the command bus through, the read back data will be stored in this register. The user can use this register to get the read back data and judge the curren tx delay line is right or not

DDRPHY_REG85

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	cha_cat_auto_cs_train_err The auto command bus cs train error flag of channel a. [0]: The training result of csb for rank0 is abnormal if enable the cs train. [1]: The training result of csb for rank1 is abnormal if enable the cs train. [2]: Can't find the vref pass window of channel a csb for rank0 if enable the cs train. [3]: Can't find the vref pass window of channel a csb for rank1 if enable the cs train. [4]: Can't find the tx delay line pass window of channel a csb for rank0 if enable the cs train. [5]: Can't find the tx delay line pass window of channel a csb for rank1 if enable the cs train. [6]: The start point of the channel a CSB0 training is abnormal if enable the cs train. The training will be fail. [7]: The start point of the channel a CSB1 training is abnormal if enable the cs train. The training will be fail.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	chb_cat_auto_cs_train_err The auto command bus cs train error flag of channel b. [0]: The training result of csb for rank0 is abnormal if enable the cs train. [1]: The training result of csb for rank1 is abnormal if enable the cs train. [2]: Can't find the vref pass window of channel b csb for rank0 if enable the cs train. [3]: Can't find the vref pass window of channel b csb for rank1 if enable the cs train. [4]: Can't find the tx delay line pass window of channel b csb for rank0 if enable the cs train. [5]: Can't find the tx delay line pass window of channel b csb for rank1 if enable the cs train. [6]: The start point of the channel b CSB0 training is abnormal if enable the cs train. The training will be fail. [7]: The start point of the channel b CSB1 training is abnormal if enable the cs train. The training will be fail.
7:4	RO	0x0	reserved
3	RO	0x0	cha_cat_done The auto command bus train complete signal of channel a. Active high.
2	RO	0x0	chb_cat_done The auto command bus train complete signal of channel b. Active high
1	RO	0x0	cha_cat_bp_cmd_send_done The flag of channel b that the phy compelte to send the CBT command when enable the command bus training bypass mode. Active high. The user needs to wait this bit change to 1'b1 when it prepares to send the next CBT command
0	RO	0x0	chb_cat_bp_cmd_send_done The flag of channel a that the phy compelte to send the CBT command when enable the command bus training bypass mode. Active high. The user needs to wait this bit change to 1'b1 when it prepares to send the next CBT command.

DDRPHY_REGAD

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RO	0x00	reg_rd_train_readback_data_valid_byte The readback data valid signal when enable the read training bypass mode. Active High. When enable the read training bpass mode, after send out the read command and the read back data will be received by the phy and store in the following registers. When this bit is high, it means the read back data is valid. [0]: The read back data valid signal of byte0. [1]: The read back data valid signal of byte1. [2]: The read back data valid signal of byte2. [3]: The read back data valid signal of byte3. [4]: The read back data valid signal of byte4

Bit	Attr	Reset Value	Description
19:15	RO	0x00	reg_train_done_for_rd_to_reg The done signal of read train for byte0 to byte4. Active high. [0]: The done signal of the read train for byte0. [1]: The done signal of the read train for byte1. [2]: The done signal of the read train for byte2. [3]: The done signal of the read train for byte3. [4]: The done signal of the read train for byte4
14:10	RO	0x00	reg_train_error_for_rd_byte The error signal of read train for byte0 to byte4. Active high. [0]: The error signal of the read train for byte0. [1]: The error signal of the read train for byte1. [2]: The error signal of the read train for byte2. [3]: The error signal of the read train for byte3. [4]: The error signal of the read train for byte4.
9:5	RO	0x00	reg_wr_train_done_byte The done flag of the write training for byte0 to byte4. High means done. [0]: The done flag of the write training for byte0. [1]: The done flag of the write training for byte1. [2]: The done flag of the write training for byte2. [3]: The done flag of the write training for byte3. [4]: The done flag of the write training for byte4
4:0	RO	0x00	reg_wr_train_error_byte The error flag of the write training for byte0 to byte4. High means error. [0]: The error flag of the write training for byte0. [1]: The error flag of the write training for byte1. [2]: The error flag of the write training for byte2. [3]: The error flag of the write training for byte3. [4]: The error flag of the write training for byte4

1.4.3 Registers Summary For DDR Monitor

Name	Offset	Size	Reset Value	Description
DDRMON_IP_VERSION	0x0000	W	0x00000023	DDR Monitor IP Version
DDRMON_CTRL	0x0004	W	0x00000008	DDR Monitor Control Register
DDRMON_INT_STATUS	0x0008	W	0x00000000	Interrupt Status
DDRMON_INT_MASK	0x000C	W	0x00000000	Interrupt mask control
DDRMON_TIMER_COUNT	0x0010	W	0x00000000	The DFI Timer Threshold
DDRMON_FLOOR_NUMBER	0x0014	W	0x00000000	The Low Threshold in the Comparison of DDR Access
DDRMON_TOP_NUMBER	0x0018	W	0x00000000	The High Threshold in the Comparison of DDR Access
DDRMON_DFI_ACT_NUM	0x001C	W	0x00000000	DFI Active Command Number
DDRMON_DFI_WR_NUM	0x0020	W	0x00000000	DFI Write Command Number
DDRMON_DFI_RD_NUM	0x0024	W	0x00000000	DFI Read Command Number
DDRMON_COUNT_NUM	0x0028	W	0x00000000	Timer Count Number
DDRMON_DFI_ACCESS_NUM	0x002C	W	0x00000000	DFI Read And Write Command Number
DDRMON_TOP_LP_NUMBER	0x0030	W	0x00000000	The High Threshold In The Comparison Of DDR Cke Low
DDRMON_FLOOR_LP_NUMBER	0x0034	W	0x00000000	The Low Threshold In The Comparison Of DDR Cke Low
DDRMON_DFI_SREX_NUM	0x0038	W	0x00000000	Number Of Cke Low For DFI Self-refresh

Name	Offset	Size	Reset Value	Description
DDRMON_DFI_PDEX_NUM	0x003C	W	0x00000000	Number Of Cke Low For DFI Power Down
DDRMON_DFI_CLKSTOP_NUM	0x0040	W	0x00000000	Number Of Cke Low For DFI Clkstop
DDRMON_DFI_LP_NUM	0x0044	W	0x00000000	Total Number Of Cke Low
DDRMON_DFI_PHY_LP_NUM	0x0048	W	0x00000000	DDR Phy Low Power
DDRMON_IF_CTRL	0x0200	W	0x00000000	DDR Interface Control Register
DDRMON_MSTID	0x0204	W	0x00000000	Master And AXI ID Of DDR Command
DDRMON_IDMSK	0x0208	W	0x00000000	Master And AXI ID MASK Of DDR Command
DDRMON_WR_START_ADDR	0x020C	W	0x00000000	Write Start Address
DDRMON_WR_END_ADDR	0x0210	W	0x00000000	Write End Address
DDRMON_RD_START_ADDR	0x0214	W	0x00000000	Read Start Address
DDRMON_RD_END_ADDR	0x0218	W	0x00000000	Read End Address
DDRMON_FIFO0_ADDR	0x0240	W	0x00000000	DDR Controller Interface Address FIFO0
DDRMON_FIFO0_ID	0x0244	W	0x00000000	DDR Controller Interface Command ID FIFO0
DDRMON_FIFO1_ADDR	0x0248	W	0x00000000	DDR Controller Interface Address FIFO1
DDRMON_FIFO1_ID	0x024C	W	0x00000000	DDR Controller Interface Command ID FIFO1
DDRMON_FIFO2_ADDR	0x0250	W	0x00000000	DDR Controller Interface Address FIFO2
DDRMON_FIFO2_ID	0x0254	W	0x00000000	DDR Controller Interface Command ID FIFO2
DDRMON_FIFO3_ADDR	0x0258	W	0x00000000	DDR Controller Interface Address FIFO3
DDRMON_FIFO3_ID	0x025C	W	0x00000000	DDR Controller Interface Command ID FIFO3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

1.4.4 Detail Registers Description

DDRMON_IP_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x23	ip_version DDR monitor IP version

DDRMON_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:8	RO	0x00	reserved
7:6	RW	0x0	rank_cs_num define the rank number for monitor 2'b01 1 rank 2'b10 2 rank other value: 4 rank
5	RW	0x0	ddr4_en 1'b1: Enable 1'b0: Disable
4	RW	0x0	lpddr4_en 1'b1: Enable 1'b0: Disable
3	RW	0x1	hardware_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	lpddr23_en Enable lpddr2 or lpddr3 1'b1: Enable 1'b0: Disable
1	RW	0x0	software_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	timer_cnt_en 1'b1: Enable 1'b0: Disable

DDRMON_INT_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
12	RO	0x0	rd_addr_hit This is the interrupt status read address hit the setting range.
11	RO	0x0	wr_addr_hit This is the interrupt status write address hit the setting range.
10	RO	0x0	over_int_phylp This is the interrupt status of DDR PHY LP number over than high threshold. Only valid for lpddr2/lpddr3/lpddr4.
9	RO	0x0	below_int_phylp This is the interrupt status of DDR PHY LP number less than low threshold. Only valid for lpddr2/lpddr3/lpddr4.
8	RO	0x0	over_int_clkstop This is the interrupt status of DDR clk stop number over than high threshold. Only valid for lpddr2/lpddr3/lpddr4.
7	RO	0x0	below_int_clkstop This is the interrupt status of DDR clk stop number less than low threshold. Only valid for lpddr2/lpddr3/lpddr4.

Bit	Attr	Reset Value	Description
6	RO	0x0	over_int_pdex This is the interrupt status of DDR power down number over than high threshold.
5	RO	0x0	below_int_pdex This is the interrupt status of DDR power down number less than low threshold.
4	RW	0x0	compare_statistics This is the interrupt status to statistics the number of activate, write or read command and so on.
3	RW	0x0	over_int_srex This is the interrupt status of DDR self refresh number over than high threshold.
2	RW	0x0	below_int_srex This is the interrupt status of DDR self refresh number less than low threshold.
1	RO	0x0	over_int This is the interrupt status of DDR read and write burst number more than high threshold.
0	RO	0x0	below_int This is the interrupt status of DDR read and write burst number less than low threshold.

DDRMON_INT_MASK

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:11	RO	0x00	reserved
10	RW	0x0	rd_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
9	RW	0x0	wr_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
8	RW	0x0	over_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
7	RW	0x0	below_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
6	RO	0x0	over_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
5	RO	0x0	below_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

Bit	Attr	Reset Value	Description
4	RW	0x0	compare_statistics_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
3	RW	0x0	over_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x0	below_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RO	0x0	over_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RO	0x0	below_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_TIMER_COUNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	timer_count The timer counter threshold, the statistics of DDR access only be done when timer counter is less then this threshold in hardware mode, in OSC clock cycle.

DDRMON_FLOOR_NUMBER

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_number The low threshold in the comparison of DDR access.

DDRMON_TOP_NUMBER

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_number The high threshold in the comparison of DDR access.

DDRMON_DFI_ACT_NUM

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_act_num DFI active command number in the statistics range.

DDRMON_DFI_WR_NUM

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wr_num DFI write command number in the statistics range.

DDRMON_DFI_RD_NUM

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rd_num DFI read command number in the statistics range.

DDRMON_COUNT_NUM

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_count_num The DFI counter number in the statistics range, in DDR clock cycle.

DDRMON_DFI_ACCESS_NUM

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_access_num DFI read and write command number in the statistics range.

DDRMON_TOP_LP_NUMBER

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_lp_number The high threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_FLOOR_LP_NUMBER

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_lp_number The low threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_DFI_SREX_NUM

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srex_num DFI self-refresh number during cke low.

DDRMON_DFI_PDEX_NUM

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_pdex_num DFI power down number during cke low.

DDRMON_DFI_CLKSTOP_NUM

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_clkstop_num DFI clkstop number during cke low. Only valid for lpddr2/3/4.

DDRMON_DFI_LP_NUM

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_lp_num The sum of DFI self-refresh, power down and clkstop number during cke low.

DDRMON_DFI_PHY_LP_NUM

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_num Phy low power count number during the time both dfi_lp_req and dfi_lp_ack assert.

DDRMON_IF_CTRL

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:3	RO	0x0000	reserved
2	RW	0x0	if_mon_en 1'b1: Enable 1'b0: Disable
1	RO	0x0	reserved
0	RW	0x0	direction 1'b1: Read 1'b0: Write

DDRMON_MSTID

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_mstid High 7 bits: Master ID Low 10 bits: AXI command ID

DDRMON_IDMSK

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_idmsk When bit set to high, this bit of MSTID will be masked, and does not take part in the ID comparison.

DDRMON_WR_START_ADDR

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr Write start address for address comparison.

DDRMON_WR_END_ADDR

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr Write end address for address comparison.

DDRMON_RD_START_ADDR

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr Read start address for address comparison.

DDRMON_RD_END_ADDR

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr Read end address for address comparison.

DDRMON_FIFO0_ADDR

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo0_addr DDR controller interface address FIFO0.

DDRMON_FIFO0_ID

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo0_id DDR controller interface command ID FIFO0.

DDRMON_FIFO1_ADDR

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo1_addr DDR controller interface address FIFO1.

DDRMON_FIFO1_ID

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo1_id DDR controller interface command ID FIFO1.

DDRMON_FIFO2_ADDR

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo2_addr DDR controller interface address FIFO2.

DDRMON_FIFO2_ID

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo2_id DDR controller interface command ID FIFO2.

DDRMON_FIFO3_ADDR

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo3_addr DDR controller interface address FIFO3.

DDRMON_FIFO3_ID

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo3_id DDR controller interface command ID FIFO3.

1.4.5 Registers Summary For HWFFC

Name	Offset	Size	Reset Value	Description
HWFFC_HWFFC_EN	0x0000	W	0x00000000	HWFFC enable register
HWFFC_HWFFC_MODE	0x0004	W	0x00000000	HWFFC mode
HWFFC_HWFFC_CTRL	0x0008	W	0x00000000	HWFFC control
HWFFC_HWFFC_INT_STATUS	0x000C	W	0x00000000	Int status
HWFFC_HWFFC_CNT	0x0010	W	0x00000000	Count
HWFFC_HWFFC_INT_EN	0x0014	W	0x00000000	Int Enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

1.4.6 Detail Registers Description

HWFFC_HWFFC_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	hwffc_en 1'b0 diable hwffc function 1'b1 enable hwffc function, this bit should be configured at the last of a sequence of a software operations.

HWFFC_HWFFC_MODE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	hwffc_mode To choose hwffc mode, which are 2'b00 automode 2'b01 semi-auto mode 2'b11 sw mode The differences of 3 modes are: Auto mode send hwffc request to ddrc and switch clock automatically. Semi-auto mode send hwffc request to ddrc automatically but clock switch is handle by software. In SW mode, software controls sending request to ddrc and clock switch.

HWFFC_HWFFC_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	hwffc_clk_switch_sw when bit10 of HWFFC_CTRL=1, hardware clk_switch value = hwffc_clk_switch_sw

Bit	Attr	Reset Value	Description
10	RW	0x0	clk_switch_sw_en 1'b1 hardware clk_switch value equals to hwffc_clk_switch_sw(bit 11 of HWFFC_CTRL) 1'b0 disable this function
9	RW	0x0	clk_switch_semi_en 1'b1 hardware clock switch is enabled for semi-auto mode 1'b0 hardware clock switch is not enabled for semi-auto mode
8	RW	0x0	clk_switch_auto_en 1'b1: hardware clock switch is enabled for auto mode 1'b0: hardware clock switch is not enabled for auto mode
7	RW	0x0	ignore_phy_ready 1'b0: after clock switch, wait a phy ready signal and continue 1'b1: Do not wait phy ready signal when hwffc
6	RW	0x0	hwffc_clk_switch_load Only used in auto mode or semi-auto mode The initial value of cru switch signal
5	RW	0x0	hwffc_clk_switch_init Only used in auto mode or semi-auto mode 1'b1: load the initial value of cru switch signal, which is a mux select pin of a clock switch. 1'b0: Disable loading
4	RW	0x0	csysreq_ddrc_sw Only used in SW mode When in SW mode, configure this bit to send csysreq_ddrc request to the controller. 1'b0: send request 1'b1: not send request
3	RW	0x0	csysdiscamdrain_ddrc Disable CAM draining for DDRC Hardware Fast Frequency Change. When asserted, Self-Refresh can be entered without draining CAM. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1).
2:1	RW	0x0	csysrequency_ddrc Target frequency for DDRC Hardware Fast Frequency Change. This signal is effective only when Hardware Fast Frequency Change is requested (that is, csysreq_ddrc=0 and csysmode_ddrc=1).
0	RW	0x0	csysmode_ddrc The csysmode_ddrc value DDRC Hardware Fast Frequency Change mode. 1'b0: Hardware Low-Power is requested 1'b1: Hardware Fast Frequency Change is requested

HWFFC_HWFFC_INT_STATUS

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	csysack_ddrc DDRC Hardware Low-Power Request Acknowledge. Acknowledgement from the peripheral (DDRC) of a system low-power request.
2	RO	0x0	csysack_ddrc DDRC Hardware Low-Power Clock Active. Indicates that the peripheral (DDRC) requires its clock signal

Bit	Attr	Reset Value	Description
1	RC/W1C	0x0	hwffc_done_int 1'b1: a hwffc done interrupt is detected 1'b0: no hwffc done interrupt is detected
0	RC/W1C	0x0	hwffc_clk_switch_int 1'b1: a clock switch interrupt is detected 1'b0: no clock switch interrupt is detected

HWFFC_HWFFC_CNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwffc_cnt only used for auto mode How many ddrc clock cycle wait during clk switch, in case of pll lock issue.

HWFFC_HWFFC_INT_EN

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	hwffc_done_int_en 1'b1: enable hwffc done interrupt 1'b0: diable hwffc done interrupt
0	RW	0x0	hwffc_clk_switch_int_en 1'b1: enable hwffc clock switch interrupt 1'b0: diable hwffc clock switch interrupt

1.5 Interface Description

DDR IOs from DDR PHY are listed as following Table.

Table 1-1DDR IO description

Pin Name	Description
CK	Positive differential clock
CKB	Negative differential clock
CKE	Active-high clock enable signal for two chip select.
CSBi (i=0,1)	Active-low chip select signal. There are two chip select.
ACTN	Activation command input.
BA[1:0] BG[1:0]	Bank address signal. For DDR3, BA0 should connect to the BA0. BA1 should connect to BA1. BG0 should connect to BA2. For DDR4, please connect directly. Unused for LPDDRn.
A[17:0]	Address signal.
DQ[31:0]	Bidirectional data line
DQS[3:0]	Positive differential bidirectional data strobes
DQSB[3:0]	Negative differential bidirectional data strobes.
DM[3:0]	Active-low data mask signal.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RESETN	Reset signal.

The DDR PHY supports more than one SDRAM type and the command pad of DDR PHY is named in the format of DDR4. The PHY supports different command map for different SDRAM type and also supports to use the register to control the map between the commands, and then the user can be very conveniently to design the Combo Memory System based on the different command map function. The default command map relationship shows in the following table. When the user uses the mem_select[2:0](reg01[2:0])to choose the memory type, thecommand will change to the default command map. The user should accord to the following table to connectthe

command pad to the SDRAM pad.

Table 1-2 DDR IO Mapping Table

CMD PAD OF PHY (DDR4)	DDR3	LPDDR3	LPDDR3 4RANK	LPDDR4	LPDDR4 4rank
A0	A9	-	-	CK_B	CK_2
A1	A2	-	-	-	-
A2	A4	A6	A6	CA1_A	CA1_A
A3	A3	-	CSB2	CKE1_A	CKE2
A4	BA1	A3	A3	CA3_B	CA3_B
A5	A11	A2	A2	CA5_B	CA5_B
A6	A13	A1	A1	CA1_B	CA1_B
A7	A8	-	-	ODT0_B	ODT0_B
A8	A6	A9	A9	ODT0_A	ODT0_A
A9	A5	-	-	CKB_B	CKB_2
A10	A10	-	-	CKE0_B	CKE1
A11	A7	A8	A8	CA0_A	CA0_A
A12	BA2	-	-	CA3_A	CA3_A
A13	A14	A0	A0	CA0_B	CA0_B
A14	A15	A5	A5	CA4_A	CA4_A
A15	A0	-	-	CA2_A	CA2_A
A16	RASB	A7	A7	CA5_A	CA5_A
A17	-	-	-	-	-
ACTN	CASB	-	CSB3	CKE1_B	CKE3
BA0	A1	-	-	CA2_B	CA2_B
BA1	A12	A4	A4	CA4_B	CA4_B
BG0	WEN	-	ODT3	ODT1_B	ODT2_B
BG1	BA0	-	ODT2	ODT1_A	ODT2_A
CKE	CKE	CKE	CKE	CKE0_A	CKE0
CKB	CKB	CKB	CKB	CKB_A	CKB_0
CK	CK	CK	CK	CK_A	CK_0
CSB0	ODT1	ODT0	ODT0	CSB0_A	CSB0
CSB1	CSB1	ODT1	ODT1	CSB1_A	CSB2
ODT0	ODT0	CSB1	CSB1	CSB1_B	CSB3
ODT1	CSB0	CSB0	CSB0	CSB0_B	CSB1
RESETN	RESETN	-	-	RESETN	RESETN

At the PHY top-level, the mapping relationships between the DQ pads and dfi_wrdata/dfi_rddata shows in the following table. When connecting a DDR3/DDR4/LPDDR3 memory to the interface, there is a default mapping between the DDR3/DDR4/LPDDR3 signals to the PHY top-level pins.

Table 1-3 Default DDR DQ IO Mapping Table for DDR3/DDR4/LPDDR3/LPDDR4

PHY TOP-LEVEL PINS	SDRAM	dfi_wrdata/dfi_rddata
A_DQ[7:0]	DQ[7:0]	dfi_wrdata[7:0]/dfi_rddata[7:0]
A_DQ[15:8]	DQ[15:8]	dfi_wrdata[15:8]/dfi_rddata[15:8]
B_DQ[7:0]	DQ[15:8]	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[15:8]	DQ[31:24]	dfi_wrdata[31:24]/dfi_rddata[31:24]

RK3568 support a remap feature from DFI DQ byte to SDRAM DQ byte. By default, DRAM DQ0 maps to DFI DQ0, DRAM DQ1 maps to DFI DQ1, and so on. If software wants to map DRAM DQ0 with DFI DQ1, and DRAM DQ1 map to DFI DQ2, DRAM DQ2 maps to DFI DQ3 and DRAM DQ3 map to DFI DQ0, it should configure DDR_GRF_CON3 before DRAM access.

Table 1-4 Example DDR DQ IO <-> DFI Remapping

PHY TOP-LEVEL PINS	GRF	dfi_wrdata/dfi_rddata

A_DQ[7:0]	grf_ddr_con3[9:8]=1	dfi_wrdata[15:8]/dfi_rddata[15:8]
A_DQ[15:8]	grf_ddr_con3[11:10]=2	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[23:16]	grf_ddr_con3[13:12]=3	dfi_wrdata[31:24]/dfi_rddata[31:24]
B_DQ[31:24]	grf_ddr_con3[15:14]=0	dfi_wrdata[7:0]/dfi_rddata[7:0]

1.6 Application Notes

1.6.1 Initialization

1. UMCTL2 & DDR PHY Initialization

1. Assert the resets (presetn, core_ddrc_rstn and aresetn_0 of UMCTL2)
2. Configure PLL of DDR PHY and wait PLL lock.
3. De-assert presetn if clocks are active and stable.
4. Initial UMCTL2 register and PHY Register
5. Start PHY initialization with DFIMISC[5] register of UMCTL2
6. De-assert the remaining resets (core_ddrc_rstn and aresetn_0 of UMCTL2)
7. Wait UMCTL2 initialization done (STAT.operation_mode==normal)
8. Start PHY dqs calibrationwith PHYREG2 register and wait calibration finish with PHY REG91 register.
9. (Optional) After dqs calibration, start write leveling training with PHYREG2 register and wait write leveling training finish with PHY REG92 register.
10. Start to write and read

2. DDR3/DDR3L Initialization Sequence

The initialization steps for DDR3/DDR3L SDRAMs are as follows:

1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires atleast 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR2 with INIT4.emr2 value followed byNOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS command to load MR3 with INIT4.emr3 followed by NOP/deselect for duration ofDRAMTMG3.t_mrd.
7. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration ofDRAMTMG3.t_mrd.
8. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration ofDRAMTMG3.t_mod.
9. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
10. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
11. The UMCTL2 controller is now ready for normal operation.

3. DDR4 Initialization Sequence

The initialization steps for DDR4 SDRAMs are as follows:

1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires atleast 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500 us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR3 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS (mode register set) command to load MR6 with INIT7.mr6 value followed byNOP/deselect for duration of DRAMTMG3.t_mrd.
7. Issue MRS (mode register set) command to load MR5 with INIT6.mr5 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
8. Issue MRS (mode register set) command to load MR4 with INIT7.mr4 value followed by

NOP/deselect for duration of DRAMTMG3.t_mrd.
9. Issue MRS command to load MR2 with INIT4.emr2 followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
10. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
11. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t_mod.
12. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
13. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
14. The UMCTL2 controller is now ready for normal operation.

4. LPDDR3 Initialization Sequence

The initialization steps for LPDDR3 SDRAMs are as follows:
1. Power-up.
2. CKE is held low for a duration specified by INIT0.pre_cke_x1024. The clock is checked to be stable forduration specified by INIT2.min_stable_clock_x1 (minimum of 5 clock cycles) prior to the first low tohigh transition of CKE.
3. Assert CKE for INIT0.post_cke_x1024 (specification requires at least 200 us).
4. A MRW (Reset) command is issued to MRW63 register. Values of MA<7:0> = 3FH and OP<7:0> =00H is used for this command. The MRW reset command brings the device to the device autoinitialization (resetting) state in the power-on initialization sequence.
5. Issue NOP/deselect for duration specified by INIT2.idle_after_reset_x32 (specification requires 1 usminimum) and INIT5.max_auto_init_x1024 (specification requires maximum time of 10 us).
6. An MRW ZQ initialization calibration command is issued to the memory to register MR10 to initiatethe ZQ calibration. Values of MA<7:0> = 0AH and OP<7:0>= FFH is used for this command.
7. Issue NOP/deselect for duration specified by INIT5.dev_zqinit_x32 (specification requires aminimum time of 1us).
8. Program MR2 register by setting MR2 register to INIT3.emr followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
9. Program MR1 register by setting MR1 register to INIT3.mr followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
10. Program MR3 register by setting MR3 register to INIT4.emr2 followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
11. Schedule multiple all bank refresh.
12. The UMCTL2 controller is now ready for normal operation.

5. LPDDR4 Initialization Sequence

The initialization steps for LPDDR4 SDRAMs are as follows:
1. Power-up.
2. Maintain dfi_reset_n and dfi_reset_n_ref low for duration specified by INIT1.dram_rstn_x1024.Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 2ms.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024. Specification requires at least 2 us.
5. Issue MRS (mode register set) command to load MR13 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t_mrw.
6. Issue MRS (mode register set) command to load MR1 with INIT3.mr value followed by NOP/deselect for duration of DRAMTMG3.t_mrw.
7. Issue MRS (mode register set) command to load MR2 with INIT3.emr value followed by NOP/deselect for duration of DRAMTMG3.t_mrw.
8. Issue MRS (mode register set) command to load MR3 with INIT4.emr2 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
9. Issue ZQCal Start command and wait for ZQCTL0.t_zq_long_nop.
10. Issue ZQCal Latch command and wait for ZQCTL0.t_zq_short_nop.
11. Schedule multiple refresh.

12. The UMCTL2 controller is now ready for normal operation.

1.6.2 High Speed IO Drive Strength

The register related to the CMD IO drive strength shows in the following table.

Table 1-5 The related register of the DATA IO drive strength

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
0xf4	RW	reg_cmd_abutnrcomp_reg	[28:24]	5'b01110	The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4-7 and Table 4 8.
	RW	reg_cmd_abutprcomp_reg	[20:16]	5'b01110	The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
	RW	reg_cmd_abutnrcomp_ck0_reg	[12:8]	5'b01110	The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
	RW	reg_cmd_abutprcomp_ck0_reg	[4:0]	5'b01110	The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.

The register related to the DATA IO drive strength shows in the following table.

Table 1-6 The related register of the DATA IO drive strength

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
0x304	RW	reg_a_l_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table
		reg_a_l_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table
		reg_a_l_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
		reg_a_l_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
0x484	RW	reg_a_h_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for A_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_a_h_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for A_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_a_h_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for A_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_a_h_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for A_DQ[15:8]. The resistance relation with the configuration show in table
0x604	RW	reg_b_l_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for B_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_b_l_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for B_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_b_l_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for B_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_b_l_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for B_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
0x784	RW	reg_b_h_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for B_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_b_h_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for B_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
		reg_b_h_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for B_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_b_h_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for B_DQ[15:8]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
0x904	RW	reg_c_l_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for C_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_c_l_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for C_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_c_l_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for C_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"
		reg_c_l_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for C_DQ[7:0]. The resistance relation with the configuration show in table "DQ/DQS driving strength/odt table"

Table 1-7 DDR4 CMD drive strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	22.08	23.09	24.19	25.4	ohm
pull-down	20.75	21.69	22.72	23.86	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	26.73	28.22	29.88	31.74	ohm
pull-down	25.12	26.51	28.07	29.83	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units

pull-up	72.56	84.65	101.58	126.98	ohm
pull-down	68.17	79.53	95.44	119.3	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	169.3	253.95	507.9	+∞	ohm
pull-down	159.07	238.6	477.2	+∞	ohm

Table 1-6 LPDDR4 CMD drive strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	23.53	24.6	25.77	27.06	ohm
pull-down	20.72	21.66	22.69	23.83	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	28.48	30.07	31.84	33.83	ohm
pull-down	25.08	26.47	28.03	29.78	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	77.31	90.2	108.24	135.3	ohm
pull-down	68.07	79.42	95.3	119.13	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	180.4	270.6	541.2	+∞	ohm
pull-down	158.83	238.25	476.5	+∞	ohm

Table 1-7 DDR4 DQ/DQS drive strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	22.08	23.09	24.19	25.4	ohm
pull-down	20.75	21.69	22.72	23.86	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	26.73	28.22	29.88	31.74	ohm
pull-down	25.12	26.51	28.07	29.83	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	33.86	36.28	39.07	42.33	ohm

pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	72.56	84.65	101.58	126.98	ohm
pull-down	68.17	79.53	95.44	119.3	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	169.3	253.95	507.9	+∞	ohm
pull-down	159.07	238.6	477.2	+∞	ohm

Table 1-8 LPDDR4 DQ/DQS drive strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	23.53	24.6	25.77	27.06	ohm
pull-down	20.72	21.66	22.69	23.83	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	28.48	30.07	31.84	33.83	ohm
pull-down	25.08	26.47	28.03	29.78	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	77.31	90.2	108.24	135.3	ohm
pull-down	68.07	79.42	95.3	119.13	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	180.4	270.6	541.2	+∞	ohm
pull-down	158.83	238.25	476.5	+∞	ohm

Table 1-11 LPDDR4X DQ/DQS drive strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	22.08	23.09	24.19	25.4	ohm
pull-down	20.75	21.69	22.72	23.86	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	26.73	28.22	29.88	31.74	ohm
pull-down	25.12	26.51	28.07	29.83	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm

Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	72.56	84.65	101.58	126.98	ohm
pull-down	68.17	79.53	95.44	119.3	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	169.3	253.95	507.9	+∞	ohm
pull-down	159.07	238.6	477.2	+∞	ohm

1.6.3 Command Perbit De-Skew Control

The DDR PHY supports to use the per-bit de-skew to adjust the delay of the command PAD to change the phase of the command which will be sent to the SDRAM.
For DDR4, the user can use the register to change the per-bit de-skew of the command directly.
Because the PHY supports the default command pad mapping, the user needs to change the corresponding register after the command pad mapping.
For example, if the user chooses DDR4 SDRAM mode, it can change the phase A0 directlythrough the reg_a0_invdelaysel register.The following table gives the detail description about the relationship between the control register and SDRAM PAD.

Table 1-9 The CMD Per Bit De-skew Control Map for SDRAM

NAME	ADDR	BIT	DEFAULT	SDRAM PAD			
				DDR4	DDR3	LPDDR3	LPDDR4
reg_a0_invdelaysel	0x104	[31,24]	8'h80	A0	A9	-	CK_B
reg_a1_invdelaysel		[23,16]	8'h80	A1	A2	-	-
reg_a2_invdelaysel		[15,8]	8'h80	A2	A4	A6	CA1_A
reg_a3_invdelaysel		[7,0]	8'h80	A3	A3	-	CKE1_A
reg_a4_invdelaysel	0x108	[31,24]	8'h80	A4	BA1	A3	CA3_B
reg_a5_invdelaysel		[23,16]	8'h80	A5	A11	A2	CA5_B
reg_a6_invdelaysel		[15,8]	8'h80	A6	A13	A1	CA1_B
reg_a7_invdelaysel		[7,0]	8'h80	A7	A8	-	ODT0_B
reg_a8_invdelaysel	0x10c	[31,24]	8'h80	A8	A6	A9	ODT0_A
reg_a9_invdelaysel		[23,16]	8'h80	A9	A5	-	CKB_B
reg_a10_invdelaysel		[15,8]	8'h80	A10	A10	-	CKE0_B
reg_a11_invdelaysel		[7,0]	8'h80	A11	A7	A8	CA0_A
reg_a12_invdelaysel	0x110	[31,24]	8'h80	A12	BA2	-	CA3_A
reg_a13_invdelaysel		[23,16]	8'h80	A13	A14	A0	CA0_B
reg_a14_invdelaysel		[15,8]	8'h80	A14	A15	A5	CA4_A
reg_a15_invdelaysel		[7,0]	8'h80	A15	A0	-	CA2_A
reg_a16_invdelaysel	0x114	[31,24]	8'h80	A16	RASB	A7	CA5_A
reg_a17_invdelaysel		[23,16]	8'h80	A17	-	-	-
reg_ba0_invdelaysel		[15,8]	8'h80	BA0	A1	-	CA2_B
reg_ba1_invdelaysel		[7,0]	8'h80	BA1	A12	A4	CA4_B
reg_bg0_invdelaysel	0x118	[31,24]	8'h80	BG0	WEN	-	ODT1_B
reg_bg1_invdelaysel		[23,16]	8'h80	BG1	BA0	-	ODT1_A
reg_cke0_invdelaysel		[15,8]	8'h80	CKE	CKE	CKE	CKE0_A

NAME	ADDR	BIT	DEFAULT	SDRAM PAD			
				DDR4	DDR3	LPDDR3	LPDDR4
reg_ck_invdelaysel		[7,0]	8'h80	-	-	-	-
reg_ckb_invdelaysel	0x11c	[31,24]	8'h80	CKB	CKB	CKB	CKB_A
reg_csb0_invdelaysel		[23,16]	8'h80	CK	CK	CK	CK_A
reg_odt0_invdelaysel		[15,8]	8'h80	ODT0	ODT0	CSB1	CSB1_B
reg_resetn_invdelaysel		[7,0]	8'h80	ODT1	CSB0	CSB0	CSB0_B
reg_actn_invdelaysel	0x120	[31,24]	8'h80	CSB0	ODT1	ODT0	CSB0_A
reg_cke1_invdelaysel		[23,16]	8'h80	CSB1	CSB1	ODT1	CSB1_A
reg_csb1_invdelaysel		[15,8]	8'h80	RESETN	RESETN	-	RESETN
reg_odt1_invdelaysel		[7,0]	8'h80	ACTN	CASN	-	CKE1_B

For LPDDR4, the SDRAM supports the command bus train function, so the command per-bit de-skew can be controlled by the register directly or it can be control by the command bus trainmodule. The command per-bit de-skew control path shows in the following figure.

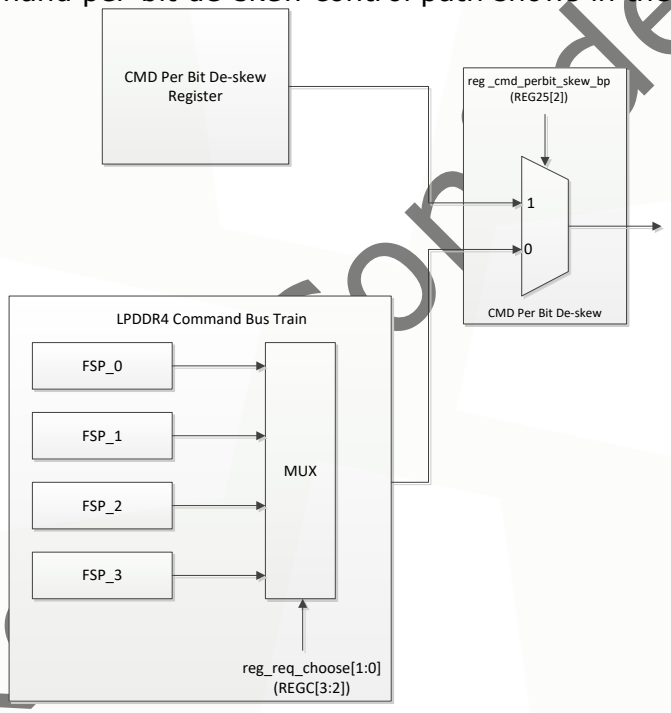


Fig.1-3 CMD Per Bit De-skew Ctrl Path of LPDDR4

After power up, apb reset and phy reset, reg_cmd_perbit_skew_bp(REG25[2]) is 1'b0. The PHY will choose the command bus train reset value to control the command per-bit de-skew. When set reg_cmd_perbit_skew_bp(REG25[2])to 1'b1, then the user can use the register to control the command per-bit de-skew directly.

The FSP_0/FSP_1/FSP_2/FSP_3 blocks in the command bus train module are used to control thecommand per-bit de-skew for different frequency groups. When enable the auto command bustrain function, the FSP_n will control the command per-bit de-skew according to the

reg_freq_choose[1:0](REGC[3:2]) automatically. After complete the auto command bus train, the train value will be locked in the FSP_n module, then the user canusethereg_freq_choose[1:0](REGC[3:2])to switch frequency quickly. The user also canuse the register to update the FSP_n lock value after the command bus train. The steps show below:

1. Configure the per-bit de-skew value of the command through the corresponding register. For example, if you want to change the per-bit de-skew of the CA1_A, configure the desired value tothe reg_a13_invdelaysel.

2. Use the register reg_freq_choose[1:0](REGC[3:2]) to choose the frequency point.
For example, if you want to change the per-bit de-skew of the command at frequency point 2,
configure the 0x02 to reg_freq_choose[1:0](REGC[3:2]).
3. Set the reg_ca_perbit_skew_update(REG22[6]) to 1'b1 to update the lock value andrecover to 1'b0.
4. After these steps, the per-bit de-sew of command belong to frequency point 2 will change and be locked again.
The above configure path is enabled when reg_cmd_perbit_skew_bp(REG25[2]) set to 1'b0.
When reg_cmd_perbit_skew_bp(REG25[2])set to 1'b1, the user can use the register to controlthe per-bit de-skew directly. The register directly control path is useful when enable the commandbus train bypass mode.

1.6.4 Data Perbit De-Skew Control

The address offset of different data channels shows in following table.

Table 1-10 The address offset of each channel

CHANNEL	ADDRESS_OFFSET
Byte0(CS0)	0x320
Byte0(CS1)	0x340
Byte0(CS2)	0x400
Byte0(CS3)	0x420
Byte1(CS0)	0x4a0
Byte1(CS1)	0x4c0
Byte1(CS2)	0x580
Byte1(CS3)	0x5a0
Byte2(CS0)	0x620
Byte2(CS1)	0x640
Byte2(CS2)	0x900
Byte2(CS3)	0x920
Byte3(CS0)	0x9a0
Byte3(CS1)	0x9c0
Byte3(CS2)	0xa80
Byte3(CS3)	0xaa0

Byte0 CS0 bit has a following feature for TX and RX

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
0x320	reg_a_l_cs0_dm_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DM0 for RANK0
0x324	reg_a_l_cs0_dq0_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQ0 for RANK0
	reg_a_l_cs0_dq1_in_vdelaysel	[23,16]	0x80	The register used to control the tx delay line of the A_DQ1 for RANK0
	reg_a_l_cs0_dq2_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQ2 for RANK0
	reg_a_l_cs0_dq3_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DQ3 for RANK0
0x328	reg_a_l_cs0_dq4_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQ4 for RANK0
	reg_a_l_cs0_dq5_in_vdelaysel	[23,16]	0x80	The register used to control the tx delay line of the A_DQ5 for RANK0

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
	reg_a_l_cs0_dq6_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQ6 for RANK0
	reg_a_l_cs0_dq7_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DQ7 for RANK0
0x32c	reg_a_l_cs0_dqs_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQS for RANK0
	reg_a_l_cs0_dqs_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQSB for RANK0
0x330	reg_a_l_cs0_loop_invdelaysel	[28,24]	0x0	The register used to choose the obs signal to check delay line control of the byte0 for RANK0. 5'd0: Choose to the current value to control the rx delay line of A_DQ0 for RANK0. 5'd1: Choose to the current value to control the rx delay line of A_DQ1 for RANK0. 5'd2: Choose to the current value to control the rx delay line of A_DQ2 for RANK0. 5'd3: Choose to the current value to control the rx delay line of A_DQ3 for RANK0. 5'd4: Choose to the current value to control the rx delay line of A_DQ4 for RANK0. 5'd5: Choose to the current value to control the rx delay line of A_DQ5 for RANK0. 5'd6: Choose to the current value to control the rx delay line of A_DQ6 for RANK0. 5'd7: Choose to the current value to control the rx delay line of A_DQ7 for RANK0. 5'd8: Choose to the current value to control the rx delay line of A_DM0 for RANK0. 5'd9: Choose to the current value to control the rx delay line of A_DQS0 for RANK0. 5'd10: Choose to the current value to control the rx delay line of A_DQSB0 for RANK0. 5'd16: Choose to the current value to control the tx delay line of A_DQ0 for RANK0 5'd17: Choose to the current value to control the tx delay line of A_DQ1 for RANK0.

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
				5'd18: Choose to the current value to control the tx delay line of A_DQ2 for RANK0. 5'd19: Choose to the current value to control the tx delay line of A_DQ3 for RANK0. 5'd20: Choose to the current value to control the tx delay line of A_DQ4 for RANK0. 5'd21: Choose to the current value to control the tx delay line of A_DQ5 for RANK0. 5'd22: Choose to the current value to control the tx delay line of A_DQ6 for RANK0. 5'd23: Choose to the current value to control the tx delay line of A_DQ7 for RANK0. 5'd24: Choose to the current value to control the tx delay line of A_DM0 for RANK0. 5'd25 Choose to the current value to control the tx delay line of A_DQS0 for RANK0. 5'd26: Choose to the current value to control the tx delay line of A_DQSB0 for RANK0.
	reg_a_l_cs0_dm_invdelayselrx	[14,8]	0x0	The register used to control the rx delay line of the A_DM0 for RANK0
0x334	reg_a_l_cs0_dq0_in_vdelayselrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQ0 for RANK0
	reg_a_l_cs0_dq1_in_vdelayselrx	[23,16]	0x80	The register used to control the rx delay line of the A_DQ1 for RANK0
	reg_a_l_cs0_dq2_in_vdelayselrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQ2 for RANK0
	reg_a_l_cs0_dq3_in_vdelayselrx	[7,0]	0x80	The register used to control the rx delay line of the A_DQ3 for RANK0
0x338	reg_a_l_cs0_dq4_in_vdelayselrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQ4 for RANK0
	reg_a_l_cs0_dq5_in_vdelayselrx	[23,16]	0x80	The register used to control the rx delay line of the A_DQ5 for RANK0

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
0x33c	reg_a_l_cs0_dq6_in_vdelay selrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQ6 for RANK0
	reg_a_l_cs0_dq7_in_vdelay selrx	[7,0]	0x80	The register used to control the rx delay line of the A_DQ7 for RANK0
	reg_a_l_cs0_dqs_in_vdelay selrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQS for RANK0
	reg_a_l_cs0_dqs_in_vdelay selrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQSB for RANK0

There are three paths to control the TX data Perbit de-skew show in thefollowing table.

Table 1-11 TX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the TX data Perbit de-skew directly.	reg_dq_wr_train_en(REGA0[1]) set to 0. reg_wl_bypass(REG04[7]) set to 1. Generate the posedge of reg_wl_freq_update(REG44[28])
Write Leveling	Using the write levelingresult.	reg_wl_bypass(REG04[7]) set to 0.
Write Training	Using the write trainingresult.	reg_dq_wr_train_en(REGa0[1]) set to 1. reg_wl_bypass(REG04[7]) set to 1.

There are two paths to control the RX data Perbit de-skew show in thefollowing table.

Table 1-12 RX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the RX data Perbit de-skew directly.	reg_dq_rd_train_en(REG94[0]) set to 0 and reg_rd_train_predef_en(REG94[14]) set to 0. Generate the posedge of reg_rd_train_freq_update(REG94[2])
Read Training	Using the read trainingresult.	reg_dq_rd_train_en(REG94[0]) set to 1 or reg_rd_train_predef_en(REG94[14]) set to 1.

1.6.5 DDR PHY Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination forhigh-frequency operation. The DDR PHY supports the auto command bus trainfunction to center the internal VREF(ca) in the CA data eye and adjustment of the CS and CAsignals to meet setup/hold requirements.

When enable the auto command bus train function, the PHY will complete the train of the VREF(ca), CS and CA automatically. The auto command bus train flow shows in the following steps.

1. Configure reg_phy_sdram_nitial(reg0x26[7]) to 1'b1 to fix the input of the command path
2. PHY initialization
3. Configure reg_clk_div_cnt(reg0x4e[3:0]) to choose the divider for the low speed
4. Configure reg_tmrw(reg0x11[7:4]/reg_tcacd(reg0x11[3:0])/reg_tvrefca)reg0x12[7:0]/reg_tcaent(reg0x13[7:0])/reg_tckelck(reg0x14[7:4])/reg_tdstrain(reg0x14[3:0])/reg_tadr(reg0x15[7:4])/reg_txcbt(reg0x15[3:0])/reg_tfc(reg0x16[7:0]) to configure the timing parameter for auto cat train
5. Configure reg_cat_rank_num(reg0x21[7:6]) = 2'b11 to chosse the ca train rank reg_lpddr4_ca_odt(reg0x20[5:4]=2'b01 to terminate the rank0 (or reg_lpddr4_ca_odt(reg0x20[5:4] = 2'b10 to terminate the rank1)
6. Configure reg_cat_cs_train_valude(reg0x21[5:0]) reg_cat_ca_train_value(reg0x22[5:0])

to choose the cs and ca training pattern
7. Configure reg_cha_cat_cs_check_value(reg0x76[5:0])
regchb_cat_cs_check_value(reg0x77[5:0]) reg_cha_cat_ca_check_value(reg0x78[5:0])
reg_chb_cat_ca_check_value(reg0x79[5:0]) to choose the cs and ca training pattern
8. Configure reg_cat_enable(reg0x10[0]) to 1'b1 to enable the auto command bus train
9. Configure reg_cat_start(reg0x10[1]) to 1'b1 to start the auto command bus train
10. Wait auto command bus train done by read reg0x93[1:0], when it equals to 2'b11(for two ranks), it means complete the auto command bus train.
11. Configure reg_cat_start(reg0x10[1]) to 1'b0 to exit the auto command bus train
12. Configure reg_cat_enable(reg0x10[0]) to 1'b0 to disable the auto command bus train
13. Read register reg0x3a0-reg0x3df to get the ca train result
The command bus train not only adjusts the phase of the CA bus but also adjusts the phase of the CS. The user can use the reg_cat_skep_cs_train(REG0x38[2]) to control the enable or disable ofthe cstrain. When this signal sets to 1, the PHY will skip the cstrain; when this signal sets to0, the PHY will enable the cstrain.
The PHY support two modes cstrain controlled by the reg_cs_pwc_disable(REG0x38[7]):
Normal cstrain (reg_cs_pwc_disable = 1): When choose the normal cstrain mode, the pulse width of the CS will keep the same width of the CK period.
Modulation cstrain (reg_cs_pwc_disable =0): It is the default mode. When choose this mode,
the pulse width of the CS will the 75% of the CK period when the CS is in the train mode (after
the frequency changes from the FSP[X] to FSP[Y]). The state shows in the following figure.

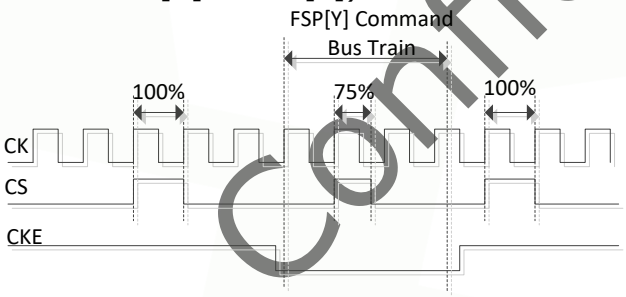


Fig.1-4 Modulation cstrain mode

If the user enables the Modulation cstrain mode, the CS Train is based on the 75% pulse widthof the normal CS. So the cstrain result has fixed 25% offset and need to compensate 12.5% offset using the special register after the command bus train. After that, the CS will go to the bestpoint of the cstrain.
The user uses the following registers to complete the compensation of the cs train result.

Table 1-13 Compensation of the ca and cs train result

ADDR	SIGNAL	DESCRIPTION
0x40[29:24]	reg_cha_cat_cs_check_value	The check value of channel A when do the cs train
0x40[21:16]	reg_chb_cat_cs_check_value	The check value of channel A when do the cs train
0x40[13:8]	reg_cha_cat_ca_check_value	The check value of channel A when do the ca train
0x40[5:0]	reg_chb_cat_ca_check_value	The check value of channel A when do the ca train

This register should be set after the command bus train and before change the frequency to the train frequency point.

1.6.6 DDR PHY RX DQS Calibration

DDR PHY auto dqs calibration function has been implemented in the PHY. The entire training processes only need to configure the register to start andwait for finish.
The entire training process is as follows:
1. PHY's register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY's register beginning calibration.

ADDR	BIT	DEFAULT	DESCRIPTION
0x4	5:2	0xe	The rank select signal of the rx-dqs calibration fuction. Low is valid. 4'b0000: The rx-dqs calibration result will auto switch between the RANK0, RANK1,RANK2,RANK3 according to the DFI interface command after the rx-dqs calibration training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the auto rx-dqs calibration training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the auto rx-dqs calibration training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the auto rx-dqs calibration training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the auto rx-dqs calibration training. 4'b11: Reserved. Note: Can't set to 2'b00 when enable the rx-dqs calibration training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the rx-dqs calibration training.
	1	0x0	set calibration bypass mode(1:bypass mode; 0:nomal)
	0	0x0	The auto rx-dqs calibration training enable signal. High is valid. 0: Keep current state or exit the auto rx-dqs calibration training. 1: Enable the auto rx-dqs calibration training function.
0x20c	6		The rx dqs calib complete signal. Active high. Only change to 1'b1 when all open channel have compelte the rx dqs calibration
	5		The error flag of the rx dqs calib. Active high.
	4:0		The rx dqs calib complete signal of each channel. Active high. [0]: The rx dqs calib complete of byte0. [1]: The rx dqs calib complete of byte1. [2]: The rx dqs calib complete of byte2. [3]: The rx dqs calib compelte of byte3. [4]: The rx dqs calib compelte of byte4

4. Wait for the calibration finish by PHYREG0x20c.
5. Normal read and writes operation can begin.

1.6.7 DDR PHY Write Leveling Training

DDR PHY auto write leveling training function has been implemented in the PHY. The entire training processes only need to configure the register to start and wait for finish。
The entire training process is as follows:
1. PHY’s register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY REG0x4 to configure the dram mode register which used to enable dram write leveling training function.
4. Set the PHY's register to begintraining.

ADDR	BIT	DEFAULT	DESCRIPTION
0x4	31:16	0x0	[23:16]Write leveling load mode [7:0]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same

ADDR	BIT	DEFAULT	DESCRIPTION
			setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register should keep the same value with the MR1[7:0]. For LPDDR3/LPDDR4, this register should keep the same value with the MR2[7:0]. Please reference to the section 4.5.2 to get more information. [31:24]"Write leveling load mode [15:8]. Relate to the register 10’ h002 [2]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register [13:8] should keep the same value with the MR1[13:8] and this register[15:14] should set 2'b01. For LPDDR3/LPDDR4, this register should set to 8'h0.
	11:8	0xe	The rank select signal of the write-leveling fuction. Low is valid. 4'b0000: The write-leveling result will auto switch between the RANK0 ,RANK1,RANK2,RANK3 according to the DFI interface command after the write-leveling training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the write-leveling training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the write-leveling training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the write-leveling training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the write-leveling training. 4'b1111: Reserved. Note: Can't set to 4'b0000 when enable the write-levleing training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the write-leveling training.
	7	0x0	The tx perbit-skew bypass function enable signal. High is valid. 0: Use the write-leveling training result to control the tx perbit-skew delay. The A_DQ0~A_DQ7/A_DM0 will use the A_DQS0 training result. The A_DQ8~A_DQ15/A_DM1 will use the A_DQS1 training result. The B_DQ0~A_DQ7/A_DM0 will use the B_DQS0 training result. The B_DQ8~A_DQ15/A_DM0 will use the B_DQS1 training result. 1: Use the register to control the tx perbit-skew delay. Each data pad has an independet controller register.

ADDR	BIT	DEFAULT	DESCRIPTION
	6	0x0	The write-leveling training enable signal. High is valid. 0: Keep current state or exit the write-leveling training state. 1: Eanble the write-leveling training function
0x44	28	0x0	The data tx delay line control value update signal. Active high. In the default mode, the tx delay line is controlled by the write-levevling/write training result according to the frequency point. If the user wants to change the value to adjust the delay line, the user can use the bypass registers (invdelay_t) that show in the Table "Data Perbit De-skew Control Registers For TX And RX" to set the value and set this signal “1”. Then the bypass register value will be updated to the control register of the tx perbit skew base on the current frequency point.
0x02c	12:8		The write leveling complete signal of each channel. Active high. [0]: The write leveling complete of byte0. [1]: The write leveling complete of byte1. [2]: The write leveling complete of byte2. [3]: The write leveling compelte of byte3. [4]: The write leveling compelte of byte4

5. Wait for the calibration finish by polling PHY REG92. The write leveling results can be read from the following registers.

Table 1-14 The write leveling result for all bytes

ADDR	BIT	DEFAULT	DESCRIPTION
0x370	[23:16]	0x0	The write-leveling result of byte0 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte0 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x44c	[23:16]	0x0	The write-leveling result of byte0 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte0 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x4f0	[23:16]	0x0	The write-leveling result of byte1 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte1 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x5cc	[23:16]	0x0	The write-leveling result of byte1 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte1 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x670	[23:16]	0x0	The write-leveling result of byte2 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte2 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x74c	[23:16]	0x0	The write-leveling result of byte2 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte2 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x7f0	[23:16]	0x0	The write-leveling result of byte3 for RANK0. The user can get the write-leveling result after the write-leveling training complete

	[7:0]	0x0	The write-leveling result of byte3 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x8cc	[23:16]	0x0	The write-leveling result of byte3 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte3 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x970	[23:16]	0x0	The write-leveling result of byte4 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte4 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0xa4c	[23:16]	0x0	The write-leveling result of byte4 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte4 for RANK3. The user can get the write-leveling result after the write-leveling training complete

6. Normal read and writes operation can begin.

1.6.8 DDR PHY Read Train

The DDR PHY supports the read training. It includes three modes:

- Auto MPR/MPC Mode(Only support for DDR3/DDR4/LPDDR3/LPDDR4)
- Predefined mode (Only support DDR3/DDR4/LPDDR3/LPDDR4)
- Bypass Mode(Only support LPDDR3 and LPDDR4)

Auto MPR/MPC Mode: When the PHY chooses the DDR3/DDR4, it will use the MPR command to complete the read training of the Auto-Mode. When the PHY chooses theLPDDR3/LPDDR4, it will use the RD DQ Calibration command to complete the read training of the Auto-Mode and BP-Mode.

Predefine mode: you should write data to SDRAM and make sure the data has been written to the SDRAM at the specified location. For example, you can write data when SDRAM working at low frequency. Then the PHY read the data which you write to SDRAM.

When we enable the read training, the PHY will adjust the per-bit de-skew to change the delay ofthe RX DQS and RX DQ to find the optimal position. The adjust range of the per-bit de-skew isfrom 6'h0 to 6'h3f.

In rx vref training, we change the value of phy's vref. When set a new vref value to PHY, we should wait 800ns to update it. And the adjust range of the vref is from 8'h00 to 8'hff. You can
change the PHY's vref value yourself by configuring the associated register.

For predefined mode, the phy can support rx vref training. If you enable the vref training function, the predefinedread training have 3 steps, step1 adjust per-bitde-skew (step1_delay),step2 adjust vref(step2_vref), step3 adjust per-bit de-skew(step3_delay) again. When you disable vreftraining function, the predefinedread training only have step1.When step1 done, all steps done.

During the training, if you set reg_phy_refresh_en to 1'b1, the PHY support to do auto refresh
by itself. If you use this function, the controller should send a refresh (both rank in

themeantime) after training enable, otherwise the PHY will keep waiting.
When the user enables the normal read training function, it will complete the read training automatically. The normal read training using the following steps.
1. Open PHY auto refresh function in training(if you need) by configuring reg_phy_refresh_en=0x1.
2. Choose the read training rank using the reg_rdtrain_cs_sel=2'b10(rank0).
3. Configure the MR15/MR20/MR32/MR40 through reg_lpddr4_mr15_value/reg_lpddr4_mr20_value/reg_lpddr4_mr32_value/reg_lpddr4_mr40_value to choose the read training pattern(Only for lpddr4).
4. choose the dqs phase before read training by setting cha_reg_l_rd_train_dqs_default/cha_reg_r_rd_train_dqs_default/chb_reg_l_rd_train_dqs_default/chb_reg_r_rd_train_dqs_default=0xe.
5. Enable the read training by setting reg_dq_rd_train_en=0x1.
6. Send a auto refresh(rank0 and rank1 in the meantime) if you open PHY auto refresh function.
7. Wait the train done by polling the reg_train_true_done=0x1.
8. Check the read train state by read cha(b)_train_done_for_rd_to_reg[1:0].High means error.
9. Exit the Read train by setting reg_dq_rd_train_en=0x0.

1.6.9 DDR PHY Write Train

The DDR PHY supports the write training. It only supports the auto mode.When the PHY chooses the DDR3/DDR4/LPDDR3, it will use the normal write and readcommand to complete the write training. When the PHY chooses the LPDDR4, it will use theDQS-DQ training mode command to complete the write training.
When we enable the write training, the PHY will adjust the per-bit de-skew to change the delay ofthe TX DQ to find the optimal position(The dqs will keep to the phase find by the write-levelingwhen enable the write leveling function). The adjust range of the per-bit de-skew is from 6'h0 to6'h3f.
The PHY can support tx vref training(only for LPDDR4). If you enable the vref training function,the wr training have 3 steps, step1 adjust per-bit de-skew(step1_delay), step2 adjust vref(step2_vref), step3 adjust per-bit de-skew(step3_delay) again. When you close vref trainingfunction, the wr training only have step1, when step1 done ,all step done.
When the user enables the normal write training function, it will complete the write trainingautomatically. The normal write training using steps shows below.
1. Configure the initial address(write data to this address) reg_train_col_address/reg_train_ba_address/reg_train_row_address.
2. If you set reg_wrtrain_check_data_value_random_gen=0x0, configure the check data value as the data you want to write to SDRAM(10*BL8).
3. If you need the PHY do refresh in training, you should configure the reg_phy_trefi, reg_phy_trfc, reg_max_refi_cnt. Then enable the reg_phy_refresh_en=0x1.
4. Choose the write training rank using the reg_wrtrain_cs_sel=0x2(rank0).
5. If you need the PHY do tx vref training, you should configure reg_train_vref_step_max, reg_train_vref_step_min, reg_wrtrain_lpddr4_vref_range, reg_wrtrain_vref_wait_vref_cnt_50ns.
6. If you enable the DBI function, and want to do wr training with DBI function open, you should set reg_ddr4_dbi=0x1 first(Only for DDR4).
7. Choose the dqs phase before write training by setting reg_wr_train_dqs_default_bypass=0x1. Otherwise PHY will choose the write leveling training result.
8. Choose the write training auto mode by setting reg_dq_wr_train_auto=0x1.
9. Enable the tx vref training by setting(if need) reg_train_vref_en=0x1. Enable the write training by setting reg_dq_wr_train_en=0x1.
10. Send a auto refresh if you open PHY auto refresh function.
11. Wait the wr train done by polling the train_all_step_done=0x1.
12. Check the wr train state by read train_step1_error, train_step2_error, train_step3_error. High means error.
13. Exit the write training by setting reg_dq_wr_train_en=0x0.

1.6.10 DDR Monitor

1. DDR read or write address monitor

DDR monitor module can store 4 consecutive read or write addresses in real time. We can read these addresses by APB bus for debug when system enters abnormal state.

The steps of configuration to monitor DDR read or write address:

- Configure DDRMON_DDR_IF_CTRL.direction to select storing read or write address.
- Set DDRMON_DDR_IF_CTRL.if_mon_en to '1' to enable DDR monitor.
- When system is abnormal, we can read the register to get the current four addresses.

2. DDR access address monitor within a specified range

Sometimes we want to confirm whether DDR read or write within a specified address range, then we can configure the address range and enable this function.

The steps of configuration to monitor DDR access address within a specified range:

Configure thewrite address range registers DDRMON_WR_START_ADDR, DDRMON_WR_END_ADDR, and read address registers DDRMON _RD_START_ADDR, DDRMON _RD_END_ADDR.

- Enable interrupt by configure the register DDRMON_INT_MASK[6:5] to 0.
- Set DDRMON_DDR_IF_CTRL.if_mon_en to '1' to enable DDR address monitor.
- If the read or write addresses hit the range, then interrupt will assert, and we can read the interrupt status register DDRMON_INT_STATUS.

3. DDR access command statistics

This module can do the statistics about DDR access command, like write, read and active by monitoring DFI interface. There are two mode to do statistics, hardware mode and software mode. Two thresholds can be set, if read and write command number is more than high threshold, or less than low threshold, the interrupt will be asserted.

4. DDR low power statistics

It does the statistics the low power period such as DDR self-refresh, power down, clkstop and PHY low power. After compare statistics interrupt asserts, the low power period represent in correspond count register will be updated and can be accessed through APB bus interface.

Hardware mode

In hardware mode, a dfi timer is used to specify a statistics period, the command statistics is done in the statistics period. The dfi timer is running in 24MHz. After dfi timer counts to the threshold, and update the statistics value, the dfi timer will restart automatically, and count again.

The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON_CTRL.hardware_en as '1' to enable hardware mode.
- Configure register DDRMON_TIMER_COUNT to set the dfi timer count threshold, the statistics is done in the period of timer being less than the value of DDRMON_TIMER_COUNT.
- Configure register DDRMON_CTRL.lpddr23_en and DDRMON_CTRL.lpddr4_en to set the DDR mode:

DDRMON_CTRL.lpddr23_en	DDRMON_CTRL.lpddr4_en	DDRMON_CTRL.ddr4_en	DDR mode
1	0	0	LPDDR3
0	0	0	DDR3
0	1	0	LPDDR4
0	0	1	DDR4

- Configure register DDRMON_FLOOR_NUMBER to specify the low threshold of interrupt, and configure register DDRMON_TOP_NUMBER to specify the high threshold of interrupt.
- Configure register DDRMON_CTRL.timer_cnt_en as '1' to start hardware mode.
- Wait for the interrupt to do following process. We also can read the read, write and active command number separately.

Software mode

In software mode, the statistics is controlled by software.

The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON_CTRL.lpddr23_en, DDRMON_CTRL.lpddr4_en and

DDRMON_CTRL.ddr4_en to set the DDR mode like hardware mode.

- Configure register DDRMON_CTRL.software_en as '1' to enable software mode statistics.
- Configure register DDRMON_CTRL.software_en as '0' to stop the statistics, and generate the statistics result. We can read the read, write and active command number separately.

1.6.11 HWFFC

To enable Hardware Fast Frequency change function, software must configure DDR_GRF_CON3[6:3] to 0x3, which means DDRC low power interface is controlled by HWFFC block.

And following software procedure is example for how to used HWFFC function auto mode.

1. Enable DDR clock switch function by configure CRU_MISC_CON0[13] to 1'b1.
2. Clear dfi_init_start by configuring DDRC_DFIMISC[5] to 1'b0.
3. Enable DDRC HWFFC function by configure DDRC.DDRC_HWFFCCTL to 0x3
4. Configure timing related register for Frequency 1 to 3
5. Configure DDRC.DDRC_MSTR[29] for frequency mode
6. Configure DDRC.DDRC_MSTR[3:2] for target frequency
7. Configure HWFFC.HWFFC_MODE to 0x0 to choose auto mode
8. Configure HWFFC.HWFFC_CTRL = 0x1(fast freq change) | 0x1<<1 (FSP1) | 0x1<<5 (load initial value) | 0x1<<7(ignore phy ready) | 0x1<<8 (auto clock switch en)
9. Configure HWFFC.HWFFC_CTRL[5] to 0x0 to disable loading initial clk switch value.
10. Configure HWFFC.HWFFC_CNT for PLL lock time
11. Configure HWFFC.HWFFC_EN[0] to 1'b1 to enable HWFFC
12. Wait for DDRC_HWFFCSTAT[1:0] to 0x0
13. Configure DDRC.DDRC_HWFFCCTL[3:2] to 0x0 to disable HWFFC function for DDRC
14. Configure HWFFC.HWFFC_EN[0] to 0x0 to disable HWFFC function for HWFFC block.
15. Write-leveling and RXdqs training.
16. DDR access

Chapter 2 DDR Converter of Frequency (DCF)

2.1 Overview

DDR Converter of Frequency (DCF) is used to implement DDR frequency conversion without the participation of CPU. DCF is connected to SOC through an AXI Master and an APB Slave, with a DMAC and instruction buffer inside. Beforehand, software puts into SRAM formulary pieces of instructions which consist of all the register-related configurations in the process of frequency conversion. When started-up, DCF automatically reads instructions to the inside buffer by means of DMA, and implement register configuration after analysis. A done signal will be provided for CPU after all the instructions are analyzed.

DCF supports the following features:

- AMBA 32-bit AXI compliant
- Support DMA operation from SRAM to buffer
  - Support burst8 only
  - LLP not supported
- Support 2 internal instruction registers : r0 & r1
- Support following software instructions:
  - IDL (delay)
  - LDR (read register)
  - STR (write register)
  - ISB (write with flush)
  - Bitwise AND
  - Bitwise OR
  - Bitwise INV
  - LSR (left shift)
  - RSR (right shift)
  - ADD
  - SUB
  - POLLEQ (poll a register until the value match)
  - POLLNEQ (poll a register until the value mismatch)
  - CMPEQ (compare if equal)
  - CMPNEQ (compare if unequal)
  - BL (jump upwards or downwards, 8bytes align)
- Support following program functions through combination of basic instructions
  - If-else
  - while
  - loop
  - for

2.2 Block Diagram

DCF comprises with:

- An AXI Master Interface
- An APB Slave Interface
- A DMA controller
- An Instruction Buffer
- Instruction analyzer

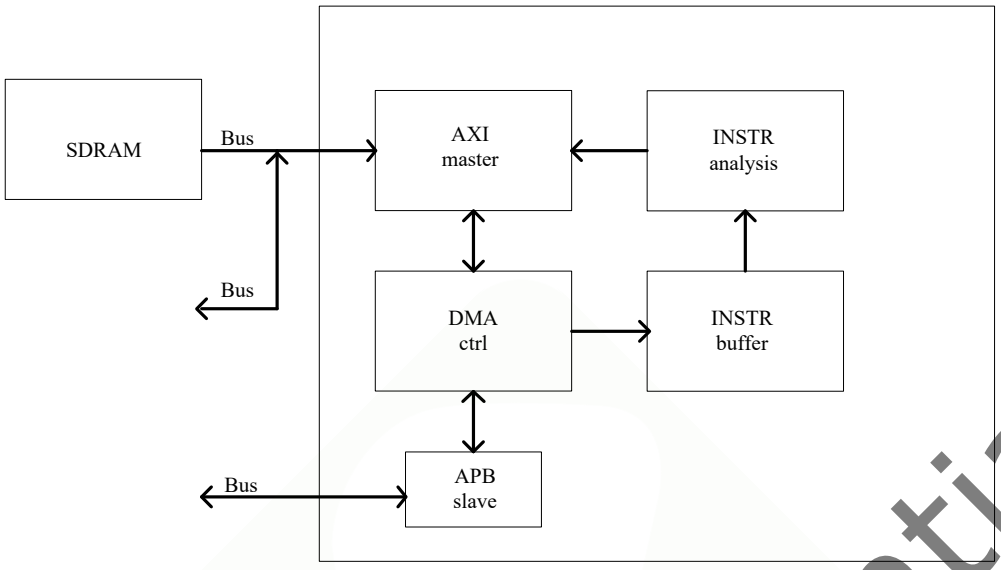


Fig.2-1 DCF Block Diagram

2.3 Register Description

2.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DCF_CTRL	0x0000	W	0x00000000	DCF Control Register
DCF_STATUS	0x0004	W	0x00000001	DCF Internal Status Register
DCF_ADDR	0x0008	W	0x00000000	DCF Instruction Start Address Register
DCF_ISR	0x000c	W	0x00000000	DCF Interrupt Status Register
DCF_TIMEOUT_CYC	0x0014	W	0xffffffff	DCF Instruction Timeout Cycle Register
DCF_CURR_R0	0x0020	W	0x00000000	Current Internal R0 Value Register
DCF_CURR_R1	0x0024	W	0x00000000	Current Internal R1 Value Register
DCF_CMD_COUNTER	0x0028	W	0x00000000	Current Command Counter Value Register
DCF_LAST_ADDR1	0x0030	W	0x00000000	Last 1 Instruction Address Register
DCF_LAST_ADDR2	0x0034	W	0x00000000	Last 2 Instruction Address Register
DCF_LAST_ADDR3	0x0038	W	0x00000000	Last 3 Instruction Address Register
DCF_LAST_ADDR4	0x003c	W	0x00000000	Last 4 Instruction Address Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.3.2 Detail Registers Description

DCF_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	vop_hw_en 1'b1 : Enable 1'b0 : Disable
1	WO	0x0	timeout_en 1'b1: Enable 1'b0: Disable

Bit	Attr	Reset Value	Description
0	WO	0x0	start This bit will be auto cleared when DCF is done. 1'b1: Start DCF 1'b0: Stop DCF

DCF_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	WO	0x0	dma_done_st 1'b1: DCF has fetched all the instructions.
6	WO	0x0	instr_done_st 1'b1: DCF has done all the instructions analysis.
5	WO	0x0	dma_error_st 1'b1 : Error response received when DCF is fetching instructions.
4	WO	0x0	instr_error_st 1'b1 : Error response received when DCF is handling instructions.
3	WO	0x0	dcf_timeout_st 1'b1: DCF timeout
2	WO	0x0	dcf_edge_trigger_st 1'b1 : DCF is triggered by dma_finish from vop.
1	WO	0x0	dcf_level_trigger_st 1'b1 : DCF is triggered by one of the following sources: vop_standby / vop_clockgating / vop_powndown
0	RO	0x1	dcf_idle_st 1'b1 : DCF is idle 1'b0 : DCF is busy

DCF_ADDR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr DCF instruction fetch start address

DCF_ISR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	dcf_error 1'b1: Error response or timeout during DDR change frequency.
0	WO	0x0	dcf_done 1'b1: DDR change frequency completed. 1'b0: DDR change frequency not completed.

DCF_TIMEOUT_CYC

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	timeout Calculated by axi clock

DCF_CURR_R0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r0 R0 value is sampled when dcf_done or dcf_error occurs.

DCF_CURR_R1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r1 R1 value is sampled when dcf_done or dcf_error occurs.

DCF_CMD_COUNTER

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cmd_counter cmd_counter value is sampled when dcf_done or dcf_error occurs. it records the number of pieces of instructions among DCF.

DCF_LAST_ADDR1

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr1 Value is sampled when dcf_done or dcf_error occurs. it records the last 1 instruction address.

DCF_LAST_ADDR2

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	last_addr2 Value is sampled when dcf_done or dcf_error occurs. it records the last 2 instruction address.

DCF_LAST_ADDR3

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr3 Value is sampled when dcf_done or dcf_error occurs. it records the last 3 instruction address.

DCF_LAST_ADDR4

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr4 Value is sampled when dcf_done or dcf_error occurs. it records the last 4 instruction address.

2.4 Application Notes

2.4.1 DCF Work Flow

1、 Software needs to open up a separate space in SRAM and loads a series of instructions in advance. The instruction should consists of:
   a、 Configure msch and cpu idle.
   b、 Configure Memory Controller to move DDR into Low-power State.
   c、 Reset DDRPHY if needed.
   d、 Configure Clock frequency, wait for PLL lock.
   e、 Configure all the Timing-relative registers.

f、 De-assert DDRPHY reset if needed.
g、 Initialize DDRPHY, do calibration.
h、 Configure Memory Controller to move DDR into Access State.

2、 Software configure DCF, notifying the start_addr, and then start DCF.
3、 DCF will transfer instruction data through DMA from SRAM to an internal buffer.
4、 In the meanwhile, An instruction analysis module will read these instructions from buffer, and transform them to corresponding bus-relative operations, including Write&Read registers, delay some clock cycles, arithmetic operation and so on.
5、 By Axi master, DCF will configure uPCTL、DDRPHY、CRU module to implement the procedure of DDR frequency conversion.
6、 DCF will recognize the last command, and generate a dcf_done interrupt for CPU.

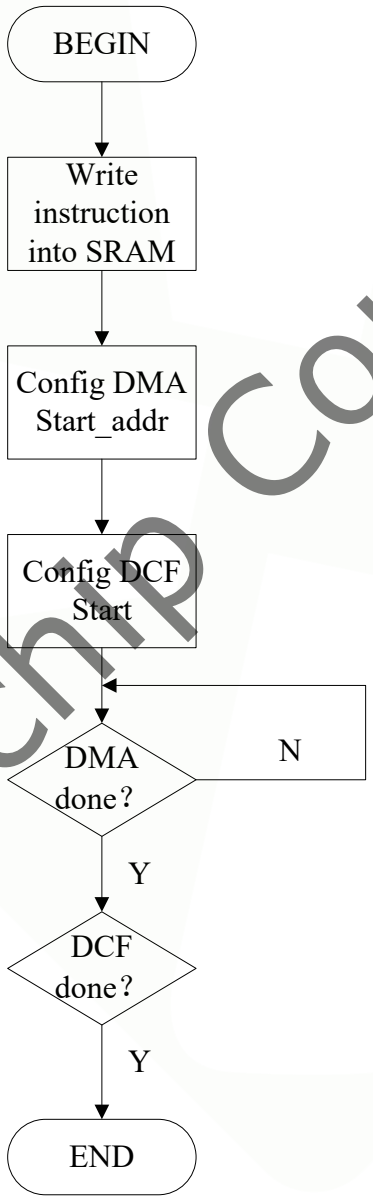


Fig.2-2 DCF work flow

2.4.2 Instruction Format

One piece of instruction, which is 64bit, should consist of the information of:

1、 Address
2、 Data

3、 Command

63:59	58:34	33:32	31:0
cmd[4:0]	addr[26:2]	(r1,r0)	data

The overall principle of instruction information is:

1、 Address[31:27] is reserved for 5bit command, which represents the corresponding operation.
2、 Address[1:0] is used to indicate operation of r0 or r1.
3、 Address[26:2] is the real bus address. If 0, it means no bus operation ; if not 0, it means a combination of 2 instructions with a bus operation ahead and an arithmetic c operation followed in order to improve efficiency.

For example, let us analyze the instruction: 0f620002_00000003

1、 Command is 1,which represents an bitwise AND operation.
2、 Address is 0xff620000, represents a bus-read operation.
3、 R1 is indicated, represents that the middle result is stored into internal register r1.
4、 Data is 0x00000003, represents that the operation value is 0x3.
So, this instruction will do following operations:
- LDR #0xff620000, r1 ; //read register 0xff620000, and store value into r1
- AND r1, 0x00000003 ; //r1 is bitwise AND with 0x3, and re-store the result

The following table lists all the supported command

INSTR	cmd[4:0	addr[26:2]	R1	R0	Data[31:0]	
IDLE	5'h00	NA	NA	NA	#data	IDL #data
AND	5'h01	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; AND r0 #data
			1	0	#data	ldr #addr r1 ; AND r1 #data
			1	1	NA	ldr #addr r1 ; AND r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	AND r0 #data
			1	0	#data	AND r1 #data
			1	1	NA	AND r1 r0
OR	5'h02	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; OR r0 #data
			1	0	#data	ldr #addr r1 ; OR r1 #data
			1	1	NA	ldr #addr r1 ; OR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	OR r0 #data
			1	0	#data	OR r1 #data
			1	1	NA	OR r1 r0
INV	5'h03	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; XOR r0 ^#data
			1	0	#data	ldr #addr r1 ; XOR r1 ^#data
			1	1	#data	ldr #addr r1 ; XOR r1 ^r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	NA	INV r0
			1	0	NA	INV R1
			1	1	NA	SWP r0 r1
LSR	5'h04	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; LSR r0 #data
			1	0	#data	ldr #addr r1 ; LSR r1 #data
			1	1	NA	ldr #addr r1 ; LSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	LSR r0 #data
			1	0	#data	LSR r1 #data
			1	1	NA	LSR r1 r0

INSTR	cmd[4:0	addr[26:2]	R1	R0	Data[31:0]	
RSR	5'h05	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; RSR r0 #data
			1	0	#data	ldr #addr r1 ; RSR r1 #data
			1	1	NA	ldr #addr r1 ; RSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	RSR r0 #data
			1	0	#data	RSR r1 #data
			1	1	NA	RSR r1 r0
CMPEQ	5'h06	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPEQ r0 #data,flag
			1	0	#data	ldr #addr r0 ; CMPEQ r1 #data,flag
			1	1	NA	ldr #addr r0 ; CMPEQ r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPEQ r0 #data, flag
			1	0	#data	CMPEQ r1 #data, flag
			1	1	NA	CMPEQ r1 r0, flag
CMPNE	5'h07	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPNE r0 #data,flag
			1	0	#data	ldr #addr r1 ; CMPNE r1 #data,flag
			1	1	NA	ldr #addr r1 ; CMPNE r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPNE r0 #data, flag
			1	0	#data	CMPNE r1 #data, flag
			1	1	NA	CMPNE r1 r0, flag
ADD	5'h08	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; ADD r0 #data
			1	0	#data	ldr #addr r0 ; ADD r1 #data
			1	1	NA	ldr #addr r0 ; ADD r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	ADD r0 #data
			1	0	#data	ADD r1 #data
			1	1	NA	ADD r1 r0
SUB	5'h09	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; SUB r0 #data
			1	0	#data	ldr #addr r0 ; SUB r1 #data
			1	1	NA	ldr #addr r0 ; SUB r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	SUB r0 #data
			1	0	#data	SUB r1 #data
			1	1	NA	SUB r1 r0
STR	5'h0a	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
ISB	5'h0b	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
POLEQ	5'h0c	NA	0	1	#data	poll r0=#data,repeat last command
			1	0	#data	poll r1=#data,repeat last command
			1	1	NA	poll r1=r0,repeat last command

INSTR	cmd[4:0	addr[26:2]	R1	R0	Data[31:0]	
POLNEQ	5'h0d	NA	0	1	#data	poll r0!=#data,repeat last command
			1	0	#data	poll r1!=#data,repeat last command
			1	1	NA	poll r1!=r0,repeat last command
BL_U	5'h0e	ALL 0	NA	NA	#data	brr #data,?flag (upwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (upwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
BL_D	5'h0f	ALL 0	NA	NA	#data	brr #data,?flag (downwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (downwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
DMA_S	5'h10	NA	NA	NA	#data	set dma_start_addr = #data
DMA_D	5'h11	NA	NA	NA	#data	set dma_end_addr = #data
DMA_DO	5'h12	NA	NA	NA	#data	set dma_length = #data (byte) dma_start
END	5'h13	NA	NA	NA	NA	End of instruction

2.4.3 Hardware Trigger Flow

When DCF_CTRL.vop_hw_en is enabled, DCF can be triggered by any of the followed three sources: dma_finish 、vop_standby、vop_clkgate_en.

DCF is edge sensitive for dma_finish signal, and level sensitive for vop_standby and vop_clkgate_en signal.

When DCF is working, a dcf_idle is driven to low to indicate vop not to exit vop_standby status. And when DCF is not working, dcf_idle is driven to high for SOC and VOP to inquire.

Chapter 3 SPINLOCK

3.1 Overview

The hardware spinlock used for spinlock status storage. All the CPU can access spinlock to get the lock status.

3.2 Block Diagram

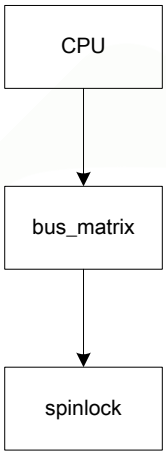


Fig.3-1 Spinlock in System

3.3 Register Description

3.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

3.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPINLOCK_status_n (range of n is 0~63)	0x0+4*n	W	0x00000000	spinlock status controller register_n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.3.3 Detail Register Description

SPINLOCK_status_n

Address: Operational Base + offset (0x0000+4*n)

Bit	Attr	Reset Value	Description
31:4	RO	0x000000	reserved reserved
3:0	RW	0x0	spinlock_status when 4bits is 0, 4bits can be written with new value. when 4bits is not 0, 4bits cannot be written. when write data is 0x0000, 4bits clean to 0.

Chapter 4 Crypto

4.1 Overview

Crypto is a hardware accelerator for encrypting or decrypting. It supports the most commonly used algorithm: DES/3DES, AES, SHA1, SHA256, MD5 and PKA.

The Crypto supports following features:

- Support Link List Item (LLI) DMA transfer
- Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
- Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
- Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
- Support up to 8-channels configuration

4.2 Block Diagram

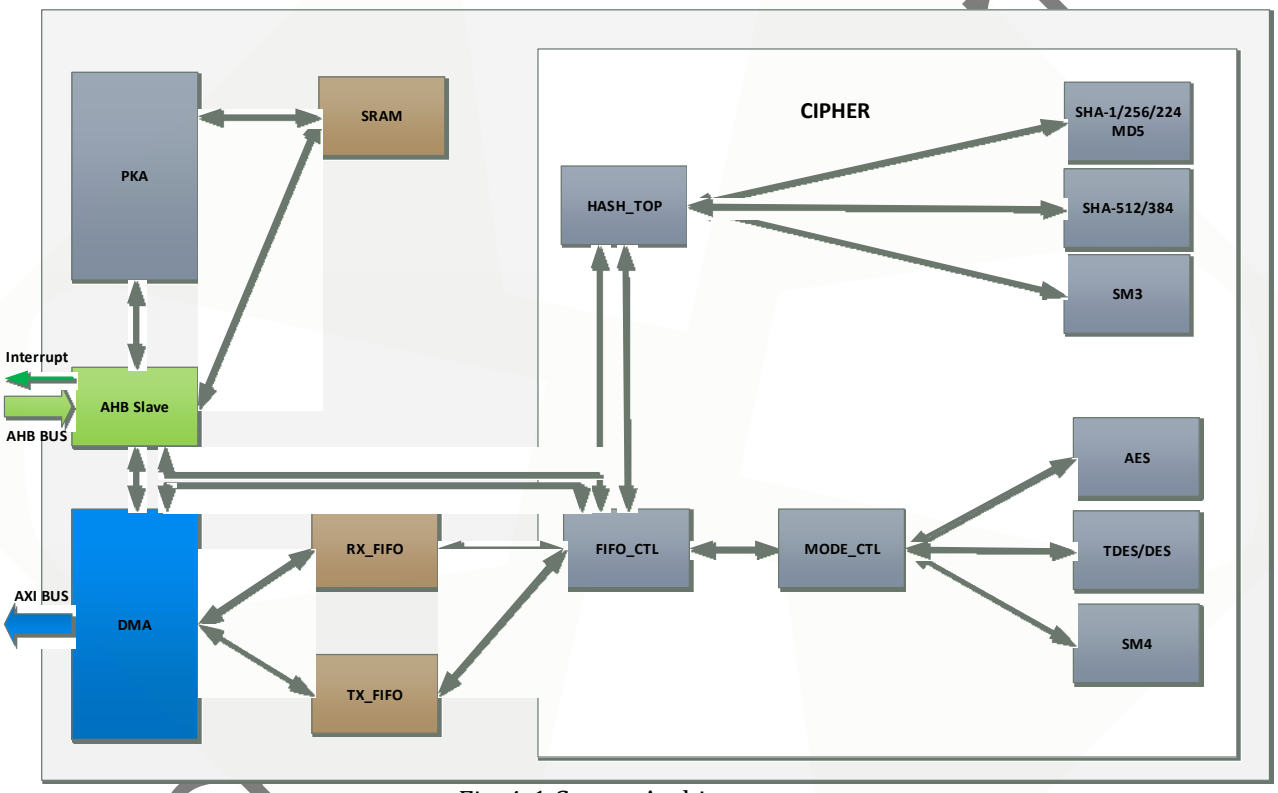


Fig. 4-1 Crypto Architecture

Crypto contains several modules : AHB_Slave, DMA, CIPHER, PKA.

AHB_Slave

AHB_Slave is used to configure registers. This module is in HCLK domain.

DMA

DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to external memory. DMA uses 64-bits AXI3 protocol with max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in ACLK domain.

CIPHER

CIPHER contains AES, SM4, DES/TDES and HASH engines. And it also supports various mode operations. The source data is either from RX_FIFO , or from other engine output. The result data is sending either to TX_FIFO, or Registers in module AHB_Slave. This module is in CLK_CORE domain.

PKA

PKA is used to accelerate mathematical operations for big numbers. It supports - Modular

arithmetic (addition, subtraction, multiplication and division), Regular arithmetic (addition, subtraction, multiplication and division), Modular inversion, Modular exponentiation, Logical operations (AND, OR, XOR, SHIFT). PKA has a SRAM which is used to store source , result and intermediate data for PKA operations. The software driver could use PKA operations to implement complicate calculation, such as RSA, ECC etc. It could support up to 4096 bits RSA modular exponentiation calculation. This module is in CLK_PKA domain.

4.3 Register description

4.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CRYPTO_CLK_CTL	0x0000	W	0x00000001	Clock Control Register
CRYPTO_RST_CTL	0x0004	W	0x00000000	Reset Control Register
CRYPTO_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
CRYPTO_DMA_INT_ST	0x000c	W	0x00000000	DMA Interrupt Status Register
CRYPTO_DMA_CTL	0x0010	W	0x00000000	DMA Control Register
CRYPTO_DMA_LLI_ADDR	0x0014	W	0x00000000	DMA LIST Start Address Register
CRYPTO_DMA_ST	0x0018	W	0x00000000	DMA Status Register
CRYPTO_DMA_STATE	0x001c	W	0x00000000	DMA State Register
CRYPTO_DMA_LLI_RADDR	0x0020	W	0x00000000	DMA LLI Read Address Register
CRYPTO_DMA_SRC_RADDR	0x0024	W	0x00000000	DMA Source Data Read Address Register
CRYPTO_DMA_DST_WADDR	0x0028	W	0x00000000	DMA Destination Data Read Address Register
CRYPTO_DMA_ITEM_ID	0x002c	W	0x00000000	DMA Descriptor ID Register
CRYPTO_FIFO_CTL	0x0040	W	0x00000003	FIFO Control Register
CRYPTO_BC_CTL	0x0044	W	0x00000000	Block Cipher Control Register
CRYPTO_HASH_CTL	0x0048	W	0x00000004	Hash Control Register
CRYPTO_CIPHER_ST	0x004c	W	0x00000000	Cipher Status Register
CRYPTO_CIPHER_STATE	0x0050	W	0x00000400	Cipher Current State Register
CRYPTO_CHn_IV_0	0x0100	W	0x00000000	Channel n IV Register 0
CRYPTO_CHn_IV_1	0x0104	W	0x00000000	Channel n IV Register 1
CRYPTO_CHn_IV_2	0x0108	W	0x00000000	Channel n IV Register 2
CRYPTO_CHn_IV_3	0x010c	W	0x00000000	Channel n IV Register 3
CRYPTO_CHn_KEY_0	0x0180	W	0x00000000	Channel n KEY Register 0
CRYPTO_CHn_KEY_1	0x0184	W	0x00000000	Channel n KEY Register 1
CRYPTO_CHn_KEY_2	0x0188	W	0x00000000	Channel n KEY Register 2
CRYPTO_CHn_KEY_3	0x018c	W	0x00000000	Channel n KEY Register 3
CRYPTO_CHn_PKEY_0	0x0200	W	0x00000000	Channel n Private KEY Register 0
CRYPTO_CHn_PKEY_1	0x0204	W	0x00000000	Channel n Private KEY Register 1
CRYPTO_CHn_PKEY_2	0x0208	W	0x00000000	Channel n Private KEY Register 2
CRYPTO_CHn_PKEY_3	0x020c	W	0x00000000	Channel n Private KEY Register 3
CRYPTO_CHn_PC_LEN_0	0x0280	W	0x00000000	Channel n PC Length Register 0

Name	Offset	Size	Reset Value	Description
CRYPTO_CHn_PC_LEN_1	0x0284	W	0x00000000	Channel n PC Length Register 1
CRYPTO_CHn_ADA_LEN_0	0x02c0	W	0x00000000	Channel n ADA Length Register 0
CRYPTO_CHn_ADA_LEN_1	0x02c4	W	0x00000000	Channel n ADA Length Register 1
CRYPTO_CHn_IV_LEN_0	0x0300	W	0x00000000	Channel n IV Length Register 0
CRYPTO_CHn_TAG_0	0x0320	W	0x00000000	Channel n Tag Register 0
CRYPTO_CHn_TAG_1	0x0324	W	0x00000000	Channel n Tag Register 1
CRYPTO_CHn_TAG_2	0x0328	W	0x00000000	Channel n Tag Register 2
CRYPTO_CHn_TAG_3	0x032c	W	0x00000000	Channel n Tag Register 3
CRYPTO_HASH_DOUT_0	0x03a0	W	0x00000000	HASH Data Output Register 0
CRYPTO_HASH_DOUT_1	0x03a4	W	0x00000000	HASH Data Output Register 1
CRYPTO_HASH_DOUT_2	0x03a8	W	0x00000000	HASH Data Output Register 2
CRYPTO_HASH_DOUT_3	0x03ac	W	0x00000000	HASH Data Output Register 3
CRYPTO_HASH_DOUT_4	0x03b0	W	0x00000000	HASH Data Output Register 4
CRYPTO_HASH_DOUT_5	0x03b4	W	0x00000000	HASH Data Output Register 5
CRYPTO_HASH_DOUT_6	0x03b8	W	0x00000000	HASH Data Output Register 6
CRYPTO_HASH_DOUT_7	0x03bc	W	0x00000000	HASH Data Output Register 7
CRYPTO_HASH_DOUT_8	0x03c0	W	0x00000000	HASH Data Output Register 8
CRYPTO_HASH_DOUT_9	0x03c4	W	0x00000000	HASH Data Output Register 9
CRYPTO_HASH_DOUT_10	0x03c8	W	0x00000000	HASH Data Output Register 10
CRYPTO_HASH_DOUT_11	0x03cc	W	0x00000000	HASH Data Output Register 11
CRYPTO_HASH_DOUT_12	0x03d0	W	0x00000000	HASH Data Output Register 12
CRYPTO_HASH_DOUT_13	0x03d4	W	0x00000000	HASH Data Output Register 13
CRYPTO_HASH_DOUT_14	0x03d8	W	0x00000000	HASH Data Output Register 14
CRYPTO_HASH_DOUT_15	0x03dc	W	0x00000000	HASH Data Output Register 15
CRYPTO_TAG_VALID	0x03e0	W	0x00000000	TAG Valid Register
CRYPTO_HASH_VALID	0x03e4	W	0x00000000	HASH Output Valid Register
CRYPTO_VERSION	0x03f0	W	0x00000000	CRYPTO Vertion Number Register
CRYPTO_RAM_CTL	0x0480	W	0x00000000	RAM Control Register
CRYPTO_RAM_ST	0x0484	W	0x00000001	RAM Status Register
CRYPTO_DEBUG_CTL	0x04a0	W	0x00000000	PKA Debug Control Register
CRYPTO_DEBUG_ST	0x04a4	W	0x00000001	PKA Debug Status Register
CRYPTO_DEBUG_MONITOR	0x04a8	W	0x0000feef	PKA Debug Monitor Bus Register
CRYPTO_PKA_MEM_MAP0	0x0800	W	0x00000000	PKA Memory Map 0 Register
CRYPTO_PKA_MEM_MAP1	0x0804	W	0x00000000	PKA Memory Map 1 Register
CRYPTO_PKA_MEM_MAP2	0x0808	W	0x00000000	PKA Memory Map 2 Register
CRYPTO_PKA_MEM_MAP3	0x080c	W	0x00000000	PKA Memory Map 3 Register
CRYPTO_PKA_MEM_MAP4	0x0810	W	0x00000000	PKA Memory Map 4 Register
CRYPTO_PKA_MEM_MAP5	0x0814	W	0x00000000	PKA Memory Map 5 Register
CRYPTO_PKA_MEM_MAP6	0x0818	W	0x00000000	PKA Memory Map 6 Register
CRYPTO_PKA_MEM_MAP7	0x081c	W	0x00000000	PKA Memory Map 7 Register
CRYPTO_PKA_MEM_MAP8	0x0820	W	0x00000000	PKA Memory Map 8 Register
CRYPTO_PKA_MEM_MAP9	0x0824	W	0x00000000	PKA Memory Map 9 Register

Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_MEM_MAP10	0x0828	W	0x00000000	PKA Memory Map 10 Register
CRYPTO_PKA_MEM_MAP11	0x082c	W	0x00000000	PKA Memory Map 11 Register
CRYPTO_PKA_MEM_MAP12	0x0830	W	0x00000000	PKA Memory Map 12 Register
CRYPTO_PKA_MEM_MAP13	0x0834	W	0x00000000	PKA Memory Map 13 Register
CRYPTO_PKA_MEM_MAP14	0x0838	W	0x00000000	PKA Memory Map 14 Register
CRYPTO_PKA_MEM_MAP15	0x083c	W	0x00000000	PKA Memory Map 15 Register
CRYPTO_PKA_MEM_MAP16	0x0840	W	0x00000000	PKA Memory Map 16 Register
CRYPTO_PKA_MEM_MAP17	0x0844	W	0x00000000	PKA Memory Map 17 Register
CRYPTO_PKA_MEM_MAP18	0x0848	W	0x00000000	PKA Memory Map 18 Register
CRYPTO_PKA_MEM_MAP19	0x084c	W	0x00000000	PKA Memory Map 19 Register
CRYPTO_PKA_MEM_MAP20	0x0850	W	0x00000000	PKA Memory Map 20 Register
CRYPTO_PKA_MEM_MAP21	0x0854	W	0x00000000	PKA Memory Map 21 Register
CRYPTO_PKA_MEM_MAP22	0x0858	W	0x00000000	PKA Memory Map 22 Register
CRYPTO_PKA_MEM_MAP23	0x085c	W	0x00000000	PKA Memory Map 23 Register
CRYPTO_PKA_MEM_MAP24	0x0860	W	0x00000000	PKA Memory Map 24 Register
CRYPTO_PKA_MEM_MAP25	0x0864	W	0x00000000	PKA Memory Map 25 Register
CRYPTO_PKA_MEM_MAP26	0x0868	W	0x00000000	PKA Memory Map 26 Register
CRYPTO_PKA_MEM_MAP27	0x086c	W	0x00000000	PKA Memory Map 27 Register
CRYPTO_PKA_MEM_MAP28	0x0870	W	0x00000000	PKA Memory Map 28 Register
CRYPTO_PKA_MEM_MAP29	0x0874	W	0x00000000	PKA Memory Map 29 Register
CRYPTO_PKA_MEM_MAP30	0x0878	W	0x00000000	PKA Memory Map 30 Register
CRYPTO_PKA_MEM_MAP31	0x087c	W	0x00000000	PKA Memory Map 31 Register
CRYPTO_PKA_OPCODE	0x0880	W	0x00000000	PKA Operation Code Register
CRYPTO_N_NP_TO_T1_ADDR	0x0884	W	0x000ff820	N_NP_TO_T1_ADDR Register
CRYPTO_PKA_STATUS	0x0888	W	0x00000001	PKA Status Register
CRYPTO_PKA_SW_RESET	0x088c	W	0x00000000	software reset of PKA
CRYPTO_PKA_L0	0x0890	W	0x00000000	PKA Length 0 Register
CRYPTO_PKA_L1	0x0894	W	0x00000000	PKA Length 1 Register
CRYPTO_PKA_L2	0x0898	W	0x00000000	PKA Length 2 Register
CRYPTO_PKA_L3	0x089c	W	0x00000000	PKA Length 3 Register
CRYPTO_PKA_L4	0x08a0	W	0x00000000	PKA Length 4 Register
CRYPTO_PKA_L5	0x08a4	W	0x00000000	PKA Length 5 Register
CRYPTO_PKA_L6	0x08a8	W	0x00000000	PKA Length 6 Register
CRYPTO_PKA_L7	0x08ac	W	0x00000000	PKA Length 7 Register
CRYPTO_PKA_PIPE_RDY	0x08b0	W	0x00000001	PKA pipe is ready for new opcode
CRYPTO_PKA_DONE	0x08b4	W	0x00000001	PKA Done Register
CRYPTO_PKA_MON_SELECT	0x08b8	W	0x00000000	PKA Monitor Select Register
CRYPTO_PKA_DEBUG_REG_EN	0x08bc	W	0x00000000	PKA Debug Enable Register
CRYPTO_DEBUG_CNT_ADDR	0x08c0	W	0x00000000	Debug Counter Address Register
CRYPTO_DEBUG_EXT_ADDR	0x08c4	W	0x00000000	Debug Extra Address Register

Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_DEBUG_HALT	0x08c8	W	0x00000000	PKA Debug Halt State Register
CRYPTO_PKA_MON_READ	0x08d0	W	0x0000feef	PKA Monitor Read Register
CRYPTO_PKA_INT_ENA	0x08d4	W	0x00000000	PKA Interrupt Enable Register
CRYPTO_PKA_INT_ST	0x08d8	W	0x00000000	PKA Interrupt Status Register
CRYPTO_SRAM_ADDR	0x1000	W	0x00000000	SRAM Base Address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.3.3 Detail Register Description

CRYPTO_CLK_CTL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x1	auto_clkgate_en 1: enable. CRYPTO will gate unused Block Cipher and HASH module automatically to save power. 0: disable. Symmetric Cipher and HASH Module clock will be always available.

CRYPTO_RST_CTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:3	RO	0x0	reserved
2	RW	0x0	sw_pka_reset Software set this bit to start a reset to PKA module. After the reset is done, CRYPTO will clear this bit.
1	RW	0x0	reserved
0	R/WSC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

CRYPTO_DMA_INT_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
7	RW	0x0	lockstep_flag_int_en 1: enable ; 0: disable;
6	RW	0x0	zero_len_int_en 1: enable ; 0: disable;
5	RW	0x0	list_err_int_en 1: enable ; 0: disable;
4	RW	0x0	src_err_int_en 1: enable ; 0: disable.
3	RW	0x0	dst_err_int_en 1: enable ; 0: disable;
2	RW	0x0	src_item_done_int_en 1: enable ; 0: disable.
1	RW	0x0	dst_item_done_int_en 1: enable ; 0: disable.
0	RW	0x0	list_done_int_en 1: enable ; 0: disable.

CRYPTO_DMA_INT_ST

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	W1C	0x0	sync_lockstep_flag Indicate that crypto was attacked. After the bit is read, the application should write 1 to clear this bit for next time use.
6	W1C	0x0	zero_len Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use.
5	W1C	0x0	list_err Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.

Bit	Attr	Reset Value	Description
4	W1C	0x0	src_err Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.
3	W1C	0x0	dst_err Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.
2	W1C	0x0	src_item_done Indicate that DMA has completed a read transfers which the current list descriptor pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.
1	W1C	0x0	dst_item_done Indicate that DMA has completed a write transfers which the current list descriptor pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.
0	W1C	0x0	list_done Indicate that DMA has completed all the transfers which the list descriptors pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_DMA_CTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0	reserved
1	R/WSC	0x0	dma_restart If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor . The application could restart DMA by asserting this bit when DMA data for next state is ready. Crypto will continue with previous transfer, and clear the bit automatically.
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then Crypto will clear the bit automatically .

CRYPTO_DMA_LLI_ADDR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	dma_lli_addr When DMA_CTL.start asserted, Crypto will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration.
2:0	RO	0x0	reserved

CRYPTO_DMA_ST

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	dma_busy 1: dma busy ; 0: dma idle ;

CRYPTO_DMA_STATE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RO	0x0	dma_lli_state For debug use only. 00: IDLE STATE; 01: FETCH STATE ; 10: WORK STATE ;
3:2	RO	0x0	dma_src_state For debug use only. 00: IDLE STATE; 01: LOAD STATE ; 10: WORK STATE ;
1:0	RO	0x0	dma_dst_state For debug use only. 00: IDLE STATE; 01: LOAD STATE ; 10: WORK STATE ;

CRYPTO_DMA_LLI_RADDR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lli_raddr For debug use only. It indicates the current dma lli read address.

CRYPTO_DMA_SRC_RADDR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_src_raddr For debug use only. It indicates the current dma source read address.

CRYPTO_DMA_DST_WADDR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_dst_waddr For debug use only. It indicates the current dma destination write address.

CRYPTO_DMA_ITEM_ID

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dma_item_id For debug use only. It indicates the current descriptor ID.

CRYPTO_FIFO_CTL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0	reserved
1	RW	0x1	dout_byteswap 1: little endian ; 0: big endian .
0	RW	0x1	din_byteswap 1: little endian ; 0: big endian .

CRYPTO_BC_CTL

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:16	WO	0x000	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:10	RO	0x0	reserved
9:8	RW	0x0	bc_cipher_sel 00: AES ; 01: SM4; 10: DES ; 11: TDES .
7:4	RW	0x0	mode FOR AES, 0x0: ECB ; 0x1: CBC ; 0x2: CTS ; 0x3: CTR ; 0x4: CFB ; 0x5: OFB ; 0x6: XTS ; 0x7: CCM; 0x8: GCM; 0x9: CMAC ; 0xA: CBC-MAC. Others: Reserved. For TDES/DES , 0x0: ECB ; 0x1: CBC ; 0x4: CFB ; 0x5: OFB ; Others: Reserved.
3:2	RW	0x0	key_size For AES , 00: 128 bit ; 01: 192 bit ; 10: 256 bit ; 11: reserved. For TDES/DES, it is reserved.
1	RW	0x0	decrypt 1: decrypt ; 0: encrypt .
0	RW	0x0	bc_enable 1: enable ; 0: disable .

CRYPTO_HASH_CTL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:8	RO	0x0	reserved
7:4	RW	0x0	hash_cipher_sel 0x0: SHA-1 ; 0x1: MD-5 ; 0x2: SHA-256 ; 0x3: SHA-224 ; 0x4: SM3 ; 0x8: SHA-512 ; 0x9: SHA-384 ; 0xA: SHA-512/224 ; 0xB: SHA-512/256 ; Others: Reserved.
3	RW	0x0	hmac_enable Crypto supports HMAC-SHA1, HMAC-SHA256, HMAC_SHA512, HMAC-MD5, HMAC-SM3. 1: enable ; 0: disable. Note: If hmac_enable set '1', hash_cipher_sel must set 0x6 when chose HMAC-SM3 mode; hash_cipher_sel set the corresponding value when chose other mode.
2	RW	0x1	hw_pad_enable 1: enable ; 0: disable .
1	RW	0x0	hash_src_sel 0: from RX-FIFO ; 1: from TX-FIFO .
0	RW	0x0	hash_enable 1: enable ; 0: disable.

CRYPTO_CIPHER_ST

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	hash_busy 1: busy ; 0: idle ;
0	RO	0x0	block_cipher_busy 1: busy ; 0: idle ;

CRYPTO_CIPHER_STATE

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:10	RW	0x01	hash_state For debug use only. 00001: IDLE State ; 00010: IPAD State ; 00100: TEXT State; 01000: OPAD State; 10000: OPAD EXT State .
9:8	RW	0x0	gcm_state For debug use only. 00: IDLE State; 01: PRE State; 10: NA State; 11: PC State.
7:6	RW	0x0	ccm_state For debug use only. 00: IDLE State; 01: PRE State; 10: NA State; 11: PC State.
5:4	RW	0x0	parallel_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved
3:2	RW	0x0	mac_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved

Bit	Attr	Reset Value	Description
1:0	RO	0x0	serial_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved

CRYPTO_CHn_IV_0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_0 Channel n range from 0 to 7. CHn_IV_0 address = 0x0100 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_1 Channel n range from 0 to 7. CHn_IV_1 address = 0x0104 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_2 Channel n range from 0 to 7. CHn_IV_2 address = 0x0108 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_3

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_3 Channel n range from 0 to 7. CHn_IV_3 address = 0x010c + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_KEY_0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_0 Channel n range from 0 to 7. CHn_KEY_0 address = 0x0180 + 0x10 * n .

CRYPTO_CHn_KEY_1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_1 Channel n range from 0 to 7. CHn_KEY_1 address = 0x0184 + 0x10 * n .

CRYPTO_CHn_KEY_2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_2 Channel n range from 0 to 7. CHn_KEY_2 address = 0x0188 + 0x10 * n .

CRYPTO_CHn_KEY_3

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_3 Channel n range from 0 to 7. CHn_KEY_3 address = 0x018c + 0x10 * n .

CRYPTO_CHn_PKEY_0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_pkey_0 Channel n range from 0 to 7. CHn_PKEY_0 address = 0x0200 + 0x10 * n .

CRYPTO_CHn_PKEY_1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_pkey_1 Channel n range from 0 to 7. CHn_PKEY_1 address = 0x0204 + 0x10 * n .

CRYPTO_CHn_PKEY_2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_pkey_2 Channel n range from 0 to 7. CHn_PKEY_2 address = 0x208 + 0x10 * n .

CRYPTO_CHn_PKEY_3

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_key_3 Channel n range from 0 to 7. CHn_PKEY_3 address = 0x020c + 0x10 * n .

CRYPTO_CHn_PC_LEN_0

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pc_len_0 Channel n range from 0 to 7. CHn_PC_LEN_0 address = 0x0280 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_PC_LEN_1

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_pc_len_1 Channel n range from 0 to 7. CHn_PC_LEN_1 address = 0x0284 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_ADA_LEN_0

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_ada_len_0 Channel n range from 0 to 7. CHn_ADA_LEN_0 address = 0x02c0 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_ADA_LEN_1

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:0	RW	0x00000000	chn_ada_len_1 Channel n range from 0 to 7. CHn_ADA_LEN_1 address = 0x02c4 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_IV_LEN_0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	chn_iv_len Channel n range from 0 to 7. CHn_IV_LEN_0 address = 0x0300 + 0x4 * n . Length in byte unit. Up to 16 byte IV for GCM

CRYPTO_CHn_TAG_0

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_0 Channel n range from 0 to 7. CHn_TAG_0 address = 0x0320 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_1

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_1 Channel n range from 0 to 7. CHn_TAG_1 address = 0x0324 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_2

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_2 Channel n range from 0 to 7. CHn_TAG_2 address = 0x0328 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_3

Address: Operational Base + offset (0x032c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_3 Channel n range from 0 to 7. CHn_TAG_3 address = 0x032c + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_HASH_DOUT_0

Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_0 0'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_1

Address: Operational Base + offset (0x03a4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_1 1'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_2

Address: Operational Base + offset (0x03a8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_2 2'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_3

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_3 3'th output word for all hash function, in big endian.This is MD5 last output word. HASH_DOUT_4 ~ HASH_DOUT_15 is invalid data for MD5.

CRYPTO_HASH_DOUT_4

Address: Operational Base + offset (0x03b0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_4 4'th output word for all hash function, in big endian.This is SHA-1 last output word. HASH_DOUT_5 ~ HASH_DOUT_15 is invalid data for SHA-1.

CRYPTO_HASH_DOUT_5

Address: Operational Base + offset (0x03b4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_5 5'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_6

Address: Operational Base + offset (0x03b8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_6 6'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_7

Address: Operational Base + offset (0x03bc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_7 7'th output word for all hash function, in big endian.This is SHA-256/224 last output word. HASH_DOUT_8 ~ HASH_DOUT_15 is invalid data for SHA-256/224.

CRYPTO_HASH_DOUT_8

Address: Operational Base + offset (0x03c0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_8 8'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_9

Address: Operational Base + offset (0x03c4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_9 9'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_10

Address: Operational Base + offset (0x03c8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_10 10'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_11

Address: Operational Base + offset (0x03cc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_11 11'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_12

Address: Operational Base + offset (0x03d0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_12 12'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_13

Address: Operational Base + offset (0x03d4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_13 13'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_14

Address: Operational Base + offset (0x03d8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_14 14'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_15

Address: Operational Base + offset (0x03dc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_15 15'th output word for all hash function, in big endian.This is SHA-512, SHA-384, SHA-512/224, SHA-512/256 last output word.

CRYPTO_TAG_VALID

Address: Operational Base + offset (0x03e0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	W1C	0x0	ch7_tag_valid When channel 7 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 7 tag is valid ; 0: channel 7 tag is invalid ;
6	W1C	0x0	ch6_tag_valid When channel 6 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 6 tag is valid ; 0: channel 6 tag is invalid ;
5	W1C	0x0	ch5_tag_valid When channel 5 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 5 tag is valid ; 0: channel 5 tag is invalid ;

Bit	Attr	Reset Value	Description
4	W1C	0x0	ch4_tag_valid When channel 4 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 4 tag is valid ; 0: channel 4 tag is invalid ;
3	W1C	0x0	ch3_tag_valid When channel 3 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 3 tag is valid ; 0: channel 3 tag is invalid ;
2	W1C	0x0	ch2_tag_valid When channel 2 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 2 tag is valid ; 0: channel 2 tag is invalid ;
1	W1C	0x0	ch1_tag_valid When channel 1 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 1 tag is valid ; 0: channel 1 tag is invalid ;
0	W1C	0x0	ch0_tag_valid When channel 0 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 0 tag is valid ; 0: channel 0 tag is invalid ;

CRYPTO_HASH_VALID

Address: Operational Base + offset (0x03e4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	hash_valid When HASH calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: HASH_DOUT is valid ; 0: HASH_DOUT is invalid ;

CRYPTO_VERSION

Address: Operational Base + offset (0x03f0)

Bit	Attr	Reset Value	Description
31:0	RO	0x01010010	version_num Version number: V1.0.0.1.

CRYPTO_RAM_CTL

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x0	ram_pka_rdy Indicate whether ram is controlled by PKA engine. 0: ram is controlled by CPU. 1: ram is controlled by CRYPTO PKA engine.

CRYPTO_RAM_ST

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	clk_ram_rdy Indicate whether clk_ram is stable, and ready for use. 0: not stable ; 1: stable.

CRYPTO_DEBUG_CTL

Address: Operational Base + offset (0x04a0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x0	pka_debug_mode 1: PKA is in debug mode ; 0: PKA is in normal mode.

CRYPTO_DEBUG_ST

Address: Operational Base + offset (0x04a4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_debug_clk_en For debug use only.

CRYPTO_DEBUG_MONITOR

Address: Operational Base + offset (0x04a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000feef	pka_monitor_bus For debug use only.

CRYPTO_PKA_MEM_MAP0

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map0 memory map 0 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP1

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map1 memory map 1 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP2

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map2 memory map 2 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP3

Address: Operational Base + offset (0x080c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map3 memory map 3 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP4

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map4 memory map 4 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP5

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map5 memory map 5 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP6

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map6 memory map 6 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP7

Address: Operational Base + offset (0x081c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map7 memory map 7 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP8

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map8 memory map 8 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP9

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map9 memory map 9 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP10

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map10 memory map 10 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP11

Address: Operational Base + offset (0x082c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map11 memory map 11 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP12

Address: Operational Base + offset (0x0830)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map12 memory map 12 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP13

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map13 memory map 13 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP14

Address: Operational Base + offset (0x0838)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map14 memory map 14 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP15

Address: Operational Base + offset (0x083c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map15 memory map 15 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP16

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map16 memory map 16 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP17

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map17 memory map 17 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP18

Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map18 memory map 18 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP19

Address: Operational Base + offset (0x084c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map19 memory map 19 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP20

Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map20 memory map 20 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP21

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map21 memory map 21 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP22

Address: Operational Base + offset (0x0858)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map22 memory map 22 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP23

Address: Operational Base + offset (0x085c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map23 memory map 23 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP24

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map24 memory map 24 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP25

Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map25 memory map 25 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP26

Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map26 memory map 26 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP27

Address: Operational Base + offset (0x086c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map27 memory map 27 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP28

Address: Operational Base + offset (0x0870)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map28 memory map 28 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP29

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map29 memory map 29 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP30

Address: Operational Base + offset (0x0878)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map30 memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP31

Address: Operational Base + offset (0x087c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map31 memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_OPCODE

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:27	WO	0x00	opcode Defines the PKA operation 0x04 Add,Inc 0x05 Sub,Dec,Neg 0x06 ModAdd,ModInc 0x07 ModSub,ModDec,ModNeg 0x08 AND,TST0,CLR0 0x09 OR,COPY,SET0 0xa XOR,FLIP0,INVERT,COMPARE 0xc SHR0 0xd SHR1 0xe SHL0 0xf SHL1 0x10 MulLow 0x11 ModMul 0x12 ModMulN 0x13 ModExp 0x14 Division 0x15 Div 0x16 ModDiv 0x00 Terminate
26:24	WO	0x0	len The virtual length address 0-7. Virtual address 0 point to PKA_L0. Virtual address 1 point to PKA_L1. ... Virtual address 7 point to PKA_L7.
23:18	WO	0x00	reg_a Operand A virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
17:12	WO	0x00	reg_b Operand B virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
11:6	WO	0x00	reg_r Result register virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.

Bit	Attr	Reset Value	Description
5:0	WO	0x00	tag Tag.

CRYPTO_N_NP_TO_T1_ADDR

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x1f	reg_t1 Virtual address of temporary register number 1. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
14:10	RW	0x1e	reg_t0 Virtual address of temporary register number 0. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
9:5	RW	0x01	reg_np Virtual address of register np. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
4:0	RW	0x00	reg_n Virtual address of register n. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.

CRYPTO_PKA_STATUS

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:14	RO	0x00	tag Tag of the Last Operation.
13:9	RO	0x00	opcode the last OPCODE.
8	RO	0x0	pka_cpu_busy PKA is busy memory control is by PKA.
7	RO	0x0	modinv_of_zero modular inverse of zero flag.

Bit	Attr	Reset Value	Description
6	RO	0x0	alu_sign_out sign of the last operation(MSB).
5	RO	0x0	alu_carry Carry of the last ALU operation.
4	RO	0x0	div_by_zero Division by 0.
3	RO	0x0	alu_mod_ovflw Modular overflow flag.
2	RO	0x0	alu_out_zero ALU out is 0.
1	RO	0x0	pka_busy PKA is busy.
0	RO	0x1	pipe_is_busy PKA ready signal 0 : pipe full 1 : PKA ready for new command.

CRYPTO_PKA_SW_RESET

Address: Operational Base + offset (0x088c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	pka_sw_reset PKA software reset the reset mechanism will take about four PKA clocks until the reset line is de-asserted.

CRYPTO_PKA_L0

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l0 PKA length 0, in bit unit.

CRYPTO_PKA_L1

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l1 PKA length 1, in bit unit.

CRYPTO_PKA_L2

Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l2 PKA length 2, in bit unit.

CRYPTO_PKA_L3

Address: Operational Base + offset (0x089c)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l3 PKA length 3, in bit unit.

CRYPTO_PKA_L4

Address: Operational Base + offset (0x08a0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l4 PKA length 4, in bit unit.

CRYPTO_PKA_L5

Address: Operational Base + offset (0x08a4)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l5 PKA length 5, in bit unit.

CRYPTO_PKA_L6

Address: Operational Base + offset (0x08a8)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l6 PKA length 6, in bit unit.

CRYPTO_PKA_L7

Address: Operational Base + offset (0x08ac)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l7 PKA length 7, in bit unit.

CRYPTO_PKA_PIPE_RDY

Address: Operational Base + offset (0x08b0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_pipe_rdy PKA pipe is ready for new opcode

CRYPTO_PKA_DONE

Address: Operational Base + offset (0x08b4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_done PKA operation is completed and pipe is empty.

CRYPTO_PKA_MON_SELECT

Address: Operational Base + offset (0x08b8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	pka_mon_select PKA monitor select which PKA fsm monitor is being output.

CRYPTO_PKA_DEBUG_REG_EN

Address: Operational Base + offset (0x08bc)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pka_debug_reg_en Enable all the debug mechanism when set.

CRYPTO_DEBUG_CNT_ADDR

Address: Operational Base + offset (0x08c0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	R/WSC	0x00000	debug_cnt_addr The clock counter initial values. clock is disabled when counter expires. Triggered when pka_debug_en is set.

CRYPTO_DEBUG_EXT_ADDR

Address: Operational Base + offset (0x08c4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	debug_ext_addr Disable the debug Mechanism

CRYPTO_PKA_DEBUG_HALT

Address: Operational Base + offset (0x08c8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	pka_debug_halt In debug mode: PKA is in halt state.

CRYPTO_PKA_MON_READ

Address: Operational Base + offset (0x08d0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_mon_read This is the PKA monitor bus register output.

CRYPTO_PKA_INT_ENA

Address: Operational Base + offset (0x08d4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pka_int_ena 1: enable pka interrupt. 0: disable pka interrupt

CRYPTO_PKA_INT_ST

Address: Operational Base + offset (0x08d8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	pka_int_st Indicate that PKA operation completes . After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_SRAM_ADDR

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sram_addr Sram address starts from 0x1000 to 0x1fff. When RAM_CTL.ram_pka_rdy == 0, application could access sram. Otherwise, application can't .

4.4 Application Note

4.4.1 Clock & Reset

There are 4 clock domains in Crypto. The clock and reset signals are described in the following table .

Table 4-1 Crypto Clock & Reset Description

Signal	Attr	Description
hclk	clock	AHB clock
aclk	clock	AXI master clock
clk_core	clock	Cipher work clock
clk_pka	clock	PKA work clock

Signal	Attr	Description
hresetn	reset	Asynchronously assert, synchronously de-assert to hclk, low active
aresetn	reset	Asynchronously assert, synchronously de-assert to aclk, low active
resetn_core	reset	Asynchronously assert, synchronously de-assert to clk_core, low active
resetn_pka	reset	Asynchronously assert, synchronously de-assert to clk_pka, low active

Each function need different clocks. The applications could gate the un-used clock to save power. Please see the following table for detail information.

Table 4-2 Crypto Clock & Reset Description

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
AES	ON	ON	ON	OFF
DES/TDES	ON	ON	ON	OFF
SM4	ON	ON	ON	OFF
HASH/HMAC	ON	ON	ON	OFF
PKA	ON	OFF	OFF	ON

Even when CLK_CORE is on, Crypto is doing some cipher job. And Crypto could still be able to automatically gate most parts of un-used blocks to save more power, if CRYPTO_CLK_CTL.auto_clkgate_en is set to '1' . The default value for this bit is also '1' .
Application could do a soft reset to a certain clock domain. Please refer to "Chapter CRU" for more details.

4.4.2 Performance

Cipher performance is shown in the following table.

Table 4-3 Crypto Performance Description

Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
DES	8	200	18	88	352
TDES	8	200	55	29	116
AES-128	16	200	12	266	1066
AES-192	16	200	14	228	914
AES-256	16	200	16	200	800
SM4	16	200	34	94	376
SM3	64	200	66	194	NA
SHA-1	64	200	81	158	NA
MD5	64	200	65	196	NA
SHA-256/224	64	200	65	196	NA
SHA-512/384/ 512_224/ 512_256	128	200	81	316	NA

There are 2 column throughput rates in the table, 1 is serial mode, the other is parallel mode. In parallel mode, there are 4 engines working at the same time . So the speed is 4 times than serial mode. Parallel mode includes ECB/CTR/XTS both encryption and decryption mode, CFB/CBC/CTS only decryption mode. Other modes are serial. HASH doesn't have parallel mode.
For PKA, the cycles for each calculation are not certain. It depends on the parameters. Take RSA-2048 for example, it takes about 28M cycles to finish a calculation. PKA can run 300 Mhz. It means it can run over 10 times per second.

4.4.3 DMA

DMA supports Link List Item (LLI) DMA transaction.

- Each item contains 8 bytes, and start address should be 8 bytes align ;
- We suggest that DATA start address is 8 bytes align ;

- Total DATA length is byte align.
- Support segmenting HASH/HMAC DATA into multi sections. We suggest that each section DATA length is a multiple of 64 bytes, except this section is the last section.

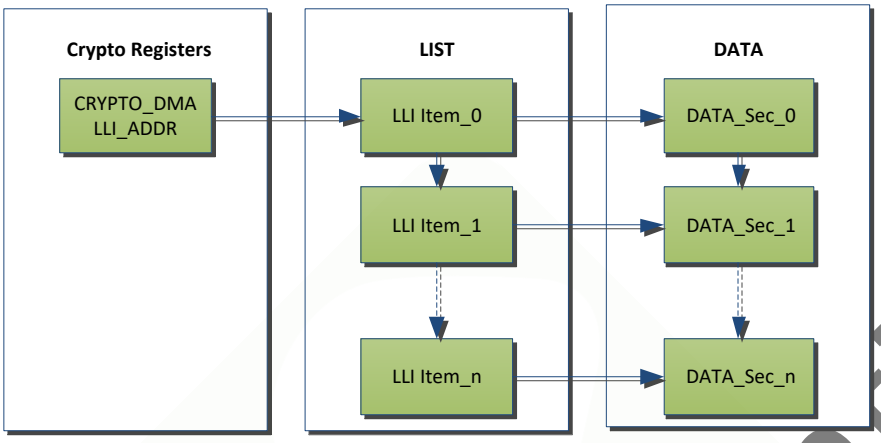


Fig.4-2 LLI DMA Usage

As shown in the Figure above, Register CRYPTO_DMA_LLI_ADDR points to 1'st LLI item in external memory. Each LLI item contains DATA address, length, control information and next LLI item pointer, except the last LLI item. The last item doesn't have the next LLI Item pointer. After the last LLI item is finished , DMA will go to idle state.
LLI item definition is shown in the following table.

Table 4-4 LLI Item Description

offset	Def	Description
0x00	SRC_ADDRESS[31:0]	Source data start address
0x04	SRC_LENGTH[31:0]	Source data length，in byte unit
0x08	DST_ADDRESS[31:0]	Destination data start address
0x0c	DST_LENGTH[31:0]	Destination data length，in byte unit
0x10	USER_DEFINE[31:0]	Used in cipher block
0x14	Reserved	Reserved
0x18	DMA_CTRL[31:0]	Used in DMA block
0x1c	NEXT_ADDRESS[31:0]	Next LLI item address. When DMA_CTRL.LAST = "1"，NEXT_ADDRESS is invalid.

DMA_CTRL: the definition is shown in the following table.

Table 4-5 LLI Item dma_ctl Description

Bit	Def	Definition
[31:24]	ITEM_ID[7:0]	Used to identify LLI items.
[23:16]	Reserved	Reserved
[15:11]	Reserved	Reserved
10	Source_item_done enable	When source data fetch is completed, CRYPTO_DMA_INT_ST.source_item_done will assert if this bit is set.
9	Dst_item_done enable	When destination data fetch is completed, CRYPTO_DMA_INT_ST.dst_item_done will assert if this bit is set.
8	List_done enable	When all LLI items transfer is completed, CRYPTO_DMA_INT_ST.list_done will assert if this bit is set.

Bit	Def	Definition
[7:2]	Reserved	Reserved
1	PAUSE	Indicate DMA will hold on after executes current item. DMA won't go on unless CRYPTO_DMA_CTL.restart is configured
0	LAST	Indicate current item is the last one. After executes current item, DMA will return to IDLE state.

Table 4-6 LLI Item user_define Description

Bit	Signal	Description
31:7	Reserved	Reserved
6:4	Chnl_num	channel number, from 0 to 7 .
3	String_attr	indicate current item's attribution. 1: ADA ; 0: PC(plaintext or ciphertext)
2	String_last	indicate current item is the string last item
1	String_start	indicate current item is the string first item
0	Cipher_start	indicate current item is the cipher first item

4.4.4 Multi-Channel Map

There are 8-channel configurations for AES or DES/TDES operation. For different key-size, the map is different. Please find the register map in the following table.

Table 4-7 LLI Item user_define Description

Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/...)
AES-128/ DES	0	0	0	CH0_KEY0-3/ CH0_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	0	n	CHn_KEY0-3/ CHn_KEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	0	7	CH7_KEY0-3/ CH7_KEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	0	1	0	CH0_PKEY0-3/ CH0_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	1	n	CHn_PKEY0-3/ CHn_PKEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	1	7	CH7_PKEY0-3/ CH7_PKEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	1	NA	0	OTP_KEY[255:128]	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	1	NA	n	OTP_KEY[127:0]	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	1	NA	7	OTP_KEY[127:0]	CH7_IV0-3/ CH7_IV0-1
AES-192/ TDES	0	0	0	CH0_KEY0-3, CH1_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	0	1	CH2_KEY0-3, CH3_KEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	0	0	2	CH4_KEY0-3, CH5_KEY0-1	CH2_IV0-3/ CH2_IV0-1

Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/...)
AES-192/ TDES	0	0	3	CH6_KEY0-3, CH7_KEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/ TDES	0	1	0	CH0_PKEY0-3, CH1_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	1	1	CH2_PKEY0-3, CH3_PKEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	0	1	2	CH4_PKEY0-3, CH5_PKEY0-1	CH2_IV0-3/ CH2_IV0-1
AES-192/ TDES	0	1	3	CH6_PKEY0-3, CH7_PKEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/ TDES	0	NA	4-7	not supported	not supported
AES-192/ TDES	1	NA	0	OTP[255:64]	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	1	NA	1-7	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH1_IV0-3/ CH1_IV0-1
AES-256	0	0	2	CH4_KEY0-3, CH5_KEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	0	3	CH6_KEY0-3, CH7_KEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH1_IV0-3/ CH1_IV0-1
AES-256	0	1	2	CH4_PKEY0-3, CH5_PKEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	1	3	CH6_PKEY0-3, CH7_PKEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	NA	4-7	not supported	not supported
AES-256	1	NA	0	OTP[255:0]	CH0_IV0-3/ CH0_IV0-1
AES-256	1	NA	1-7	not supported	not supported

In AES-XTS mode, there are 2 keys, and only AES-128 and AES-256 mode are. Please refer to the following table for detail information.

Table 4-8 LLI Item user_define Description

Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-128	0	0	0	CH0_KEY0-3	CH4_KEY0-3	CH0_IV0-3
AES-128	0	0	1	CH1_KEY0-3	CH5_KEY0-3	CH1_IV0-3
AES-128	0	0	2	CH2_KEY0-3	CH6_KEY0-3	CH2_IV0-3

Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-128	0	0	3	CH3_KEY0-3	CH7_KEY0-3	CH3_IV0-3
AES-128	0	1	0	CH0_PKEY0-3	CH4_PKEY0-3	CH0_IV0-3
AES-128	0	1	1	CH1_PKEY0-3	CH5_PKEY0-3	CH1_IV0-3
AES-128	0	1	2	CH2_PKEY0-3	CH6_PKEY0-3	CH2_IV0-3
AES-128	0	1	3	CH3_PKEY0-3	CH7_PKEY0-3	CH3_IV0-3
AES-128	0	NA	4-7	not supported	not supported	not supported
AES-128	1	NA	NA	not supported	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH4_KEY0-CH5_KEY3	CH0_IV0-3
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH6_KEY0-CH7_KEY3	CH1_IV0-3
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH4_PKEY0-CH5_PKEY3	CH0_IV0-3
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH6_PKEY0-CH7_PKEY3	CH1_IV0-3
AES-256	0	NA	2-7	not supported	not supported	not supported
AES-256	1	NA	NA	not supported	not supported	not supported

Note: The difference between CHn_KEY and CHn_PKEY is that: CHn_KEY could be read/write, CHn_PKEY could be write , but can't be read . The read value for CHn_PKEY is all '0'.

4.4.5 HASH Data Path

HASH and AES could run in parallel way. There are 2 paths lead to AES-HASH function. One is AES-HASH-RX mode, the other is AES-HASH-TX mode.

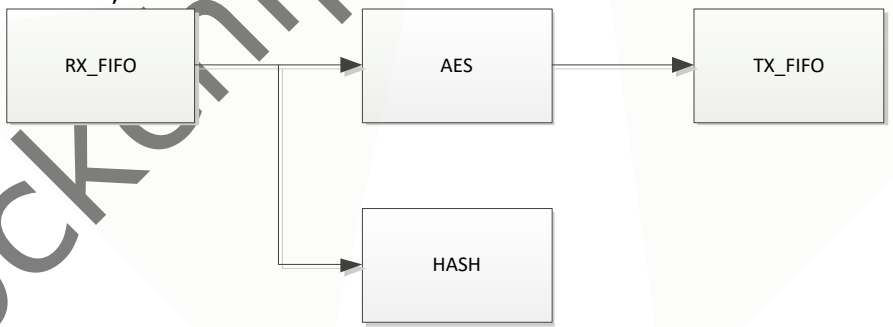


Fig.4-3 AES-HASH-RX mode

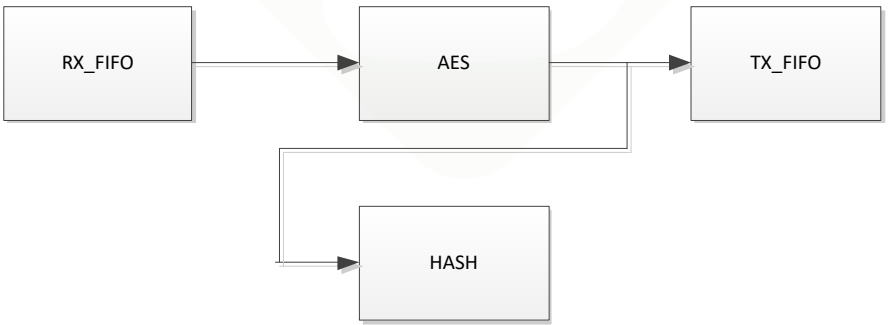


Fig.4-4 AES-HASH-TX mode

As shown in the figures above, we could facilitate operations in some cases. For example, secure boot, we need both AES and HASH operations for the same blocks of data. The data HASH gets from RX_FIFO or TX_FIFO is byteswaped if the byteswap function is configured.

4.4.6 Program Steps

The application could succeed various crypto operations if they program properly.

- Program the LLI address to DMA_LLI_ADDR;
- Program KEY , IV, or other parameter if needed ;
- Program BC_CTL or HASH_CTL for control information;
- Prepare LLI Item;
- Enable interrupt, or do nothing.

All these operations could be in any order.

- Program DMA_CTL.start to start the operation;

This step should be the last configuration step. After this register is configured, other registers should not be changed.

- Wait interrupt asserted, or just poll the DMA_INT_ST bits .
- Program DMA_INT_ST to clear interrupt status, and get the result.

The application could also use LLI.pause when the next LLI item is not ready. After the new item is prepared, the application could program DMA_CTL.restart to continue previous operation.

Chapter 5 True Random Number Generator(TRNG)

5.1 Overview

TRNG is a true random number generator to generate random number:

- A 32 bits AHB slave
- The generated random number length can be configured as 64bits 128bits, 192bits and 256 bits
- OSC is available in four lengths
- The sampling period for random number per bit is available

5.2 Block Diagram

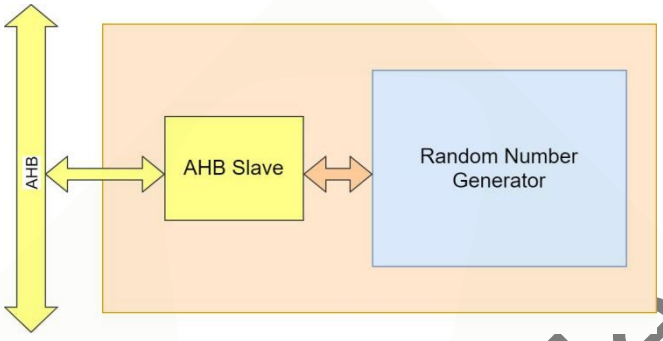


Fig. 5-1 TRNG Block Diagram

TRNG is comprised of:

- AHB Slave

The AHB slave implements the AHB slave operation. Its data bus width is 32 bits.

- Random Number Generator

The Random Number Generator generate true random number according to register configuration.

5.3 Function Description

5.3.1 Operation

- **True random number generate**

User first configures the RNG_SAMPLE_CNT and RNG_CTL register, excluding the rng_start field of the RNG_CTL register. The rng_start field of the RNG_CTL register is then finally configured to start the random number generation. Wait until the rng_start field of the RST_CTL register reads out a value of 0, which indicates that the random number is generated.

- **Reset operation**

User write 0x00020002 to RST_CTL register. Then, wait until the RST_CTL register reads out a value of 0. After these operations, TRNG clear RNG_DOUT and the internal state.

5.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

5.4.1 Registers Summaryc

Name	Offset	Size	Reset Value	Description
TRNG_RST_CTL	0x0004	W	0x00000000	Reset Control Register
TRNG_RNG_CTL	0x0400	W	0x0000000C	RNG Control Register
TRNG_RNG_SAMPLE_CNT	0x0404	W	0x00000000	RNG Sample Counter Register
TRNG_RNG_DOUT_0	0x0410	W	0x00000000	RNG Data Output Register 0
TRNG_RNG_DOUT_1	0x0414	W	0x00000000	RNG Data Output Register 1
TRNG_RNG_DOUT_2	0x0418	W	0x00000000	RNG Data Output Register 2
TRNG_RNG_DOUT_3	0x041C	W	0x00000000	RNG Data Output Register 3
TRNG_RNG_DOUT_4	0x0420	W	0x00000000	RNG Data Output Register 4
TRNG_RNG_DOUT_5	0x0424	W	0x00000000	RNG Data Output Register 5
TRNG_RNG_DOUT_6	0x0428	W	0x00000000	RNG Data Output Register 6
TRNG_RNG_DOUT_7	0x042C	W	0x00000000	RNG Data Output Register 7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Double WORD (64 bits) access

5.4.2 Detail Register Description

TRNG_RST_CTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
16:2	RO	0x0000	reserved
1	R/WSC	0x0	sw_rng_reset Software set this bit to start a reset to TRNG module. After the reset is done, CRYPTO will clear this bit.
0	RO	0x0	reserved

TRNG_RNG_CTL

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:6	RO	0x000	reserved
5:4	RW	0x0	rng_len 2'b00: 64 bit 2'b01: 128 bit 2'b10: 192 bit 2'b11: 256 bit
3:2	RW	0x3	ring_sel There are 4 osc rings choice to decide the rng output data. 2'b00: Slowest osc ring 2'b01: faster than osc ring 0 2'b10: faster than osc ring 1 2'b11: fastest osc ring
1	RW	0x0	rng_enable 1'b1: Enable 1'b0: Disable
0	R/WSC	0x0	rng_start The application triggers this bit to start collect rng output data. After rng is started, CRYPTO will clear the bit automatically. 1'b1: Start 1'b0: Do nothing

TRNG_RNG_SAMPLE_CNT

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rng_sample_cnt RNG collects osc ring output bit every rng_sample_cnt time. The value of rng_sample_cnt affects RNG output data rate, the value more bigger, the rate more slower.

TRNG_RNG_DOUT_0

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_0 The 32'th osc ring bit is captured in RNG_DOUT_0.bit31.

TRNG_RNG_DOUT_1

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_1 The 64'th osc ring bit is captured in RNG_DOUT_1.bit31. If RNG_CTL.rng_len = 0x00, the last valid bit of RNG is stored in RNG_DOUT_1.bit31, and RNG_DOUT_2 ~ RNG_DOUT_7 are invalid.

TRNG_RNG_DOUT_2

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_2 The 96'th osc ring bit is captured in RNG_DOUT_2.bit31.

TRNG_RNG_DOUT_3

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_3 The 128'th osc ring bit is captured in RNG_DOUT_3.bit31. If RNG_CTL rng_len = 0x01, the last valid bit of RNG is stored in RNG_DOUT_3.bit31, and RNG_DOUT_4 ~ RNG_DOUT_7 are invalid.

TRNG_RNG_DOUT_4

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_4 The 160'th osc ring bit is captured in RNG_DOUT_4.bit31.

TRNG_RNG_DOUT_5

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_5 The 192'th osc ring bit is captured in RNG_DOUT_5.bit31. If RNG_CTL.rng_len = 0x02, the last valid bit of RNG is stored in RNG_DOUT_5.bit31, and RNG_DOUT_6~ RNG_DOUT_7 are invalid.

TRNG_RNG_DOUT_6

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_6 The 224'th osc ring bit is captured in RNG_DOUT_6.bit31.

TRNG_RNG_DOUT_7

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_7 The 256'th osc ring bit is captured in RNG_DOUT_7.bit31. If RNG_CTL.rng_len = 0x03, the last valid bit of RNG is stored in RNG_DOUT_7.bit31.

5.5 Application Notes

- When random numbers do not meet randomness requirements, user can resolve the problem by adjusting the RNG_SAMPLE_CNT register and ring_sel field of RNG_CTL register.

Chapter 6 Mobile Storage Host Controller

6.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.

The Host Controller is instantiated for SDMMC0, SDMMC1, SDMMC2. The interface difference between these instances is shown in "Interface Description".

The Host Controller supports following features:

- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single engine used for Transmit and Receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support Secure Digital memory protocol commands
  - Support Secure Digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support Command Completion Signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support card detection
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit, 4-bit modes
  - Supports 4-bit DDR
  - Support boot in 1-bit and 4-bit SDR modes
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
  - Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively. The max number of delay element number is 256

6.2 Block Diagram

The Host Controller consists of the following main functional blocks.

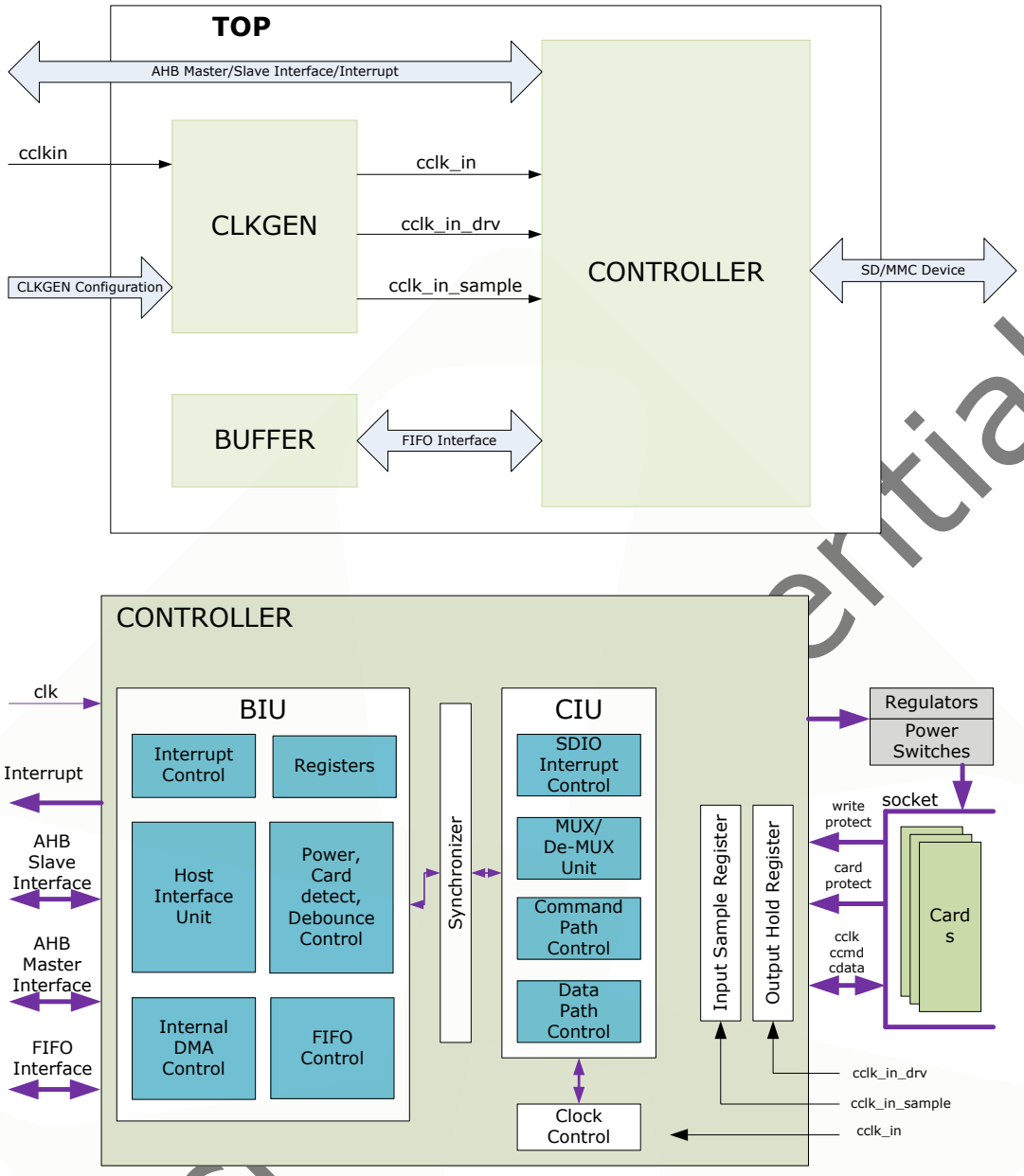


Fig. 6-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

6.3 Function Description

6.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access

- Power control and card detection

6.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

6.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD – Command
- SDMMC_CMDARG – Command Argument
- SDMMC_BYTCNT – Byte Count
- SDMMC_BLKSIZ – Block Size
- SDMMC_CLKDIV – Clock Divider
- SDMMC_CLKENA – Clock Enable
- SDMMC_CLKSRC – Clock Source
- SDMMC_TMOUT – Timeout
- SDMMC_CTYPE – Card Type

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:

3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.
- If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

6.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.

The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.

The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.

Notes:

Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.
The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 6-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period.

Bits	Interrupt	Description
		Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.

4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level.
		Recommendation:
		In DMA modes, this interrupt should not be enabled.
		In non-DMA mode:
		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation:

Bits	Interrupt	Description
		In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

6.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock(clk), and the second port is connected to the card clock(cclk_in).

Notes: The FIFO controller does not support simultaneous read/write access from the same port. For debugging purposes, the software may try to write into the FIFO and read back the data; results are indeterminate, since the design does not support read/write access from the same port.

6.3.1.5 Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

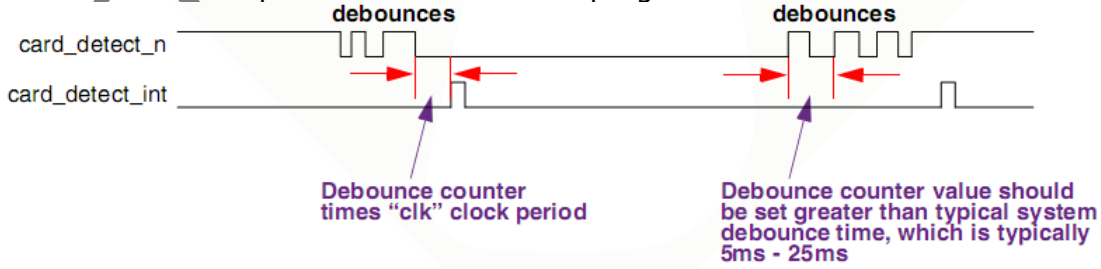


Fig. 6-2 SD/MMC Card-Detect Signal

6.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

6.3.2.1 Command Path

The command path performs the following functions:

- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.
- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:

- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

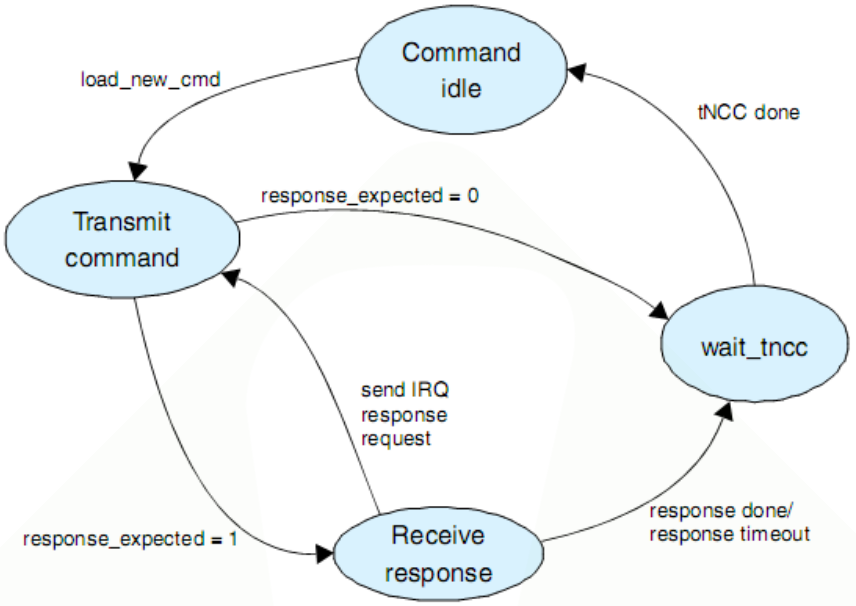


Fig. 6-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU

If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller

of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

6.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

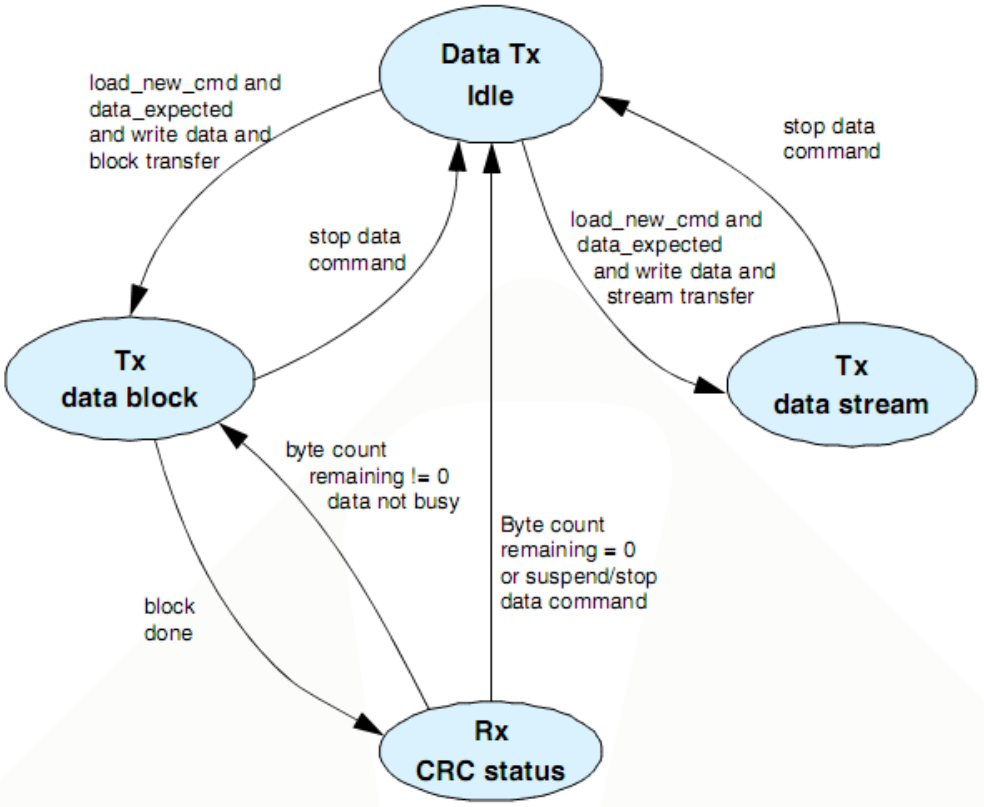


Fig. 6-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register.

Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

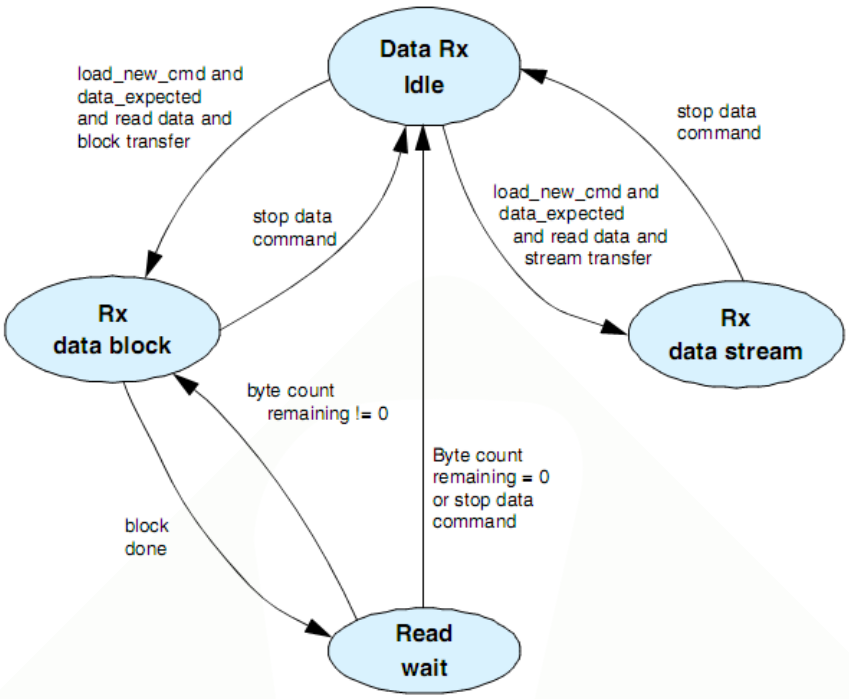


Fig. 6-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full. An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.

If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 6-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block	>0	No	Pre-defined multiple block

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	write			

*①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.
- Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

6.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 6-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

6.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.
- Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

6.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.
- Clock Control register – cclk_out can be enabled or disabled for each card under the

following conditions:

- clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
- Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.
- FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

6.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.
- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU
  - Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
  - Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.

- Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.
- Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

6.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

6.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.

You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

6.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

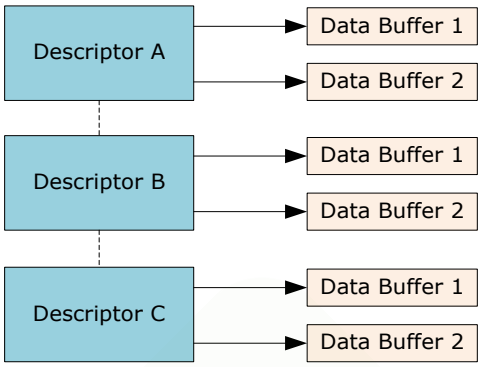


Fig. 6-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

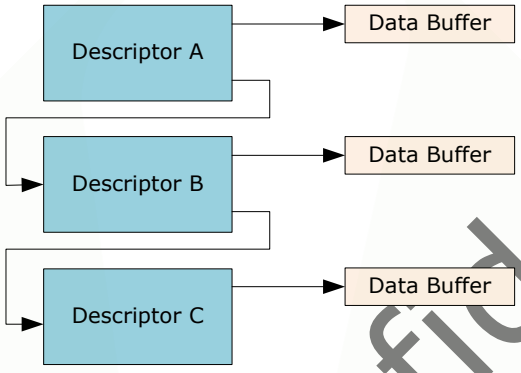


Fig. 6-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

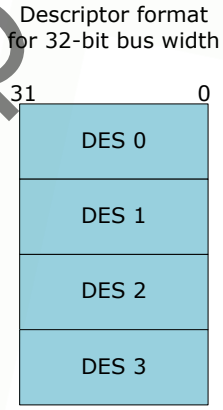


Fig. 6-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 6-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits:

Bit	Name	Description
		● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

■ The DES1 element contains the buffer size.

Table 6-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

■ The DES2 element contains the address pointer to the data buffer.

Table 6-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus

Bit	Name	Description
		widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 6-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

6.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the

descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer. An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

6.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 25ps~56ps for every delay element; the max delay element number is 256.
The architecture is as follows.

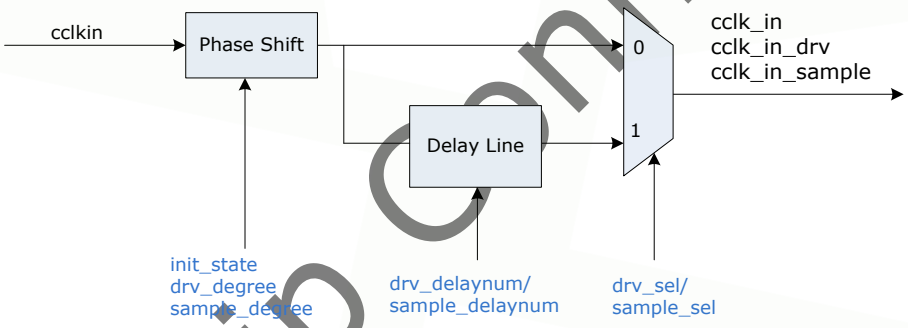


Fig. 6-9 Clock Generation Unit

6.4 Register Description

6.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000c	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001c	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register
SDMMC_CMD	0x002c	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003c	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register

Name	Offset	Size	Reset Value	Description
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004c	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005c	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x00000000	User ID register
SDMMC_VERID	0x006c	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008c	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010c	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

6.4.2 Detail Register Description

SDMMC_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer
24:12	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.

Bit	Attr	Reset Value	Description
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit. 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	WO	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	WO	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
0	WO	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card.

SDMMC_CMD

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.

Bit	Attr	Reset Value	Description
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved

Bit	Attr	Reset Value	Description
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)

Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response.

SDMMC_RESP3

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response.

SDMMC_MINTSTS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set.
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	WO	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	WO	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
15:0	WO	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy.
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status

Bit	Attr	Reset Value	Description
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card.

SDMMC_TBBCNT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO.

SDMMC_DEBNCE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usrid User identification register

SDMMC_VERID

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: DW_DMA 2'b10: GENERIC_DMA 2'b11: NON-DW-DMA
15:10	RO	0x1f	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ..... 6'h1f: 32 bits others: Reserved
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits others: Reserved

Bit	Attr	Reset Value	Description
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

SDMMC_IDSTS

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

SDMMC_CARDTHRCTL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if zcard_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_FIFO_BASE

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

6.5 Interface Description

6.5.1 SDMMC0 Interface Description

Table 6-8 SDMMC Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc0_cclk	O	SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1/GPIO2_A2_d	GRF_GPIO2A_IOMUX_L[11:8]=4'h1
sdmmc0_ccmd	I/O	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	GRF_GPIO2A_IOMUX_L[7:4]=4'h1
sdmmc0_cdata0	I/O	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	GRF_GPIO1D_IOMUX_H[7:4]=4'h1
sdmmc0_cdata1	I/O	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	GRF_GPIO1D_IOMUX_H[11:8]=4'h1
sdmmc0_cdata2	I/O	SDMMC0_D2/JTAG_TCK/UART5_CTSn_M0/GPIO1_D7_u	GRF_GPIO1D_IOMUX_H[15:12]=4'h1
sdmmc0_cdata3	I/O	SDMMC0_D3/JTAG_TMS/UART5_RTSn_M0/GPIO2_A0_u	GRF_GPIO2A_IOMUX_L[3:0]=4'h1
sdmmc0_cdetn	I	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	PMU_GRF_GPIO0A_IOMUX_H[3:0]=4'h1
sdmmc0_pwr	O	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	PMU_GRF_GPIO0A_IOMUX_H[7:4]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

6.5.2 SDMMC1 Interface Description

Table 6-9 SDIO Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc1_cclk	O	SDMMC1_CLK/GMAC0_TXCLK/UART9_TX_M0/GPIO2_B0_d	GRF_GPIO2B_IOMUX_L[3:0]=4'h1
sdmmc1_ccmd	I/O	SDMMC1_CMD/GMAC0_TXD3/UART9_RX_M0/GPIO2_A7_u	GRF_GPIO2A_IOMUX_H[15:12]=4'h1
sdmmc1_cdata0	I/O	SDMMC1_D0/GMAC0_RXD2/UART6_RX_M0/GPIO2_A3_u	GRF_GPIO2A_IOMUX_L[15:12]=4'h1
sdmmc1_cdata1	I/O	SDMMC1_D1/GMAC0_RXD3/UART6_TX_M0/GPIO2_A4_u	GRF_GPIO2A_IOMUX_H[3:0]=4'h1
sdmmc1_cdata2	I/O	SDMMC1_D2/GMAC0_RXCLK/UART7_RX_M0/GPIO2_A5_u	GRF_GPIO2A_IOMUX_H[7:4]=4'h1
sdmmc1_cdata3	I/O	SDMMC1_D3/GMAC0_TXD2/UART7_TX_M0/GPIO2_A6_u	GRF_GPIO2A_IOMUX_H[11:8]=4'h1
sdmmc1_cdetn	I	SDMMC1_DET/I2C4_SCL_M1/UART8_CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	GRF_GPIO2B_IOMUX_L[11:8]=4'h1
sdmmc1_pwr	O	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	GRF_GPIO2B_IOMUX_L[7:4]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

6.5.3 SDMMC2 Interface Description

Table 6-10 SDMMC2 M0 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc2_cclk	O	CIF_D5/EBC_SDDO5/SDMMC2_CLK_M0/I2S1_SDI1_M1/VOP_BT656_D5_M1/GPIO3_D3_d	GRF_GPIO3D_IOMUX_L[15:12]=4'h3
sdmmc2_ccmd	I/O	CIF_D4/EBC_SDDO4/SDMMC2_CMD_M0/I2S1_SDI0_M1/VOP_BT656_D4_M1/GPIO3_D2_d	GRF_GPIO3D_IOMUX_L[11:8]=4'h3
sdmmc2_cdata0	I/O	CIF_D0/EBC_SDDO0/SDMMC2_D0_M0/I2S1_MCLK_M1/VOP_BT656_D0_M1/GPIO3_C6_d	GRF_GPIO3C_IOMUX_H[11:8]=4'h3
sdmmc2_cdata1	I/O	CIF_D1/EBC_SDDO1/SDMMC2_D1_M0/I2S1_SCLK_TX_M1/VOP_BT656_D1_M1/GPIO3_C7_d	GRF_GPIO3C_IOMUX_H[15:12]=4'h3

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc2_cdata2	I/O	CIF_D2/EBC_SDDO2/SDMMC2_D2_M0/I2S1_LRCK_TX_M1/VOP_BT656_D2_M1/GPIO3_D0_d	GRF_GPIO3D_IOMUX_L[3:0]=4'h3
sdmmc2_cdata3	I/O	CIF_D3/EBC_SDDO3/SDMMC2_D3_M0/I2S1_SDO0_M1/VOP_BT656_D3_M1/GPIO3_D1_d	GRF_GPIO3D_IOMUX_L[7:4]=4'h3
sdmmc2_cdetn	I	CIF_D6/EBC_SDDO6/SDMMC2_DET_M0/I2S1_SDI2_M1/VOP_BT656_D6_M1/GPIO3_D4_d	GRF_GPIO3D_IOMUX_H[3:0]=4'h3
sdmmc2_pwr	O	CIF_D7/EBC_SDDO7/SDMMC2_PWREN_M0/I2S1_SDI3_M1/VOP_BT656_D7_M1/GPIO3_D5_d	GRF_GPIO3D_IOMUX_H[7:4]=4'h3

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 6-11 SDMMC2 M1 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc2_cclk	O	LCDC_D13/VOP_BT1120_CLK/GMAC1_TXCLK_M0/I2S3_SDI_M0/SDMMC2_CLK_M1/GPIO3_A6_d	GRF_GPIO3A_IOMUX_H[11:8]=4'h5
sdmmc2_ccmd	I/O	LCDC_D12/VOP_BT1120_D4/GMAC1_RXD3_M0/I2S3_SDO_M0/SDMMC2_CMD_M1/GPIO3_A5_d	GRF_GPIO3A_IOMUX_H[7:4]=4'h5
sdmmc2_cdata0	I/O	LCDC_D8/VOP_BT1120_D0/SPI1_CS0_M1/PCIE30X1_PERSTn_M1/SDMMC2_D0_M1/GPIO3_A1_d	GRF_GPIO3A_IOMUX_L[7:4]=4'h5
sdmmc2_cdata1	I/O	LCDC_D9/VOP_BT1120_D1/GMAC1_TXD2_M0/I2S3_MCLK_M0/SDMMC2_D1_M1/GPIO3_A2_d	GRF_GPIO3A_IOMUX_L[11:8]=4'h5
sdmmc2_cdata2	I/O	LCDC_D10/VOP_BT1120_D2/GMAC1_TXD3_M0/I2S3_SCLK_M0/SDMMC2_D2_M1/GPIO3_A3_d	GRF_GPIO3A_IOMUX_L[15:12]=4'h5
sdmmc2_cdata3	I/O	LCDC_D11/VOP_BT1120_D3/GMAC1_RXD2_M0/I2S3_LRCK_M0/SDMMC2_D3_M1/GPIO3_A4_d	GRF_GPIO3A_IOMUX_H[3:0]=4'h5
sdmmc2_cdetn	I	LCDC_D14/VOP_BT1120_D5/GMAC1_RXCLK_M0/SDMMC2_DET_M1/GPIO3_A7_d	GRF_GPIO3A_IOMUX_H[15:12] =4'h4
sdmmc2_pwr	O	LCDC_D15/VOP_BT1120_D6/ETH1_REFCLKO_25M_M0/SDMMC2_PWREN_M1/GPIO3_B0_d	GRF_GPIO3B_IOMUX_L[3:0]=4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

6.6 Application Notes

6.6.1 Card-Detect and Write-Protect Mechanism

Following figure illustrates how the SD/MMC card detection and write-protect signals are connected. Most of the SD/MMC sockets have card-detect pins. When no card is present, card_detect_n is 1 due to the pull-up. When the card is inserted, the card-detect pin is shorted to ground, which makes card_detect_n go to 0. Similarly in SD cards, when the write-protect switch is toward the left, it shorts the write_protect port to ground.

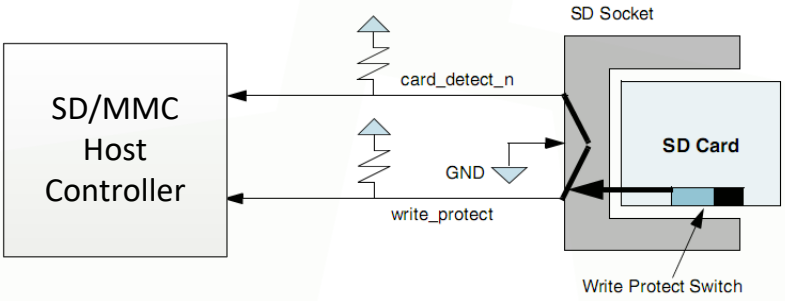


Fig. 6-10 SD/MMC Card-Detect and Write-Protect

6.6.2 SD/MMC Termination Requirement

Following Figure illustrates the SD/MMC termination requirements, which is required to pull up ccmd and cdata lines on the device bus. The recommended specification for pull-up on the ccmd line (Rcmd) is 4.7K - 100K for MMC, and 10K - 100K for an SD. The recommended pull-up on the cdata line (Rdat) is 50K - 100K.

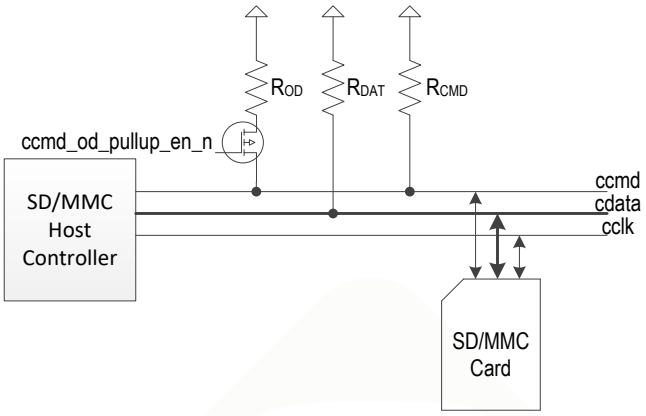


Fig. 6-11 SD/MMC Card Termination

Rcmd and Rod Calculation

The SD/MMC card enumeration happens at a very low frequency – 100-400KHz. Since the MMC bus is a shared bus between multiple cards, during enumeration open-drive mode is used to avoid bus conflict. Cards that drive 0 win over cards that drive "z". The pull-up in the command line pulls the bus to 1 when all cards drive "z". During normal data transfer, the host chooses only one card and the card driver switches to push-pull mode.

For example, if enumeration is done at 400KHz and the total bus capacitance is 200 pf, the pull-up needed during enumeration is:

2.2 RC = rise-time = 1/400KHz

R = 1/(2.2 * C * 100KHz)

= 1/(2.2 x 200 x 10**-12 x 400 x 10**3)

= 1/(17.6 x 10**-5)

= 5.68K

The ROD and RCMD should be adjusted in such a way that the effective pull-up is at the maximum 5.68K during enumeration. If there are only a few cards in the bus, a fixed RCMD resister is sufficient and there is no need for an additional ROD pull-up during enumeration. You should also ensure the effective pull-up will not violate the Iol rating of the drivers.

In SD mode, since each card has a separate bus, the capacitance is less, typically in the order of 20-30pf (host capacitance + card capacitance + trace + socket capacitance). For example, if enumeration is done at 400KHz and the total bus capacitance is 20pf, the pull-up needed during enumeration is:

2.2 RC = rise-time = 1/400KHz

R = 1/(2.2 * C * 100KHz)

= 1/(2.2 x 20 x 10**-12 x 400 x 10**3)

= 1/(1.76 x 10**-5)

= 56.8K

Therefore, a fixed 56.8K permanent Rcmd is sufficient in SD mode to enumerate the cards. The driver of the SD/MMC on the "command" port needs to be only a push-pull driver. During enumeration, the SD/MMC emulates an open-drain driver by driving only a 0 or a"z" by controlling the ccmd_out and ccmd_out_en signals.

6.6.3 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

If the card is enumerated in SDR50, or DDR50 mode, then the application must program the use_hold_reg bit[29] in the SDMMC_CMD register to 1'b0 (phase shift of cclk_in_drv = 0) or 1'b1 (phase shift of cclk_in_drv>0). If the card is enumerated in SDR12 or SDR25 mode, the application must program the use_hold_reg bit[29] in the SDMMC_CMD register to 1'b1. This programming should be done for all data transfer commands and non-data commands that are sent to the card. When the use_hold_reg bit is programmed to 1'b0, the Host Controller bypasses the Hold Registers in the transmit path. The value of this bit should not be changed when a Command or Data Transfer is in progress. For more details on using

use_hold_reg and the implementation requirements for meeting the Card input hold time, refer to "Recommended Usage" in following table.

Table 6-12 Recommended Usage of use_hold_reg

No.	Speed Mode	use_hold_reg	cclk_in (MHz)	clk_in_drv (MHz)	clk_divider	Phase shift
1	SDR104	1'b0	200	200	0	0
2	SDR104	1'b1	200	200	0	Tunable> 0
3	SDR50	1'b0	100	100	0	0
4	SDR50	1'b1	100	100	0	Tunable> 0
5	DDR50 (8bit)	1'b0	100	100	1	0
6	DDR50 (8bit)	1'b1	100	100	1	Tunable> 0
7	DDR50 (4bit)	1'b0	50	50	0	0
8	DDR50 (4bit)	1'b1	50	50	0	Tunable> 0
9	SDR25	1'b1	50	50	0	Tunable> 0
10	SDR12	1'b1	50	50	1	Tunable> 0

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable all clocks. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source registers, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed. If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting

the FIFO reset, you should wait until this bit is cleared.
One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO. It is recommended that you not change the FIFO threshold register in the middle of data transfers.

6.6.4 Programming Sequence

6.6.4.1 Initialization

Following figure illustrates the initialization flow.

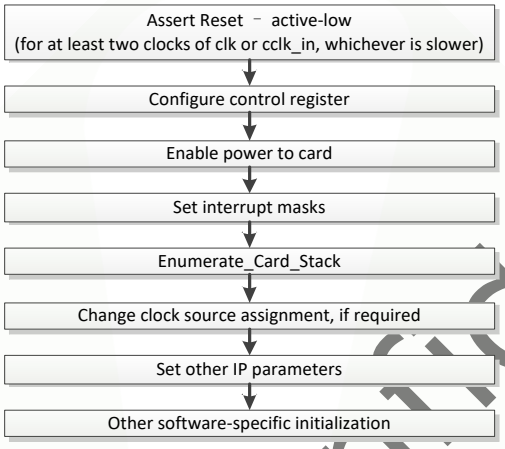


Fig. 6-12 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
- (10*((TAAC*Fop)+(100*NSAC))
- Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.
- FIFO threshold value in bytes in the SDMMC_FIFOTH register.

6.6.4.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

6.6.4.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:
1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
4) Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

6.6.4.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.

For basic commands or non-data commands, follow these steps:
1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 6-13 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		

Parameter	Value	Description
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:
- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

6.6.4.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively.

For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

6.6.4.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 6-14 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by

sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.
- When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

6.6.4.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 6-15 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.
- When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

6.6.4.8 Stream Read

A stream read is like the block read mentioned in "Single-Block or Multiple-Block Read", except for the following bits in the Command register:

transfer_mode = 1; //Stream transfer
cmd_index = CMD20;

A stream transfer is allowed for only a single-bit bus width.

6.6.4.9 Stream Write

A stream write is exactly like the block write mentioned in "Single-Block or Multiple-Block Write", except for the following bits in the Command register:

transfer_mode = 1;//Stream transfer
cmd_index = CMD11;

In a stream transfer, if the byte count is 0, then the software must send the STOP command. If the byte count is not 0, then when a given number of bytes completes a transfer, the Host Controller sends the STOP command. Completion of this AUTO_STOP command is reflected by the Auto_command_done interrupt. A response to an AUTO_STOP is stored in the SDMMC_RESP1 register@0x34.
A stream transfer is allowed for only a single-bit bus width.

6.6.4.10 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.

- Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

6.6.4.11 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.
3) Clear the read_wait bit in the SDMMC_CTRL register.

6.6.4.12 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the

SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

6.6.4.13 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

6.6.4.14 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill

data in the FIFO in order to start transferring data to the card.

- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

6.6.5 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.

However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.

SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.

If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.

Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.

To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

6.6.5.1 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

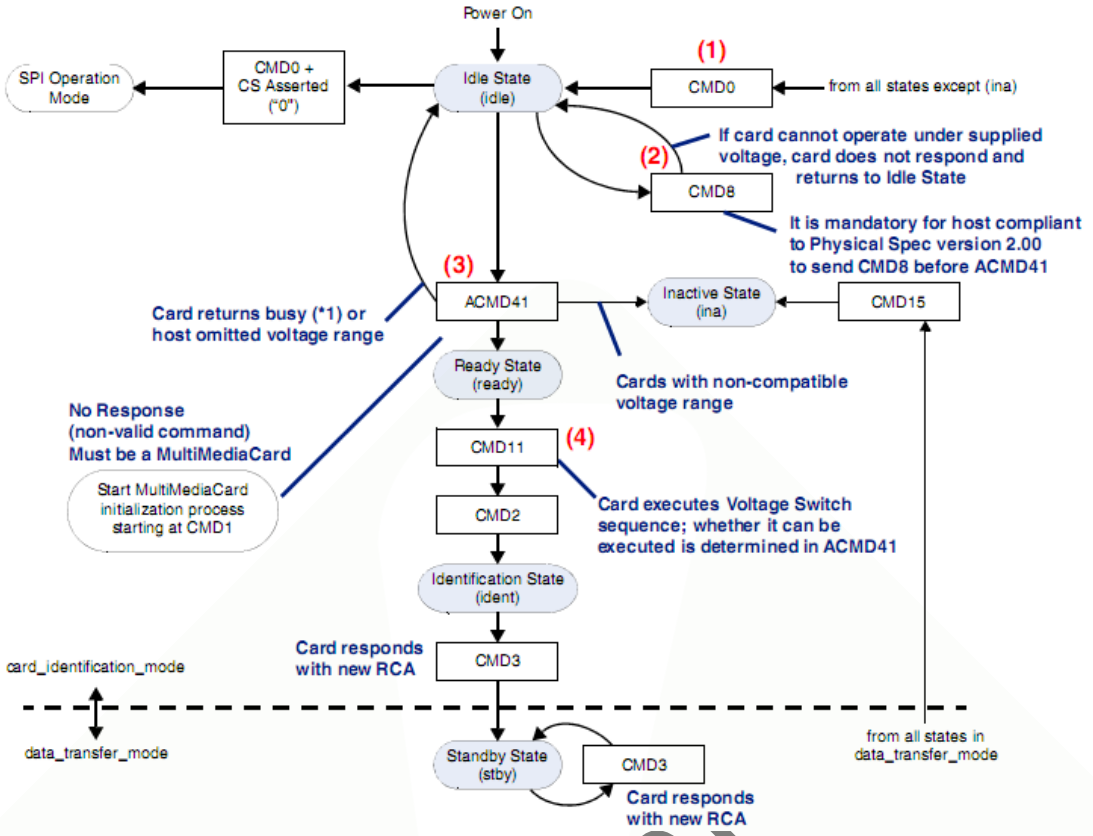


Fig. 6-13 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

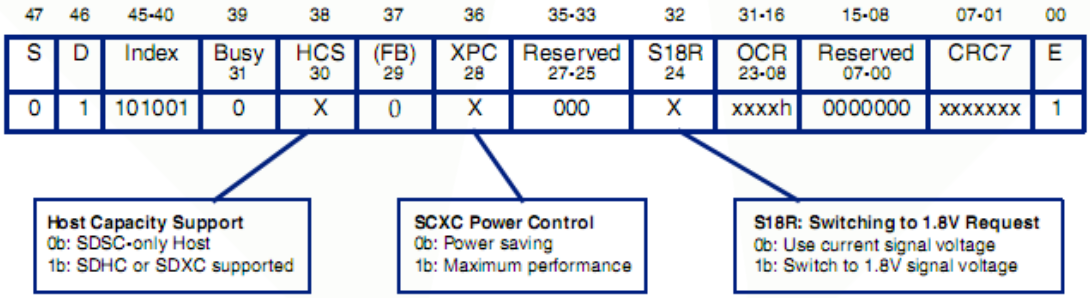


Fig. 6-14 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

47	46	45-40	39	38	37	36-33	32	31-16	15-08	07-01	00
S	D	Index	Busy 31	CCS 30	Rsvd 29	Reserved 28-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E
0	0	111111	X	X	0	0000	X	xxxxh	0000000	1111111	1

Busy Status
0b: On Initialization
1b: Initialization complete

Card Capacity Status
0b: SDSC
1b: SCHC or SCXC

S18R: Switching to 1.8V Accepted
0b: Continues current voltage signalling
1b: Ready for switching signal voltage

Fig. 6-15 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

4) If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

6.6.5.2Voltage Switch Normal Scenario

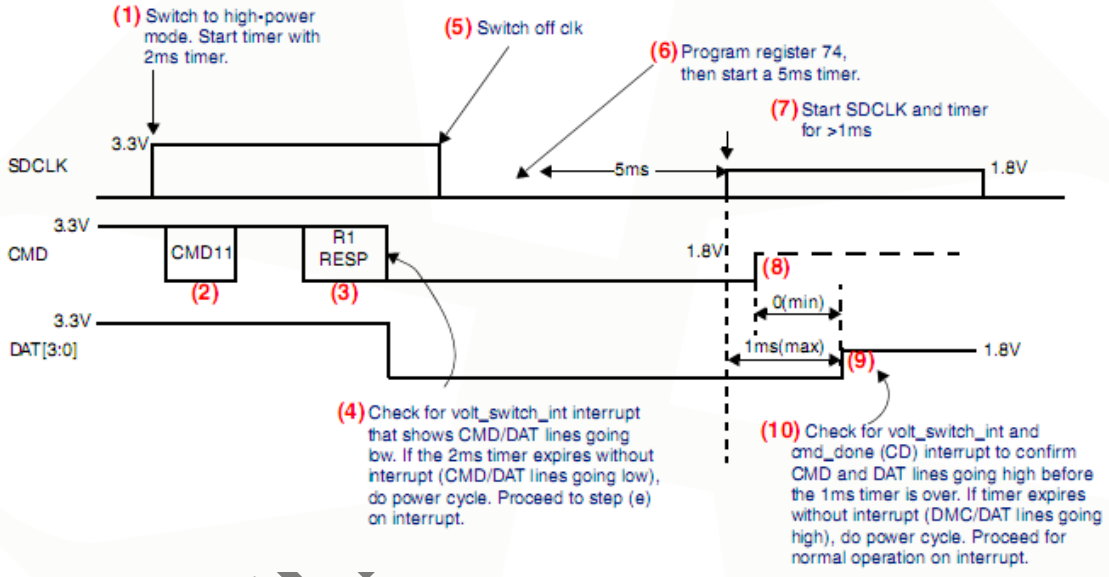


Fig. 6-16 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below: Total cycles required for CMD11 = 48 cycles
Total cycles required for RESP R1 = 48 cycles
Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
Total = 48+48 + 60 = 160
Minimum frequency during enumeration is 100 KHz; that is, 10us
Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be

masked during the voltage switch sequence.

If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle. Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

6.6.5.3 Voltage Switch Error Scenario

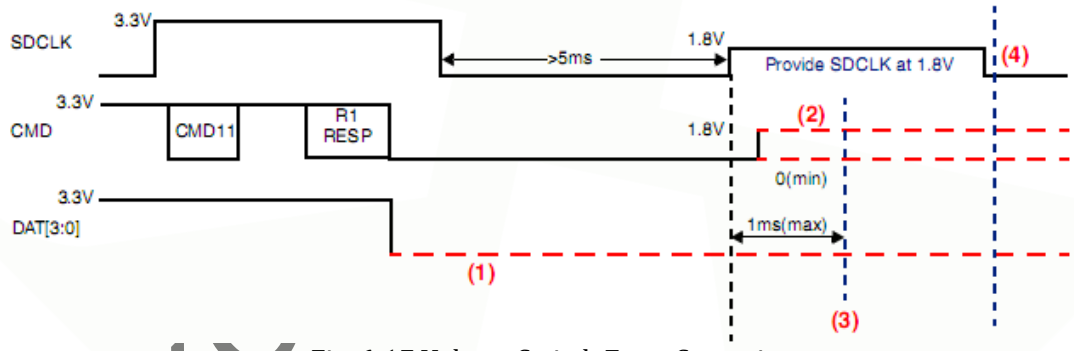


Fig. 6-17 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
  - If voltage switching is properly done, CMD and DAT line goes high.
  - If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

6.6.6 DDR Operation

6.6.6.14-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

2) To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

6.6.6.28-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The SDMMC_CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHSREG[16] register (ddr_reg bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.
4) Depending on the card number, the SDMMC_CTYPE [16] bits should be set in order to make the host work in the 8-bit mode.

6.6.6.3eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

6.6.6.4Reset Command/Moving From DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.
3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

6.6.7 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:

1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.
3) Set the following resets:
- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 µs or cclk_in period, whichever is greater
6) After a minimum of 1 µs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200 µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

6.6.8 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

6.6.8.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

6.6.8.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 6-16 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	greater than or equal to 1
4	greater than or equal to 4
8	greater than or equal to 8
16	greater than or equal to 16
32	greater than or equal to 32
64	greater than or equal to 64
128	greater than or equal to 128
256	greater than or equal to 256

6.6.9 Variable Delay Usage

The delay time of every element is in the range of 32ps~70ps, varying with different voltage and temperature.

The control signals for variable delay element usage are shown as follows.

6.6.9.1 SDMMC0 Variable Delay Usage

Table 6-17 Configuration for SDMMC0 Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC_CON0[0]	0	Soft initial state for phase shift.

Signal Name	Source	Default	Description
drv_degree[1:0]	CRU_SDMMC_CON0[2:1]	2	Phase shift for cclk_in_drv. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree
drv_delaynum[7:0]	CRU_SDMMC_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDMMC_CON0[11]	0	cclk_in_drv source selection: 1'b0: use clock after phase_shift 1;b1: use clock after phase_shift and delay line
sample_degree[1:0]	CRU_SDMMC_CON1[2:1]	0	Phase shift for cclk_in_sample. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree
sample_delaynum[7:0]	CRU_SDMMC_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDMMC_CON1[11]	0	cclk_in_sample source selection: 1'b0: use clock after phase_shift 1'b1: use clock after phase_shift and delay line

6.6.9.2SDMMC1 Variable Delay Usage

Table 6-18 Configuration for SDMMC1 Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC1_CON0[0]	0	Soft initial state for phase shift.
drv_degree[1:0]	CRU_SDMMC1_CON0[2:1]	2	Phase shift for cclk_in_drv. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree
drv_delaynum[7:0]	CRU_SDMMC1_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDMMC1_CON0[11]	0	cclk_in_drv source selection: 1'b0: use clock after phase_shift 1;b1: use clock after phase_shift and delay line
sample_degree[1:0]	CRU_SDMMC1_CON1[2:1]	0	Phase shift for cclk_in_sample. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree
sample_delaynum[7:0]	CRU_SDMMC1_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDMMC1_CON1[11]	0	cclk_in_sample source selection: 1'b0: use clock after phase_shift 1'b1: use clock after phase_shift and delay line

6.6.9.3SDMMC2 Variable Delay Usage

Table 6-19 Configuration for SDMMC2 Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC2_CON0[0]	0	Soft initial state for phase shift.
drv_degree[1:0]	CRU_SDMMC2_CON0[2:1]	2	Phase shift for cclk_in_drv. 2'h0: 0-degree 2'h1: 90-degree

Signal Name	Source	Default	Description
			2'h2: 180-degree 2'h3: 270-degree
drv_delaynum[7:0]	CRU_SDMMC2_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDMMC2_CON0[11]	0	cclk_in_drv source selection: 1'b0: use clock after phase_shift 1;b1: use clock after phase_shift and delay line
sample_degree[1:0]	CRU_SDMMC2_CON1[2:1]	0	Phase shift for cclk_in_sample. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree
sample_delaynum[7:0]	CRU_SDMMC2_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDMMC2_CON1[11]	0	cclk_in_sample source selection: 1'b0: use clock after phase_shift 1'b1: use clock after phase_shift and delay line

The following outlines the steps for clock generation sequence:

1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

6.6.10 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.

Command for tuning is different for different cards.

- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.

7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

6.6.11 Card Detection Method

There are many methods for SDMMC0/SDMMC1/SDMMC2 device detection.

- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port. 0 represents presence of card. This method is available only for SDMMC0/SDMMC1/SDMMC2.
- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals. This method is available only for SDMMC0/SDMMC1/SDMMC2.

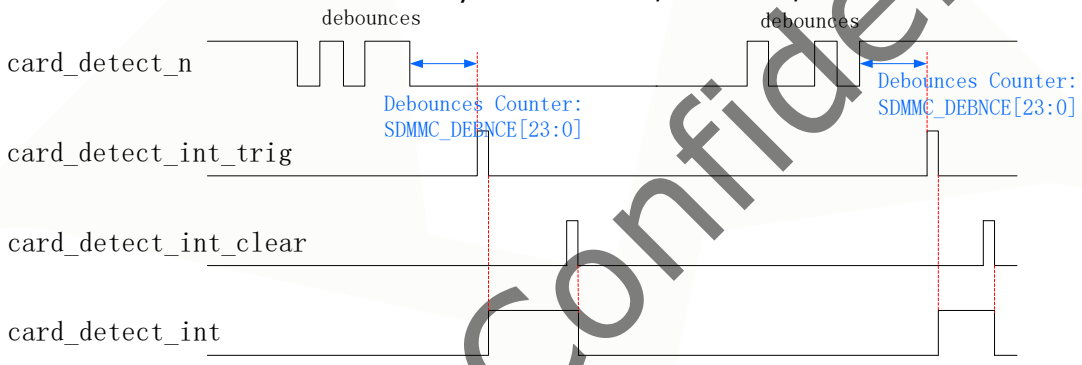


Fig. 6-18 Card Detection Method 2

- Method3: Using card detection unit in GRF, outputting detect_dual_edge_int connecting to IRQ[184] for SDMMC0/IRQ[185] for SDMMC1/IRQ[186] for SDMMC2. Similar to Method2, except that the debounce time is configurable by PMUGRF_SDMMC_DET; and the insertion/removal detection interrupt can be enabled or cleared respectively.

The detailed register information is:

Table 6-20 Register for SDMMC0 Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SD_DETECT_CON[0]	0	sdmmc detect_n signal rise edge interrupt enable. 1: enable 0: disable
sd_detect_fall_edge_detect_en	PMUGRF_SD_DETECT_CON[1]	0	sd_detect_falling_edge enable 0: disable 1: enable
sd_detect_rising_edge_dectect_status	PMUGRF_SD_DETECT_STATUS[0]	0	sd_detect_rising_edge status 0: disable 1: enable
sd_detect_fall_edge_detect_status	PMUGRF_SD_DETECT_STATUS[1]	0	sd_detect_falling_edge status 0: disable 1: enable
sd_detect_rising_edge_dectect_clr	PMUGRF_SD_DETECT_CLR[0]	0	sd_detect_rising_edge clear 0: disable 1: enable
sd_detect_fall_edge_detect_clr	PMUGRF_SD_DETECT_CLR[1]	0	sd_detect_falling_edge clear 0: disable 1: enable

Table 6-21 Register for SDMMC1 Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SD_DETECT_CON[2]	0	sdmmc detect_n signal rise edge interrupt enable. 1: enable 0: disable
sd_detect_fall_edge_detect_en	PMUGRF_SD_DETECT_CON[3]	0	sd_detect_falling_edge enable 0: disable 1: enable
sd_detect_rising_edge_dectect_status	PMUGRF_SD_DETECT_STATUS[2]	0	sd_detect_rising_edge status 0: disable 1: enable
sd_detect_fall_edge_detect_status	PMUGRF_SD_DETECT_STATUS[3]	0	sd_detect_falling_edge status 0: disable 1: enable
sd_detect_rising_edge_dectect_clr	PMUGRF_SD_DETECT_CLR[2]	0	sd_detect_rising_edge clear 0: disable 1: enable
sd_detect_fall_edge_detect_clr	PMUGRF_SD_DETECT_CLR[3]	0	sd_detect_falling_edge clear 0: disable 1: enable

Table 6-22 Register for SDMMC2 Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SD_DETECT_CON[4]	0	sdmmc detect_n signal rise edge interrupt enable. 1: enable 0: disable
sd_detect_fall_edge_detect_en	PMUGRF_SD_DETECT_CON[5]	0	sd_detect_falling_edge enable 0: disable 1: enable
sd_detect_rising_edge_dectect_status	PMUGRF_SD_DETECT_STATUS[4]	0	sd_detect_rising_edge status 0: disable 1: enable
sd_detect_fall_edge_detect_status	PMUGRF_SD_DETECT_STATUS[5]	0	sd_detect_falling_edge status 0: disable 1: enable
sd_detect_rising_edge_dectect_clr	PMUGRF_SD_DETECT_CLR[4]	0	sd_detect_rising_edge clear 0: disable 1: enable
sd_detect_fall_edge_detect_clr	PMUGRF_SD_DETECT_CLR[5]	0	sd_detect_falling_edge clear 0: disable 1: enable

- Method4: Using filtered card_detect_n with the debounce time PMUGRF_SDMMC_DET for interrupt source, connecting to IRQ [187] directly. This method is available only for SDMMC0.

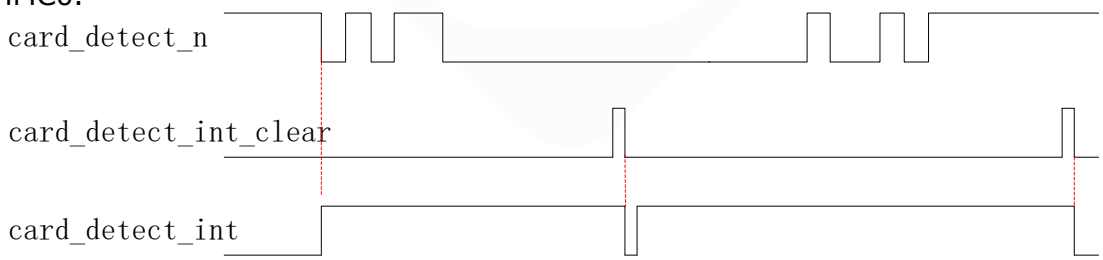


Fig. 6-19 Card Detection Method 4

6.6.12 SDMMC IOMUX With JTAG

The IO for sdmmc0_cdata2/sdmmc0_cdata3 is shared with jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If SGRF_SOC_CON2[4] is equal to 1 and SD/MMC card is not detected within detection time(in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

Chapter 7 eMMC Host Controller

7.1 Overview

The eMMC Host Controller is highly configurable and programmable, and provides high performance eMMC Host Controller with AXI as the bus interface for data transfer (master interface) and AHB as its slave interface.

It supports following features:

- Supports SD-HCI Host version 4 mode or less
  - Supports same SD-HCI register set for eMMC transfers
  - Supports Command Queuing Engine (CQE) and compliant with eMMC CQ HCI
  - Supports the following data transfer types: CPU, SDMA, AMDM2, ADMA3
- Supports eMMC protocols including eMMC 5.1
  - Supports Auto-tuning
  - Supports 4-bit/8-bit interface
  - Supports legacy, High Speed SDR, High Speed DDR, HS200, and HS400 speed modes
  - Supports boot operation and alternative boot operation
- AHB Slave Interface: Supports 32-bit data width and address width
- AXI Master Interface: Supports 32-bit address width and 64-bit data width
- Clock adjustment: support phase auto adjustment for transmit clock, sample clock and data strobe.

7.2 Block Diagram

The Host Controller consists of the following main functional blocks.

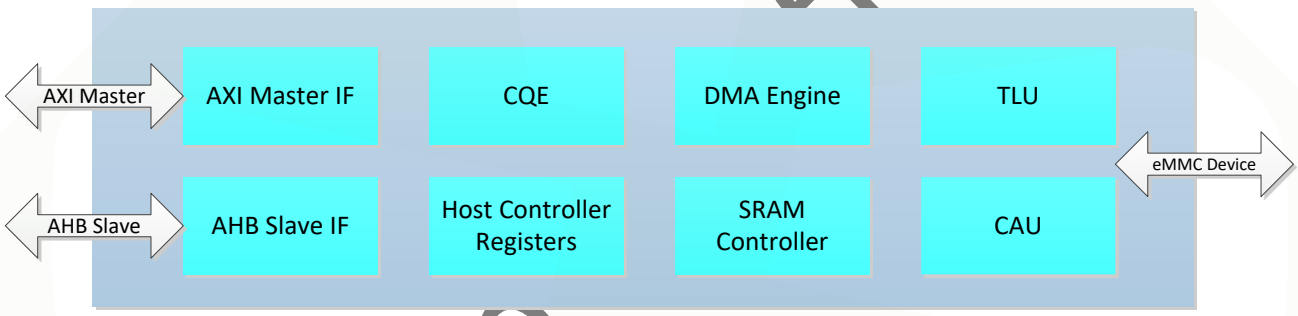


Fig. 7-1 EMMC Host Control Block Diagram

7.3 Function Description

7.3.1 The AXI Master Bus Interface Unit

This Master Bus Interface Unit implements the logic to transfer data on the AMBA Extensible Interface Bus (AXI) bus. The AXI interface transfers data to and from the system memory through the AXI master bus interface, respectively.

7.3.2 The AHB Slave Bus Interface Unit

The AHB slave bus interface module implements the logic to primarily access the host registers by using an external AMBA high-performance (AHB) bus.

7.3.3 Host Controller Registers

The host controller register unit comprises of the standard SD host controller registers as specified in the SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20a. It also includes Command Queuing registers compliance to JEDEC eMMC 5.1 HCI specification.

7.3.4 DMA Engine

The DMA Engine unit handles data transfer between the host and system memory.

- Support SDMA/ADMA2/ADMA3 modes
- Fetch the descriptor and data
- The same DMA engine is used to interleave data transfer and descriptor fetch. This enables new task descriptor fetches (for CMD44 and CMD45) while DMA is moving data during task execution (for CMD46 and CMD47).
- The AXI transaction ID 0 is used for moving data and AXI transaction ID 1 is used to fetch task descriptors.

- Pre-fetch data for back-to-back eMMC write commands
- Write back the received data packets to the system memory

7.3.5 SRAM Controller

The SRAM controller interfaces the packet buffer of the host and the transaction controller units. The SRAM is a single clock single-port RAM synchronous to the core base clock. The width is 64-bit, the depth is 288-location.

7.3.6 Command Queuing Engine

This module implements command queuing and includes the following:

- Task scheduler with the ability to prioritize execution of tasks
- Control logic for descriptor fetch
- Control and sequence task submission and execution
- Status polling
- Timers and counter dedicated for CQE operation
- Interrupt coalescing logic

7.3.7 Transfer Level Unit

The TLU manages the command/response and data flow for communication with memory cards.

7.3.8 Clock Adjustment Unit

The clock adjustment unit (CAU) will detect the clock period and get the delay precision, adjust the clock phase base on the dedicate delay element. Also, you can program the register to set the delay precision. The flowing clocks supports adjustment: transmit clock, sample clock and data strobe.

7.4 Register Description

7.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EMMC_SDMASA	0x0000	W	0x00000000	SDMA System Address Register
EMMC_BLOCKSIZE	0x0004	HW	0x00000000	Block Size Register
EMMC_BLOCKCOUNT	0x0006	HW	0x00000000	16-bit Block Count Register
EMMC_ARGUMENT	0x0008	W	0x00000000	Argument Register
EMMC_XFER_MODE	0x000C	HW	0x00000000	Transfer Mode Register
EMMC_CMD	0x000E	HW	0x00000000	Command Register
EMMC_RESP01	0x0010	W	0x00000000	Response Register 0/1
EMMC_RESP23	0x0014	W	0x00000000	Response Register 2/3
EMMC_RESP45	0x0018	W	0x00000000	Response Register 4/5
EMMC_RESP67	0x001C	W	0x00000000	Response Register 6/7
EMMC_BUF_DATA	0x0020	W	0x00000000	Buffer Data Port Register
EMMC_PSTATE	0x0024	W	0x19FF0000	Present State Register
EMMC_HOST_CTRL1	0x0028	B	0x00000000	Host Control 1 Register
EMMC_PWR_CTRL	0x0029	B	0x00000000	Power Control Register
EMMC_BGAP_CTRL	0x002A	B	0x00000000	Block Gap Control Register
EMMC_CLK_CTRL	0x002C	HW	0x00000000	Clock Control Register
EMMC_TOUT_CTRL	0x002E	B	0x00000000	Timeout Control Register
EMMC_SW_RST	0x002F	B	0x00000000	Software Reset Register
EMMC_NORMAL_INT_STAT	0x0030	HW	0x00000000	Normal Interrupt Status Register
EMMC_ERROR_INT_STAT	0x0032	HW	0x00000000	Error Interrupt Status Register
EMMC_NORMAL_INT_STAT_EN	0x0034	HW	0x00000000	Normal Interrupt Status Enable Register
EMMC_ERROR_INT_STAT_EN	0x0036	HW	0x00000000	Error Interrupt Status Enable Register
EMMC_NORMAL_INT_SIGNAL_EN	0x0038	HW	0x00000000	Normal Interrupt Signal Enable Register
EMMC_ERROR_INT_SIGNAL_EN	0x003A	HW	0x00000000	Error Interrupt Signal Enable Register

Name	Offset	Size	Reset Value	Description
EMMC_AUTO_CMD_STAT	0x003C	HW	0x00000000	Auto CMD Error Status Register
EMMC_HOST_CTRL2	0x003E	HW	0x00000000	Host Control 2 Register
EMMC_CAPABILITIES1	0x0040	W	0x40EDC880	Capabilities Register 1
EMMC_CAPABILITIES2	0x0044	W	0x000A207F	Capabilities Register 2
EMMC_FORCE_AUTO_CMD_STAT	0x0050	HW	0x00000000	Force Event Register for Auto CMD Error Status Register
EMMC_FORC_ERR_INT_STAT	0x0052	HW	0x00000000	Force Event Register for Error Interrupt Status Register
EMMC_ADMA_ERR_STAT	0x0054	B	0x00000000	ADMA Error Status Register
EMMC_ADMA_SA	0x0058	W	0x00000000	ADMA System Address Register
EMMC_PRESET_INIT	0x0060	HW	0x00000000	Preset Value for Initialization
EMMC_PRESET_DS	0x0062	HW	0x00000000	Preset Value for Default Speed
EMMC_PRESET_HS	0x0064	HW	0x00000000	Preset Value for High Speed
EMMC_PRESET_SDR12	0x0066	HW	0x00000000	Preset Value for SDR12
EMMC_PRESET_SDR25	0x0068	HW	0x00000000	Preset Value for SDR25
EMMC_PRESET_SDR50	0x006A	HW	0x00000000	Preset Value for SDR50
EMMC_PRESET_SDR104	0x006C	HW	0x00000000	Preset Value for SDR104
EMMC_PRESET_DDR50	0x006E	HW	0x00000000	Preset Value for DDR50
EMMC_ADMA_ID	0x0078	W	0x00000000	ADMA3 Integrated Descriptor Address Register
EMMC_SLOT_INTR_STATUS	0x00FC	HW	0x00000000	Slot Interrupt Status Register
EMMC_HOST_CNTRL_VERS	0x00FE	HW	0x00001005	Host Controller Version
EMMC_CQVER	0x0180	W	0x00000510	Command Queuing Version Register
EMMC_CQCAP	0x0184	W	0x00000000	Command Queuing Capabilities Register
EMMC_CQCFG	0x0188	W	0x00000000	Command Queuing Configuration Register
EMMC_CQCTRL	0x018C	W	0x00000000	Command Queuing Control Register
EMMC_CQIS	0x0190	W	0x00000000	Command Queuing Interrupt Status Register
EMMC_CQISE	0x0194	W	0x00000000	Command Queuing Interrupt Status Enable Register
EMMC_CQISGE	0x0198	W	0x00000000	Command Queuing Interrupt Signal Enable Register
EMMC_CQIC	0x019C	W	0x00000000	Command Queuing Interrupt Coalescing Register
EMMC_CQTDLBA	0x01A0	W	0x00000000	Command Queuing Task Descriptor List Base Address Register
EMMC_CQTDBR	0x01A8	W	0x00000000	Command Queuing DoorBell Register
EMMC_CQTDBN	0x01AC	W	0x00000000	Command Queuing TaskClear Notification Register
EMMC_CQDQS	0x01B0	W	0x00000000	Command Queuing Device Queue Status Register
EMMC_CQDPT	0x01B4	W	0x00000000	Command Queuing Device Pending Tasks Register
EMMC_CQTCLR	0x01B8	W	0x00000000	Command Queuing Task Clear Register

Name	Offset	Size	Reset Value	Description
EMMC_CQSSC1	0x01C0	W	0x00011000	Command Queuing Send Status Configuration 1 Register
EMMC_CQSSC2	0x01C4	W	0x00000000	Command Queuing Send Status Configuration 2 Register
EMMC_CQCRDCT	0x01C8	W	0x00000000	Command Queuing Command Response For Direct Command Register
EMMC_CQRMEM	0x01D0	W	0xFDF9A080	Command Queuing Command Response Mode Rrror Mask Register
EMMC_CQTERRI	0x01D4	W	0x00000000	Command Queuing Task Error Information Register
EMMC_CQCRI	0x01D8	W	0x00000000	Command Queuing Command Response Index Register
EMMC_CQCRA	0x01DC	W	0x00000000	Command Queuing Command Response Argument Register
EMMC_VER_ID	0x0500	W	0x00000000	Host Version ID Register
EMMC_VER_TYPE	0x0504	W	0x00000000	Host Version Type Register
EMMC_HOST_CTRL3	0x0508	B	0x00000001	Host Control 3 Register
EMMC_EMMC_CTRL	0x052C	HW	0x0000000C	EMMC Control Register
EMMC_BOOT_CTRL	0x052E	HW	0x00000000	Boot Control Register
EMMC_AT_CTRL	0x0540	W	0x00000000	Boot Control Register
EMMC_AT_STAT	0x0544	W	0x00000000	Boot Control Register
EMMC_DLL_CTRL	0x0800	W	0x00000000	DLL Global Control Register
EMMC_DLL_RXCLK	0x0804	W	0x00000000	DLL Control Register For RXCLK
EMMC_DLL_TXCLK	0x0808	W	0x00000000	DLL Control Register For TXCLK
EMMC_DLL_STRBIN	0x080C	W	0x00000000	DLL Control Register For STRBIN
EMMC_DLL_STATUS0	0x0840	W	0x00000000	DLL Status Register 0
EMMC_DLL_STATUS1	0x0844	W	0x00000000	DLL Status Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

7.4.2 Detail Register Description

EMMC_SDMASA

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BLOCKCNT_SDMASA 32-bit Block Count (SDMA System Address). 1. SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. 2. 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. Values: 32'hFFFFFFFF: 1 Block ..... 32'h00000002: 2 Blocks 32'h00000001: 1 Block 32'h00000000: Stop Count Note: a. For Host Version 4 Enable = 0, the Host driver does not program the system address in this register while operating in ADMA mode. The system address must be programmed in the ADMA System Address register. b. For Host Version 4 Enable = 0, the Host driver programs a non-zero 32-bit block count value in this register when Auto CMD23 is enabled for non-DMA and ADMA modes. Auto CMD23 cannot be used with SDMA. c. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register.

EMMC_BLOCKSIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	SDMA_BUF_BDARY SDMA Buffer Boundary. These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: 3'h0: 4K bytes SDMA Buffer Boundary 3'h1: 8K bytes SDMA Buffer Boundary 3'h2: 16K bytes SDMA Buffer Boundary 3'h3: 32K bytes SDMA Buffer Boundary 3'h4: 64K bytes SDMA Buffer Boundary 3'h5: 128K bytes SDMA Buffer Boundary 3'h6: 256K bytes SDMA Buffer Boundary 3'h7: 512K bytes SDMA Buffer Boundary

Bit	Attr	Reset Value	Description
11:0	RW	0x000	XFER_BLOCK_SIZE Transfer Block Size. These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Values: 12'h1: 1 byte 12'h2: 2 bytes 12'h3: 3 bytes ..... 12'h1FF: 511 byte 12'h200: 512 bytes ..... 12'h800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer.

EMMC_BLOCKCOUNT

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BLOCK_CNT 16-bit Block Count. If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Values: 16'h0: Stop Count 16'h1: 1 Block 16'h2: 2 Blocks ..... 16'hFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0 before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes.

EMMC_ARGUMENT

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARGUMENT Command Argument. These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format.

EMMC_XFER_MODE

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	RESP_INT_DISABLE Response Interrupt Disable. The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Note: During tuning (when the Execute Tuning bit in the Host Control2 register is set), the Command Complete Interrupt is not generated irrespective of the Response Interrupt Disable setting. Values: 1'b0: Response Interrupt is enabled 1'b1: Response Interrupt is disabled
7	RW	0x0	RESP_ERR_CHK_ENABLE Response Error Check Enable. The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: a. Response error check must not be enabled for any response type other than R1 and R5. b. Response check must not be enabled for the tuning command. Values: 1'b0: Response Error Check is disabled 1'b1: Response Error Check is enabled
6	RW	0x0	RESP_TYPE Response Type R1/R5. This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Values: 1'b0: R1 1'b1: R5
5	RW	0x0	MULTI_BLK_SEL Multi/Single Block Select. This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Values: 1'b0: Single Block 1'b1: Multiple Block

Bit	Attr	Reset Value	Description
4	RW	0x0	DATA_XFER_DIR Data Transfer Direction Select. This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: 1'b0: Write (Host to Card) 1'b1: Read (Card to Host)
3:2	RW	0x0	AUTO_CMD_ENABLE Auto Command Enable. This field determines use of Auto Command functions. Values: 2'h0: Auto Command Disabled 2'h1: Auto CMD12 Enable 2'h2: Auto CMD23 Enable 2'h3: Auto CMD Auto Select
1	RW	0x0	BLOCK_COUNT_ENABLE Block Count Enable. This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. Values: 1'b0: Disable 1'b1: Enable
0	RW	0x0	DMA_ENABLE DMA Enable. This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: 1'b0: No data transfer or Non-DMA data transfer 1'b1: DMA Data transfer

EMMC_CMD

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x00	CMD_INDEX Command Index. These bits are set to the command number that is specified in bits 45-40 of the Command Format.

Bit	Attr	Reset Value	Description
7:6	RW	0x0	CMD_TYPE Command Type. These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: 2'h0: Normal 2'h1: Suspend 2'h2: Resume 2'h3: Abort
5	RW	0x0	DATA_PRESENT_SEL Data Present Select. This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: a. Command using the CMD line b. Command with no data transfer but using busy signal on the DAT[0] line c. Resume Command Values: 1'b0: No Data Present 1'b1: Data Present
4	RW	0x0	CMD_IDX_CHK_ENABLE Command Index Check Enable. This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: a. Index Check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. b. For the tuning command, this bit must always be set to enable the index check. Values: 1'b0: Disable 1'b1: Enable
3	RW	0x0	CMD_CRC_CHK_ENABLE Command CRC Check Enable. This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: a. CRC Check enable must be set to 0 for the command with no response, R3 response, and R4 response. b. For the tuning command, this bit must always be set to 1 to enable the CRC check. Values: 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	SUB_CMD_FLAG Sub Command Flag. This bit distinguishes between a main command and a sub command. Values: 1'b0: Main Command 1'b1: Sub Command
1:0	RW	0x0	RESP_TYPE_SELECT Response Type Select. This bit indicates the type of response expected from the card. Values: 2'h0: No Response 2'h1: Response length 136 2'h2: Response length 48 2'h3: Response length 48, check Busy after response.

EMMC_RESP01

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP01 Command Response. These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67 register.

EMMC_RESP23

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP23 Command Response. These bits reflect 71-40 bits of the SD/eMMC Response Field.

EMMC_RESP45

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	RESP45 Command Response. These bits reflect 103-72 bits of the Response Field.

EMMC_RESP67

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP67 Command Response These bits reflect bits 135-104 of SD/EMMC Response Field. For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field).

EMMC_BUF_DATA

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BUF_DATA Buffer Data. These bits enable access to the Host Controller packet buffer.

EMMC_PSTATE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x1	SUB_CMD_STAT Sub Command Status. This bit is used to distinguish between a main command and a sub command status. Values: 1'b0: Main Command Status 1'b1: Sub Command Status
27	RO	0x1	CMD_ISSUE_ERR Command Not Issued by Error. This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error. Values: 1'b0: No error for issuing a command 1'b1: Command cannot be issued
26:25	RO	0x0	reserved
24	RO	0x1	CMD_LINE_LVL Command-Line Signal Level. This bit is used to check the CMD line level to recover from errors and for debugging. These bits reflect the value of the sd_cmd_in signal.
23:20	RO	0xf	DAT_3_0 DAT[3:0] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (lower nibble) signal.
19	RO	0x1	WR_PROTECT_SW_LVL Write Protect Switch Pin Level. This bit is supported only for memory and combo cards. This bit reflects the synchronized value of the card_write_prot signal. Values: 1'b0: Write protected 1'b1: Write enabled
18	RO	0x1	CARD_DETECT_PIN_LEVEL Card Detect Pin Level. This bit reflects the inverse synchronized value of the card_detect_n signal. Values: 1'b0: No card present 1'b1: Card Present
17	RO	0x1	CARD_STABLE Card Stable. This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: 1'b0: Reset or Debouncing 1'b1: No Card or Inserted

Bit	Attr	Reset Value	Description
16	RO	0x1	CARD_INSERTED Card Inserted. This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: 1'b0: Reset, Debouncing, or No card 1'b1: Card Inserted
15:12	RO	0x0	reserved
11	RO	0x0	BUF_RD_ENABLE Buffer Read Enable. This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: 1'b0: Read disable 1'b1: Read enable
10	RO	0x0	BUF_WR_ENABLE Buffer Write Enable. This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: 1'b0: Write disable 1'b1: Write enable
9	RW	0x0	RD_XFER_ACTIVE Read Transfer Active. This bit indicates whether a read transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
8	RO	0x0	WR_XFER_ACTIVE Write Transfer Active. This status indicates whether a write transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
7:4	RO	0x0	DAT_7_4 DAT[7:4] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of the sd_dat_in (upper nibble) signal.
3	RO	0x0	RE_TUNE_REQ Re-Tuning Request. Host Controller does not generate retuning request. The software must maintain the Retuning timer.

Bit	Attr	Reset Value	Description
2	RO	0x0	DAT_LINE_ACTIVE DAT Line Active (SD/eMMC Mode only). This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates wh ther a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD/eMMC bus. Values: 1'b0: DAT Line Inactive 1'b1: DAT Line Active
1	RO	0x0	CMD_INHIBIT_DAT Command Inhibit (DAT). This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. For the UHS-II mode, this bit is irrelevant and always returns 0. Values: 1'b0: Can issue command which used DAT line 1'b1: Cannot issue command which used DAT line
0	RO	0x0	CMD_INHIBIT Command Inhibit (CMD). If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: 1'b0: Host Controller is ready to issue a command 1'b1: Host Controller is not ready to issue a command

EMMC_HOST_CTRL1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
7	RW	0x0	CARD_DETECT_SIG_SEL Card Detect Signal Selection. This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period. Values: 1'b0: SDCD# (card_detect_n signal) is selected (for normal use) 1'b1: Card Detect Test Level is selected (for test purpose)
6	RW	0x0	CARD_DETECT_TEST_LVL Card Detect Test Level. This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: 1'b0: No Card 1'b1: Card Inserted

Bit	Attr	Reset Value	Description
5	RW	0x0	EXT_DAT_XFER Extended Data Transfer Width. This bit controls 8-bit bus width mode of embedded device. Values: 1'b0: Bus Width is selected by the Data Transfer Width 1'b1: 8-bit Bus Width
4:3	RW	0x0	DMA_SEL DMA Select. This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: 32-bit Address ADMA2 is selected 2'h3: Reserved Values: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected
2	RW	0x0	HIGH_SPEED_EN High Speed Enable. In SD/eMMC mode, this bit is used to determine the selection of preset value for High Speed mode. Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Values: 1'b0: Normal Speed mode 1'b1: High Speed mode
1	RW	0x0	DAT_XFER_WIDTH Data Transfer Width. For SD/eMMC mode,this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: 1'b0: 1-bit mode 1'b1: 4-bit mode
0	RO	0x0	reserved

EMMC_PWR_CTRL

Address: Operational Base + offset (0x0029)

Bit	Attr	Reset Value	Description
7:1	RO	0x00	reserved
0	RW	0x0	SD_BUS_PWR If this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the CLK_CTRL_R register. Values: 1'b0: Power off 1'b1: Power on

EMMC_BGAP_CTRL

Address: Operational Base + offset (0x002A)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3	RW	0x0	INT_AT_BGAP Interrupt At Block Gap. This bit is valid only in the 4-bit mode of an SDIO card and is used to select a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer.
2	RW	0x0	RD_WAIT_CTRL Read Wait Control. This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. Values: 1'b0: Disable Read Wait Control 1'b1: Enable Read Wait Control
1	RW	0x0	CONTINUE_REQ Continue Request. This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: 1'b0: No Affect 1'b1: Restart
0	RW	0x0	STOP_BG_REQ Stop At Block Gap Request. This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: 1'b0: Transfer 1'b1: Stop

EMMC_CLK_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	FREQ_SEL SDCLK/RCLK Frequency Select. These bits are used to select the frequency of the SDCLK signal. These bits depend on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, these bits are set by the Host Driver. If Preset Value Enable = 1, these bits are automatically set to a value specified in one of the Preset Value register. The value is reflected on the lower 8-bit of the card_clk_freq_selsignal. 1. 10-bit Divided Clock Mode: 10'h000: Base clock (10MHz - 255 MHz) 10'h001: 1/2 Divided Clock 10'h002: 1/4 Divided Clock ..... 10'h3ff: 1/2046 Divided clock 2. Programmable Clock Mode: 10'h000: Base clock * M 10'h001: Base clock * M /2 10'h002: Base clock * M /3 ..... 10'h3ff: Base clock * M /1024
7:6	RW	0x0	UPPER_FREQ_SEL These bits specify the upper 2 bits of 10-bit SDCLK/RCLK Frequency Select control.
5	RW	0x0	CLK_GEN_SELECT Clock Generator Select. This bit is used to select the clock generator mode in SDCLK/RCLK Frequency Select. If Preset Value Enable = 0, this bit is set by the Host Driver. If Preset Value Enable = 1, this bit is automatically set to a value specified in one of the Preset Value registers. The value is reflected on the card_clk_gen_sel signal. Values: 1'b0: Divided Clock Mode 1'b1: Programmable Clock Mode
4:3	RO	0x0	reserved
2	RW	0x0	SD_CLK_EN SD/eMMC Clock Enable. This bit stops the SDCLK or RCLK when set to 0. The SDCLK/RCLK Frequency Select bit can be changed when this bit is set to 0. Values: 1'b0: Disable providing SDCLK/RCLK 1'b1: Enable providing SDCLK/RCLK
1	RO	0x0	INTERNAL_CLK_STABLE Internal Clock Stable. This bit enables the Host Driver to check the clock stability twice after the Internal Clock Enable bit is set and after the PLL Enable bit is set. This bit reflects the synchronized value of the intclk_stable signal after the Internal Clock Enable bit is set to 1 and also reflects the synchronized value of the card_clk_stable signal after the PLL Enable bit is set to 1. Values: 1'b0: Not Ready 1'b1: Ready

Bit	Attr	Reset Value	Description
0	RW	0x0	INTERNAL_CLK_EN Internal Clock Enable. This bit is set to 0 when the Host Driver is not using the Host Controller. The Host Controller must stop its internal clock to enter a very low power state. However, registers can still be read and written to. The value is reflected on the intclk_en signal. Note: If this bit is not used to control the internal clock (base clock and master clock), it is recommended to set this bit to 1 . Values: 1'b0: Stop 1'b1: Oscillate

EMMC_TOUT_CTRL

Address: Operational Base + offset (0x002E)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	TOUT_CNT Data Timeout Counter Value. This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). Values: 4'h0: TMCLK * 2^13 4'h1: TMCLK * 2^14 ..... 4'he: TMCLK * 2^27 4'hf: Reserved

EMMC_SW_RST

Address: Operational Base + offset (0x002F)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	SW_RST_DAT Software Reset For DAT line. This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: a. Buffer Data Port register: Buffer is cleared and initialized. b. Present state register: Buffer Read Enable Buffer Write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) c. Block Gap Control register: Continue Request Stop At Block Gap Request d. Normal Interrupt status register: Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Values: 1'b0: Work 1'b1: Reset
1	RW	0x0	SW_RST_CMD Software Reset For CMD line. This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: a. Present State register - Command Inhibit (CMD) bit b. Normal Interrupt Status register - Command Complete bit c. Error Interrupt Status - Response error statuses related to Command Inhibit (CMD) bit Values: 1'b0: Work 1'b1: Reset
0	RW	0x0	SW_RST_ALL Software Reset For All. This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: 1'b0: Work 1'b1: Reset

EMMC_NORMAL_INT_STAT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
15	RO	0x0	ERROR_INT_STAT Error Interrupt. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: 1'b0: No Error 1'b1: Error
14	W1C	0x0	CQE_EVENT Command Queuing Event. This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. Values: 1'b0: No Event 1'b1: Command Queuing Event is detected
13	RO	0x0	FX_EVENT FX Event. This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: 1'b0: No Event 1'b1: FX Event is detected
12	RO	0x0	RE_TUNE_EVENT Re-tuning Event. This bit is set if the Re-Tuning Request changes from 0 to 1. Re-Tuning request is not supported.
11:9	RO	0x0	reserved
8	RO	0x0	CARD_INTERRUPT Card Interrupt. This bit reflects the synchronized value of DAT[1] Interrupt Input for SD Mode. Values: 1'b0: No Card Interrupt 1'b1: Generate Card Interrupt
7	W1C	0x0	CARD_REMOVAL Card Removal. This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Removed
6	W1C	0x0	CARD_INSERTION Card Insertion. This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Inserted
5	W1C	0x0	BUF_RD_READY Buffer Read Ready. This bit is set if the Buffer Read Enable changes from 0 to 1. Values: 1'b0: Not ready to read buffer 1'b1: Ready to read buffer

Bit	Attr	Reset Value	Description
4	W1C	0x0	BUF_WR_READY Buffer Write Ready. This bit is set if the Buffer Write Enable changes from 0 to 1. Values: 1'b0: Not ready to write buffer 1'b1: Ready to write buffer
3	W1C	0x0	DMA_INTERRUPT DMA Interrupt. This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: 1'b0: No DMA Interrupt 1'b1: DMA Interrupt is generated
2	W1C	0x0	BGAP_EVENT Block Gap Event. This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: 1'b0: No Block Gap Event 1'b1: Transaction stopped at block gap
1	W1C	0x0	XFER_COMPLETE Transfer Complete. This bit is set when a read/write transfer and a command with status busy is completed. Values: 1'b0: Not complete 1'b1: Command execution is completed
0	W1C	0x0	CMD_COMPLETE Command Complete. In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: 1'b0: No Command Complete 1'b1: Command Complete

EMMC_ERROR_INT_STAT

Address: Operational Base + offset (0x0032)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	W1C	0x0	BOOT_ACK_ERR Boot Acknowledgement Error. This bit is set when there is a timeout for boot acknowledgement or when detecting boot ack status having a value other than 010. This is applicable only when boot acknowledgement is expected in eMMC mode. Values: 1'b0: No Error 1'b1: Error

Bit	Attr	Reset Value	Description
11	W1C	0x0	RESP_ERR Response Error, Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1. Values: 1'b0: No Error 1'b1: Error
10	W1C	0x0	TUNING_ERR Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select is set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver must discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. Values: 1'b0: No Error 1'b1: Error
9	W1C	0x0	ADMA_ERR ADMA Error. This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: a. Error response received from System bus (Master I/F) b, ADMA3,ADMA2 Descriptors invalid c. CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: 1'b0: No Error 1'b1: Error

Bit	Attr	Reset Value	Description
8	W1C	0x0	AUTO_CMD_ERR Auto CMD Error. This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: 1'b0: No Error 1'b0: Error
7	RO	0x0	reserved
6	W1C	0x0	DATA_END_BIT_ERR Data End Bit Error. This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: 1'b0: No Error 1'b1: Error
5	W1C	0x0	DATA_CRC_ERR Data CRC Error. This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: 1'b0: No Error 1'b1: Error
4	W1C	0x0	DATA_TOUT_ERR Data Timeout Error. This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: a. Busy timeout for R1b, R5b type b. Busy timeout after Write CRC status c. Write CRC Status timeout d. Read Data timeout Values: 1'b0: No Error 1'b1: Time out
3	W1C	0x0	CMD_IDX_ERR Command Index Error. This bit is set if a Command Index error occurs in the command respons in SD/eMMC mode. Values: 1'b0: No Error 1'b1: Error
2	W1C	0x0	CMD_END_BIT_ERR Command End Bit Error. This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: 1'b0: No Error 1'b1: End Bit Error generated

Bit	Attr	Reset Value	Description
1	W1C	0x0	CMD_CRC_ERR Command CRC Error. Command CRC Error is generated in SD/eMMC mode for following two cases. a. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. b. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: 1'b0: No Error 1'b1: CRC Error generated
0	W1C	0x0	CMD_TOUT_ERR Command Timeout Error. In SD/eMMC Mode,this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: 1'b0: No Error 1'b1: Time out

EMMC_NORMAL_INT_STAT_EN

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_STAT_EN CQE Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_STAT_EN Card Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_STAT_EN Card Removal Status Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_STAT_EN Card Insertion Status Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
5	RW	0x0	BUF_RD_READY_STAT_EN Buffer Read Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_STAT_EN Buffer Write Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_STAT_EN DMA Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_STAT_EN Block Gap Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_STAT_EN Transfer Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_STAT_EN Command Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_STAT_EN

Address: Operational Base + offset (0x0036)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_STAT_EN Boot Acknowledgment Error Statusl Enable.. Values: 1'b0: Masked 1'b1: Enabled
11	RW	0x0	RESP_ERR_STAT_EN Response Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_STAT_EN Tuning Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_STAT_EN ADMA Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
8	RW	0x0	AUTO_CMD_ERR_STAT_EN Auto CMD Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_STAT_EN Data End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_STAT_EN Data CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_STAT_EN Data Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_STAT_EN Command Index Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_STAT_EN Command End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_STAT_EN Command CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_STAT_EN Command Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_NORMAL_INT_SIGNAL_EN

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_SIGNAL_EN CQE Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	CARD_INTERRUPT_SIGNAL_EN Card Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_SIGNAL_EN Card Removal Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_SIGNAL_EN Card Insertion Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_SIGNAL_EN Buffer Read Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_SIGNAL_EN Buffer Write Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_SIGNAL_EN DMA Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_SIGNAL_EN Block Gap Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_SIGNAL_EN Transfer Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_SIGNAL_EN Command Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_SIGNAL_EN

Address: Operational Base + offset (0x003A)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_SIGNAL_EN Boot Acknowledgment Error Signal Enable.. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
11	RW	0x0	RESP_ERR_SIGNAL_EN Response Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_SIGNAL_EN Tuning Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_SIGNAL_EN ADMA Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_SIGNAL_EN Auto CMD Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_SIGNAL_EN Data End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_SIGNAL_EN Data CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_SIGNAL_EN Data Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_SIGNAL_EN Command Index Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_SIGNAL_EN Command End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_SIGNAL_EN Command CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	CMD_TOUT_ERR_SIGNAL_EN Command Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_AUTO_CMD_STAT

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RO	0x0	CMD_NOT_ISSUED_AUTO_CMD12 Command Not Issued By Auto CMD12 Error. If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: No Error 1'b1: Not Issued
6	RO	0x0	reserved
5	RO	0x0	AUTO_CMD_RESP_ERR Auto CMD Response Error. This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: 1'b0: No Error 1'b1: Error
4	RO	0x0	AUTO_CMD_IDX_ERR Auto CMD Index Error. This bit is set if the command index error occurs in response to a command. Values: 1'b0: No Error 1'b1: Error
3	RO	0x0	AUTO_CMD_EBIT_ERR Auto CMD End Bit Error. This bit is set when detecting that the end bit of command response is 0. Values: 1'b0: No Error 1'b1: End Bit Error Generated
2	RO	0x0	AUTO_CMD_CRC_ERR Auto CMD CRC Error. This bit is set when detecting a CRC error in the command response. Values: 1'b0: No Error 1'b1: CRC Error Generated

Bit	Attr	Reset Value	Description
1	RO	0x0	AUTO_CMD_TOUT_ERR Auto CMD Timeout Error. This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: 1'b0: No Error 1'b1: Time out
0	RO	0x0	AUTO_CMD12_NOT_EXEC Auto CMD12 Not Executed. If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: Executed 1'b1: Not Executed

EMMC_HOST_CTRL2

Address: Operational Base + offset (0x003E)

Bit	Attr	Reset Value	Description
15	RW	0x0	PRESET_VAL_ENABLE Preset Value Enable. This bit enables automatic selection of SDCLK frequency and Driver strength Preset Value registers. When Preset Value Enable is set, SDCLK frequency generation (Frequency Select and Clock Generator Select) and the driver strength selection are performed by the controller. These values are selected from set of Preset Value registers based on selected speed mode. Values: 1'b0: SDCLK and Driver Strength are controlled by Host Driver 1'b1: Automatic Selection by Preset Value are Enabled
14	RW	0x0	ASYNC_INT_ENABLE Asynchronous Interrupt Enable. This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: 1'b0: Disabled 1'b1: Enabled
13	RW	0x0	ADDRESSING 64-bit Addressing. This bit is effective when Host Version 4 Enable is set to 1. Values: 1'b0: 32 bits addressing 1'b1: 64 bits addressing

Bit	Attr	Reset Value	Description
12	RW	0x0	HOST_VER4_ENABLE Host Version 4 Enable. This bit selects either Version 3.00 compatible mode or Version 4 mode. Functions of following fields are modified for Host Version 4 mode: a. SDMA Address: SDMA uses ADMA System Address (05Fh-058h) instead of SDMA System Address register (003h-000h) b. ADMA2/ADMA3 selection: ADMA3 is selected by DMA select in Host Control 1 register c. 64-bit ADMA Descriptor Size: 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1 d. Selection of 32-bit/64-bit System Addressing: Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register e. 32-bit Block Count: SDMA System Address register (003h-000h) is modified to 32-bit Block Count register. Values: 1'b0: Version 3.00 compatible mode 1'b1: Version 4 mode
11	RW	0x0	CMD23_ENABLE CMD23 Enable. If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 datatransfer. Values: 1'b0: Auto CMD23 is disabled 1'b1: Auto CMD23 is enabled
10	RW	0x0	ADMA2_LEN_MODE ADMA2 Length Mode. This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: 1'b0: 16-bit Data Length Mode 1'b1: 26-bit Data Length Mode
9	RO	0x0	reserved
8	RW	0x0	UHS2_IF_ENABLE This bit should be set to 0 for SD/eMMC Interface.
7	RW	0x0	SAMPLE_CLK_SEL Sampling Clock Select. This bit is used by the Host Controller to select the sampling clock in SD/eMMC mode to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. Values: 1'b0: Fixed clock is used to sample data 1'b1: Tuned clock is used to sample data
6	RW	0x0	EXEC_TUNING Execute Tuning. This bit is set to 1 to start the tuning procedure in UHSI/eMMC speed modes and this bit is automatically cleared when tuning procedure is completed. Values: 1'b0: Not Tuned or Tuning completed 1'b1: Execute Tuning

Bit	Attr	Reset Value	Description
5:4	RO	0x0	reserved
3	RW	0x0	SIGNALING_EN 1.8V Signaling Enable. Values: 1'b0: 3.3V Signalling 1'b1: 1.8V Signalling
2:0	RW	0x0	UHS_MODE_SEL UHS Mode/eMMC Speed Mode Select. These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. Values: 3'h0: SDR12/Legacy 3'h1: SDR25/High Speed SDR 3'h2: SDR50 3'h3: SDR104/HS200 3'h4: DDR50/High Speed DDR 3'h7: HS400 Others: Reserved

EMMC_CAPABILITIES1

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x1	SLOT_TYPE Slot Type. These bits indicate usage of a slot by a specific Host System. 2'h0: Removable Card Slot 2'h1: Embedded Slot for One Device 2'h2: Shared Bus Slot (SD mode) 2'h3: Reserved
29	RO	0x0	ASYNC_INT_SUPPORT Asynchronous Interrupt Support (SD Mode only). Values: 1'b0: Asynchronous Interrupt Not Supported 1'b1: Asynchronous Interrupt Supported
28	RO	0x0	SYS_ADDR_64_V3 64-bit System Address Support for V3. This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL =11b). Values: 1'b0: 64-bit System Address for V3 is Not Supported 1'b1: 64-bit System Address for V3 is Supported

Bit	Attr	Reset Value	Description
27	RO	0x0	SYS_ADDR_64_V4 64-bit System Address Support for V4. This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: 1'b0: 64-bit System Address for V4 is Not Supported 1'b1: 64-bit System Address for V4 is Supported
26:24	RO	0x0	reserved
23	RO	0x1	SUS_RES_SUPPORT Suspense/Resume Support. This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: 1'b0: Not Supported 1'b1: Supported
22	RO	0x1	SDMA_SUPPORT SDMA Support. This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: 1'b0: SDMA not Supported 1'b1: SDMA Supported
21	RO	0x1	HIGH_SPEED_SUPPORT High Speed Support. This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: 1'b0: High Speed not Supported 1'b1: High Speed Supported
20	RO	0x0	reserved
19	RO	0x1	ADMA2_SUPPORT ADMA2 Support. This bit indicates whether the Host Controller is capable of using ADMA2. Values: 1'b0: ADMA2 not Supported 1'b1: ADMA2 Supported

Bit	Attr	Reset Value	Description
18	RO	0x1	Embedded_8_BIT 8-bit Support for Embedded Device. This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. Values: 1'b0: 8-bit Bus Width not Supported 1'b1: 8-bit Bus Width Supported
17:16	RO	0x1	MAX_BLK_LEN Maximum Block Length. This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit. Values: 2'h0: 512 Byte 2'h1: 1024 Byte 2'h2: 2048 Byte 2'h3: Reserved
15:8	RO	0xc8	BASE_CLK_FREQ Base Clock Frequency for SD clock. These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depend on the Host Controller Version. (1) 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h1: 2 MHz ..... 8'h3f: 63 MHz Others: Reserved (2) 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h0: 2 MHz ..... 8'hff: 255 MHz
7	RO	0x1	TOUT_CLK_UNIT Timeout Clock Unit. This bit shows the unit of base clock frequency used to detect Data TImeout Error. Values: 1'b0: KHz 1'b1: MHz
6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	TOUT_CLK_FREQ Timeout Clock Frequency. This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be KHz or MHz. 6'h0: Get information through another method 6'h1: 1KHz / 1MHz 6'h2: 2KHz / 2MHz 6'h3: 3KHz / 3MHz ..... 6'h3f: 63KHz / 63MHz

EMMC_CAPABILITIES2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ADMA3_SUPPORT ADMA3 Support. This bit indicates whether the Host Controller is capable of using ADMA3. Values: 1'b0: ADMA3 not Supported 1'b1: ADMA3 Supported
24	RO	0x0	reserved
23:16	RO	0x0a	CLK_MUL Clock Multiplier. These bits indicate the clock multiplier of the programmable clock generator. Setting these bits to 0 means that the Host Controller does not support a programmable clock generator. Values: 8'h0: Clock Multiplier is not Supported 8'h1: Clock Multiplier M = 2 8'h2: Clock Multiplier M = 3 ..... 8'hFF: Clock Multiplier M = 256
15:14	RO	0x0	RE_TUNING_MODES Re-Tuning Modes. Values: These bits select the re-tuning method and limit the maximum data length. Values: 2'h0: Timer 2'h1: Timer and Re-Tuning Request (Not supported) 2'h2: Auto Re-Tuning (for transfer) 2'h3: Reserved
13	RO	0x1	USE_TUNING_SDR50 Use Tuning for SDR50. Values: 1'b0: SDR50 does not require tuning 1'b1: SDR50 requires tuning
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RO	0x0	RETUNE_CNT Timer Count for Re-Tuning. Values: 4'h0: Re-Tuning Timer disabled 4'h1: 1 seconds 4'h2: 2 seconds 4'h3: 4 seconds ..... 4'hB: 1024 seconds 4'hC~4'hE: Reserved 4'hF: Get information from other source
7	RO	0x0	reserved
6	RO	0x1	DRV_TYPED This bit indicates support of Driver Type D for 1.8 Signaling. Values: 1'b0: Driver Type D is Not Supported 1'b1: Driver Type D is Supported
5	RO	0x1	DRV_TYPEC This bit indicates support of Driver Type C for 1.8 Signaling. Values: 1'b0: Driver Type C is Not Supported 1'b1: Driver Type C is Supported
4	RO	0x1	DRV_TYPEA This bit indicates support of Driver Type A for 1.8 Signaling. Values: 1'b0: Driver Type A is Not Supported 1'b1: Driver Type A is Supported
3	RO	0x1	UHS2_SUPPORT UHS-II Support. Values: 1'b0: UHS-II is Not Supported 1'b1: UHS-II is Supported
2	RO	0x1	DDR50_SUPPORT DDR50 Support. Values: 1'b0: DDR50 is Not Supported 1'b1: DDR50 is Supported
1	RO	0x1	SDR104_SUPPORT SDR104 Support. Values: 1'b0: SDR104 is Not Supported 1'b1: SDR104 is Supported
0	RO	0x1	SDR50_SUPPORT SDR50 Support. Values: 1'b0: SDR50 is Not Supported 1'b1: SDR50 is Supported

EMMC_FORCE_AUTO_CMD_STAT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7	WO	0x0	FORCE_CMD_NOT_ISSUED_AUTO_CMD12 Force Event for Command Not Issued By Auto CMD12 Error. Values: 1'b0: Not Affected 1'b1: Command Not Issued By Auto CMD12 Error Status is set
6	RO	0x0	reserved
5	WO	0x0	FORCE_AUTO_CMD_RESP_ERR Force Event for Auto CMD Response Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Response Error Status is set
4	WO	0x0	FORCE_AUTO_CMD_IDX_ERR Force Event for Auto CMD Index Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Index Error Status is set
3	WO	0x0	FORCE_AUTO_CMD_EBIT_ERR Force Event for Auto CMD End Bit Error. Values: 1'b0: Not Affected 1'b1: Auto CMD End Bit Error Status is set
2	WO	0x0	FORCE_AUTO_CMD_CRC_ERR Force Event for Auto CMD CRC Error. Values: 1'b0: Not Affected 1'b1: Auto CMD CRC Error Status is set
1	WO	0x0	FORCE_AUTO_CMD12_TOUT_ERR Force Event for Auto CMD Timeout Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Timeout Error Status is set
0	WO	0x0	FORCE_AUTO_CMD12_NOT_EXEC Force Event for Auto CMD12 Not Executed. Values: 1'b0: Not Affected 1'b1: Auto CMD12 Not Executed Status is set

EMMC_FORC_ERR_INT_STAT

Address: Operational Base + offset (0x0052)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	WO	0x0	FORCE_BOOT_ACK_ERR Force Event for Boot Ack error. Values: 1'b0: Not Affected 1'b1: Boot ack Error Status is set
11	WO	0x0	FORCE_RESP_ERR Force Event for Response Error. Values: 1'b0: Not Affected 1'b1: Response Error Status is set

Bit	Attr	Reset Value	Description
10	WO	0x0	FORCE_TUNING_ERR Force Event for Tuning Error (UHS-I Mode only) Values: 1'b0: Not Affected 1'b1: Tuning Error Status is set
9	WO	0x0	FORCE_ADMA_ERR Force Event for ADMA Error. Values: 1'b0: Not Affected 1'b1: ADMA Error Status is set
8	WO	0x0	FORCE_AUTO_CMD_ERR Force Event for Auto CMD Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Error Status is set
7	RO	0x0	reserved
6	WO	0x0	FORCE_DATA_END_BIT_ERR Force Event for Data End Bit Error. Values: 1'b0: Not Affected 1'b1: Data End Bit Error Status is set
5	WO	0x0	FORCE_DATA_CRC_ERR Force Event for Data CRC Error. Values: 1'b0: Not Affected 1'b1: Data CRC Error Status is set
4	WO	0x0	FORCE_DATA_TOUT_ERR Force Event for Data Timeout Error. Values: 1'b0: Not Affected 1'b1: Data Timeout Error Status is set
3	WO	0x0	FORCE_CMD_IDX_ERR Force Event for Command Index Error. Values: 1'b0: Not Affected 1'b1: Command Index Error Status is set
2	WO	0x0	FORCE_CMD_END_BIT_ERR Force Event for Command End Bit Error. Values: 1'b0: Not Affected 1'b1: Command End Bit Error Status is set
1	WO	0x0	FORCE_CMD_CRC_ERR Force Event for Command CRC Error. Values: 1'b0: Not Affected 1'b1: Command CRC Error Status is set
0	WO	0x0	FORCE_CMD_TOUT_ERR Force Event for Command Timeout Error. Values: 1'b0: Not Affected 1'b1: Command Timeout Error Status is set

EMMC_ADMA_ERR_STAT

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved
2	RO	0x0	ADMA_LEN_ERR ADMA Length Mismatch Error States. This error occurs in the following instances: a. While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length; b. When the total data length cannot be divided by the block length Values: 1'b0: No Error 1'b1: Error
1:0	RO	0x0	ADMA_ERR_STATES ADMA Error States. These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: 2'h0: Stop DMA - SYS_ADR register points to a location next to the error descriptor 2'h1: Fetch Descriptor - SYS_ADR register points to the error descriptor 2'h2: Never set this state 2'h3: Transfer Data - SYS_ADR register points to a location next to the error descriptor

EMMC_ADMA_SA

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_SA ADMA System Address. These bits indicate the 32 bits of the ADMA system address. a. SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location b. ADMA2: This register stores the byte address of the executing command of the descriptor table c. ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.

EMMC_PRESET_INIT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DS

Address: Operational Base + offset (0x0062)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_HS

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR12

Address: Operational Base + offset (0x0066)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR25

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR50

Address: Operational Base + offset (0x006A)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR104

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DDR50

Address: Operational Base + offset (0x006E)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator

Bit	Attr	Reset Value	Description
9:0	RO	0x000	FREQ_SEL_VAL SDCLK/RCLK Frequency Select Value. 10-bit preset value to be set in SDCLK/RCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_ADMA_ID

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_ID ADMA Integrated Descriptor Address. These bits indicate the 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address.

EMMC_SLOT_INTR_STATUS

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RO	0x00	INTR_SLOT Interrupt signal for each Slot. Host Controller support single card slot. This register shall always return 0.

EMMC_HOST_CNTRL_VERS

Address: Operational Base + offset (0x00FE)

Bit	Attr	Reset Value	Description
15:8	RO	0x10	VENDOR_VERSION_NUM Vendor Version Number.
7:0	RO	0x05	SPEC_VERSION_NUM Specification Version Number. Values: 8'h0: SD Host Controller Specification Version 1.00 8'h1: SD Host Controller Specification Version 2.00 8'h2: SD Host Controller Specification Version 3.00 8'h3: SD Host Controller Specification Version 4.00 8'h4: SD Host Controller Specification Version 4.10 8'h5: SD Host Controller Specification Version 4.20 Others: Reserved

EMMC_COVER

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x5	EMMC_VER_MAJOR eMMC Major Version Number (digit left of decimal point), in BCD format
7:4	RO	0x1	EMMC_VER_MINOR eMMC Minor Version Number(digit right of decimal point), in BCD format
3:0	RO	0x0	EMMC_VER_SUFFIX eMMC Version Suffix (2nd digit right of decimal point), in BCD format

EMMC_CQCAP

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	CRYPTO_SUPPORT Crypto Support. This bit indicates whether the Host Controller supports cryptographic operations. Values: 1'b0: Crypto not Supported 1'b1: Crypto Supported
27:16	RO	0x000	reserved
15:12	RO	0x0	ITCFMUL Internal Timer Clock Frequency Multiplier. ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. 4'h0: 0.001 MHz 4'h1: 0.01 MHz 4'h2: 0.1 MHz 4'h3: 1 MHz 4'h4: 10 MHz Others: Reserved
11:10	RO	0x0	reserved
9:0	RO	0x000	ITCFVAL Internal Timer Clock Frequency Value. TCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_ STATUS (CMD13) polling. The clock frequency is calculated as ITCFVAL* ITCFMUL. For example, to encode 19.2 MHz, ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz) 192 * 0.1 MHz=19.2 MHz

EMMC_CQCFG

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DCMD_EN Direct Command (DCMD) Enable. This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Values: 1'b0: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1'b1: Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	TASK_DESC_SIZE This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queueing Enable bit is 0 (command queueing is disabled) Values: 1'b0: Task descriptor size is 64 bits 1'b1: Task descriptor size is 128 bits
7:2	RO	0x00	reserved
1	RW	0x0	CR_GENERAL_EN Crypto General Enable. Enable/Disable bit for Crypto Engine. If cryptographic operations are not supported, this status bit is reserved. Values: 1'b0: Disable cryptographic operations for all transactions 1'b1: Enable cryptographic operations for transactions where TD.CE=1 or CRNQP.CE=1
0	RW	0x0	CQ_EN Command Queueing Enable. When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, the software verifies that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it clears all previous tasks (if any) before setting this bit to 0. Values: 1'b0: Disable command queuing 1'b1: Enable command queuing

EMMC_CQCTRL

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	CLR_ALL_TASKS Clear all tasks. This bit can only be written when the controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. Values: 1'b0: Programming 0 has no effect 1'b1: Clears all the tasks in the controller
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	HALT Halt request and resume. Values: 1'b0: RESUME_CQE. Software writes 0 to this bit to exit from the halt state and resume CQE activity 1'b1: HALT_CQE. Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE completes the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE does not issue new commands and indicates to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus.

EMMC_CQIS

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	TCL Task Cleared Interrupt. This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL). Values: 1'b0: TCL Interrupt is not set 1'b1: TCL Interrupt is set
2	W1C	0x0	RED Response Error Detected Interrupt. This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Values: 1'b0: RED Interrupt is not set 1'b1: RED Interrupt is set
1	W1C	0x0	TCC Task Complete Interrupt. This status bit is asserted(if CQISTE.TCC=1) when at least one of the following two conditions are met: a. A task is completed and the INT bit is set in its Task Descriptor b. Interrupt caused by Interrupt Coalescing logic Values: 1'b0: TCC Interrupt is not set 1'b1: TCC Interrupt is set
0	W1C	0x0	HAC Halt Complete Interrupt. This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state. Values: 1'b0: HAC Interrupt is not set 1'b1: HAC Interrupt is set

EMMC_CQISE

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_STE Task Cleared Interrupt status enable. Values: 1'b0: CQIS.TCL is disabled 1'b1: CQIS.TCL is set when its interrupt condition is active
2	RW	0x0	RED_STE Response Error Detected Interrupt status enable. Values: 1'b0: CQIS.RED is disabled 1'b1: CQIS.RED is set when its interrupt condition is active
1	RW	0x0	TCC_STE Task Complete Interrupt status enable. Values: 1'b0: CQIS.TCC is disabled 1'b1: CQIS.TCC is set when its interrupt condition is active
0	RW	0x0	HAC_STE Halt Complete Interrupt status enable. Values: 1'b0: CQIS.HAC is disabled 1'b1: CQIS.HAC is set when its interrupt condition is active

EMMC_CQISGE

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_SGE Task Cleared Interrupt signal enable. Values: 1'b0: CQIS.TCL interrupt signal generation is disabled 1'b1: CQIS.TCL interrupt signal generation is active
2	RW	0x0	RED_SGE Response Error Detected Interrupt signal enable. Values: 1'b0: CQIS.RED interrupt signal generation is disabled 1'b1: CQIS.RED interrupt signal generation is active
1	RW	0x0	TCC_SGE Task Complete Interrupt signal enable. Values: 1'b0: CQIS.TCC interrupt signal generation is disabled 1'b1: CQIS.TCC interrupt signal generation is active
0	RW	0x0	HAC_SGE Halt Complete Interrupt signal enable. Values: 1'b0: CQIS.HAC interrupt signal generation is disabled 1'b1: CQIS.HAC interrupt signal generation is active

EMMC_CQIC

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RW	0x0	INTC_EN Interrupt Coalescing Enable Bit. Values: 1'b0: Interrupt coalescing mechanism is disabled 1'b1: Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated
30:21	RO	0x000	reserved
20	RO	0x0	INTC_STAT Interrupt Coalescing Status Bit. This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). Values: 1'b0: INT0 Task completions have not occurred since last counter reset (INTC counter == 0) 1'b1: At least one INT0 task completion has been counted (INTC counter > 0)
19:17	RO	0x0	reserved
16	WO	0x0	INTC_RST Counter and Timer Reset. When host driver writes 1, the interrupt coalescing timer and counter are reset. Values: 1'b0: No Effect 1'b1: Interrupt coalescing timer and counter are reset
15	WO	0x0	INTC_TH_WEN Interrupt Coalescing Counter Threshold Write Enable. When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle. Values: 1'b0: Clears INTC_TH_WEN 1'b1: Sets INTC_TH_WEN
14:13	RO	0x0	reserved
12:8	WO	0x00	INTC_TH Interrupt Coalescing Counter Threshold filed. Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. 5'h0: Interrupt coalescing feature disabled 5'h1: Interrupt coalescing interrupt generated after 1 task when INT=0 completes 5'h2: Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes ..... 5'h1f: Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation.

Bit	Attr	Reset Value	Description
7	WO	0x0	TOUT_VAL_WEN When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle. Values: 1'b0: clears TOUT_VAL_WEN 1'b1: Sets TOUT_VAL_WEN
6:0	RW	0x00	TOUT_VAL Interrupt Coalescing Timeout Value. Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. 7'h0: Timer is disabled. Timeout-based interrupt is not generated 7'h1: Timeout on 01x1024 cycles of timer clock frequency 7'h2: Timeout on 02x1024 cycles of timer clock frequency ..... 7'h7f: Timeout on 127x1024 cycles of timer clock frequency In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation.

EMMC_CQTDLBA

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDLBA Task Descriptor List Base Address. This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on Byte1 KByte boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

EMMC_CQTDBR

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DBR Command Queueing Task Doorbell. Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: a. When a task execution is completed (with success or error) b. The task is cleared using CQTCLR register c. All tasks are cleared using CQCTL register d. CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.

EMMC_CQTDBN

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCN Task Complete Notification. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has completed execution (with success or errors) Bit-N(0): Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

EMMC_CQDQS

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQS Device Queue Status. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Device has marked task N as ready for execution Bit-N(0): Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command.

EMMC_CQDPT

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPT Device Pending Tasks. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has been successfully queued into the device and is awaiting execution Bit-N(0): Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasnt been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device.

EMMC_CQTCLR

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCLR Command Queueing Task Clear. Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software must poll on the CQTCLR until it is cleared to verify that a clear operation was done.

EMMC_CQSSC1

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:16	RW	0x1	SQSCMD_BLK_CNT Send Status Command Block Counter. This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE sends status command on the CMD line, during the transfer of data block BLOCK_CNTn, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. 4'h0: SEND_QUEUE_STATUS (CMD13) command is not sent during the transaction. Instead, it is sent only when the data lines are idle. 4'h1: SEND_QUEUE_STATUS command is to be sent during the last block of the transaction. 4'h2: SEND_QUEUE_STATUS command when last 2 blocks are pending. 4'h3: SEND_QUEUE_STATUS command when last 3 blocks are pending. ..... 4'hf: SEND_QUEUE_STATUS command when last 15 blocks are pending. Should be programmed only when CQCFG.CQ_EN is '0'.
15:0	RW	0x1000	SQSCMD_IDLE_TMR Send Status Command Idle Timer. This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 ns. Should be programmed only when CQCFG.CQ_EN is '0'.

EMMC_CQSSC2

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	SQSCMD_RCA Send Queue RCA. This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE copies this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

EMMC_CQCRDCT

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DCMD_RESP Direct Command Last Response. This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller.

EMMC_CQRMEM

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0xfdf9a080	RESP_ERR_MASK Response Mode Error Mask. The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. 1'b0: When a R1/R1b response is received, bit i in the device status is ignored. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. 1'b1: When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. Note: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic.

EMMC_CQTERRI

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	TRANS_ERR_FIELDS_VALID Data Transfer Error Field Valid. This bit is updated when an error is detected while a data transfer transaction was in progress. Values: 1'b0: Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX 1'b1: Data transfer related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields
30:29	RO	0x0	reserved
28:24	RO	0x00	TRANS_ERR_TASKID Data Transfer Error Task ID. This field captures the ID of the task that was executed and whose data transfer has errors.
23:22	RO	0x0	reserved
21:16	RO	0x00	TRANS_ERR_CMD_INDX Data Transfer Error Command Index. This field captures the index of the command that was executed and whose data transfer has errors.
15	RO	0x0	RESP_ERR_FIELDS_VALID Response Mode Error Fields Valid. This bit is updated when an error is detected while a command transaction was in progress. Values: 1'b0: Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX 1'b1: Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields

Bit	Attr	Reset Value	Description
14:13	RO	0x0	reserved
12:8	RO	0x00	RESP_ERR_TASKID Response Mode Error Task ID. This field captures the ID of the task which was executed on the command line when the error occurred.
7:6	RO	0x0	reserved
5:0	RO	0x00	RESP_ERR_CMD_INDX Response Mode Error Command Index. This field captures the index of the command that was executed on the command line when the error occurred.

EMMC_CQCRI

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	CMD_RESP_INDX Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

EMMC_CQCRA

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CMD_RESP_ARG Last Command Response Argument. This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

EMMC_VER_ID

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_ID Current version number.

EMMC_VER_TYPE

Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_TYPE Version type.

EMMC_HOST_CTRL3

Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	SW_CG_DIS Internal clock gating disable control. This bit must be used to disable IP's internal clock gating when required. when disabled clocks are not gated. Clocks to the core (except hclk) must be stopped when programming this bit. Values: 1'b0: Internal clock gating is disabled, clocks are not gated internally 1'b1: Internal clock gates are active and clock gating is controlled internally
3:1	RO	0x0	reserved
0	RW	0x1	CMD_CONFLICT_CHECK Command conflict check. Host Controller monitors the CMD line whenever a command is issued and checks whether the value driven on sd_cmd_out matches the value on sd_cmd_in at next subsequent edge of cclk_tx to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (t_card_clk_period - t_setup), where t_setup is the setup time of a flop in Host Controller. The I/O pad delay is consistent across CMD and DATA lines, and it is within the value: (2*t_card_clk_period - t_setup) Values: 1'b0: Disable command conflict check 1'b1: Check for command conflict after 1 card clock cycle

EMMC_EMMC_CTRL

Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	CQE_PREFETCH_DISABLE Enable or Disable CQE's PREFETCH feature. This field allows Software to disable CQE's data prefetch feature when set to 1. Values: 1'b0: CQE can Prefetch data for sucessive WRITE transfers and pipeline sucessive READ transfers 1'b1: Prefetch for WRITE and Pipeline for READ are disabled
9	RW	0x0	CQE_ALGO_SEL Scheduler algorithm selected for execution. This bit selects the Algorithm used for selecting one of the many ready tasks for execution. Values: 1'b0: Priority based reordering with FCFS to resolve equal priority tasks 1'b1: First come First serve, in the order of DBR rings
8	RW	0x0	ENH_STROBE_ENABLE Enhanced Strobe Enable. This bit instructs Host to sample the CMD line using data strobe for HS400 mode. Values: 1'b0: CMD line is sampled using cclk_rx for HS400 mode 1'b1: CMD line is sampled using data strobe for HS400 mode
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x1	EMMC_RST_N_OE Output Enable control for EMMC Device Reset signal PAD control. Values: 1'b0: sd_rst_n_oe is 0 1'b1: sd_rst_n_oe is 1
2	RW	0x1	EMMC_RST_N EMMC Device Reset signal control. This register field controls the sd_rst_n output of Host Controller. Values: 1'b0: Reset to eMMC device asserted 1'b1: Reset to eMMC device is deasserted
1	RW	0x0	DISABLE_DATA_CRC_CHK Disable Data CRC Check. This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: 1'b0: DATA CRC check is enabled 1'b1: DATA CRC check is disabled
0	RW	0x0	CARD_IS_EMMC eMMC Card present. This bit indicates the type of card connected. An application program this bit based on the card connected to Host Controller. Values: 1'b0: Card connected to Host Controller is a non-eMMC card 1'b1: Card connected to Host Controller is an eMMC card

EMMC_BOOT_CTRL

Address: Operational Base + offset (0x052E)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	BOOT_TOUT_CNT Boot Ack Timeout Counter Value. This value determines the interval by which boot ack timeout (50 ms) is detected when boot ack is expected during boot operation. Values: 4'h0: TMCLK x 2^13 4'h1: TMCLK x 2^14 ..... 4'hE: TMCLK x 2^27 4'hF: Reserved
11:9	RO	0x0	reserved
8	RW	0x0	BOOT_ACK_ENABLE Boot Acknowledge Enable. When this bit set, Host checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: 1'b1: Boot Ack enable 1'b0: Boot Ack disable

Bit	Attr	Reset Value	Description
7	RW	0x0	VALIDATE_BOOT Validate Mandatory Boot Enable bit. This bit is used to validate the MAN_BOOT_EN bit. Values: 1'b1: Validate Mandatory boot enable bit 1'b0: Ignore Mandatory boot Enable bit
6:1	RO	0x00	reserved
0	RW	0x0	MAN_BOOT_EN Mandatory Boot Enable. This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The Host Controller clears this bit after the boot transfer is completed or terminated. Values: 1'b1: Mandatory boot enable 1'b0: Mandatory boot disable

EMMC_AT_CTRL

Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:19	RW	0x0	POST_CHANGE_DLY Time taken for phase switching and stable clock output. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
18:17	RW	0x0	PRE_CHANGE_DLY Maximum Latency specification between cclk_tx and cclk_rx. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
16	RW	0x0	TUNE_CLK_STOP_EN Clock stopping control for Tuning and auto-tuning circuit. When enabled, clock gate control output (clk2card_on) is pulled low before changing phase select codes on tuning_cclk_sel and autotuning_cclk_sel. This effectively stops the Device/Card clock, cclk_rx. Changing phase code when clocks are stopped ensures glitch free phase switching. Values: 1'b0: Clocks not stopped 1'b1: Clocks stopped during phase code change
15:5	RO	0x000	reserved
4	RW	0x0	SW_TUNE_EN This fields enables software-managed tuning flow. Values: 1'b0: Software-managed tuning disabled 1'b1: Software-managed tuning enabled

Bit	Attr	Reset Value	Description
3	RW	0x0	RPT_TUNE_ERR Framing errors are not generated when executing tuning. This debug bit allows users to report these errors. Values: 1'b0: Default mode where as per host no errors are reported 1'b1: Debug mode for reporting framing errors
2	RW	0x0	SWIN_TH_EN Sampling window Threshold enable. Selects the tuning mode. Field should be programmed only when SAMPLE_CLK_SEL is '0'. Values: 1'b0: LARGEST_WIN_MODE. Tuning engine sweeps all taps and settles at the largest window. 1'b1: THRESHOLD_MODE. Tuning engine selects the first complete sampling window that meets the threshold set by SWIN_TH_VAL field.
1:0	RO	0x0	reserved

EMMC_AT_STAT

Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	L_EDGE_PH_CODE Left Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Left edge of sampling window.
15:8	RO	0x00	R_EDGE_PH_CODE Right Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Right edge of sampling window.
7:0	RW	0x00	CENTER_PH_CODE Centered Phase code. Reading this field returns the current value on tuning_cclk_sel output. Setting AT_CTRL.SW_TUNE_EN enables software to write to this field and its contents are reflected on tuning_cclk_sel.

EMMC_DLL_CTRL

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	DLL_BYPASS_MODE DLL bypass mode select. 1'b0: Normal 1'b1: Bypass
23:16	RW	0x00	DLL_START_POINT DLL start point for phase detect.
15:8	RW	0x00	DLL_INCRMENT DLL increment value.
7:2	RO	0x00	reserved
1	RW	0x0	DLL_SRST DLL soft reset indication. 1'b0: Normal work 1'b1: Reset

Bit	Attr	Reset Value	Description
0	RW	0x0	DLL_START DLL working indication. 1'b0: DLL is not working 1'b1: DLL is working

EMMC_DLL_RXCLK

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RX_CLK_SRC_SEL RX clock source selection. 1'b0: RX clock source is inverted. 1'b1: RX clock source is no-inverted. This bit should be set to 1 for normal operation.
28	RW	0x0	RX_CLK_CHANGE_WINDOW RX clock change window. When high, RX clock is gated.
27	RW	0x0	RX_CLK_OUT_SEL RX clock output selection. 1'b0: RX clock output is from RX clock source or RX clock source with invertion, determined by RX_CLK_SRC_SEL 1'b1: RX clock output is delayed by delayline
26	RW	0x0	RX_DELAY_NUM_SEL Delay number selection for RX clock. 1'b0: Delaynum comes from hardware calculation 1'b1: Delaynum comes from software (RX_DELAY_NUM)
25	RW	0x0	RX_TAP_VALUE_SEL Tap value selection for RX clock. 1'b0: Tapvalue equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tapvalue comes from software (TX_TAP_VALUE)
24	RW	0x0	RX_TAP_NUM_SEL Tapnum selection for RX clock. 1'b0: Tapnum comes from tuning result 1'b1: Tapnum comes from software (RX_TAP_NUM)
23:16	RW	0x00	RX_DELAY_NUM Total delay number of selected tap for RX clock.
15:8	RW	0x00	RX_TAP_VALUE Tap value for RX clock. It denotes delay element number for RX clock.
7:5	RO	0x0	reserved
4:0	RW	0x00	RX_TAP_NUM Tap number for RX clock. Every clock is divided into 32 taps equably, and the max value is 31. Use tapnum to select which tap to be used for RX clock.

EMMC_DLL_TXCLK

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	TX_CLK_OUT_SEL TX clock output selection. 1'b0: TX clock output is from TX clock source with invertion 1'b1: TX clock output is delayed by delayline

Bit	Attr	Reset Value	Description
26	RW	0x0	TX_DELAY_NUM_SEL Delay number selection for TX clock. 1'b0: Delaynum comes from hardware calculation 1'b1: Delaynum comes from software (TX_DELAY_NUM)
25	RW	0x0	TX_TAP_VALUE_SEL Tap value selection for TX clock. 1'b0: Tapvalue equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tapvalue comes from software (TX_TAP_VALUE)
24	RW	0x0	TX_TAP_NUM_SEL Tapnum selection for TX clock. 1'b0: Tapnum is 8 1'b1: Tapnum comes from software (TX_TAP_NUM)
23:16	RW	0x00	TX_DELAY_NUM Total delay number of selected tap for TX clock.
15:8	RW	0x00	TX_TAP_VALUE Tap value for TX clock. It denotes delay element number for TX clock.
7:5	RO	0x0	reserved
4:0	RW	0x00	TX_TAP_NUM Tap number for TX clock. Every clock is divided into 32 taps equably, and the max value is 31. Use tapnum to select which tap to be used for TX clock.

EMMC_DLL_STRBIN

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	STRBIN_DELAY_ENA STRBIN delay enable. 1'b0: Disable 1'b1: Enable
26	RW	0x0	STRBIN_DELAY_NUM_SEL Delay number selection for STRBIN. 1'b0: Delaynum comes from hardware calculation 1'b1: Delaynum comes from software (STRBIN_DELAY_NUM)
25	RW	0x0	STRBIN_TAP_VALUE_SEL Tap value selection. 1'b0: Tapvalue equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tapvalue comes from software (STRBIN_TAP_VALUE)
24	RW	0x0	STRBIN_TAP_NUM_SEL Tapnum selection for STRBIN. 1'b0: Tapnum is 8 1'b1: Tapnum comes from software (STRBIN_TAP_NUM)
23:16	RW	0x00	STRBIN_DELAY_NUM Total delay number of selected tap for STRBIN.
15:8	RW	0x00	STRBIN_TAP_VALUE Tap value for STRBIN. It denotes delay element number for STRBIN.
7:5	RO	0x0	reserved
4:0	RW	0x00	STRBIN_TAP_NUM Tap number for STRBIN. Every clock is divided into 32 taps equably, and the max value is 31. Use tapnum to select which tap to be used for STRBIN.

EMMC_DLL_STATUS0

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	DLL_LOCK_TIMEOUT DLL phase detection is timeout or not. 1'b0: Not timeout 1'b1: Timeout
8	RO	0x0	DLL_LOCK DLL lock indication. 1'b0: DLL is not locked 1'b1: DLL is locked
7:0	RO	0x00	DLL_LOCK_VALUE DLL lock value for half sdclk cycle. It denotes the delay element number needed for DLL locked. It is valid when dll_lock is high.

EMMC_DLL_STATUS1

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	DLL_STRBIN_DELAY_VALUE Delay element number used for STRBIN.
15:8	RO	0x00	DLL_RXCLK_DELAY_VALUE Delay element number used for RX clock.
7:0	RO	0x00	DLL_TXCLK_DELAY_VALUE Delay element number used for TX clock.

7.5 Interface Description

7.5.1 EMMC Interface Description

Table 7-1 EMC Interface Description

Module Pin	Direction	PAD Name	IOMUX Setting
emmc_cclk	O	EMMC_CLKOUT/FLASH_DQS/GPIO1_C5_d	GRF_GPIO1C_IOMUX_H[7:4]=4'h1
emmc_ccmd	I/O	EMMC_CMD/FLASH_WRn/GPIO1_C4_u	GRF_GPIO1C_IOMUX_H[3:0]=4'h1
emmc_cdata0	I/O	EMMC_D0/FLASH_D0/GPIO1_B4_u	GRF_GPIO1B_IOMUX_H[3:0]=4'h1
emmc_cdata1	I/O	EMMC_D1/FLASH_D1/GPIO1_B5_u	GRF_GPIO1B_IOMUX_H[7:4]=4'h1
emmc_cdata2	I/O	EMMC_D2/FLASH_D2/GPIO1_B6_u	GRF_GPIO1B_IOMUX_H[11:8]=4'h1
emmc_cdata3	I/O	EMMC_D3/FLASH_D3/GPIO1_B7_u	GRF_GPIO1B_IOMUX_H[15:12]=4'h1
emmc_cdata4	I/O	EMMC_D4/FLASH_D4/GPIO1_C0_u	GRF_GPIO1C_IOMUX_L[3:0]=4'h1
emmc_cdata5	I/O	EMMC_D5/FLASH_D5/GPIO1_C1_u	GRF_GPIO1C_IOMUX_L[7:4]=4'h1
emmc_cdata6	I/O	EMMC_D6/FLASH_D6/GPIO1_C2_u	GRF_GPIO1C_IOMUX_L[11:8]=4'h1
emmc_cdata7	I/O	EMMC_D7/FLASH_D7/GPIO1_C3_u	GRF_GPIO1C_IOMUX_L[15:12]=4'h1
emmc_strbin	I	EMMC_DATA_STROBE/FSPI_CS1n/FLASH_CLE/GPIO1_C6_d	GRF_GPIO1C_IOMUX_H[11:8]=4'h1
emmc_rstn	O	EMMC_RSTn/FSPI_D2/FLASH_WPn/GPIO1_C7_d	GRF_GPIO1C_IOMUX_H[15:12]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

7.6 Application Notes

7.6.1 Clock Adjustment

Phase detection is needed if you want to know the card clock's precision before clock adjustment. The detection flow is as below:

(1) Set EMMC_DLL_CTRL[1]=1 to reset the EMMC DLL; then set EMMC_DLL_CTRL[1]=0 to dis-reset EMMC DLL;

(2) Set DLL_START_POINT in EMMC_DLL_CTRL[23:16]; set DLL_INCREMENT in EMMC_DLL_CTRL[15:8], and set EMMC_DLL_CTRL[0] to start the DLL phase detection.

(3) Wait for DLL lock until EMMC_DLL_STATUS0[8] equals to 1. Get the EMMC_DLL_STATUS0[7:0] as the locked value for the half card clock cycle time.

(4) If EMMC_DLL_STATUS0[9]=1 and EMMC_DLL_STATUS0[8]=0, the detection is timeout, you can adjust the DLL_START_POINT or DLL_INCREMENT to re-detection. You need to set EMMC_DLL_CTRL[0] to 0 before you restart phase detection as(1)~(3).

After phase detection, the clock's precision is shown in EMMC_DLL_STATUS0[7:0](DLL_LOCK_VALUE) based on delay element. We can calculate the delay element numbers requirement for TXCLK/RXLCK/STRBIN(denoted as "XX") as follows:

(1) Get tap value: if XX_TAP_VALUE_SEL=0, tap value equals to (DLL_LOCK_VALUE*2)%256; else tap value is set by software, XX_TAP_VALUE;

(2) Get tap number: if XX_TAP_NUM_SEL=0, tap number comes from Host Controller; else tap number is set by software, XX_TAP_NUM;

(3) Get required delay element numbers: if XX_DELAY_NUM_SEL=0, delay element number equals to tap value* tap number; else delay element number is set by software, XX_DELAY_NUM.

The adjustment value for every clock(XX) is equals to required delay element numbers*delay time of every element.

The delay time of every element is in the range of 32ps~70ps, varying with different voltage and temperature.

Chapter 8 Nand Flash Controller (NandC)

8.1 Overview

Nand Flash Controller (NandC) is used to control data transmission from host to flash device or from flash device to host. NandC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.

NandC supports the following features:

- Software Interface Type
  - Support directly mode
  - Support LLP(Linked List Pointer) mode
- Flash Interface Type
  - Support Asynchronous Flash Interface with 8bits data width ("Asyn8x" for short)
  - Support ONFI Synchronous Flash Interface ("ONFI Syn" for short)
  - Support Toggle Flash Interface ("Toggle" for short)
  - Support 2 flash devices at most
- Flash Type
  - Support Managed NAND Flash(LBA) and Raw NAND Flash(NO-LBA)
  - Support SLC/MLC/TLC Flash
- Flash Interface Timing
  - Asyn8x: configurable timing, one byte per two host clocks at the fastest speed
  - ONFI Syn: configurable timing, two bytes per two host clocks at the fastest speed
  - Toggle: configurable timing, two byte per two host clocks at the fastest speed
- Randomizer Ability
  - Support two randomizer mode with different polynomial
  - Support two randomizer width, 8bit and 16bit parallel
- BCH/ECC Ability
  - 24bit/1KB BCH/ECC: support 24 bit BCH/ECC, which can detect and correct up to 24 error bits in every 1K bytes data
  - 40bit/1KB BCH/ECC: support 40 bit BCH/ECC, which can detect and correct up to 40 error bits in every 1K bytes data
  - 60bit/1KB BCH/ECC: support 60 bit BCH/ECC, which can detect and correct up to 60 error bits in every 1K bytes data
  - 70bit/1KB BCH/ECC: support 70 bit BCH/ECC, which can detect and correct up to 70 error bits in every 1K bytes data
  - 24bit/512B BCH/ECC: support 24 bit BCH/ECC, which can detect and correct up to 24 error bits in every 512 bytes data
  - 40bit/512B BCH/ECC: support 40 bit BCH/ECC, which can detect and correct up to 40 error bits in every 512 bytes data
  - 60bit/512B BCH/ECC: support 60 bit BCH/ECC, which can detect and correct up to 60 error bits in every 512 bytes data
  - 70bit/512B BCH/ECC: support 70 bit BCH/ECC, which can detect and correct up to 70 error bits in every 512 bytes data
- Transmission Ability
  - Support 32K bytes data transmission at a time at most
  - Support two transfer working modes: Bypass or DMA
  - Support two transfer codewords size for Managed NAND Flash: 1024 bytes/codeword or 512 bytes/codeword
- Internal Memory
  - 2 built-in srams, and the size is 1k bytes respectively
  - Can be accessed by other masters
  - Can be operated in pingpong mode by other masters

8.2 Block Diagram

NandC comprises with:

- MIF: AHB Master Interface
- SIF : AHB Slave Interface
- SRIF : Sram Interface

- TRANSC : Transfer Controller
- LLPC : LLP Controller
- BCHENC : BCH Encoder
- BCHDEC : BCH Decoder
- RANDMZ : Randomizer
- FIF_GEN : Flash Interface Generation
- DLC : Delay Line Controller
- NAND_IO : Flash IO Interface

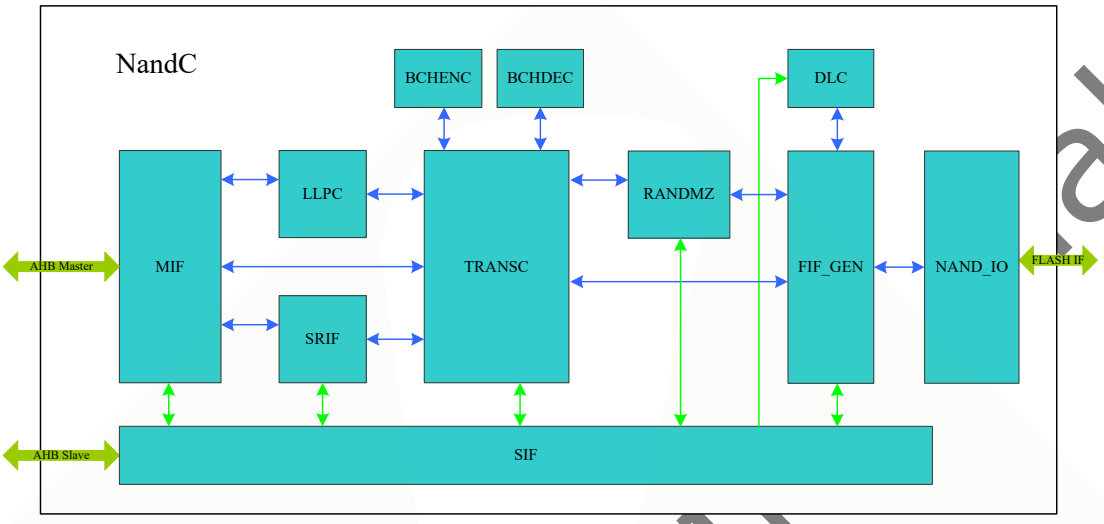


Fig. 8-1 NandC Block Diagram

8.3 Function Description

8.3.1 AHB Interface

There is an AHB master interface in NandC, which is selectable and configurable. It is responsible for transferring data from external memory to internal memory when flash program, or inverse when flash read; and transferring LLP data from external memory to internal register file when LLP is active.

There is an AHB slave interface in NandC. It is responsible for accessing registers and internal memories. The addresses of these registers and memories are listed in 1.4.1.

8.3.2 Flash Type/Flash Interface

Flash device with different types of interfaces is supported. These interfaces include: asynchronous 8bits flash interface, ONFI synchronous flash interface, toggle flash interface, and so on. You can select one of them by software (configure FMCTL) to suit for these devices. Also you can configure their timing parameters by software (configure FMWAIT_ASYN/FMWAIT_SYN) to have your desired rate.

8.3.3 Linked List Pointer Mode (LLP)

To save the software resource and improve the performance, a LLP is add, which is selectable. When LLP is selected, the flash operation instructions stored in external memory with specific format should be loaded for flash working. The detailed format and working flow are referred to 15.7.8.

8.3.4 BCH Encoder/BCH Decoder

The BCH Encoder is responsible for encoding data to be written into flash device. The max encoded length is 1152bytes, in which the data length is 1024bytes, system information is 4bytes, BCH code is 124bytes.

The BCH Decoder is responsible for decoding data read from flash device. The max decoded length is 1152bytes, in which the data length is 1024bytes, spare length is 128bytes.

8.3.5 Randomizer

To improve device lifetime, a randomizer is added in NandC. It includes two parts: Scrambler and Descrambler, which is responsible for scrambling data to be written into flash after bch encoding, and descrambling data read from flash before bch decoding.

8.3.6 Delay Line Controller

For ONFI Synchronous Flash or Toggle Flash, the data read from flash follows with a strobe

signal: DQS, where a skew between them exists. To remove the skew and improve the timing between data and DQS, a Delay Line Controller is needed. It is responsible for detecting the phase of the signal similar to DQS, determining the element number to be shifted, and then shifting the DQS with the determined number.

8.3.7 NAND_IO

Different Interface signals such as asynchronous, onfi and toggle interface are multiplexed and some related logic are included.

8.4 Register Description

8.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Name	Offset	Size	Reset Value	Description
NANDC_FMCTL	0x0000	W	0x00000A00	Flash Interface Control Register
NANDC_FMWAIT_ASYN	0x0004	W	0x3F3FF7FF	Flash Timing Control Register For Asynchronous Timing
NANDC_FMWAIT_SYN	0x0008	W	0x00000000	Flash Timing Control Register For Synchronous Timing
NANDC_FLCTL	0x0010	W	0x00100000	Internal Transfer Control Register
NANDC_FIFO_ACCESS	0x0014	W	0x00000000	FIFO access Register
NANDC_BCHCTL	0x0020	W	0x00000008	BCH Control Register
NANDC_MTRANS_CFG	0x0030	W	0x000001D0	Bus Transfer Configuration Register
NANDC_MTRANS_SADDR0	0x0034	W	0x00000000	Start Address Register For Page Data Transmission
NANDC_MTRANS_SADDR1	0x0038	W	0x00000000	Start Address Register For Spare Data Transmission
NANDC_MTRANS_STAT	0x0040	W	0x00000000	Bus Transfer Status Register
NANDC_MTRANS_STAT2	0x0044	W	0x00000000	Bus Transfer Status Register2
NANDC_DLL_CTL_REG0	0x0050	W	0x007F7F05	DLL Control Register 0
NANDC_DLL_CTL_REG1	0x0054	W	0x00000022	DLL Control Register 1
NANDC_DLL_OBS_REG0	0x0058	W	0x00000200	DLL Status Register
NANDC_NANDC_VER	0x0080	W	0x56393030	Nandc Version Register
NANDC_LLP_CTL	0x0090	W	0x00000000	LLP Control Register
NANDC_LLP_STAT	0x0094	W	0x00000001	LLP Status Register
NANDC_LLI_FOP7	0x00A0	W	0x00000000	LLI flash operation byte 7;
NANDC_LLI_FOP8	0x00A4	W	0x00000000	LLI flash operation byte 8;
NANDC_LLI_FOP9	0x00A8	W	0x00000000	LLI flash operation byte 9;
NANDC_LLI_FOP10	0x00AC	W	0x00000000	LLI flash operation byte 10;
NANDC_LLI_FOP11	0x00B0	W	0x00000000	LLI flash operation byte 11;
NANDC_LLI_FOP12	0x00B4	W	0x00000000	LLI flash operation byte 12;
NANDC_LLI_FOP13	0x00B8	W	0x00000000	LLI flash operation byte 13;
NANDC_LLI_FOP14	0x00BC	W	0x00000000	LLI flash operation byte 14;
NANDC_LLI_NXT_LLP	0x00C0	W	0x00000000	Next LLI
NANDC_LLI_FOP0	0x00C4	W	0x00000000	LLI flash operation byte 0;
NANDC_LLI_FOP1	0x00C8	W	0x00000000	LLI flash operation byte 1;

Name	Offset	Size	Reset Value	Description
NANDC_LLI_FOP2	0x00CC	W	0x00000000	LLI flash operation byte 2;
NANDC_LLI_FOP3	0x00D0	W	0x00000000	LLI flash operation byte 3;
NANDC_LLI_FOP4	0x00D4	W	0x00000000	LLI flash operation byte 4;
NANDC_LLI_FOP5	0x00D8	W	0x00000000	LLI flash operation byte 5;
NANDC_LLI_FOP6	0x00DC	W	0x00000000	LLI flash operation byte 6;
NANDC_INTEN	0x0120	W	0x00000000	NandC Interrupt Enable Register
NANDC_INTCLR	0x0124	W	0x00000000	NandC Interrupt Clear Register
NANDC_INTST	0x0128	W	0x00000000	NandC Interrupt Status Register
NANDC_BCHST0	0x0150	W	0x80000000	BCH Status Register For Codeword 0~1
NANDC_BCHST1	0x0154	W	0x00000000	BCH Status Register For Codeword 2~3
NANDC_BCHST2	0x0158	W	0x00000000	BCH Status Register For Codeword 4~5
NANDC_BCHST3	0x015C	W	0x00000000	BCH Status Register For Codeword 6~7
NANDC_BCHST4	0x0160	W	0x00000000	BCH Status Register For Codeword 8~9
NANDC_BCHST5	0x0164	W	0x00000000	BCH Status Register For Codeword 10~11
NANDC_BCHST6	0x0168	W	0x00000000	BCH Status Register For Codeword 12~13
NANDC_BCHST7	0x016C	W	0x00000000	BCH Status Register For Codeword 14~15
NANDC_BCHST8	0x0170	W	0x00000000	BCH Status Register For Codeword 16~17
NANDC_BCHST9	0x0174	W	0x00000000	BCH Status Register For Codeword 18~19
NANDC_BCHST10	0x0178	W	0x00000000	BCH Status Register For Codeword 20~21
NANDC_BCHST11	0x017C	W	0x00000000	BCH Status Register For Codeword 22~23
NANDC_BCHST12	0x0180	W	0x00000000	BCH Status Register For Codeword 24~25
NANDC_BCHST13	0x0184	W	0x00000000	BCH Status Register For Codeword 26~27
NANDC_BCHST14	0x0188	W	0x00000000	BCH Status Register For Codeword 28~29
NANDC_BCHST15	0x018C	W	0x00000000	BCH Status Register For Codeword 30~31
NANDC_SPARE0_0	0x0200	W	0xFFFFFFFF	System Information for codeword 0

Name	Offset	Size	Reset Value	Description
NANDC_SPARE1_0	0x0204	W	0xFFFFFFFF	System Information for codeword 1
NANDC_RANDMZ_CFG	0x0208	W	0x00000000	Randomizer Configure Register
NANDC_SEED_BCHST	0x020C	W	0x00000000	Bchst Seed

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.2 Detail Register Description

NANDC_FMCTL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	data_mux_sel Used to select nandc pin function. 1'b0: dq0~7 pin used as "DQ[0]~[7]" function. 1'b1: dq0~7 pin used as "DQ[7]~[0]" function.
22	RW	0x0	cmd_mux_sel Used to select nandc pin function. 1'b0: Wp pin used as "WP" function, We pin used as "WE" function, Ale pin used as "ALE" function, Cle pin used as "CLE" function. 1'b1: Wp pin used as "CLE" function, We pin used as "ALE" function, Ale pin used as "WE" function, Cle pin used as "WP" function.
21	RW	0x0	diff_mux_sel Used to select nandc pin function. 1'b0: rdn pin used as "RE" function, dqs pin used as "DQS" function. 1'b1: rdn pin used as "DQS" function, dqs pin used as "RE" function.
20:18	RW	0x0	sif_read_delay Used to control the delay time when asynchronous mode.
17	RO	0x0	flash_abort_stat Function1: flash_abort_stat, RO. Function2: flash_abort_clear, RW, auto clear. flash_abort_stat is set to 1 when flash abort if flash_abort_en=1, set to 0 when flash_abort_clear=1.

Bit	Attr	Reset Value	Description
16	RW	0x0	flash_abort_en Flash abort protect enable signal, 1 active. 1'b0: Flash abort protect disable. 1'b1: Flash abort protect enable. Notes: 1. When in dma mode, if the time from last read operation start to the last read valid exceeds 1024 cycles, flash_abort_stat is set to high. 2. When in bypass mode, if the time from current read operation start to the read valid exceed 1024 cycles, flash_abort_stat is set to high. 3. When in llp bypass read/read match mode, when the operation is long than 1024 cycles, flash_abort_stat is set to high.
15	RW	0x0	syn_mode Toggle enable signal, 1 active. 1'b0: ONFI synchronous flash 1'b1: Toggle synchronous flash
14	RW	0x0	syn_clken Synchronous flash clock enable signal, 1 active. Only available in Synchronous Mode. 1'b0: Flash clock is disabled. 1'b1: Flash clock is enabled.
13	RW	0x0	tm Timing mode indication. 1'b0: Asynchronous Mode 1'b1: Synchronous Mode (Toggle or ONFI Synchronous)
12	RO	0x0	reserved
11	RO	0x1	dma_f_flag Indication for the all f byte in the current DMA transmission. 1'b0: The transmission is not all f. 1'b1: The transmission is all f.
10	RO	0x0	fifo_empty FIFO empty signal. 1'b0: FIFO is not empty; 1'b1: FIFO is emtpy;
9	RO	0x1	frdy Flash ready/busy indicate signal. 1'b0: Flash is busy. 1'b1: Flash is ready. This bit is the sample of the pin of R/Bn.
8	RW	0x0	wp Flash write protect. 1'b0: Flash program/erase disabled. 1'b1: Flash program/erase enabled. This bit is output to the pin of WPn.

Bit	Attr	Reset Value	Description
7	RW	0x0	fcs7 Flash memory chip 7 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
6	RW	0x0	fcs6 Flash memory chip 6 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
5	RW	0x0	fcs5 Flash memory chip 5 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
4	RW	0x0	fcs4 Flash memory chip 4 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
3	RW	0x0	fcs3 Flash memory chip 3 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
2	RW	0x0	fcs2 Flash memory chip 2 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
1	RW	0x0	fcs1 Flash memory chip 1 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.
0	RW	0x0	fcs0 Flash memory chip 0 select control. 1'b1: Hold flash memory chip select activity. 1'b0: Flash memory chip select activity free.

NANDC_FMWAIT_ASYN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	fmw_dly_en fmw_dly enable signal, 1 active.
29:24	RW	0x3f	fmw_dly The number of delay cycle between two codeword transmission.
23	RO	0x0	reserved
22:18	RW	0x0f	wait_frdy_dly The number of delay cycle to accept the flash ready signal.

Bit	Attr	Reset Value	Description
17:12	RW	0x3f	csrw When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the falling edge of CSn to the falling edge of RDn or WRn. The min value of csrw is 0.
11	RW	0x0	hard_rdy Hardware handshaking controller bit. When asserted, an external device asserts signal "RDY" to extend a wait-state access and the rest bits in this register will be ignored.
10:5	RW	0x3f	rwpw When in Asynchronous mode or Toggle address/command mode, this field specifies the width of RDn or WRn in processor clock cycles, 0x0<=rwpw<=0x3f.
4:0	RW	0x1f	rwcs When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the rising edge of RDn or WRn to the rising edge of CSn, 0x0<=rwcs<=0x1f.

NANDC_FMWAIT_SYN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ssyn_xle_sel ALE/CLE selection signal for ONFI synchronous flash. 1'b0: ALE/CLE aligned to the falling edge of WRN. 1'b1: ALE/CLE aligned to the center of WRN low level.
14:9	RW	0x00	pst Write/Read Postamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for Postamb- le time.
8:3	RW	0x00	pre Write/Read Preamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycle for preamble time.
2:0	RW	0x0	fclk Half hclk cycle number for flash clock for ONFI synchronous mode or Toggle data mode.

NANDC_FLCTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	bypass_fifo_mode The enable sigal for bypass with fifo mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	async_tog_mix Nandc async mode and tog mode compatible control 1'b0: Async write data can't be read by tog read. 1'b1: Async write data can be read by tog read.
28	RW	0x0	low_power Nandc low power control 1'b0: Normal mode 1'b1: Low power mode
27:22	RW	0x00	page_num Transmission codeword number in internal DMA mode when bus-mode is master-mode. 1~32: 1~32 codeword. default: Not support. Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is master-mode.
21	RW	0x0	page_size Transmission codeword size in internal DMA mode. 1'b0: 1024bytes/codeword 1'b1: 512bytes/codeword Note: only used when lba_en=1.
20	RO	0x1	tr_rdy Internal DMA transmission ready indication. 1'b0: Internal DMA transmission is busy. 1'b1: Internal DMA transmission is ready. When reading flash, tr_rdy should not be set to 1 until all data transmission and correct finished. When programing flash, tr_rdy should not be set to 1 until all data transmission finished. Notes: Only active in internal DMA mode.
19	RW	0x0	bchst_trans Transmission the status of BCH to external memory. 1'b0: Not transmission 1'b1: Transmission
18:13	RO	0x00	reserved
12	RW	0x0	lba_spare_sel Spare byte number selector when lba_en=1. 1'b0: Spare size is 0. 1'b1: Spare size is 4bytes.

Bit	Attr	Reset Value	Description
11	RW	0x0	lba_en LBA mode indication, 1 active. 1'b0: NO-LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by BCHCTL[16](bchpage), spare size is 46/74/109 bytes or 127 bytes determined by BCHCTL[27:25]. 1'b1: LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by FLCTL[21](page_size), spare size is determined by FLCTL[12](lba_spare_sel). Notes: a. When lba_en is active, BCH CODEC should be disabled, spare_size and page_size are configurable. b. When lba_en is active, cor_able is inactive.
10	RW	0x0	cor_able Auto correct enable indication, 1 active. 1'b0: Auto correct disable 1'b1: Auto correct enable Notes: a. Only active in internal DMA mode. b. lba_en is prior to cor_able. When lba_en=1, cor_able is ignored.
9	RW	0x0	trans_seed Transfer the randomizer seed to flash. 1'b0: Not transfer the seed to flash. 1'b1: Transfer the seed to flash.
8	RW	0x0	not_trans_data Not Transfer the data. 1'b0: Transfer the data with spare. 1'b1: Not transfer the data.
7	RW	0x0	flash_st_mod Mode for NandC to start internal data transmission in internal DMA mode. 1'b0: Busy mode: hardware should not start internal data transmission until flash is ready even flash_st is asserted. 1'b1: Ready mode: hardware should start internal data transmission directly when flash_st is asserted. Notes: Only active in internal DMA mode.

Bit	Attr	Reset Value	Description
6:5	RW	0x0	tr_count Transmission codeword number in internal DMA mode when bus-mode is slave-mode. 2'b00: 0 codeword need transferred 2'b01: 1 codeword need transferred 2'b10: 2 codeword need transferred 2'b11: Not supported Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is slave-mode.
4	RW	0x0	st_addr Start buffer address. 1'b0: Start transfer from sram0. 1'b1: Start transfer from sram1. Notes: Only active in internal DMA mode.
3	RW	0x0	bypass NandC internal DMA bypass indication. 1'b0: Bypass the internal DMA, data are transferred to/from flash by direct path. 1'b1: Internal DMA active, data are transferred to/from flash by internal DMA.
2	R/W SC	0x0	flash_st Start signal for NandC to transfer data between flash and internal buffer in internal DMA mode. When asserted, it will auto cleared. 1'b0: Not start transmission. 1'b1: Start transmission. Notes: Only active in internal DMA mode.
1	RW	0x0	flash_rdn Indicate data flow direction. 1'b0: NandC read data from flash. 1'b1: NandC write data to flash
0	R/W SC	0x0	flash_rst NandC software reset indication. When asserted, it will auto cleared. 1'b0: Not software reset 1'b1: Software reset Notes: flash_rst is prior to flash_st.

NANDC_FIFO_ACCESS

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	fifo_cnt Indicate valid data number 2'b00: Indicate byte0~2 are invalid. 2'b01: Indicate byte0 is valid. 2'b10: Indicate byte0~1 are valid. 2'b11: Indicate byte0~2 are valid.
29:28	WO	0x0	byte2_attr Indicate byte2 attribute. 2'b00: Data 2'b01: Address 2'b10: Command 2'b11: Data
27:26	WO	0x0	byte1_attr Indicate byte1 attribute 2'b00: Data 2'b01: Address 2'b10: Command 2'b11: Data
25:24	WO	0x0	byte0_attr Indicate byte0 attribute 2'b00: Data 2'b01: Address 2'b10: Command 2'b11: Data
23:16	WO	0x00	fifo_byte2 Byte2 of transfer data
15:8	WO	0x00	fifo_byte1 Byte1 of transfer data
7:0	WO	0x00	fifo_byte0 Byte0 of transfer data

NANDC_BCHCTL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RW	0x0	bchmode BCH mode selection 3'b000: 70bitBCH 3'b001: 24bitBCH 3'b010: 40bitBCH 3'b011: 60bitBCH
24:17	RW	0x00	bchthres BCH error number threshold

Bit	Attr	Reset Value	Description
16	RW	0x0	bchpage The data size indication when BCH is active. 1'b0: 1024 bytes, all the 1024 bytes data in codeword are valid data to be transferred. 1'b1: 512 bytes, higher 512bytes are valid, and lower 512bytes are invalid and stuffed with 0xff. Notes: a. Only active when data transferred in internal DMA mode. b. Only active for asynchronous flash.
15:4	RO	0x000	reserved
3	RW	0x1	bchepd BCH encoder/decoder power down indication. 1'b0: BCH encoder/decoder working. 1'b1: BCH encoder/decoder not working.
2	RW	0x0	bch_gate_en Bch decoder clock gating enable, high active. 1'b0: Normal mode 1'b1: Clock gating mode
1	RW	0x0	wcnt_clear To clear the write counter of BCHST. When asserted, it will auto cleared. 1'b0: Not clear the counter. 1'b1: Clear the counter.
0	R/W SC	0x0	bchrst BCH software reset indication. When asserted, it will auto cleared. 1'b0: Not software reset 1'b1: Software reset Notes: a. BCH Decoder should be software reset before decode begin. b. bch software reset should be used with nandc software reset at the same time.

NANDC_MTRANS_CFG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	redundance_size The num of all f byte to write to flash, the maximum of the size is 2K -1.
15	R/W SC	0x0	ahb_rst ahb master interface software reset, auto cleared.

Bit	Attr	Reset Value	Description
14	RW	0x0	fl_pwd Flash power down indication, 1 active. 1'b0: Flash power on, data transferred through master interface is data that to be written into or read from flash. 1'b1: Flash power down, data transferred through master interface is not data that to be written into or read from flash. NandC is just used as DMA for external memory and internal memory.
13:9	RW	0x00	incr_num AHB Master incr num indication. incr_num=1~16. When burst=001, software should configure incr_num. Notes: Only active for master-mode.
8:6	RW	0x7	burst AHB Master burst type indication 3'b000: Single transfer 3'b011: 4-beat burst 3'b101: 8-beat Burst 3'b111: 16-beat burst default: Not supported Notes: Only active for master-mode.
5:3	RW	0x2	hsize AHB Master data size indication. 3'b000: 8 bits 3'b001: 16 bits 3'b010: 32 bits default: Not supported Notes: Only active for master-mode.
2	RW	0x0	bus_mode Bus interface selection. 1'b0: Slave interface, flash data is transferred through slave interface. 1'b1: Master interface, flash data is transferred through master interface.
1	RW	0x0	ahb_wr Data transfer direction through master interface. 1'b0: Write direction(internal memory ->external memory). 1'b1: Read direction(external memory->internal memory). Notes: a. Only active for master-mode. b. When read flash(flash_rdn=0), ahb_wr=1; when program flash(flash_rdn=1), ahb_wr=0.

Bit	Attr	Reset Value	Description
0	R/W SC	0x0	ahb_wr_st Start indication for loading data from external memory to internal memory or storing data from internal memory to external memory through master. When asserted, it will auto cleared. Notes: a. Only active for master-mode and fl_pwd=1. b. When fl_pwd=0, flash is active, NandC start to transfer data through master interface if flash_st=1. c. When fl_pwd=1, flash is not active, NandC start to transfer data through master interface if ahb_wr_st=1.

NANDC_MTRANS_SADDR0

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr0 Start address for page data transmision. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_SADDR1

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr1 Start address for spare data. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_STAT

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RO	0x00	mtrans_cnt Finished counter for codeword transmission through Master interface. Notes: Only active for master-mode.
15:0	RO	0x0000	bus_err Bus error indication for codeword0~15. Bit 0: Bus error for codeword 0. ..... Bit 15: Bus error for codeword 15. Notes: Only active for master-mode.

NANDC_MTRANS_STAT2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	bus_err2 Bus error indication for codeword16~31. Bit 0: Bus error for codeword 16 ..... Bit 15: Bus error for codeword 31 Notes: Only active for master-mode.

NANDC_DLL_CTL_REG0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x7f	dll_dqs_dly_bypass Holds the read DQS delay setting when the DLL is operating in bypass mode.
15:8	RW	0x7f	dll_dqs_dly Holds the read DQS delay setting when the DLL is operating in normal mode. Typically, this value is 1/4 of a clock cycle. Each increment of this field represents 1/128th of a clock cycle.
7:0	RW	0x05	dll_start_point DLL Start Point Control. This value is loaded into the DLL at initialization and is the value at which the DLL will begin searching for a lock. Each increment of this field represents 1/128th of a clock cycle.

NANDC_DLL_CTL_REG1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:4	RW	0x02	dll_incr DLL Increment Value. This sets the increment used by the DLL when searching for a lock. It is recommended keeping this field small (around 0x4) to keep the steps gradual.
3:2	RW	0x0	dll_qtren Quarter flag of DLL, active in no-bypass mode. 2'b01: 1/4 fclk, dqs_dly=128. 2'b10: 1/8 fclk, dqs_dly=64. Default: dqs_dly=dll_dqs_dly(DLL_CTL_REG0[15:8]). When dll_qtr='b01 or 'b10, software not need to configure dll_dqs_dly, and hardware should delay the input signal for 1/4 or 1/8 fclk cycle time. When dll_qtr=0, software need to configure dll_dqs_dly.

Bit	Attr	Reset Value	Description
1	RW	0x1	dll_bypass DLL Bypass Control, 1active 1'b0: DLL not bypass, dll_dqs_dleay= dqs_dly 1'b1: DLL bypass, dll_dqs_dleay= dll_dqs_dly_bypass
0	RW	0x0	dll_start Start signal for DLL, 1 active. Notes: It will keep high until dll disabled.

NANDC_DLL_OBS_REG0

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:9	RO	0x01	dll_dqs_delay_value Report the delay value for the read DQS signal.
8:1	RO	0x00	dll_lock_value Reports the DLL encoder value from the master DLL to the slave DLL's. The slaves use this value to set up their delays for the clk_wr and read DQS signals.
0	RO	0x0	dll_lock DLL Lock indication 1'b0: DLL has not locked. 1'b1: DLL is locked.

NANDC_NANDC_VER

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x56393030	version Version indication for NANDC

NANDC_LLP_CTL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	llp_loc Starting address for LLI0, 64byte align.
5	RW	0x0	llp_frdy Working time for FOP_WAIT_FRDY for all FOP in first LLP group. 1'b0: FOP_WAIT_FRDY begin working when started. 1'b1: FOP_WAIT_FRDY not begin working until 16 cycles later after started.
4:3	RO	0x0	reserved
2	R/WSC	0x0	llp_rst Reset signal for LLP. When asserted, it will auto cleared.

Bit	Attr	Reset Value	Description
1	RW	0x0	llp_mode 1'b0: Current LLI only has FOP. 1'b1: Current LLI has both CFG and FOP.
0	RW	0x0	llp_en Enable signal for LLP 1'b0: LLP disable 1'b1: LLP enable

NANDC_LLP_STAT

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	llp_stat Latest LLI_LOC finished, 64byte align.
5:2	RO	0x0	reserved
1	RO	0x0	llp_err Error status for llp load or execute 1'b0: LLP is correct. 1'b1: LLP is error.
0	RO	0x1	llp_rdy Ready status for all llp load 1'b0: LLP load is busy. 1'b1: LLP load is ready.

NANDC_LLI_FOP7

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID

Bit	Attr	Reset Value	Description
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready; "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation. Indicate flash write data(command/address/data). Flash read with match operation. Indicate match pattern data.

NANDC_LLI_FOP8

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready; "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RW	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP9

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select; "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP10

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.

Bit	Attr	Reset Value	Description
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select; "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP11

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID

Bit	Attr	Reset Value	Description
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP12

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP13

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP14

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.

Bit	Attr	Reset Value	Description
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_NXT_LLP

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	loc Starting address for next LLI
5	RW	0x0	frdy Flash_rdy will not be used until 16 cycles after FOP_WAIT_FRDY start, "1" active.
4:2	RO	0x0	reserved
1	RO	0x0	llp_mode 1'b0: Next LLI only has FOP. 1'b1: Next LLI has both FOP and CFG.
0	RO	0x0	en Enable signal for next LLP.

NANDC_LLI_FOP0

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP1

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.

Bit	Attr	Reset Value	Description
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP2

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID

Bit	Attr	Reset Value	Description
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP3

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP4

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP5

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.

Bit	Attr	Reset Value	Description
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_LLI_FOP6

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Fop_type Flash operation type. 3'b000: Nop operation. 3'b001: Flash bypass write operation. 3'b010: Flash bypass read operation. 3'b011: Flash bypass read with match operation. 3'b100: Flash DMA write/read operation.
28	RO	0x0	Fop_matchmod When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. When FOP_MATCHMOD=0, it is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.
27:24	RO	0x0	Fop_cs Flash chip select, "1" active. 4'b1000~4'b1111: Indicate select cs0~cs7.
23:20	RO	0x0	Fop_nxtid Next FOP ID

Bit	Attr	Reset Value	Description
19	RO	0x0	Fop_wait_frdy Indicate the current FOP will excute when flash ready, "1" active.
18	RO	0x0	Fop_wait_trdy Indicate the current FOP will excute when DMA transfer ready, "1" active.
17:16	RO	0x0	Fop_addr Flash address type, FOP_ADDR[0]-ALE, FOP_ADDR[1]-CLE.
15:0	RO	0x0000	Fop_inst Flash write operation: Indicate flash write data(command/address/data). Flash read with match operation: Indicate match pattern data.

NANDC_INTEN

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	Seed_bcherr_int_en Enable for seed bch error interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When seed bcherr_int_en is active, an interrupt is generated.
8	RW	0x0	Seed_bchfail_int_en Enable for seed bch fail interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When seed bchfail_int_en is active, an interrupt is generated if seed bch decode failed.
7	RW	0x0	rd_1stpage_int_en Enable for the first page read interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When sif_bus_wr is active, an interrupt is generated if the first page read operation is finished.
6	RW	0x0	master_idle_int_en Enable for master idle interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When master_idle_int_en is active, an interrupt is generated if posedge of master idle happen.

Bit	Attr	Reset Value	Description
5	RW	0x0	flash_abort_int_en Enable for flash read abort interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When flash_abort_int_en is active, an interrupt is generated if DQS input is abort. Available when flash interface is ONFI synchronous or toggle. When read data number is out of range of flash page size, dqs input is abort. An interrupt is generated if flash_abort_int_en is enable.
4	RW	0x0	llp_int_en Enable for LLP finished interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When llp_en_en is active, an interrupt is generated if LLP operation is finished.
3	RW	0x0	bchfail_int_en Enable for bch fail interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When bchfail_int_en is active, an interrupt is generated if bch decode failed.
2	RW	0x0	bcherr_int_en Enable for bch error interrupt. 1'b0: Interrupt disable. 1'b1: interrupt enable. When bcherr_int_en is active, an interrupt is generated if bch decode error bit is larger than bchthres(BCHCTL[26:19]).
1	RW	0x0	frdy_int_en Enable for flash_rdy interrupt. 1'b0: Interrupt disable. 1'b1: Interrupt enable. When frdy_int_en is active, an interrupt is generated if flash R/B# changes from 0 to 1.
0	RW	0x0	dma_int_en Enable for internal DMA transfer finished interrupt. 1'b0: Interrupt disable. 1'b0: Interrupt enable. When dma_int_en is active, an interrupt is generated if page_num(FLCTL[27:22]) of flash data transfer in DMA mode is finished.

NANDC_INTCLR

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	R/WSC	0x0	Seed_bcherr_int_clr Clear for seed bch error interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
8	R/WSC	0x0	Seed_bchfail_int_clr Clear for seed bch decode fail interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
7	R/WSC	0x0	rd_1stpage_int_clr Clear for first page read interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
6	R/WSC	0x0	master_idle_int_clr Clear for master idle interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
5	R/WSC	0x0	flash_abort_int_clr Clear for flash abort interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt Available when flash interface is ONFI synchronous or toggle
4	R/WSC	0x0	llp_int_clr Clear for LLP finished interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
3	R/WSC	0x0	bchfail_int_clr Clear for bch decode fail interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
2	R/WSC	0x0	bcherr_int_clr Clear for bch error interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt

Bit	Attr	Reset Value	Description
1	R/WSC	0x0	frdy_int_clr Clear for flash_rdy interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt
0	R/WSC	0x0	dma_int_clr Clear for internal DMA transfer finished interrupt. When asserted, this bit will be auto cleared. 1'b0: Not clear interrupt 1'b1: Clear interrupt

NANDC_INTST

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	Seed_bcherr_int_stat Staus for seed bch decode error interrupt, high active.
8	RO	0x0	Seed_bchfail_int_stat Staus for seed bch decode fail interrupt, high active.
7	RO	0x0	rd_1stpage_int_stat Status for first page read interrupt, high active.
6	RO	0x0	master_idle_int_stat Status for master idle interrupt, high active.
5	RO	0x0	flash_abort_int_stat Status for flash abort, high active. Available when flash interface is ONFI synchronous or toggle.
4	RO	0x0	llp_int_stat Status for LLP finished interrupt, high active.
3	RO	0x0	bchfail_int_stat Status for bch decode fail interrupt, high active.
2	RO	0x0	bcherr_int_stat Status for bch error interrupt, high active.
1	RO	0x0	frdy_int_stat Status for flash_rdy interrupt, high active.
0	RO	0x0	dma_int_stat Status for internal DMA transfer finished interrupt, high active.

NANDC_BCHST0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31	RO	0x1	bchst_bchrdy Ready indication for bch encoder/decoder, 1 active. 1'b0: Bch encoder/decoder is busy. 1'b1: Bch encoder/decoder is ready.

Bit	Attr	Reset Value	Description
30	RC	0x0	decode_done_rdy Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
29:27	RO	0x0	reserved
26	RO	0x0	all_f_flag1 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum1 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail1 Indication for the 1st backup codeword decoded failed or not. 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done1 Indication for finishing decoding the 1st backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf1 Indication for error found in 1st backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag0 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum0 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail0 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done0 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf0 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST1

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	all_f_flag3 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum3 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail3 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done3 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf3 Indication for error found in 1st backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag2 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum2 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail2 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done2 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf2 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST2

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag5 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum5 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail5 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done5 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf5 Indication for error found in 1st backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag4 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum4 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail4 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done4 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf4 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST3

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag7 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum7 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail7 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done7 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf7 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag6 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum6 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail6 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done6 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf0 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST4

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag9 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum9 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail9 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done9 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf9 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag8 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum8 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail8 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done8 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf8 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST5

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag11 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum11 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail11 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done11 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf11 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag10 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum10 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail10 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done10 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf10 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST6

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag13 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum13 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail13 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done13 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf13 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag12 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum12 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail12 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done12 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf12 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST7

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag15 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum15 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail15 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done15 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf15 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag14 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum14 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail14 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done14 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf14 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST8

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag17 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum17 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail17 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done17 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf17 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag16 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum16 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail16 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done16 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf16 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST9

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag19 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum19 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail19 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done19 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf19 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag18 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum18 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail18 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done18 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf18 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST10

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag21 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum21 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail21 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done21 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf21 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag20 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum20 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail20 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done20 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf20 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST11

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag23 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum23 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail23 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done23 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf23 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag22 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum22 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail22 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done22 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf22 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST12

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag25 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum25 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail25 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done25 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf25 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag24 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum24 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail24 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done24 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf24 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST13

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag27 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum27 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail27 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done27 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf27 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag26 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum26 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail26 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done26 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf26 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST14

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag29 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum29 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail29 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done29 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf29 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag28 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum28 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail28 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done28 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf28 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_BCHST15

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26	RO	0x0	all_f_flag31 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
25:19	RO	0x00	err_tnum31 Indication for the number of error in current backup codeword.
18	RO	0x0	decode_fail31 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
17	RO	0x0	decode_done31 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
16	RO	0x0	errf31 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found
15:11	RO	0x00	reserved
10	RO	0x0	all_f_flag30 Indication for the all f byte in the current codeword. 1'b0: The current codeword is not all f. 1'b1: The current codeword is all f.
9:3	RO	0x00	err_tnum30 Indication for the number of error in current backup codeword.
2	RO	0x0	decode_fail30 Indication for current backup codeword decode failed or not 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	decode_done30 Indication for finishing decoding the current backup codeword. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	errf30 Indication for error found in current backup codeword. 1'b0: No error 1'b1: Error found

NANDC_SPARE0_0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 The 4th system byte of codeword 0.
23:16	RW	0xff	system_2 The 3rd system byte of codeword 0.

Bit	Attr	Reset Value	Description
15:8	RW	0xff	system_1 The 2nd system byte of codeword 0.
7:0	RW	0xff	system_0 The 1st system byte of codeword 0.

NANDC_SPARE1_0

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	system_3 The 4th system byte of codeword 1.
23:16	RW	0xff	system_2 The 3rd system byte of codeword 1.
15:8	RW	0xff	system_1 The 2nd system byte of codeword 1.
7:0	RW	0xff	system_0 The 1st system byte of codeword 1.

NANDC_RANDMZ_CFG

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RW	0x0	randmz_en Randomizer enable indication, 1 active. 1'b0: Randomizer not active. 1'b1: Randomizer active. Notes: a. Not active when data transmission in bypass mode. b. Just active for data, but not for address and command. c. Not active when BchPage=1.
30:29	RW	0x0	randmz_mode Randomizer mode 2'b00: Samsung randomizer Polynomial=1+x+x^15 2'b10: Samsung randomizer Polynomial=1+x^14+x^15
28:20	RO	0x000	reserved
19:0	RW	0x00000	randmz_seed When Samsung randomizer: The seed for randomizer(initial value). When Toshiba randomizer: Seed Agitation Register.

NANDC_SEED_BCHST

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	seed_bchst_rdy Indication for randmz seed bchst is ready or not. 1'b0: bchst is not ready. 1'b1: bchst is ready.
4:3	RW	0x0	seed_err_tnum Indication for the number of error in randmz seed.
2	RO	0x0	seed_decode_fail Indication for randmz seed decode failed or not. 1'b0: Decode successfully 1'b1: Decode fail
1	RO	0x0	seed_decode_done Indication for finishing decoding the randmz seed. 1'b0: Not finished 1'b1: Finished
0	RO	0x0	seed_errf Indication for error found in randmz seed. 1'b0: No error 1'b1: Error found

8.5 Interface Description

Table 8-1 NandC Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
flash_ale	O	FSPI_CLK/FLASH_ALE/GPIO1_D0_d	GRF_GPIO1D_IOMUX_L [2:0]=3'b010
flash_cle	O	EMMC_DATA_STROBE/FSPI_CS1n/FLASH_CLE/GPIO1_C6_d	GRF_GPIO1C_IOMUX_H [10:8]=3'b011
flash_wrn	O	EMMC_CMD/FLASH_WRn/GPIO1_C4_u	GRF_GPIO1C_IOMUX_H [2:0]=3'b010
flash_rdn	O	FSPI_D1/FLASH_RDn/GPIO1_D2_u	GRF_GPIO1D_IOMUX_L [10:8]=3'b010
flash_data[0]	I/O	EMMC_D0/FLASH_D0/GPIO1_B4_u	GRF_GPIO1B_IOMUX_H [2:0]=3'b010
flash_data[1]	I/O	EMMC_D1/FLASH_D1/GPIO1_B5_u	GRF_GPIO1B_IOMUX_H [6:4]=3'b010
flash_data[2]	I/O	EMMC_D2/FLASH_D2/GPIO1_B6_u	GRF_GPIO1B_IOMUX_H [10:8]=3'b010
flash_data[3]	I/O	EMMC_D3/FLASH_D3/GPIO1_B7_u	GRF_GPIO1B_IOMUX_H [14:12]=3'b010
flash_data[4]	I/O	EMMC_D4/FLASH_D4/GPIO1_C0_u	GRF_GPIO1C_IOMUX_L [2:0]=3'b010
flash_data[5]	I/O	EMMC_D5/FLASH_D5/GPIO1_C1_u	GRF_GPIO1C_IOMUX_L [6:4]=3'b010
flash_data[6]	I/O	EMMC_D6/FLASH_D6/GPIO1_C2_u	GRF_GPIO1C_IOMUX_L [10:8]=3'b010
flash_data[7]	I/O	EMMC_D7/FLASH_D7/GPIO1_C3_u	GRF_GPIO1C_IOMUX_L [14:12]=3'b010
flash_dqs	I/O	EMMC_CLKOUT/FLASH_DQS/GPIO1_C5_d	GRF_GPIO1C_IOMUX_H [6:4]=3'b010
flash_rdy	I	FSPI_D0/FLASH_RDY/GPIO1_D1_u	GRF_GPIO1D_IOMUX_L [6:4]=3'b010
flash_csn0	O	FSPI_CS0n/FLASH_CS0n/GPIO1_D3_u	GRF_GPIO1D_IOMUX_L [14:12]=3'b010
flash_csn1	O	FSPI_D3/FLASH_CS1n/GPIO1_D4_u	GRF_GPIO1D_IOMUX_H [2:0]=3'b010
flash_wp	O	EMMC_RSTn/FSPI_D2/FLASH_WPn/GPIO1_C7_d	GRF_GPIO1C_IOMUX_H [14:12]=3'b010

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

Table 8-2 NandC Interface Connection

Module Pin	Direction	Flash Interface		
		Asyn8x	ONFI	Toggle
flash_csni(i=0~1)	O	√	√	√
flash_ale	O	√	√	√
flash_cle	O	√	√	√
flash_wrn	O	√	√	√
flash_rdn	O	√	√	√
flash_data[7:0]	I/O	√	√	√
flash_dqs	I/O	-	√	√
flash_rdy	I	√	√	√

8.6 Application Notes

8.6.1 BCHST/SPARE Application

8.6.1.1 BCHST

There are 16 BCHST-registers in NandC to store 32 codeword's BCH decode status(bchst) information. Every register stores 2 codeword's bchst information except BCHST0, which not only includes bchst information, but also includes one bit for *bchrdy*.

Let bchst_cwd0~bchst_cwd31 be the bchst information for 32 codewords. NandC support bchst transfer function. Software can enable the function by FLCTL[19]. When FLCTL[19]=1, Nandc will transmit the status of BCH to external memory, and software need configure spare step to 8. Detailed format for spare data and BCH status in every unit is shown in figures1.3.

8.6.1.2 SPARE

SPARE includes two register-groups, SPARE0 and SPARE1. Each group has 1 register: SPARE0_0 and SPARE1_0.

When in bch encoding, SPARE0_0 stores system information for codeword in sram0; SPARE1_0 stores system information for codeword in sram1.

When in bch decoding, SPARE0_0 stores the spare data read from flash for codeword in sram0; SPARE1_0 stores the spare data read from flash for codeword in sram1.

8.6.2 Bus Mode Application

MTRANS_CFG[2] determines whether the data load/store between internal memory and external memory is through slave interface or master interface.

8.6.2.1 Slave Mode

When MTRANS_CFG[2]=0, slave is selected. i. e. , flash data load/store between internal memory and external memory is through slave interface by cpu or external DMA.

In this mode, software should store page data into internal memory and spare data into SPARE registers before starting flash program operation; and should load page data from internal memory and spare data from SPARE registers after finishing flash read operation.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are unused. The transfer codeword number is determined by FLCTL[6:5], and the maximum number is 2.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transfer is finished.

8.6.2.2 Master Mode

When MTRANS_CFG[2]=1, master is selected. i. e. , flash data load/store between internal memory and external memory is through master interface.

In this mode, software should initialize page data and spare data into external memory, and set their addresses in MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash program operation. Similarly, software should configure MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash read operation and could read data from addresses in MTRANS_SADDR0 and MTRANS_SADDR1 after NandC transfer finish.

In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are used. The transfer codeword number is determined by FLCTL[27:22], and the maximum number is 32.

The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transmission is finished.

When MTRANS_CFG[2]=1, page data and spare data are stored in the continuous space of external memory respectively.

For page data, source address is named Saddr0, specified in MTRANS_SADDR0. The space can be divided into many continuous units, and the unit size(named PUnit) is 1024 bytes or 512 bytes determined by FLCTL[21] and FLCTL[11]:

a. when FLCTL[11]=0, PUnit is always equal to 1024 bytes
b. when FLCTL[11]=1 and FLCTL[21]=0, PUnit is equal to 1024 bytes
c. when FLCTL[11]=1 and FLCTL[21]=1, PUnit is equal to 512 bytes

For spare data, source address is named Saddr1, specified in MTRANS_SADDR1. The space can be divided into many continuous units, and the unit size(named SUnit) is 4 bytes or 8 bytes determined by FLCTL[19]:

a. When FLCTL[19]=0 , SUnit is equal to 4 bytes
b. When FLCTL[19]=1 , SUnit is equal to 8 bytes

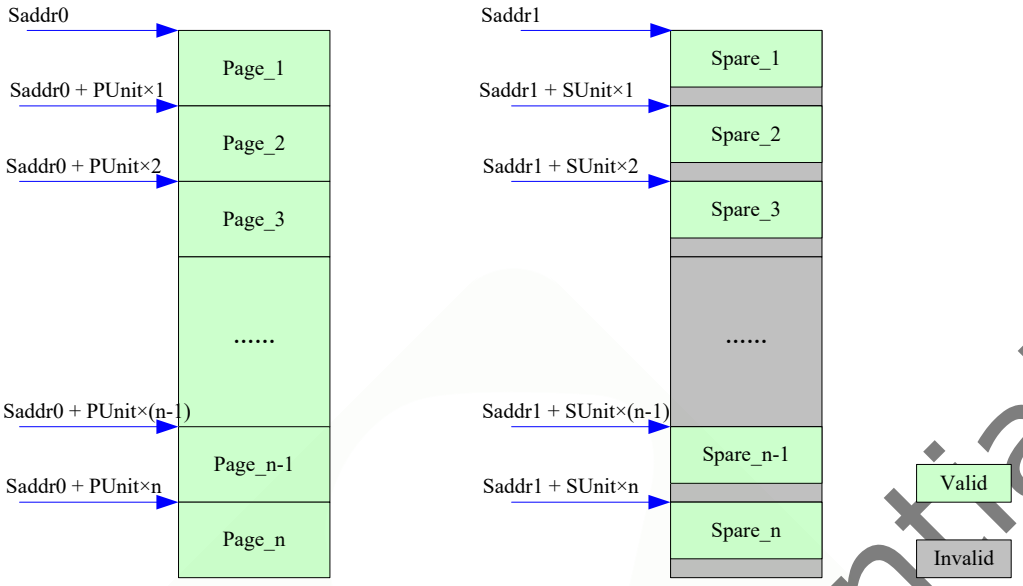


Fig.8-2 NandC Address Assignment

The detailed format for page data and spare data in every unit is shown in following figures.

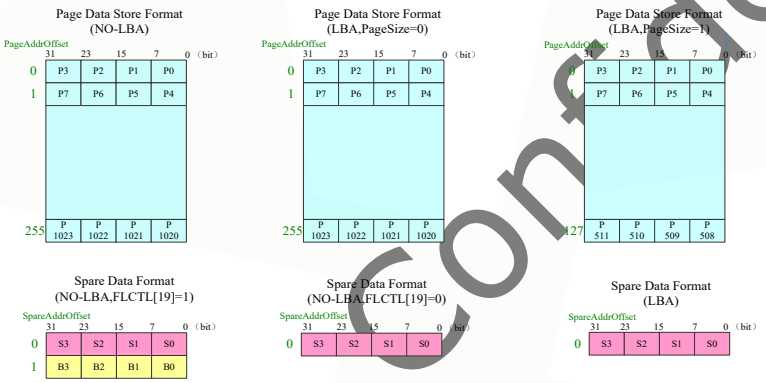


Fig.8-3 NandC Data Format

8.6.3 BchPage Application

BCHCTL[16] determines whether codeword size for page data is 1024 bytes or 512 bytes when FLCTL[11] is 0.

8.6.3.1 1024bytes

When BCHCTL[16]=0, BchPage=0, hardware needs to write 1024 bytes page data and spare data into flash or read 1024 bytes page data and spare data from flash. All the 1024 bytes page data and spare data are encoded when writing or decoded when reading.

8.6.3.2 512bytes

When BCHCTL[16]=1, BchPage=1, hardware needs to write 512 bytes page data and spare data into flash or read 512 bytes page data and spare data from flash.

In this mode, the page data unit size for BCH encoder and BCH decoder is still 1024byte. So to support BCH encoder and decoder, software should configure page data as follows:1th~512th bytes are invalid data which must be stuffed with 0xff, 513th~1024th bytes arevalid page data.

However, Randomizer function is not supported under this condition.

8.6.4 PageSize/SpareSize Application

FLCTL[21] determines whether the codeword size is 1024 bytes or 512 bytes when FLCTL[11] is 1.

8.6.4.1 Big Page

When FLCTL[11]=0(LbaEn=0), the flash to be operated is Raw NAND Flash. Every codeword size is 1024 bytes and FLCTL[21] should always be set to 0, and the PageStep in external memory is 1024 bytes if bus mode is master mode.

At this mode, the spare size and SpareStep in external memory are determined by

FLCTL[19] as follows:
FLCTL[19]=0: spare size=4bytes , SpareStep=4bytes
FLCTL[19]=1: spare size=4bytes , SpareStep=8bytes

8.6.4.2 Small Page

When FLCTL[11]=1, LbaEn=1, the flash to be operated is Managed NAND Flash. Every codeword size could be 1024 bytes or 512 bytes according to FLCTL[21]. If FLCTL[21]=0, codeword size is 1024 bytes, PageStep in external memory is 1024 bytes, and SpareStep is 4bytes. If FLCTL[21]=1, codeword size is 512 bytes, PageStep in external memory is 512 bytes, and SpareStep is 4 bytes.
At this mode, the spare size is configured in FLCTL[12], and the max available number is 4.
In the summary, the total data size in every codeword for flash or for software including page data and spare data, is determined by BCHCTL[27:25], FLCTL[11], FLCTL[21], BCHCTL[4]. Their relationship is shown as follows.

Table 8-3 NandC Page/Spare size for flash

Page/spare size for software		Page size/codeword	Spare size/codeword
FLCTL[11]=0	24bit ECC	1024 byte	(4+42)byte
	40 bit ECC	1024 byte	(4+70)byte
	60 bit ECC	1024 byte	(4+105)byte
	70 bit ECC	1024 byte	(4+123)byte
FLCTL[11]=1	FLCTL[21]=0	1024 byte	FLCTL[12]
	FLCTL[21]=1	512 byte	FLCTL[12]

Notes: that "page/spare size for flash" means that hardware should transfer these numbers of bytes in every codeword to or from flash.

8.6.5 Randomizer Application

RANDMZ_CFG[31] determines whether randomizer is enable or not. When RANDMZ_CFG[31] equals to 1, randomizer is active. Data should be scrambled before written into flash, and descrambled after read from flash.
RANDMZ_CFG[30] determines the randomizer polynomial.
When RANDMZ_CFG[30]=0, Polynomial=1+x+x^15
When RANDMZ_CFG[30]=1, Polynomial=1+x^14+x^15
RANDMZ_CFG[19:0] is the seed for randomizer. It should be ensured that data in the same page should have the same randomizer polynomial and randomizer seed when in flash program or flash read operation.
The data unit for randomizer is one codeword(data+spare).
However, Randomizer is just available for data transfer by internal DMA mode, but not by for bypass mode. Furthermore, it should not be enable if BCHCTL[16]=0 (BchPage=512bytes).

8.6.6 DLL Application

When Toggle Flash or ONFI Synchronous Flash interface is active, DLL should be used to adjust DQS input with DQ when reading flash.
There are 2 registers for DLL configuration(DLL_CFG_REG0 and DLL_CFG_REG1), and 1 register for DLL status(DLL_OBS_REG0).
The usage guide is as follows:
If bypass mode is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 1, and set *dll_dqs_dly_bypass* in DLL_CFG_REG0[23:16] to determine the dll element number needed. And then set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.
If auto adjusting is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 0, and set the *dll_start_point* in DLL_CFG_REG0[7:0] and *dll_incr* in DLL_CFG_REG1[11:4]. You also should set the adjusting mode *dll_qtren* in DLL_CFG_REG1[3:2] to compute the dll element number needed. If *dll_qtren*=2'b00, the dll element number is determined by *dll_dqs_dly* in DLL_CFG_REG0[15:8]; otherwise, it is 1/4 or 1/8 of the total number of dll elements used for *dll_qtren*=2'b01 or *dll_qtren*=2'b10 separately. The last step is to set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.
If you want to monitor the dll working status, you could read DLL_OBS_REG0. If DLL_OBS_REG0[0]=0, it means that DLL is not locked, and still in detecting status. Otherwise, it means that DLL is locked, and *dll_lock_value* in DLL_OBS_REG0[8:1] is the total number of dll elements used, *dll_dqs_delay_value* in DLL_OBS_REG0[16:9] is the total number of DQS delay used.

8.6.7 NandC Interrupt Application

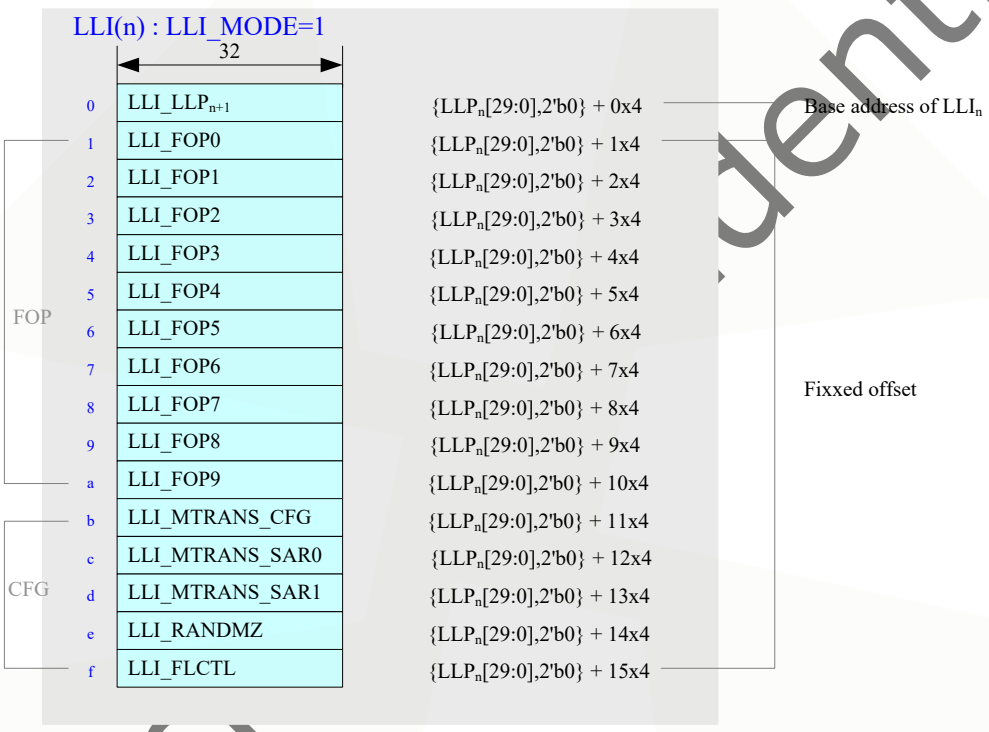
NandC has 1 interrupt output signal and 10 interrupt sources: seed bch error interrupt source, seed bch fail interrupt source, read first page interrupt source, master idle interrupt source, flash abort interrupt source, LLP interrupt source, dma finish interrupt source, flash ready interrupt source, bch error interrupt source, bchfail interrupt source. When one or more of these interrupt source are enabled, NandC interrupt is asserted if one or more interrupt source is high. Software can determine the interrupt source by reading INTST and clear interrupt by writing corresponding bit in INTCLR.

8.6.8 LLP Application

LLP is used in NandC to store and execute instruction groups configured in external memory by software. When LLPCTL[0]=1, LLP is active, NandC will load instruction groups stored in {LLPCTL[31:6], 6'h0} and execute them. Next instruction groups should not be loaded until current instruction execution finished.

8.6.8.1 LLP Structure

The structure of LLP is shown as follows:



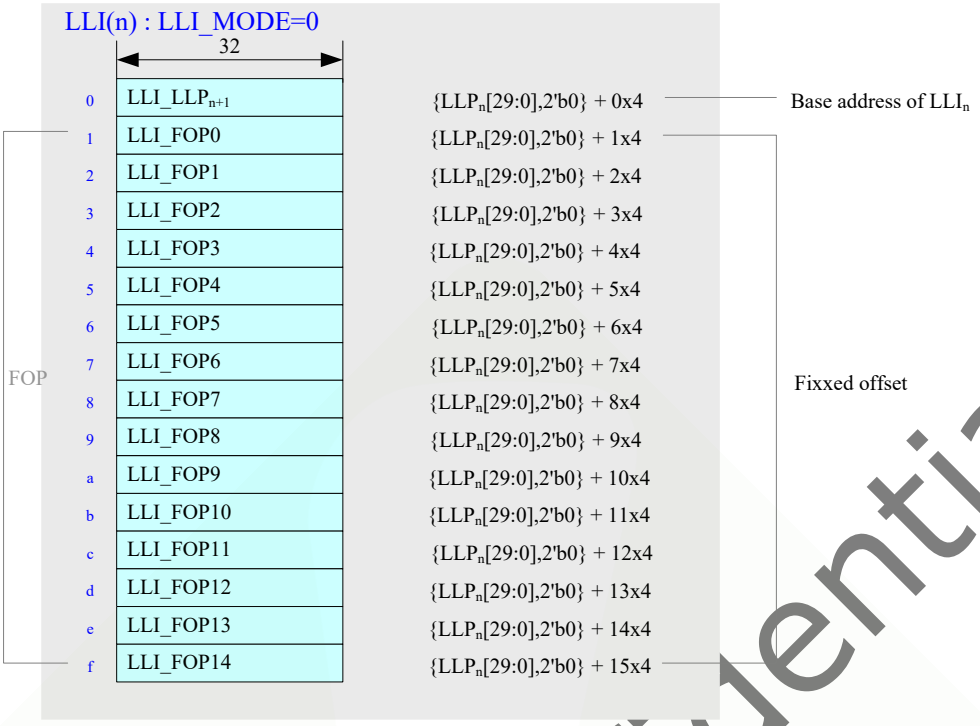


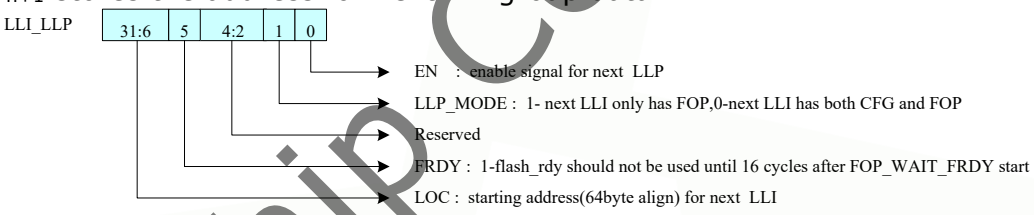
Fig.8-4 NandC LLP Data Format

LLI_MODE is determined by LLPCTL[1]. If current operation is flash program or flash read, then LLI_MODE=1 is need; otherwise, LLI_MODE=0 is workable.

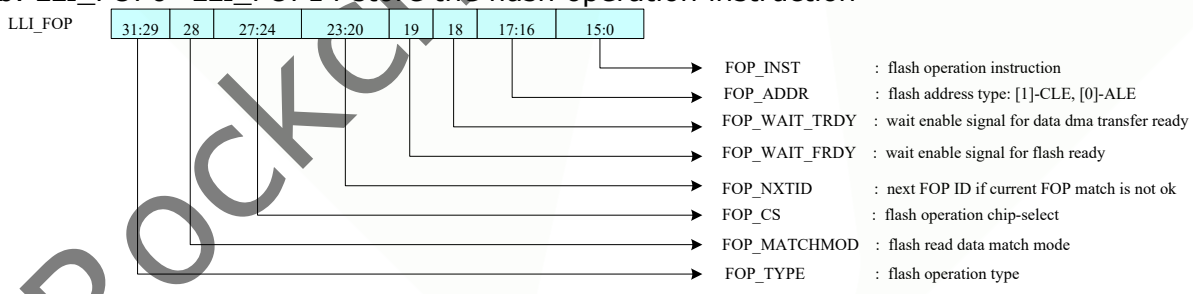
In addition, you could do more than one flash operation in one LLP group, but you should not separate one flash operation into two LLI groups.

8.6.8.2 LLI Format

a. LLI_LLP$_{n+1}$ stores the address for next LLI group data



b. LLI_FOP0~LLI_FOP14 store the flash operation instruction



FOP_TYPE:
000 : nop
001 : flash write
010 : flash read
011 : flash read with match operation
100 : DMA

When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. It is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.

c. LLI_MTRANS_CFG/LLI_MTRANS_SADDR0/LLI_MTRANS_SADDR1/ LLI_RANDMZ/ LLI_FLCTL store the configuration for MTRANS_CFG/ MTRANS_SADDR0/MTRANS_SADDR1/RANDMZ/FLCTL.

8.6.8.3 LLP Working Mode

There are two working modes for LLP:
a. Normal mode: LLPCTL[0] is kept to 1 until all LLP loading and executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].
b. Pause mode: LLPCTL[0] is changed from 1 to 0 during LLP loading or LLP executing. NandC should not stop working until current LLP executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

8.6.9 Seed Application

Nandc supports randomizer seed transmission. When FLCTL[9]=1 and RANDMZ_CFG[31]=1,Nandc will transmit seed to flash before page data transmission and receive seed before page data receiving.
Seed has BCH encoder/decoder separately and support 1bit BCH. Software can query seed BCH result by accessing SEED_BCHST.

8.6.10 Redundance Application

Nandc supports write "FF" to flash as redundance. Software can configure redundance size by NANDC_MTRANS_CFG[26:16].

8.6.11 IOMUX Application

Nandc support IOMUX. Software can change pin function by FMCTL[23:21].

Chapter 9 NPU

9.1 Overview

NPU is the process unit which is dedicated to neural network. It is designed to accelerate the neural network arithmetic in field of AI (artificial intelligence) such as machine vision and natural language processing. The variety of applications for AI is expanding, and currently provides functionality in a variety of areas, including face tracking as well as gesture and body tracking, image classification, video surveillance, automatic speech recognition (ASR) and advanced driver assistance systems (ADAS).

NPU supports the following features:

- AHB interface used for configuration only support single
- AXI interface used to fetch data from memory
- Support integer 8, integer 16, float 16,Bfloat 16 operation
- 512 integer 8 MAC operations per cycle
- 128 integer 16 MAC operations per cycle
- 128 float 16 MAC operations per cycle
- 128 bfloat 16 MAC operations per cycle
- 256KB internal buffer
- Inference Engine : TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

9.2 Block Diagram

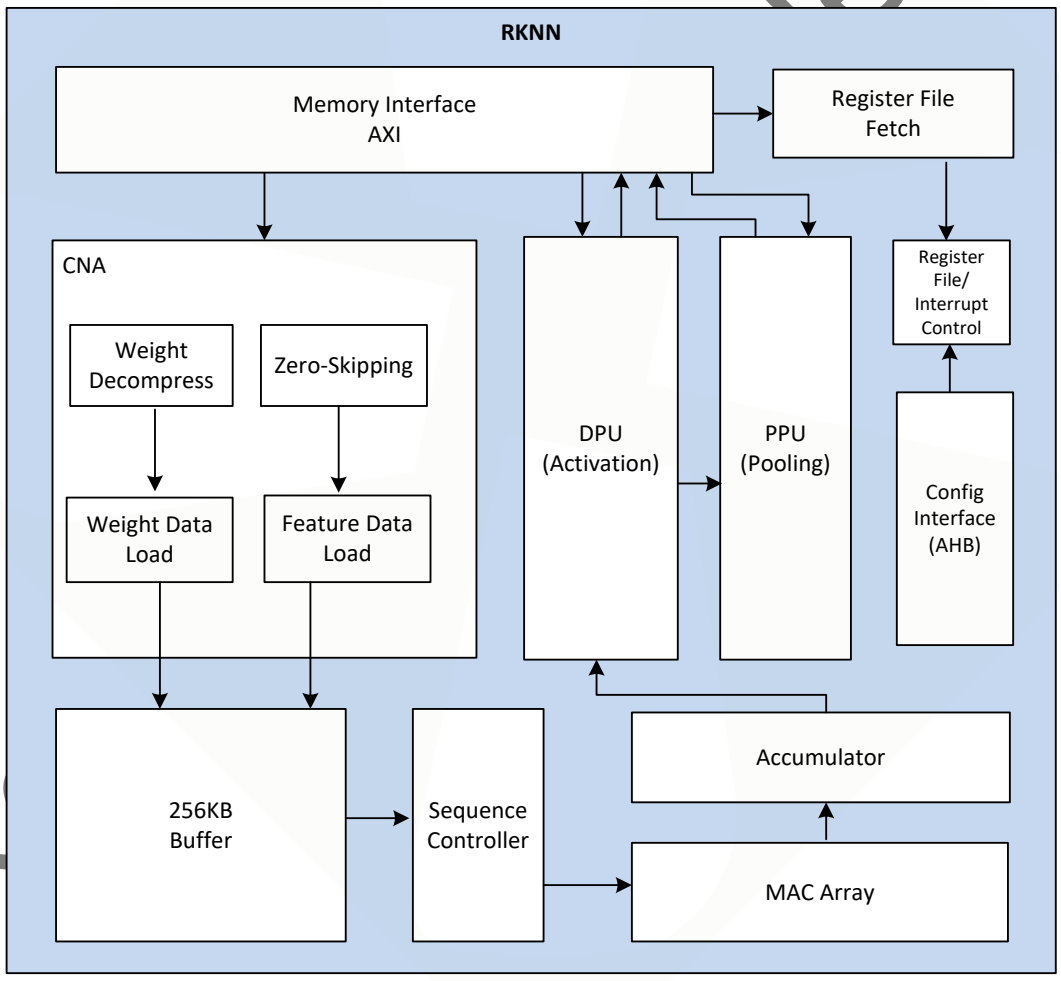


Fig. 9-1 NPU Architecture

9.3 Function Description

9.3.1 AHB/AXI Interface

The AXI master interface is used to fetch data from memory that is attached to the Soc AXI interconnect. The AHB slave interface is used to access the registers for configuration, debug and test.

9.3.2 Neural Network Accelerating Engine

As the unit name, this engine is the main process unit for Neural Network arithmetic. This unit include convolution pre-process controller, internal buffer, mac array, accumulator. It provides parallel convolution MAC for recognition functions and int8, int16, fp16 and bfloat16 are supported. It also provide function: softmax, transpose, data format conversion, …etc.

9.3.3 Dot Processing Unit

Dot Processing Unit mainly provide activate function followed by output data from accumulator cell, such as leaky_relu, relu, relux, sigmod, tanh… are supported.

9.3.4 Plane Processing Unit

Plane Processing Unit mainly provide pooling function followed by output data from dot processing unit, such as average pooling, max pooling, min pooling… are supported.

9.3.5 Register File Fetch Unit

Register File Fetch Unit fetch register configuration from external system memory through AXI
interface.

9.4 Register Description

9.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

9.4.2 PC Registers Summary

Name	Offset	Size	Reset Value	Description
PC_op_en	0x0008	W	0x00000000	Operator enable register
PC_addr	0x0010	W	0x00000000	PC source address register
PC_amount	0x0014	W	0x00000000	Amount of PC fetch data register
PC_interrupt_mask	0x0020	W	0x00000000	Interrupt mask register
PC_interrupt_clear	0x0024	W	0x00000000	Interrupt clear register
PC_interrupt_status	0x0028	W	0x00000000	Interrupt status register
PC_interrupt_raw_status	0x002C	W	0x00000000	Interrupt raw status register
PC_task_con	0x0030	W	0x00000000	Task control register
PC_task_dma_base_addr	0x0034	W	0x00000000	Task dma base address register
PC_task_status	0x003C	W	0x00000000	Task status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.3 PC Detail Registers Description

PC_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this bit 1, to trigger the pc to fetch register setting for each task.Pc_sel must set to 0 ,to enable this bit.

PC_addr

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	base_addr This is the address for dma instruction where it located.
2:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	pc_sel 0 : Pc mode, use axi dma to fetch register config, 1 : Slave mode, use ahb to set register.

PC_amount

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_amount The reigster number need to be fetched of one task. Each register takes 64bits, it is combined as following: bit[63:48] indicates which block the register forward to. bit[47:16] the register's value bit[15: 0] the register's offset address in each block. bit[56] =1 means this register is for pc block. bit[57] =1 cna bit[58] =1 cmac bit[59] =1 accu bit[60] =1 dpu bit[61] =1 dpu_rdma bit[62] =1 ppu bit[63] =1 ppu_rdma bit[55] =1 to set each block's op_en eg. 64'h0081_0000_007f_0008 will set each block's op_en(cna,cmac,...,ppu_rdma). note: op_en is strongly recommended set at the end of register list. before op_en, 64'h0041_xxxx_xxxx_xxxx must be set.

PC_interrupt_mask

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	int_mask mask[0] : Cna feature group 0 interrput mask. set 1 to enable interrupt. mask[1] : Cna feature group 1 mask[2] : Cna weight group 0 mask[3] : Cna weight group 1 mask[4] : Cna csc group 0 mask[5] : Cna csc group 1 mask[6] : Accu group 0 mask[7] : Accu group 1 mask[8] : Dpu group 0 mask[9] : Dpu group 1 mask[10] : Ppu group 0 mask[11] : Ppu group 1 mask[12] : Dma read error mask[13] : Dma write error note: In pc mode , int mask set the last one task's interrupt masking.

PC_interrupt_clear

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	W1C	0x0000	int_clr done_clr[0] : Cna feature group 0 interrupt clear done_clr[1] : Cna feature group 1 done_clr[2] : Cna weight group 0 done_clr[3] : Cna weight group 1 done_clr[4] : Cna csc group 0 done_clr[5] : Cna csc group 1 done_clr[6] : Accu group 0 done_clr[7] : Accu group 1 done_clr[8] : Dpu group 0 done_clr[9] : Dpu group 1 done_clr[10] : Ppu group 0 done_clr[11] : Ppu group 1 done_clr[12] : Dma read error done_clr[13] : Dma write error

PC_interrupt_status

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	int_st int_st[0] : Cna feature group 0 interrupt status, which and with mask bit int_st[1] : Cna feature group 1 int_st[2] : Cna weight group 0 int_st[3] : Cna weight group 1 int_st[4] : Cna csc group 0 int_st[5] : Cna csc group 1 int_st[6] : Accu group 0 int_st[7] : Accu group 1 int_st[8] : Dpu group 0 int_st[9] : Dpu group 1 int_st[10] : Ppu group 0 int_st[11] : Ppu group 1 int_st[12] : Dma read error int_st[13] : Dma write error

PC_interrupt_raw_status

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	W1C	0x0000	int_raw_st int_st[0] : Cna feature group 0 interrupt raw status int_st[1] : Cna feature group 1 int_st[2] : Cna weight group 0 int_st[3] : Cna weight group 1 int_st[4] : Cna csc group 0 int_st[5] : Cna csc group 1 int_st[6] : Accu group 0 int_st[7] : Accu group 1 int_st[8] : Dpu group 0 int_st[9] : Dpu group 1 int_st[10] : Ppu group 0 int_st[11] : Ppu group 1 int_st[12] : Dma read error int_st[13] : Dma write error

PC_task_con

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	W1C	0x0	task_last_layer_clear 1: Clear the task last layer signal to 0. Before task started , it is suggestted to clear.
13	W1C	0x0	task_count_clear Clear the counter that counting current task. Before task started , it is suggestted to clear.
12	RW	0x0	task_pp_off 1 : Tasks' register are fetched in ping-pong mode The second group register setting is fetched immedidately after first group's register fetching is finished. 0 : Ping-pong mode off The second group register setting is fetched after first group task operation is finished.
11:0	RW	0x000	task_number Set the total task number to be exected.

PC_task_dma_base_addr

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_base_addr This is for each dma's base addr. For feature dma, weight dma, dpu dma, ppu dma, the address is set as offset address. Final address appear on axi bus is base_addr+offset_address.

PC_task_status

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	task_status [11:0] : Current task counter value, [12] : Indicate the first task is operating, [13] : Indicate the last task is operating, [12] : Indicate the first task's register is fetching, [13] : Indicate the last task's register is fetching.

9.4.4 CNA Registers Summary

Name	Offset	Size	Reset Value	Description
CNA_s_status	0x0000	W	0x00000000	Statue register
CNA_s_pointer	0x0004	W	0x00000000	Single Pointer Register
CNA_op_en	0x0008	W	0x00000000	Operator enable register
CNA_conv_con1	0x000C	W	0x00000000	Convolution control register 1
CNA_conv_con2	0x0010	W	0x00000000	Convolution control register 2
CNA_conv_con3	0x0014	W	0x00000000	Convolution control register 3
CNA_conv_con4	0x0018	W	0x00000000	Convolution control register 4
CNA_data_size0	0x0020	W	0x00000000	Feature size register 0
CNA_data_size1	0x0024	W	0x00000000	Feature size register 1
CNA_data_size2	0x0028	W	0x00000000	Feature size register 2
CNA_data_size3	0x002C	W	0x00000000	Feature size register 3
CNA_weight_size0	0x0030	W	0x00000000	Weight size register 0
CNA_weight_size1	0x0034	W	0x00000000	Weight size register 1
CNA_weight_size2	0x0038	W	0x00000000	Weight size register 2
CNA_cbuf_con0	0x0040	W	0x00000000	Cbuf control register 0
CNA_cbuf_con1	0x0044	W	0x00000000	Cbuf control register 0
CNA_cvt_con0	0x004C	W	0x00000000	Convert control register 0
CNA_cvt_con1	0x0050	W	0x00000000	Convert control register 1
CNA_cvt_con2	0x0054	W	0x00000000	Convert control register 2
CNA_cvt_con3	0x0058	W	0x00000000	Convert control register 3
CNA_cvt_con4	0x005C	W	0x00000000	Convert control register 4
CNA_fc_con0	0x0060	W	0x00000000	Full connected control register 0
CNA_fc_con1	0x0064	W	0x00000000	Full connected control register 1
CNA_pad_con0	0x0068	W	0x00000000	Convolution pad control register
CNA_feature_data_addr	0x0070	W	0x00000000	Feature data source address
CNA_fc_con2	0x0074	W	0x00000000	Full connected control register 2
CNA_dma_con0	0x0078	W	0x00000000	DMA control register 0
CNA_dma_con1	0x007C	W	0x00000000	DMA control register 1
CNA_dma_con2	0x0080	W	0x00000000	DMA control register 2
CNA_fc_data_size0	0x0084	W	0x00000000	Full connected feature size control register 0
CNA_fc_data_size1	0x0088	W	0x00000000	Full connected feature size control register 1
CNA_clk_gate	0x0090	W	0x00000000	Clock gating register
CNA_dcomp_ctrl	0x0100	W	0x00000000	Decompress control register
CNA_dcomp_regnum	0x0104	W	0x00000000	Decompress register numbers register
CNA_dcomp_addr0	0x0110	W	0x00000000	Weight decompress source address 0 register
CNA_dcomp_addr1	0x0114	W	0x00000000	Weight decompress source address 1 register
CNA_dcomp_addr2	0x0118	W	0x00000000	Weight decompress source address 2 register
CNA_dcomp_addr3	0x011C	W	0x00000000	Weight decompress source address 3 register
CNA_dcomp_addr4	0x0120	W	0x00000000	Weight decompress source address 4 register
CNA_dcomp_addr5	0x0124	W	0x00000000	Weight decompress source address 5 register

Name	Offset	Size	Reset Value	Description
CNA_dcomp_addr6	0x0128	W	0x00000000	Weight decompress source address 6 register
CNA_dcomp_addr7	0x012C	W	0x00000000	Weight decompress source address 7 register
CNA_dcomp_amount4	0x0130	W	0x00000000	Weight decompress source data amount 4 register
CNA_dcomp_amount5	0x0134	W	0x00000000	Weight decompress source data amount 5 register
CNA_dcomp_amount6	0x0138	W	0x00000000	Weight decompress source data amount 6 register
CNA_dcomp_amount7	0x013C	W	0x00000000	Weight decompress source data amount 7 register
CNA_dcomp_amount0	0x0140	W	0x00000000	Weight decompress source data amount 0 register
CNA_dcomp_amount1	0x0144	W	0x00000000	Weight decompress source data amount 1 register
CNA_dcomp_amount2	0x0148	W	0x00000000	Weight decompress source data amount 2 register
CNA_dcomp_amount3	0x014C	W	0x00000000	Weight decompress source data amount 3 register
CNA_CBUF_DBG_CON	0x0210	W	0x00000000	Debug control register
CNA_CBUF_DBG_STA0	0x0214	W	0x00000000	Cbuf debug status register 0
CNA_CBUF_DBG_STA1	0x0218	W	0x00000000	Cbuf debug status register 1
CNA_CBUF_DBG_STA2	0x021C	W	0x00000000	Cbuf debug status register 2
CNA_CBUF_DBG_STA3	0x0220	W	0x00000000	Cbuf debug status register 3
CNA_CBUF_DBG_STA4	0x0224	W	0x00000000	Cbuf debug status register 4
CNA_CBUF_DBG_STA5	0x0228	W	0x00000000	Cbuf debug status register 5
CNA_CBUF_DBG_STA6	0x022C	W	0x00000000	Cbuf debug status register 6
CNA_CBUF_DBG_STA7	0x0230	W	0x00000000	Cbuf debug status register 7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.5 CNA Detail Registers Description

CNA_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

CNA_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

CNA_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

CNA_conv_con1

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	de_conv Enable deconvolution function 1'h0 : Disable 1'h1 : Enable
15:12	RW	0x0	argb_in 4'h8: 1 channel input mode, 4'ha: 3 channel input mode, 4'hb: 4 channel input mode.
11:10	RO	0x0	reserved
9:8	RW	0x0	proc_precision Process precision 2'h0 : Input precision is int 8 2'h1 : Input data precision is int 16 2'h2 : Input data precision is float 16 2'h3 : reserved
7:6	RO	0x0	reserved
5:4	RW	0x0	in_precision Input precision 2'h0 : Input precision is int 8 2'h1 : Input data precision is int 16 2'h2 : Input data precision is float 16 2'h3 : reserved
3:0	RW	0x0	conv_mode Convolution mode: 4'h0: Direct convolution, 4'h3: Depthwise convolution.

CNA_conv_con2

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	kernel_group In int8, 32 kernels form 1 group , in int16 or fp16, 16 kernels form 1 group. Eg, weight kernel is 256, in int8, you can set this register to be 256/32 -1 = 15.
15:14	RO	0x0	reserved
13:4	RW	0x000	feature_grains Feature data rows needs to be buffered before convolution start. It's suggested to set this field as y_stride+weight_height+1.
3:0	RO	0x0	reserved

CNA_conv_con3

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:21	RW	0x00	atrous_y_dilation Pad numbers inserted in feature map column between 2 pixels.
20:16	RW	0x00	atrous_x_dilation Pad numbers inserted in feature map row between 2 pixels. Set this register value >0 will enable atrous convolution.
15:14	RO	0x0	reserved
13:11	RW	0x0	deconv_y_stride Pad numbers inserted in feature map column between 2 pixels.
10:8	RW	0x0	deconv_x_stride Pad numbers inserted in feature map row between 2 pixels.
7:6	RO	0x0	reserved
5:3	RW	0x0	conv_y_stride Stride value in y direction.
2:0	RW	0x0	conv_x_stride Stride value in x direction.

CNA_conv_con4

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	rgb_bytelength Byte length of argb feature map.

CNA_data_size0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	datain_width Input feature data width.
15:11	RO	0x00	reserved
10:0	RW	0x000	datain_height Input feature data height.

CNA_data_size1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	dat_channel_true If the input channel is not integer times of 8(int8) or 4(int 16/float 16), set the real channel number in this field.
15:0	RW	0x0000	datain_channel Input feature data channel number. Int 8 mode, this number should be integer times of 8. Int 16/float 16 mode, should be integer times of 4.

CNA_data_size2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dataout_width Data width after convolution.
15:0	RO	0x0000	reserved

CNA_data_size3

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	dataout_automics Data automics after convolution which is data out total pixels number.

CNA_weight_size0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	weight_bytes Weight bytes in total for this convlution.

CNA_weight_size1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	weight_bytes_per_kernel Weight bytes for one kernel group.

CNA_weight_size2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	weight_width Kernel width.
23:21	RO	0x0	reserved
20:16	RW	0x00	weight_height Kernel height.
15:14	RO	0x0	reserved
13:0	RW	0x0000	weight_kernels Weight kernels.

CNA_cbuf_con0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	weight_reuse Weight data reuse enable. 1'b0 : disable , 1'b1 : enable data reuse. fetching weight directly from internal buffer.
12	RW	0x0	data_reuse Feature data reuse enable 1'b0 : disable , 1'b1 : enable data reuse. fetching data directly from internal buffer.
11	RO	0x0	reserved
10:8	RW	0x0	data_bank2 Bank numbers for fc zero-skipping feature data. In FC zero-skipping mode, set to be 1, Otherwise, must set to be 0.
7	RO	0x0	reserved
6:4	RW	0x0	weight_bank Bank numbers for weight data. 3'h1 : Bank 7 occupied by weight data, 3'h2 : Bank 6/7 occupied by weight data, ... 3'h7 : Bank 1-7 occupied by weight data.
3	RO	0x0	reserved
2:0	RW	0x0	data_bank Bank numbers for feature data 3'h0 : Bank 0 occupied by feature data, 3'h1 : Bank 0 and bank 1 occupied by feature data, 3'h2 : Bank 0/1/2 occupied by feature data, ... 3'h6 : Bank 0-6 occupied by feature data.

CNA_cbuf_con1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	entries_per4surf Entries per 4 surface. How many bank space needed to stor 4 surface feature map row. actually, it equals to datain_width.
15:13	RO	0x0	reserved
12:0	RW	0x0000	data_entries How many bank space needed to store one feature map row.

CNA_cvt_con0

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:22	RW	0x00	cvt_truncate_3 Cvt truncate value 3.
21:16	RW	0x00	cvt_truncate_2 Cvt truncate value 2.
15:10	RW	0x00	cvt_truncate_1 Cvt truncate value 1.
9:4	RW	0x00	cvt_truncate_0 Cvt truncate value 0.

Bit	Attr	Reset Value	Description
3	RW	0x0	data_sign Feature data is signed or unsigned. 1'b0 : unsigned, 1'b1 : signed.
2	RW	0x0	round_type 0 : odd in , even not, 1 : round-up 0.5 to 1.
1	RW	0x0	cvt_type 1: cvt function will do add first, then multiply, 0: multiply first, then add.
0	RW	0x0	cvt_en Enable cvt function. 1'b0 : diable, 1'b1 : enable cvt function.

CNA_cvt_con1

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale1 Multiplier operand for 1st layer .
15:0	RW	0x0000	cvt_offset1 Adder operand for 1st layer .

CNA_cvt_con2

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale2 Multiplier operand for 2nd layer.
15:0	RW	0x0000	cvt_offset2 Adder operand for 2nd layer.

CNA_cvt_con3

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale3 Multiplier operand for 3rd layer.
15:0	RW	0x0000	cvt_offset3 Adder operand for 3rd layer.

CNA_cvt_con4

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale4 Multiplier operand for 4th layer.
15:0	RW	0x0000	cvt_offset4 Adder operand for 4th layer.

CNA_fc_con0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	fc_skip_data FC zero skipping data. Skipped feature data value, normally set to 0.
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	fc_skip_enable FC zero skipping enable. 1'b0 : disable, 1'b1: enable skip some feature data value, normally skip zero. When one pixel feature data is 0, the corresponding weight data is not fetched from system memory.

CNA_fc_con1

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	dat_offset Feature data offset in fc skip mode.

CNA_pad_con0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	pad_value Pad value.
15:8	RO	0x00	reserved
7:4	RW	0x0	pad_left Pad numbers in left of the feature map.
3:0	RW	0x0	pad_top Pad numbers in top of the feature map.

CNA_feature_data_addr

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	feature_base_addr Read feature data address.
2:0	RO	0x0	reserved

CNA_fc_con2

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	wt_offset Weight offset in fc skip mode.

CNA_dma_con0

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	wt_burst_len Read weight data axi burst len.
15:8	RW	0x00	fetch_pixel_len Length of feature data for each surface.
7:4	RO	0x0	reserved
3:0	RW	0x0	dat_burst_len Read feature data axi burst len.

CNA_dma_con1

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	line_stride Feature map actual width.

CNA_dma_con2

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	surf_stride Feature map actual surface areo.

CNA_fc_data_size0

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	datain_width_dma Width of feature map for fc mode.
15:11	RO	0x00	reserved
10:0	RW	0x000	datain_height_dma Height of feature map for fc mode.

CNA_fc_data_size1

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	datain_channel_dma Channel of feature map for fc mode.

CNA_clk_gate

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sbuf_cs_disable_clkgate 1: Disable sbuf clock auto gate, 0: Auto clock gate is enabled.
4	RW	0x0	cbuf_cs_disable_clkgate 1: Disable cbuf clock auto gate, 0: Auto clock gate is enabled.
3	RO	0x0	reserved
2	RW	0x0	csc_disable_clkgate 1 : Disable csc block clk gate, 0 : Auto clock gate is enabled.
1	RW	0x0	cna_wt_disable_clkgate 1 : Disable weight block clk gate, 0 : Auto clock gate is enabled.
0	RW	0x0	cna_feature_disable_clkgate 1 : Disable feature block clk gate, 0 : Auto clock gate is enabled.

CNA_dcomp_ctrl

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	decomp_control 3'h0 : Disable weight decompress, 3'h1 : Enable weight decompress.

CNA_dcomp_regnum

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	dcomp_regnum Decompress register numbers register.

CNA_dcomp_addr0

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr0 Weight decompress source address 0.
2:0	RO	0x0	reserved

CNA_dcomp_addr1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr1 Weight decompress source address 1.
2:0	RO	0x0	reserved

CNA_dcomp_addr2

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr2 Weight decompress source address 2.
2:0	RO	0x0	reserved

CNA_dcomp_addr3

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr3 Weight decompress source address 3.
2:0	RO	0x0	reserved

CNA_dcomp_addr4

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr4 Weight decompress source address 4.
2:0	RO	0x0	reserved

CNA_dcomp_addr5

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr5 Weight decompress source address 5.
2:0	RO	0x0	reserved

CNA_dcomp_addr6

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr6 Weight decompress source address 6.
2:0	RO	0x0	reserved

CNA_dcomp_addr7

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	decompress_addr7 Weight decompress source address 7.
2:0	RO	0x0	reserved

CNA_dcomp_amount4

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount4 Weight decompress source data amount 4.

CNA_dcomp_amount5

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount5 Weight decompress source data amount 5.

CNA_dcomp_amount6

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount6 Weight decompress source data amount 6.

CNA_dcomp_amount7

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount7 Weight decompress source data amount 7.

CNA_dcomp_amount0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount0 Weight decompress source data amount 0.

CNA_dcomp_amount1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount1 Weight decompress source data amount 1.

CNA_dcomp_amount2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount2 Weight decompress source data amount 2.

CNA_dcomp_amount3

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount3 Weight decompress source data amount 3.

CNA_CBUF_DBG_CON

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	reg2dp_dbg_cbuf_rdsel Reg2dp_dbg_cbuf_rdsel.
12:0	RW	0x0000	reg2dp_dbg_cbuf_raddr Reg2dp_dbg_cbuf_raddr.

CNA_CBUF_DBG_STA0

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data0 Cbuf_debug_data0.

CNA_CBUF_DBG_STA1

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data1 Cbuf_debug_data1.

CNA_CBUF_DBG_STA2

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data2 Cbuf_debug_data2.

CNA_CBUF_DBG_STA3

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data3 Cbuf_debug_data3.

CNA_CBUF_DBG_STA4

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data4 Cbuf_debug_data4.

CNA_CBUF_DBG_STA5

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data5 Cbuf_debug_data5.

CNA_CBUF_DBG_STA6

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data6 Cbuf_debug_data6.

CNA_CBUF_DBG_STA7

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_debug_data7 Cbuf_debug_data7.

9.4.6 CMAC Registers Summary

Name	Offset	Size	Reset Value	Description
CMAC_s_status	0x0000	W	0x00000000	Statue register
CMAC_s_pointer	0x0004	W	0x00000000	Single Pointer Register
CMAC_op_en	0x0008	W	0x00000000	Operator enable register
CMAC_misc ctrl	0x000C	W	0x00000000	CMAC misc control register
CMAC_gat_ctrl	0x0010	W	0x00000000	Clock gating control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.7 CMAC Detail Registers Description

CMAC_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

CMAC_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.

Bit	Attr	Reset Value	Description
0	RW	0x0	pointer Which register group ready to be setted.

CMAC_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

CMAC_misc ctrl

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	proc_precision Process precision. 2'h0 : Int8, 2'h1 : Int16, 2'h2 : Fp16, 2'h3 : Bf16.
11:2	RO	0x000	reserved
1	RW	0x0	dw_en If enable depthwise convolution.
0	RW	0x0	reg_qd_en Enable calculate feature data summury.

CMAC_gat_ctrl

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	slcg_op_en Gating enable signal.

9.4.8 ACCU Registers Summary

Name	Offset	Size	Reset Value	Description
ACCU_s_status	0x0000	W	0x00000000	Statue register
ACCU_s_pointer	0x0004	W	0x00000000	Single Pointer Register
ACCU_op_en	0x0008	W	0x00000000	Operator enable register
ACCU_misc_cfg	0x000C	W	0x00000000	ACCU misc control register
ACCU_dataout_size_0	0x0010	W	0x00000000	Dataout size register 0
ACCU_dataout_size_1	0x0014	W	0x00000000	Dataout size register 1
ACCU_clip_truncate	0x002C	W	0x00000000	Truncate register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.9 ACCU Detail Registers Description

ACCU_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

ACCU_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

ACCU_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

ACCU_misc_cfg

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:14	RW	0x00	soft_gating Soft_gating.
13:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	proc_precision Process precision. 2'h0 : Int8, 2'h1 : Int16, 2'h2 : Fp16, 2'h3 : Bf16.
7:2	RO	0x00	reserved
1	RW	0x0	dw_en If enable depthwise convolution.
0	RW	0x0	reg_qd_en Enable calculate feature data summury.

ACCU_dataout_size_0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dataout_height Output height of feature data.
15:0	RW	0x0000	dataout_width Output width of feature data.

ACCU_dataout_size_1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dataout_channel Output channel of feature data.

ACCU_clip_truncate

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	cvt_round Truncate type.
4:0	RW	0x00	clip_truncate Truncate value.

9.4.10 DPU Registers Summary

Name	Offset	Size	Reset Value	Description
DPU_s_status	0x0000	W	0x00000000	Statue register
DPU_s_pointer	0x0004	W	0x00000000	Single Pointer Register
DPU_op_en	0x0008	W	0x00000000	Operator enable register
DPU_feature_mode_cfg	0x000C	W	0x00000000	Feature mode configuration register
DPU_data_format	0x0010	W	0x00000000	Data format control register
DPU_offset_pend	0x0014	W	0x00000000	Offset pend register
DPU_dst_base_addr	0x0020	W	0x00000000	Destination address register
DPU_dst_surface_stride	0x0024	W	0x00000000	Destination surface stride register
DPU_data_cube_width	0x0030	W	0x00000000	Feature width register
DPU_data_cube_height	0x0034	W	0x00000000	Feature height register
DPU_data_cube_notch_addr	0x0038	W	0x00000000	Feature notch address register
DPU_data_cube_channel	0x003C	W	0x00000000	Feature channel register

Name	Offset	Size	Reset Value	Description
DPU_bs_cfg	0x0040	W	0x00000000	BS control register
DPU_bs_alu_cfg	0x0044	W	0x00000000	BS ALU control register
DPU_bs_mul_cfg	0x0048	W	0x00000000	BS MUL control register
DPU_bs_relux_cmp_value	0x004C	W	0x00000000	BS RELUX compare data register
DPU_bs_ow_cfg	0x0050	W	0x00000000	BS offset of weight control register
DPU_bs_ow_op	0x0054	W	0x00000000	BS offset of weight register
DPU_bn_cfg	0x0060	W	0x00000000	BN control register
DPU_bn_alu_cfg	0x0064	W	0x00000000	BN ALU control register
DPU_bn_mul_cfg	0x0068	W	0x00000000	BN MUL control register
DPU_bn_relux_cmp_value	0x006C	W	0x00000000	BN RELUX compare data register
DPU_ew_cfg	0x0070	W	0x00000000	EW control register
DPU_ew_op_cvt_offset_value	0x0074	W	0x00000000	Convert offset in EW
DPU_ew_op_cvt_scale_value	0x0078	W	0x00000000	Convert scale in EW
DPU_ew_relux_cmp_value	0x007C	W	0x00000000	EW RELUX compare data register
DPU_out_cvt_offset	0x0080	W	0x00000000	Out convert offset register
DPU_out_cvt_scale	0x0084	W	0x00000000	Out scale offset register
DPU_out_cvt_shift	0x0088	W	0x00000000	Out shift offset register
DPU_ew_op_src_value_0	0x0090	W	0x00000000	Configuration value for ew operator 0
DPU_ew_op_src_value_1	0x0094	W	0x00000000	Configuration value for ew operator 1
DPU_ew_op_src_value_2	0x0098	W	0x00000000	Configuration value for ew operator 2
DPU_ew_op_src_value_3	0x009C	W	0x00000000	Configuration value for ew operator 3
DPU_ew_op_src_value_4	0x00A0	W	0x00000000	Configuration value for ew operator 4
DPU_ew_op_src_value_5	0x00A4	W	0x00000000	Configuration value for ew operator 5
DPU_ew_op_src_value_6	0x00A8	W	0x00000000	Configuration value for ew operator 6
DPU_ew_op_src_value_7	0x00AC	W	0x00000000	Configuration value for ew operator 7
DPU_lut_access_cfg	0x0100	W	0x00000000	LUT access configuration register
DPU_lut_access_data	0x0104	W	0x00000000	LUT access data register
DPU_lut_cfg	0x0108	W	0x00000000	LUT configuration register
DPU_lut_info	0x010C	W	0x00000000	LUT info register
DPU_lut_le_start	0x0110	W	0x00000000	LE LUT start address register
DPU_lut_le_end	0x0114	W	0x00000000	LE LUT end address register
DPU_lut_lo_start	0x0118	W	0x00000000	LO LUT start address register
DPU_lut_lo_end	0x011C	W	0x00000000	LO LUT end address register
DPU_lut_le_slope_scale	0x0120	W	0x00000000	LE LUT slope scale register
DPU_lut_le_slope_shift	0x0124	W	0x00000000	LE LUT slope offset register
DPU_lut_lo_slope_scale	0x0128	W	0x00000000	LO LUT slope scale register
DPU_lut_lo_slope_shift	0x012C	W	0x00000000	LO LUT slope offset register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.11 DPU Detail Registers Description

DPU_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

DPU_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

DPU_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

DPU_feature_mode_cfg

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	tp_en If enable transpose .

Bit	Attr	Reset Value	Description
29:26	RW	0x0	rgp_type Regroup type. 4'h0: Cut all input (64bit), 4'h1: Cut 8bit, 4'h2: Cut 16bit, 4'h3: Cut 32bit.
25	RW	0x0	nonalign If nonalign mode is enable.If the output data flow is sampe with the input data flow, this mode can be used.
24:9	RW	0x0000	surf_len In nonalign mode, how many 8bytes to be stored.
8:7	RW	0x0	burst_len Burst length, 0:burst4, 1:burst8, 2:burst16.
6	RO	0x0	reserved
5:4	RW	0x0	conv_mode 0: Direct convolution mode, 3: Depthwise convlution mode.
3:1	RW	0x0	output_mode Where the dpu core output goes. 0: If the output goes to ppu, high is active, 2: If the output goes to outside, high is active.
0	RW	0x0	flying_mode If flying mode is enable.

DPU_data_format

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	out_precision Output precision. 3'h0 : Int8, 3'h1 : Int16, 3'h2 : Fp16, 3'h3 : Bf16, 3'h4 : Int32, 3'h5 : Fp32.
28:26	RW	0x0	in_precision Input precision same with dpu_rdma. 3'h0 : Int8, 3'h1 : Int16, 3'h2 : Fp16, 3'h3 : Bf16, 3'h4 : Int32, 3'h5 : Fp32.
25:16	RW	0x000	ew_truncate_neg Shift value in ew core for negtive data.
15:10	RW	0x00	bn_mul_shift_value_neg Shift value in bn core for negtive data.
9:4	RW	0x00	bs_mul_shift_value_neg Shift value in bs core for negtive data.
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	proc_precision Process precision. Same as proc_precision above.

DPU_offset_pend

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	offset_pend What value the extra channel be set.

DPU_dst_base_addr

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_base_addr Destination address of output feature map.

DPU_dst_surface_stride

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	dst_surface_stride Output shape surface stride.
2:0	RO	0x0	reserved

DPU_data_cube_width

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	width Feature width (minus 1).

DPU_data_cube_height

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	areo How many pixel to be processed in minmax op once.
24:22	RW	0x0	minmax_ctl Minmax control signal. [0]: enable minmax op; [1]: minmax type; [2]: probability only;
21:13	RO	0x000	reserved
12:0	RW	0x0000	height Feature height (minus 1).

DPU_data_cube_notch_addr

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	notch_addr_1 How many pixel from the end of width to the end of the shape line end 1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	notch_addr_0 How many pixel from the end of width to the end of the shape line end 0.

DPU_data_cube_channel

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	ori_channel Original output channel(minus 1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	channel Feature channel(minus 1). Rules are list following: dc 16b: Align to 8, dc 8b : Align to 16, dw 16b:Align to 16, dw 8b : Align to 32.

DPU_bs_cfg

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	bs_alu_src Where the alu operand from. 1'h0:From configure register, 1'h1:From outside.
7	RW	0x0	bs_relux_en If enable relu x.
6	RW	0x0	bs_relu_bypass Bypass relu op.
5	RW	0x0	bs_mul_prelu If enable prelu.
4	RW	0x0	bs_mul_bypass Bypass bs core mul op.
3:2	RW	0x0	bs_alu_algo BS core alu op type. 2'h0: Max, 2'h1: Min, 2'h2: Add.
1	RW	0x0	bs_alu_bypass Bypass bs core alu op.
0	RW	0x0	bs_bypass Bypass bs core.

DPU_bs_alu_cfg

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_alu_operand Bs core alu operand.

DPU_bs_mul_cfg

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bs_mul_operand BS core mul operand.
15:14	RO	0x0	reserved
13:8	RW	0x00	bs_mul_shift_value Shift value in bs core for positive data.
7:1	RO	0x00	reserved
0	RW	0x0	bs_mul_src Where the mul operand from. 0: from configure register, 1: from outside.

DPU_bs_relux_cmp_value

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_relux_cmp_dat Relux compare data in bs core.

DPU_bs_ow_cfg

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	rgp_cnter Regroup counter. 3'h0 : Select all data, 3'h1 : Select 1 from every 2, 3'h2 : Select 1 from every 4, 3'h3 : Select 1 from every 8.
28:11	RO	0x00000	reserved
10:8	RW	0x0	size_e_2 How many 8channel in a row the last output line(minus 1).
7:5	RW	0x0	size_e_1 How many 8channel in a row the middle output line(minus 1).
4:2	RW	0x0	size_e_0 How many 8channel in a row the first output line(minus 1).
1	RW	0x0	od_bypass Bypass cpend.
0	RW	0x0	ow_src Where the cpend operand from. 1'b0: From configure register, 1'b1: From outside.

DPU_bs_ow_op

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ow_op Cpend operand.

DPU_bn_cfg

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	bn_alu_src Where the alu operand from. 1'b0: From configure register, 1'b1: From outside.

Bit	Attr	Reset Value	Description
7	RW	0x0	bn_relux_en If enable relux.
6	RW	0x0	bn_relu_bypass Bypass relu.
5	RW	0x0	bn_mul_prelu If enable prelu.
4	RW	0x0	bn_mul_bypass Bypass bn core mul op.
3:2	RW	0x0	bn_alu_algo BN core alu op type. 2'h0: Max, 2'h1: Min, 2'h2: Add.
1	RW	0x0	bn_alu_bypass Bypass bn alu op.
0	RW	0x0	bn_bypass Bypass bn core.

DPU_bn_alu_cfg

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_alu_operand BN core alu operand.

DPU_bn_mul_cfg

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bn_mul_operand BN core mul operand.
15:14	RO	0x0	reserved
13:8	RW	0x00	bn_mul_shift_value Shift value in bs core for positive data.
7:1	RO	0x00	reserved
0	RW	0x0	bn_mul_src Where the mul operand from. 1'b0: From configure register, 1'b1: From outside.

DPU_bn_relux_cmp_value

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_relux_cmp_dat Relux compare data in bs core.

DPU_ew_cfg

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31	RW	0x0	ew_cvt_type Convert type of ew input convert when if 0.5. 1'b0 : Mul first, 1'b1 : Add first.

Bit	Attr	Reset Value	Description
30	RW	0x0	ew_cvt_round rounding type of ew input convert. 1'h0 : If the integer is odd, carr 1, 1'h1 : Carry 1 no matter what the integer is.
29:28	RW	0x0	ew_data_mode 2'h0 : Per channel, 2'h1 : Per pixel, 2'h2 : Per channel by pixel.
27:11	RO	0x00000	reserved
10	RW	0x0	ew_relux_en If enable relux.
9	RW	0x0	ew_relu_bypass Bypass relu.
8	RW	0x0	ew_op_cvt_bypass Bypass ew core operand convert.
7	RW	0x0	ew_lut_bypass Bypass lut.
6	RW	0x0	ew_op_src Where the operator operand from. 1'h0 : Configure register, 1'h1 : Outside.
5	RW	0x0	ew_mul_prelu If enable prelu.
4:3	RW	0x0	ew_alu_algo BS core alu op type. 2'h0: Max, 2'h1: Min, 2'h2: Add.
2	RW	0x0	ew_op_type Operator type. 1'b0:Alu, 1'b1:Mul.
1	RW	0x0	ew_op_bypass Bypass ew core alu and mul op.
0	RW	0x0	ew_bypass Bypass ew core.

DPU_ew_op_cvt_offset_value

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_op_cvt_offset EW convert offset.

DPU_ew_op_cvt_scale_value

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	ew_truncate EW core shift value.
21:16	RW	0x00	ew_op_cvt_shift EW convert shift value.
15:0	RW	0x0000	ew_op_cvt_scale EW convert scale.

DPU_ew_relux_cmp_value

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_relux_cmp_dat EW relux compare data.

DPU_out_cvt_offset

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	out_cvt_offset Out convert offset.

DPU_out_cvt_scale

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	out_cvt_scale Out convert scale.

DPU_out_cvt_shift

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31	RW	0x0	cvt_type Convert type of out convert when if 0.5. 0'b0 : Mul first, 1'b1 : Add first.
30	RW	0x0	cvt_round Rounding type of out convert when if 0.5 1'b0 : If the integer is odd, carry 1, 1'b1 : Carry 1 no matter what the integer is.
29:12	RO	0x00000	reserved
11:0	RW	0x000	out_cvt_shift Out convert shift value.

DPU_ew_op_src_value_0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_0 The 1st ew operand for ew core op.

DPU_ew_op_src_value_1

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_1 The 2nd ew operand for ew core op.

DPU_ew_op_src_value_2

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_2 The 3thd ew operand for ew core op.

DPU_ew_op_src_value_3

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_3 The 4th ew operand for ew core op.

DPU_ew_op_src_value_4

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_4 The 5th ew operand for ew core op.

DPU_ew_op_src_value_5

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_5 The 6th ew operand for ew core op.

DPU_ew_op_src_value_6

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_6 The 7th ew operand for ew core op.

DPU_ew_op_src_value_7

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand_7 The 8th ew operand for ew core op.

DPU_lut_access_cfg

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	lut_access_type LUT access type.
16	RW	0x0	lut_table_id LUT access id.
15:10	RO	0x00	reserved
9:0	RW	0x000	lut_addr LUT access address.

DPU_lut_access_data

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	lut_access_data LUT access data.

DPU_lut_cfg

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lut_hybrid_priority LUT priority when hybrid happened.
5	RW	0x0	lut_oflow_priority LUT priority when over flow happened.
4	RW	0x0	lut_uflow_priority LUT priority when under flow happened.

Bit	Attr	Reset Value	Description
3:2	RW	0x0	lut_lo_le_mux LUT lo le mux control.
1:0	RO	0x0	reserved

DPU_lut_info

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	lut_lo_index_select LUT LO index select.
15:8	RW	0x00	lut_le_index_select LUT LE index select.
7:0	RO	0x00	reserved

DPU_lut_le_start

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_le_start LUT LE start point.

DPU_lut_le_end

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_le_end LUT LE end point.

DPU_lut_lo_start

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_lo_start LUT LO start point.

DPU_lut_lo_end

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_lo_end LUT LO end point.

DPU_lut_le_slope_scale

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lut_le_slope_oflow_scale LUT LE slope scale when over flow happened.
15:0	RW	0x0000	lut_le_slope_uflow_scale LUT LE slope scale when under flow happened.

DPU_lut_le_slope_shift

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x00	lut_le_slope_oflow_shift LUT LE slope shift when over flow happened.
4:0	RW	0x00	lut_le_slope_uflow_shift LUT LE slope shift when under flow happened.

DPU_lut_lo_slope_scale

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lut_lo_slope_oflow_scale LUT LO slope scale when over flow happened.
15:0	RW	0x0000	lut_lo_slope_uflow_scale LUT LO slope scale when under flow happened.

DPU_lut_lo_slope_shift

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x00	lut_lo_slope_oflow_shift LUT LO slope shift when over flow happened.
4:0	RW	0x00	lut_lo_slope_uflow_shift LUT LO slope shift when under flow happened.

9.4.12 DPU_RDMA Registers Summary

Name	Offset	Size	Reset Value	Description
DPU_RDMA_s_status	0x0000	W	0x00000000	Statue register
DPU_RDMA_s_pointer	0x0004	W	0x00000000	Single Pointer Register
DPU_RDMA_op_en	0x0008	W	0x00000000	Operator enable register
DPU_RDMA_data_cube_width	0x000C	W	0x00000000	Feature width register
DPU_RDMA_data_cube_height	0x0010	W	0x00000000	Feature height register
DPU_RDMA_data_cube_channel	0x0014	W	0x00000000	Feature channel register
DPU_RDMA_src_base_addr	0x0018	W	0x00000000	Source address of feature map
DPU_RDMA_brdma_cfg	0x001C	W	0x00000000	BRDMA control register
DPU_RDMA_bs_base_addr	0x0020	W	0x00000000	BRDMA source address
DPU_RDMA_bs_data_amount	0x0024	W	0x00000000	BRDMA data amount
DPU_RDMA_nrdma_cfg	0x0028	W	0x00000000	NRDMA control register
DPU_RDMA_bn_base_addr	0x002C	W	0x00000000	NRDMA source address register
DPU_RDMA_bn_data_amount	0x0030	W	0x00000000	BRDMA data amount
DPU_RDMA_erdma_cfg	0x0034	W	0x00000000	ERDMA control register
DPU_RDMA_ew_base_addr	0x0038	W	0x00000000	ERDMA source address
DPU_RDMA_ew_areo_stride	0x003C	W	0x00000000	ERDMA areo stride register
DPU_RDMA_ew_surf_stride	0x0040	W	0x00000000	ERDMA surface stride register
DPU_RDMA_feature_mode_cfg	0x0044	W	0x00000000	Feature mode control register
DPU_RDMA_src_dma_cfg	0x0048	W	0x00000000	Source DMA configuration register
DPU_RDMA_surf_notch	0x004C	W	0x00000000	Surf notch address control register

Name	Offset	Size	Reset Value	Description
DPU_RDMA_pad_cfg	0x0064	W	0x00000000	Pad configuration register
DPU_RDMA_weight	0x0068	W	0x00000000	ARB weight register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.13 DPU_RDMA Detail Registers Description

DPU_RDMA_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

DPU_RDMA_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

DPU_RDMA_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

DPU_RDMA_data_cube_width

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	width Width(need to minus 1).

DPU_RDMA_data_cube_height

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	height Height(need to minus 1).

DPU_RDMA_data_cube_channel

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	channel Channel(need to minus 1).

DPU_RDMA_src_base_addr

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_base_addr Fly_mode src address.

DPU_RDMA_brdma_cfg

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:1	RW	0x0	brdma_data_use How many data type need to be read. [0]:If read alu operand, set 1 to enable, [1]:If read cpend operand, set 1 to enable, [2]:If read mul operand, set 1 to enable.
0	RW	0x0	brdma_disable If disable brdma.

DPU_RDMA_bs_base_addr

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_base_addr Base addr to read bs alu,bs cpend,bs mul operand.

DPU_RDMA_bs_data_amount

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_data_amount How many 8bytes need to be read, need to minus 1.

DPU_RDMA_nrdma_cfg

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:1	RW	0x0	nrdma_data_use How many data type need to be read. [0]:If read alu operand, set 1 to enable; [1]:If read cpend operand, set 1 to enable, (tie to 0, cause BN do not have cpend) [2]:If read mul operand, set 1 to enable.
0	RW	0x0	nrdma_disable If disable nrdma.

DPU_RDMA_bn_base_addr

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_base_addr Base addr to read bn alu,bn mul operand.

DPU_RDMA_bn_data_amount

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_data_amount How many 8bytes need to be read, need to minus 1.

DPU_RDMA_erdma_cfg

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	erdma_data_mode If the read data is per channel or per pixel. 0: Per channel, 1: Per pixel. 2: Per channel by pixel.
29:3	RO	0x0000000	reserved
2	RW	0x0	erdma_data_size If the read data is 8bit. 0: 8bit, 1: 16bit.
1	RO	0x0	reserved
0	RW	0x0	erdma_disable If disable erdma.

DPU_RDMA_ew_base_addr

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_base_addr Base addr to read ew operand.

DPU_RDMA_ew_areo_stride

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	ew_areo_stride The feature areo need to be read by erdma.If erdma_data_mode is per channel, it need set to be 0, else is (width+1)*(height+1).
2:0	RO	0x0	reserved

DPU_RDMA_ew_surf_stride

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	ew_surf_stride The surface stride of the element wise feature map; If erdma_data_mode is per channel, it need set to be 1.
2:0	RO	0x0	reserved

DPU_RDMA_feature_mode_cfg

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	shrink_enable If in_precision is i16 or fp16, and out_precision is i8, this bit need set to be high. And it is flymode only.
17:15	RW	0x0	in_precision Input data precision. 0:INT8, 1:INT16, 2:FP16, 3:INT32, 4:FP32.
14:13	RW	0x0	burst_len Burst length 0: Burst4, 1: Burst8, 2: Burst16.
12:7	RO	0x00	reserved
6:5	RW	0x0	proc_precision Process precision 0:INT8 1:INT16 2:FP16.
4:3	RO	0x0	reserved
2:1	RW	0x0	conv_mode Convolution mode. 0:Dc 3:Depthwise
0	RW	0x0	flying_mode Flying_mode enable. 0:Dpu core main data is from convolution output; 1:Dpu core main data is from mrdma.

DPU_RDMA_src_dma_cfg

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	line_notch_addr How many pixel from the end of width end to the shape feature line end.
18:14	RO	0x00	reserved
13	RW	0x0	pooling_method Pooling method. 0: Average pooling(up sampling can use this mode), 1: Min or max pooling.
12	RW	0x0	up_en If enable unpooling.
11:9	RW	0x0	ker_stride_height Unpooling kernel stride height(minus 1).

Bit	Attr	Reset Value	Description
8:6	RW	0x0	ker_stride_width Unpooling kernel stride width(minus 1).
5:3	RW	0x0	ker_height Unpooling kernel height(minus 1).
2:0	RW	0x0	ker_width Unpooling kernel width(minus 1).

DPU_RDMA_surf_notch

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	surf_notch_addr How many pixel from the end of this process feature map to the end of the shape feature map.
2:0	RO	0x0	reserved

DPU_RDMA_pad_cfg

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pad_value Pad value.
15:7	RO	0x000	reserved
6:4	RW	0x0	pad_top Unpooling top pad.
3	RO	0x0	reserved
2:0	RW	0x0	pad_left Unpooling left pad.

DPU_RDMA_weight

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	e_weight The arbiter weight for erdma.
23:16	RW	0x00	n_weight The arbiter weight for nrdma.
15:8	RW	0x00	b_weight The arbiter weight for brdma.
7:0	RW	0x00	m_weight The arbiter weight for mrdma.

9.4.14 PPU Registers Summary

Name	Offset	Size	Reset Value	Description
PPU_s_status	0x0000	W	0x00000000	Statue register
PPU_s_pointer	0x0004	W	0x00000000	Single Pointer Register
PPU_op_en	0x0008	W	0x00000000	Operator enable register
PPU_data_cube_in_width	0x000C	W	0x00000000	Feature width register
PPU_data_cube_in_height	0x0010	W	0x00000000	Feature height register
PPU_data_cube_in_channel	0x0014	W	0x00000000	Feature channel register
PPU_data_cube_out_width	0x0018	W	0x00000000	Output width register
PPU_data_cube_out_height	0x001C	W	0x00000000	Output height register

Name	Offset	Size	Reset Value	Description
PPU_data_cube_out_channel	0x0020	W	0x00000000	Output channel register
PPU_operation_mode_cfg	0x0024	W	0x00000000	PPU operation register
PPU_pooling_kernel_cfg	0x0034	W	0x00000000	Pooling kernel control register
PPU_recip_kernel_width	0x0038	W	0x00000000	Recipe width register
PPU_recip_kernel_height	0x003C	W	0x00000000	Recipe height register
PPU_pooling_padding_cfg	0x0040	W	0x00000000	Pooling pad configuration register
PPU_pooling_padding_value_1_cfg	0x0044	W	0x00000000	Pooling pad value register 0
PPU_pooling_padding_value_2_cfg	0x0048	W	0x00000000	Pooling pad value register 1
PPU_pooling_padding_value_3_cfg	0x004C	W	0x00000000	Pooling pad value register 2
PPU_pooling_padding_value_4_cfg	0x0050	W	0x00000000	Pooling pad value register 3
PPU_dst_base_addr	0x0070	W	0x00000000	Destination address register
PPU_dst_surface_stride	0x007C	W	0x00000000	Destination surface stride
PPU_data_format	0x0084	W	0x00000000	Data format control register
PPU_misc_ctrl	0x00DC	W	0x00000000	Misc control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.15 PPU Detail Registers Description

PPU_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

PPU_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.

Bit	Attr	Reset Value	Description
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

PPU_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

PPU_data_cube_in_width

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_width Pooling cube width (need to minus 1).

PPU_data_cube_in_height

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_height Pooling cube height (need to minus 1).

PPU_data_cube_in_channel

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_channel Pooling cube channel (need to minus 1).

PPU_data_cube_out_width

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_out_width Pooling output cube width (need to minus 1).

PPU_data_cube_out_height

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_out_height Pooling output cube height (need to minus 1).

PPU_data_cube_out_channel

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_out_channel Pooling output cube channel (need to minus 1).

PPU_operation_mode_cfg

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	bf16_en If bf16 mode, cfg:1 else cfg: 0
30	RW	0x0	index_en If enable output the position of each kernel.
29	RO	0x0	reserved
28:16	RW	0x0000	notch_addr How many pixel from the end of the width end to the shape line end.
15:8	RO	0x00	reserved
7:5	RW	0x0	use_cnt Use count .
4	RW	0x0	flying_mode Where the pooling cube from 0: Dpu 1: Outside
3:2	RO	0x0	reserved
1:0	RW	0x0	pooling_method Pooling method 0: Average pooling; 1: Max pooling 2: Min pooling

PPU_pooling_kernel_cfg

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	kernel_stride_height Pooling kernel stride height (need to minus 1).
19:16	RW	0x0	kernel_stride_width Pooling kernel stride width (need to minus 1).
15:12	RO	0x0	reserved
11:8	RW	0x0	kernel_height Pooling kernel height (need to minus 1).
7:4	RO	0x0	reserved
3:0	RW	0x0	kernel_width Pooling kernel width (need to minus 1).

PPU_recip_kernel_width

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	recip_kernel_w The Reciprocal of the shape kernel width multiple 2^16.

PPU_recip_kernel_height

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	recip_kernel_height The Reciprocal of the shape kernel height multiple 2^16.

PPU_pooling_padding_cfg

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	pad_bottom Pooling bottom pad.
11	RO	0x0	reserved
10:8	RW	0x0	pad_right Pooling right pad.
7	RO	0x0	reserved
6:4	RW	0x0	pad_top Pooling top pad.
3	RO	0x0	reserved
2:0	RW	0x0	pad_left Pooling left pad.

PPU_pooling_padding_value_1_cfg

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_1x Pad_value*1.

PPU_pooling_padding_value_2_cfg

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_2x Pad_value*2.

PPU_pooling_padding_value_3_cfg

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_3x Pad_value*3.

PPU_pooling_padding_value_4_cfg

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_4x Pad_value*4.

PPU_dst_base_addr

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dst_base_address Base addr the output cube goes.
3:0	RO	0x0	reserved

PPU_dst_surface_stride

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dst_surf_stride Output shape areo.
3:0	RO	0x0	reserved

PPU_data_format

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	index_add If index_en enable , this register is dst_surface_stride x number of cube surface(every 8bytes per surface), else it equals to dst_surface_stride.
2	RW	0x0	dpu_flyin If the data from dpu, and dpu data is from outside ,this bit set to be 1.
1:0	RW	0x0	proc_precision Proc_precision.

PPU_misc_ctrl

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	surf_len In nonalign mode, how many 8bytes to be stored.
15:8	RO	0x00	reserved
7	RW	0x0	nonalign Noalign mode enable.
6:4	RO	0x0	reserved
3:0	RW	0x0	rd_burst_len Burst length 3:Burst4, 7:Burst8, 15:Burst16.

9.4.16 PPU_RDMA Registers Summary

Name	Offset	Size	Reset Value	Description
PPU_RDMA_s_status	0x0000	W	0x00000000	Statue register
PPU_RDMA_s_pointer	0x0004	W	0x00000000	Single Pointer Register
PPU_RDMA_op_en	0x0008	W	0x00000000	Operator enable register
PPU_RDMA_data_cube_in_width	0x000C	W	0x00000000	Data width register
PPU_RDMA_data_cube_in_height	0x0010	W	0x00000000	Data height register
PPU_RDMA_data_cube_in_channel	0x0014	W	0x00000000	Data channel register
PPU_RDMA_flying_mode	0x0018	W	0x00000000	Flying mode control register
PPU_RDMA_src_base_addr	0x001C	W	0x00000000	Source address register
PPU_RDMA_src_line_stride	0x0024	W	0x00000000	Source line stride

Name	Offset	Size	Reset Value	Description
PPU_RDMA_src_surface_stride	0x0028	W	0x00000000	Source surface stride
PPU_RDMA_data_format	0x0030	W	0x00000000	Data format register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.17 Detail Registers Description

PPU_RDMA_s_status

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 0: Executer 1 is in idle state, 1: Executer 1 is operating, 2: Executer 1 is operating, executer 0 is waiting to operate .
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 0: Executer 0 is in idle state, 1: Executer 0 is operating, 2: Executer 0 is operating, executer 1 is waiting to operate .

PPU_RDMA_s_pointer

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear 1: Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode 1: Pointer ping-pong by pointer, eg. if current pointer is 0, next pointer will toggle to 1, 0: Pointer ping-pong by executer, eg. if current executer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en 1: Enable executer auto ping-pong.
1	RW	0x0	pointer_pp_en 1: Enable pointer auto ping-pong.
0	RW	0x0	pointer Which register group ready to be setted.

PPU_RDMA_op_en

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_enable Set this register will trigger cna block operate. This register and after this are all shadowed for ping-pong operation.

PPU_RDMA_data_cube_in_width

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_width Pooling cube width (need to minus 1).

PPU_RDMA_data_cube_in_height

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_height Pooling cube height (need to minus 1).

PPU_RDMA_data_cube_in_channel

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_channel Pooling cube channel(need to minus 1).

PPU_RDMA_flying_mode

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fly_mode Where the pooling cube from. 0: From dpu, 1: From outside.

PPU_RDMA_src_base_addr

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	source_base_addr Base address of the pooling cube .

PPU_RDMA_src_line_stride

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	source_line_stride Pooling cube shape width.
2:0	RO	0x0	reserved

PPU_RDMA_src_surface_stride

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	source_surface_stride Pooling cube shape areo.
2:0	RO	0x0	reserved

PPU_RDMA_data_format

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	in_precision Input precision, 0: INT8 1: INT16 2: FP16.

9.4.18 DMA Registers Summary

Name	Offset	Size	Reset Value	Description
DMA_CFG_OUTSTANDING	0x0000	W	0x00000000	Outstanding control register
DMA_RD_WEIGHT_0	0x0004	W	0x00000000	Read weight register 0
DMA_WR_WEIGHT_0	0x0008	W	0x00000000	Write weight register 0
DMA_CFG_ID_ERROR	0x000C	W	0x00000000	Error ID register
DMA_RD_WEIGHT_1	0x0010	W	0x00000000	Read weight register 1
DMA_CFG_DMA_FIFO_CLR	0x0014	W	0x00000000	DMA FIFO clear configuration register
DMA_CFG_DMA_ARB	0x001C	W	0x00000000	DMA arbiter configuration register
DMA_CFG_DMA_RD_QOS	0x0020	W	0x00000000	Read DMA QOS configuration register
DMA_CFG_DMA_RD_CFG	0x0024	W	0x00000000	Read DMA configuration register
DMA_CFG_DMA_WR_CFG	0x0028	W	0x00000000	Write DMA configuration register
DMA_CFG_DMA_WSTRB	0x002C	W	0x00000000	DMA WSTRB configuration register
DMA_CFG_STATUS	0x0030	W	0x00000000	STATUS register
DMA_DDR_FD_WRITE_BW	0x0034	W	0x00000000	Feature write BW summery register
DMA_DDR_FD_READ_BW	0x0038	W	0x00000000	Feature read BW summery register
DMA_DDR_WT_READ_BW	0x003C	W	0x00000000	Weight read BW summery register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.19 DMA Detail Registers Description

DMA_CFG_OUTSTANDING

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	wr_os_cnt Wr_os_cnt.
7:0	RW	0x00	rd_os_cnt Rd_os_cnt.

DMA_RD_WEIGHT_0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	read_weight_pdp Rd_weight_pdp.
23:16	RW	0x00	read_weight_dpu Rd_weight_dpu.
15:8	RW	0x00	read_weight_kernel Rd_weight_kernel.
7:0	RW	0x00	read_weight_feature Rd_weight_feature.

DMA_WR_WEIGHT_0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	write_weight_pdp Wr_weight_pdp.
7:0	RW	0x00	write_weight_dpu Wr_weight_dpu.

DMA_CFG_ID_ERROR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:6	RW	0x0	wr_resp_id Wr_resp_id.
5	RO	0x0	reserved
4:0	RW	0x00	rd_resp_id Rd_resp_id.

DMA_RD_WEIGHT_1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	monitor_clr Monitor_clr.
30:8	RO	0x000000	reserved
7:0	RW	0x00	read_weight_pc Rd_weight_pc.

DMA_CFG_DMA_FIFO_CLR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	fifo_clr Dma_fifo_clr.

DMA_CFG_DMA_ARB

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	wr_arbit_model Wr_arbit_model.
8	RW	0x0	rd_arbit_model Rd_arbit_model.
7	RO	0x0	reserved
6:4	RW	0x0	wr_fix_arb Wr_fix_arb.
3	RO	0x0	reserved
2:0	RW	0x0	rd_fix_arb Rd_fix_arb.

DMA_CFG_DMA_RD_QOS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	rd_pc_qos Rd_pc_qos.
7:6	RW	0x0	rd_ppu_qos Rd_pdp_qos.
5:4	RW	0x0	rd_dpu_qos Rd_dpu_qos.
3:2	RW	0x0	rd_kernel_qos Rd_kernel_qos.
1:0	RW	0x0	rd_feature_qos Rd_feature_qos.

DMA_CFG_DMA_RD_CFG

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	rd_arlock Rd_arlock.
11:8	RW	0x0	rd_arcache Rd_arcache.
7:5	RW	0x0	rd_arprot Rd_arprot.
4:3	RW	0x0	rd_arburst Rd_arburst.
2:0	RW	0x0	rd_arsize Rd_arsize.

DMA_CFG_DMA_WR_CFG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	wr_awlock Wr_awlock.
11:8	RW	0x0	wr_awcache Wr_awcache.
7:5	RW	0x0	wr_awprot Wr_awprot.
4:3	RW	0x0	wr_awburst Wr_awburst.
2:0	RW	0x0	wr_awsize Wr_awsize.

DMA_CFG_DMA_WSTRB

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_wstrb Wr_wstrb.

DMA_CFG_STATUS

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	idle Idle status.
7:0	RO	0x00	reserved

DMA_DDR_FD_WRITE_BW

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fd_write_bw Ddr_fd_write_bw.

DMA_DDR_FD_READ_BW

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fd_read_bw Ddr_fd_read_bw.

DMA_DDR_WT_READ_BW

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wt_read_bw Ddr_wt_read_bw.

9.4.20 GLOBAL Registers Summary

Name	Offset	Size	Reset Value	Description
GLOBAL_OP_EN	0x0008	W	0x00000000	Operator enable register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

9.4.21 GLOBAL Detail Registers Description

GLOBAL_OP_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ppu_rdma_op_en PPU_RDMA enable.
5	RW	0x0	ppu_op_en PPU enable.
4	RW	0x0	dpu_rdma_op_en DPU_RDMA enable.
3	RW	0x0	dpu_op_en DPU enable.
2	RW	0x0	accu_op_en ACCU enable.
1	RW	0x0	cmac_op_en CMAC enable.
0	RW	0x0	cna_op_en Cna enable.

9.5 Application Notes

9.5.1 ping-pong registers

In order to reduce the time of fetch registers, every Calculate Core and Control Core of NPU has its owner ping-pong registers. Configure the group 0 when use the group 1, and configure the group 1 when use group 0. As a result of hiding the time of fetch registers. Writing S_POINTER of every block can enable this function.

9.5.2 Clock and Reset

- Clock Domains

NPU has two clock domains, one is AHB clock, the other is AXI clock. AHB clock, which is the

clock for AHB interface, while AXI clock, which is the clock for AXI interface. AXI clock also used for core clock for every Calculate Core and Control Core. Clock frequency can be controlled by CRU, please refer to the relevant sections. Automatic localized clock gating is employed throughout the design in order to minimize the dynamic power consumption. Almost all of the flip-flops are clock gated in the design. Block level clock gating also implemented in every separate block. If a block and the interface to the block are both idle, then the clock of that block will be gated automatically. This feature can be disabled by software.

- NPU Reset

Correspond to the clock domain, there are two reset signals. Aresetn, the reset signal for AXI interface and every Calculate Core and Control Core.Hresetn is the AHB interface reset pin and which is synchronized to the AHB clock domain.
All the two signals must be asserted for a minimum of 32 core clock cycles, using the slowest of the two clocks. Then two signals must be release at the same time.

9.5.3 NPU Interrupt Application

NPU has 1 interrupt output signal and it remains asserted until the host processor clears the interrupt. Each bit of PC_INTERRUPT_STATUS represents one of the 17 possible events that the NPU can signal to the host processor. By setting the bits of the interrupt enable register (PC_INTERRUPT_MASK) the programmer can control which of those events will generate an interrupt.

9.5.4 NPU Debugging Support

NPU provide some debug registers help figure out the problem when NPU crashed or some else happened. These register are list below.

Table 9-1 Debug register list

Registers	Describe
pc_interrupt_status	int_st[0] : cna feature group 0 interrupt status, which and with mask bit int_st[1] : cna feature group 1 int_st[2] : cna weight group 0 int_st[3] : cna weight group 1 int_st[4] : cna csc group 0 int_st[5] : cna csc group 1 int_st[6] : accu group 0 int_st[7] : accu group 1 int_st[8] : dpu group 0 int_st[9] : dpu group 1 int_st[10] : ppu group 0 int_st[11] : ppu group 1 int_st[12] : dma read error int_st[13] : dma write error int_st[16] : mmu error
cna_dc_status	[14:3] buffer full or empty signal; [2:0] fetch data and weight status
cna_csc_status	[2:0] which condition is missed for normal work.

9.5.5 NPU operate flow

NPU has two types of work mode: slave configured mode and PC work mode. PC work mode need to initial register information to the system memory, then obey flowing flows as Fig. 1-2 shows.
The information of registers initial to the system memory need to generate by the op you want to specify. So we describe the normal work flows by describe the slave configured mode.

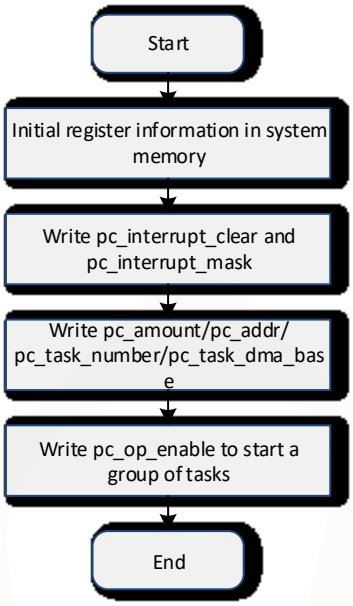


Fig. 9-2 PC flow

convolution flow

NPU supports variety of convolution and matrix multiplication. If use the MAC array to calculate, the work flow obey the Fig. 1-3, and if use DPU CORE calculate, work flow obey the Fig. 1-4.

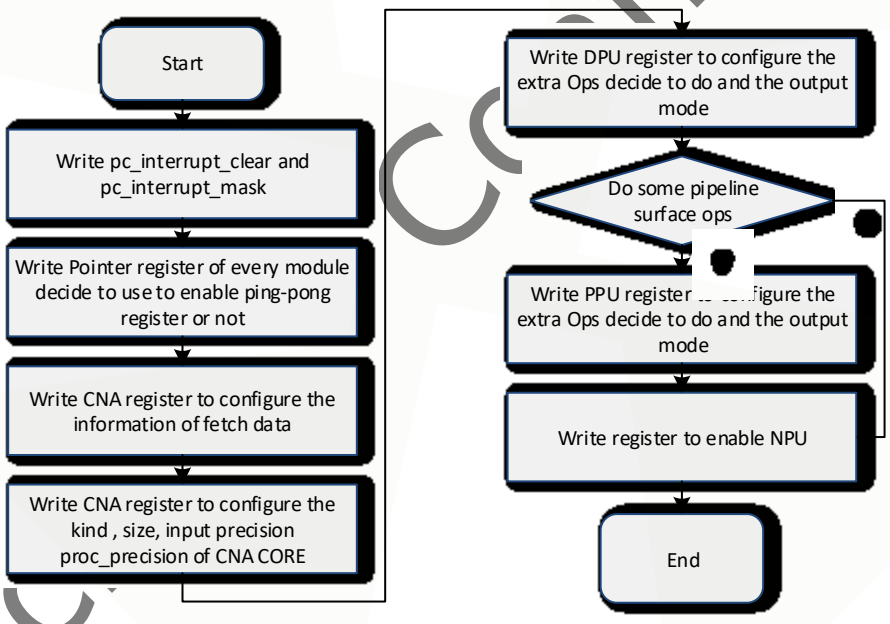


Fig. 9-3 convolution flow 1

In step 1, do not set PPU mask bit if don't use PPU.

In step 3, you need to configure the size of feature map, and the input precision, process precision, grains, entries and weight size, including weight height, weight width, kernels and weight bytes etc.

In step 4, you need to configure process precision, conv_mode and auto gating registers of CMAC and CNA sequence controller.

In step 5, you can specify some operators to the outputs of convolution according to configure the DPU_CORE. DPU CORE has some fixed operators, also you can specify some programmed operators.

In step 6, you can do some extra operators to the outputs of DPU, pooling for example.

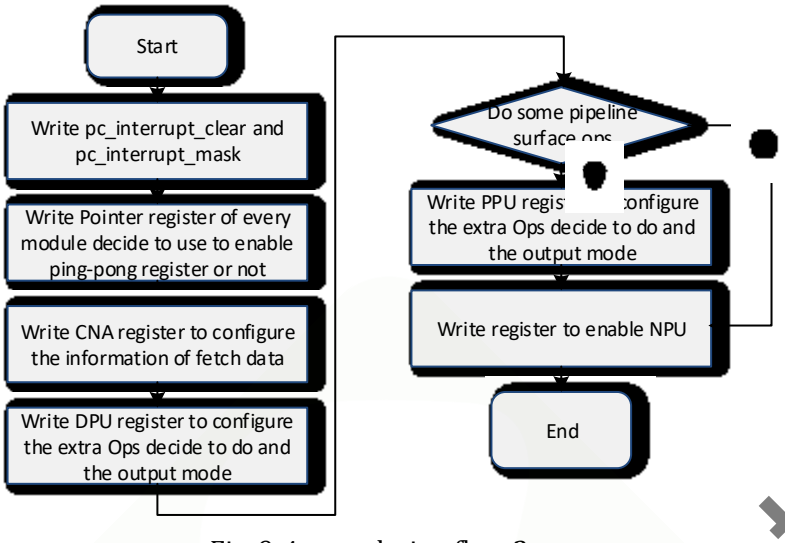


Fig. 9-4 convolution flow 2

In step 3, you need to configure the size of feature map, and the input precision, process precision, grains, entries and weight size, including height, width, kernels and weight bytes etc. Here we supply zero skipping switch, if there's a lot of zero or some number else in the feature map, you can enable zero skipping by writing cna_fc_con0, cna_fc_con1 and cna_fc_con2, as a result of without reading the weights correspond to the pixel in the feature map. In zero skipping mode, you can specify the feature map size for read different from the feature map size for calculate.

If enable zero skipping, the conv_mode of DPU must configure to be 3, and must bypass the BS_CORE. The alu_src must set to be 0, the mul_src must set to be 1, and the alu_algo must set be 3. We bypass BS_CORE, and use BN_CORE to calculate convolution, so the extra operators have to achive by EW_CORE. But we use NRDMA to read operands to EW_CORE when ew_src is 1.

- Pooling flow

You can use PPU in two ways, pipeline with DPU, and flying mode separately. The first one is described above, we describe the second flow below.

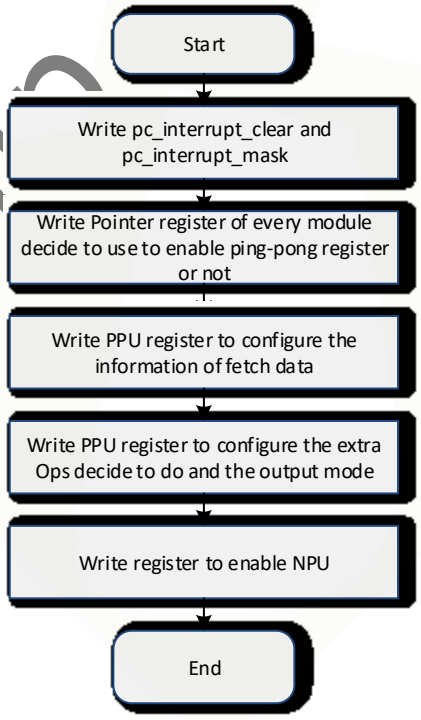


Fig. 9-5 Pooling flow

In step 4, we supply two type of output mode, 8byte align per pixel and nonalign mode. In some cases with uncomfortable feature map size, you can enable nonalign mode by writing ppu_misc_ctrl_nonalign and ppu_misc_ctrl_surf_len.

- separate op flow

As for the operators that NPU do not fixed, you can combine DPU and PPU to achieve it. Following

we describe the DPU flying mode flow.

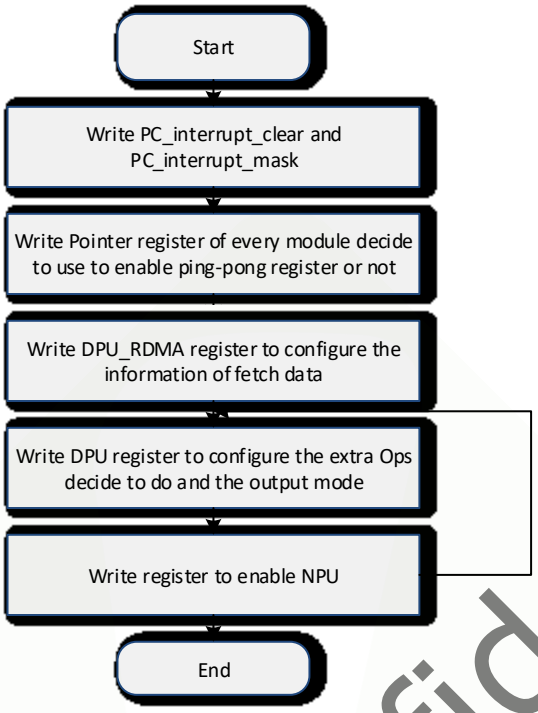


Fig. 9-6 DPU flying mode flow

In step 3, you can enable MRDMA , BRDMA, NRDMA, ERDMA to fetch data. NPU supports 6 types of data input precision.

In step 4, you can configure BS_ALU_BYPASS, BS_MUL_BYPASS, BS_RELU_BYPASS, BS_MUL_PRELU, BS_MUL_SHIFT, BS_RELUX_EN etc. to specify the operators you want to achive.

Chapter 10 Multi-format Video Encoder and Decoder

10.1 Overview

VPU_Combo is composed by the VDPU121,VDPU346, VEPU121(JPEG encoder only) and VEPU540 to realize the high quality video decoding and encoding.
VDPU121 can support such as H.263,MPEG1/2/4 and so on,max solution is up to 1920x1088.
VDPU346 can support such as H265 and H264 and VP9 decoder,max solution is up to 4096x2304.
VDPU720 can support JPEG decoder.
VEPU121 can support JPEG encoder.
VEPU540 can support H265 and H264 encoder encoder,max resolution is up to 4096x4096.

10.1.1 Feature

The features of VDPU121 and VDPU346 decoder are listed as follows:

- MMU embedded with MMU interrupt support
- H.265 HEVC/MVC Main10 Profile yuv420@L5.1 up to 4096x2304@60fps
- H.264 AVC/MVC Main10 Profile yuv400/yuv420/yuv422/@L5.1 up to 4096x2304@30fps
- VP9 Profile0/2 yuv420@L5.1 up to 4096x2304@60fps
- VP8 verision2,up to 1920x1088@60fps
- VC1 Simple Profile@low,medium,high levels,Main Profile@low,medium,high levels, Advanced Profile@level0~3,up to 1920x1088@60fps
- MPEG-4 Simple Profile@L0~6,Advanced Simple Profile@L0~5,up to 1920x1088@60fps
- MPEG-2 Main Profile,low medium and high levels,up to 1920x1088@60fps
- MPEG-1 Main Profile,low,medium and high levels,up to 1920x1088@60fps
- H.263 Profile0,levels 10-70,up to 720x576@60fps
- JPEG Baseline interleaved,up to 8176x8176@76 milion pixels per second

The features of VDPU720 decoder are listed as follows:

- Supports JPEG decoding
  - 48x48 to 65536x65536(4295Mpixels)，Step size 8 pixels
  - Baseline interleaved, and supports ROI (region of image) decode

The features of VEPU12X encoder are listed as follows:

- JPEG:
  - Baseline Non-progressive
  - up to 8192x8192 resolution
  - up to 90 million pixels per second

The features of VEPU540 encoder are listed below:

- HEVC main profile encoding, up to level 5.0
- H.264 high profile encoding, up to level 5.1
- Resolution up to 4096x4096
- Intelligent encoding to improve subjective quality
- Block level bitrate control
- Slice split
- Block based ROI configuration
- 8-area OSD
- Support link table mode
- YUV/RGB video source with rotation and mirror
- Frame buffer compression
- MMU inside

10.2 Block Diagram

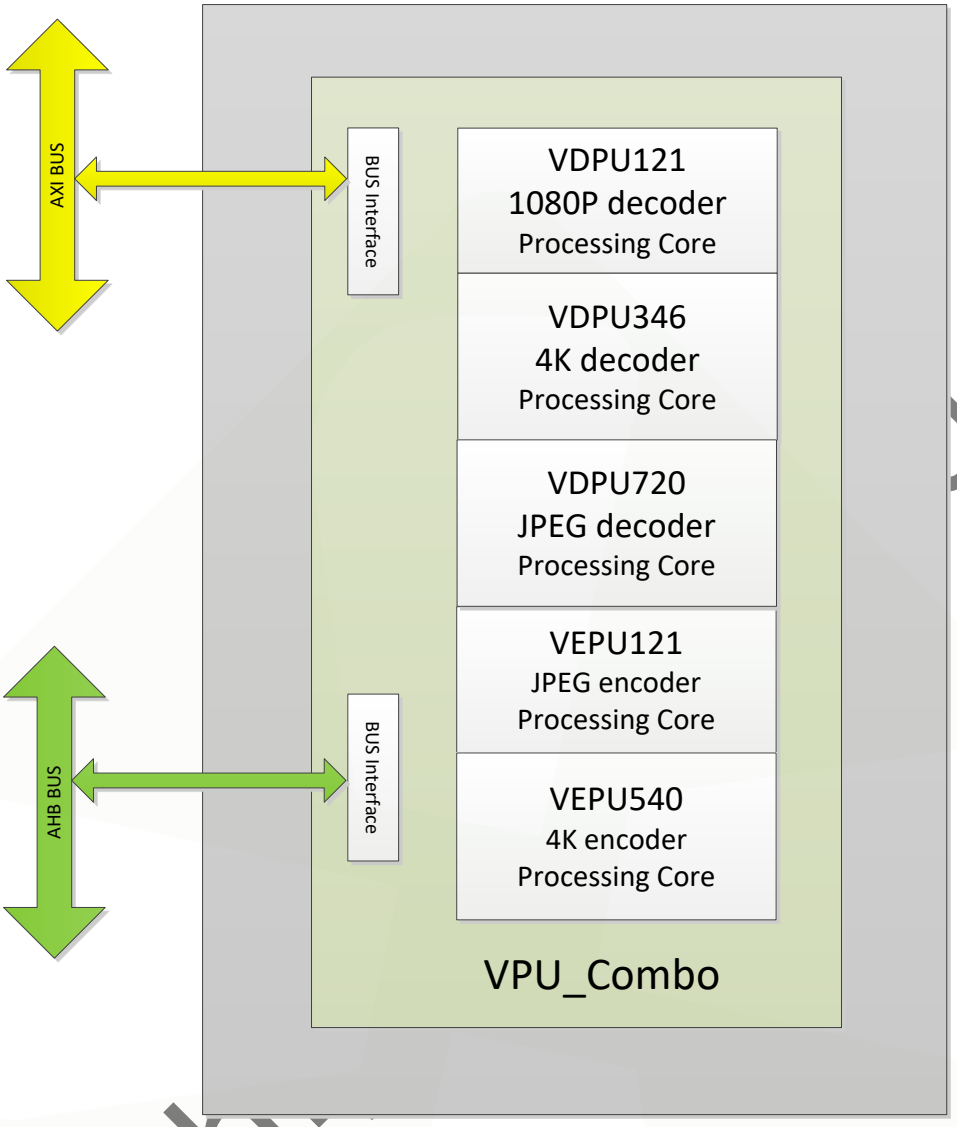


Fig. 10-1 VPU Combo Block Diagram

As shown in the figures above, CPU accesses to the decoder register bank through AHB bus. Bitstream and other necessary data are fed into processing core though AXI read channel, and after several steps of decoding process, decoded pictures and other information data are transferred to designated location in the DDR through AXI write channel.

VDPU121 1080P processing core support multi-format decoder,such as mpeg4,h.263 and so on.

VDPU720 processing core support jpeg decoder.

VEPU121 1080P processing core support jpeg encoder.

VDPU346 4K decoder processing core can support h.265/vp9/h.264 video standard decoder,max solution size is 4096x2304.

VEPU540 4K encoder processing core can support HEVC/H.264 video encoder，max solution size is 4096x4096

Please note that VDPU121 and VEPU121 and VDPU346 and VEPU540 is four IP cores, so such four processing core can be work together.

10.3 Video frame format

This chapter describes different input and output video frame formats supported by VCODEC. Each function module has its own supported video frame formats, and this chapter describes all the video frame formats.

10.3.1 YCbCr 4:2:0 Planar Format

In the planar format, each video sample component forms one memory plane. Within one plane, the data has to be stored linearly and contiguously in the memory as shown in fellows. The luminance samples are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The chrominance samples are stored in two planes also in raster scan order (Cb0Cb1 Cb2Cb3 Cb4…. and Cr0Cr1 Cr2Cr3 Cr4….). In this format each pixel takes 12 bits of memory.

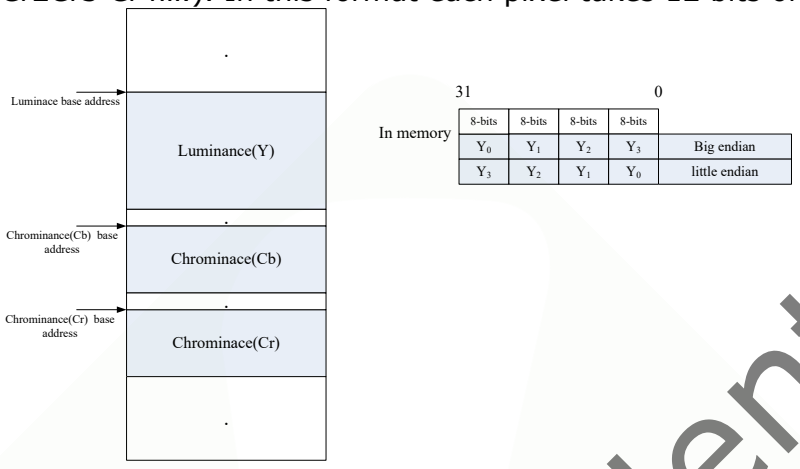


Fig. 10-2 VCODEC YCbCr 4:2:0 planar format

10.3.2 YCbCr 4:2:0 Semi-Planar format

In semi-planar YcbCr4:2:0 format the luminance samples from one plane in memory, and chrominance samples from another. Within one plane, the data has to be stored linearly and contiguously in the memory. The luminance pixels are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The interleaved chrominance CbCr samples are stored in raster-scan order in memory as Cb0Cr0 Cb1Cr1 Cb2 Cr2 Cb3Cr3 Cb4 Cr4….

Semi-Planar format supports both progressive and interlaced format as presented in Fig.10-3. The interlaced format may be alternative line or each line.

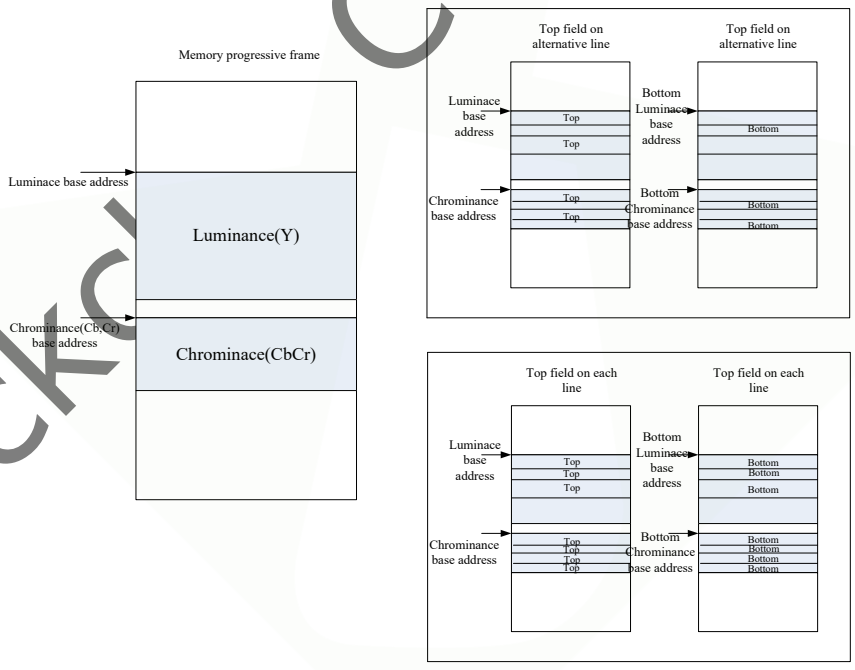


Fig. 10-3 VCODEC YCbCr 4:2:0 Semi-planar format

10.3.3 YCbCr 4:2:0 Tiled Semi-Planar Format

Like the YCbCr 4:2:0 semi-planar format, the tiled semi-planar format is also organized in the memory on two separate planes. The difference between these formats is that in tiled format the pixel samples are not anymore in raster-scan order but are stored macroblock (16x16 pixels) by macroblock. The samples of each macroblock are stored in consecutive addresses and the macroblocks are ordered from left to right and from top to down as Fi.10-4. When this format used as input data format, it causes the lowest bus load to the system

as there is minimal amount of non-sequential memory addressing required when reading the input data to the post-processor.

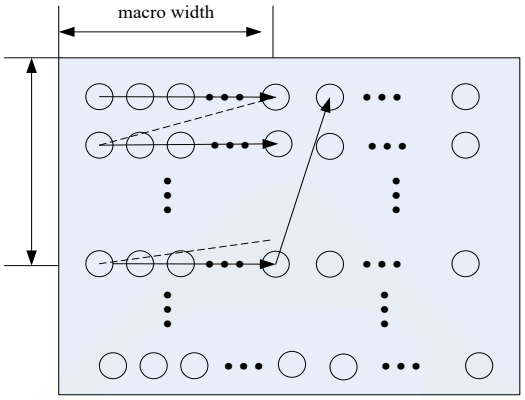


Fig. 10-4 VCODEC Tile scan mode

10.3.4 YCbCr 4:2:2 Interleaved Format

In the interleaved YCbCr 4:2:2 format the pixel samples from a single plane in which the data has to be stored linearly and contiguously as shown in Fig.10-5. The pixel data is in raster scan order and the chrominance samples are interleaved between the luminance samples as Y0Cb0 Y1Cr0 Y2 Cb1 Y3Cr1 Y4 Cb2…. YCrCb, CbYCrY and CrYCbY component orders are supported also. In this format, each pixel takes 16 bits in the memory.

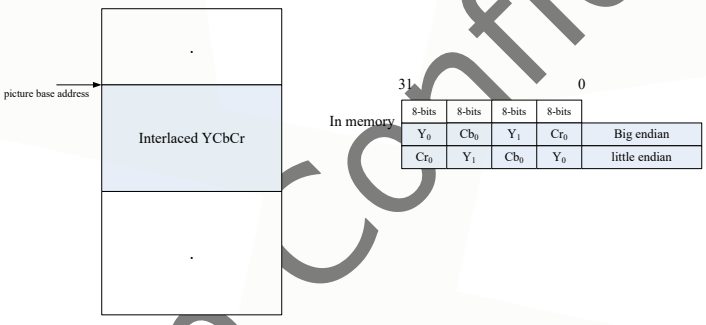


Fig. 10-5 VCODEC YCbCr4:2:2 Interleaved format

10.3.5 AYCbCr 4:4:4 Interleaved Format

In the interleaved YcbCr 4:2:2 format, the pixel samples from a single plane in which the data has to be stored linearly and contiguously as show in Fig.10-6. The pixel data is in raster scan order and the chrominance and alpha channel samples are interleaved between the luminance samples as A0Y0 Cb0Cr0 A1 Y1 Cb1Cr1….

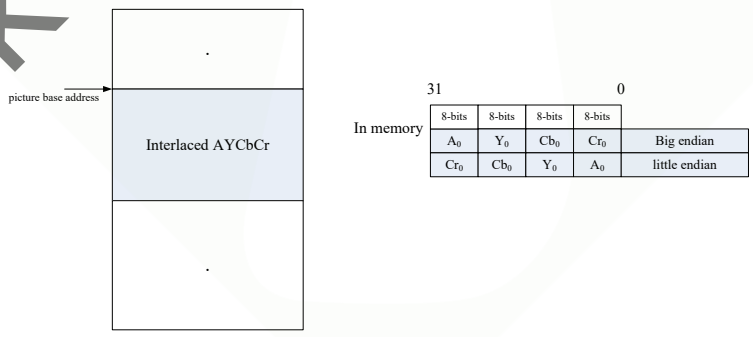


Fig. 10-6 VCODEC AYCbCr 4:4:4 Interleaved format

10.3.6 RGB 16bpp Format

In this format each pixel is represented by 16 or less bits containing the red, blue and green samples. There are several 16bpp formats which use different number of bits for each sample. For example the RGB 5-5-5 format uses 5 bits for each sample and 1 bit is left unused or can represent a transparency flag, where RGB 5-6-5 uses 6 bits for the G sample and 5 bits for R and B samples. Common for all 16bpp types is that two pixels fit into one

32-bit space.

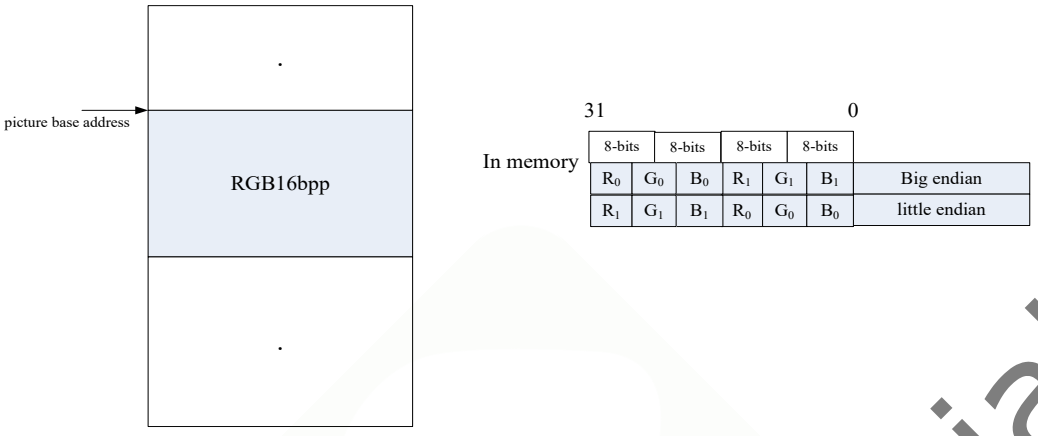


Fig. 10-7 VCODEC RGB 16bpp format

10.3.7 RGB 32bpp Format

Any RGB format that has its pixels represented by more than 16bits each is considered to be of 32bpp type. Typically in this format each pixel is represented by three bytes containing a red, blue and green sample and a 4th byte which can be empty or hold an alpha blending value. Common for all 32bpp types is that only one pixel fit into one 32-bit space. The data has to be stored linearly and contiguously in the memory.

10.3.8 Frame Buffer Compress (FBC) Format

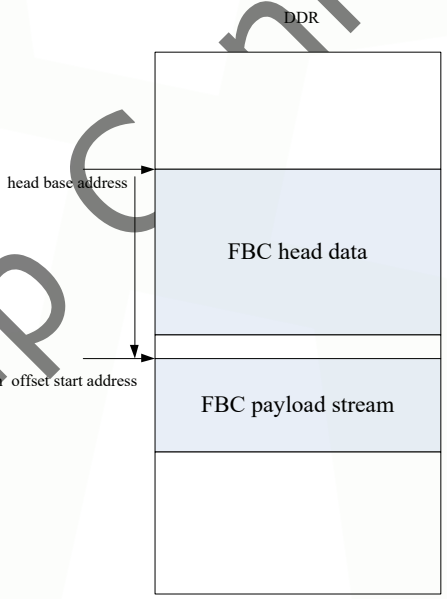


Fig. 10-9 FBC output format

As shown in the figures above,FBC output format include FBC head data and FBC payload stream.Every 16x16 block used one FBC head,every FBC head will take up 128bit ddr space, FBC HEAD is raster store and can support virtual stride .The payload stream use compact mode ,and the maximum ddr space which be required is equal to uncompress picture size.

10.4 Function Description

10.4.1 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:
1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

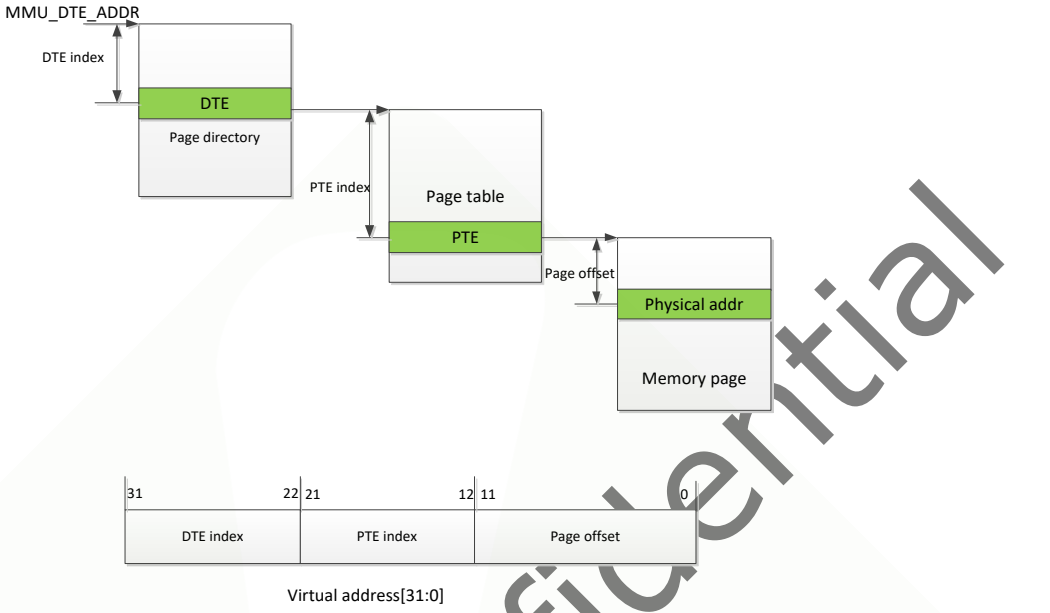


Fig. 10-8 structure of two-level page table

10.4.2 VDPU121 feature supported

1. MPEG-4 decoder

The features that video decoder supports about MPEG-4/H.263 shows as below Table 10-1.

Table 10-1 MPEG-4/H.263 feature

Feature	Decoder support
Input data format	MPEG-4/H.263 elementary video stream
Decoding scheme	Frame by frame(or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1920x1088(MPEG-4) 48x48 to 720x576(H.263) Step size 16 pixels
Maximum frame rate	60fps at 1920x1088
Maximum bit rate	As specified by MPEG-4 ASP level5
Error detection and concealment	Supported

The decoder of MPEG-4/H.263 has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in MPEG-4 data partitioned stream decoding.

2. MPEG-2/MPEG-1 decoder

The features of MPEG-2/MPEG-1 supported by decoder are shown as Table 10-2.

Table 10-2 MPEG-2/MPEG-1 features

Feature	Decoder support
Input data format	MPEG-2/MPEG-1 elementary video stream
Decoding scheme	Frame by frame(or field by field)

Feature	Decoder support
	Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1920x1088 Step size 16 pixels
Maximum frame rate	60fps at 1920x1088
Maximum bit rate	As specified by MPEG-2 MP high level
Error detection and concealment	Supported

The dataflow of MPEG-2/MPEG-1 is the same of H.264 HW performs entropy decoding as Table 10-9.

10.4.3 VDPU346 feature supported

1. H265/MVC

Table 10-3 Video H.265 decoder features

Feature	Decoder support
Input data format	H265 byte unit stream/MVC stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 Semi-Planar FBC output format
Supported image size	64x64 to 4096x2304 step size 16pixels
Profile/level	Main10 level 5.1
Maximum frame rate	YCbCr 4:2:0 4096x2304 @60fps
Maximum bit rate	800MBPS
Error detection And concealment	Supported

2. H264/MVC

Table 10-4 Video H.264 decoder features

Feature	Decoder support
Input data format	H264byte or NAL unit stream/SVC stream/MVC stream
Decoding scheme	Frame by frame(or field by field) Slice by slice
Output data format	YCbCr 4:0:0 (monochrome) YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:2 semi-planar raster-scan
Supported image size	16x16 to 4096x2304 step size 16 pixels
Profile and Level	Main10 level 5.1
Maximum frame rate	4096x2304 @30fps
Maximum bit rate	-
Error detection And concealment	Supported

3. VP9

Table 10-5 Video H.265 decoder features

Feature	Decoder support
Input data format	VP9 byte unit stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 Semi-Planar FBC output format
Supported image size	64x64 to 4096x2304

Feature	Decoder support
	step size 16pixels
Profile/level	Profile0/2 level5.1
Maximum frame rate	YCbCr 4:2:0 4096x2304 @60fps
Maximum bit rate	-
Error detection And concealment	Supported

10.4.4 VDPU346 Config Register Linked List Pointer mode(LLP mode)

VDPU346 Video decoder support link table mode to improve decoder continuity and reduce CPU participate and interrupt response time. In this mode, the register which used for config will be prepare into DDR, after that user enable link table mode, and then our decoder will fetch the register config information through AXI bus frame by frame. On link table mode, the decoder will auto finish all the frame decoder which be prepared in DDR, and not need CPU participate.

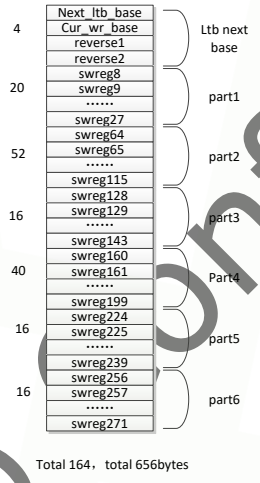


Fig. 10-9 Link table register prepare in DDR format

As show in the above Fig, Link table register prepare in DDR format, each frame config information need 656bytes in DDR. When Link table register work mode be actived,MMU should be config in first,and then parpare register to ddr,at last to config LLP ctrl register to start decoder.

After hardware decoder one frame, will write back some information to DDR where the write back base address is current config storage addr base. All the write back information are listed in the follows table.

Table 10-6 Link table write back register

offset	Description
0x0	swreg224_sta_int
0x4	swreg225_sta_err_info
0x8	swreg226_sta_cabac_error_status
0xc	swreg227_sta_colmv_error_ref_picidx
0x10	swreg228_sta_cabac_error_ctu_offset
0x14	swreg229_sta_saowr_ctu_offset

offset	Description
0x18	swreg230_sta_slice_dec_num
0x1c	swreg231_sta_frame_error_ctu_num
0x20	swreg232_sta_error_packet_num
0x24	swreg233_sta_err_ctu_num_in_ro
0x28	swreg258_debug_perf_rd_max_latency_num
0x2c	swreg259_perf_rd_latency_samp_num
0x30	swreg260_debug_perf_rd_latency_acc_sum
0x34	swreg261_debug_perf_rd_axi_total_byte
0x38	swreg262_debug_perf_wr_axi_total_byte
0x3c	swreg263_debug_perf_working_cnt
0x40	assign info_data0[31:0] = {8'h0,dec_sw_ctu_num[23:0]};
0x44	assign info_data1[31:0] = inter_sw_reflst_idx_use[31:0];
0x48	assign info_data2[31:0] = {12'h0,inter_sw_pu_cnt_sum[19:0]};
0x4c	assign info_data3[31:0] = {inter_sw_mv_y_min_out[15:0],inter_sw_mv_x_min_out[15:0]};
0x50	assign info_data4[31:0] = {inter_sw_mv_y_max_out[15:0],inter_sw_mv_x_max_out[15:0]};
0x54	assign info_data5[31:0] = inter_sw_mv_x_out_sum[31:0];
0x58	assign info_data6[31:0] = inter_sw_mv_y_out_sum[31:0];
0x5c	assign info_data7[31:0] = inter_sw_mv_x_out_abs_sum[31:0];
0x60	assign info_data8[31:0] =

offset	Description
	inter_sw_mv_y_out_abs_sum[31:0];
0x64	assign info_data9[31:0] = {{(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_y_out_abs_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_x_out_abs_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1:32]};
0x68	assign info_data10[31:0] = {16'h0,cu8x8_skip_num[15:0]};
0x6c	assign info_data11[31:0] = {{(32-TU_SKIP_SUM_WIDTH){1'b0}},tu_skip_sum[TU_SKIP_SUM_WIDTH-1:0]};
0x70	assign info_data12[31:0] = {8'b0,1'b0,cr_qp_max[6:0],1'b0,cb_qp_max[6:0],1'b0,luma_qp_max[6:0]};
0x74	assign info_data13[31:0] = {8'b0,1'b0,cr_qp_min[6:0],1'b0,cb_qp_min[6:0],1'b0,luma_qp_min[6:0]};
0x78	assign info_data14[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},luma_qp_sum[QP_SUM_WIDTH-1:0]};
0x7c	assign info_data15[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},cb_qp_sum[QP_SUM_WIDTH-1:0]};
0x80	assign info_data16[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},cr_qp_sum[QP_SUM_WIDTH-1:0]};
0x84	assign info_data17[31:0] = {12'd0,inter_sw_mv_x_pu_cnt_sum[19:0]};
0x88	assign info_data18[31:0] = {12'd0,inter_sw_mv_y_pu_cnt_sum[19:0]};
0x8c	swreg274_sta_ pix_range_y
0x90	swreg275_sta_ pix_range_u

offset	Description
0x94	swreg276_sta_ pix_range_v

The base address of config link table mode is RKVDEC_BASE+0x100.

10.4.5 VDPU346 Qos mode

In VDPU34X hardware, we support QOS mode, in this mode, we can request high priority to fetch data, you can control QOS work by config swreg270 and swreg271.For more detail, you can see the register description.
User should accord to the soc system to select appropriate level.

10.4.6 VDPU346 Error Processing

1. Error types

Table 10-7 VDPU346 Error Types

Error type	Description
timeout error	The VDPU34X IP will monitor if it was always be hold on idle state,and if it stay on IDLE too much long times, will give timeout error.
bus error	It will detect the axi data read and write,if there have any error happened, if it done, it will give bus error.
refer frame error	If the reference frame required by the decoder which is invalid, the hardware will give reference frame error.
stream error	If the stream meet some error, such as stream packet loss, some syntax elements value are irrationality, it will give an stream error.
mmu page fault	If the mmu page is not ready, but used by decoder, the decoder will give an mmu page fault interrupt, and after that, the software should go to prepare the missing mmu page on DDR and config hardware continue to decoder.
LLP work error	If any error happened when LLP work mode be actived, the decoder will stop next frame decoding, and then give an error interrupt, wait soft to process.

The decoder should need to be reset no matter what error types be detected. For decoder reset,it have two reset mode,you can let hardware reset itself if any error happened, or you also can select use software to config cru reset, you can config swreg2[23] to select the mode.

10.4.7 VDPU346 Decoder Output Frame Buffer Size Requested

We define variables ceilM(N) as follows:

$$\text{ceil(M,N)}=ceilM(N)=((N+M-1)/M)*M$$

1）. LLP register buffer size
For LLP work mode, LLP register buffer will be required. Every frame will require 512 byte DDR space. Then, buffer size calculate formula be defined as follows:

$$LLP\_register\_buffer\_size=frame\_num*512byte$$

There frame_num is the number of frame will be prepare in DDR when work on LLP mode.
2). Output frame decoder buffer size
If output select YCbCr 4:2:0 semi-planar raster-scan format, you can use follows formula to calculate the decoder frame buffer size.

$$luma\_frame\_buffer\_size=y\_vir\_hor\_stride*pic\_h*bit\_depth\_y/8$$

$$chroma\_frame\_buffer\_size=uv\_vir\_hor\_stride*(pic\_h/2)*bit\_depth\_c/8$$

$$frame\_buffer\_size=luma\_frame\_buffer\_size+chroma\_frame\_buffer\_size$$

There:

- y_vir_hor_stirde: The virtual stride of luma, it must should more bigger than picture width
- uv_vir_hor_stride: The virtual stride of chroma, it must should more big than picture width for YCbCr 4:2:0
- bit_depth_y/c: Main10 or main, its value will be 10 or 8

Second, if FBC format be selected,you can use follows formula to calculate the decoder

frame buffer size.

$$fbc\_head\_buffer\_size = vir\_hor\_fbc\_head * (pic\_h + 19) / 16$$

$$payload\_buffer\_size = ceil64(pic\_w) * (ceil64(pic\_h) + 16)$$

$$max\_fbc\_buffer\_size = fbc\_head\_buffer\_size + payload\_buffer\_size$$

There:

- vir_hor_fbc_head:the horizontal virtual stride of fbc head,its valud should more bigger than $ceil64(pic\_w)/16$.

But payload real buffer size space used will less than payload_buffer_size,it will according to FBC compress rate.

3). Output frame colmv buffer size

If colmv compress be disabled, you can use follows formula to calculate the decoder frame buffer size.

Table 10-8 Colmv uncompress info

Format	Colmv_size	Colmv space(bytes unit)
h264	4x4	8
hevc	16x16	16
vp9	8x8	16
avs2	16x16	8

So, the colmv uncompress size is:

$$colmv\_buffer\_size0 = (ceil64(pic\_w) * ceil64(pic\_h) / (colmv\_size * colmv\_size)) * colmv\_bytes$$

The buffer size unit is byte unit.

If colmv compress be active, you can use follows formula to calculate the decoder frame buffer size.

segment_w = (64 * colmv_size * colmv_size) / ctu_size

segment_h = ctu_size

pic_w_align = *ceil*(pic_w, segment_w)

pic_h_align = *ceil*(pic_h, segment_h)

seg_cnt_w=pic_w_align/segment_w

seg_cnt_h=pic_h_align/segment_h

segment_head_line_size=ceil（seg_cnt_w,16）

seg_head_size=segment_head_line_size*seg_cnt_h

seg_payload_size=seg_cnt_w*seg_cnt_h*64*colmv_bytes

colmv_compress_size=seg_head_size+seg_payload_size

where:

- *c*tu_*size*:*ct*u size;
- colmv_size：the block size for each colmv
- colmv_bytes：each colmv space used

4). Error info buffer size

If error infomation be enable write to DDR, the error info buffer size will be required, and we can use the follows formula to calculate the error info buffer size.

$$error\_info\_buffer\_size = ceil2(slice\_num) * 8$$

only h264 and h265 support error info output.

10.4.8 VDPU346 Decoder temporary Buffer Size Requested

The temporary buffer only used when VDPU346 on working status.The data write to temporary buffer size is row and col buffer data,we suggest row buffer used internal sram buffer will enhance the decoder performance.

Row buffer and Col buffer size require are listed as fellows.

Table 10-9 Row or Col buffer size required

data type	required condtion	buffer size
Inter Row	H.265/H.264/VP9	6*pic_width
	H.264,mbaff	6*pic_width

data type	required condtion	buffer size
Recon Row	H.265/H.264,not mbaff/VP9	3* pic_width
Dblk Row	H.265	9*pic_width
	H.264	16*pic_width
	VP9	22* pic_width
Sao Row	H.265	4* pic_width
Fbc Row	H.264	3* pic_width
	VP9	10* pic_width
Inter Col	H.265/VP9, have col tile	3* pic_height
Filterd Col	H.265,have col tile	36* pic_height
	VP9,have col tile	31* pic_height

10.4.9 VDPU720 feature supported

1. JPEG Decoder
JPEG features supported by decoder are as shown in Table 10-10.

Table 10-10 JPEG features

Feature	Decoder support
Input data format	JFIF file format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Decoding scheme	frame by frame
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Supported image size	48x48 to 65536x65536(4295Mpixels) Step size 8 pixels
Maximum frame rate	Up to 240 million pixels pre second
Thumbnail decoding	JPEG compressed thumbnails supported
Restart marker frequency decoding	Supported
MJPEG	Supported
Error detection	Supported

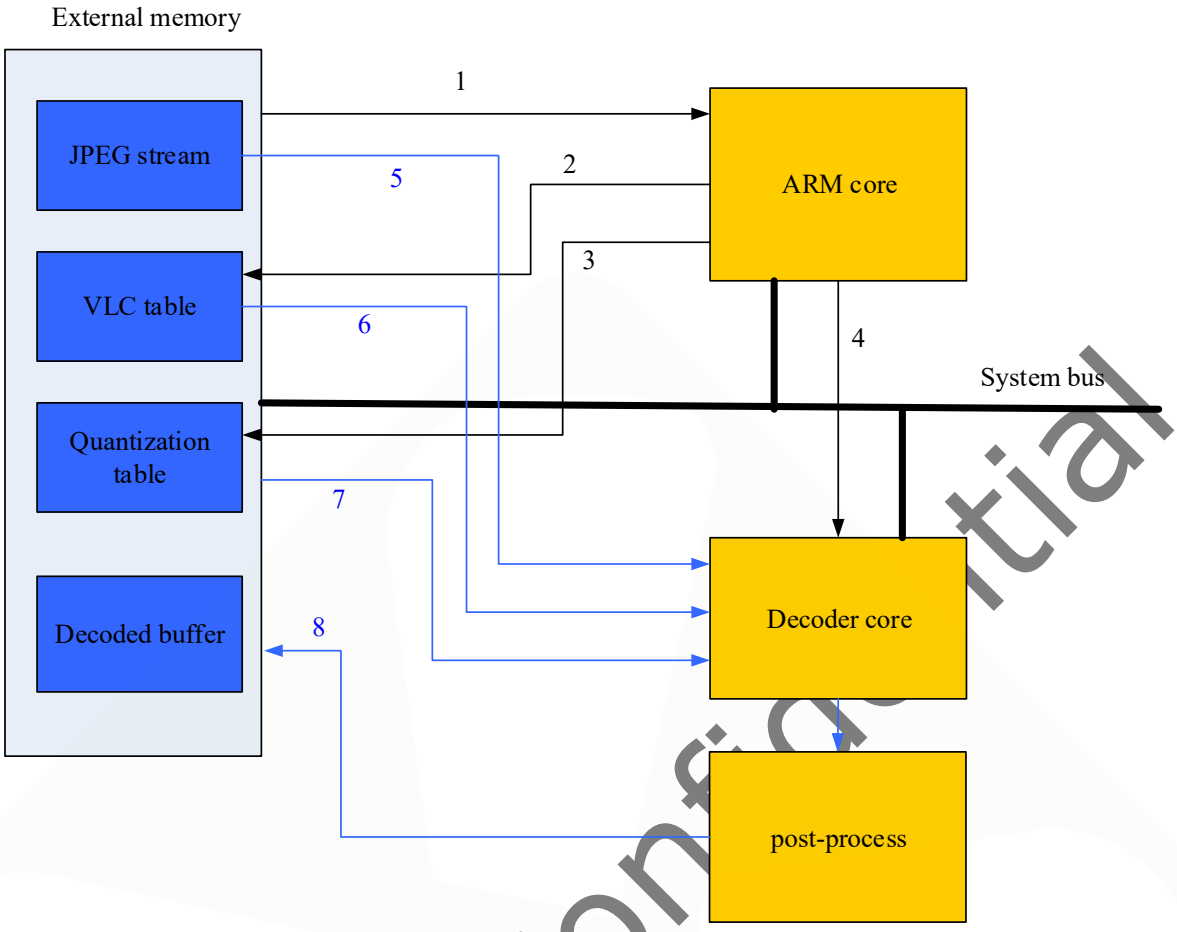


Fig. 10-10 The dataflow of JPEG decoder and post-processor

The data flow of jpeg decoder is as Fig. 10-10 shown. The decoder software starts decoding the picture by parsing the stream headers (1) and then writes the following items to external memory:
VLC tables (2)
Quantization tables (3)
Last step for the software is to write the hardware control registers and to enable the hardware (4). After starting hardware, SW waits interrupt from HW.
Hardware decodes the picture by reading stream (5), VLC (6) and QP (7) tables. Hardware writes the decoded output picture memory one macroblock at a time (8). When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.
The follow image post-processor only support combined mode.

2. Image Post-processor
The features supported by Post-processor are as show in Table 10-11.

Table 10-11 Post-processor features

Feature	Post-processor support
Input data format	Any format generated by the decoder in combined mode YCbCr 4:2:0 semi-planar YCbCr 4:2:0 planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2

Feature	Post-processor support
Post-processor scheme	Frame by frame. Post-processor handles the image macroblock by macroblock.
Input image source	Internal source
Output data format	YCbCr 4:2:0 semi-planar YCbCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2 Fully configurable RGB channel lengths and locations inside 24 bits, e.g. RGB 24-bit (8-8-8), RGB 16-bit(5-6-5).
Input image size	48x48 to 65536x65536 Step size 8 pixels
Output image size	16x16 to 65536x65536 Horizontal step size 1 Vertical step size 1
Image down-scaling	Proprietary averaging filter Arbitrary, integer scaling ratio separately for both dimensions 0/2/4/8 down-scaling ratio
YCbCr to RGB color conversion	BT.601 compliant BT.709 compliant User definable conversion coefficient
Dithering	2x2 ordered spatial dithering for 4,5 and 6 bit RGB channel precision
Output picture	support raster or tile mode picture out luma 8x8 block tile

In pipe-line mode, the post-processor works together with the multi-format decoder. The PP will take its input directly from the decoder. The dataflow is as Fig. 10-11 show.

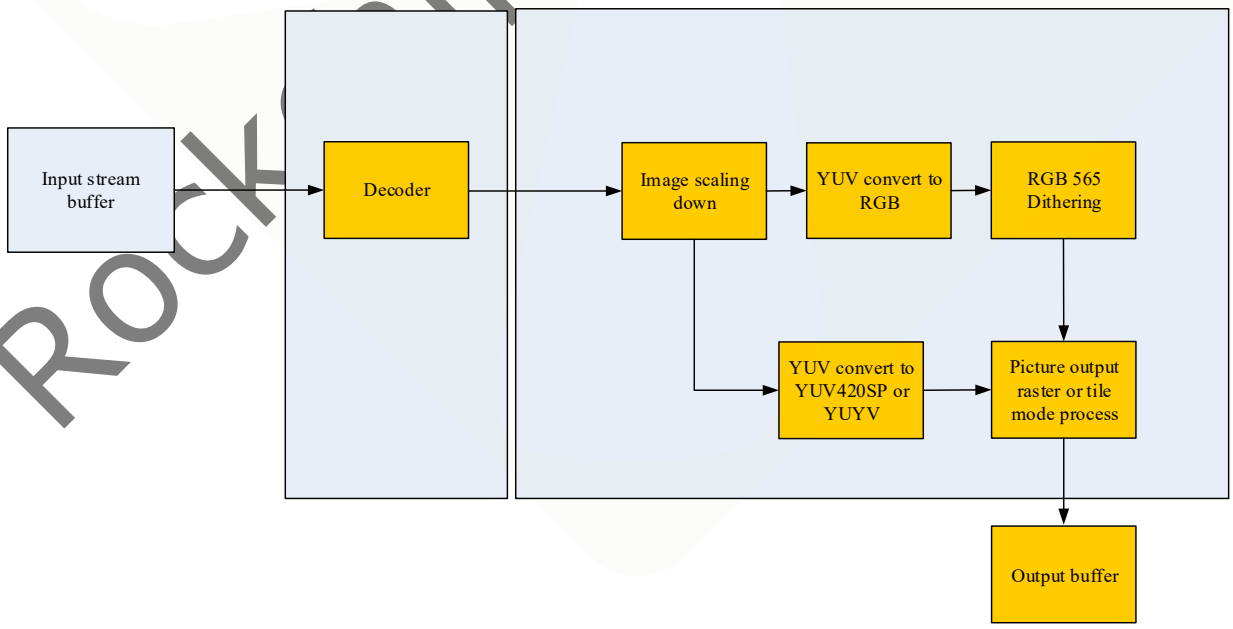


Fig. 10-11 Post-process Dataflow

10.4.10 VEPU121 feature supported

1. JPEG encoder

The JPEG features supported by encoder are shown as follows.

Table 10-12 Video Jpeg encoder feature

Feature	Encoder support
Input data format	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbYCr 4:2:2① CbYCrY 4:2:2 Interleaved① RGB formats:① RGB444 to BGR444 RGB555 to BGR555 RGB565 to BGR565 RGB888 to BRG888 RGB101010 and BRG 101010
Output data format	JFIF FILE format 1.02 Non-progressive JPEG
Supported image size	96x96 to 8192x8192(64 million pixels) Step size 4 pixels
Maximum Data rate	Up to 90 million pixels per second

①internally encoder handles image only in 4:2:0 format

1.4.10 VEPU540 H.264 or HEVC Encoding

VEPU can perform one frame H.264 or HEVC encoding by register configuration. User should allocate DDR buffer, configure VEPU through AHB slave port, and then wait for frame finish interrupt.

VEPU also have batch processing mode (the so called link-table mode). User should configure the link table node in DDR, start VEPU, and then wait for frame or sequence finish. User can also add new frames to be encoded while VEPU is processing the previous one.

1.4.11 VEPU540 Video Source Pre-process

VEPU can read video source of different color formats such as ARGB, RGB, YUV422/420 P/SP, and Arm AFBC YUV422/420. It also supports image clipping, rotation, mirror and OSD insertion.

1.4.12 VEPU540 ROI Configuration

User can configure QP and I/P selection for each 16x16 block through VEPU ROI configuration.

10.5 Register Description

10.5.1 Internal Address Mapping

This section describes the control/status registers of the codec.

If VDPU121 decoder is chosen to work, the register base address is VDPU121_base.
If VDPU346 decoder is chosen to work, the register base address is VDPU346_base.
If VDPU720 decoder is chosen to work, the register base address is VDPU720_base.
If VEPU121 encoder is chosen to work, the register base address is VEPU121_base.
If VEPU540 encoder is chosen to work, the register base address is VEPU540_base.
All the register config base are listed as follows:

Table 10-13 Base address of config

Config Register	Base addr
VDPU121 function config base	VDPU121_base
VDPU121 mmu config base	VDPU121_base+0x400
VDPU346 link table config base	VDPU346_base+0x100
VDPU346 function config base	VDPU346_base+0x200
VDPU346 cache config base	VDPU346_base+0x700 for luma channel VDPU346_base+0x740 for chroma channel

Config Register	Base addr
VDPU346 mmu config base	VDPU346_base+0x800 for read channel VDPU346_base+0x840 for write channel
VDPU720 function config base	VDPU720_base
VDPU720 mmu config base	VDPU720_base+0x480
VDPU720 link table config base	VDPU720_base+0x300
VEPU121 function config base	VEPU121_base
VEPU121 mmu config base	VEPU121_base+0x800
VEPU540 function config base	VEPU540_base
VEPU540 mmu config base	VEPU540_base+0xF00

Table 10-14 Base address value

Base addr	value
VDPU121_base	0xFDEA_0400
VDPU346_base	0xFDF8_0000
VDPU720_base	0xFDED_0000
VEPU121_base	0xFDEE_0000
VEPU540_base	0XFDF4_0000

10.5.2 VDPU121 Registers Summary

Name	Offset	Size	Reset Value	Description
VDPU_SWREG0_NEW_VERSION	0x0000	W	0x03680000	ID register(read only)when vpu share memory with hevc, this register is not be used.
VDPU_SWREG0	0x0000	W	0x00000000	Register0000 Description
VDPU_SWREG1	0x0004	W	0x00000000	Interrupt register decoder
VDPU_SWREG2	0x0008	W	0x01000400	Device configuration register decoder
VDPU_SWREG3	0x000c	W	0x00000001	Device control register 0 (decode, picture type etc)
VDPU_SWREG4_H264	0x0010	W	0x00000000	Decoder control register 1 (picture parameters)
VDPU_SWREG4	0x0010	W	0x00000000	Decoder control register 1(picture parameters)
VDPU_SWREG5	0x0014	W	0x00000000	Decoder control register2 (stream decoding table selects)
VDPU_SWREG5_H264	0x0014	W	0x00000000	Decoder control register2 (stream decoding table selects)
VDPU_SWREG6	0x0018	W	0x00000000	Decoder control register 3 (stream buffer information)
VDPU_SWREG7	0x001c	W	0x00000000	Decoder control register 4 (H264, VC-1 control)

Name	Offset	Size	Reset Value	Description
VDPU_SWREG8	0x0020	W	0x00000000	Decoder control register 5(H264, VC-1 control)
VDPU_SWREG9	0x0024	W	0x00000000	Base address for MB-control (RLC) /VC-1 intensity control 0.
VDPU_SREG10_H264_RLC	0x0028	W	0x00000000	Base address for differential motion vector base address (RLC-mode)/H264 P initial fwd ref pic list register(4-9)/ VC-1 intensity control 1.
VDPU_SREG10_H264	0x0028	W	0x00000000	Base address for differential motion vector base address (RLC-mode)/H264 P initial fwd ref pic list register(4-9)/VC-1 intensity control 1.
VDPU_SWREG11_H264_RLC	0x002c	W	0x00000000	Base address for H.264 intra prediction 4x4/base address for MPEG-4 DC component (RLC)/H264 P initial fwd ref pic list register(10-15)/VC-1 intensity control 2
VDPU_SWREG11_H264	0x002c	W	0x00000000	Base address for H.264 intra prediction 4x4/base address for MPEG-4 DC component (RLC)/H264 P initial fwd ref pic list register(10-15)/VC-1 intensity control 2
VDPU_SWREG12	0x0030	W	0x00000000	Base address for RLC data (RLC)/ stream start address/decoded end addr register (VLC)
VDPU_SWREG13	0x0034	W	0x00000000	Base address for decoded picture/ base address for JPEG decoder output luminance picture
VDPU_SWREG14	0x0038	W	0x00000000	Base address for reference picture index 0/base address for JPEG decoder output chrominance picture
VDPU_SWREG15_JPEG_ROI	0x003c	W	0x00000000	JPEG roi control
VDPU_SWREG15	0x003c	W	0x00000000	Base address for reference picture index 1/JPEG control

Name	Offset	Size	Reset Value	Description
VDPU_SWREG16	0x0040	W	0x00000000	Base address for reference picture index 2/List of VLC code lengths in first JPEG AC table
VDPU_SWREG17	0x0044	W	0x00000000	Base address for reference picture index 3/List of VLC code lengths in first JPEG AC table
VDPU_SWREG18	0x0048	W	0x00000000	Base address for reference picture index 4/VC1 control/MPEG4 MVD control/List of VLC code lengths in first JPEG AC table/VC-1 intensity control 4.
VDPU_SWREG19	0x004c	W	0x00000000	Base address for reference picture index 5/MPEG4 TRB/TRD delta 0/VC-1 intensity control 3 List of VLC code lengths in first/second JPEG AC table.
VDPU_SWREG20	0x0050	W	0x00000000	Base address for reference picture index 6/MPEG4 TRB/TRD delta -1/List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits.
VDPU_SWREG21	0x0054	W	0x00000000	Base address for reference picture index 7/MPEG4 TRB/TRD delta 1 / List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits.
VDPU_SWREG22	0x0058	W	0x00000000	Base address for reference picture index 8/List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits.
VDPU_SWREG23	0x005c	W	0x00000000	Base address for reference picture index 9 / List of VLC code lengths in first JPEG DC table. Note: The h264 decoder will use these bits.
VDPU_SWREG24	0x0060	W	0x00000000	Base address for reference picture index 10/List of VLC code lengths in first JPEG DC table. Note: The h264 decoder will use these bits.

Name	Offset	Size	Reset Value	Description
VDPU_SWREG25	0x0064	W	0x00000000	Base address for reference picture index 11/List of VLC code lengths in second JPEG DC table. Note: The h264 decoder will use these bits.
VDPU_SWREG26	0x0068	W	0x00000000	Base address for reference picture index 12/list of VLC code lengths in second JPEG DC table. Note: The h264 decoder will use these bits.
VDPU_SWREG27	0x006c	W	0x00000000	Base address for reference picture index 13/VC-1 bitpl mbctrl. Note: the h264 decoder will use these bits.
VDPU_SWREG28	0x0070	W	0x00000000	Base address for reference picture index14. Note: The h264 decoder will use these bits.
VDPU_SWREG29	0x0074	W	0x00000000	Base address for reference picture index15. Note: The h264 decoder will use these bits.
VDPU_SWREG30	0x0078	W	0x00000000	Reference picture numbers for index 0 and 1 (H264 VLC).
VDPU_SWREG31	0x007c	W	0x00000000	Reference picture numbers for index 2 and 3 (H264 VLC).
VDPU_SWREG32	0x0080	W	0x00000000	Reference picture numbers for index 4 and 5 (H264 VLC).
VDPU_SWREG33	0x0084	W	0x00000000	Reference picture numbers for index 6 and 7 (H264 VLC).
VDPU_SWREG34	0x0088	W	0x00000000	Reference picture numbers for index 8 and 9 (H264 VLC)/MPEG4, VC1 prediction filter taps
VDPU_SWREG35_JPEG_ROI	0x008c	W	0x00000000	JPEG roi offset/dc base address
VDPU_SWREG35	0x008c	W	0x00000000	Reference picture numbers for index 10 and 11 (H264 VLC)/VC1 prediction filter taps

Name	Offset	Size	Reset Value	Description
VDPU_SWREG36	0x0090	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps
VDPU_SWREG36_JPEG_ROI	0x0090	W	0x00000000	JPEG roi offset/dc length
VDPU_SWREG37	0x0094	W	0x00000000	Reference picture numbers for index 14 and 15 (H264 VLC).
VDPU_SWREG38	0x0098	W	0x00000000	Reference picture long term flags (H264 VLC).
VDPU_SWREG38_H264	0x0098	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps
VDPU_SWREG39	0x009c	W	0x00000000	Reference picture valid flags (H264 VLC).
VDPU_SWREG39_H264	0x009c	W	0x00000000	Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps
VDPU_SWREG40	0x00a0	W	0x00000000	Base address for standard dependent tables
VDPU_SWREG41	0x00a4	W	0x00000000	Base address for direct mode motion vectorsNote: The h264 decoder will use these bits.
VDPU_SWREG42	0x00a8	W	0x00000000	Bi_dir initial ref pic list register (0-2). Note: The h264 decoder will use these bits.
VDPU_SWREG43	0x00ac	W	0x00000000	Bi-dir initial ref pic list register (3-5). Note: The h264 decoder will use these bits.
VDPU_SWREG44	0x00b0	W	0x00000000	Bi-dir initial ref pic list register (6-8). Note: The h264 decoder will use these bits.
VDPU_SWREG45	0x00b4	W	0x00000000	Bi-dir initial ref pic list register (9-11). Note: The h264 decoder will use these bits.
VDPU_SWREG46	0x00b8	W	0x00000000	Bi-dir initial ref pic list register (12- 14). Note: The h264 decoder will use these bits.

Name	Offset	Size	Reset Value	Description
VDPU_SWREG47	0x00bc	W	0x00000000	Bi-dir and P fwd initial ref pic list register (15 and P 0-3). Note: The h264 decoder will use these bits.
VDPU_SWREG48	0x00c0	W	0x00000000	Error concealment register
VDPU_SWREG49	0x00c4	W	0x00000000	Prediction filter tap register for H264, MPEG4, VC1
VDPU_SWREG50	0x00c8	W	0xfbb56f80	Synthesis configuration register decoder 0 (read only)
VDPU_SWREG51	0x00cc	W	0x00000000	Reference picture buffer control register
VDPU_SWREG52	0x00d0	W	0x00000000	Reference picture buffer information register 1 (read only)
VDPU_SWREG53	0x00d4	W	0x00000000	Reference picture buffer information register 2 (read only)
VDPU_SWREG54	0x00d8	W	0xe5da0000	Synthesis configuration register decoder 1 (read only)
VDPU_SWREG55	0x00dc	W	0x00000000	Reference picture buffer 2/Advanced prefetch control register
VDPU_SWREG56	0x00e0	W	0x00000000	Reference buffer information register 3 (read only)
VDPU_SWREG57_INTRA_INTER	0x00e4	W	0x00000000	Intra_dll3t,intra_dblspeed, inter_dblspeed, stream_len_hi
VDPU_SWREG57	0x00e4	W	0x00000000	Intra_dll3t,intra_dblspeed, inter_dblspeed, stream_len_hi
VDPU_SWREG58	0x00e8	W	0x00000000	Decoder debug register 0 (read only)
VDPU_SWREG59	0x00ec	W	0x00000000	H264 Chrominance 8 pixel interleaved data base
VDPU_SWREG60	0x00f0	W	0x00000000	Interrupt register post-processor
VDPU_SWREG61	0x00f4	W	0x01010100	Device configuration register post-processor
VDPU_SWREG62	0x00f8	W	0x00000000	Deinterlace control register

Name	Offset	Size	Reset Value	Description
VDPU_SWREG63	0x00fc	W	0x00000000	Base address for reading post-processing input picture uminance (top field/frame)
VDPU_SWREG64	0x0100	W	0x00000000	Base address for reading post-processing input picture Cb/Ch (topfield/frame)
VDPU_SWREG65	0x0104	W	0x00000000	Base address for reading post-processing input picture Cr
VDPU_SWREG66	0x0108	W	0x00000000	Base address for writing post-processed picture luminance/RGB
VDPU_SWREG67	0x010c	W	0x00000000	Base address for writing post-processed picture Ch
VDPU_SWREG68	0x0110	W	0x00000000	Register for contrast adjusting
VDPU_SWREG69	0x0114	W	0x00000000	Register for colour conversion and contrast adjusting
VDPU_SWREG70	0x0118	W	0x00000000	Register for colour conversion 0
VDPU_SWREG71	0x011c	W	0x00000000	Register for colour conversion 1 + rotation mode
VDPU_SWREG72	0x0120	W	0x00000000	PP input size and cropping register
VDPU_SWREG73	0x0124	W	0x00000000	PP input picture base address for Y bottom field
VDPU_SWREG74	0x0128	W	0x00000000	PP input picture base for Ch bottom field
VDPU_SWREG79	0x013c	W	0x00000000	Scaling ratio register 1 & padding for B
VDPU_SWREG80	0x0140	W	0x00000000	Scaling register 0 ratio & padding for R and G
VDPU_SWREG81	0x0144	W	0x00000000	Scaling ratio register 2
VDPU_SWREG82	0x0148	W	0x00000000	Rmask register
VDPU_SWREG83	0x014c	W	0x00000000	Gmask register
VDPU_SWREG84	0x0150	W	0x00000000	Bmask register

Name	Offset	Size	Reset Value	Description
VDPU_SWREG85	0x0154	W	0x00000000	Post-processor control register
VDPU_SWREG86	0x0158	W	0x00000000	Mask 1 start coordinate register
VDPU_SWREG87	0x015c	W	0x00000000	Mask 2 start coordinate register
VDPU_SWREG88	0x0160	W	0x00000000	Mask 1 size and PP original width register
VDPU_SWREG89	0x0164	W	0x00000000	Mask 2 size register
VDPU_SWREG90	0x0168	W	0x00000000	PiP register 0
VDPU_SWREG91	0x016c	W	0x00000000	PiP register 1 and dithering control
VDPU_SWREG92	0x0170	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG93	0x0174	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG94	0x0178	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG95	0x017c	W	0x00000000	Base address for alpha blend 2 gui component
VDPU_SWREG98	0x0188	W	0x00000000	PP outupt width/height extension
VDPU_SWREG99	0x018c	W	0xe000f000	PP fuse register (read only)
VDPU_SWREG100	0x0190	W	0xff874780	Synthesis configuration register post-processor (read only)
VDPU_SWREG101	0x0194	W	0x00000000	Soft reset signals
VDPU_SWREG103	0x019c	W	0x00000000	Axi ddr rdata num, the unit is byte
VDPU_SWREG104	0x01a0	W	0x00000000	Vdpu write data byte num
VDPU_SWREG105	0x01a4	W	0x00000000	Monitor signal sellected
VDPU_SWREG106	0x01a8	W	0x00000000	Performance montor cnt0
VDPU_SWREG107	0x01ac	W	0x00000000	Performance montor cnt1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.3 VDPU121 Detail Registers Description

VDPU_SWREG0_NEW_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:24	RO	0x3	Major_version 1'b0: 1080p support 1'b1: 2160p support
23:16	RO	0x68	Minor_version 0: Audis 1: Audi 2: Maybach 3: Audib FF: Share memory with hevc, so should read version from hevc register
15:0	RW	0x0000	Build The rtl's svn num in ic server

VDPU_SWREG0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Pro_num project number
15:12	RW	0x0	Major_version Major version
11:4	RW	0x00	Minor_version Minor version
3	RW	0x0	ID_ASCII_EN ASCII type product ID enable
2:0	RW	0x0	Build_version Build version

VDPU_SWREG1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	Reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	Sw_dec_pic_inf B slice detected. This signal is driven high during picture ready interrupt if B-type slice is found. This bit does not launch interrupt but is used to inform SW about h264 tools. Note: The h264 decoder will use these bits.
23:19	RO	0x00	Reserved
18	RW	0x0	Sw_dec_timeout Interrupt status bit decoder timeout. When high the decoder 0 has been idling for too long. HW will self reset. Possible only if timeout interrupt is enabled. Note: The h264 decoder will use these bits.
17	RW	0x0	Sw_dec_slice_int Interrupt status bit dec_slice_decoded. When high SW must set new base addresses for Sw_dec_out_base and. Sw_jpg_ch_out_base before reseting this status bit. Used for JPEG snapshot modes. Note: The JPEG decoder will use these bits.
16	RW	0x0	Sw_dec_error_int Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. Note: The h264 decoder will use these bits.
15	RW	0x0	Sw_dec_aso_int Interrupt status bit ASO (Arbitrary Slice Ordering) detected.When high, ASO detected in input data stream decoding. HW will self reset. Note: The h264 decoder will use these bits.
14	RW	0x0	Sw_dec_buffer_int Interrupt status bit input buffer empty. When high, Input stream buffer is empty but picture is not ready. HW will not self reset. Note: The h264 decoder will use these bits.
13	RW	0x0	Sw_dec_bus_int Interrupt status bit bus. Error response from bus. HW will self reset. Note: The h264 decoder will use these bits.
12	RW	0x0	Sw_dec_rdy_int Interrupt status bit decoder. When this bit is high decoder has decoded a picture. HW will self reset. Note: The h264 decoder will use these bits.
11:9	RO	0x0	Reserved
8	RW	0x0	Sw_dec_irq Decoder IRQ. When high, decoder requests an interrupt. SW will reset this after interrupt is handled. Note: The h264 decoder will use these bits.
7:5	RO	0x0	Reserved
4	RW	0x0	Sw_dec_irq_dis Decoder IRQ disable. When high, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt statuses. Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
3:1	RO	0x0	Reserved
0	RW	0x0	Sw_dec_en Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or ASO or stream error is detected or bus error or timeout interrupt is given. Note: The h264 decoder will use these bits.

VDPU_SWREG2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	Sw_dec_axi_rd_id Read ID used for decoder reading services in AXI bus (if connected to AXI). Note: The h264 decoder will use these bits.
23	RW	0x0	Sw_dec_timeout_e Timeout interrupt enable. If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. Note: The h264 decoder will use these bits.
22	RW	0x0	Sw_dec_strswap32_e Decoder input 32bit data swap for stream data (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)). Note: The h264 decoder will use these bits.
21	RW	0x0	Sw_dec_strendian_e Decoder input endian mode for stream data: 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order) Note: The h264 decoder will use these bits.
20	RW	0x0	Sw_dec_inswap32_e Decoder input 32bit data swap for other than stream data (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) Note: The h264 decoder will use these bits.
19	RW	0x0	Sw_dec_outswap32_e Decoder output 32bit data swap (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)). Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
18	RW	0x0	Sw_dec_data_disc_e Data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally. Note: The h264 decoder will use these bits.
17	RW	0x0	sw_tiled_mode_msb Tiled mode msb. Concanated to Tiled mode lsb which form 2 bit tiled mode. Definition of tiledmode: 2'd0: Tiled mode not enabled 2'd1: Tiled mode enabled for 8x4 tile size 2'd2, 2'd3: Reserved Note: The h264 decoder will use these bits.
16:11	RW	0x00	Sw_dec_latency Decoder master interface additional latency. Can be used to slow down decoder HW between services in steps of 8 clock cycles: 6'd0: No latency 6'd1: Minimum 8 cycles of IDLE between services 6'd2: Minimum 16 cycles of IDLE between services ... 6'd63: Minimum latency of 504 cycles of IDLE between services Note: The h264 decoder will use these bits.
10	RW	0x1	Sw_dec_clk_gate_e Decoder dynamic clock gating enable: 1'b0: Clock is running for all structures 1'b1: Clock is gated for decoder structures that are not used Note: Clock gating value can be changed only when decoder is disabled.
9	RW	0x0	Sw_dec_in_endian Decoder input endian mode for other than stream data: 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order) Note: The h264 decoder will use these bits.
8	RW	0x0	Sw_dec_out_endian Decoder output endian mode: 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order) Note: The h264 decoder will use these bits.
7	RW	0x0	Sw_tiled_mode_lsb Tiled mode lsb. Concatenated to Tiled mode msb which form 2 bit tiled mode. Defined in tiled_mode_msb. Note: The h264 decoder will use these bits.
6	RW	0x0	Sw_dec_adv_pre_dis Advanced PREFETCH mode disable (advanced reference picture reading mode for video). Note: The h264 decoder will use these bits.
5	RW	0x0	Sw_dec_scmd_dis AXI Single Command Multiple Data 0 disable. (where only the first addresses of the burst are given from address generator). This bit is used to disable the feature (possible SW workaround if something is not working correctly). Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
4:0	RW	0x00	Sw_dec_max_burst Maximum burst length for decoder bus transactions. Valid values: AXI: 1-16 Note: The h264 decoder will use these bits.

VDPU_SWREG3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Sw_dec_mode Decoding mode: 0 = H.264, 1 = MPEG-4, 2 = H.263, 3 = JPEG, 4 = VC-1, 5 = MPEG-2, 6 = MPEG-1, 11 = AVS, Others = reserved Note: All the decoder mode will use these bits.
27	RW	0x0	Sw_rlc_mode_e RLC mode enable: 1'b1: HW decodes video from RLC input data + side information (Differential MV's, separate DC coeffs, Intra 4x4 modes, MB control). Valid only for H.264 Baseline and MPEG- 4 SP. 1'b0: HW decodes video from bit stream (VLC mode) + side information (bitplane data in VC-1). Note: The h264 and MPEG4 decoder will use these bits.
26	RW	0x0	Sw_skip_mode AVS: 1'b0: Special MB type code indicates skipped mbs 1'b1: Means that skipped mbs are indicated using skip_run - syntax element like in
24	RW	0x0	Sw_pjpeg_e Progressive JPEG enable: 1'b0: Baseline JPEG 1'b1: Progressive JPEG
23	RW	0x0	Sw_pic_interlace_e Coding mode of the current picture: 1'b0: Progressive 1'b1: Interlaced Note: The h264 decoder will use these bits.
22	RW	0x0	Sw_pic_fieldmode_e Structure of the current picture (residual structure) 1'b0: Frame structure, this means MBAFF structured picture for interlaced sequence 1 = field structure Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
21	RW	0x0	Sw_pic_b_e B picture enable for current picture: 1'b0: Picture type is I or P depending on sw_pic_inter_e 1'b1: Picture type is BI (vc1)/D (mpeg1) or B depending on sw_pic_inter_e (not valid for H264 since its slice based information)
20	RW	0x0	Sw_pic_inter_e Picture type. 1'b1: Inter type (P) 1'b0: Intra type (I) See also sw_pic_b_e
19	RW	0x0	Sw_pic_topfield_e If field structure is enabled this bit informs which one of the fields is being decoded: 1'b0: Bottom field 1'b1: Top field Note: The h264 decoder will use these bits.
18	RW	0x0	Sw_fwd_interlace_e Coding mode of forward reference picture: 1'b0: Progressive 1'b1: Interlaced Note: For backward reference picture the coding mode is always same as for current picture.
16	RW	0x0	Sw_ref_topfield_e Indicates which field should be used as reference if sw_ref_frames = 0 : 1'b0: Bottom field 1'b1: Top field Used only in VC-1 mode
15	RW	0x0	Sw_dec_out_dis Disable decoder output picture writing: 1'b0: Decoder output picture is written to external memory 1'b1: Decoder output picture is not written to external memory Note: The h264 decoder will use these bits.
14	RW	0x0	Sw_filtering_dis De-block filtering disable 1'b1: Filtering is disabled for current picture 1'b0: Filtering is enabled for current picture Note: The h264 decoder will use these bits.
13	RW	0x0	Sw_pic_fixed_quant Sw_pic_fixed_quant (DEC mode is VC-1 and AVS) 1'b0: Quantization parameter can vary inside picture 1'b1: Quantization parameter is fixed (pquant) Sw_mvc_e(DEC mode is H264) Multi view coding enable. Possible for H264 only Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
12	RW	0x0	Sw_write_mvs_e Direct mode motion vector write enable for current picture / MPEG2 motion vector write enable for error concealment Purposes: 1'b0: Writing disabled for current picture 1'b1: The direct mode motion vectors are written to external Memory. H264 direct mode motion vectors are written to DPB aside with the corresponding reference picture. Other decoding mode dir mode mvs are written to external memory starting from Sw_dir_mv_base. Note: The h264 decoder will use these bits.
11	RW	0x0	Sw_reftopfirst_e Indicates which FWD reference field has been decoded first. 1'b0: FWD reference bottom field 1'b1: FWD reference top field Note: The h264 decoder will use these bits.
10	RW	0x0	Sw_seq_mbaff_e Sequence includes MBAFF coded pictures. Note: The h264 decoder will use these bits.
9	RW	0x0	Sw_picord_count_e H264_high config: Picture order count table read enable. If enabled HW will read picture order counts from memory in the beginning of picture. Note: The h264 decoder will use these bits.
8	RW	0x0	Sw_dec_timeout_mode When 1'b0 , timeout cycle is 181'b1 When 1'b1, timeout cycle is 221'b1 Note: The h264 decoder will use these bits.
7:0	RW	0x01	Sw_dec_axi_wr_id Write ID used for decoder writing services in AXI bus (if connected to AXI). Note: The h264 decoder will use these bits.

VDPU_SWREG4_H264

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15) /16) Note: The h264 decoder will use these bits.
22:19	RO	0x0	Reserved
18:11	RW	0x00	Sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also For single field (of interlaced content) is being decoded Note: The h264 decoder will use these bits.
10:5	RO	0x00	Reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	Sw_ref_frames H.264: Num_ref_frames, maximum number of short and long term reference frames in decoded picture buffer.

VDPU_SWREG4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Sw_pic_mb_width Picture width in macroblocks = ((width in pixels + 15)/16).
22:19	RW	0x0	Sw_mb_width_off The amount of meaningfull horizontal pixels in last MB (width offset) 0 if exactly 16 pixels multiple picture and all the horizontal pixels in last MB are meaningfull.
18:11	RW	0x00	Sw_pic_mb_height_p Picture height in macroblocks =((height in pixels+15)/16). Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded.
10:7	RW	0x0	Sw_mb_height_off The amount of meaningfull vertical pixels in last MB (height offset 0 if exactly 16 pixels multiple picture and all the vertical pixels in last MB are meaningfull.
6	RW	0x0	Sw_alt_scan_e Indicates alternative vertical scan method used for interlaced frames.
5:3	RW	0x0	Sw_pic_mb_w_ext Picture mb width extension. If sw_pic_mb_width does not fit to 9 bits then these bits are used to increase the range up to 11 bits (used as 3 msb).
2:0	RW	0x0	Sw_pic_mb_h_ext Picture mb height extension. If sw_pic_mb_height_p does not fit to 9 bits then these bits are used to increase the range up to 11 bits (used as 3 msb).

VDPU_SWREG5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base).
25	RW	0x0	Sw_sync_marker_e Sync markers enable: 1'b0: Synch markers are not used. 1'b1: Synch markers are used. For progressive JPEG this indicates that there are restart markers in the stream after restart interval steps.

Bit	Attr	Reset Value	Description
24	RW	0x0	Sw_type1_quant_e MPEG4: Type 1 quantization enable 1'b0: Type 2 inverse Q method 1'b1: Type 1 inverse Q method (Q-tables used) H264 (h264_high config), scaling matrix enable: 1'b0: Normal transform 1'b1: Use scaling matrix for transform (read from external
23:19	RW	0x00	Sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	Sw_ch_qp_offset2 Chroma Qp filter offset for cr type.
13:1	RO	0x0000	Reserved
0	RW	0x0	Sw_fieldpic_flag_e Flag for stream that field_pic_flag exists in stream.

VDPU_SWREG5_H264

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Sw_strm_start_bit Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base).
25	RO	0x0	Reserved
24	RW	0x0	Sw_type1_quant_e MPEG4: Type 1 quantization enable 1'b0: Type 2 inverse Q method 1'b1: Type 1 inverse Q method (Q-tables used) H264 (h264_high config), scaling matrix enable: 1'b0: Normal transform 1'b1: Use scaling matrix for transform (read from external
23:19	RW	0x00	Sw_ch_qp_offset Chroma Qp filter offset. (For H.264 this offset concerns Cb only)
18:14	RW	0x00	Sw_ch_qp_offset2 Chroma Qp filter offset for cr type.
13:1	RO	0x0000	Reserved
0	RW	0x0	Sw_fieldpic_flag_e Flag for stream that field_pic_flag exists in stream.

VDPU_SWREG6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_start_code_e Bit for indicating stream start code existence: 1'b0: Stream doesn't contain start codes 1'b1: Stream contains start codes Note: The h264 decoder will use these bits.
30:25	RW	0x00	Sw_init_qp Initial value for quantization parameter (picture quantizer). Note: The h264 decoder will use these bits.
24	RW	0x0	Sw_ch_8pix_ileav_e Enable for additional chrominance data format writing where decoder writes chrominance in group of 8 pixels of Cb and then corresponding 8 pixels of Cr. Data is written to sw_dec_ch8pix_base. Cannot be used if tiled mode is enabled. Note: The h264 decoder will use these bits.
23:0	RW	0x000000	Sw_stream_len Amount of stream data bytes in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (associates with Sw_rlc_vlc_base). For VC-1 the buffer must include data for one picture/slice of the picture. For H264/MPEG4/H263/MPEG2/MPEG1 the buffer must include at least data for one slice/VP of the picture. For JPEG the buffer size must be a multiple of 256 bytes or the amount of data for one picture. Note: The h264 decoder will use these bits.

VDPU_SWREG7

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_cabac_e CABAC enable Note: The h264 decoder will use these bits.
30	RW	0x0	Sw_blackwhite_e 1'b0: 4:2:0 sampling format 1'b1: 4:0:0 sampling format (H264 monochroma) Note: The h264 decoder will use these bits.
29	RW	0x0	Sw_dir_8x8_infer_e Specifies the method to use to derive luma motion vectors in B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag (see direct_8x8_inference flag). Note: The h264 decoder will use these bits.
28	RW	0x0	Sw_weight_pred_e Weighted prediction enable for P slices. Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
27:26	RW	0x0	Sw_weight_bipr_idc Weighted prediction specification for B slices: 2'b00: Default weighted prediction is applied to B slices 2'b01: Explicit weighted prediction shall be applied to B slices 2'b10: Implicit weighted prediction shall be applied to B slices Note: The h264 decoder will use these bits.
25:21	RO	0x00	Reserved
20:16	RW	0x00	Sw_framenum_len H.264: Bit length of frame_num in data stream. Note: The h264 decoder will use these bits.
15:0	RW	0x0000	Sw_framenum Current frame_num, used to identify short-term reference frames. Used in reference picture reordering. Note: The h264 decoder will use these bits.

VDPU_SWREG8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_const_intra_e Constrained_intra_pred_flag equal to 1 specifies that intra prediction uses only. Neighbouring intra macroblocks in prediction. When equal to 0 also neighbouring. Inter macroblocks are used in intra prediction process. Note: The h264 decoder will use these bits.
30	RW	0x0	Sw_filt_ctrl_pres Deblocking_filter_control_present_flag indicates whether extra variables controlling characteristics of the deblocking filter are present in the slice header. Note: The h264 decoder will use these bits.
29	RW	0x0	Sw_rdpic_cnt_pres Redundant_pic_cnt_present_flag specifies whether. Redundant_pic_cnt syntax elements. Note: The h264 decoder will use these bits.
28	RW	0x0	Sw_8x8trans_flag_e 8x8 transform flag enable for stream decoding. Note: The h264 decoder will use these bits.
27:17	RW	0x000	Sw_refpic_mk_len Length of decoded reference picture marking bits. Note: The h264 decoder will use these bits.
16	RW	0x0	Sw_idr_pic_e IDR (instantaneous decoding refresh) picture flag. Note: The h264 decoder will use these bits.
15:0	RW	0x0000	Sw_idr_pic_id Idr_pic_id, identifies IDR (instantaneous decoding refresh) picture. Note: The h264 decoder will use these bits.

VDPU_SWREG9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Sw_pps_id Pic_parameter_set_id, identifies the picture parameter set that is referred to in the slice header. Note: The h264 decoder will use these bits.
23:19	RW	0x00	Sw_refidx1_active Pecifies the maximum reference index that can be used while decoding inter predicted macro blocks. Note: The h264 decoder will use these bits.
18:14	RW	0x00	Sw_refidx0_active Specifies the maximum reference index that can be used while decoding inter predicted macro blocks. This is same as in previous decoders (width increased with q bit). Note: The h264 decoder will use these bits.
13:8	RO	0x00	Reserved
7:0	RW	0x00	Sw_poc_length Length of picture order count field in stream. Note: The h264 decoder will use these bits.

VDPU_SREG10_H264_RLC

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_diff_mv_base For H264 and MPEG4, RLC mode: Differential motion vector base address.

VDPU_SREG10_H264

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_pinit_rlist_f9 Initial reference picture list for P forward picid 9
24:20	RW	0x00	Sw_pinit_rlist_f8 Initial reference picture list for P forward picid 8
19:15	RW	0x00	Sw_pinit_rlist_f7 Initial reference picture list for P forward picid 7
14:10	RW	0x00	Sw_pinit_rlist_f6 Initial reference picture list for P forward picid 6
9:5	RW	0x00	Sw_pinit_rlist_f5 Initial reference picture list for P forward picid 5

Bit	Attr	Reset Value	Description
4:0	RW	0x00	Sw_pinit_rlist_f4 Initial reference picture list for P forward picid 4

VDPU_SWREG11_H264_RLC

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_i4x4_or_dc_base RLC mode: H.264: Intra prediction 4x4 mode base address. RLC mode: MPEG-4: DC component base address.

VDPU_SWREG11_H264

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_pinit_rlist_f15 Initial reference picture list for P forward picid 15
24:20	RW	0x00	Sw_pinit_rlist_f14 Initial reference picture list for P forward picid 14
19:15	RW	0x00	Sw_pinit_rlist_f13 Initial reference picture list for P forward picid 13
14:10	RW	0x00	Sw_pint_rlist_f12 Initial reference picture list for P forward picid 12
9:5	RW	0x00	Sw_pint_rlist_f11 Initial reference picture list for P forward picid 11
4:0	RW	0x00	Sw_pint_rlist_f10 Initial reference picture list for P forward picid 10

VDPU_SWREG12

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_rlc_vlc_base RLC mode: Base address for RLC data (swreg3.sw_rlc_mode_e = 1). VLC mode: Stream start address / end addr+I288ess with byte precision (swreg4.rlc_mode_en = 0), start bit number in swreg5. stream_start_bit. When sw_dec_buffer_int is high or sw_dec_e is low this register contains HW return value of last_byte_address (not valid for jpeg) where stream has been read (and used) in accuracy of byte. For debug purposes the last_byte_address is also written when stream error/ASO is detected even though it may not be accurate. Note: The h264 decoder will use these bits.

VDPU_SWREG13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_dec_out_base Video: Base address for decoder output picture. Points directly to start of decoder output picture or field. JPEG snapshot: Base address for decoder output luminance picture. Note: The h264 decoder will use these bits.

VDPU_SWREG14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer0_base Base address for reference picture index 0. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer0_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer0_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG15_JPEG_ROI

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	Reserved
19	RW	0x0	Sw_jpegroi_in_endian Sw_jpegroi_in_endian 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order)
18	RW	0x0	Sw_jpegroi_in_swap32 Sw_jpegroi_in_swap32 1'b0: No swapping of 32 bit words 1'b1: 32bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1 byte order (also little endian should be enabled).
17:16	RW	0x0	Sw_roi_sample_size ROI MB num sample each time 2'b00: 1 2'b01: 8 2'b10: 16 2'b11: 8
15:12	RW	0x0	Sw_roi_distance The distance between the sample MB and ROI start MB
11:10	RW	0x0	Sw_roi_out_sel ROI output selection 2'b00: Output offset/dc 2'b01: Output picture 2'b10: Output offset/dc and picture 2'b11: Output offset/dc
9	RW	0x0	Sw_roi_decode JPEG ROI decode 1'b0: Build offset/dc table 1'b1: ROI decode
8	RW	0x0	Sw_roi_en JPEG roi mode enable 1'b0: Normal jpeg decode mode 1'b1: JPEG roi mode

VDPU_SWREG15

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer1_base Base address for reference picture index 1. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer1_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer1_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG16

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer2_base Base address for reference picture index 2. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer2_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer2_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer3_base Base address for reference picture index 3. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer3_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer3_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer4_base Base address for reference picture index 4. See picture index definition from toplevel_sp Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
1	RW	0x0	Sw_refer4_field_e Refer picture consist of single fields or frame: 1'b0: Teference picture consists of frame 1'b1: Teference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer4_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG19

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer5_base Base address for reference picture index 5. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer5_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer5_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG20

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer6_base Base address for reference picture index 6. See picture index definition from toplevel_sp. Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer6_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer6_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG21

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer7_base Base address for reference picture index 7. See picture index definition from toplevel_sp Note: The h264 decoder will use these bits.
1	RW	0x0	Sw_refer7_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields Note: The h264 decoder will use these bits.
0	RW	0x0	Sw_refer7_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture Note: The h264 decoder will use these bits.

VDPU_SWREG22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer8_base Base address for reference picture index 8. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer8_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer8_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG23

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer9_base Base address for reference picture index 9. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer9_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields

Bit	Attr	Reset Value	Description
0	RW	0x0	Sw_refer9_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG24

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer10_base Base address for reference picture index 10. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer10_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer10_top_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG25

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2	RW	0x0	Sw_refer11_base Base address for reference picture index 11. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer11_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer11_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG26

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer12_base Base address for reference picture index 12. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer12_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer12_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG27

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer13_base Base address for reference picture index 13. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer13_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer13_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG28

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer14_base Base address for reference picture index 14. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer14_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer14_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG29

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_refer15_base Base address for reference picture index 15. See picture index definition from toplevel_sp.
1	RW	0x0	Sw_refer15_field_e Refer picture consist of single fields or frame: 1'b0: Reference picture consists of frame 1'b1: Reference picture consists of fields
0	RW	0x0	Sw_refer15_topc_e Which field of reference picture is closer to current picture: 1'b0: Bottom field is closer to current picture 1'b1: Top field is closer to current picture

VDPU_SWREG30

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer1_nbr Number for reference picture index 1.
15:0	RW	0x0000	Sw_refer0_nbr Number for reference picture index 0.

VDPU_SWREG31

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer3_nbr Number for reference picture index 3
15:0	RW	0x0000	Sw_refer2_nbr Number for reference picture index 2

VDPU_SWREG32

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer5_nbr Number for reference picture index 5
15:0	RW	0x0000	Sw_refer4_nbr Number for reference picture index 4

VDPU_SWREG33

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer7_nbr Number for reference picture index 7
15:0	RW	0x0000	Sw_refer6_nbr Number for reference picture index 6

VDPU_SWREG34

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer9_nbr Number for reference picture index 9
15:0	RW	0x0000	Sw_refer8_nbr Number for reference picture index 8

VDPU_SWREG35_JPEG_ROI

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_jpegdcoff_base JPEG roi offest/dc base address

VDPU_SWREG35

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer11_nbr Number for reference picture index 11
15:0	RW	0x0000	Sw_refer10_nbr Number for reference picture index 10

VDPU_SWREG36

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer13_nbr Number for reference picture index 13
15:0	RW	0x0000	Sw_refer12_nbr Number for reference picture index 12

VDPU_SWREG36_JPEG_ROI

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	Reserved
16:0	RW	0x00000	Sw_jpegdcoff_len The number of 64bit jpegdcoff, it can be used both when Sw_roi_decode is 1b0 or 1b1.

VDPU_SWREG37

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refer15_nbr Number for reference picture index 15
15:0	RW	0x0000	Sw_refer14_nbr Number for reference picture index 14

VDPU_SWREG38

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Sw_pred_bc_tap_3_3 Prediction filter set 3, tap 3
21:12	RW	0x000	Sw_pred_bc_tap_4_0 Prediction filter set 4, tap 0
11:2	RW	0x000	Sw_perd_bc_tap_4_1 Prediction filter set 4, tap 1

VDPU_SWREG38_H264

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer_lterm_e Long term flag for reference picture index [31:0].

VDPU_SWREG39

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Sw_pred_bc_tap_4_2 Prediction filter set 4, tap 2

Bit	Attr	Reset Value	Description
21:12	RW	0x000	Sw_pred_bc_tap_4_3 Prediction filter set 4, tap 3
11:2	RW	0x000	Sw_pred_bc_tap_5_0 Prediction filter set 5, tap 0

VDPU_SWREG39_H264

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer_valid_e Valid flag for reference picture index [31:0]

VDPU_SWREG40

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_qtable_base Base address for standard dependent tables: JPEG= AC,DC, QP tables MPEG4=QP table base address if type 1 quantization is used MPEG2=QP table base address H.264=base address for various tables Note: The h264 decoder will use these bits.

VDPU_SWREG41

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_dir_mv_base Direct mode motion vector write/read base address. For H264 this is used only for direct mode motion vector write base. Progressive JPEG: ACDC coefficient read/write base address. If current round is for DC components this base address is pointing to luminance (separate base addresses for chrominance), for AC component rounds this base is used for current type

VDPU_SWREG42

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
29:25	RW	0x00	Sw_binit_rlist_b2 Initial reference picture list for bi- direct backward picid 2
24:20	RW	0x00	Sw_binit_rlist_f2 Initial reference picture list for bi- direct forward picid 2
19:15	RW	0x00	Sw_binit_rlist_b1 Initial reference picture list for bi- direct backward picid 1
14:10	RW	0x00	Sw_binit_rlist_f1 Initial reference picture list for bi- direct forward picid 1
9:5	RW	0x00	Sw_binit_rlist_b0 Initial reference picture list for bi- direct backward picid 0
4:0	RW	0x00	Sw_binit_rlist_f0 Initial reference picture list for bi- direct forward picid 0

VDPU_SWREG43

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_binit_rlist_b5 Initial reference picture list for bi- direct backward picid 5
24:20	RW	0x00	Sw_binit_rlist_f5 Initial reference picture list for bi- direct forward picid 5
19:15	RW	0x00	Sw_binit_rlist_b4 Initial reference picture list for bi- direct backward picid 4
14:10	RW	0x00	Sw_binit_rlist_f4 Initial reference picture list for bi- direct forward picid 4
9:5	RW	0x00	Sw_binit_rlist_b3 Initial reference picture list for bi- direct backward picid 3
4:0	RW	0x00	Sw_binit_rlist_f3 Initial reference picture list for bi- direct forward picid 3

VDPU_SWREG44

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_binit_rlist_b8 Initial reference picture list for bi- direct backward picid 8
24:20	RW	0x00	Sw_binit_rlist_f8 Initial reference picture list for bi- direct forward picid 8
19:15	RW	0x00	Sw_binit_rlist_b7 Initial reference picture list for bi- direct backward picid 7

Bit	Attr	Reset Value	Description
14:10	RW	0x00	Sw_binit_rlist_f7 Initial reference picture list for bi- direct forward picid 7
9:5	RW	0x00	Sw_binit_rlist_b6 Initial reference picture list for bi- direct backward picid 6
4:0	RW	0x00	Sw_binit_rlist_f6 Initial reference picture list for bi- direct forward picid 6

VDPU_SWREG45

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_binit_rlist_b11 Initial reference picture list for bi-direct backward picid 11
24:20	RW	0x00	Sw_binit_rlist_f11 Initial reference picture list for bi-direct forward picid 11
19:15	RW	0x00	Sw_binit_rlist_b10 Initial reference picture list for bi-direct backward picid 10
14:10	RW	0x00	Sw_binit_rlist_f10 Initial reference picture list for bi-direct forward picid 10
9:5	RW	0x00	Sw_binit_rlist_b9 Initial reference picture list for bi-direct backward picid 9
4:0	RW	0x00	Sw_binit_rlist_f9 Initial reference picture list for bi-direct forward picid 9

VDPU_SWREG46

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_binit_rlist_b14 Initial reference picture list for bi-direct backward picid 14
24:20	RW	0x00	Sw_binit_rlist_f14 Initial reference picture list for bi-direct forward picid 14
19:15	RW	0x00	Sw_binit_rlist_b13 Initial reference picture list for bi-direct backward picid 13
14:10	RW	0x00	Sw_binit_rlist_f13 Initial reference picture list for bi-direct forward picid 13
9:5	RW	0x00	Sw_binit_rlist_b12 Initial reference picture list for bi-direct backward picid 12
4:0	RW	0x00	Sw_binit_rlist_f12 Initial reference picture list for bi-direct forward picid 12

VDPU_SWREG47

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:25	RW	0x00	Sw_pinit_rlist_f3 Initial reference picture list for P forward picid 3
24:20	RW	0x00	Sw_pinit_rlist_f2 Initial reference picture list for P forward picid 2
19:15	RW	0x00	Sw_pinit_rlist_f1 Initial reference picture list for P forward picid 1
14:10	RW	0x00	Sw_pinit_rlist_f0 Initial reference picture list for P forward picid 0
9:5	RW	0x00	Sw_binit_rlist_b15 Initial reference picture list for bi-direct backward picid 15
4:0	RW	0x00	Sw_binit_rlist_f15 Initial reference picture list for bi-direct forward picid 15

VDPU_SWREG48

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Sw_startmb_x Start MB from SW for X dimension. Used in error concealment case. Note: The h264 decoder will use these bits.
22:15	RW	0x00	Sw_startmb_y Start MB from SW for Y dimension. Used in error concealment case. Note: The h264 decoder will use these bits.

VDPU_SWREG49

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Sw_pred_bc_tap_0_0 Prediction filter set 0, tap 0 Note: The h264 decoder will use these bits.
21:12	RW	0x000	Sw_pred_bc_tap_0_1 Prediction filter set 0, tap 1 Note: The h264 decoder will use these bits.
11:2	RW	0x000	Sw_pred_bc_tap_0_2 Prediction filter set 0, tap 2 Note: The h264 decoder will use these bits.

VDPU_SWREG50

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31	RO	0x1	Sw_DEC_MPEG2_PROF Decoding format support, MPEG-2 / MPEG-1 1'b0: Not supported 1'b1: Supported
30:29	RO	0x3	Sw_DEC_VC1_PROF Decoding format support, VC-1 2'd0: Not supported 2'd1: Supported up to simple profile 2'd2: Supported up to main profile 2'd3: Supported up to advanced profile
28	RO	0x1	Sw_DEC_JPEG_PROF Decoding format support, JPEG 1'b0: Not supported 1'b1: Supported
27:26	RO	0x2	Sw_DEC_MPEG4_PROF Decoding format support, MPEG-4 / H.263 2'd0: Not supported 2'd1: Supported up to simple profile 2'd2: Supported up to advanced simple profile
25:24	RO	0x3	Sw_DEC_H264_PROF Decoding format support, H.264 2'd0: Not supported 2'd1: Supported up to baseline profile 2'd2: Supported up to high profile labeled stream with restricted high profile tools Note: The h264 decoder will use these bits.
22	RO	0x0	Sw_DEC_PJEPEG_EXIT Progressive JPEG support: 1'b0: Not supported 1'b1: Supported
21	RO	0x1	Sw_DEC_OBUFF_LEVEL Decoder output buffer level: 1'b0: 1 MB buffering is used 1'b1: 4 MB buffering is used Note: The h264 decoder will use these bits.
20	RO	0x1	Sw_REF_BUFF_EXIST Note: The h264 decoder will use these bits.
19:16	RO	0x5	Sw_DEC_BUS_STRD Note: The h264 decoder will use these bits.
15:14	RO	0x1	Sw_DEC_SYNTH_LAN Note: The h264 decoder will use these bits.
13:12	RO	0x2	Sw_DEC_BUS_WIDTH 2'd0: Error 2'd1: 32 bit bus 2'd2: 64 bit bus 2'd3: 128 bit bus Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
10:0	RO	0x780	Sw_DEC_MAX_OWIDTH Max configured decoder video resolution that can be decoded. Informed as width of the picture in pixels Note: The h264 decoder will use these bits.

VDPU_SWREG51

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_refbu_e Refer picture buffer enable: 1'b0: Refer picture buffer disabled 1'b1: Refer picture buffer enabled. Valid if picture size is QVGA or more Note: The h264 decoder will use these bits.
30:19	RW	0x000	Sw_refbu_thr Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed). Note: The h264 decoder will use these bits.
18:14	RW	0x00	Sw_refbu_picid The used reference picture ID for reference buffer usage Note: The h264 decoder will use these bits.
13	RW	0x0	Sw_refbu_eval_e Enable for HW internal reference ID calculation. If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture. Note: The h264 decoder will use these bits.
12	RW	0x0	Sw_refbu_fparmod_e Field parity mode enable. Used in refbufferd evaluation mode 1'b0: Use the result field of the evaluation 1'b1: Use the parity mode field Note: The h264 decoder will use these bits.
11:9	RO	0x0	Reserved
8:0	RW	0x000	Sw_refbu_y_offset Y offset for refbufferd. This coordinate is used to compensate the global motion of the video for better buffer hit rate. Note: The h264 decoder will use these bits.

VDPU_SWREG52

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refbu_hit_sum The sum of the refbufferd hits of the picture. Determined for each 8x8 luminance partition of the picture. The proceeding of the HW calculation can be read during HW decoding. Note: The h264 decoder will use these bits.
15:0	RW	0x0000	Sw_refbu_intra_sum The sum of the luminance 8x8 intra partitons of the picture. The proceeding of the HW calculation can be read during HW decoding. Note: The h264 decoder will use these bits.

VDPU_SWREG53

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved
21:0	RW	0x000000	Sw_refbu_y_mv_sum The sum of the decoded motion vector y-components of the picture. The first luminance motion vector of each MB is used in calculation. Other motion vectors of the MB are discarded. Each motion vector is saturated between 256-255 before calculation. The proceeding of the HW calculation can be read during HW decoding. Note: The h264 decoder will use these bits.

VDPU_SWREG54

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31	RO	0x1	Sw_DEC_JPEG_EXTENS JPEG sampling support extension for 411 and 444 samplings and support for bigger max resolution than 16 Mpix (up to 67Mpixels): 1'b0: Not supported 1'b1: Supported
30	RO	0x1	Sw_DEC_REFBU_ILACE Refbufferd support for interlaced content: 1'b0: Not supported 1'b1: Supported Note: The h264 decoder will use these bits.
28	RO	0x0	Sw_REF_BUFF2_EXIST Reference picture buffer 2 usage: 1'b0: Not supported 1'b1: Reference buffer 2 is used Note: The h264 decoder will use these bits.

Bit	Attr	Reset Value	Description
25	RO	0x0	Sw_DEC_RTL_ROM ROM implementation type (If design includes ROMs) 1'b0: ROMs are implemented from actual ROM units 1'b1: ROMs are impelemted from RTL
22	RO	0x1	Sw_DEC_AVS_PROF Decoding format support, AVS 1'b0: Not supported 1'b1: Supported
21:20	RO	0x1	Sw_DEC_MVC_PROF Decoding format support, MVC 1'b0: Not supported 1'b1: Supported
18:17	RO	0x1	Sw_DEC_TILED_L Tiled mode support level 2'd0: Not supported 2'd1: Supported with 8x4 tile size 2'd2, 2'd3: Reserved Note: The h264 decoder will use these bits.

VDPU_SWREG55

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_refbu2_buf_e Refer picture buffer 2 enable: 1'b0: Refer picture buffer disabled 1'b1: Refer picture buffer enabled. Valid if picture size is QVGA or more (can be turned of by HW if threshold value reached). Note: The h264 decoder will use these bits.
30:19	RW	0x000	Sw_refbu2_thr Reference buffer disable threshold value (buffer miss amount). Used to buffer shut down (if more misses than allowed). Note: The h264 decoder will use these bits.
18:14	RW	0x00	Sw_refbu2_picid The used reference picture ID for reference buffer usage Note: The h264 decoder will use these bits.
13:0	RW	0x0000	Sw_apf_threshold Advanced prefetch threshold value. If current MB exceeds the threshold the advanced mode is not used. Value 0 disables threshold usage and advanced. Refetch usage is restricted by internal memory limitation only. Note: The h264 decoder will use these bits.

VDPU_SWREG56

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_refbu_top_sum The sum of the top partitions of the picture Note: The h264 decoder will use these bits.
15:0	RW	0x0000	Sw_refbu_bot_sum The sum of the bottom partitions of the picture Note: The h264 decoder will use these bits.

VDPU_SWREG57_INTRA_INTER

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	Reserved
14:8	RO	0x00	Debug_service Service_wr[2:0], service_rd[3:0].
7	RW	0x0	Sw_cache_en 1'b1: Cache enable 1'b0: Cache disable When Sw_cache_en is 1'b1, Sw_pref_sigchan should also be 1'b1.
6	RW	0x0	Sw_pref_sigchan 1'b1: Prefetch single channel enable.
5	RW	0x0	Sw_axiwr_sel 1'b0: Auto sel encoder axi signals and decoder axi signals. 1'b1: Sel decoder axi signals (it only use to set bu_dec_e to 1'b0 in the middle of a frame).
4	RW	0x0	Sw_paral_bus When it is set to 1'b1, the axi support read and write service parallel; when it is set to 1'b0, the axi only support read and write serial.
3	RW	0x0	Sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block.
2	RW	0x0	Sw_intra_dblspeed Intra double speed enable.
1	RW	0x0	Sw_inter_dblspeed Inter double speed enable.
0	RW	0x0	Sw_stream_len_hi The extension bit of Sw_stream_len.

VDPU_SWREG57

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31	RW	0x0	Fuse_dec_h264 1'b1: H.264 enabled

Bit	Attr	Reset Value	Description
30	RW	0x0	Fuse_dec_mpeg4 1'b1: MPEG-4/H.263 enabled
29	RW	0x0	Fuse_dec_mpeg2 1'b1: MPEG-2/MPEG-1 enabled N
27	RW	0x0	Fuse_dec_jpeg 1'b1: JPEG enabled
25	RW	0x0	Fuse_dec_vc1 1'b1: VC1 enabled
24	RW	0x0	Fuse_dec_pjpeg 1'b1: Progressive JPEG enabled (Requires also JPEG to be enabled
19	RW	0x0	Fuse_dec_avs 1'b1: AVS enabled
18	RW	0x0	Fuse_dec_mvc Enabled (requires also H264 to be enabled)
17:16	RO	0x0	Reserved
15	RW	0x0	Fuse_dec_maxw_1920 1'b1: Max video width up to 1920 pixels enabled. Priority coded with priority 1.
14	RW	0x0	Fuse_dec_maxw_1280 1'b1: Max video width up to 1280 pixels enabled. Priority coded with priority 2.
13	RW	0x0	Fuse_dec_maxw_720 1'b1: Max video width up to 720 pixels enabled. Priority coded with priority 3.
12	RW	0x0	Fuse_dec_maxw_352 1'b1: Max video width up to 352 pixels enabled. Priority coded with priority 4
11:8	RO	0x0	Reserved
7	RW	0x0	Fuse_dec_refbuffer 1'b1: Reference buffer used

VDPU_SWREG58

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved
30	RO	0x0	Debug_mv_req Mvst_mv_req signal value
29	RO	0x0	Debug_rlc_req Prtr_res_y_req signal value
28	RO	0x0	Debug_res_y_req Prtr_res_y_req signal value
27	RO	0x0	Debug_res_c_req Prtr_res_c_req signal value

Bit	Attr	Reset Value	Description
26	RO	0x0	Debug_strm_da_e Strm_da_e signal value
25	RO	0x0	Debug_framerdy Dfbu_framerdy signal value
24	RO	0x0	Debug_filter_req Dfbu_req_e signal value
23	RO	0x0	Debug_referreq0 Drbu_referreq0 signal value
22	RO	0x0	Debug_referreq1 Prbu_referreq1 signal value
21	RO	0x0	Reserved
20:0	RO	0x000000	Debug_dec_mb_count HW internal MB counter value

VDPU_SWREG59

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_dec_ch8pix_base Base address for additional chrominance data format where chrominance is interleaved in group of 8 pixels. The usage is enabled by Sw_ch_8pix_ileav_e. Note: The h264 decoder will use these bits.

VDPU_SWREG60

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	Reserved
13	RW	0x0	Sw_pp_bus_int Interrupt status bit bus. Error response from bus. In pipeline mode this bit is not used.
12	RW	0x0	Sw_pp_rdy_int Interrupt status bit pp. When this bit is high post processor has processed a picture in external mode. In pipeline mode this bit is not used.
11:9	RO	0x0	Reserved
8	RW	0x0	Sw_pp_irq Post-processor IRQ. SW will reset this after interrupt is handled. HINTpp is not used for pp if IRQ disable pp is high (Sw_pp_irq_n_e = 1). In pipeline mode this bit is not used.
7:5	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	Sw_pp_irq_dis Post-processor IRQ disable. When high, there are no interrupts from HW concerning post processing. Polling must be used to see the interrupt.
3:2	RO	0x0	Reserved
1	RW	0x0	Sw_pp_pipeline_e Decoder C post-processing pipeline enable: 1'b0: Post-processing is processing different picture than decoder or is disabled 1'b1: Post-processing is performed in pipeline with decoder
0	RW	0x0	Sw_pp_e External mode post-processing enable. This bit will start the post-processing operation. Not to be used if PP is in pipeline with decoder (Sw_pp_pipeline_e = 1). HW will reset this when picture is post-processed.

VDPU_SWREG61

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	Sw_pp_axi_rd_id Read ID used for AXI PP read services (if connected to AXI)
23:16	RW	0x01	Sw_pp_axi_wr_id Write ID used for AXI PP write services (if connected to AXI)
15	RO	0x0	Reserved
14	RW	0x0	Sw_pp_scmd_dis AXI Single Command Multiple Data disable.
13	RW	0x0	Sw_pp_in_a2_endsel Endian/swap select for Alpha blend input source 2: 1'b0: Use PP in endian/swap definitions (Sw_pp_in_endian, Sw_pp_in_swap) 1'b1: Use Ablend source 1 endian/swap definitions
12	RW	0x0	Sw_pp_in_a1_swap32 Alpha blend source 1 input 32bit data swap (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
11	RW	0x0	Sw_pp_in_a1_endian Alpha blend source 1 input data byte endian mode. 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order)

Bit	Attr	Reset Value	Description
10	RW	0x0	Sw_pp_in_swap32_e PP input 32bit data swap (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))
9	RW	0x0	Sw_pp_data_disc_e PP data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally.
8	RW	0x1	Sw_pp_clkgate_e PP dynamic clock gating enable: 1'b1: Clock is gated from PP structures that are not used 1'b0: Clock is running for all PP structures Note: Clock gating value can be changed only when PP is not enabled
7	RW	0x0	Sw_pp_in_endian PP input picture byte endian mode. Used only if PP is in standalone mode. If PP is running pipelined with the decoder, this bit has no effect. 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order)
6	RW	0x0	Sw_pp_out_endian PP output picture endian mode for YCbCr data or for any data if config value Sw_PP_OEN_VERSION=1 1'b0: Big endian (0-1-2-3 order) 1'b1: Little endian (3-2-1-0 order) Note: For Sw_PP_OEN_VERSION=0, 16 bit RGB data this bit works as pixel swapping bit. For 32 bit RGB this bit has no meaning.
5	RW	0x0	Sw_pp_out_swap32_e PP output data word swap (may be used for 64 bit environment): 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order (also little endian should be enabled)).
4:0	RW	0x00	Sw_pp_max_burst Maximum burst length for PP bus transactions. 1-16

VDPU_SWREG62

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_deint_e De-interlace enable. Input data is in interlaced format and deinterlacing needs to be performed.
30	RO	0x0	Reserved
29:16	RW	0x0000	Sw_deint_threshold Threshold value used in deinterlacing.

Bit	Attr	Reset Value	Description
15	RW	0x0	Sw_deint_blend_e Blend enable for deinterlacing.
14:0	RW	0x0000	Sw_deint_edge_det Edge detect value used for deinterlacing.

VDPU_SWREG63

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_pp_in_lu_base Base address for post-processing input luminance picture. If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only.

VDPU_SWREG64

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_pp_in_cb_base Base address for post-processing input Cb picture or for both chrominance pictures (if chrominances interleaved). If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only.

VDPU_SWREG65

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_pp_in_cr_base Base address for post-processing input cr picture. Used in external mode only.

VDPU_SWREG66

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_pp_out_lu_base Base address for post-processing output picture (luminance/YUYV/RGB).

VDPU_SWREG67

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_pp_out_ch_base Base address for post-processing output chrominance picture (interleaved chrominance).

VDPU_SWREG68

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Sw_contrast_thr1 Threshold value 1, used with contrast adjusting.
23:20	RO	0x0	Reserved
19:10	RW	0x000	Sw_contrast_off2 Offset value 2, used with contrast adjusting.
9:0	RW	0x000	Sw_contrast_off1 Offset value 1, used with contrast adjusting.

VDPU_SWREG69

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_pp_in_start_ch For YUYV 422 input format. Enable for start_with_chrominance. 1'b0: The order is Y0CbY0Cr or Y0CrY0Cb 1'b1: The order is CbY0CrY0 or CrY0CbY0
30	RW	0x0	Sw_pp_in_cr_first For YUYV 422 input format and YCbCr 420 semiplanar format. Enable for Cr first (before Cb) 1'b0: The order is Y0CbY0Cr or CbY0CrY0 (if 420 semiplanar chrominance: CbCrCbCr) 1'b1: The order is Y0CrY0Cb or CrY0CbY0 (if 420 semiplanar chrominance: CrCbCrCb)
29	RW	0x0	Sw_pp_out_start_ch For YUYV 422 output format. Enable for start_with_chrominance. 1'b0: The order is Y0CbY0Cr or Y0CrY0Cb 1'b1: The order is CbY0CrY0 or CrY0CbY0
28	RW	0x0	Sw_pp_out_cr_first For YUYV 422 output format. Enable for Cr first (before Cb) 1'b0: The order is Y0CbY0Cr or CbY0CrY0 1'b1: The order is Y0CrY0Cb or CrY0CbY0
27:18	RW	0x000	Sw_color_coeffa2 Coefficient a2, used with Y pixel to calculate all color components.
17:8	RW	0x000	Sw_color_coeffa1 Coefficient a1, used with Y pixel to calculate all color components.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Sw_contrast_thr2 Threshold value 2, used with contrast adjusting.

VDPU_SWREG70

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:20	RW	0x000	Sw_color_coeffd Coefficient d, used with Cb to calculate green component value.
19:10	RW	0x000	Sw_color_coeffc Coefficient c, used with Cr to calculate green component value.
9:0	RW	0x000	Sw_color_coeffb Coefficient b, used with Cr to calculate red component value.

VDPU_SWREG71

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:21	RW	0x000	Sw_crop_startx Start coordinate x for the cropped area in macroblocks.
20:18	RW	0x0	Sw_rotation_mode Rotation mode: 3'b000: Rotation disabled 3'b001: Rotate + 90 3'b010: Rotate C 90 3'b011: Horizontal flip (mirror) 3'b100: Vertical flip 3'b101: Rotate 180
17:10	RW	0x00	Sw_color_coefff Coefficient f, used with Y to adjust brightness.
9:0	RW	0x000	Sw_color_coeffe Coefficient e, used with Cb to calculate blue component value.

VDPU_SWREG72

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Sw_crop_starty Start coordinate y for the cropped area in macroblocks.

Bit	Attr	Reset Value	Description
23	RO	0x0	Reserved
22:18	RW	0x00	Sw_rangemap_coef_y Range map value for Y component (RANGE_MAPY+9 in VC-1 standard).
17	RO	0x0	Reserved
16:9	RW	0x00	Sw_pp_in_height PP input picture height in MBs. Can be cropped from a bigger input picture in external mode.
8:0	RW	0x000	Sw_pp_in_width PP input picture width in MBs. Can be cropped from a bigger input picture in external mode.

VDPU_SWREG73

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_pp_bot_yin_base PP input Y base for bottom field.

VDPU_SWREG74

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Sw_pp_bot_cin_base PP input C base for bottom field (mixed chrominance).

VDPU_SWREG79

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_rangemap_y_e Range map enable for Y component (RANGE_MAPY_FLAG in VC-1 standard). For VC1 main profile this bit is used as range expansion enable.
30	RW	0x0	Sw_rangemap_c_e Range map enable for chrominance component (RANGE_MAPUV_FLAG in VC-1 standard).
29	RW	0x0	Sw_ycbcr_range Defines the YCbCr range in RGB conversion: 1'b0: 16 --> 235 for Y, 16 --> 240 for Chrominance 1'b1: 0 --> 255 for all components

Bit	Attr	Reset Value	Description
28	RW	0x0	Sw_rgb_pix_in32 RGB pixel amount/ 32 bit word 1'b0: 1 RGB pixel/32 bit 1'b1: 2 RGB pixels/32 bit
27:23	RW	0x00	Sw_rgb_r_padd Amount of ones that will be padded in front of the R-component.
22:18	RW	0x00	Sw_rgb_g_padd Amount of ones that will be padded in front of the G-component.
17:0	RW	0x00000	Sw_scale_wratio Scaling ratio for width (outputw-1/inputw-1)

VDPU_SWREG80

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved
30	RW	0x0	Sw_pp_fast_scale_e 1'b0: Fast downscaling is not enabled. 1'b1: Fast downscaling is enabled. The quality of the picture is decreased but performance is improved.
29:27	RW	0x0	Sw_pp_in_struct PP input data picture structure: 3'd0: Top field / progressive frame structure: Read input data from top field base address /frame base address and read every line. 3'd1: Bottom field structure: Read input data from bottom field base address and read every line. 3'd2: Interlaced field structure: Read input data from both top and bottom field base address and take every line from each field. 3'd3: Interlaced frame structure: Read input data from both top and bottom field base address and take every second line from each field. 3'd4: Ripped top field structure: Read input data from top field base address and read every second line. 3'd5: Ripped bottom field structure: Read input data from bottom field base address and read every second line
26:25	RW	0x0	Sw_hor_scale_mode Horizontal scaling mode: 2’b00: Off 2’b01: Upscale 2’b10: Downscale
24:23	RW	0x0	Sw_ver_scale_mode Vertical scaling mode: 2’b00: Off 2’b01: Upscale 2’b10: Downscale
22:18	RW	0x00	Sw_rgb_b_padd Amount of ones that will be padded in front of the B-component.

Bit	Attr	Reset Value	Description
17:0	RW	0x00000	Sw_scale_hratio Scaling ratio for height (outputh-1/inputh-1) .

VDPU_SWREG81

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_wscale_invra Inverse scaling ratio for width, or ch (inputw-1 / outputw-1)
15:0	RW	0x0000	Sw_hscale_invra Inverse scaling ratio for height or cv (inputh-1 / outputh-1)

VDPU_SWREG82

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_r_mask Bit mask for R component (and alpha channel)

VDPU_SWREG83

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_g_mask Bit mask for G component (and alpha channel)

VDPU_SWREG84

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_b_mask Bit mask for B component (and alpha channel)

VDPU_SWREG85

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Sw_pp_in_format PP input picture data format 3'd0: YUYV 4:2:2 interleaved (supported only in external mode) 3'd1: YCbCr 4:2:0 Semi-planar in linear raster-scan format 3'd2: YCbCr 4:2:0 planar (supported only in external mode) 3'd3: YCbCr 4:0:0 (supported only in pipelined mode) 3'd4: YCbCr 4:2:2 Semi-planar (supported only in pipelined mode) 3'd5: YCbCr 4:2:0 Semi-planar in tiled format (supported only in 3'dexternal mode (8170 decoder only) 3'd6: YCbCr 4:4:0 Semi-planar (supported only in pipelined mode, possible for jpeg only) 3'd7: Escape pp input data format. Defined in swreg86
28:26	RW	0x0	Sw_pp_out_format PP output picture data format: 3'd0: RGB 3'd1: YCbCr 4:2:0 planar (Not supported) 3'd2: YCbCr 4:2:2 planar (Not supported) 3'd3: YUYV 4:2:2 interleaved 3'd4: YCbCr 4:4:4 planar (Not supported) 3'd5: YCh 4:2:0 chrominance interleaved 3'd6: YCh 4:2:2 (Not supported) 3'd7: YCh 4:4:4 (Not supported)
25:15	RW	0x000	Sw_pp_out_height Scaled picture height in pixels (Must be dividable by 2 or by any if Pixel Accurate PP output configuration is enabled) Max scaled picture height is 1920 pixels or maximum three times the input source height minus 8 pixels.
14:4	RW	0x000	Sw_pp_out_width Scaled picture width in pixels. Must be dividable by 8 or by any if Pixel Accurate PP output configuration is enabled. Max scaled picture width is 1920 pixels or maximum three times the input source width minus 8 pixels.
3	RW	0x0	Sw_pp_out_tiled_e Tiled mode enable for PP output. Can be used only for YCbYCr 422 output format. Can be used only if correponding configuration supports this feature. Tile size is 4x4 pixels.
2	RW	0x0	Sw_pp_out_swap16_e PP output swap 16 swaps 16 bit halfs inside of 32 bit word. Can be used for 16 bit RGB to change pixel orders but is valid also for any output format. Note: requires that configuration of Sw_PPD_OEN_VERSION=1.
1	RW	0x0	Sw_pp_crop8_r_e PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the un-rotated input picture is used for PP input.
0	RW	0x0	Sw_pp_crop8_d_e PP input picture height is not 16 pixels multiple. Only 8 pixel rows of the most down MB of the un-rotated input picture is used for PP input.

VDPU_SWREG86

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Sw_pp_in_format_es Escape PP in format. Used if Sw_pp_in_format is defined to 7: 0 1'b0: YCbCr 4:4:4 1'b1: YCbCr 4:1:1
28	RO	0x0	Reserved
27:23	RW	0x00	Sw_rangemap_coef_c Range map value for chrominance component (RANGE_MAPUV+9 in VC-1 standard).
22	RW	0x0	Sw_mask1_ablend_e Mask 1 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 1 base address. Alpha blending can be enabled only for RGB/ YUYV 422 data.
21:11	RW	0x000	Sw_mask1_starty Vertical start pixel for mask area 1. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions.
10:0	RW	0x000	Sw_mask1_startix Horizontal start pixel for mask area 1. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions.

VDPU_SWREG87

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_mask2_ablend_e Mask 2 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 2 base address. Alpha blending can be enabled only for RGB/YUYV 422 data.
21:11	RW	0x000	Sw_mask_starty Verical start pixel for mask area 2. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions.
10:0	RW	0x000	Sw_mask2_startx Horizontal start pixel for mask area 2. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions.

VDPU_SWREG88

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	Sw_ext_orig_width PP input picture original width in macro blocks.
22	RW	0x0	Sw_mask1_e Mask 1 enable. If mask 1 is used this bit is high.
21:11	RW	0x000	Sw_mask1_endy Mask 1 end coordinate y in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateY, ScaledHeight].
10:0	RW	0x000	Sw_mask1_endx Mask 1 end coordinate x in pixels (inside of PPD output picture). Range must be between [Mask1StartCoordinateX, ScaledWidth].

VDPU_SWREG89

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22	RW	0x0	Sw_mask2_e Mask 2 enable. If mask 1 is used this bit is high.
21:11	RW	0x000	Sw_mask2_endy Mask 2 end coordinate y in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateY,ScaledHeight].
10:0	RW	0x000	Sw_mask2_endx Mask 2 end coordinate x in pixels (inside of PP output picture). Range must be between [Mask2StartCoordinateX,ScaledWidth].

VDPU_SWREG90

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29	RW	0x0	Sw_right_cross_e Right side overcross enable. 1'b0: No right side overcross. 1'b1: Right side overcross.
28	RW	0x0	Sw_left_cross_e Left side overcross enable. 1'b0: No left side overcross. 1'b1: Left side overcross.
27	RW	0x0	Sw_up_cross_e Upward overcross enable. 1'b0: No upward overcross. 1'b1: Upward overcross.

Bit	Attr	Reset Value	Description
26	RW	0x0	Sw_down_cross_e Downward overcross enable. 1'b0: No downward overcross. 1'b1: Downward overcross.
25:15	RW	0x000	Sw_up_cross Amount of upward overcross (vertical pixels outside of display from the upper side). Range must be between [0, ScaledHeight].
14:11	RO	0x0	Reserved
10:0	RW	0x000	Sw_down_cross Amount of downward overcross (vertical pixels outside of displayfrom the down side). Range must be between [0, ScaledHeight].

VDPU_SWREG91

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Sw_dither_select_r Dithering control for R channel: 2'b00: Dithering disabled 2'b01: Use four-bit dither matrix 2'b10: Use five-bit dither matrix 2'b11: Use six-bit dither matrix
29:28	RW	0x0	Sw_dither_select_g Dithering control for G channel: 2'b00: Dithering disabled 2'b01: Use four-bit dither matrix 2'b10: Use five-bit dither matrix 2'b11: Use six-bit dither matrix
27:26	RW	0x0	Sw_dither_select_b Dithering control for B channel: 2'b00: Dithering disabled 2'b01: Use four-bit dither matrix 2'b10: Use five-bit dither matrix 2'b11: Use six-bit dither matrix
25:24	RO	0x0	Reserved
23:22	RW	0x0	Sw_pp_tiled_mode Input data is in tiled mode (at the moment valid only for YCbCr 420 data, pipeline or external mode): 2'b00: Tiled mode not used 2'b01: Tiled mode enabled for 8x4 sized tiles 2'b10, 2'b11: Reserved
21:11	RW	0x000	Sw_right_cross Amount of right side overcross (Horizontal pixels outside of display from the right side). Range must be between [0, ScaledWidth].
10:0	RW	0x000	Sw_left_cross Amount of left side overcross (Horizontal pixels outside of display from the left side). Range must be between [0, ScaledWidth].

VDPU_SWREG92

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Sw_pp_in_h_ext Extended PP input height. Used with JPEG.
28:26	RW	0x0	Sw_pp_in_w_ext Extended PP input width. Used with JPEG.
25:23	RW	0x0	Sw_crop_starty_ext Extended PP input crop start coordinate x. Used with JPEG.
22:20	RW	0x0	Sw_crop_start_ext Extended PP input crop start coordinate y. Used with JPEG.
19:12	RO	0x00	Reserved
11:0	RW	0x000	Sw_display_width Width of the display in pixels. Max HDTV (1920).

VDPU_SWREG93

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_abledn1_base Base address for alpha blending input 1 (if mask1 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 1 size or with ablend1_scanline if ablend cropping is supported in configuration.

VDPU_SWREG94

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_ablend2_base Base address for alpha blending input 2 (if mask2 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 2 size or with ablend2_scanline if ablend cropping is supported in configuration.

VDPU_SWREG95

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	Reserved
25:13	RW	0x0000	Sw_ablend2_scan Scanline width in pixels for Ablend 2. Usage enabled if corresponding configuration bit is enabled.
12:0	RW	0x0000	Sw_ablend1_scan Scanline width in pixels for Ablend 1. Usage enabled if corresponding configuration bit is enabled.

VDPU_SWREG98

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	Sw_pp_out_h_ext PP output heightextension.
0	RW	0x0	Sw_pp_out_w_ext PP output widthextension.

VDPU_SWREG99

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31	RO	0x1	Fuse_pp_pp 1'b1: PP enabled.
30	RO	0x1	Fuse_pp_deint 1'b1: Deinterlacing enabled.
29	RO	0x1	Fuse_pp_ablend 1'b1: Alpha Blending enabled.
28:16	RO	0x0000	Reserved
15	RO	0x1	Fuse_pp_maxw_1920 1'b1: Max PP output width up to 1920 pixels enabled. Priority coded with priority 1.
14	RO	0x1	Fuse_pp_maxw_1280 1'b1: Max PP output width up to 1280 pixels enabled. Priority coded with priority 2.
13	RO	0x1	Fuse_pp_maxw_720 1'b1: Max PP output width up to 720 pixels enabled. Priority coded with priority 3.
12	RO	0x1	Fuse_pp_maxw_352 1'b1: Max PP output width up to 352 pixels enabled. Priority coded with priority 4.

VDPU_SWREG100

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31	RO	0x1	SW_ABLEND_CROP_E Alpha blending support for input cropping: 1'b0: Not supported. External memory must include the exact image of the area being alpha blended. 1'b1: Supported. External memory can include a picture from blended area can be cropped. Requires usage of swreg95.
30	RO	0x1	SW_PPD_PIXAC_E Pixel Accurate PP output mode exists: 1'b0: PIP, Scaling and masks can be adjusted by steps of 8 pixels (width) or 2 pixels (height). 1'b1: PIP, Scaling and masks can be adjusted by steps of 1 pixel for RGB and 2 pixels for subsampled chroma formats (by using bus specific write strobe functionality).
29	RO	0x1	SW_PPD_TILED_EXIST PP output YCbYCr 422 tiled support (4x4 pixel tiles) 1'b0: Not supported 1'b1: Supported
28	RO	0x1	SW_PPD_DITH_EXIST Dithering exists: 1'b0: No 1'b1: Yes
27:26	RO	0x3	SW_PPD_SCALE_LEVEL Scaling support: 2'b00: No scaling 2'b01: Scaling with lo performance architecture 2'b10: Scaling with high performance architecture 2'b11: Scaling with high performance architecture + fast
25	RO	0x1	SW_PPD_DEINT_EXIST De-interlacing exits: 1'b0: No 1'b1: Yes
24	RO	0x1	SW_PPD_BLEND_EXIST Alpha blending exists: 1'b0: No 1'b1: Yes
23	RO	0x1	SW_PPD_IBUFF_LEVEL PP input buffering level: 1'b0: 1 MB input buffering is used 1'b1: 4 MB input buffering is used
22:19	RO	0x0	Reserved
18	RO	0x1	SW_PPD_OEN_VERSION PP output endian version: 1'b0: Endian mode supported for other than RGB 1'b1: Endian mode supported for any output format
17	RO	0x1	SW_PPD_OBUFF_LEVEL PP output buffering level: 1'b0: 1 unit output buffering is used 1'b1: 4 unit output buffering is used

Bit	Attr	Reset Value	Description
16	RO	0x1	SW_PPD_PP_EXIST PPD exists: 1'b0: No 1'b1: Yes
15:14	RO	0x1	SW_PPD_IN_TILED_L PPD input tiled mode support level 1'b0: Not supported 1'b1: 8x4 tile size supported
13:11	RO	0x0	Reserved
10:0	RO	0x780	SW_PPD_MAX_OWIDTH Max supported PP output width in pixels

VDPU_SWREG101

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x0	Sw_soft_reset Softreset pulse signal Write to 1'b1, valid; Write to 1'b0, invalid;

VDPU_SWREG102

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Vpu_work_cycle Write initial/reset value in the begin of frame start, then will auto count base this value.

VDPU_SWREG103

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_axi_ddr_rdata Axi ddr rdata num, the unit is byte.

VDPU_SWREG104

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x0	Sw_axi_ddr_wdata Vdpu write data byte num

VDPU_SWREG105

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	Reserved
19:16	RW	0x0	Mon_sig_sel1 Select the counter be used for which to calculate cycle num 4'b0000: Don't work. 4'b0001: Mv buffer hold back stream decode working cycles 4'b0010: The output fifo of cabac keep full cycles. 4'b0011: The Code stream parsing block working cycles. 4'b0100: Scd block can't write data to scd buffer cycles. 4'b0101: The speed of reconsitution and interpolation fast than reference frames fetch cycles. 4'b0110: The speed of reconsitution and interpolation slow than reference frames fetch cycles. 4'b0111: The cycles filter block hold back pred block. 4'b1000: The cycles of pred block waiting for Residual data. 4'b1001: The cycles of bus Related modules working.
15:4	RO	0x000	Reserved
3:0	RW	0x0	Mon_sig_sel0 Select the counter be used for which to calculate cycle num 4'b0000: Don't work. 4'b0001: Mv buffer hold back stream decode working cycles. 4'b0010: The output fifo of cabac keep full cycles. 4'b0011: The Code stream parsing block working cycles. 4'b0100: Scd block can't write data to scd buffer cycles. 4'b0101: The speed of reconsitution and interpolation fast than reference frames fetch cycles. 4'b0110: The speed of reconsitution and interpolation slow than reference frames fetch cycles. 4'b0111: The cycles filter block hold back pred block. 4'b1000: The cycles of pred block waiting for Residual data. 4'b1001: The cycles of bus Related modules working.

VDPU_SWREG106

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Performance_mon_cnt0 The counter for the selected signal valid cycles which describe in swreg105[3:0]. Write initial/reset value

VDPU_SWREG107

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Performance_mon_cnt1 The counter for the selected signal valid cycles which describe in swreg105[19:16] Write initial/reset value.

10.5.4 VDPU121 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state
VCODEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
VCODEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
VCODEC_MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
VCODEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
VCODEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.5 VDPU121 MMU Detail Registers Description

VCODEC_MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

VCODEC_MMU_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY 1'b1:The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command. 1'b1: Page fault is active
0	RO	0x0	PAGING_ENABLED 1'b0: Paging is disabled 1'b1: Paging is enabled

VCODEC_MMU_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET

VCODEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

VCODEC_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE ddress to be invalidated from the page table cache

VCODEC_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error status
0	RW	0x0	PAGE_FAULT Page fault status

VCODEC_MMU_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	WO	0x0	READ_BUS_ERROR Write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT Write 1 to page fault clear

VCODEC_MMU_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Enable the read bus interrupt source when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT Enable the page fault interrupt source when this bit is set to 1'b1

VCODEC_MMU_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RO	0x0	READ_BUS_ERROR 1'b1: Read bus error status
0	RO	0x0	PAGE_FAULT 1'b1: Page fault

VCODEC_MMU_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x1	Mmu_auto_clkgating When it is 1'b1, the mmu will auto gating it self

10.5.6 VDPU346 Registers Summary

Name	Offset	Size	Reset Value	Description
Rkvdec_Swreg0_id	0x0000	W	0x00000000	ID register (read only)
Rkvdec_Swreg8_in_out	0x0020	W	0x00000000	Data input and output endian setting and sys ctrl.
Rkvdec_Swreg9_dec_mode	0x0024	W	0x00000000	Dec mode
Rkvdec_Swreg10_dec_e	0x0028	W	0x00000000	Decoder enable
Rkvdec_Swreg11_important_en	0x002c	W	0x00000000	Interrupt and decoder enable register.
Rkvdec_Swreg12_sencodary_en	0x0030	W	0x00000000	Sys ctrl
Rkvdec_Swreg13_en_mode_set	0x0034	W	0x00000000	Enable register.
Rkvdec_Swreg14_fbc_param_set	0x0038	W	0x00000000	Fbc parem set.
Rkvdec_Swreg15_stream_param_set	0x003c	W	0x00000000	Stream param set
Rkvdec_Swreg16_stream_len	0x0040	W	0x00000000	Amount of stream bytes in the input buffer or amount ot rlc bytes in the input buffer.
Rkvdec_Swreg17_slice_number	0x0044	W	0x00000000	The current frame slice number
Rkvdec_Swreg18_y_hor_stride	0x0048	W	0x00000000	Picture horizontal virtual stride.
Rkvdec_Swreg19_uv_hor_stride	0x004c	W	0x00000000	Picture parametes
Rkvdec_Swreg20_y_stride	0x0050	W	0x00000000	The output picture y fac virtual stride.Suggest this register to config to even for advance ddr performance.

Rkvdec_Swreg20_fbc_payload_offset	0x0050	W	0x00000000	Register0004 Description
Rkvdec_Swreg21_error_ctrl_set	0x0054	W	0x00000000	Error sys ctrl
Rkvdec_Swreg22_err_roi_ctu_offset_start	0x0058	W	0x00000000	It will cal the error ctu num in the roi.It will include the st ctu and end ctu.
Rkvdec_Swreg23_err_roi_ctu_offset_end	0x005c	W	0x00000000	It will cal the error ctu num in the roi.It will include the st ctu and end ctu.
Rkvdec_Swreg24_cabac_error_en_lowbits	0x0060	W	0x00000000	Cabac error enable config.
Rkvdec_Swreg25_cabac_error_en_highbits	0x0064	W	0x00000000	Cabac error enable high bits config.
Rkvdec_Swreg26_block_gating_en	0x0068	W	0x00000000	Block gating enable ctrl flag.
Rkvdec_Swreg64_vp9_set	0x0100	W	0x00000000	Vp9 compressed header offset.2014.11.19 del this register, because we can decode out sw_vp9_cprheader_offset from the stream.
Rkvdec_Swreg64_h26x_set	0x0100	W	0x00000000	For H26x use
Rkvdec_Swreg65_cur_poc	0x0104	W	0x00000000	Hevc & h264 & avs2 :the poc of cur picture.
Rkvdec_Swreg66_h264_cur_poc1	0x0108	W	0x00000000	When cur is field, h264 cur poc for bottom field.
Rkvdec_Swreg67_vp9_segid_grp0	0x010c	W	0x00000000	Vp9 segid syntax grp0.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg67_ref0_poc	0x010c	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 0.

Rkvdec_Swreg68_vp9_segid_grp1	0x0110	W	0x00000000	Vp9 segid syntax grp1.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg68_ref1_poc	0x0110	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 1.
Rkvdec_Swreg69_vp9_segid_grp2	0x0114	W	0x00000000	Vp9 segid syntax grp2.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg69_ref2_poc	0x0114	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 2.
Rkvdec_Swreg70_vp9_segid_grp3	0x0118	W	0x00000000	Vp9 segid syntax grp3.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg70_ref3_poc	0x0118	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 3.
Rkvdec_Swreg71_vp9_segid_grp4	0x011c	W	0x00000000	Vp9 segid syntax grp4.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg71_ref4_poc	0x011c	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 4.
Rkvdec_Swreg72_vp9_segid_grp5	0x0120	W	0x00000000	Vp9 segid syntax grp5.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg72_ref5_poc	0x0120	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 5.
Rkvdec_Swreg73_vp9_segid_grp6	0x0124	W	0x00000000	Vp9 segid syntax grp6.When write it is for last frame.When read it is for cur frame.
Rkvdec_Swreg73_ref6_poc	0x0124	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 6.
Rkvdec_Swreg74_vp9_segid_grp7	0x0128	W	0x00000000	Vp9 segid syntax grp7.When write it is for last frame.When read it is for cur frame.

Rkvdec_Swreg74_ref7_poc	0x0128	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 7.
Rkvdec_Swreg75_vp9_info_lastframe	0x012c	W	0x00000000	Vp9 info for lastframe.
Rkvdec_Swreg75_ref8_poc	0x012c	W	0x00000000	Hevc & h264: The poc of reference picture index 8.
Rkvdec_Swreg76_vp9_cprheader_config	0x0130	W	0x00000000	Vp9 compressed header config info.
Rkvdec_Swreg76_ref9_poc	0x0130	W	0x00000000	Hevc & h264: The poc of reference picture index 9.
Rkvdec_Swreg77_vp9_intercmd_num	0x0134	W	0x00000000	Vp9 intercmd num.
Rkvdec_Swreg77_ref10_poc	0x0134	W	0x00000000	Hevc & h264: The poc of reference picture index 10.
Rkvdec_Swreg78_vp9_stream_size	0x0138	W	0x00000000	Vp9 last tile size.
Rkvdec_Swreg78_ref11_poc	0x0138	W	0x00000000	Hevc & h264: The poc of reference picture index 11.
Rkvdec_Swreg79_vp9_lastf_y_hor_virstride	0x013c	W	0x00000000	Vp9 last frame y horizontal virstride.
Rkvdec_Swreg79_ref12_poc	0x013c	W	0x00000000	Hevc & h264: The poc of reference picture index 12.
Rkvdec_Swreg80_vp9_lastf_uv_hor_virstride	0x0140	W	0x00000000	Vp9 last frame uv horizontal virstride.
Rkvdec_Swreg80_ref13_poc	0x0140	W	0x00000000	Hevc & h264: The poc of reference picture index 13.
Rkvdec_Swreg81_vp9_goldenf_y_hor_virstride	0x0144	W	0x00000000	Vp9 golden frame y horizontal virstride.
Rkvdec_Swreg81_ref14_poc	0x0144	W	0x00000000	Hevc & h264: The poc of reference picture index 14.

Rkvdec_Swreg82_vp9_golden_uv_hor_virstride	0x0148	W	0x00000000	Vp9 golden uv horizontal virstirde.
Rkvdec_Swreg82_ref15_poc	0x0148	W	0x00000000	H264: The poc of reference picture index 15.Hevc: Used for mvc.Vp9: Now is no use.
Rkvdec_Swreg83_vp9_altreff_y_hor_virstride	0x014c	W	0x00000000	Vp9 altref frame y horizontal virstride.
Rkvdec_Swreg83_ref16_poc	0x014c	W	0x00000000	H264: The poc of reference picture index 16.Hevc & vp9: Now is no use.
Rkvdec_Swreg84_vp9_altreff_uv_hor_virstride	0x0150	W	0x00000000	Vp9 altreff uv horizontal virstirde.2015.10.23, change from 9bits to 10bits.
Rkvdec_Swreg84_ref17_poc	0x0150	W	0x00000000	H264: The poc of reference picture index 17.Hevc & vp9: Now is no use.
Rkvdec_Swreg85_vp9_lastf_y_virstride	0x0154	W	0x00000000	Last ref ystride
Rkvdec_Swreg85_ref18_poc	0x0154	W	0x00000000	H264: The poc of reference picture index 18.Hevc & vp9: Now is no use.
Rkvdec_Swreg86_vp9_golden_y_virstride	0x0158	W	0x00000000	Vp9 golden y stride
Rkvdec_Swreg86_ref19_poc	0x0158	W	0x00000000	H264: The poc of reference picture index 19.Hevc & vp9: Now is no use.
Rkvdec_Swreg87_vp9_altref_y_virstride	0x015c	W	0x00000000	Altref ref ystride
Rkvdec_Swreg87_ref20_poc	0x015c	W	0x00000000	H264: The poc of reference picture index 20.Hevc & vp9: Now is no use.
Rkvdec_Swreg88_vp9_lref_hor_scale	0x0160	W	0x00000000	Horizontal scaling factor for last reference picture.

Rkvdec_Swreg88_ref21_poc	0x0160	W	0x00000000	H264: The poc of reference picture index 21.Hevc & vp9: Now is no use.
Rkvdec_Swreg89_vp9_lref_ver_scale	0x0164	W	0x00000000	Vertical scaling factor for last reference picture.
Rkvdec_Swreg89_ref22_poc	0x0164	W	0x00000000	H264: The poc of reference picture index 22.Hevc & vp9: Now is no use.
Rkvdec_Swreg90_vp9_gref_hor_scale	0x0168	W	0x00000000	Horizontal scaling factor for golden reference picture.
Rkvdec_Swreg90_ref23_poc	0x0168	W	0x00000000	H264: The poc of reference picture index 23.Hevc & vp9: Now is no use.
Rkvdec_Swreg91_vp9_gref_ver_scale	0x016c	W	0x00000000	Vertical scaling factor for golden reference picture.
Rkvdec_Swreg91_ref24_poc	0x016c	W	0x00000000	H264: The poc of reference picture index 24.Hevc & vp9: Now is no use.
Rkvdec_Swreg92_vp9_aref_hor_scale	0x0170	W	0x00000000	Horizontal scaling factor for alfter reference picture.
Rkvdec_Swreg92_ref25_poc	0x0170	W	0x00000000	H264: The poc of reference picture index 25.Hevc & vp9: Now is no use.
Rkvdec_Swreg93_vp9_aref_ver_scale	0x0174	W	0x00000000	Vertical scaling factor for alfter reference picture.
Rkvdec_Swreg93_ref26_poc	0x0174	W	0x00000000	H264: The poc of reference picture index 26.Hevc & vp9: Now is no use.
Rkvdec_Swreg94_vp9_ref_deltas_lastframe	0x0178	W	0x00000000	Vp9 ref deltas
Rkvdec_Swreg94_ref27_poc	0x0178	W	0x00000000	H264: The poc of reference picture index 27.Hevc & vp9: Now is no use.

Rkvdec_Swreg95_ref28_poc	0x017c	W	0x00000000	H264: The poc of reference picture index 28.Hevc & vp9: Now is no use.
Rkvdec_Swreg96_ref29_poc	0x0180	W	0x00000000	H264: The poc of reference picture index 29.Hevc & vp9: Now is no use.
Rkvdec_Swreg97_ref30_poc	0x0184	W	0x00000000	H264: The poc of reference picture index 30.Hevc & vp9: Now is no use.
Rkvdec_Swreg98_ref31_poc	0x0188	W	0x00000000	H264: The poc of reference picture index 31.Hevc & vp9: Now is no use.
Rkvdec_Swreg99_hevc_ref_valid	0x018c	W	0x00000000	Valid flag for picture index 0 ~14.
Rkvdec_Swreg99_h264_reg0_3_info	0x018c	W	0x00000000	Rreference picture index 0~3
Rkvdec_Swreg99_avs2_reg0_3_info	0x018c	W	0x00000000	Rreference picture index 0~3
Rkvdec_Swreg100_avs2_reg4_7_info	0x0190	W	0x00000000	Rreference picture index 4~7
Rkvdec_Swreg100_h264_reg4_7_info	0x0190	W	0x00000000	Rreference picture index 4~7
Rkvdec_Swreg101_h264_reg8_11_info	0x0194	W	0x00000000	Rreference picture index 8~11
Rkvdec_Swreg102_h264_reg12_15_info	0x0198	W	0x00000000	Rreference picture index 12~15
Rkvdec_Swreg103_vp9_prob_en	0x019c	W	0x00000000	Vp9_prob_en config.
Rkvdec_Swreg103_hevc_mvc0	0x019c	W	0x00000000	Hevc mvc config register.
Rkvdec_Swreg103_avs2_ctrl_extra	0x019c	W	0x00000000	Avs2 ctrl register

Rkvdec_Swreg104_hevc_mvc1	0x01a0	W	0x00000000	Hevc MVC ctrl register.
Rkvdec_Swreg105_vp9cnt_upd_en_avs2_headlen	0x01a4	W	0x00000000	Avs2_head_len and Vp9 count update en.
Rkvdec_Swreg106_vp9_frame_width_last	0x01a8	W	0x00000000	Last frame frame_size_width.
Rkvdec_Swreg107_vp9_frame_height_last	0x01ac	W	0x00000000	Last frame frame_size_height.
Rkvdec_Swreg108_vp9_frame_width_golden	0x01b0	W	0x00000000	Golden frame_size_width.
Rkvdec_Swreg109_vp9_frame_height_golden	0x01b4	W	0x00000000	Golden frame_size_height.
Rkvdec_Swreg110_vp9_frame_width_altref	0x01b8	W	0x00000000	Alfter frame_size_width.
Rkvdec_Swreg111_vp9_frame_height_altref	0x01bc	W	0x00000000	Alfter frame_size_height.
Rkvdec_Swreg112_error_ref_info	0x01c0	W	0x00000000	Refer error is top or bot field flag.
Rkvdec_Swreg128_strm_rlc_base	0x0200	W	0x00000000	The stream or rlc data base address.
Rkvdec_Swreg129_rlcwrite_base	0x0204	W	0x00000000	The base address of rlcwrite base address.When frame is ready, it is the address of the end of rlcwrite address.
Rkvdec_Swreg129_error_info_base	0x0204	W	0x00000000	The base address of error info
Rkvdec_Swreg130_decout_base	0x0208	W	0x00000000	Base address of decoder output picture.Suggest this register to config to even for advance ddr performance.
Rkvdec_Swreg131_colmv_cur_base	0x020c	W	0x00000000	Cur frame colmv output addr.

Rkvdec_Swreg132_error_ref_base	0x0210	W	0x00000000	Error reference frame base address.
Rkvdec_Swreg133_rcb_intrar_base	0x0214	W	0x00000000	Rcb intra row base address, unit: 64byts align.
Rkvdec_Swreg134_rcb_transdr_base	0x0218	W	0x00000000	Rcb transd row base address, unit: 64byts align.
Rkvdec_Swreg135_rcb_transdc_base	0x021c	W	0x00000000	Rcb transd col base address, unit: 64byts align.
Rkvdec_Swreg136_rcb_strmdr_base	0x0220	W	0x00000000	Rcb stream row base address, unit: 64byts align.
Rkvdec_Swreg137_rcb_interr_base	0x0224	W	0x00000000	Rcb inter row base address, unit: 64byts align.
Rkvdec_Swreg138_rcb_interc_base	0x0228	W	0x00000000	Rcb inter col base address, unit: 64byts align.
Rkvdec_Swreg139_rcb_dblkr_base	0x022c	W	0x00000000	Rcb dblock row base address, unit: 64byts align.
Rkvdec_Swreg140_rcb_saor_base	0x0230	W	0x00000000	Rcb sao row base address, unit: 64byts align.
Rkvdec_Swreg141_rcb_fbcr_base	0x0234	W	0x00000000	Rcb fbc row base address, unit: 64byts align.
Rkvdec_Swreg142_rcb_filtc_col_base	0x0238	W	0x00000000	Rcb filter col base address, unit: 64byts align.
Rkvdec_Swreg160_vp9_delta_prob_base	0x0280	W	0x00000000	The base address of prob.
Rkvdec_Swreg161_avs2_head_base	0x0284	W	0x00000000	The base address of avs2 head.
Rkvdec_Swreg161_pps_base	0x0284	W	0x00000000	The base address of pps.
Rkvdec_Swreg162_vp9_last_prob_base	0x0288	W	0x00000000	It only used when hardware parse prob.This base addr is for last prob.

Rkvdec_Swreg163_rps_base	0x028c	W	0x00000000	The base address of rps.
Rkvdec_Swreg164_vp9_referlast_base	0x0290	W	0x00000000	Base address for reference picture.Suggest this register to config to even for advance ddr performance.
Rkvdec_Swreg164_ref0_base	0x0290	W	0x00000000	Base address for reference picture index0.
Rkvdec_Swreg165_vp9_refergolden_base	0x0294	W	0x00000000	Base address for golden picture.Suggest this register to config to even for advance ddr performance.
Rkvdec_Swreg165_ref1_base	0x0294	W	0x00000000	Base address for reference picture index1.
Rkvdec_Swreg166_vp9_referalfter_base	0x0298	W	0x00000000	Base address for alfter picture.Suggest this register to config to even for advance ddr performance.
Rkvdec_Swreg166_ref2_base	0x0298	W	0x00000000	Base address for reference picture index2.
Rkvdec_Swreg167_ref3_base	0x029c	W	0x00000000	Base address for reference picture index3.
Rkvdec_Swreg167_vp9count_base	0x029c	W	0x00000000	Vp9 count base addr.
Rkvdec_Swreg168_ref4_base	0x02a0	W	0x00000000	Base address for reference picture index4.
Rkvdec_Swreg168_vp9_segidlast_base	0x02a0	W	0x00000000	Base address for last frame segment id.
Rkvdec_Swreg169_ref5_base	0x02a4	W	0x00000000	Base address for reference picture index5.
Rkvdec_Swreg169_avp9_segidcur_base	0x02a4	W	0x00000000	Base address for cur frame segment id.

Rkvdec_Swreg170_ref6_base	0x02a8	W	0x00000000	Base address for reference picture index6.
Rkvdec_Swreg170_vp9_refcolmv_base	0x02a8	W	0x00000000	Vp9 refcolmv base addr.
Rkvdec_Swreg171_ref7_base	0x02ac	W	0x00000000	Base address for reference picture index7.
Rkvdec_Swreg171_vp9_intercmd_base	0x02ac	W	0x00000000	Inter cmd base addr.
Rkvdec_Swreg172_h26x_ref8_base	0x02b0	W	0x00000000	Base address for reference picture index8.
Rkvdec_Swreg172_vp9_update_prob_wr_base	0x02b0	W	0x00000000	Hardware parse prob: Used as vp9 prob write base.
Rkvdec_Swreg173_h26x_ref9_base	0x02b4	W	0x00000000	Base address for reference picture index9.
Rkvdec_Swreg174_h26x_ref10_base	0x02b8	W	0x00000000	Base address for reference picture index10.
Rkvdec_Swreg175_h26x_ref11_base	0x02bc	W	0x00000000	Base address for reference picture index11.
Rkvdec_Swreg176_h26x_ref12_base	0x02c0	W	0x00000000	Base address for reference picture index12.
Rkvdec_Swreg177_h26x_ref13_base	0x02c4	W	0x00000000	Base address for reference picture index13.
Rkvdec_Swreg178_h26x_ref14_base	0x02c8	W	0x00000000	Base address for reference picture index14.
Rkvdec_Swreg179_h26x_ref15_base	0x02cc	W	0x00000000	Base address for reference picture index15.
Rkvdec_Swreg180_scanlist_addr	0x02d0	W	0x00000000	The addr for scanlist table.
Rkvdec_Swreg181_colmv_ref0_base	0x02d4	W	0x00000000	Ref0 frame colmv base addr.

Rkvdec_Swreg182_colmv_ref1_base	0x02d8	W	0x00000000	Ref1 frame colmv base addr.
Rkvdec_Swreg183_colmv_ref2_base	0x02dc	W	0x00000000	Ref2 frame colmv base addr.
Rkvdec_Swreg184_colmv_ref3_base	0x02e0	W	0x00000000	Ref3 frame colmv base addr.
Rkvdec_Swreg185_colmv_ref4_base	0x02e4	W	0x00000000	Ref4 frame colmv base addr.
Rkvdec_Swreg186_colmv_ref5_base	0x02e8	W	0x00000000	Ref5 frame colmv base addr.
Rkvdec_Swreg187_colmv_ref6_base	0x02ec	W	0x00000000	Ref6 frame colmv base addr.
Rkvdec_Swreg188_colmv_ref7_base	0x02f0	W	0x00000000	Ref7 frame colmv base addr.
Rkvdec_Swreg189_colmv_ref8_base	0x02f4	W	0x00000000	Ref8 frame colmv base addr.
Rkvdec_Swreg190_colmv_ref9_base	0x02f8	W	0x00000000	Ref9 frame colmv base addr.
Rkvdec_Swreg191_colmv_ref10_base	0x02fc	W	0x00000000	Ref10 frame colmv base addr.
Rkvdec_Swreg192_colmv_ref11_base	0x0300	W	0x00000000	Ref11 frame colmv base addr.
Rkvdec_Swreg193_colmv_ref12_base	0x0304	W	0x00000000	Ref12 frame colmv base addr.
Rkvdec_Swreg194_colmv_ref13_base	0x0308	W	0x00000000	Ref13 frame colmv base addr.
Rkvdec_Swreg195_colmv_ref14_base	0x030c	W	0x00000000	Ref14 frame colmv base addr.
Rkvdec_Swreg196_colmv_ref15_base	0x0310	W	0x00000000	Ref15 frame colmv base addr.

Rkvdec_Swreg197_cabactbl_base	0x0314	W	0x00000000	Hevc & H264: The base address of cabac table.
Rkvdec_Swreg224_sta_int	0x0380	W	0x00000000	Decoder status
Rkvdec_Swreg225_sta_err_info	0x0384	W	0x00000000	Error info status.
Rkvdec_Swreg226_sta_cabac_error_status	0x0388	W	0x00000000	Cabac error status.
Rkvdec_Swreg227_sta_colmv_error_ref_picidx	0x038c	W	0x00000000	Colmv error ref picidx.
Rkvdec_Swreg228_sta_cabac_error_ctu_offset	0x0390	W	0x00000000	Cabac error ctu offset.
Rkvdec_Swreg229_sta_saowr_ctu_offset	0x0394	W	0x00000000	When there is any error, it is for the position of sao decode output to busifd.
Rkvdec_Swreg230_sta_slice_dec_num	0x0398	W	0x00000000	Slice dec num
Rkvdec_Swreg231_sta_frame_error_ctu_num	0x039c	W	0x00000000	H264 and hevc error ctu number.
Rkvdec_Swreg232_sta_error_packet_num	0x03a0	W	0x00000000	Error packet number
Rkvdec_Swreg233_sta_err_ctu_num_in_roI	0x03a4	W	0x00000000	The error ctu num in roi.
Rkvdec_Swreg256_debug_perf_latency_ctrl0	0x0400	W	0x00000000	Axi performance latency module contrl register.
Rkvdec_Swreg257_debug_perf_latency_ctrl1	0x0404	W	0x00000000	Debug perf latency ctrl.
Rkvdec_Swreg258_debug_perf_rd_max_latency_num	0x0408	W	0x00000000	Read max latency number.

Rkvdec_Swreg259_perf_rd_latency_samp_num	0x040c	W	0x00000000	The number of bigger than configed threshold value.
Rkvdec_Swreg260_debug_perf_rd_latency_acc_sum	0x0410	W	0x00000000	Total sample number.
Rkvdec_Swreg261_debug_perf_rd_axi_total_byte	0x0414	W	0x00000000	The bandwidth of total read bytes.
Rkvdec_Swreg262_debug_perf_wr_axi_total_byte	0x0418	W	0x00000000	The bandwidth of total write bytes.
Rkvdec_Swreg263_debug_perf_working_cnt	0x041c	W	0x00000000	The total running cycle of current frame.
Rkvdec_Swreg265_debug_perf_sel	0x0424	W	0x00000000	Performance montor ctrl.
Rkvdec_Swreg266_debug_perf_cnt0	0x0428	W	0x00000000	Performance count value0.
Rkvdec_Swreg267_debug_perf_cnt1	0x042c	W	0x00000000	Performance count value1.
Rkvdec_Swreg268_debug_perf_cnt2	0x0430	W	0x00000000	Performance count value2.
Rkvdec_Swreg269_vp9_error_info	0x0434	W	0x00000000	Performance count value2.
Rkvdec_Swreg270_debug_qos_ctrl	0x0438	W	0x00000000	AXI bus hurry ctrl.
Rkvdec_Swreg271_debug_wait_cycle_qos	0x043c	W	0x00000000	Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr, it will give hurry.
Rkvdec_Swreg272_debug_int	0x0440	W	0x00000000	Debug info
Rkvdec_Swreg273_sta_b_frame_flag	0x0444	W	0x00000000	Register0003 Description

Rkvdec_Swreg274_pix_range_y	0x0448	W	0x00000000	It will montior current frame max or min pix value.
Rkvdec_Swreg275_pix_range_u	0x044c	W	0x00000000	It will montior current frame max or min pix value.
Rkvdec_Swreg276_pix_range_v	0x0450	W	0x00000000	It will montior current frame max or min pix value.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.7 VDPU346 Detail Registers Description

Rkvdec_Swreg0_id

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Prod_num Prod code
15:8	RO	0x00	Major_ver Major verision
7:0	RO	0x00	Minor_ver Minor version

Rkvdec_Swreg8_in_out

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	Sw_out_swap64_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
8	RW	0x0	Sw_out_cbcr_swap 1'b0: Cb(u) is in the lower address, cr(v) is in the higher address. 1'b1: Cb(u) is in the higher address,cr(v) is in the lower address. Sw_in_cbcr_swap is the same with sw_out_cbcr_swap.
7	RW	0x0	Sw_out_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words. 1'b1: 32 bit data words are swapped.
6	RW	0x0	Sw_out_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
5	RW	0x0	Sw_str_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
4	RW	0x0	Sw_str_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped.

3	RW	0x0	Sw_str_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
2	RW	0x0	Sw_in_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
1	RW	0x0	Sw_in_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words. 1'b1: 32 bit data words are swapped.
0	RW	0x0	Sw_in_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.

Rkvdec_Swreg9_dec_mode

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	Sw_dec_mode 10'd0: Hevc 10'd1: H264 10'd2: Vp9 10'd3: Avs2 Other: reversed

Rkvdec_Swreg10_dec_e

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format. HW will reset this when picture is processed stream error for vp9 & hevc & (h264 when sw_h264_error_mode is 1'b0).

Rkvdec_Swreg11_important_en

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sw_pix_range_det_e 1'b0: pix range detect disable 1'b1: pix range detect enable
23:22	RO	0x0	reserved
21	RW	0x0	Sw_force_softreset_valid When sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle. When sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle. We suggest such bit always be config to 0 except when soft want to force reset.
20	RW	0x0	Sw_softrst_en_p Softreset enable signal, write 1 to soft reset, write 0 invalid, puls register.
19:11	RO	0x0	reserved
10	RW	0x0	Sw_dec_e_rewrite_valid Sw_dec_e rewrite valid signal, maybe for only when buffer empty, restart the decoder use.
9:7	RO	0x0	reserved
6	RW	0x0	Sw_buf_empty_en Buffer empty interrupt enable, now is for no use.
5	RW	0x0	Sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	Sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status.

3	RO	0x0	reserved
2	RW	0x0	Sw_dec_e_strmd_clkgate_dis In streamd module, there contains HEVC, H264, VP9, AVS2 modules, when it is 1'b1, these modules will no auto clkgate.
1	RW	0x0	Sw_dec_clkgate_e 1'b0: Clock is running for all structures. 1'b1: Clock is gated for decoder structures that are not used.
0	RO	0x0	reserved

Rkvdec_Swreg12_sencodary_en
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	Sw_scanlist_addr_valid_en 1'b0 : Scanlsit addr get from pps table. 1'b1 : Scanlist addr get from config.
7	RW	0x0	Sw_wait_reset_en 1'b0: Hardware will auto reset when error occur. 1'b1: Wait software process reset when error occur.
6	RW	0x0	Sw_collect_info_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	Sw_error_info_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	Sw_buspr_slot_disable 1'b1: Bus prefetch slot manage disable.
3	RO	0x0	reserved
2	RW	0x0	Sw_fbc_e 1'b0: Fbc disable 1'b1: Fbc enable
1	RW	0x0	Sw_colmv_compress_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	Sw_wr_ddr_align_en 1'b1: Set to 1 only when hevc mode decoder.

Rkvdec_Swreg13_en_mode_set
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_filter_outbuf_mode active at sw_fbc_e=1 0: fbchead write ddr with 64byte align 1: fbchead write ddr not almost 64byte align
30	RO	0x0	reserved
29	RW	0x0	sw_rd_ctrl_prior_mode 1'b0 : rcb data prior higher than referance data 1'b1 : rcb data prior lower than referance data
28	RW	0x0	sw_rd_prior_mode 1'b0 : used default mode 1'b1 : used ctrl mode
27:25	RO	0x0	reserved
24	RW	0x0	Sw_cur_pic_is_idr All frame is I frame flag.
23:22	RO	0x0	reserved
21	RW	0x0	Sw_ycacherd_prior 1'b0: Y cacherd prior is higher than uv. 1'b1: Y cache prior is equal than uv. Fbc mode: Sw_head_prior_high_en. 1'b0: Fbc head fetch data prior normal. 1'b1: Fbc head fetch data prior high.
20:19	RO	0x0	reserved

18	RW	0x0	Sw_error_mode For H264/hevc/avs2: 1'b0: When there is any error, the hardware will stop the decoder and reset itself. 1'b1: When there is any error, the hardware will wait the end signal of deblocking and then reset request. It is recommend that when vp9, it is configed to 1'b0.
17:16	RO	0x0	reserved
15	RW	0x0	Sw_colmv_error_mode 1'b0: When there is any colmv error, the hardware will stop the decoder and reset itself. 1'b1: When there is any colmv error, the hardware will wait the end signal of deblocking and then reset itself.
14:13	RO	0x0	reserved
12	RW	0x0	Sw_allow_not_wr_unref_bframe 1'b1: If dec not referance b frame, will not write to ddr. If wan't to set this bit to 1, should set sw_scl_down_en=1 also. It only used in hevc and unsupport tile mode.
11:10	RO	0x0	reserved
9	RW	0x0	Sw_h26x_streamd_error_mode 1'b0: When there is any stream error, the streamd will stop the decoder and reset itself. 1'b1: When there is any stream error, the streamd will try to decode next slice.
8:7	RO	0x0	reserved

6	RW	0x0	Sw_stmerror_waitdecfifo_empty When it is 1'b0, the stream error process will no wait the ca2decfifo empty; when it is 1'b1, the stream error process will wait the ca2decfifo empty, when sw_dec_mode is HEVC and VP9. It always take effect. When sw_dec_mode is H264. It only take effect, when sw_h264_error_mode is 1'b0.
5:4	RO	0x0	reserved
3	RW	0x0	Sw_dec_commonirq_mode 1'b0: In H264 and vp9 mode, the interrrupt will wait strmd end pulse. 1'b1: In H264 and vp9 mode, the interrupt will not wait strmd end plus.
2:1	RO	0x0	reserved
0	RW	0x0	Sw_timeout_mode Timeout mode select. 1'b0: Time_cycles is 241'b1. 1'b1: Time_cycles is 181'b1.

Rkvdec_Swreg14_fbc_param_set
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	Sw_fbc_h264_exten_4or8_flag It was h264 mbaff flag. 1'b0: Not mabff 1'b1: Mabff
5:4	RO	0x0	reserved
3	RW	0x0	Sw_allow_16x8_cp_flag 1'b0: Not allow 1'b1: Allow The config value is depend on vop work mode.
2:1	RO	0x0	reserved
0	RW	0x0	Sw_fbc_force_uncompress 1'b0: Allow fbce compress yuv block. 1'b1: Force all yuv block use uncompress mode.

Rkvdec_Swreg15_stream_param_set
Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:5	RW	0x00	Sw_strm_start_bit Exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base).
4:2	RO	0x0	reserved
1	RW	0x0	Sw_rlc_mode 1'b0: Hw decodes video from bit stream. 1'b1: Hw decodes video from RLC input data.
0	RW	0x0	Sw_rlc_mode_direct_write Cabac decode output direct write enable. When this bit is enable, all the module other than cabac and busifd are not work.

Rkvdec_Swreg16_stream_len

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_stream_len Amount of stream 8bits in the input buffer, byte unitL. The max of sw_stream_len: min(65536x65536x1.5x1.5,4G) = 4G.

Rkvdec_Swreg17_slice_number

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:0	RW	0x0000000	Sw_slice_num Hevc: Slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame), just only used for rps read. The meaning from count from 1, so it will be in 1~200. H264: Slice number in a frame (0~4095, when it is 1, it real means 1 slice in a frame). Vp9: No use.

Rkvdec_Swreg18_y_hor_stride

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_y_hor_virstride Picture horizontal virtual stride (the unit is 128bit). The max is (4096x1.5 + 128) /16 = 0x188. Suggest this register to config to even for advance ddr performance. Fbc mode: Used for head hor virstirde. 2015.10.23, change from 9 bit to 10bit.

Rkvdec_Swreg19_uv_hor_stride

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_uv_hor_virstride Picture horizontal virtual stride (the unit is 128bit). The max is (4096x1.5 + 128) /16 = 0x188. Suggest this register to config to even for advance ddr performance.

Rkvdec_Swreg20_y_stride

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_y_virstride The output picture y virtual stride (the unit is 128bit). The max:min((65536x1.5 +128) x 65536,4G) = 4G. We can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4). 2015.10.23, change from 20bits to 21bits.

Rkvdec_Swreg20_fbc_payload_offset

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_fbc_payload_base_addr The offset should be 128bit align. [Note]: The payload will be store in the base: Sw_decout_base + Sw_payload_st_offset.
3:0	RO	0x0	reserved

Rkvdec_Swreg21_error_ctrl_set

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	Sw_roi_error_ctu_cal_en 1'b0: Disable 1'b1: Enable
23:8	RO	0x0	reserved
7:3	RW	0x00	Sw_picidx_replace Hevc: [4:1]: Default pic idx [0]: Invalid H264: [4:1]: Default pic idx [0]: Field mode, 0 is top field.
2	RW	0x0	Sw_error_deb_en 1'b0: Disable 1'b1: Enable Only valid when sw_error_prc_intra_mode_sel = 1'b1.
1	RW	0x0	Sw_error_intra_mode 1'b0: Use inter mode to proc error ctu. 1'b1: Use intra mode to proc error ctu.
0	RW	0x0	Sw_inter_error_prc_mode 1'b0: Mv used pred. 1'b1: Mv=0, and sw_error_ref_base will be used.

Rkvdec_Swreg22_err_roi_ctu_offset_start
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	Sw_roi_y_ctu_offset_st The start offset of ctu_y when roi check.
15:12	RO	0x0	reserved
11:0	RW	0x000	Sw_roi_x_ctu_offset_st The start offset of ctu_x when roi check.

Rkvdec_Swreg23_err_roi_ctu_offset_end

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	Sw_roi_y_ctu_offset_end The end offset of ctu_y when roi check.
15:12	RO	0x0	reserved
11:0	RW	0x000	Sw_roi_x_ctu_offset_end The end offset of ctu_x when roi check.

Rkvdec_Swreg24_cabac_error_en_lowbits

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_cabac_error_en_lowbits Cabac error enable config.

Rkvdec_Swreg25_cabac_error_en_highbits

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	Sw_cabac_error_en_highbits Cabac error enable high bits config.

Rkvdec_Swreg26_block_gating_en

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_reg_cfg_gating_en Field0000 Description
30:20	RO	0x0	reserved
19:16	RW	0x0	Sw_block_gating_en_level2 Every bits: 1'b0: Disable 1'b1: Enable auto gating
15:0	RW	0x0000	sw_block_gating_en Block gating enable ctrl flag.

Rkvdec_Swreg64_vp9_set

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_cprheader_offset Vp9 compressed header offset, at most 2000 probs, 10bit per prob, 20000 bit at most. Now is for no use, because it can read from the last syntax of the uncompressed header.

Rkvdec_Swreg64_h26x_set

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Sw_h264_first_slice_flag 1'b1: First packet in the frame, for h264 decode to read rps/pps data, because the first_mb_in_slice may be wrong, so need this syntax.
3	RW	0x0	Sw_h26x_stream_lastpacket When sw_h26x_stream_mode is 1'b1, sw_h26x_stream_lastpacket. 1'b0: This packet is not the last packet of frame. 1'b1: The packet is the last packet of frame.
2	RW	0x0	Sw_h26x_stream_mode 1'b0: Stream packet is slice by slice or frame by frame, should use sw_h26x_frame_orslice. 1'b1: Stream packet is random, should use sw_h26x_stream_last.
1	RW	0x0	Sw_h26x_rps_mode 1'b0: Hardware parse rps mode. 1'b1: Software parse rps mode.
0	RW	0x0	Sw_h26x_frame_orslice For H26x use 1'b0: Frame 1'b1: Slice When sw_h26x_streamd_mode is 1'b0, this register is valid.

Rkvdec_Swreg65_cur_poc
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_cur_poc The poc of the cur picture. For H264, it may be cur frame poc or cur top field poc.

Rkvdec_Swreg66_h264_cur_poc1

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_h264_cur_poc1 H264 cur poc for bottom field.

Rkvdec_Swreg67_vp9_segid_grp0

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid0_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid0_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid0_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid0_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid0_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid0_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid0_frame_qp_delta_en Frame_qp_delta feature enable.
0	RW	0x0	Sw_vp9segid_abs_delta Used to decide quant and loopfilter param.

Rkvdec_Swreg67_ref0_poc

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer0_poc Hevc & h264 & avs2: The poc of reference picture index 0.

Rkvdec_Swreg68_vp9_segid_grp1

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid1_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid1_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid1_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid1_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid1_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid1_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid1_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg68_ref1_poc

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer1_poc Hevc & h264 & avs2: The poc of reference picture index 1.

Rkvdec_Swreg69_vp9_segid_grp2

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid2_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid2_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid2_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid2_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid2_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid2_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid2_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg69_ref2_poc

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer2_poc Hevc & h264 & avs2: The poc of reference picture index 2.

Rkvdec_Swreg70_vp9_segid_grp3

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid3_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid3_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid3_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid3_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid3_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid3_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid3_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg70_ref3_poc
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer3_poc Hevc & h264 & avs2: The poc of reference picture index 3.

Rkvdec_Swreg71_vp9_segid_grp4
Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid4_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid4_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid4_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid4_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid4_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid4_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid4_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg71_ref4_poc
Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer4_poc Hevc & h264 & avs2: The poc of reference picture index 4.

Rkvdec_Swreg72_vp9_segid_grp5
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid5_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid5_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid5_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid5_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid5_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid5_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid5_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg72_ref5_poc
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer5_poc Hevc & h264 & avs2: The poc of reference picture index 5.

Rkvdec_Swreg73_vp9_segid_grp6
Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid6_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid6_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid6_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid6_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid6_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid6_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid6_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg73_ref6_poc

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer6_poc Hevc & h264 & avs2: The poc of reference picture index 6.

Rkvdec_Swreg74_vp9_segid_grp7

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	Sw_vp9segid7_frame_skip_en Frame skip feature enable.
21:20	RW	0x0	Sw_vp9segid7_referinfo Specifies segment i's reference_info which is used to get ref_frame[0].
19	RW	0x0	Sw_vp9segid7_referinfo_en Frame reference info enable.
18:12	RW	0x00	Sw_vp9segid7_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level.
11	RW	0x0	Sw_vp9segid7_frame_loopfitler_value_en Frame_loopfilter_value feature enable.
10:2	RW	0x000	Sw_vp9segid7_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant.
1	RW	0x0	Sw_vp9segid7_frame_qp_delta_en Frame_qp_delta feature enable.
0	RO	0x0	reserved

Rkvdec_Swreg74_ref7_poc

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer7_poc Hevc & h264 & avs2: The poc of reference picture index 7.

Rkvdec_Swreg75_vp9_info_lastframe

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RW	0x0	Sw_vp9_color_space_lastkeyframe Vp9 last keyframe color_space.
19	RW	0x0	Sw_vp9_last_widhheight_eqcur Last width and height equal cur frame.
18	RW	0x0	Sw_vp9_last_intra_only Vp9 last frame intra only flag, to give inter command use. It is for last_dec_frame.
17	RW	0x0	Sw_vp9_last_showframe For cal the flag use_prev_in_find_mv_refs which is to inter cmd. It is for last_dec_frame.
16	RW	0x0	Sw_segmentation_enable_lstframe 1'b1: Sw_segmentation_enable for last frame. It is for last_dec_frame.
15:14	RO	0x0	reserved
13:0	RW	0x0000	Sw_vp9_mode_deltas_lastframe Vp9 mode deltas It is for last dec frame.

Rkvdec_Swreg75_ref8_poc
Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer8_poc Hevc & h264: The poc of reference picture index 8.

Rkvdec_Swreg76_vp9_cprheader_config
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:3	RW	0x0	Sw_vp9_frame_reference_mode Frame_reference_mode specifies frame reference mode. SINGLE_REFERENCE = 0, COMPOUND_REFERENCE = 1, REFERENCE_MODE_SELECT = 2, REFERENCE_MODES = 3, When frame_reference_mode_flag0 is not present ,it equal to 0 by default. When frame_reference_mode_flag1 is not present ,it equal to 0 by default. frame_reference_mode = frame_reference_mode_flag0 == 0 ? frame_reference_mode_flag1 == 0 ? REFERENCE_MODE_SELECT : COMPOUND_REFERENCE) : SINGLE_REFERENCE

2:0	RW	0x0	Sw_vp9_tx_mode
			Tx_mode specifies frame transform mode.
			ONLY_4X4 = 0, // only 4x4 transform used.
			ALLOW_8X8 = 1, // allow block transform size up to 8x8.
			ALLOW_16X16 = 2, // allow block transform size up to 16x16.
			ALLOW_32X32 = 3, // allow block transform size up to 32x32.
			TX_MODE_SELECT = 4, // transform specified for each block.

Rkvdec_Swreg76_ref9_poc
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer9_poc Hevc & h264: The poc of reference picture index 9.

Rkvdec_Swreg77_vp9_intercmd_num
Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	Sw_vp9_intercmd_num When rlc_mode is 1'b1, for sw_vp9_intercmd_num. It's unit is 128bit. It count from 1.

Rkvdec_Swreg77_ref10_poc
Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer10_poc Hevc & h264: The poc of reference picture index 10.

Rkvdec_Swreg78_vp9_stream_size
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_vp9_stream_size The size of vp9 compressed header and compressed frame data. Its unit is byte. The real meaning the current frame size.

Rkvdec_Swreg78_ref11_poc
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer11_poc Hevc & h264: The poc of reference picture index 11.

Rkvdec_Swreg79_vp9_lastf_y_hor_virstride
Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_lastfy_hor_virstride Vp9 last frame y horizontal virstride. 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of last frame.

Rkvdec_Swreg79_ref12_poc
Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer12_poc Hevc & h264: The poc of reference picture index 12.

Rkvdec_Swreg80_vp9_lastf_uv_hor_virstride
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_lastfuv_hor_virstride Vp9 last frame uv horizontal virstride. 2015.10.23, change from 9bits to 10bits.

Rkvdec_Swreg80_ref13_poc
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer13_poc Hevc & h264: The poc of reference picture index 13.

Rkvdec_Swreg81_vp9_goldenf_y_hor_virstride
Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_goldenfy_hor_virstride Vp9 golden frame y horizontal virstride. 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of golden frame.

Rkvdec_Swreg81_ref14_poc
Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer14_poc Hevc & h264: The poc of reference picture index 14.

Rkvdec_Swreg82_vp9_golden_uv_hor_virstride
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_goldenuv_hor_virstride Vp9 golden uv horizontal virstirde. 2015.10.23, change from 9bits to 10bits.

Rkvdec_Swreg82_ref15_poc
Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer15_poc The poc of reference picture index 15. Used to hevc for mvc.

Rkvdec_Swreg83_vp9_altreff_y_hor_virstride
Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_altreffy_hor_virstride Vp9 altref frame y horizontal virstride. 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of after frame.

Rkvdec_Swreg83_ref16_poc
Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer16_poc H264: The poc of reference picture index 16. Hevc & vp9: Now is no use.

Rkvdec_Swreg84_vp9_altreff_uv_hor_virstride
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	sw_vp9_altreffuv_hor_virstride Vp9 altreff uv horizontal virstirde. 2015.10.23, change from 9bits to 10bits.

Rkvdec_Swreg84_ref17_poc
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer17_poc H264: The poc of reference picture index 17. Hevc & vp9: Now is no use.

Rkvdec_Swreg85_vp9_lastf_y_virstride
Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_vp9_lastfy_virstride Vp9 last frame y stride. 2015.10.23, change from 20bits to 21bits.

Rkvdec_Swreg85_ref18_poc

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer18_poc H264: The poc of reference picture index 18. Hevc & vp9: Now is no use.

Rkvdec_Swreg86_vp9_golden_y_virstride

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_vp9_goldeny_virstride Vp9 golden frame y stride. 2015.10.23, change from 20bits to 21bits.

Rkvdec_Swreg86_ref19_poc

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer19_poc H264: The poc of reference picture index 19. Hevc & vp9: Now is no use.

Rkvdec_Swreg87_vp9_altref_y_virstride

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_vp9_altrefy_virstride Vp9 altref frame y stride. Change from 20bits to 21bits.

Rkvdec_Swreg87_ref20_poc
Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer20_poc H264: The poc of reference picture index 20. Hevc & vp9: Now is no use.

Rkvdec_Swreg88_vp9_lref_hor_scale
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_lref_hor_scale Horizontal scaling factor for last reference picture. Sw_vp9_lref_hor_scale = (last_ref_width / cur_width) * 0x4000.

Rkvdec_Swreg88_ref21_poc
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer21_poc H264: The poc of reference picture index 21. Hevc & vp9: Now is no use.

Rkvdec_Swreg89_vp9_lref_ver_scale
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_lref_ver_scale Vertical scaling factor for last reference picture.

Rkvdec_Swreg89_ref22_poc
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer22_poc H264: The poc of reference picture index 22. Hevc & vp9: Now is no use.

Rkvdec_Swreg90_vp9_gref_hor_scale
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_gref_hor_scale Horizontal scaling factor for golden reference picture. Sw_vp9_gref_hor_scale = (golden_ref_width / cur_width) * 0x4000.

Rkvdec_Swreg90_ref23_poc
Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer23_poc H264: The poc of reference picture index 23. Hevc & vp9: Now is no use.

Rkvdec_Swreg91_vp9_gref_ver_scale
Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_gref_ver_scale Vertical scaling factor for golden reference picture.

Rkvdec_Swreg91_ref24_poc
Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer24_poc H264: The poc of reference picture index 24. Hevc & vp9: Now is no use.

Rkvdec_Swreg92_vp9_aref_hor_scale
Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_aref_hor_scale Horizontal scaling factor for alfter reference picture. Sw_vp9_gref_hor_scale = (alfter_ref_width / cur_width) * 0x4000.

Rkvdec_Swreg92_ref25_poc
Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer25_poc H264: The poc of reference picture index 25. Hevc & vp9: Now is no use.

Rkvdec_Swreg93_vp9_aref_ver_scale
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_vp9_aref_ver_scale Vertical scaling factor for alfter reference picture.

Rkvdec_Swreg93_ref26_poc
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer26_poc H264: The poc of reference picture index 26. Hevc & vp9: Now is no use.

Rkvdec_Swreg94_vp9_ref_deltas_lastframe
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_vp9_ref_deltas_lastframe Vp9 ref deltas of lastframe, for cal loopfilter filter type use.

Rkvdec_Swreg94_ref27_poc
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer27_poc H264: The poc of reference picture index 27. Hevc & vp9: Now is no use.

Rkvdec_Swreg95_ref28_poc
Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer28_poc H264: The poc of reference picture index 28. Hevc & vp9: Now is no use.

Rkvdec_Swreg96_ref29_poc
Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer29_poc H264: The poc of reference picture index 29. Hevc & vp9: Now is no use.

Rkvdec_Swreg97_ref30_poc
Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer30_poc H264: The poc of reference picture index 30. Hevc & vp9: Now is no use.

Rkvdec_Swreg98_ref31_poc
Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_refer31_poc H264: The poc of reference picture index 31. Hevc & vp9: Now is no use.

Rkvdec_Swreg99_hevc_ref_valid
Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	Sw_hevc_ref_valid_14 Valid flag for picture index 14.
25	RW	0x0	Sw_hevc_ref_valid_13 Valid flag for picture index 13.
24	RW	0x0	Sw_hevc_ref_valid_12 Valid flag for picture index 12.
23:20	RO	0x0	reserved
19	RW	0x0	Sw_hevc_ref_valid_11 Valid flag for picture index 11.
18	RW	0x0	Sw_hevc_ref_valid_10 Valid flag for picture index 10.
17	RW	0x0	Sw_hevc_ref_valid_9 Valid flag for picture index 9.
16	RW	0x0	Sw_hevc_ref_valid_8 Valid flag for picture index 8.
15:12	RO	0x0	reserved
11	RW	0x0	Sw_hevc_ref_valid_7 Valid flag for picture index 7.
10	RW	0x0	Sw_hevc_ref_valid_6 Valid flag for picture index 6.
9	RW	0x0	Sw_hevc_ref_valid_5 Valid flag for picture index 5.
8	RW	0x0	Sw_hevc_ref_valid_4 Valid flag for picture index 4.

7:4	RO	0x0	reserved
3	RW	0x0	Sw_hevc_ref_valid_3 Valid flag for picture index 3.
2	RW	0x0	Sw_hevc_ref_valid_2 Valid flag for picture index 2.
1	RW	0x0	Sw_hevc_ref_valid_1 Valid flag for picture index 1.
0	RW	0x0	Sw_hevc_ref_valid_0 Valid flag for picture index 0.

Rkvdec_Swreg99_h264_reg0_3_info
Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref3_colmv_use_flag Ref3 colmv use flag.
26	RW	0x0	Sw_ref3_botfield_used Ref3 bottom field is used, the same meaning with ref_valid.
25	RW	0x0	Sw_ref3_topfield_used Ref3 top field is used, the same meaning with ref_valid.
24	RW	0x0	Sw_ref3_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref2_colmv_use_flag Ref2 colmv use flag.
18	RW	0x0	Sw_ref2_botfield_used Ref2 bottom field is used, the same meaning with ref_valid.
17	RW	0x0	Sw_ref2_topfield_used Ref2 top field is used, the same meaning with ref_valid.
16	RW	0x0	Sw_ref2_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref1_colmv_use_flag Ref1 colmv use flag.
10	RW	0x0	Sw_ref1_botfield_used Ref1 bottom field is used, the same meaning with ref_valid.

9	RW	0x0	Sw_ref1_topfield_used Ref1 top field is used, the same meaning with ref_valid.
8	RW	0x0	Sw_ref1_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref0_colmv_use_flag Ref0 colmv use flag.
2	RW	0x0	Sw_ref0_botfield_used Ref0 bottom field is used, the same meaning with ref_valid.
1	RW	0x0	Sw_ref0_topfield_used Ref0 top field is used, the same meaning with ref_valid.
0	RW	0x0	Sw_ref0_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg99_avs2_reg0_3_info
Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref3_valid_flag Reference picture3 used flag. 1'b0: Not be valid 1'b1: Be valid
26	RW	0x0	Sw_ref3_botfield_used Refer3 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
25	RO	0x0	reserved
24	RW	0x0	Sw_ref3_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref2_valid_flag Reference picture2 used flag. 1'b0: Not be valid 1'b1: Be valid
18	RW	0x0	Sw_ref2_botfield_used Refer2 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
17	RO	0x0	reserved
16	RW	0x0	Sw_ref2_field 1'b0: Frame 1'b1: Field

15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref1_valid_flag Reference picture1 used flag. 1'b0: Not be valid 1'b1: Be valid
10	RW	0x0	Sw_ref1_botfield_used Refer1 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
9	RO	0x0	reserved
8	RW	0x0	Sw_ref1_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref0_valid_flag Reference picture0 used flag. 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref0_botfield_used Refer0 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	reserved
0	RW	0x0	Sw_ref0_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg100_avs2_reg4_7_info

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref7_valid_flag Reference picture7 used flag. 1'b0: Not be valid 1'b1: Be valid
26	RW	0x0	Sw_ref7_botfield_used Refer7 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
25	RO	0x0	reserved
24	RW	0x0	Sw_ref7_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref6_valid_flag Reference picture6 used flag. 1'b0: Not be valid 1'b1: Be valid
18	RW	0x0	Sw_ref6_botfield_used Refer6 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
17	RO	0x0	reserved
16	RW	0x0	Sw_ref6_field 1'b0: Frame 1'b1: Field

15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref5_valid_flag Reference picture5 used flag. 1'b0: Not be valid 1'b1: Be valid
10	RW	0x0	Sw_ref5_botfield_used Refer5 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
9	RO	0x0	reserved
8	RW	0x0	Sw_ref5_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref4_valid_flag Reference picture4 used flag. 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	Sw_ref4_botfield_used Refer4 is bottow field flag. 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	reserved
0	RW	0x0	Sw_ref4_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg100_h264_reg4_7_info

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref7_colmv_use_flag Ref7 colmv use flag.
26	RW	0x0	Sw_ref7_botfield_used Ref7 bottom field is used, the same meaning with ref_valid.
25	RW	0x0	Sw_ref7_topfield_used Ref7 top field is used, the same meaning with ref_valid.
24	RW	0x0	Sw_ref7_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref6_colmv_use_flag Ref6 colmv use flag.
18	RW	0x0	Sw_ref6_botfield_used Ref6 bottom field is used, the same meaning with ref_valid.
17	RW	0x0	Sw_ref6_topfield_used Ref6 top field is used, the same meaning with ref_valid.
16	RW	0x0	Sw_ref6_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref5_colmv_use_flag Ref5 colmv use flag.
10	RW	0x0	Sw_ref5_botfield_used Ref5 bottom field is used, the same meaning with ref_valid.

9	RW	0x0	Sw_ref5_topfield_used Ref5 top field is used, the same meaning with ref_valid.
8	RW	0x0	Sw_ref5_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref4_colmv_use_flag Ref4 colmv use flag.
2	RW	0x0	Sw_ref4_botfield_used Ref4 bottom field is used, the same meaning with ref_valid.
1	RW	0x0	Sw_ref4_topfield_used Ref4 top field is used, the same meaning with ref_valid.
0	RW	0x0	Sw_ref4_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg101_h264_reg8_11_info
Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref11_colmv_use_flag Ref11 colmv use flag.
26	RW	0x0	Sw_ref11_botfield_used Ref11 bottom field is used, the same meaning with ref_valid.
25	RW	0x0	Sw_ref11_topfield_used Ref11 top field is used, the same meaning with ref_valid.
24	RW	0x0	Sw_ref11_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref10_colmv_use_flag Ref10 colmv use flag.
18	RW	0x0	Sw_ref10_botfield_used Ref10 bottom field is used, the same meaning with ref_valid.
17	RW	0x0	Sw_ref10_topfield_used Ref10 top field is used, the same meaning with ref_valid.
16	RW	0x0	Sw_ref10_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref9_colmv_use_flag Ref9 colmv use flag.
10	RW	0x0	Sw_ref9_botfield_used Ref9 bottom field is used, the same meaning with ref_valid.

9	RW	0x0	Sw_ref9_topfield_used Ref9 top field is used, the same meaning with ref_valid.
8	RW	0x0	Sw_ref9_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref8_colmv_use_flag Ref8 colmv use flag.
2	RW	0x0	Sw_ref8_botfield_used Ref8 bottom field is used, the same meaning with ref_valid.
1	RW	0x0	Sw_ref8_topfield_used Ref8 top field is used, the same meaning with ref_valid.
0	RW	0x0	Sw_ref8_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg102_h264_reg12_15_info
Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	Sw_ref15_colmv_use_flag Ref15 colmv use flag.
26	RW	0x0	Sw_ref15_botfield_used Ref15 bottom field is used, the same meaning with ref_valid.
25	RW	0x0	Sw_ref15_topfield_used Ref15 top field is used, the same meaning with ref_valid.
24	RW	0x0	Sw_ref15_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	Sw_ref14_colmv_use_flag Ref14 colmv use flag.
18	RW	0x0	Sw_ref14_botfield_used Ref14 bottom field is used, the same meaning with ref_valid.
17	RW	0x0	Sw_ref14_topfield_used Ref14 top field is used, the same meaning with ref_valid.
16	RW	0x0	sw_ref14_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	Sw_ref13_colmv_use_flag Ref13 colmv use flag.
10	RW	0x0	Sw_ref13_botfield_used Ref13 bottom field is used, the same meaning with ref_valid.

9	RW	0x0	Sw_ref13_topfield_used Ref13 top field is used, the same meaning with ref_valid.
8	RW	0x0	Sw_ref13_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	Sw_ref12_colmv_use_flag Ref12 colmv use flag.
2	RW	0x0	Sw_ref12_botfield_used Ref12 bottom field is used, the same meaning with ref_valid.
1	RW	0x0	Sw_ref12_topfield_used Ref12 top field is used, the same meaning with ref_valid.
0	RW	0x0	Sw_ref12_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg103_vp9_prob_en
Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31	RW	0x0	Sw_vp9_inter_coef_rfsh_flag 1'b0: Inter coef unneed refresh in current intra frame. 1'b1: Inter coef should be refresh in current intra frame.
30	RW	0x0	Sw_vp9_last_key_frame_flag The flag of last frame is key frame. 1'b0: Not key frame. 1'b1: Key frame.
29	RW	0x0	Sw_vp9_allow_high_precision_mv The enable of high precision mv prob refresh update. 1'b0: Disable 1'b1: Enable
28	RW	0x0	Sw_vp9_interp_filter_switch_en The enable of interp filter prob refresh update. 1'b0: Disable 1'b1: Enable
27	RW	0x0	Sw_vp9_comp_ref_rfsh_en The enable of comp reference prob refresh update. 1'b0: Disable 1'b1: Enable
26	RW	0x0	Sw_vp9_single_ref_rfsh_en The enable of single reference prob refresh update. 1'b0: Disable 1'b1: Enable
25	RW	0x0	Sw_vp9_ref_mode_rfsh_en The enable of reference mode prob refresh update. 1'b0: Disable 1'b1: Enable

24	RW	0x0	Sw_vp9_txfmmode_rfsh_en The enable of tx mode prob refresh update. 1'b0: Disable 1'b1: Enable
23	RW	0x0	Sw_vp9_intra_only_flag The flag of intra only. 1'b0: Inter frame. 1'b1: Intra only frame（include key frame）.
22	RW	0x0	Sw_vp9_prob_save_en The flag of write updated prob to DDR. 1'b0: Not need write updated prob to DDR. 1'b1: Will write updated prob to DDR.
21	RW	0x0	Sw_vp9_refresh_en The enbale of prob backward refresh. 1'b0: Disable refresh parse. 1'b1: Enable refresh parse.
20	RW	0x0	Sw_vp9_prob_update_en The enable of used hardware to parse prob. 1'b0: Software parse prob. 1'b1: Hardware parse prob.
19:0	RO	0x0	reserved

Rkvdec_Swreg103_hevc_mvc0

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_ref_pic_layer_same_with_cur Referance picture layer same with current picture.

Rkvdec_Swreg103_avs2_ctrl_extra

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Sw_avs2_slice_hor_pos_ctrl 1'b0: Use default 255. 1'b1: Use fixed 256.

Rkvdec_Swreg104_hevc_mvc1

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	Sw_mvc_poc15_valid_flag Mvc poc15 valid flag.
17	RW	0x0	Sw_rps_poc_lsb_aligned_flag Rps POC lsb aligned flag.
16	RW	0x0	Sw_poc_reset_info_present_flag The flag of poc reset infomation.
15	RW	0x0	Sw_max_one_active_ref_layer_flag The flag of max referance referance layer be actived.
14	RW	0x0	Sw_default_ref_layers_active_flag The flag of default referance layers which be actived.
13:8	RW	0x00	Sw_num_reflayer_pics The number of referance layer pictures.
7	RO	0x0	reserved
6:1	RW	0x00	Sw_num_direct_ref_layers The number of direct referance layers.
0	RW	0x0	Sw_poc_lsb_not_present_flag Poc lsb not present flag.

Rkvdec_Swreg105_vp9cnt_upd_en_avs2_headlen
Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Sw_vp9count_update_en When 1'b1, the hardware will always update count. When 1'b0, the hardware will auto check whether update the count.
3:0	RW	0x0	Sw_avs2_head_len It's unit is 128bit. 4'd0: 128bit 4'd1: 2*128bit 4'd2: 3*128bit ..... 4'd15: 16*128bit

Rkvdec_Swreg106_vp9_frame_width_last
Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_framewidth_last Last frame frame_size_width.

Rkvdec_Swreg107_vp9_frame_height_last
Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_frameheight_last Last frame frame_size_height.

Rkvdec_Swreg108_vp9_frame_width_golden
Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_framewidth_golden Golden frame_size_width

Rkvdec_Swreg109_vp9_frame_height_golden
Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_frameheight_golden Golden frame_size_height.

Rkvdec_Swreg110_vp9_frame_width_altref
Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_framewidth_alfter Alfter frame_size_width.

Rkvdec_Swreg111_vp9_frame_height_altref
Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	Sw_frameheight_alfter Alfter frame_size_height.

Rkvdec_Swreg112_error_ref_info
Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Sw_ref_error_botfield_used For inter, 1'b1: Botfield is used.
2	RW	0x0	Sw_ref_error_topfield_used For inter, 1'b1: Topfield is used.
1	RW	0x0	Sw_avs2_ref_error_topfield Refer error is top field flag. 1'b0: Bottom field flag. 1'b1: Top field flag.
0	RW	0x0	Sw_avs2_ref_error_field 1'b0: Frame 1'b1: Field

Rkvdec_Swreg128_strm_rlc_base
Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_strm_rlc_base When swreg2.sw_rlc_mode =1, it is base address for rlc data. When swreg2.sw_rlc_mode =0, it is base address for stream, after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream. The address should 128bit align.
3:0	RO	0x0	reserved

Rkvdec_Swreg129_rlcwrite_base
Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_rlcwrite_base The base address of rlcwrite(the address should 64bit align). Cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid.
2:0	RO	0x0	reserved

Rkvdec_Swreg129_error_info_base

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_error_info_base The base address of error info
2:0	RO	0x0	reserved

Rkvdec_Swreg130_decout_base

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_decout_base Base address of decoder output picture, the address should be 128bit align. In H264 decode format, the top field and bottom field are the same addr. Fbc mode: Fbc_head_base_addr[27:0]: the head base of fbc wr.
3:0	RO	0x0	reserved

Rkvdec_Swreg131_colmv_cur_base

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_cur_base Only valid when sw_colmv_mode is 1'b1. Cur frame colmv base addr, for HEVC,H264 and vp9.
3:0	RO	0x0	reserved

Rkvdec_Swreg132_error_ref_base

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_error_ref_base Error reference frame base address.
3:0	RO	0x0	reserved

Rkvdec_Swreg133_rcb_intrar_base

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_intrar_base Rcb intra row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg134_rcb_transdr_base

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_transdr_base Rcb transd row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg135_rcb_transdc_base

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_transdc_base Rcb transd col base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg136_rcb_strmdr_base

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_strmdr_base Rcb stream row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg137_rcb_interr_base

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_interr_base Rcb inter row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg138_rcb_interc_base

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_interc_base Rcb inter col base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg139_rcb_dblkr_base

Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_dblkr_base Rcb dblock row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg140_rcb_saor_base

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_saor_base Rcb sao row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg141_rcb_fbcr_base

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_fbcr_base Rcb fbc row base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg142_rcb_filtc_col_base

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Sw_rcb_filtc_base Rcb filter col base address, unit: 64byts align.
5:0	RO	0x0	reserved

Rkvdec_Swreg160_vp9_delta_prob_base

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_delta_prob_base The base address of prob.
3:0	RO	0x0	reserved

Rkvdec_Swreg161_avs2_head_base

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_avs2_head_base The base address of avs2 head (the address should 128bit align). It will include sequence and picture level syntax.
3:0	RO	0x0	reserved

Rkvdec_Swreg161_pps_base

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_pps_base The base address of pps (the address should 128bit align). It is for storing sps(sequence parameter set) and pps(picture parameter set).
3:0	RO	0x0	reserved

Rkvdec_Swreg162_vp9_last_prob_base

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_last_porb_base The base address of last prob (the address should 128bit align).
3:0	RO	0x0	reserved

Rkvdec_Swreg163_rps_base

Address: Operational Base + offset (0x028c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_rps_base Rps(reference picture set) base address (the address should 128bit align).
3:0	RO	0x0	reserved

Rkvdec_Swreg164_vp9_referlast_base

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_last_base Base address for last (the address should be 128bit align). Fbc mode: Vp9 last ref frame head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg164_ref0_base

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer0_base Base address for reference picture index0 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref0 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg165_vp9_refergolden_base

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9golden_base Base address for golden (the address should be 128bit align). Fbc mode: Vp9 golden ref frame head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg165_ref1_base

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer1_base Base address for reference picture index1 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref1 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg166_vp9_referalfter_base

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9alfter_base Base address for alfter (the address should be 128bit align). Fbc mode: Vp9 after ref frame head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg166_ref2_base

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer2_base Base address for reference picture index2 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref2 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg167_ref3_base

Address: Operational Base + offset (0x029c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer3_base Base address for reference picture index3 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref3 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg167_vp9count_base

Address: Operational Base + offset (0x029c)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Sw_vp9_count_prob_base Software parse prob: Used as vp9 count write base.
2:0	RO	0x0	reserved

Rkvdec_Swreg168_ref4_base

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer4_base Base address for reference picture index4 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref4 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg168_vp9_segidlast_base

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9segidlast_base Base address for vp9 last frame segment id (the address should be 128bit align).
3:0	RO	0x0	reserved

Rkvdec_Swreg169_ref5_base

Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer5_base Base address for reference picture index5 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref5 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg169_avp9_segidcur_base

Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9segidcur_base Base address for vp9 cur frame segment id (the address should be 128bit align).
3:0	RO	0x0	reserved

Rkvdec_Swreg170_ref6_base

Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer6_base Base address for reference picture index6 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref6 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg170_vp9_refcolmv_base
Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_refcolmv_base Vp9 refcolmv base addr.
3:0	RO	0x0	reserved

Rkvdec_Swreg171_ref7_base
Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer7_base Base address for reference picture index7 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref7 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg171_vp9_intercmd_base
Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_intercmd_base Vp9 inter command base addr, when sw_rlc_mode is 1'b1. When sw_dec_mode is VP9 and sw_rlc_mode is 1'b1, when read this register, after a frame is decoded ready or error (stream error, time out, bus error), it is the end address of the intercmd.
3:0	RO	0x0	reserved

Rkvdec_Swreg172_h26x_ref8_base
Address: Operational Base + offset (0x02b0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer8_base Base address for reference picture index8 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref8 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg172_vp9_update_prob_wr_base

Address: Operational Base + offset (0x02b0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_vp9_update_prob_wr_base Hardware parse prob: Used as vp9 prob write base.
3:0	RO	0x0	reserved

Rkvdec_Swreg173_h26x_ref9_base

Address: Operational Base + offset (0x02b4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer9_base Base address for reference picture index9 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref9 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg174_h26x_ref10_base

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer10_base Base address for reference picture index10 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref10 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg175_h26x_ref11_base

Address: Operational Base + offset (0x02bc)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer11_base Base address for reference picture index11 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref11 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg176_h26x_ref12_base

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer12_base Base address for reference picture index12 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref12 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg177_h26x_ref13_base

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer13_base Base address for reference picture index13 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref13 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg178_h26x_ref14_base

Address: Operational Base + offset (0x02c8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer14_base Base address for reference picture index14 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref14 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg179_h26x_ref15_base

Address: Operational Base + offset (0x02cc)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_refer15_base Base address for reference picture index15 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref15 head base.
3:0	RO	0x0	reserved

Rkvdec_Swreg180_scanlist_addr

Address: Operational Base + offset (0x02d0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_scanlist_addr Should be align to 16byte, and will be used for h264 and hevc.
3:0	RO	0x0	reserved

Rkvdec_Swreg181_colmv_ref0_base

Address: Operational Base + offset (0x02d4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref0_base Only valid when sw_colmv_mode is 1'b1. Ref0 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg182_colmv_ref1_base

Address: Operational Base + offset (0x02d8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref1_base Only valid when sw_colmv_mode is 1'b1. Ref1 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg183_colmv_ref2_base
Address: Operational Base + offset (0x02dc)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref2_base Only valid when sw_colmv_mode is 1'b1. Ref2 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg184_colmv_ref3_base
Address: Operational Base + offset (0x02e0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref3_base Only valid when sw_colmv_mode is 1'b1. Ref3 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg185_colmv_ref4_base
Address: Operational Base + offset (0x02e4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref4_base Only valid when sw_colmv_mode is 1'b1. Ref4 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg186_colmv_ref5_base
Address: Operational Base + offset (0x02e8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref5_base Only valid when sw_colmv_mode is 1'b1. Ref5 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg187_colmv_ref6_base
Address: Operational Base + offset (0x02ec)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref6_base Only valid when sw_colmv_mode is 1'b1. Ref6 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg188_colmv_ref7_base
Address: Operational Base + offset (0x02f0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref7_base Only valid when sw_colmv_mode is 1'b1. Ref7 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg189_colmv_ref8_base
Address: Operational Base + offset (0x02f4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref8_base Only valid when sw_colmv_mode is 1'b1. Ref8 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg190_colmv_ref9_base
Address: Operational Base + offset (0x02f8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref9_base Only valid when sw_colmv_mode is 1'b1. Ref9 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg191_colmv_ref10_base
Address: Operational Base + offset (0x02fc)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref10_base Only valid when sw_colmv_mode is 1'b1. Ref10 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg192_colmv_ref11_base
Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref11_base Only valid when sw_colmv_mode is 1'b1. Ref11 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg193_colmv_ref12_base
Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref12_base Only valid when sw_colmv_mode is 1'b1. Ref12 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg194_colmv_ref13_base
Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref13_base Only valid when sw_colmv_mode is 1'b1. Ref13 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg195_colmv_ref14_base
Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref14_base Only valid when sw_colmv_mode is 1'b1. Ref14 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg196_colmv_ref15_base
Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_colmv_ref15_base Only valid when sw_colmv_mode is 1'b1. Ref15 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

Rkvdec_Swreg197_cabactbl_base
Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Sw_cabactbl_base Hevc & H264: The base address of cabac table.
3:0	RO	0x0	reserved

Rkvdec_Swreg224_sta_int
Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	Sw_softreset_rdy When it is 1'b1, it says that softreset has been done.
8	RW	0x0	Sw_cabu_end_sta Hevc: Cabac decode end status. H264 & vp9 : Streamd decode status.
7	RW	0x0	Sw_colmv_ref_error_sta Hevc & vp9: When it is 1'b1, it means that inter module read the invalid dpb frame. It will self reset the hardware. H264: When it is 1'b1, it means that inter module read the invalid dpb frame. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.
6	RW	0x0	Sw_buf_empty_sta Buffer empty status, only when sw_buf_empty_en is 1'b1 , this bit is valid, now is for no valid.
5	RW	0x0	Sw_dec_timeout_sta When high the decoder has been idling for too long. It will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid.
4	RW	0x0	Sw_dec_error_sta Hevc & vp9: When high, an error is found in input data stream decoding. It will self reset the hardware. H264: When high, an error is found in input data stream decoding. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.
3	RW	0x0	Sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware.

2	RW	0x0	Sw_dec_rdy_sta When this bit is high, decoder has decoded a picture(the loop filter module send out a frame rdy).
1	RW	0x0	Sw_dec_irq_raw The raw status of sw_dec_irq,SW should reset this bit after interrupt is handled.
0	RW	0x0	Sw_dec_irq When high, decoder requests an interrrupt. Sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0).

Rkvdec_Swreg225_sta_err_info

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	Sw_strmd_detect_error_sta Streamd logic error detected, it will stop decode.
0	RW	0x0	Sw_dec_frame_error_sta 1'b1: All frame ctu error.

Rkvdec_Swreg226_sta_cabac_error_status

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	Sw_cabac_error_status In HEVC & H264, it is called cabac error status.

Rkvdec_Swreg227_sta_colmv_error_ref_picidx

Address: Operational Base + offset (0x038c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	Sw_colmv_ref_picidx When sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module. It is for H264 and HEVC.

Rkvdec_Swreg228_sta_cabac_error_ctu_offset

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	Sw_cabac_error_ctu_offset_y For all HEVC and H264 and VP9. For vp9, it is the value of stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x.
15:12	RO	0x0	reserved
11:0	RW	0x000	Sw_cabac_error_ctu_offset_x For all HEVC and H264 and VP9. For vp9, it is the value of stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x.

Rkvdec_Swreg229_sta_saowr_ctu_offset

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Sw_saowr_yoffset Saowr y offset , its unit is 4 line pixel. 16'd0: Sao begin to write 0~3 pic line. 16'd1: Sao begin to write 4-7 pic line. ..... Only valid when ip has any error.
15:0	RW	0x0000	Sw_saowr_xoffet Saowr x address offset, its unit is 128bit. 16'd0: Sao begin to write cur line first 128bit. 16'd1: Sao begin to write cur line second 128bit. ..... Only valid when ip has any error.

Rkvdec_Swreg230_sta_slice_dec_num
Address: Operational Base + offset (0x0398)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:0	RO	0x0000000	Sw_slicedec_num H264 decoded num, the max slice num for H264 is 4096.

Rkvdec_Swreg231_sta_frame_error_ctu_num
Address: Operational Base + offset (0x039c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	Sw_frame_ctu_error_num H264 and hevc error ctu number

Rkvdec_Swreg232_sta_error_packet_num
Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	Sw_error_packet_num Error packet number.

Rkvdec_Swreg233_sta_err_ctu_num_in_roI
Address: Operational Base + offset (0x03a4)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RO	0x000000	Sw_error_ctu_num_in_roi The error ctu num in roi.

Rkvdec_Swreg256_debug_perf_latency_ctrl0
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	Sw_rd_latency_thr Rd channel latency threshold.
15:12	RO	0x0	reserved
11:4	RW	0x00	Sw_rd_latency_id Rd channel id for performance test.
3	RW	0x0	Sw_axi_cnt_type 1'b0: Axi transfer num count. 1'b1: Ddr align transfer num count.
2	RO	0x0	reserved
1	RW	0x0	Sw_axi_perf_clr 1'b0: Software clear disable. 1'b1: Software clear enalbe. Clear pulse.
0	RW	0x0	Sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

Rkvdec_Swreg257_debug_perf_latency_ctrl1
Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	Sw_rd_band_width_mode 1'b0: Cal all id. 1'b1: Cal sw_ar_count_id.
23:16	RW	0x00	Sw_aw_count_id Sw_aw_count_id
15:12	RO	0x0	reserved
11:4	RW	0x00	Sw_ar_count_id Sw_ar_count_id
3	RW	0x0	Sw_aw_cnt_id_type 1'b0: Count all wr-channels. 1'b1: Count sw_wr_cont_id wr-channel only.
2	RW	0x0	Sw_ar_cnt_id_type 1'b0: Count all rd-channels. 1'b1: Count sw_ar_cont_id rd-channel only.
1:0	RW	0x0	Sw_addr_align_type 2'd0: 16 byte align. 2'd1: 32byte align. 2'd2: 64byte align. 2'd3: 128byte align.

Rkvdec_Swreg258_debug_perf_rd_max_latency_num

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Sw_rd_max_latency_num Read max latency number.

Rkvdec_Swreg259_perf_rd_latency_samp_num

Address: Operational Base + offset (0x040c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_rd_latency_samp_num The number of bigger than configed threshold value.

Rkvdec_Swreg260_debug_perf_rd_latency_acc_sum

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_rd_latency_acc_sum Total sample number.

Rkvdec_Swreg261_debug_perf_rd_axi_total_byte

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_rd_axi_total_byte The bandwidth of total read bytes.

Rkvdec_Swreg262_debug_perf_wr_axi_total_byte

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_wr_axi_total_byte The bandwidth of total write bytes.

Rkvdec_Swreg263_debug_perf_working_cnt

Address: Operational Base + offset (0x041c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_working_cnt The total running cycle of current frame.

Rkvdec_Swreg265_debug_perf_sel

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

21:16	RW	0x00	Sw_perf_cnt2_sel 6'd0: Don't work. 6'd1: Cycles counter for cabac in buffer empty. 6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'd3: Cycles counter for cabac out buffer empty. 6'd4: Cycles counter for cabac out buffer full. 6'd5: Cycles counter for transd input data ready. 6'd6: Cycles counter for transd write data to recon allow. 6'd7: Cycles counter for dec2transd cmd empty. 6'd8: Cycles counter for dec2transd cmd full. 6'd9: Cycles counter for transd2dblk bs fifo empty. 6'd10: Cycles counter for transd2dblk bs fifo full. 6'd11: Cycles counter for dec2intra cmd fifo empty. 6'd12: Cycles counter for dec2intra cmd fifo full. 6'd13: Cycles counter for mc2recon cmd fifo empty. 6'd14: Cycles counter for mc2recon cmd fifo full. 6'd15: Cycles counter for mc2recon data fifo empty. 6'd16: Cycles counter for mc2recon data fifo full. 6'd17: Cycles counter for recon2filter data write allow. 6'd18: Cycles counter for inter2busifd cmd fifo empty. 6'd19: Cycles counter for inter2busifd cmd fifo full. 6'd20: Cycles counter for busifd2mc data fifo empty. 6'd21: Cycles counter for busifd2mc data fifo full. 6'd22: Cycles counter for bus un-working status(idle status). 6'd23: Cycles counter for dec2inter cmd fifo empty. 6'd24: Cycles counter for dec2inter cmd fifo full. 6'd25: Cycles counter for inter2mc cmd fifo empty. 6'd26: Cycles counter for inter2mc cmd fifo full. 6'd27: Cycles counter for inter2dblk bs fifo empty. 6'd28: Cycles counter for inter2dblk bs fifo full.

			6'd29: Cycles counter for colmv_rbuf_empty. 6'd30: Cycles counter for colmv_rbuf_full. 6'd31: Cycles counter for colmv_wbuf_empty. 6'd32: Cycles counter for colmv_wbuf_da_full. 6'd33: Cycles counter for dblk work status. 6'd34: Cycles counter for dblk work status. 6'd35: Cycles counter for dec2loopfilter cmd fifo empty. 6'd36: Cycles counter for dec2loopfilter cmd fifo full. 6'd37: Cycles counter for sao input data valid. 6'd38: Cycles counter for busifd hold back sao write data. 6'd39: Cycles counter for bus process writing output buffer data. 6'd40: Counter for dec_ctrl read cmd num. 6'd41: Error ctu num when stream error happen. 6'd42: Inter reflist idx which be used flag. 6'd43: Pu num, 4*4 unit. 6'd44: mv_y_min[15:0], mv_x_min[15:0]. 6'd45: mv_y_max[15:0], mv_x_max[15:0]. 6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'd48: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'd49: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]. 6'd51: The cu skip num, unit is 8*8. 6'd52: The tu skip num, unit is 4*4. 6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]. 6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]. 6'd55: The sum of luma qp, unit is 4*4. 6'd56: The sum of cb qp, unit is 4*4. 6'd57: The sum of cr qp, unit is 4*4.

			6'd58: The count of mv_x. 6'd59: The count of mv_y.
15:14	RO	0x0	reserved

13:8	RW	0x00	Sw_perf_cnt1_sel 6'd0: Don't work. 6'd1: Cycles counter for cabac in buffer empty. 6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'd3: Cycles counter for cabac out buffer empty. 6'd4: Cycles counter for cabac out buffer full. 6'd5: Cycles counter for transd input data ready. 6'd6: Cycles counter for transd write data to recon allow. 6'd7: Cycles counter for dec2transd cmd empty. 6'd8: Cycles counter for dec2transd cmd full. 6'd9: Cycles counter for transd2dblk bs fifo empty. 6'd10: Cycles counter for transd2dblk bs fifo full. 6'd11: Cycles counter for dec2intra cmd fifo empty. 6'd12: Cycles counter for dec2intra cmd fifo full. 6'd13: Cycles counter for mc2recon cmd fifo empty. 6'd14: Cycles counter for mc2recon cmd fifo full. 6'd15: Cycles counter for mc2recon data fifo empty. 6'd16: Cycles counter for mc2recon data fifo full. 6'd17: Cycles counter for recon2filter data write allow. 6'd18: Cycles counter for inter2busifd cmd fifo empty. 6'd19: Cycles counter for inter2busifd cmd fifo full. 6'd20: Cycles counter for busifd2mc data fifo empty. 6'd21: Cycles counter for busifd2mc data fifo full. 6'd22: Cycles counter for bus un-working status(idle status). 6'd23: Cycles counter for dec2inter cmd fifo empty. 6'd24: Cycles counter for dec2inter cmd fifo full. 6'd25: Cycles counter for inter2mc cmd fifo empty. 6'd26: Cycles counter for inter2mc cmd fifo full. 6'd27: Cycles counter for inter2dblk bs fifo empty. 6'd28: Cycles counter for inter2dblk bs fifo full.

			6'd29: Cycles counter for colmv_rbuf_empty. 6'd30: Cycles counter for colmv_rbuf_full. 6'd31: Cycles counter for colmv_wbuf_empty. 6'd32: Cycles counter for colmv_wbuf_da_full. 6'd33: Cycles counter for dblk work status. 6'd34: Cycles counter for dblk work status. 6'd35: Cycles counter for dec2loopfilter cmd fifo empty. 6'd36: Cycles counter for dec2loopfilter cmd fifo full. 6'd37: Cycles counter for sao input data valid. 6'd38: Cycles counter for busifd hold back sao write data. 6'd39: Cycles counter for bus process writing output buffer data. 6'd40: Counter for dec_ctrl read cmd num. 6'd41: Error ctu num when stream error happen. 6'd42: Inter reflist idx which be used flag. 6'd43: Pu num, 4*4 unit. 6'd44: mv_y_min[15:0], mv_x_min[15:0]. 6'd45: mv_y_max[15:0], mv_x_max[15:0]. 6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'd48: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'd49: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]. 6'd51: The cu skip num, unit is 8*8. 6'd52: The tu skip num, unit is 4*4. 6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]. 6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]. 6'd55: The sum of luma qp, unit is 4*4. 6'd56: The sum of cb qp, unit is 4*4. 6'd57: The sum of cr qp, unit is 4*4.

			6'd58: The count of mv_x. 6'd59: The count of mv_y.
7:6	RO	0x0	reserved

5:0	RW	0x00	Sw_perf_cnt0_sel 6'd0: Don't work. 6'd1: Cycles counter for cabac in buffer empty. 6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'd3: Cycles counter for cabac out buffer empty. 6'd4: Cycles counter for cabac out buffer full. 6'd5: Cycles counter for transd input data ready. 6'd6: Cycles counter for transd write data to recon allow. 6'd7: Cycles counter for dec2transd cmd empty. 6'd8: Cycles counter for dec2transd cmd full. 6'd9: Cycles counter for transd2dblk bs fifo empty. 6'd10: Cycles counter for transd2dblk bs fifo full. 6'd11: Cycles counter for dec2intra cmd fifo empty. 6'd12: Cycles counter for dec2intra cmd fifo full. 6'd13: Cycles counter for mc2recon cmd fifo empty. 6'd14: Cycles counter for mc2recon cmd fifo full. 6'd15: Cycles counter for mc2recon data fifo empty. 6'd16: Cycles counter for mc2recon data fifo full. 6'd17: Cycles counter for recon2filter data write allow. 6'd18: Cycles counter for inter2busifd cmd fifo empty. 6'd19: Cycles counter for inter2busifd cmd fifo full. 6'd20: Cycles counter for busifd2mc data fifo empty. 6'd21: Cycles counter for busifd2mc data fifo full. 6'd22: Cycles counter for bus un-working status(idle status). 6'd23: Cycles counter for dec2inter cmd fifo empty. 6'd24: Cycles counter for dec2inter cmd fifo full. 6'd25: Cycles counter for inter2mc cmd fifo empty. 6'd26: Cycles counter for inter2mc cmd fifo full. 6'd27: Cycles counter for inter2dblk bs fifo empty. 6'd28: Cycles counter for inter2dblk bs fifo full.

			6'd29: Cycles counter for colmv_rbuf_empty. 6'd30: Cycles counter for colmv_rbuf_full. 6'd31: Cycles counter for colmv_wbuf_empty. 6'd32: Cycles counter for colmv_wbuf_da_full. 6'd33: Cycles counter for dblk work status. 6'd34: Cycles counter for dblk work status. 6'd35: Cycles counter for dec2loopfilter cmd fifo empty. 6'd36: Cycles counter for dec2loopfilter cmd fifo full. 6'd37: Cycles counter for sao input data valid. 6'd38: Cycles counter for busifd hold back sao write data. 6'd39: Cycles counter for bus process writing output buffer data. 6'd40: Counter for dec_ctrl read cmd num. 6'd41: Error ctu num when stream error happen. 6'd42: Inter reflist idx which be used flag. 6'd43: Pu num, 4*4 unit. 6'd44: mv_y_min[15:0], mv_x_min[15:0]. 6'd45: mv_y_max[15:0], mv_x_max[15:0]. 6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'd48: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'd49: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]. 6'd51: The cu skip num, unit is 8*8. 6'd52: The tu skip num, unit is 4*4. 6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]. 6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]. 6'd55: The sum of luma qp, unit is 4*4. 6'd56: The sum of cb qp, unit is 4*4. 6'd57: The sum of cr qp, unit is 4*4.

			6'd58: The count of mv_x. 6'd59: The count of mv_y.

Rkvdec_Swreg266_debug_perf_cnt0
Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_cnt0 Performance count value0

Rkvdec_Swreg267_debug_perf_cnt1
Address: Operational Base + offset (0x042c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_cnt1 Performance count value1.

Rkvdec_Swreg268_debug_perf_cnt2
Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Sw_perf_cnt2 Performance count value2.

Rkvdec_Swreg269_vp9_error_info
Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vp9_error_ctu1_en If the error ctu offset be valid.
30:26	RO	0x0	reserved
25:16	RW	0x000	Sw_vp9_error_ctu1_y The error ctu offset y
15:10	RO	0x0	reserved
9:0	RW	0x000	Sw_vp9_error_ctu1_x The error ctu offset x

Rkvdec_Swreg270_debug_qos_ctrl

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	sw_axi_rd_qos Field0000 Description
27:26	RO	0x0	reserved
25:24	RW	0x0	Sw_axi_rd_hurry_level 2'b00: Hurry off. 2'b01~2'b11: Hurry level.
23:22	RO	0x0	reserved
21:20	RW	0x0	sw_axi_wr_qos Field0000 Description
19:18	RO	0x0	reserved
17:16	RW	0x0	Sw_axi_wr_hurry_level 2'b00: Hurry off. 2'b01~2'b11: Hurry level.
15:8	RO	0x0	reserved
7:0	RW	0x00	Sw_bus2mc_buf_qos_level Range is: 0~255. The value is means that sw_bus2mc_buffer_qos_level <= left space, it will give hurry.

Rkvdec_Swreg271_debug_wait_cycle_qos

Address: Operational Base + offset (0x043c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_wr_hurry_wait_cycle Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr,it will give hurry.

Rkvdec_Swreg272_debug_int

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RO	0x00	Sw_streamfifo_space2full It is for debug use, to tell the stream fifo space to full. For HEVC , H264 and VP9.
15:12	RO	0x0	reserved
11:6	RO	0x00	Sw_wr_tansfer_cnt Field0002 Description
5	RO	0x0	Sw_stream_rdburst_cnteq0_towr Field0001 Description
4	RO	0x0	Sw_cabu_rlcend_valid_real Field0000 Description
3	RO	0x0	Sw_colmvwr_frame_rdy_real Field0000 Description
2	RO	0x0	Sw_saobu_frame_rdy_valid Field0000 Description
1	RO	0x0	Sw_saowr_frame_rdy Field0000 Description
0	RO	0x0	Sw_bu_rw_clean 1'b0: Bus busy. 1'b1: Bus idle.

Rkvdec_Swreg273_sta_b_frame_flag

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31	RO	0x0	Sw_pps_no_ref_bframe_dec_r 1'b1: Find this frame is not referace B frame.
30:19	RO	0x0	reserved
18:0	RO	0x00000	Sw_bus_status_flag Field0000 Description

Rkvdec_Swreg274_pix_range_y

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x000	Sw_y_max_value The max value of luma
15:10	RO	0x0	reserved
9:0	RW	0x000	Sw_y_min_value The min value of luma

Rkvdec_Swreg275_pix_range_u

Address: Operational Base + offset (0x044c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x000	Sw_u_max_value The max value of chroma u
15:10	RO	0x0	reserved
9:0	RO	0x000	Sw_u_min_value The min value of chroma u

Rkvdec_Swreg276_pix_range_v

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	Sw_v_max_value The max value of chroma v
15:10	RO	0x0	reserved
9:0	RO	0x000	Sw_v_min_value The min value of chroma v

10.5.8 VDPU346 CACHE Registers Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x07100206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	Clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	Maximum read register
pref_cache_ENABLE	0x001c	W	0x00000003	Enables cacheable accesses and cache read allocation
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	Performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	Performance counter 0 value register

Name	Offset	Size	Reset Value	Description
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: Bad hit number, slave
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	Performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.9 VDPU346 CACHE Detail Registers Description

pref_cache_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Minor verision
15:8	RO	0x01	VERSION_MAJOR Major verision
7:0	RO	0x01	VERSION_MINOR The id of product

pref_cache_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Log2 external bus width in bits
23:16	RO	0x10	CACHE_SIZE Log2 cache size in bytes For Y channel, its value is 0x10 For UV channel, its value is 0xf
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

pref_cache_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	DATA_BUSY Set when the cache is busy handling data.
0	RW	0x0	CMD_BUSY Set when the cache is busy handling commands.

pref_cache_COMMAND

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	Reserved
5:4	RW	0x0	Sw_addrb_sel 2'b00: To sel b[14:6] 2'b01: To sel b[15:9], b[7:6] 2'b10: To sel b[16:10], b[7:6] 2'b11: To sel b[17:11], b[7:6]
3:0	RW	0x0	COMMAND 1'b1: Clear entire cache

pref_cache_CLEAR_PAGE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE Writing an address, invilidates all lines in that page from the cache.

pref_cache_MAX_READS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	Reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount.

pref_cache_ENABLE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	Reserved
4	RW	0x0	Sw_cache_linsize 1'b0: The cache line is 32bytes 1'b1: The cache line is 64bytes
3	RW	0x0	Sw_cache_clk_disgate Cache clk disgate When it is 1'b0, enable cache clk auto clkgating When it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	Sw_readbuffer_counter_reject_en Default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: Normal origin counter reject
1	RW	0x1	Permit_cache_read_allocate 1'b1: Permit cache read allocate
0	RW	0x1	Permit_cacheable_access 1'b1: Permit cacheable access

pref_cache_PERFCNT_SRC0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	Reserved
6:0	RW	0x00	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: Disabled 1: Total clock cycles 2: Active clock cycles 3: Read transactions, master 4: Word reads, master 5: Read transactions, slave 6: Word reads, slave 7: Read hit, slave 8: Read misses, slave 9: Read invalidates, slave 10: Cacheable read transactions, slave 11: Bad hit number, slave

pref_cache_PERFCNT_VAL0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

pref_cache_PERFCNT_SRC1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	Reserved
6:0	RW	0x00	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: Disabled 1: Total clock cycles 2: Active clock cycles 3: Read transactions, master 4: Word reads, master 5: Read transactions, slave 6: Word reads, slave 7: Read hit, slave 8: Read misses, slave 9: Read invalidates, slave 10: Cacheable read transactions, slave 11: Bad hit nmber, slave

pref_cache_PERFCNT_VAL1

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

10.5.10 VDPU346 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
rkvdec_mmu_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state
rkvdec_mmu_STATUS	0x0004	W	0x00000018	MMU status register

Name	Offset	Size	Reset Value	Description
rkvdec_mmu_COMMAND	0x0008	W	0x00000000	MMU command register
rkvdec_mmu_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
rkvdec_mmu_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
rkvdec_mmu_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_AUTO_GATING	0x0024	W	0x00000001	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.11 VDPU346 MMU Detail Registers Description

rkvdec_mmu_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR Mmu dte base addr , the address must be 4kb aligned

rkvdec_mmu_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault.

Bit	Attr	Reset Value	Description
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty.
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled.

rkvdec_mmu_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

rkvdec_mmu_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

rkvdec_mmu_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache

rkvdec_mmu_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

rkvdec_mmu_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	WO	0x0	READ_BUS_ERROR Read bus error
0	WO	0x0	PAGE_FAULT Page fault

rkvdec_mmu_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error Enable an interrupt source if the corresponding mask bit is set to 1.
0	RW	0x0	PAGE_FAULT Page fault Enable an interrupt source if the corresponding mask bit is set to 1.

rkvdec_mmu_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RO	0x0	PAGE_FAULT Page fault

rkvdec_mmu_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x1	Mmu_auto_gating When it is 1'b1, the mmu will auto gating itself.

10.5.12 VDPU346 LLP Registers Summary

Name	Offset	Size	Reset Value	Description
rkvdec_link_swreg0_link_mode_irq	0x0000	W	0x00000000	The interript of LLP mode
rkvdec_link_swreg1_cfg_start_addr	0x0004	W	0x00000000	the address of register data
rkvdec_link_swreg2_link_mode	0x0008	W	0x00000000	The LLP table add ctrl
rkvdec_link_swreg3_config_done	0x000c	W	0x00000000	Config finish ctrl register
rkvdec_link_swreg4_decodered_num	0x0010	W	0x00000000	The frame number which have been decodered
rkvdec_link_swreg5_dec_total_num	0x0014	W	0x00000000	The total needed decoder number
rkvdec_link_swreg6_link_mode_en	0x0018	W	0x00000000	LLP enable flag

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.13 VDPU346 LLP Detail Registers Description

rkvdec_link_swreg0_link_mode_irq

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	Reserved
9	RW	0x0	rkvdec_irq_raw The irq of decodered
8	RW	0x0	Link_table_irq When high, decoder requests an interrupt. link table irq = Sw_dec_irq_raw && (Sw_dec_irq_dis == 1'b0)
7:3	RO	0x00	Reserved
2	RW	0x0	Sw_error_irq_dis 1'b0: If there are any error ,not matter Sw_dec_irq_dis ,it will give an interrupt. 1'b1: If it will give interrept ,it only according to Sw_dec_irq_dis
1	RW	0x0	Cache_cfg_mode_sel 1'b0: Use rtl default value to config cache, ip will auto clr cache when it begin to start dec a frame. 1'b1: Use config in ddr to config cache .

rkvdec_link_swreg1_cfg_start_addr

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reg_cfg_addr It should be align to 32 byte.

rkvdec_link_swreg2_link_mode

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	Link_mode 1'b0: Normal mode,the first to start link mode 1'b1: Add extra ready frame to decoder
30	RO	0x0	Reserved
29:0	RW	0x00000000	Pre_frame_num 1'b1: Config 1 frame

rkvdec_link_swreg3_config_done

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved

Bit	Attr	Reset Value	Description
0	WO	0x0	Config_done After config okay, config this bit to 1

rkvdec_link_swreg4_decodered_num

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	Decoder_error_flag 1'b0: No error 1'b1: Error, you will need to see swreg1 to check error type.
30	RO	0x0	Reserved
29:0	RO	0x00000000	Decoder_num The frame number which have been decodered

rkvdec_link_swreg5_dec_total_num

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:0	RO	0x00000000	Dec_total_num The total needed decoder number

rkvdec_link_swreg6_link_mode_en

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x0	Link_mode_en When error see by hw, it will auto reset to 0.

10.5.14 VDPU720 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDJPEG_swreg0_id	0x0000	W	0x00000000	ID register (read only)
RKDJPEG_swreg1_int	0x0004	W	0x00000000	interrupt and decoder enable register
RKDJPEG_swreg2_sys	0x0008	W	0x00000000	rk jpeg decoder system ctrl
RKDJPEG_swreg3_pic_size	0x000c	W	0x00000000	picture width and height size
RKDJPEG_swreg4_pic_format	0x0010	W	0x00000000	jpeg picture format configurate
RKDJPEG_swreg5_hor_virstride	0x0014	W	0x00000000	sw_y_hor_virstride and sw_uv_hor_virstride configurate
RKDJPEG_swreg6_y_virstride	0x0018	W	0x00000000	sw_y_virstride configurate
RKDJPEG_swreg7_table_len	0x001c	W	0x00000000	dequant table and huffman table length Description
RKDJPEG_swreg8_strm_len	0x0020	W	0x00000000	rk jpeg stream length and start byte info Description
RKDJPEG_swreg9_qtbl_base	0x0024	W	0x00000000	dequant table DDR base address Description
RKDJPEG_swreg10_htbl_mincode_base	0x0028	W	0x00000000	huffman mincode table DDR base address Description
RKDJPEG_swreg11_htbl_value_base	0x002c	W	0x00000000	huffman value table DDR base address Description
RKDJPEG_swreg12_strm_base	0x0030	W	0x00000000	stream data DDR base address Description
RKDJPEG_swreg13_dec_out_base	0x0034	W	0x00000000	rk jpeg recon decoder output data DDR address Description
RKDJPEG_swreg14_strm_error	0x0038	W	0x00000000	rk jpeg decoder stream error process
RKDJPEG_swreg15_strm_mask	0x003c	W	0x00000000	rk jpeg decoder special marker process

RKDJPEG_swreg16_clk_gate	0x0040	W	0x00000000	rk jpeg decoder clk gate enable
RKDJPEG_swreg30_perf_latency_ctrl0	0x0078	W	0x00000000	rk jpeg decoder axi performance ctrl0 Description
RKDJPEG_swreg31_perf_latency_ctrl1	0x007c	W	0x00000000	rk jpeg decoder axi performance ctrl1 Description
RKDJPEG_swreg32_dbg_mcu_pos	0x0080	W	0x00000000	rk jpeg debug register with mcu position Description
RKDJPEG_swreg33_dbg_error_info	0x0084	W	0x00000000	rk jpeg debug register with error info Description
RKDJPEG_swreg34_perf_rd_max_latency_num0	0x0088	W	0x00000000	rd_max_latency_num Description
RKDJPEG_swreg35_perf_rd_latency_samp_num	0x008c	W	0x00000000	rd_latency_thr_num Description
RKDJPEG_swreg36_perf_rd_latency_acc_sum	0x0090	W	0x00000000	rd_latency_acc_sum Description
RKDJPEG_swreg37_perf_rd_axi_total_byte	0x0094	W	0x00000000	perf_rd_axi_total_byte Description
RKDJPEG_swreg38_perf_wr_axi_total_byte	0x0098	W	0x00000000	perf_wr_axi_total_byte Description
RKDJPEG_swreg39_perf_working_cnt	0x009c	W	0x00000000	perf_working_cnt Description

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.15 VDPU720 Detail Registers Description

RKDJPEG_swreg0_id

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	prod_num RKDJPEG verision
15:9	RO	0x0	reserved
8	RO	0x0	bit_depth max bit_depth support 0: 8bits 1: 12bits
7:0	RO	0x00	minor_ver 0: default 1: 8k

RKDJPEG_swreg1_int
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	sw_care_strm_error_e use for sw_error_prc_mode=1 0:not care stream error,when sw_care_strm_error_e=0, sw_dec_error_sta will not valid, mmu will not be reset at frame end, link table mode will continue without care stream error, only active error info registers; 1:care stream error;
15	RW	0x0	sw_buf_empty_force_end_flag 0:invalid 1:valid buffer empty interrupt with stream real empty so should force hardware decoder current frame end
14	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done
13	RW	0x0	sw_dec_buf_empty_sta buffer empty status, only when sw_buf_empty_e is 1'b1 , this bit is valid software should clean stream buffer empty state and set sw_buf_empty_reload_p enbale at the same time
12	RW	0x0	sw_dec_timeout_sta When high the decoder has been idling for too long. it will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid
11	RW	0x0	sw_dec_error_sta when high, an error is found in input data stream decoding.when sw_error_prc_mode is 1'b0, it will self reset the hardware, otherwise it will not

10	RW	0x0	sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware
9	RW	0x0	sw_dec_rdy_sta when this bit is high, decoder has decoded a picture (the output module send out a frame rdy)
8	RW	0x0	sw_dec_irq when high, decoder requests an interrrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7	RW	0x0	sw_wait_reset_e the enable flag of wait software system to reset flag 0: hardware will auto reset when error occur 1: wait software process reset when error occur
6	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq,SW should reset this bit after interrupt is handled
5	RW	0x0	sw_softrst_en_p softreset enable signal write 1 to soft reset, write 0 invalid puls register

4	RW	0x0	sw_buf_empty_reload_p buffer empty stream reload enable signal write 1 to reload stream data ready pulse register with hardware auto clean valid at next cycle before reload enable,strm_len register should be reset and start_of_type is zero sw_strm_base addr may be reset also. note:sw_error_prc_mode should be set to 1 when sw_buf_empty_e valid otherwise the hardware would be reset and not support buffer buffer empty reload
3	RW	0x0	sw_buf_empty_e buffer empty interrupt enable
2	RW	0x0	sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
1	RW	0x0	sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
0	RW	0x0	sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format.

RKDJPEG_swreg2_sys
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_yuv2rgb_range jpeg decoder yuv2rgb range 0: range0 limit (Y[16:235],UV[16:240],RGB[0:255]) 1: range1 full (YUV[0:255],RGB[0:255])
30	RW	0x0	sw_yuv2rgb_rec jpeg decoder yuv2rgb rec 0: BT601 1: BT709
29:27	RW	0x0	sw_yuv_out_format jpeg decoder yuv output transmit format 000:yuv out without transmit format 001:yuv2rgb888 010:yuv2rgb565 011:yuv2yuv420sp(not support yuv400 transmit to yuv420sp) 100:yuv2yuyv(only support yuv422 or yuv444, yuv444 should uv scaledown)
26	RW	0x0	sw_dec_out_sequence recon data out format when afbc off 0:raster sequence out 1:tile sequence out
25	RW	0x0	sw_fill_right_e When JPEG picture width pixels is not a multiple of 16 pixels. 0: not fill picture width to multiple of 16 pixels. 1: fill picture width to multiple of 16 pixels. HW must fill one block of zero pixel data to the right border of the picture.

24	RW	0x0	sw_fill_down_e When JPEG picture height pixels is not a multiple of 16 pixels. 0: not fill picture height to multiple of 16 pixels. 1: fill picture height to multiple of 16 pixels. HW must fill one block row of zero pixel data for the last block row of picture.
23	RO	0x0	reserved
22	RW	0x0	sw_fbc_force_uncompress 0：allow fbce compress yuv block； 1：force all yuv block use uncompress mode；
21	RW	0x0	sw_allow_16x8_cp_flag 0: not allow 1:allow the configurate value is depend on vop work mode
20	RW	0x0	sw_fbc_e 0:disable 1:fbc enable
19:18	RO	0x0	reserved
17	RW	0x0	sw_force_softreset_valid when sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.
16	RW	0x0	sw_timeout_mode timeout mode select 1'b0: TIMEOUT_CYCLES is 24 1'b1; 1'b1: TIMEOUT_CYCLES is 18 1'b1;
15:14	RO	0x0	reserved

13:12	RW	0x0	sw_scaledown_mode jpeg decoder scaledown mode 00: not scaledown 01: 1/2 scaledown 10: 1/4 scaledown 11: 1/8 scaledown
11:10	RO	0x0	reserved
9	RW	0x0	sw_out_cbcr_swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbcr_swap is the same with sw_out_cbcr_swap jpeg decoder only support for yuv4xxsp
8	RW	0x0	sw_out_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
7	RW	0x0	sw_out_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped

4	RW	0x0	sw_str_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
3	RW	0x0	sw_str_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
0	RW	0x0	sw_in_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

RKDJPEG_swreg3_pic_size
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_pic_height_m1 Picture height in pixels unit minus1(should be mcu align by hardware)
15:0	RW	0x0000	sw_pic_width_m1 Picture width in pixels unit minus1(should be mcu align by hardware)

RKDJPEG_swreg4_pic_format
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dri_mcu_num_m1 Restart marker frequency. Tells the amount of coding units between restart markers Specifies the number of MCU in the restart. the number is minus1
15	RW	0x0	sw_dri_e define restart interval marker enable 0:restart interval marker disable 1:restart interval marker enable
14	RO	0x0	reserved
13:12	RW	0x0	sw_htables_sel Amount of Huffman tables in external memory: 0 = No Huffman tables. 1 = One Huffman table. Used when picture is single type 2 = Two Huffman tables. One for luminance and one for chominances 3 = Three Huffman tables. Each type (Lu, Cb, Cr) has own Huffman table
11:10	RO	0x0	reserved
9:8	RW	0x0	sw_qtables_sel Amount of Quantization tables in external memory: 0 = No quantization tables. 1 = One quantization table. Used when picture is single type 2 = Two quantization tables. One for luminance and one for chominances 3 = Three quantization tables. Each type (Lu, Cr, Cb) has own QP-table
7	RO	0x0	reserved

6:4	RW	0x0	sw_pixel_depth Picture luma pixel depth minus8. 0:8bits 4:12bits
3	RO	0x0	reserved
2:0	RW	0x0	sw_jpeg_mode Input picture sampling format: 0 = single type, MB 1 block (4:0:0) 1 = single type, MB 6 blocks (4:1:1) 2 = three types, MB 6 blocks (4:2:0) 3 = three types, MB 4 blocks (4:2:2) 4 = three types, MB 4 blocks (4:4:0) 5 = three types, MB 3 blocks (4:4:4)

RKDJPEG_swreg5_hor_virstride

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is 65536x2/16 = 0x2000 suggest this register to configuration to even for advance DDR performance yuv444 tile mode ,uv_hor_virstride will use 16bits
15:0	RW	0x0000	sw_y_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is 65536x2/16 = 0x2000 suggest this register to configuration to even for advance DDR performance fbc mode: used for head virtual stride but rgb888 tile mode ,y_hor_virstride 16bits is not enought,will be use 17bits

RKDJPEG_swreg6_y_virstride

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_y_virstride Base address with 16 byte precision for decoder output luminance picture virtual stride
3:0	RO	0x0	reserved

RKDJPEG_swreg7_table_len

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sw_y_hor_virstride_h picture horizontal virtual stride (the unit is 128bit) high bit when rgb888 tile mode use ,y_hor_virstride 16bits is not enought,will be use 17bits
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_htbl_value_len Huffman value tables length(minus 1) with 16 byte align(128bits)
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_htbl_mincode_len Huffman maxcode mincode and accaddr length(minus 1) with 16 byte align(128bits)
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_qtbl_len quant table length(minus 1) with 16 byte align(128bits)

RKDJPEG_swreg8_strm_len

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_stream_len Amount of stream data 16 bytes(minus 1) in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (assosiates with sw_strm_in_base).
3:0	RW	0x0	sw_strm_start_byte Input stream start byte offset: 0 = 0 type, of the base addr(16bytes) offset 1 = 1 type, of the base addr(16bytes) offset 2 = 2 type, of the base addr(16bytes) offset 3 = 3 type, of the base addr(16bytes) offset 4 = 4 type, of the base addr(16bytes) offset 5 = 5 type, of the base addr(16bytes) offset 6 = 6 type, of the base addr(16bytes) offset 7 = 7 type, of the base addr(16bytes) offset …

RKDJPEG_swreg9_qtbl_base

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_qtbl_base Base address for standard dependent tables: AC,DC, QP tables 64 bytes align）
5:0	RO	0x0	reserved

RKDJPEG_swreg10_htbl_mincode_base

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_mincode_base Base address for standard dependent tables: Huffman mincode and accaddr tables 64 bytes align）
5:0	RO	0x0	reserved

RKDJPEG_swreg11_htbl_value_base
Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_value_base Base address for standard dependent tables: Huffman value tables 64 bytes align）
5:0	RO	0x0	reserved

RKDJPEG_swreg12_strm_base
Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_in_base Stream start address with 16 byte precision. Actually, start byte number in stream_start_byte.
3:0	RO	0x0	reserved

RKDJPEG_swreg13_dec_out_base
Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_dec_out_base Base address with 64 byte precision for decoder output luminance picture
5:0	RO	0x0	reserved

RKDJPEG_swreg14_strm_error
Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	sw_hfm_force_stop 0: Huffman decoder error and continue. 1: Huffman decoder error force stop the decoder and wait soft reset. [12]: AXI stream buffer empty, and without detect EOI marker stop or not(0:support fill coefficient) [11]:Huffman get EOI marker without frame end stop or not(0:support fill coefficient) [10]:Huffman coefficient overflow detect and stop or not(0:support decode next coefficient) [9]:Huffman decode DRI stream stop or not, when MCU counter is not zero with DRI marker detect(0:support fill coefficient) [8]:Huffman decode DRI stream stop or not, when MCU counter is zero without DRI marker detect(0:support skip dummy stream)
15:10	RO	0x0	reserved
9	RW	0x0	sw_strm_dri_seq_err_mode 0:stream dri sequence error do not report error pos; 1:stream dri sequence error should be report error pos(if it's first error); note: error state should be report at all case
8:7	RW	0x0	sw_strm_other_mark_mode 00:stream detect other marker do skip process and not report error pos; 01: stream detect another marker stop the decoder and wait soft reset; 10:stream detect other marker do skip process 11:stream detect other marker do with normal stream note: error state should be report at all case

6:5	RW	0x0	sw_strm_ffff_err_mode 00:stream detect ffff marker do skip first 0xff process and not report error pos; 01: stream detect another marker stop the decoder and wait soft reset; 10:stream detect ffff marker do skip first 0xff process; 11:stream detect ffff marker do with normal stream at first 0xff; note: error state should be report at all case
4:3	RW	0x0	sw_strm_r1_err_mode stream detect second select marker process mode configuration 00: ignore second select marker. 01: force stop decoder when meet the second select marker 10: do skip process when meet the second select marker 11: do with normal stream when meet the second select marker
2:1	RW	0x0	sw_strm_r0_err_mode stream detect first select marker process mode configuration 00: ignore first select marker. 01: force stop decoder when meet the first select marker 10: do skip process when meet the first select marker 11: do with normal stream when meet the first select marker
0	RW	0x0	sw_error_prc_mode 1'b0: when there is any stream error, the hardware will stop the decoder and reset itself; 1'b1: when there is any stream error, the hardware will wait the end signal of recon and then reset request;

RKDJPEG_swreg15_strm_mask
Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_strm_r1_mask mark the mask info 1:stream value[7-0] will mask and not care 0:stream value[7-0] shall match SW marker value
23:16	RW	0x00	sw_strm_r1_marker 0xffxx marker low 8bits value
15:8	RW	0x00	sw_strm_r0_mask mark the mask info 1:stream value[7-0] will mask and not care 0:stream value[7-0] shall match SW marker value
7:0	RW	0x00	sw_strm_r0_marker 0xffxx marker low 8bits value

RKDJPEG_swreg16_clk_gate
Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x0	sw_dec_gate_e total 8 bits each with follow phase 0 = Clock gate is not enable 1 = Clock gate is enable when busifd block is not working

RKDJPEG_swreg30_perf_latency_ctrl0
Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr rd channel latency threshold
7:4	RW	0x0	sw_rd_latency_id rd channel id for performance test
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type 0:axi transfer num count 1:ddr align transfer num count
2	RW	0x0	sw_axi_perf_frm_type 1'b0: clear by frame end 1'b1: clear by software configuration
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

RKDJPEG_swreg31_perf_latency_ctrl1
Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	sw_rd_total_bytes_mode 0:cal all id 1:cal sw_ar_count_id
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type 0:count all wr-channels 1:count sw_wr_cont_id wr-channel only
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type 0:count all rd-channels 1:count sw_ar_cont_id rd-channel only
1:0	RW	0x0	sw_addr_align_type sw_addr_align_type 0:16 byte align 1:32byte align 2:64byte align 3:128byte align

RKDJPEG_swreg32_dbg_mcu_pos
Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	mcu_pos_y Decoder mcu position at x coordinal with first error detect, only for read enable
15:0	RO	0x0000	mcu_pos_x Decoder mcu position at y coordinal with first error detect, only for read enable

RKDJPEG_swreg33_dbg_error_info
Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	jpeg_first_error_idx jpeg decoder first error index 4'd0:stream_dri_seq_err_sta 4'd1:stream_r0_err_sta 4'd2:stream_r1_err_sta 4'd3:stream_ffff_err_sta 4'd4:stream_other_mark_err_sta 4'd8:huffman_mcu_cnt_l 4'd9:huffman_mcu_cnt_m 4'd10:huffman_eoi_without_end 4'd11:huffman_end_without_eoi 4'd12:huffman_overflow 4'd13:huffman_buf_empty
15:14	RO	0x0	reserved
13	RW	0x0	huffman_buf_empty Decoder picture not complete, and not detect EOI with buffer empty 0:buffer not empty 1:buffer empty
12	RW	0x0	huffman_overflow Decoder Huffman coefficient overflow
11	RW	0x0	huffman_end_without_eoi Decoder Huffman frame end without get EOI marker
10	RW	0x0	huffman_eoi_without_end Decoder Huffman get EOI marker without frame end

9	RW	0x0	huffman_mcu_cnt_m Decoder dri stream mcu count more, mcu count 0 without restart mark
8	RW	0x0	huffman_mcu_cnt_l Decoder dri stream mcu count low, restart mark is coming without mcu count 0
7:5	RO	0x0	reserved
4	RW	0x0	stream_other_mark_err_sta Decoder stream other marker error detect flag, only for read enable 0:other marker not detect 1:other marker detect
3	RW	0x0	stream_ffff_err_sta Decoder stream ffff error detect flag, only for read enable 0:other marker not detect 1:other marker detect
2	RW	0x0	stream_r1_err_sta Decoder stream special marker1 error detect flag, only for read enable 0:special marker1 not detect 1:special marker1 detect
1	RW	0x0	stream_r0_err_sta Decoder stream special marker0 error detect flag, only for read enable 0:special marker0 not detect 1:special marker0 detect
0	RW	0x0	stream_dri_seq_err_sta 0:stream DRI at normal sequence 1:stream error with DRI not at normal sequence

RKDJPEG_swreg34_perf_rd_max_latency_num0

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	rd_max_latency_num_ch0 rd_max_latency_num_ch0

RKDJPEG_swreg35_perf_rd_latency_samp_num

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_thr_num_ch0 rd_latency_thr_num_ch0

RKDJPEG_swreg36_perf_rd_latency_acc_sum

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_sum rd_latency_acc_sum

RKDJPEG_swreg37_perf_rd_axi_total_byte

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

RKDJPEG_swreg38_perf_wr_axi_total_byte

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

RKDJPEG_swreg39_perf_working_cnt

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

10.5.16 VDPU720 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
rkvdec_mmu_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state
rkvdec_mmu_STATUS	0x0004	W	0x00000018	MMU status register
rkvdec_mmu_COMMAND	0x0008	W	0x00000000	MMU command register
rkvdec_mmu_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
rkvdec_mmu_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
rkvdec_mmu_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.17 VDPU720 MMU Registers Description

rkvdec_mmu_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr , the address must be 4kb aligned

rkvdec_mmu_STATUS
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

rkvdec_mmu_COMMAND
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

rkvdec_mmu_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

rkvdec_mmu_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

rkvdec_mmu_INT_RAWSTAT
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

rkvdec_mmu_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

rkvdec_mmu_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT page fault enable an interrupt source if the corresponding mask bit is set to 1

rkvdec_mmu_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

rkvdec_mmu_AUTO_GATING
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

10.5.18 VDPU720 LLP Registers Summary

Name	Offset	Size	Reset Value	Description
rkdjpeg_link_swreg0_link_mode_irq	0x0000	W	0x00000000	Register0000 Description
rkdjpeg_link_swreg1_cfg_start_addr	0x0004	W	0x00000000	the address of register data
rkdjpeg_link_swreg2_link_mode	0x0008	W	0x00000000	Register0000 Description
rkdjpeg_link_swreg3_config_done	0x000c	W	0x00000000	Register0000 Description
rkdjpeg_link_swreg4_decodered_num	0x0010	W	0x00000000	Register0000 Description
rkdjpeg_link_swreg5_dec_total_num	0x0014	W	0x00000000	Register0000 Description
rkdjpeg_link_swreg6_link_mode_en	0x0018	W	0x00000000	Register0000 Description

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.19 VDPU720 LLP Registers Description

rkdjpeg_link_swreg0_link_mode_irq
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_link_softreset_rdy when it is 1'b1, it says that softreset has been done
9	RW	0x0	rkvdec_irq_raw Field0000 Description
8	RW	0x0	link_table_irq when high, decoder requests an interrrupt. link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7:3	RO	0x0	reserved
2	RW	0x0	sw_error_irq_dis 0: if there are any error ,not matter sw_dec_irq_dis ,it will give an interrept . 1:if it will give interrept ,it only according to sw_dec_irq_dis
1	RW	0x0	cache_cfg_mode_sel 0:use rtl default value to config cache, ip will auto clr cache when it begin to start dec a frame. 1:use config in ddr to config cache .
0	RO	0x0	reserved

rkdjpeg_link_swreg1_cfg_start_addr
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	reg_cfg_addr it should be align to 32 byte
3:0	RO	0x0	reserved

rkdjpeg_link_swreg2_link_mode
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	link_mode 0: normal mode,the first to start link mode 1:add extra ready frame to decoder
30	RO	0x0	reserved
29:0	RW	0x00000000	pre_frame_num 1:config 1 frame

rkdjpeg_link_swreg3_config_done

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	config_done after config okay,config this bit to 1

rkdjpeg_link_swreg4_decodered_num

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	decoder_error_flag 0:no error 1:error,you will need to see swreg1 to check error type
30	RO	0x0	reserved
29:0	RO	0x00000000	decoder_num Field0000 Description

rkdjpeg_link_swreg5_dec_total_num

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	dec_total_num Field0000 Description

rkdjpeg_link_swreg6_link_mode_en

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	sw_link_softrst_en_p link mode software force hardware self reset enable signal write 1 to soft reset, write 0 invalid puls register
3:1	RO	0x0	reserved
0	RW	0x0	link_mode_en when error see by hw,it will auto reset to 0

10.5.20 VEPU121 Registers Summary

Name	Offset	Size	Reset Value	Description
VEPU_swreg_0	0x0000	W	0x00000000	1st quantization for jpeg lumin table
VEPU_swreg_1	0x0004	W	0x00000000	2st quantization for jpeg lumin table
VEPU_swreg_2	0x0008	W	0x00000000	3st quantization for jpeg lumin table
VEPU_swreg_3	0x000c	W	0x00000000	4st quantization for jpeg lumin table
VEPU_swreg_4	0x0010	W	0x00000000	5st quantization for jpeg lumin table
VEPU_swreg_5	0x0014	W	0x00000000	6st quantization for jpeg lumin table/part 1 for qp round
VEPU_swreg_6	0x0018	W	0x00000000	7st quantization for jpeg lumin table
VEPU_swreg_7	0x001c	W	0x00000000	8st quantization for jpeg lumin table
VEPU_swreg_8	0x0020	W	0x00000000	9st quantization for jpeg lumin table

Name	Offset	Size	Reset Value	Description
VEPU_swreg_9	0x0024	W	0x00000000	10st quantization for jpeg lumin table
VEPU_swreg_10	0x0028	W	0x00000000	11st quantization for jpeg lumin table
VEPU_swreg_11	0x002c	W	0x00000000	12st quantization for jpeg lumin table
VEPU_swreg_12	0x0030	W	0x00000000	13st quantization for jpeg lumin table
VEPU_swreg_13	0x0034	W	0x00000000	14st quantization for jpeg lumin table
VEPU_swreg_14	0x0038	W	0x00000000	15st quantization for jpeg lumin table
VEPU_swreg_15	0x003c	W	0x00000000	16st quantization for jpeg lumin table
VEPU_swreg_16	0x0040	W	0x00000000	1st quantization for jpeg chroma table
VEPU_swreg_17	0x0044	W	0x00000000	2st quantization for jpeg chroma table
VEPU_swreg_18	0x0048	W	0x00000000	3st quantization for jpeg chroma table
VEPU_swreg_19	0x004c	W	0x00000000	4st quantization for jpeg chroma table
VEPU_swreg_20	0x0050	W	0x00000000	5st quantization for jpeg chroma table
VEPU_swreg_21	0x0054	W	0x00000000	6st quantization for jpeg chroma table
VEPU_swreg_22	0x0058	W	0x00000000	7st quantization for jpeg chroma table
VEPU_swreg_23	0x005c	W	0x00000000	8st quantization for jpeg chroma table/part 3 for qp round
VEPU_swreg_24	0x0060	W	0x00000000	9st quantization for jpeg chroma table

Name	Offset	Size	Reset Value	Description
VEPU_swreg_25	0x0064	W	0x00000000	10st quantization for jpeg chroma table
VEPU_swreg_26	0x0068	W	0x00000000	11st quantization for jpeg chroma table
VEPU_swreg_27	0x006c	W	0x00000000	12st quantization for jpeg chroma
VEPU_swreg_28	0x0070	W	0x00000000	13st quantization for jpeg chroma
VEPU_swreg_29	0x0074	W	0x00000000	14st quantization for jpeg chroma
VEPU_swreg_30	0x0078	W	0x00000000	15st quantization for jpeg chroma
VEPU_swreg_31	0x007c	W	0x00000000	16st quantization for jpeg chroma
VEPU_swreg_44	0x00b0	W	0x00000000	Intra slice bitmap
VEPU_swreg_45	0x00b4	W	0x00000000	Intra slice bitmap1
VEPU_swreg_46	0x00b8	W	0x00000000	Intra macro block select register
VEPU_swreg_47	0x00bc	W	0x00000000	CIR intra control register
VEPU_swreg_48	0x00c0	W	0x00000000	Base addr for input luma
VEPU_swreg_49	0x00c4	W	0x00000000	Base address for input cb
VEPU_swreg_50	0x00c8	W	0x00000000	Input cr start address
VEPU_swreg_51	0x00cc	W	0x00000000	Stream header bits left register
VEPU_swreg_52	0x00d0	W	0x00000000	Stream header bits left register
VEPU_swreg_53	0x00d4	W	0x00000000	Stream buffer register
VEPU_swreg_54	0x00d8	W	0x01010000	Axi control register
VEPU_swreg_55	0x00dc	W	0x00000000	Qp related
VEPU_swreg_56	0x00e0	W	0x00000000	The luma reference frame start address
VEPU_swreg_57	0x00e4	W	0x00000000	The chroma reference frame start address
VEPU_swreg_58	0x00e8	W	0x00000000	The result of qp sum div2

Name	Offset	Size	Reset Value	Description
VEPU_swreg_59	0x00ec	W	0x00000000	H264 slice ctrl
VEPU_swreg_60	0x00f0	W	0x00000000	Spill ctrl
VEPU_swreg_61	0x00f4	W	0x00000000	Input luminance information
VEPU_swreg_62	0x00f8	W	0x00000000	Rlc_sum
VEPU_swreg_63	0x00fc	W	0x00000000	The reconstructed luma start address
VEPU_swreg_64	0x0100	W	0x00000000	The reconstructed chroma start address
VEPU_swreg_65_reuse	0x0104	W	0x00000000	Checkpoint 1 and 2
VEPU_swreg_66_reuse	0x0108	W	0x00000000	Checkpoint 3 and 4
VEPU_swreg_67_reuse	0x010c	W	0x00000000	Checkpoint 5 and 6
VEPU_swreg_68_reuse	0x0110	W	0x00000000	Checkpoint 7 and 8
VEPU_swreg_69_reuse	0x0114	W	0x00000000	Checkpoint 9 and 10
VEPU_swreg_70_reuse	0x0118	W	0x00000000	Checkpoint word error 1 and 2
VEPU_swreg_71_reuse	0x011c	W	0x00000000	Checkpoint word error 1 and 2
VEPU_swreg_72_reuse	0x0120	W	0x00000000	Checkpoint word error 1 and 2
VEPU_swreg_73_reuse	0x0124	W	0x00000000	Checkpoint delta QP register
VEPU_swreg_74	0x0128	W	0x00000000	Input image format
VEPU_swreg_75	0x012c	W	0x00000000	Intra/inter mode
VEPU_swreg_76_reuse	0x0130	W	0x00000000	Encoder control register 0
VEPU_swreg_77	0x0134	W	0x00000000	Output stream start address
VEPU_swreg_78	0x0138	W	0x00000000	Output control start address
VEPU_swreg_79	0x013c	W	0x00000000	Next picture luminance start address
VEPU_swreg_80	0x0140	W	0x00000000	Base address for MV output

Name	Offset	Size	Reset Value	Description
VEPU_swreg_81	0x0144	W	0x00000000	The cabac table start address
VEPU_swreg_82	0x0148	W	0x00000000	ROI area register
VEPU_swreg_83	0x014c	W	0x00000000	The second of ROI area register
VEPU_swreg_84	0x0150	W	0x00000000	Stabilization matrix1
VEPU_swreg_85	0x0154	W	0x00000000	Stabilization matrix2
VEPU_swreg_86	0x0158	W	0x00000000	Stabilization matrix3
VEPU_swreg_87	0x015c	W	0x00000000	Stabilization matrix4
VEPU_swreg_88	0x0160	W	0x00000000	Stabilization matrix5
VEPU_swreg_89	0x0164	W	0x00000000	Stabilization matrix6
VEPU_swreg_90	0x0168	W	0x00000000	Stabilization matrix7
VEPU_swreg_91	0x016c	W	0x00000000	Stabilization matrix8
VEPU_swreg_92	0x0170	W	0x00000000	Stabilization matrix9
VEPU_swreg_93	0x0174	W	0x00000000	The output of Stabilization motion sum
VEPU_swreg_94	0x0178	W	0x00000000	Output of Stabilization
VEPU_swreg_95	0x017c	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_96	0x0180	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_97	0x0184	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_98	0x0188	W	0x00000000	RGA MASK
VEPU_swreg_99	0x018c	W	0x00000000	Mv related
VEPU_swreg_100_reuse	0x0190	W	0x00000000	QP register
VEPU_swreg_101_read	0x0194	W	0x1f522780	Hw config reg
VEPU_swreg_102	0x0198	W	0x00000000	Mvc related

Name	Offset	Size	Reset Value	Description
VEPU_swreg_103	0x019c	W	0x00000000	Encoder start
VEPU_swreg_104	0x01a0	W	0x00000000	Mb control register
VEPU_swreg_105	0x01a4	W	0x00000000	Swap ctrl register
VEPU_swreg_106_reuse	0x01a8	W	0x00000000	Encoder control register 1
VEPU_swreg_107_reuse	0x01ac	W	0x00000000	JPEG control register
VEPU_swreg_108_reuse	0x01b0	W	0x00000000	Intra slice bmp2
VEPU_swreg_109	0x01b4	W	0x00001000	Encoder status
VEPU_swreg_110_read	0x01b8	W	0x48311220	Product ID
VEPU_swreg_120_183	0x01e0	W	0x00000000	Addr range: 0x01e0~0x02dc Swreg120: DMV 4p/1p penalty table values Swreg121: DMV 4p/1p penalty table values Swreg122: DMV 4p/1p penalty table values Swreg123: DMV 4p/1p penalty table values ..... Swreg183: DMV 4p/1p penalty table values

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.21 VEPU121 Detail Registers Description

VEPU_swreg_0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant1 Jpeg luma quantization 1

VEPU_swreg_1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant2 Jpeg luma quantization 2

VEPU_swreg_2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant3 Jpeg luma quantization 3

VEPU_swreg_3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant4 Jpeg luma quantization 4

VEPU_swreg_4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant5 Jpeg luma quantization 5

VEPU_swreg_5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant6 Jpeg luma quantization 6

VEPU_swreg_6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant7 Jpeg luma quantization 7

VEPU_swreg_7

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant8 Jpeg luma quantization 8

VEPU_swreg_8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant9 Jpeg luma quantization 9

VEPU_swreg_9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant10 Jpeg luma quantization 10

VEPU_swreg_10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant11 Jpeg luma quantization 11

VEPU_swreg_11

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant12 Jpeg luma quantization 12

VEPU_swreg_12

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant13 Jpeg luma quantization 13

VEPU_swreg_13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant14 Jpeg luma quantization 14

VEPU_swreg_14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_luma_quant15 Jpeg luma quantization 15

VEPU_swreg_15

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	Reserved
7:0	RW	0x00	Sw_jpeg_luma_quant16 Jpeg luma quantization 16

VEPU_swreg_16

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant1 Jpeg chroma quantization 1

VEPU_swreg_17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant2 Jpeg chroma quantization 2

VEPU_swreg_18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant3 Jpeg chroma quantization 3

VEPU_swreg_19

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant4 Jpeg chroma quantization 4

VEPU_swreg_20

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant5 Jpeg chroma quantization 5

VEPU_swreg_21

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant6 Jpeg chroma quantization 6

VEPU_swreg_22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant7 Jpeg chroma quantization 7

VEPU_swreg_23

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant8 Jpeg chroma quantization 8

VEPU_swreg_24

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant9 Jpeg chroma quantization 9

VEPU_swreg_25

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant10 Jpeg chroma quantization 10

VEPU_swreg_26

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	Reserved
8:0	RW	0x000	Sw_jpeg_chroma_quant11 Jpeg chroma quantization 11

VEPU_swreg_27

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant12 Jpeg chroma quantization 12

VEPU_swreg_28

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved
11:0	RW	0x000	Sw_jpeg_chroma_quant13 Jpeg chroma quantization 13

VEPU_swreg_29

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant14 Jpeg chroma quantization 14

VEPU_swreg_30

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	Reserved
11:0	RW	0x000	Sw_jpeg_chroma_quant15 Jpeg chroma quantization 15

VEPU_swreg_31

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Sw_jpeg_chroma_quant16 Jpeg chroma quantization 16

VEPU_swreg_44

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp0 Bit0 : Slices0 Bit1 : Slices1 Bit2 : Slices2 ..... Bit31 : Slices31

VEPU_swreg_45

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp1 Bit0 : Slices32 Bit1 : Slices33 Bit2 : Slices34 ..... Bit31 : Slices63

VEPU_swreg_46

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Intra_up_mb_area The top intra macro block's area used in row.
23:16	RW	0x00	Intra_down_mb_area The bottom intra macro block's area used in row.
15:8	RW	0x00	Intra_left_mb_area The left intra macro block's area used in column.
7:0	RW	0x00	Intra_right_mb_area The right intra macro block's area used in column.

VEPU_swreg_47

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Cir_first_intra 16'd0: Disable Other: Enable and be set
15:0	RW	0x0000	Cir_intra_mb_itvl 16'd0: Disable Other: Enable and be set

VEPU_swreg_48

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Luma_in_st_adr Input luma start address

VEPU_swreg_49

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cb_in_st_adr Input cb start address

VEPU_swreg_50

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cr_in_st_adr Input cr start address

VEPU_swreg_51

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_header_left_hbits The high 32 bit of stram header be left.

VEPU_swreg_52

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_header_left_lbits The low 32 bit of stram header be left.

VEPU_swreg_53

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Strm_bufsize_lmt The limit size of steam buffer.

VEPU_swreg_54

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	Axi_rd_id If config 0,it will be modify as 1 by HW auto
23:16	RW	0x01	Axi_wr_id If config 0,it will be modify as 1 by HW auto
15:14	RO	0x0	Reserved
13:8	RW	0x00	Burst_len Burst length
7:3	RO	0x00	Reserved
2	RW	0x0	Burst_incr_mod_sel 1'b0: Single burst selected 1'b1: Incr burst selected

Bit	Attr	Reset Value	Description
1	RW	0x0	Burst_discard 1'b0: Disable, off 1'b1: Enable, on
0	RW	0x0	Burst_disable 1'b0: Enable 1'b1: Disable

VEPU_swreg_55

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:12	RW	0x0	Roi_dlt_qp1 1st for delta qp for roi
11:8	RW	0x0	Roi_dlt_qp2 2st for delta qp for roi
7:4	RO	0x0	Reserved
3:0	RW	0x0	Qp_adjst Signed register; Range from -8 to 7

VEPU_swreg_56

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Luma_ref_st_adr The luma reference frame start address

VEPU_swreg_57

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Chroma_ref_st_adr The chroma reference frame start address

VEPU_swreg_58

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Qp_sum_div2 The result of (qp sum)/2

VEPU_swreg_59

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Reserved
28	RW	0x0	H264_qurt_pixmv_dis 1'b1: Disable 1'b0: Default, enable
27:26	RO	0x0	Reserved
25:24	RW	0x0	Dblking_flt_mode 2'd0: Enabled 2'd1: Disabled 2'd2: Disabled on slice
23	RO	0x0	Reserved
22:21	RW	0x0	H264_cabac_idc 2'd0,2'd1,2'd2: Used 2'd3: No use
20	RW	0x0	Entry_code_fmt H.264: 1'b0: Cavlc 1'b1: Cabac
19:18	RO	0x0	Reserved
17	RW	0x0	H264_trfmod_8x8 On-off for 8x8 transform used in h264
16	RW	0x0	H264_res_intermod_4x4 The restriction inter mode selected in 4x4 block
15	RW	0x0	H264_strm_mod_sel 1'b0: NAL unit 1'b1: BYTE
14:8	RW	0x00	H264_slice_num 0: One slice in currect picture 1: Two slice in currect picture .....

VEPU_swreg_60

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	Strm_st_offset
15:8	RW	0x00	Skip_mb_mode H264: SKIP macroblock mode
7:6	RO	0x0	Reserved
5:4	RW	0x0	Right_spill Div4 value Range: 0~3
3:0	RW	0x0	Bot_spill The bottom edge of image for spill pixels

VEPU_swreg_61

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	Reserved
22:20	RW	0x0	Offset_in_chroma Byte unit
19	RO	0x0	Reserved
18:16	RW	0x0	Offset_in_luma Byte unit
15:14	RO	0x0	Reserved
13:0	RW	0x0000	Row_len_in_luma

VEPU_swreg_62

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	Reserved
21:0	RW	0x000000	Rlc_sum Rlc_sum

VEPU_swreg_63

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Recon_luma_st_adr The reconstructed luma start address

VEPU_swreg_64

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Recon_chroma_st_adr The reconstructed chroma start address

VEPU_swreg_65_reuse

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_1 1st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_2 2st word used for check point used in h.264

VEPU_swreg_66_reuse

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_3 3st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_4 4st word used for check point used in h.264

VEPU_swreg_67_reuse

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_5 5st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_6 6st word used for check point used in h.264

VEPU_swreg_68_reuse

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_7 7st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_8 8st word used for check point used in h.264

VEPU_swreg_69_reuse

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_chkpt_9 9st word used for check point used in h.264
15:0	RW	0x0000	H264_chkpt_10 10st word used for check point used in h.264

VEPU_swreg_70_reuse

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_1 1st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_2 2st word error check point used in h.264

VEPU_swreg_71_reuse

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_3 3st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_4 4st word error check point used in h.264

VEPU_swreg_72_reuse

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	H264_errchkpt_5 5st word error check point used in h.264
15:0	RW	0x0000	H264_errchkpt_6 6st word error check point used in h.264

VEPU_swreg_73_reuse

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	Reserved
27:24	RW	0x0	Chkqp_1 1st for delta qp check point
23:20	RW	0x0	Chkqp_2 2st for delta qp check point
19:16	RW	0x0	Chkqp_3 3st for delta qp check point
15:12	RW	0x0	Chkqp_4 4st for delta qp check point
11:8	RW	0x0	Chkqp_5 5st for delta qp check point
7:4	RW	0x0	Chkqp_6 6st for delta qp check point
3:0	RW	0x0	Chkqp_7 7st for delta qp check point

VEPU_swreg_74

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:24	RW	0x00	Mad_thsld Value = (MAD threshold)/256
23:16	RW	0x00	Encodered_slices The number of encoder slices which used in h.264
15:8	RO	0x00	Reserved
7:4	RW	0x0	Img_fmt_in YUV420P YUV420SP YUV422 UYVY422 RGB565 RGB444 RGB888 RGB101010
3:2	RW	0x0	Img_in_rot 2'd0: No rotation 2'd1: Rotate right 90 degress 2'd2: Rotate left 90 degress

Bit	Attr	Reset Value	Description
1	RO	0x0	Reserved
0	RW	0x0	Nal_mode The output of NAL size to base control

VEPU_swreg_75

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Intramod_16x16
15:0	RW	0x0000	Intermod The intra/inter selection for inter macro block mode favor.

VEPU_swreg_76_reuse

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Pps_init_qp Pps init qp in picture used in h264. Range: 0~51
25:22	RW	0x0	Slice_flt_alpha Offset div2 Range: -6~6
21:18	RW	0x0	Slice_flt_beta Config value = (real value)/2 Signed register Range: -6 ~6
17:13	RW	0x00	Qp_offset_ch Signed register Range: -12~12
12:9	RO	0x0	Reserved
8	RW	0x0	Sw_qpass
7:5	RO	0x0	Reserved
4:1	RW	0x0	Idr_picid IDR pic ID
0	RW	0x0	Constr_intra_pred Constrained intra prediction

VEPU_swreg_77

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Output_strm_st_adr Output stream start address

VEPU_swreg_78

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Output_ctrl_st_adr Output control start address

VEPU_swreg_79

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Next_luma_st_adr Next picture luminance start address

VEPU_swreg_80

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Mv_out_st_adr Mv wr start address

VEPU_swreg_81

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Cabac_table_st_adr H264: Cabac table

VEPU_swreg_82

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	First_roi_tmb (Inside area)
23:16	RW	0x00	First_roi_bmb (Outside area)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	First_roi_lmb Qp=qp + roi1_Delta_Qp (Inside area)
7:0	RW	0x00	First_roi_rmb Qp=qp - roi1_Delta_Qp (Outside area)

VEPU_swreg_83

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Second_roi_rmb (Inside area)
23:16	RW	0x00	Second_roi_bmb (Outside area)
15:8	RW	0x00	Second_roi_lmb Qp=qp + roi1_Delta_Qp (Inside area)
7:0	RW	0x00	Second_roi_tmb Qp=qp - roi1_Delta_Qp (Outside area)

VEPU_swreg_84

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix1 (Position@ up-left)

VEPU_swreg_85

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix2 (Position @ up)

VEPU_swreg_86

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix3 (Position @up-right)

VEPU_swreg_87

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix4 (Position @ left)

VEPU_swreg_88

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix5 (Position @GMV)

VEPU_swreg_89

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix6 (Position@right)

VEPU_swreg_90

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix7 (Position@down-left)

VEPU_swreg_91

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:0	RW	0x000000	Stab_matrix8 (Position@down)

VEPU_swreg_92

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Stab_gmv_vrtl Signed register Range: -16~16
25:24	RO	0x0	Reserved
23:0	RW	0x000000	Stab_matrix9 (Position@down- right)

VEPU_swreg_93

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Stab_motion_sum Read value = (real value)/8 Range: 0~1089*253*255*53/8

VEPU_swreg_94

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Stab_min_value Range: 0~255*253*253
7:6	RW	0x0	Stab_mod_sel 2'd0: Disabled 2'd1: Stab only 2'd2: Stab+encode
5:0	RW	0x00	Stab_hor_gmv Signed register Range: -16~16

VEPU_swreg_95

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Rgb2yuv_coe2 The 2st conversion coefficien for RGB to YUV
15:0	RW	0x0000	Rgb2yuv_coe1 The 1st conversion coefficien for RGB to YUV

VEPU_swreg_96

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Rgb2yuv_coe5 The 5st conversion coefficien for RGB to YUV
15:0	RW	0x0000	Rgb2yuv_coe3 The 3st conversion coefficien for RGB to YUV

VEPU_swreg_97

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	Reserved
15:0	RW	0x0000	Rgb2yuv_coe6 The 6st conversion coefficien for RGB to YUV

VEPU_swreg_98

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	Reserved
20:16	RW	0x00	Bcmpt_mask_postition Range: 0~31
15:13	RO	0x0	Reserved
12:8	RW	0x00	Gcmpt_mask_postition Range: 0~31
7:5	RO	0x0	Reserved
4:0	RW	0x00	Rcmpt_mask_postition Range: 0~31

VEPU_swreg_99

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31	RO	0x0	Reserved
30:21	RW	0x000	Mv_1p_ply Differential MV penalty for 1p
20:11	RW	0x000	Mv_1p_4p_ply ME. DMVPenaltyQp
10:1	RW	0x000	Mv_4p_ply 4p of differential MV penalty
0	RW	0x0	Mutimv_en On-off flag for using exceed one mv every mb.

VEPU_swreg_100_reuse

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	H264_init_luma_qp Range: 0~51
25:20	RW	0x00	H264_max_qp Range: 0~51
19:14	RW	0x00	H264_min_qp Range: 0~51
13	RO	0x0	Reserved
12:0	RW	0x0000	H264_chkpt_distance Checkpoint distance for macro block

VEPU_swreg_101_read

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:12	RO	0x1f522	HW_CONFIG Field0000 Description
11:0	RO	0x780	MAX_VID_WIDTH Field0000 Description

VEPU_swreg_102

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	Reserved
23:20	RW	0x0	Mv_favor_16x16 Value = (real value)/2.
19:11	RW	0x000	Mv_ply_4x4 4x4 Mv Penalty
10:8	RW	0x0	Mvc_view_id MVC view id
7	RW	0x0	Mvc_anchor_pic_flag To specifie picture is one part of anchor access unit
6:4	RW	0x0	Mvc_priority_id MVC priority id
3:1	RW	0x0	Mvc_temporal_id MVC temporal id
0	RW	0x0	Mvc_inter_view_flag MVC inter_view_flag.

VEPU_swreg_103

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	Rreserved
28:20	RW	0x000	Enc_height Lum height (macroblock unit) H264: [6..255] JPEG: [6..511]
19:17	RO	0x0	Reserved
16:8	RW	0x000	Enc_width Lum width (macroblock unit) H264: Range: 9~255 JPEG: Range: 6~511
7:6	RW	0x0	Enc_frame_type 0: INTER 1: INTRA(IDR) 2: MVC-INTER
5:4	RW	0x0	Enc_fmt 2: JPEG 3: H264
3:1	RO	0x0	Reserved
0	RW	0x0	Enc_en Encoder enable

VEPU_swreg_104

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Mb_count_out Mb_count_out
15:0	RW	0x0000	Mb_cnt Macroblock_count

VEPU_swreg_105

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31	RW	0x0	Swap8_in 1'b0: No swap 1'b1: Swap 8bit
30	RW	0x0	Swap16_in 1'b0: No swap 1'b1: Swap 16bit
29	RW	0x0	Swap32_in 1'b0: No swap 1'b1: Swap 32bit
28	RW	0x0	Swap8_out 1'b0: No swap 1'b1: Swap 8bit
27	RW	0x0	Swap16_out 1'b0: No swap 1'b1: Swap 16bit
26	RW	0x0	Swap32_out 1'b0: No swap 1'b1: Swap 32bit
25	RO	0x0	Reserved
24	RW	0x0	Test_irq Test irq
23:20	RW	0x0	Test_counter Test counter
19	RW	0x0	Coher_test_reg Test register coherency
18	RW	0x0	Coher_test_mem Test memory coherency
17:0	RW	0x00000	Test_len Test data length

VEPU_swreg_106_reuse

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Pic_para_id H.264 picture parameter id set
23:16	RW	0x00	Intra_pred_mode H.264 intra prediction previous 4x4 mode favor
15:0	RW	0x0000	Frame_num H.264 frame number

VEPU_swreg_107_reuse

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	Reserved
29:20	RW	0x000	Mv_ply_16x8_8x16 Penalty for using 16x8 or 8x16 MV
19:10	RW	0x000	Mv_ply_8x8 Penalty for using 8x8 MV
9:0	RW	0x000	Mv_ply_8x4_4x8 Penalty for using 8x4 or 4x8 MV.

VEPU_swreg_108_reuse

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Intra_slice_bmp2 Bit0: Slices64 Bit1: Slices65 Bit2: Slices66 ..... Bit31: Slices95

VEPU_swreg_109

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	Mv_sad_wren The each MB MV and SAD be writed to mv_wr_st_adr enable
23:21	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	Rocon_write_dis Write reconstructed image disable flag
19:17	RO	0x0	Reserved
16	RW	0x0	Slice_rdyint_en Enable slice ready interruupt
15:13	RO	0x0	Reserved
12	RW	0x1	Clk_gating_en Default clk_gating_en =1'b1
11	RO	0x0	Reserved
10	RW	0x0	Int_timeout_en Enable interrupt for timeout
9	RW	0x0	Irq_clr Irq clear
8	RW	0x0	Irq_dis Irq disable
7	RO	0x0	Reserved
6	RW	0x0	Irq_timeout HW wait timeout flag
5	RW	0x0	Irq_buffer_full Buffer full flag
4	RW	0x0	Irq_bus_error Bus error irq
3	RW	0x0	Fuse_int Fuse irq
2	RW	0x0	Irq_slice_ready Slice ready flag
1	RW	0x0	Irq_frame_rdy One frame encoder sucess flag
0	RW	0x0	Enc_irq Enc interrupt

VEPU_swreg_110_read

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:16	RO	0x4831	Prod_id Product ID
15:12	RO	0x1	Major_num Major number
11:4	RO	0x22	Minor_num Minor number

Bit	Attr	Reset Value	Description
3:0	RO	0x0	Synthesis {ASCII_ID_E,BUILDNUMBER}

VEPU_swreg_120_183

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	Dmv_ply_table Addr range: 0x01e0~0x02dc Swreg120: DMV 4p/1p penalty table values Swreg121: DMV 4p/1p penalty table values Swreg122: DMV 4p/1p penalty table values Swreg123: DMV 4p/1p penalty table values ..... Swreg183: DMV 4p/1p penalty table values

10.5.22 VEPU121 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state
VCODEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
VCODEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
VCODEC_MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
VCODEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
VCODEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.23 VEPU121 MMU Detail Registers Description

VCODEC_MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

VCODEC_MMU_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	Reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master responsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY 1'b1:The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled. The mode is enabled by command. 1'b1: Page fault is active
0	RO	0x0	PAGING_ENABLED 1'b0: Paging is disabled 1'b1: Paging is enabled

VCODEC_MMU_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	Reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET

VCODEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

VCODEC_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE ddress to be invalidated from the page table cache

VCODEC_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Read bus error status
0	RW	0x0	PAGE_FAULT Page fault status

VCODEC_MMU_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	WO	0x0	READ_BUS_ERROR Write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT Write 1 to page fault clear

VCODEC_MMU_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RW	0x0	READ_BUS_ERROR Enable the read bus interrupt source when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT Enable the page fault interrupt source when this bit is set to 1'b1

VCODEC_MMU_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	Reserved
1	RO	0x0	READ_BUS_ERROR 1'b1: Read bus error status
0	RO	0x0	PAGE_FAULT 1'b1: Page fault

VCODEC_MMU_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	Reserved
0	RW	0x1	Mmu_auto_clkgating When it is 1'b1, the mmu will auto gating it self

10.5.24 VEPU540 LAYER1 Register Address Mapping

The summary of LAYER1 register is listed below.

Table 10-15 VEPU LAYER1 Address Mapping

Name	Offset	Size	Reset Value	Description
VEPU_VERSION	0x0000	W	0x50600311	VEPU version. It contains IP function summary and sub-version informations.
VEPU_ENC_STRT	0x0004	W	0x00000000	Start cmd register.(auto clock gating enable, auto reset enable and tmvp adjust enable when frame done are also allocated here.)
VEPU_ENC_CLR	0x0008	W	0x00000000	VEPU clear register
VEPU_LKT_ADDR	0x000C	W	0x00000000	Link table
VEPU_INT_EN	0x0010	W	0x00000000	VEPU interrupt enable
VEPU_INT_MSK	0x0014	W	0x00000000	VEPU interrupt mask
VEPU_INT_CLR	0x0018	W	0x00000000	VEPU interrupt clear
VEPU_INT_STA	0x001C	W	0x00000000	VEPU interrupt state
VEPU_ENC_IDLE_EN	0x0020	W	0x00000000	
VEPU_ENC_RSL	0x0030	W	0x00000000	Resolution
VEPU_ENC_PIC	0x0034	W	0x00000000	VEPU common configuration
VEPU_ENC_WDG	0x0038	W	0x00000000	VEPU watch dog configure register
VEPU_DTRNS_MAP	0x003C	W	0x00000000	Data transaction mapping (endian and order)
VEPU_DTRNS_CFG	0x0040	W	0x00000000	(AXI bus) Data transaction configuration
VEPU_SRC_FMT	0x0044	W	0x00000000	Video source format
VEPU_SRC_UDFY	0x0048	W	0x00000000	Weight of user defined formula for RGB to Y conversion
VEPU_SRC_UDFU	0x004C	W	0x00000000	Weight of user defined formula for RGB to U conversion
VEPU_SRC_UDFV	0x0050	W	0x00000000	Weight of user defined formula for RGB to V conversion

Name	Offset	Size	Reset Value	Description
VEPU_SRC_UDFO	0x0054	W	0x00000000	Offset of user defined formula for RGB to YUV conversion
VEPU_SRC_PROC	0x0058	W	0x00000000	Video source process
VEPU_SLI_CFG_H264	0x005C	W	0x00000000	Slice cross lines configuration, h264 only.
VEPU_TILE_CFG_HEVC	0x005C	W	0x00000000	Current tile configuration, hevc only.
VEPU_TILE_POS	0x0060	W	0x00000000	Current tile posion of the picture, hevc only.
VEPU_KLUT_OFST	0x0064	W	0x00000000	Offset of (RDO) chroma cost weight table
VEPU_KLUT_WGT0	0x0068	W	0x00000000	(RDO) Chroma weight table configure register0
VEPU_KLUT_WGT1	0x006C	W	0x00000000	(RDO) Chroma weight table configure register1
VEPU_KLUT_WGT2	0x0070	W	0x00000000	(RDO) Chroma weight table configure register2
VEPU_KLUT_WGT3	0x0074	W	0x00000000	(RDO) Chroma weight table configure register3
VEPU_KLUT_WGT4	0x0078	W	0x00000000	(RDO) Chroma weight table configure register4
VEPU_KLUT_WGT5	0x007C	W	0x00000000	(RDO) Chroma weight table configure register5
VEPU_KLUT_WGT6	0x0080	W	0x00000000	(RDO) Chroma weight table configure register6
VEPU_KLUT_WGT7	0x0084	W	0x00000000	(RDO) Chroma weight table configure register7
VEPU_KLUT_WGT8	0x0088	W	0x00000000	(RDO) Chroma weight table configure register8
VEPU_KLUT_WGT9	0x008C	W	0x00000000	(RDO) Chroma weight table configure register9

Name	Offset	Size	Reset Value	Description
VEPU_KLUT_WGT10	0x0090	W	0x00000000	(RDO) Chroma weight table configure register10
VEPU_KLUT_WGT11	0x0094	W	0x00000000	(RDO) Chroma weight table configure register11
VEPU_KLUT_WGT12	0x0098	W	0x00000000	(RDO) Chroma weight table configure register12
VEPU_KLUT_WGT13	0x009C	W	0x00000000	(RDO) Chroma weight table configure register13
VEPU_KLUT_WGT14	0x00A0	W	0x00000000	(RDO) Chroma weight table configure register14
VEPU_KLUT_WGT15	0x00A4	W	0x00000000	(RDO) Chroma weight table configure register15
VEPU_KLUT_WGT16	0x00A8	W	0x00000000	(RDO) Chroma weight table configure register16
VEPU_KLUT_WGT17	0x00AC	W	0x00000000	(RDO) Chroma weight table configure register17
VEPU_KLUT_WGT18	0x00B0	W	0x00000000	(RDO) Chroma weight table configure register18
VEPU_KLUT_WGT19	0x00B4	W	0x00000000	(RDO) Chroma weight table configure register19
VEPU_KLUT_WGT20	0x00B8	W	0x00000000	(RDO) Chroma weight table configure register20
VEPU_KLUT_WGT21	0x00BC	W	0x00000000	(RDO) Chroma weight table configure register21
VEPU_KLUT_WGT22	0x00C0	W	0x00000000	(RDO) Chroma weight table configure register22
VEPU_KLUT_WGT23	0x00C4	W	0x00000000	(RDO) Chroma weight table configure register23
VEPU_RC_CFG	0x00C8	W	0x00000000	Rate control configuration
VEPU_RC_QP	0x00CC	W	0x00000000	QP configuration for rate control
VEPU_RC_TGT	0x00D0	W	0x00000000	The target bit rate for rate control

Name	Offset	Size	Reset Value	Description
VEPU_RC_ADJ0	0x00D4	W	0x00000000	QP adjust configuration for rate control
VEPU_RC_ADJ1	0x00D8	W	0x00000000	QP adjust configuration for rate control
VEPU_RC_DTHD0	0x00DC	W	0x00000000	Bits rate deviation threshold0
VEPU_RC_DTHD1	0x00E0	W	0x00000000	Bits rate deviation threshold1
VEPU_RC_DTHD2	0x00E4	W	0x00000000	Bits rate deviation threshold2
VEPU_RC_DTHD3	0x00E8	W	0x00000000	Bits rate deviation threshold3
VEPU_RC_DTHD4	0x00EC	W	0x00000000	Bits rate deviation threshold4
VEPU_RC_DTHD5	0x00F0	W	0x00000000	Bits rate deviation threshold5
VEPU_RC_DTHD6	0x00F4	W	0x00000000	Bits rate deviation threshold6
VEPU_RC_DTHD7	0x00F8	W	0x00000000	Bits rate deviation threshold7
VEPU_RC_DTHD8	0x00FC	W	0x00000000	Bits rate deviation threshold8
VEPU_ROI_QTHD0	0x0100	W	0x00000000	ROI QP threshold configuration0
VEPU_ROI_QTHD1	0x0104	W	0x00000000	ROI QP threshold configuration1
VEPU_ROI_QTHD2	0x0108	W	0x00000000	ROI QP threshold configuration2
VEPU_ROI_QTHD3	0x010C	W	0x00000000	ROI QP threshold configuration3
VEPU_PIC_OFST	0x0110	W	0x00000000	Encoding picture offset
VEPU_SRC_STRD	0x0114	W	0x00000000	Video source stride
VEPU_ADR_SRC0	0x0118	W	0x00000000	Base address of the 1st storage area for video source
VEPU_ADR_SRC1	0x011C	W	0x00000000	Base address of the 2nd storage area for video source
VEPU_ADR_SRC2	0x0120	W	0x00000000	Base address of the 3rd storage area for video source
VEPU_ADR_ROI	0x0124	W	0x00000000	Base address for ROI configuration, 16 bytes aligned

Name	Offset	Size	Reset Value	Description
VEPU_ADR_RFPW_H	0x0128	W	0x00000000	Base address of header_block for compressed reference frame write, 4K bytes aligned
VEPU_ADR_RFPW_B	0x012C	W	0x00000000	Base address of body_block for compressed reference frame write, 4K bytes aligned
VEPU_ADR_RFPR_H	0x0130	W	0x00000000	Base address of header_block for compressed reference frame read, 4K bytes aligned
VEPU_ADR_RFPR_B	0x0134	W	0x00000000	Base address of body_block for compressed reference frame read, 4K bytes aligned
VEPU_ADR_CMVW	0x0138	W	0x00000000	Base address for col-located Mv write, 1KB aligned, HEVC only
VEPU_ADR_CMVR	0x013C	W	0x00000000	Base address for col-located Mv read, 1KB aligned, HEVC only
VEPU_ADR_DSPW	0x0140	W	0x00000000	Base address for down-sampled reference frame write, 1KB aligned
VEPU_ADR_DSPR	0x0144	W	0x00000000	Base address for down-sampled reference frame read, 1KB aligned
VEPU_ADR_MEIW	0x0148	W	0x00000000	Base address for ME information write, 1KB aligned
VEPU_ADR_BSBT	0x014C	W	0x00000000	Top address of bit stream buffer, 128B aligned
VEPU_ADR_BSBB	0x0150	W	0x00000000	Bottom address of bit stream buffer, 128B aligned
VEPU_ADR_BSBR	0x0154	W	0x00000000	Read address of bit stream buffer, 128B aligned
VEPU_ADR_BSBS	0x0158	W	0x00000000	Start address of bit stream buffer
VEPU_SLI_SPLT	0x015C	W	0x00000000	Slice split configuration
VEPU_SLI_BYTE	0x0160	W	0x00000000	Number of bytes for slice split
VEPU_ME_RNGE	0x0164	W	0x00000000	Motion estimation range

Name	Offset	Size	Reset Value	Description
VEPU_ME_CFG	0x0168	W	0x00090505	Motion estimation configuration
VEPU_ME_CACH	0x016C	W	0x00000000	ME cache configuration
VEPU_SYNT_LONG_REFM0	0x0170	W	0x00000000	Long term reference frame mark0 for HEVC
VEPU_SYNT_LONG_REFM1	0x0174	W	0x00000000	Long term reference frame mark1 for HEVC
VEPU_OSD_INV_CFG	0x0178	W	0x00000000	OSD color inverse configuration
VEPU_ADR_LPFW	0x017C	W	0x00000000	Base address for LPFW, 1KB aligned, HEVC only.
VEPU_ADR_LPFR	0x0180	W	0x00000000	Base address for LPFR, 1KB aligned, HEVC only.
VEPU_IPRD_CSTS	0x0194	W	0x00000000	Cost function configuration for intra prediction
VEPU_RDO_CFG_H264	0x0198	W	0x00000000	H.264 RDO configuration, share address with HEVC
VEPU_RDO_CFG_HEVC	0x0198	W	0x00000000	HEVC RDO configuration, share address with H.264
VEPU_SYNT_NAL_H264	0x019C	W	0x00000000	NAL configuration for H.264, share address with HEVC
VEPU_SYNT_NAL_HEVC	0x019C	W	0x00000000	NAL configuration for HEVC, share address with H.264
VEPU_SYNT_SPS_H264	0x01A0	W	0x00000000	Sequence parameter set syntax configuration for H.264, share address with HEVC
VEPU_SYNT_SPS_HEVC	0x01A0	W	0x00000000	Sequence parameter set syntax configuration for HEVC, share address with H.264
VEPU_SYNT_PPS_H264	0x01A4	W	0x00000000	Picture parameter set configuration for H.264, share address with HEVC
VEPU_SYNT_PPS_HEVC	0x01A4	W	0x00000000	Picture parameter set configuration for HEVC, share address with H.264

Name	Offset	Size	Reset Value	Description
VEPU_SYNT_SLI0_H264	0x01A8	W	0x00000000	Slice header configuration0 for H.264, share address with HEVC
VEPU_SYNT_SLI0_HEVC	0x01A8	W	0x00000000	Slice header configuration0 for HEVC, share address with H.264
VEPU_SYNT_SLI1_H264	0x01AC	W	0x00000000	Slice header configuration1 for H.264, share address with HEVC
VEPU_SYNT_SLI1_HEVC	0x01AC	W	0x00000000	Slice header configuration1 for HEVC, share address with H.264
VEPU_SYNT_SLI2_H264	0x01B0	W	0x00000000	Slice header configuration2 for H.264, share address with HEVC
VEPU_SYNT_SLI2_HEVC	0x01B0	W	0x00000000	Slice header configuration2 for HEVC, share address with H.264
VEPU_SYNT_REFM0_H264	0x01B4	W	0x00000000	Reference frame mark0 for H.264, share address with HEVC
VEPU_SYNT_REFM0_HEVC	0x01B4	W	0x00000000	Reference frame mark0 for HEVC, share address with H.264
VEPU_SYNT_REFM1_H264	0x01B8	W	0x00000000	Reference frame mark1 for H.264, share address with HEVC
VEPU_SYNT_REFM1_HEVC	0x01B8	W	0x00000000	Reference frame mark1 for HEVC, share address with H.264
VEPU_OSD_CFG	0x01C0	W	0x00000000	OSD configuration
VEPU_OSD_INV	0x01C4	W	0x00000000	OSD color inverse threshold
VEPU_SYNT_REFM2	0x01C8	W	0x00000000	Reference frame mark2 for HEVC
VEPU_SYNT_REFM2_H264	0x01C8	W	0x00000000	Reference frame mark2 for H264
VEPU_SYNT_REFM3	0x01CC	W	0x00000000	Reference frame mark3 for HEVC
VEPU_OSD0_POS	0x01D0	W	0x00000000	OSD region0 position
VEPU_OSD1_POS	0x01D4	W	0x00000000	OSD region1 position
VEPU_OSD2_POS	0x01D8	W	0x00000000	OSD region2 position
VEPU_OSD3_POS	0x01DC	W	0x00000000	OSD region3 position

Name	Offset	Size	Reset Value	Description
VEPU_OSD4_POS	0x01E0	W	0x00000000	OSD region4 position
VEPU_OSD5_POS	0x01E4	W	0x00000000	OSD region5 position
VEPU_OSD6_POS	0x01E8	W	0x00000000	OSD region6 position
VEPU_OSD7_POS	0x01EC	W	0x00000000	OSD region7 position
VEPU_ADR_OSD0	0x01F0	W	0x00000000	Base address for OSD region0, 16B aligned
VEPU_ADR_OSD1	0x01F4	W	0x00000000	Base address for OSD region1, 16B aligned
VEPU_ADR_OSD2	0x01F8	W	0x0	Base address for OSD region2, 16B aligned
VEPU_ADR_OSD3	0x01FC	W	0x00000000	Base address for OSD region3, 16B aligned
VEPU_ADR_OSD4	0x0200	W	0x00000000	Base address for OSD region4, 16B aligned
VEPU_ADR_OSD5	0x0204	W	0x00000000	Base address for OSD region5, 16B aligned
VEPU_ADR_OSD6	0x0208	W	0x00000000	Base address for OSD region6, 16B aligned
VEPU_ADR_OSD7	0x020C	W	0x00000000	Base address for OSD region7, 16B aligned
VEPU_ST_BSL	0x0210	W	0x00000000	Bit stream length for current frame
VEPU_ST_SSE_L32	0x0214	W	0x00000000	Low 32 bits of encoding distortion (SSE)
VEPU_ST_SSE_QP	0x0218	W	0x00000000	High 8 bits of encoding distortion (SSE) and sum of QP for the encoded frame
VEPU_ST_SAO	0x021C	W	0x00000000	Number of CTUs which adjusted by SAO
VEPU_ST_HEAD_BL	0x0220	W	0x00000000	Total bit length of RDO HeaderBits.

Name	Offset	Size	Reset Value	Description
VEPU_ST_RES_BL	0x0224	W	0x00000000	Total bit length of RDO ResidualBits.
VEPU_ST_ENC	0x0228	W	0x00000000	VEPU working status
VEPU_ST_LKT	0x022C	W	0x00000000	Status of link table mode encoding
VEPU_ST_NADR	0x0230	W	0x00000000	Address of the processing link table node
VEPU_ST_BSB	0x0234	W	0x00000000	Status of bit stream buffer
VEPU_ST_BUS	0x0238	W	0x00000000	VEPU bus status
VEPU_ST_SNUM	0x023C	W	0x00000000	Slice number status
VEPU_ST_SLEN	0x0240	W	0x00000000	Status of slice length
VEPU_ST_PNUM_P64	0x0244	W	0x00000000	Number of 64x64 inter predicted blocks
VEPU_ST_PNUM_P32	0x0248	W	0x00000000	Number of 32x32 inter predicted blocks
VEPU_ST_PNUM_P16	0x024C	W	0x00000000	Number of 16x16 inter predicted blocks
VEPU_ST_PNUM_P8	0x0250	W	0x00000000	Number of 8x8 inter predicted blocks
VEPU_ST_PNUM_I32	0x0254	W	0x00000000	Number of 32x32 intra predicted blocks
VEPU_ST_PNUM_I16	0x0258	W	0x00000000	Number of 16x16 intra predicted blocks
VEPU_ST_PNUM_I8	0x025C	W	0x00000000	Number of 8x8 intra predicted blocks
VEPU_ST_PNUM_I4	0x0260	W	0x00000000	Number of 4x4 intra predicted blocks
VEPU_ST_B8_QP0	0x0264	W	0x00000000	Number of block8x8s with QP=0
VEPU_ST_B8_QP1	0x0268	W	0x00000000	Number of block8x8s with QP=1

Name	Offset	Size	Reset Value	Description
VEPU_ST_B8_QP2	0x026C	W	0x00000000	Number of block8x8s with QP=2
VEPU_ST_B8_QP3	0x0270	W	0x00000000	Number of block8x8s with QP=3
VEPU_ST_B8_QP4	0x0274	W	0x00000000	Number of block8x8s with QP=4
VEPU_ST_B8_QP5	0x0278	W	0x00000000	Number of block8x8s with QP=5
VEPU_ST_B8_QP6	0x027C	W	0x00000000	Number of block8x8s with QP=6
VEPU_ST_B8_QP7	0x0280	W	0x00000000	Number of block8x8s with QP=7
VEPU_ST_B8_QP8	0x0284	W	0x00000000	Number of block8x8s with QP=8
VEPU_ST_B8_QP9	0x0288	W	0x00000000	Number of block8x8s with QP=9
VEPU_ST_B8_QP10	0x028C	W	0x00000000	Number of block8x8s with QP=10
VEPU_ST_B8_QP11	0x0290	W	0x00000000	Number of block8x8s with QP=11
VEPU_ST_B8_QP12	0x0294	W	0x00000000	Number of block8x8s with QP=12
VEPU_ST_B8_QP13	0x0298	W	0x00000000	Number of block8x8s with QP=13
VEPU_ST_B8_QP14	0x029C	W	0x00000000	Number of block8x8s with QP=14
VEPU_ST_B8_QP15	0x02A0	W	0x00000000	Number of block8x8s with QP=15
VEPU_ST_B8_QP16	0x02A4	W	0x00000000	Number of block8x8s with QP=16
VEPU_ST_B8_QP17	0x02A8	W	0x00000000	Number of block8x8s with QP=17
VEPU_ST_B8_QP18	0x02AC	W	0x00000000	Number of block8x8s with QP=18
VEPU_ST_B8_QP19	0x02B0	W	0x00000000	Number of block8x8s with QP=19
VEPU_ST_B8_QP20	0x02B4	W	0x00000000	Number of block8x8s with QP=20
VEPU_ST_B8_QP21	0x02B8	W	0x00000000	Number of block8x8s with QP=21
VEPU_ST_B8_QP22	0x02BC	W	0x00000000	Number of block8x8s with QP=22
VEPU_ST_B8_QP23	0x02C0	W	0x00000000	Number of block8x8s with QP=23
VEPU_ST_B8_QP24	0x02C4	W	0x00000000	Number of block8x8s with QP=24

Name	Offset	Size	Reset Value	Description
VEPU_ST_B8_QP25	0x02C8	W	0x00000000	Number of block8x8s with QP=25
VEPU_ST_B8_QP26	0x02CC	W	0x00000000	Number of block8x8s with QP=26
VEPU_ST_B8_QP27	0x02D0	W	0x00000000	Number of block8x8s with QP=27
VEPU_ST_B8_QP28	0x02D4	W	0x00000000	Number of block8x8s with QP=28
VEPU_ST_B8_QP29	0x02D8	W	0x00000000	Number of block8x8s with QP=29
VEPU_ST_B8_QP30	0x02DC	W	0x00000000	Number of block8x8s with QP=0
VEPU_ST_B8_QP31	0x02E0	W	0x00000000	Number of block8x8s with QP=31
VEPU_ST_B8_QP32	0x02E4	W	0x00000000	Number of block8x8s with QP=32
VEPU_ST_B8_QP33	0x02E8	W	0x00000000	Number of block8x8s with QP=33
VEPU_ST_B8_QP34	0x02EC	W	0x00000000	Number of block8x8s with QP=34
VEPU_ST_B8_QP35	0x02F0	W	0x00000000	Number of block8x8s with QP=35
VEPU_ST_B8_QP36	0x02F4	W	0x00000000	Number of block8x8s with QP=36
VEPU_ST_B8_QP37	0x02F8	W	0x00000000	Number of block8x8s with QP=37
VEPU_ST_B8_QP38	0x02FC	W	0x00000000	Number of block8x8s with QP=38
VEPU_ST_B8_QP39	0x0300	W	0x00000000	Number of block8x8s with QP=39
VEPU_ST_B8_QP40	0x0304	W	0x00000000	Number of block8x8s with QP=40
VEPU_ST_B8_QP41	0x0308	W	0x00000000	Number of block8x8s with QP=41
VEPU_ST_B8_QP42	0x030C	W	0x00000000	Number of block8x8s with QP=42
VEPU_ST_B8_QP43	0x0310	W	0x00000000	Number of block8x8s with QP=43
VEPU_ST_B8_QP44	0x0314	W	0x00000000	Number of block8x8s with QP=44
VEPU_ST_B8_QP45	0x0318	W	0x00000000	Number of block8x8s with QP=45
VEPU_ST_B8_QP46	0x031C	W	0x00000000	Number of block8x8s with QP=46
VEPU_ST_B8_QP47	0x0320	W	0x00000000	Number of block8x8s with QP=47

Name	Offset	Size	Reset Value	Description
VEPU_ST_B8_QP48	0x0324	W	0x00000000	Number of block8x8s with QP=48
VEPU_ST_B8_QP49	0x0328	W	0x00000000	Number of block8x8s with QP=49
VEPU_ST_B8_QP50	0x032C	W	0x00000000	Number of block8x8s with QP=50
VEPU_ST_B8_QP51	0x0330	W	0x00000000	Number of block8x8s with QP=51
VEPU_ST_CPLX_TMP	0x0334	W	0x00000000	Temporal complexity(MADP) for current encoding and reference frame
VEPU_ST_BNUM_CME	0x0338	W	0x00000000	Number of CME blocks in frame. H.264: number CME blocks (4 MBs) in 16x64 aligned extended frame, except for the CME blocks configured as force intra. HEVC: number CME blocks (CTU) in 64x64 aligned extended frame, except for the CME blocks configured as force intra.
VEPU_ST_CPLX_SPT	0x033C	W	0x00000000	Spatial complexity(MADI) for current encoding frame
VEPU_ST_BNUM_B16	0x0340	W	0x00000000	Number of 16x16 blocks in frame. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame.
VEPU_ST_CPLX_MAX_B16	0x0344	W	0x00000000	Number of 16x16 blocks which the value is bigger than sw_aq_thd15. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame.
VEPU_L2CFG_ADDR	0x03F0	W	0x00000000	Level2 configuration address
VEPU_L2CFG_WDATA	0x03F4	W	0x00000000	L2 configuration write data
VEPU_L2CFG_RDATA	0x03F8	W	0x00000000	L2 configuration read data
VEPU_OSD_PLT0	0x0400	W	0x00000000	User defined OSD palette color0
VEPU_OSD_PLT1	0x0404	W	0x00000000	User defined OSD palette color1

Name	Offset	Size	Reset Value	Description
VEPU_OSD_PLT255	0x07FC	W	0x00000000	OSD palette color255
VEPU_ST_WDG	0x085C	W	0x00000000	VEPU watch dog status
VEPU_ST_PPL	0x0860	W	0x00000000	VEPU pipe line status
VEPU_ST_SLI_NUM	0x0874	W	0x00000000	Number of slices
VEPU_DBG_DMA_RFPR	0x08E4	W	0x00000000	Debug register for DMA RFPR channel
VEPU_DBG_DMA_CH_ST	0x08E8	W	0x00000000	Debug register for DMA status
VEPU_MMU0_ADDR	0x0F00	W	0x00000000	Page table address for AXI0 MMU
VEPU_MMU0_ST	0x0F04	W	0x00000000	Status of the MMU for AXI0
VEPU_MMU0_CMD	0x0F08	W	0x00000000	MMU command for AXI0
VEPU_MMU0_PFA	0x0F0C	W	0x00000000	Address of the last page fault for MMU0
VEPU_MMU0_ZAP	0x0F10	W	0x00000000	Zap address for MMU0
VEPU_MMU0_ERR	0x0F14	W	0x00000000	MMU error
VEPU_MMU0_INT_CLR	0x0F18	W	0x00000000	Interrupt clear for MMU0
VEPU_MMU0_INT_MSK	0x0F1C	W	0x00000000	Interrupt mask for MMU0
VEPU_MMU0_INT_STA	0x0F20	W	0x00000000	Interrupt status for MMU0
VEPU_MMU0_ACKG	0x0F24	W	0x00000001	Auto clock gating for MMU0
VEPU_MMU1_ADDR	0x0F40	W	0x00000000	Page table address for AXI1 MMU
VEPU_MMU1_ST	0x0F44	W	0x00000000	Status of the MMU for AXI1
VEPU_MMU1_CMD	0x0F48	W	0x00000000	MMU command for AXI1
VEPU_MMU1_PFA	0x0F4C	W	0x00000000	Address of the last page fault for MMU1
VEPU_MMU1_ZAP	0x0F50	W	0x00000000	Zap address for MMU1
VEPU_MMU1_ERR	0x0F54	W	0x00000000	MMU error

Name	Offset	Size	Reset Value	Description
VEPU_MMU1_INT_CLR	0x0F58	W	0x00000000	Interrupt clear for MMU1
VEPU_MMU1_INT_MSK	0x0F5C	W	0x00000000	Interrupt mask for MMU1
VEPU_MMU1_INT_STA	0x0F60	W	0x00000000	Interrupt status for MMU1
VEPU_MMU1_ACKG	0x0F64	W	0x00000001	Auto clock gating for MMU1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.25 VEPU540 LAYER1 Detail Register Description

VEPU_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x50	ip_id VEPU ID. It is contant 0x50.
23	RO	0x0	reserved
22:21	RO	0x3	fbc_cap FBC capability: 2'h0: No FBC 2'h3: Support AFBC for video source and FBC for reconstructed picture Others: Reserved
20	RO	0x0	bfrm_cap B frame encoding capability. 1 means VEPU supports B frame encoding while 0 means not.
19:18	RO	0x0	filtr_cap Pre-process filter capability 2'h0: Basic pre-process filter 2'h3: No pre-process filter Others: Reserved
17:16	RO	0x0	osd_cap OSD capability. 2'h0: 8-area OSD with 256-color palette 2'h3: No OSD Others: Reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	res_cap Max resolution 4'h0: 4096x2304 4'h1: 1920x1088 Others: Reserved
11:10	RO	0x0	reserved
9	RO	0x1	hevc_cap HEVC encoding capability. 1 means VEPU supports HEVC encoding while 0 means not
8	RO	0x1	h264_cap H.264 encoding capability. 1 means VEPU supports H.264 encoding, while 0 means not.
7:0	RO	0x11	sub_ver VEPU sub-version. 0x11 for PUMA

VEPU_ENC_STRT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	enc_done_tmvp_en Enc_done need wait tmvp write done by dma.
17	RW	0x0	resetn_hw_en Encoder auto reset core clock domain when frame finished.
16	RW	0x0	cke VEPU auto clock gating enable
15:10	RO	0x00	reserved
9:8	RW	0x0	vepu_cmd VEPU command: 2'h0: N/A 2'h1: One frame encoding by register configuration 2'h2: Multi-frame encoding start with link table mode 2'h3: Multi-frame encoding update (with link table mode)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	lkt_num Number of new nodes in link table. only for link table mode.

VEPU_ENC_CLR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	force_clr Force clear. Clear all sub-modules besides regfile and AHB data path.
0	R/W SC	0x0	safe_clr Safe clr. It only clears DMA module to confirm AXI transaction integrity. 1'h0: Safe clear is not performing. 1'h1: Safe clear is performing.

VEPU_LKT_ADDR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	lkt_addr High 28 bits of the address for the first node in link table.
3:0	RO	0x0	reserved

VEPU_INT_EN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	wdg_en Watch dog(time out) interrupt enable.
7	RW	0x0	rbus_err_en AXI read channel error interrupt enable.

Bit	Attr	Reset Value	Description
6	RW	0x0	wbus_err_en AXI write channel error interrupt enable.
5	RW	0x0	brsp_otsd_en AXI write response outstanding overflow interrupt enable.
4	RW	0x0	bsf_oflw_en Bit stream buffer overflow enable.
3	RW	0x0	slc_done_en One slice encoding finish interrupt enable.
2	RW	0x0	sclr_done_en Safe clear finish interrupt enable.
1	RW	0x0	lkt_done_en Link table (node) finish interrupt enable.
0	RW	0x0	enc_done_en One frame encoding finish interrupt enable.

VEPU_INT_MSK

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	wdg_msk Watch dog(time out) interrupt mask.
7	RW	0x0	rbus_err_msk AXI read channel error interrupt mask.
6	RW	0x0	wbus_err_msk AXI write channel error interrupt mask.
5	RW	0x0	brsp_otsd_msk AXI write response outstanding overflow interrupt mask.
4	RW	0x0	bsf_oflw_msk Bit stream buffer overflow mask.
3	RW	0x0	slc_done_msk One slice encoding finish interrupt mask.

Bit	Attr	Reset Value	Description
2	RW	0x0	sclr_done_msk Safe clear finish interrupt mask.
1	RW	0x0	lkt_done_msk Link table (node) finish interrupt mask.
0	RW	0x0	enc_done_msk One frame encoding finish interrupt mask.

VEPU_INT_CLR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1C	0x0	wdg_clr Watch dog(time out) interrupt clear.
7	W1C	0x0	rbus_err_clr AXI read channel error interrupt clear.
6	W1C	0x0	wbus_err_clr AXI write channel error interrupt clear.
5	W1C	0x0	brsp_otsd_clr AXI write response outstanding overflow interrupt clear.
4	W1C	0x0	bsf_oflw_clr Bit stream buffer overflow clear.
3	W1C	0x0	slc_done_clr One slice encoding finish interrupt clear.
2	W1C	0x0	sclr_done_clr Safe clear finish interrupt clear.
1	W1C	0x0	lkt_done_clr Link table (node) finish interrupt clear.
0	W1C	0x0	enc_done_clr One frame encoding finish interrupt clear.

VEPU_INT_STA

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	wdg_sta Watch dog(time out) interrupt status.
7	RO	0x0	rbus_err_sta AXI read channel error interrupt status.
6	RO	0x0	wbus_err_sta AXI write channel error interrupt status.
5	RO	0x0	brsp_otsd_sta AXI write response outstanding overflow interrupt status.
4	RO	0x0	bsf_oflw_sta Bit stream buffer overflow status.
3	RO	0x0	slc_done_sta One slice encoding finish interrupt status.
2	RO	0x0	sclr_done_sta Safe clear finish interrupt status.
1	RO	0x0	lkt_done_sta Link table (node) finish interrupt status.
0	RO	0x0	enc_done_sta One frame encoding finish interrupt status.

VEPU_ENC_IDLE_EN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	idle_en_ahb
1	RW	0x0	idle_en_axi
0	RW	0x0	idle_en_core

VEPU_ENC_RSL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	pic_hfill Filling pixels to keep (encoding) picture height is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
25	RO	0x0	reserved
24:16	RW	0x000	pic_hd8_m1 Ceil(encoding picture height/8) -1
15:10	RW	0x00	pic_wfill Filling pixels to keep (encoding) picture width is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
9	RO	0x0	reserved
8:0	RW	0x000	pic_wd8_m1 Ceil(encoding picture width/8) -1

VEPU_ENC_PIC

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	node_int Node interrupt enable (only for link table node configuration).
30	RW	0x0	slen_fifo Slice length fifo enable.
29	RW	0x0	dchs_txe Dual-core handshake tx enable.
28	RW	0x0	dchs_rxe Dual-core handshake rx enable.
27:26	RW	0x0	dchs_txid Dual-core handshake tx ID.
25:24	RW	0x0	dchs_rxid Dual-core handshake Rx ID.
23	RW	0x0	atr_thd_sel 1'h0: Select atr_thd group0. 1'h1: Select atr_thd group1.

Bit	Attr	Reset Value	Description
22:19	RW	0x0	log2_ctu_num Logarithm of bit width to express ctu number in current picture, HEVC only.
18:14	RW	0x00	num_pic_tot_cur NumPicTotalCurr for HEVC reference picture list modification.
13:8	RW	0x00	pic_qp QP value for current frame encoding.
7:6	RO	0x0	reserved
5	RW	0x0	rdo_wgt_sel Select the group of RDO weight parameters(VEPU2_RDO_WGTA_QP* and VEPU2_RDO_WGTB*). 1'h0: Select weight group A (VEPU2_RDO_WGTA_QP*] 1'h1: Select weight group B(VEPU2_RDO_WGTB_QP*)
4	RW	0x0	bs_scp Output start code prefix.
3	RW	0x0	mei_stor Output ME(motion estimation) information.
2	RW	0x0	cur_frm_ref Current frame should be referenced in future.
1	RW	0x0	roi_en ROI(region of interest) encoding enable.
0	RW	0x0	enc_stnd Video standard. 1'h0: H.264 encoding 1'h1: HEVC encoding

VEPU_ENC_WDG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rfp_load_thd Reference picture loading timeout threshold. 8'h0: No time limit 8'hx: x*256 core clock cycles

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	vs_load_thd Video source loading timeout threshold. 24'h0: No time limit 24'hx: x*256 core clock cycles

VEPU_DTRNS_MAP

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	afbc_bsize AFBC video source loading burst size. 1'h0: 32 bytes 1'h1: 64 bytes
26:23	RW	0x0	lktw_bus_edin Data swap for link table write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
22:19	RW	0x0	roir_bus_edin Data swap for ROI configuration read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
18:15	RW	0x0	lktr_bus_edin Data swap for link table read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits

Bit	Attr	Reset Value	Description
14:12	RW	0x0	bsw_bus_edin Data swap for bis stream write channel. [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
11:8	RW	0x0	meiw_bus_edin Data swap for ME information write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
7:4	RW	0x0	src_bus_edin Data swap for video source loading channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
3	RW	0x0	rfpw_bus_ordr Swap the position of 64 bits in 128 bits for reference picture.
2	RW	0x0	dspw_bus_ordr Swap the position of 64 bits in 128 bits for down-sampled picture.
1	RW	0x0	cmvw_bus_ordr Swap the position of 64 bits in 128 bits for co-located Mv(HEVC only).
0	RW	0x0	lpfw_bus_ordr Swap the position of 64 bits in 128 bits for loop-filter write-back data between tiles(HEVC only).

VEPU_DTRNS_CFG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	axi_brsp_cke AXI write response channel check enable. [7]: Lpf write response check enable. [6]: Reconstructed picture write response check enable. [5]: ME information write response check enable. [4]: CTU information write response check enable. [3]: Down-sampled picture write response check enable. [2]: Bit stream write response check enable. [1]: Link table mode write reponse check enable. [0]: Reserved for video preprocess.
15:8	RO	0x00	reserved
7	RW	0x0	dspr_otsd Down sampled reference picture read outstanding enable. 1'h0: No outstanding 1'h1: Outstanding read, which improves data transaction efficiency, but core clock frequency should not lower than bus clock frequency.
6:0	RO	0x00	reserved

VEPU_SRC_FMT

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	src_range Video source clip (low active). 1'h0: [16:235] for luma and [16:240] for chroma. 1'h1: [0:255] for both luma and chroma.

Bit	Attr	Reset Value	Description
5:2	RW	0x0	src_cfmt Video source color format. 4'h0: BGRA8888 4'h1: RGB888 4'h2: RGB565 4'h4: YUV422 SP 4'h5: YUV422 P 4'h6: YUV420 SP 4'h7:YUV420 P 4'h8: YUYV422 4'h9: UYVY422 4'ha: YUV400 Others: Reserved
1	RW	0x0	rbuv_swap Swap the position of R and B for BGRA8888, RGB888, RGB 656 format; Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format. 1'h0: RGB or YUYV or UYVY. 1'h1: BGR or YVYU or VYUY.
0	RW	0x0	alpha_swap Swap the position of alpha and RGB for ARBG8888. 1'h0: BGRA8888 or RGBA8888. 1'h1: ABGR8888 or ARGB8888.

VEPU_SRC_UDFY

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2y Weight of RED in RGB to Y conversion formula.
17:9	RW	0x000	csc_wgt_g2y Weight of GREEN in RGB to Y conversion formula.

Bit	Attr	Reset Value	Description
8:0	RW	0x000	csc_wgt_b2y Weight of BLUE in RGB to Y conversion formula.

VEPU_SRC_UDFU

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2u Weight of RED in RGB to U conversion formula.
17:9	RW	0x000	csc_wgt_g2u Weight of GREEN in RGB to U conversion formula.
8:0	RW	0x000	csc_wgt_b2u Weight of BLUE in RGB to U conversion formula.

VEPU_SRC_UDFV

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2v Weight of RED in RGB to V conversion formula.
17:9	RW	0x000	csc_wgt_g2v Weight of GREEN in RGB to V conversion formula.
8:0	RW	0x000	csc_wgt_b2v Weight of BLUE in RGB to V conversion formula.

VEPU_SRC_UDFO

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	csc_ofst_y Offset of RGB to Y conversion formula.

Bit	Attr	Reset Value	Description
15:8	RW	0x00	csc_ofst_u Offset of RGB to U conversion formula.
7:0	RW	0x00	csc_ofst_v Offset of RGB to V conversion formula.

VEPU_SRC_PROC

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	afbcd_en AFBC decompress enable (for AFBC format video source).
29	RW	0x0	txa_en Video source texture analysis enable.
28:27	RW	0x0	src_rot Video source rotation mode. 2'h0: 0 degree 2'h1: Clockwise 90 degree 2'h2: Clockwise 180 degree 2'h3: Clockwise 270 degree
26	RW	0x0	src_mirr Video source mirror mode enable.
25:0	RO	0x0000000	reserved

VEPU_SLI_CFG_H264

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sli_crs_en Slice cut cross lines enable, using for breaking the resolution limit, h264 only.
30:0	RO	0x00000000	reserved

VEPU_TILE_CFG_HEVC

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RW	0x0	tile_en Tile cut enable, hevc only.
30:22	RO	0x000	reserved
21:16	RW	0x00	tile_h_m1 The height of current tile minus 1, based on 64 pixel, hevc only.
15:6	RO	0x000	reserved
5:0	RW	0x00	tile_w_m1 The width of current tile minus 1, based on 64 pixel, hevc only.

VEPU_TILE_POS

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	tile_y The top-left point of current tile in the vertical dirction, based on 64 pixel, hevc only.
15:6	RO	0x000	reserved
5:0	RW	0x00	tile_x The top-left point of current tile in the horizontal dirction, based on 64 pixel, hevc only.

VEPU_KLUT_OFST

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	chrm_klut_ofst Offset of (RDO) chroma cost weight table, values from 0 to 6.

VEPU_KLUT_WGT0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt1_l9 Low 9 bits of data1 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt0 Data0 in chroma cost weight table.

VEPU_KLUT_WGT1

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt2 Data2 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt1_h9 High 9 bits of data1 in chroma cost weight table.

VEPU_KLUT_WGT2

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt4_l9 Low 9 bits of data4 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt3 Data3 in chroma cost weight table.

VEPU_KLUT_WGT3

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt5 Data5 in chroma cost weight table.
13:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x000	chrm_klut_wgt4_h9 High 9 bits of data4 in chroma cost weight table.

VEPU_KLUT_WGT4

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt7_l9 Low 9 bits of data7 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt6 Data6 in chroma cost weight table.

VEPU_KLUT_WGT5

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt8 Data8 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt7_h9 High 9 bits of data7 in chroma cost weight table.

VEPU_KLUT_WGT6

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt10_l9 Low 9 bits of data10 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt9 Data9 in chroma cost weight table.

VEPU_KLUT_WGT7

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt11 Data11 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt10_h9 High 9 bits of data10 in chroma cost weight table.

VEPU_KLUT_WGT8

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt13_l9 Low 9 bits of data13 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt12 Data12 in chroma cost weight table.

VEPU_KLUT_WGT9

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt14 Data14 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt13_h9 High 9 bits of data13 in chroma cost weight table.

VEPU_KLUT_WGT10

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt16_l9 Low 9 bits of data16 in chroma cost weight table.

Bit	Attr	Reset Value	Description
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt15 Data15 in chroma cost weight table.

VEPU_KLUT_WGT11

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt17 Data17 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt16_h9 High 9 bits of data16 in chroma cost weight table.

VEPU_KLUT_WGT12

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt19_l9 Low 9 bits of data19 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt18 Data18 in chroma cost weight table.

VEPU_KLUT_WGT13

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt20 Data20 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt19_h9 High 9 bits of data19 in chroma cost weight table.

VEPU_KLUT_WGT14

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt22_l9 Low 9 bits of data22 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt21 Data21 in chroma cost weight table.

VEPU_KLUT_WGT15

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt23 Data23 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt22_h9 High 9 bits of data22 in chroma cost weight table.

VEPU_KLUT_WGT16

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt25_l9 Low 9 bits of data25 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt24 Data24 in chroma cost weight table.

VEPU_KLUT_WGT17

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt26 Data26 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt25_h9 High 9 bits of data25 in chroma cost weight table.

VEPU_KLUT_WGT18

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt28_l9 Low 9 bits of data28 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt27 Data27 in chroma cost weight table.

VEPU_KLUT_WGT19

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt29 Data29 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt28_h9 High 9 bits of data28 in chroma cost weight table.

VEPU_KLUT_WGT20

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt31_l9 Low 9 bits of data31 in chroma cost weight table.
22:18	RO	0x00	reserved

Bit	Attr	Reset Value	Description
17:0	RW	0x00000	chrm_klut_wgt30 Data30 in chroma cost weight table.

VEPU_KLUT_WGT21

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	chrm_klut_wgt32 Data32 in chroma cost weight table.
13:9	RO	0x00	reserved
8:0	RW	0x000	chrm_klut_wgt31_h9 High 9 bits of data31 in chroma cost weight table.

VEPU_KLUT_WGT22

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	chrm_klut_wgt34_l9 Low 9 bits of data34 in chroma cost weight table.
22:18	RO	0x00	reserved
17:0	RW	0x00000	chrm_klut_wgt33 Data33 in chroma cost weight table.

VEPU_KLUT_WGT23

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	chrm_klut_wgt34_h9 High 9 bits of data34 in chroma cost weight table.

VEPU_RC_CFG

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rc_ctu_num RC adjustment intervals, base on CTU number.
15:3	RO	0x0000	reserved
2	RW	0x0	aq_mode Mode of aq_delta calculation for CU32 and CU64. 1'b0: aq_delta of CU32/CU64 is calculated by corresponding MADI32/64; 1'b1: aq_delta of CU32/CU64 is calculated by corresponding 4/16 CU16 qp_deltas.
1	RW	0x0	aq_en Adaptive quantization enable.
0	RW	0x0	rc_en Rate control enable.

VEPU_RC_QP

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	rc_min_qp Min QP for rate control and AQ mode.
25:20	RW	0x00	rc_max_qp Max QP for rate control and AQ mode.
19:16	RW	0x0	rc_qp_range QP adjust range(delta_qp) in rate control. Delta_qp is constrained between -rc_qp_range to rc_qp_range.
15:0	RO	0x0000	reserved

VEPU_RC_TGT

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	ctu_ebit Target bit num for one 64x64 CTU(for HEVC) or one 16x16 MB(for H.264), with 1/16 precision.

VEPU_RC_ADJ0

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x00	qp_adj4 QP adjust step4 for rate control.
19:15	RW	0x00	qp_adj3 QP adjust step3 for rate control.
14:10	RW	0x00	qp_adj2 QP adjust step2 for rate control.
9:5	RW	0x00	qp_adj1 QP adjust step1 for rate control.
4:0	RW	0x00	qp_adj0 QP adjust step0 for rate control.

VEPU_RC_ADJ1

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	qp_adj8 QP adjust step8 for rate control.
14:10	RW	0x00	qp_adj7 QP adjust step7 for rate control.
9:5	RW	0x00	qp_adj6 QP adjust step6 for rate control.
4:0	RW	0x00	qp_adj5 QP adjust step5 for rate control.

VEPU_RC_DTHD0

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd0 Bits rate deviation threshold0.

VEPU_RC_DTHD1

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd1 Bits rate deviation threshold1.

VEPU_RC_DTHD2

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd2 Bits rate deviation threshold2.

VEPU_RC_DTHD3

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd3 Bits rate deviation threshold3.

VEPU_RC_DTHD4

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd4 Bits rate deviation threshold4.

VEPU_RC_DTHD5

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd5 Bits rate deviation threshold5.

VEPU_RC_DTHD6

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd6 Bits rate deviation threshold6.

VEPU_RC_DTHD7

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd7 Bits rate deviation threshold7.

VEPU_RC_DTHD8

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd8 Bits rate deviation threshold8.

VEPU_ROI_QTHD0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area2 Min QP for 16x16 CU inside ROI area2.
23:18	RW	0x00	qpmax_area1 Max QP for 16x16 CU inside ROI area1.
17:12	RW	0x00	qpmin_area1 Min QP for 16x16 CU inside ROI area1.

Bit	Attr	Reset Value	Description
11:6	RW	0x00	qpmax_area0 Max QP for 16x16 CU inside ROI area0.
5:0	RW	0x00	qpmin_area0 Min QP for 16x16 CU inside ROI area0.

VEPU_ROI_QTHD1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmax_area4 Max QP for 16x16 CU inside ROI area4.
23:18	RW	0x00	qpmin_area4 Min QP for 16x16 CU inside ROI area4.
17:12	RW	0x00	qpmax_area3 Max QP for 16x16 CU inside ROI area3.
11:6	RW	0x00	qpmin_area3 Min QP for 16x16 CU inside ROI area3.
5:0	RW	0x00	qpmax_area2 Max QP for 16x16 CU inside ROI area2.

VEPU_ROI_QTHD2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area7 Min QP for 16x16 CU inside ROI area7.
23:18	RW	0x00	qpmax_area6 Max QP for 16x16 CU inside ROI area6.
17:12	RW	0x00	qpmin_area6 Min QP for 16x16 CU inside ROI area6.
11:6	RW	0x00	qpmax_area5 Max QP for 16x16 CU inside ROI area5.

Bit	Attr	Reset Value	Description
5:0	RW	0x00	qpmin_area5 Min QP for 16x16 CU inside ROI area5.

VEPU_ROI_QTHD3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	qpmap_mode QP theshold generation for the CUs whose size is bigger than 16x16. 2'h0: Mean value of 16x16 CU QP thesholds 2'h1: Max value of 16x16 CU QP thesholds 2'h2: Min value of 16x16 CU QP thesholds 2'h3: Reserved
29:6	RO	0x000000	reserved
5:0	RW	0x00	qpmax_area7 Max QP for 16x16 CU inside ROI area7.

VEPU_PIC_OFST

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pic_ofst_x Horizontal offset for encoding picture.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pic_ofst_y Vertical offset for encoding picture.

VEPU_SRC_STRD

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_strd1 CHROMA stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar.
15:0	RW	0x0000	src_strd0 Video source stride0, based on pixel (byte). Note that if the video format is YUYV/UYVY/RGB/ARGB, src_strd0 is the only one component stride, if the video format is YUV420P/YUV420SP/YUV422P/YUV422SP, src_strd0 is the LUMA component stride. Note that if the video source is compressed by AFBC, src_strd0 is the header stride and it is 16-byte aligned.

VEPU_ADR_SRC0

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src0 Base address of the 1st storage area for video source, based on byte. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src0 is configured as the base address of video source frame buffer. YUV422/420 semi-planar have 2 storage area, while adr_src0 is configured as the base address of Y frame buffer. YUV422/420 planar have 3 storage area, while adr_src0 is configured as the base address of Y frame buffer. Note that if the video source is compressed by AFBC, adr_src0 is configured as the base address of header buffer, and it is 16-byte aligned.

VEPU_ADR_SRC1

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src1 Base address of the 2nd storage area for video source. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src1 is reserved. YUV422/420 semi-planar have 2 storage area, while adr_src1 is configured as the base address of CHROMA frame buffer. YUV422/420 planar have 3 storage area, while adr_src1 is configured as the base address of U frame buffer. Note that if the video source is compressed by AFBC, adr_src1 is configured as the base address of body buffer.

VEPU_ADR_SRC2

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src2 Base address of V frame buffer when video source is uncompress and color format is YUV422/420 planar.

VEPU_ADR_ROI

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	roi_addr High 28 bits of base address for ROI configuration.
3:0	RO	0x0	reserved

VEPU_ADR_RFPW_H

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpw_h_addr High 20 bits of the header_block base address for compressed reference frame write.
11:0	RO	0x000	reserved

VEPU_ADR_RFPW_B

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpw_b_addr High 20 bits of the body_block base address for compressed reference frame write.
11:0	RO	0x000	reserved

VEPU_ADR_RFPR_H

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpr_h_addr High 20 bits of the header_block base address for compressed reference frame read.
11:0	RO	0x000	reserved

VEPU_ADR_RFPR_B

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rfpr_b_addr High 20 bits of the body_block base address for compressed reference frame read.
11:0	RO	0x000	reserved

VEPU_ADR_CMVW

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	cmvw_addr High 22 bits of base address for col-located Mv write, HEVC only.
9:0	RO	0x000	reserved

VEPU_ADR_CMVR

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	cmvr_addr High 22 bits of base address for col-located Mv read, HEVC only.
9:0	RO	0x000	reserved

VEPU_ADR_DSPW

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	dspw_addr High 22 bits of base address for down-sampled reference frame write.
9:0	RO	0x000	reserved

VEPU_ADR_DSPR

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	dspr_addr High 22 bits of base address for down-sampled reference frame read.
9:0	RO	0x000	reserved

VEPU_ADR_MEIW

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	meiw_addr High 22 bits of base address for ME information write.
9:0	RO	0x000	reserved

VEPU_ADR_BSBT

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbt_addr High 25 bits of the top address of bit stream buffer.
6:0	RO	0x00	reserved

VEPU_ADR_BSBB

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbb_addr High 25 bits of the bottom address of bit stream buffer.
6:0	RO	0x00	reserved

VEPU_ADR_BSBR

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	bsbr_addr Read address of bit stream buffer, 128B aligned. VEPU will pause when write address meets read address and then send an interrupt. SW should move some data out from bit stream buffer and change this register accordingly. After that VEPU will continue processing automatically.
6:0	RO	0x00	reserved

VEPU_ADR_BSBS

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_bsbs Start address of bit stream buffer. VEPU begins to write bit stream from this address and increase address automatically. Note that the VEPU's real-time write address is marked in BSB_STUS.

VEPU_SLI_SPLT

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sli_splt_cnum_m1 Number of CTU/MB for slice split. Valid when slice is splited by CTU/MB.
15:14	RO	0x0	reserved
13	RW	0x0	sli_flsh Slice flush. Flush all the bit stream after each slice finished.
12:3	RW	0x000	sli_max_num_m1 Max slice num in one frame.
2	RW	0x0	sli_splt_cpst Slice split compensation when slice is splited by byte. Byte distortion of current slice will be compensated in the next slice.
1	RW	0x0	sli_splt_mode Slice split mode. 1'h0: Slice splited by byte. 1'h1: Slice splited by number of MB(H.264)/CTU(HEVC).
0	RW	0x0	sli_splt Slice split enable.

VEPU_SLI_BYTE

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sli_splt_byte Byte number for each slice when slice is splited by byte.

VEPU_ME_RNGE

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_frm_num Frame number difference value between current and reference frame, HEVC only.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:11	RW	0x0	rme_srch_v RME vertical search range, values from 4 to 5.
10:8	RW	0x0	rme_srch_h RME horizontal search range, values from 3 to 7.
7:4	RW	0x0	cme_srch_v CME vertical search range, base on 16 pixel.
3:0	RW	0x0	cme_srch_h CME horizontal search range, base on 16 pixels.

VEPU_ME_CFG

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	fme_dis [4]: Disable 64x64 block FME. [3]: Disable 32x32 block FME. [2]: Disable 16x16 block FME. [1]: Disable 8x8 block FME. [0]: Disable 4x4 block FME.
26:22	RW	0x00	rme_dis [4]: Disable 64x64 block RME. [3]: Disable 32x32 block RME. [2]: Disable 16x16 block RME. [1]: Disable 8x8 block RME. [0]: Disable 4x4 block RME.
21	RW	0x0	colmv_load Load co-located Mvs as predicated Mv candidates, HEVC only.
20	RW	0x0	colmv_stor Store col-Mv information to external memory, HEVC only.
19:18	RW	0x2	pmv_num PMV number (should be constant2).

Bit	Attr	Reset Value	Description
17:16	RW	0x1	mv_llmt Motion vector limit (by level), H.264 only. 2'h0: Mvy is limited to [-64,63]. Others: Mvy is limited to [-128,127].
15:8	RW	0x05	pmv_mdst_v Min vertical distance for PMV selection.
7:0	RW	0x05	pmv_mdst_h Min horizontal distance for PMV selection.

VEPU_ME_CACH

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:18	RW	0x00	cme_linebuf_w The width of CIME down-sample recon data linebuf, based on 64 pixel.
17:16	RW	0x0	cach_l2_map L2 cach mapping, base on pixels. 2'h0: 32x512 2'h1: 16x1024 2'h2: 8x2048 2'h3: 4x4096 To get better performance, the recommended configuration is as follow: 1) When picture width <= 3072, cach_l2_map = 1; 2) When picture width > 3072, cach_l2_map = 3;
15:11	RW	0x00	cme_rama_h Height of CME RAMA district, base on 4 pixels.
10:0	RW	0x000	cme_rama_max CME's max RAM address.

VEPU_SYNT_LONG_REFM0

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	poc_lsb_lt2 Poc_lsb_lt[2]
15:0	RW	0x0000	poc_lsb_lt1 Poc_lsb_lt[1]

VEPU_SYNT_LONG_REFM1

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_msb_cycl2 Delta_poc_msb_cycle_lt[2]
15:0	RW	0x0000	dlt_poc_msb_cycl1 Delta_poc_msb_cycle_lt[1]

VEPU_OSD_INV_CFG

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd_ch_inv_msk OSD color inverse expression switch for chroma component, each bit controls corresponding region. 1'h0: Expression need to determine the condition; 1'h1: Expression don't need to determine the condition;
23:16	RW	0x00	osd_lu_inv_msk OSD color inverse expression switch for luma component, each bit controls corresponding region. 1'h0: Expression need to determine the condition; 1'h1: Expression don't need to determine the condition;
15:8	RW	0x00	osd_itype OSD color inverse expression type, each bit controls corresponding region. 1'h0: AND; 1'h1: OR;
7:0	RW	0x00	osd_ch_inv_en OSD color inverse enable of chroma component, each bit controls corresponding region.

VEPU_ADR_LPFW

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	lpfw_addr High 22 bits of base address for loop-filter write-back data between tiles, hevc only.
9:0	RO	0x000	reserved

VEPU_ADR_LPFR

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	lpfr_addr High 22 bits of base address for loop-filter read data between tiles, hevc only.
9:0	RO	0x000	reserved

VEPU_IPRD_CSTS

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vthd_c CHROMA variance threshold to select intra prediction cost function.
15:12	RO	0x0	reserved
11:0	RW	0x000	vthd_y LUMA variance threshold to select intra prediction cost function.

VEPU_RDO_CFG_H264

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31	RW	0x0	satd_byps_flg Rdo cost caculation expression for intra by using sad or satd. 1'h0: SATD; 1'h1: SAD;
30:22	RO	0x000	reserved
21:20	RW	0x0	scl_lst_sel Scale list selection. 2'h0: Flat scale list. 2'h1: Default scale list. 2'h2: User defined. 2'h3: Reserved.
19	RW	0x0	atf_intra_e Intra mode anti-flicker enable.
18	RW	0x0	atf_lvl_e Block level anti-flicker enable.
17:16	RW	0x0	atf_edg Edge of anti-flicker, base on MB. the MBs inside edge should not influenced.
15	RW	0x0	atr_e Anti-ring enable.
14	RO	0x0	reserved
13	RW	0x0	ccwa_e Chroma cost weight adjustment(KLUT) enable.
12:5	RW	0x00	rdo_mask [7]: Disable intra4x4. [6]: Disable intra8x8. [5]: Disable intra16x16. [4]: Disable inter8x8 with T4. [3]: Disable inter8x8 with T8. [2]: Disable inter16x16 with T4. [1]: Disable inter16x16 with T8. [0]: Disable skip mode.

Bit	Attr	Reset Value	Description
4	RW	0x0	chrm_spcl Chroma special candidates enable.
3	RW	0x0	vlc_lmt CAVLC syntax limit.
2	RW	0x0	arb_sel Reserved
1	RW	0x0	inter_4x4 4x4 sub MB enable.
0	RW	0x0	rect_size Limit sub_mb_rect_size for low level.

VEPU_RDO_CFG_HEVC

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31	RW	0x0	satd_byps_flg Rdo cost caculation expression for intra by using sad or satd. 1'h0: SATD; 1'h1: SAD;
30:26	RO	0x00	reserved
25:24	RW	0x0	scl_lst_sel Scale list selection. 2'h0: Flat scale list. 2'h1: Default scale list. 2'h2: User defined. 2'h3: Reserved.
23	RW	0x0	ccwa_e Chroma cost weight adjustment(KLUT) enable.
22:19	RW	0x0	cu_intra_e [3]: Intra 32x32 mode enable. [2]: Intra 16x16 mode enable. [1]: Intra 8x8 mode enable. [0]: Intra 4x4 mode enable.

Bit	Attr	Reset Value	Description
18:10	RO	0x000	reserved
9:6	RW	0x0	cu_inter_e [3]: 64x64 inter mode enable. [2]: 32x32 inter mode enable. [1]: 16x16 inter mode enable. [0]: 8x8 inter mode enable.
5:4	RO	0x0	reserved
3	RW	0x0	rdoq_e Reserved
2	RW	0x0	chrm_spcl 4 special chroma candidates enable.
1	RW	0x0	ltm_idx0l0 The 1st reference frame in ref-list0 is long term.
0	RW	0x0	ltm_col Co-located picture is long term reference frame.

VEPU_SYNT_NAL_H264

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RW	0x00	nal_unit_type nal_unit_type
1:0	RW	0x0	nal_ref_idc nal_ref_idc

VEPU_SYNT_NAL_HEVC

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	nal_unit_type nal_unit_type

VEPU_SYNT_SPS_H264

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:5	RW	0x0	mpoc_lm4 log2_max_pic_order_cnt_lsb_minus4
4	RW	0x0	drct_8x8 direct_8x8_inference_flag
3:0	RW	0x0	max_fnum log2_max_frame_num_minus4

VEPU_SYNT_SPS_HEVC

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	strg_intra_smth strong_intra_smoothing_enabled_flag
19:16	RW	0x0	log2_max_poc_lsb log2_max_pic_order_cnt_lsb_minus4
15	RW	0x0	tmpl_mvp_e sps_temporal_mvp_enabled_flag
14:9	RW	0x00	num_lt_ref_pic num_long_term_ref_pics_sps
8	RW	0x0	lt_ref_pic_prsnt long_term_ref_pics_present_flag
7:1	RW	0x00	num_st_ref_pic num_short_term_ref_pic_sets
0	RW	0x0	smpl_adpt_ofst_e sample_adaptive_offset_enabled_flag

VEPU_SYNT_PPS_H264

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	dbf_cp_flg deblocking_filter_control_present_flag
23	RW	0x0	wght_pred weight_pred_flag
22:18	RW	0x00	cr_ofst second_chroma_qp_index_offset
17:13	RW	0x00	cb_ofst chroma_qp_index_offset
12:7	RW	0x00	pic_init_qp pic_init_qp_minus26 + 26
6:5	RW	0x0	num_ref1_idx num_ref_idx_l1_active_minus1
4:3	RW	0x0	num_ref0_idx num_ref_idx_l0_active_minus1
2	RW	0x0	csip_flag constrained_intra_pred_flag
1	RW	0x0	trns_8x8 transform_8x8_mode_flag
0	RW	0x0	etpy_mode entropy_coding_mode_flag

VEPU_SYNT_PPS_HEVC

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	lp_fltr_acrs_til loop_filter_across_tiles_enabled_flag
20:19	RW	0x0	cu_qp_dlt_depth diff_cu_qp_delta_depth
18	RW	0x0	sli_seg_hdr_extn slice_segment_header_extension_present_flag

Bit	Attr	Reset Value	Description
17	RW	0x0	lst_mdfy_prsnt_flg lists_modification_present_flag
16	RW	0x0	dblk_fltr_ovrd_e deblocking_filter_override_enabled_flag
15	RW	0x0	lp_fltr_acrs_sli pps_loop_filter_across_slices_enabled_flag
14	RW	0x0	chrm_qp_ofst_prsnt pps_slice_chroma_qp_offsets_present_flag. VEPU only supports PPS level chroma QP adjustmentso this field shoud be configured to 0.
13	RW	0x0	cu_qp_dlt_en cu_qp_delta_enabled_flag
12:7	RW	0x00	pic_init_qp init_qp_minus26+26
6	RW	0x0	cbc_init_prsnt_flag cabac_init_present_flag
5	RW	0x0	sgn_dat_hid_e sign_data_hiding_enabled_flag
4:2	RW	0x0	num_extr_sli_hdr num_extra_slice_header_bits
1	RW	0x0	out_flg_prsnt_flg output_flag_present_flag
0	RW	0x0	dpdnt_sli_seg_en dependent_slice_segments_enable_flag

VEPU_SYNT_SLI0_H264

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	frm_num frame_num
15:14	RO	0x0	reserved
13:12	RW	0x0	cbc_init_idc cabac_init_idc

Bit	Attr	Reset Value	Description
11	RW	0x0	num_ref_ovrd num_ref_idx_active_override_flag
10	RW	0x0	drct_smvp direct_spatial_mv_pred_flag
9:2	RW	0x00	pps_id pic_parameter_set_id
1:0	RW	0x0	sli_type slice_type: 0->P, 1->B, 2->I.

VEPU_SYNT_SLI0_HEVC

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RW	0x0	no_out_pri_pic no_output_of_prior_pics_flag
30:25	RW	0x00	sli_pps_id slice_pic_parameter_set_id
24	RW	0x0	dpdnt_sli_seg_flg dependent_slice_segment_flag
23:17	RW	0x00	sli_rsrv_flg slice_served_flag
16:15	RW	0x0	sli_type slice_type: 0->B, 1->P, 2->I.
14	RW	0x0	pic_out_flg pic_output_flag
13	RW	0x0	sli_tmprl_mvp_e slice_temporal_mvp_enabled_flag
12	RW	0x0	sli_sao_luma_flg slice_sao_luma_flag
11	RW	0x0	sli_sao_chrm_flg slice_sao_chroma_flag
10	RW	0x0	num_refidx_act_ovrd num_ref_idx_active_override_flag

Bit	Attr	Reset Value	Description
9:8	RW	0x0	num_refidx_l0_act num_ref_idx_l0_active_minus1
7:6	RW	0x0	num_refidx_l1_act num_ref_idx_l1_active_minus1
5	RW	0x0	ref_pic_lst_mdf_l0 ref_pic_list_modification_flag_l0
4	RO	0x0	reserved
3	RW	0x0	mrg_lft_flg sao_merge_left_flag
2	RW	0x0	mrg_up_flg sao_merge_up_flag
1	RW	0x0	mvd_l1_zero_flg mvd_l1_zero_flag
0	RW	0x0	cbc_init_flg cabac_init_flag

VEPU_SYNT_SLI1_H264

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	poc_lsb pic_order_cnt_lsb
15:0	RW	0x0000	idr_pid idr_pic_id

VEPU_SYNT_SLI1_HEVC

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	lst_entry_l0 list_entry_l0
26	RW	0x0	col_frm_l0_flg collocated_from_l0_flag

Bit	Attr	Reset Value	Description
25	RW	0x0	col_ref_idx collocated_ref_idx
24	RO	0x0	reserved
23:22	RW	0x0	max_mrg_cnd 5 - five_minus_max_num_merge_cand, values from 0 to 3
21:16	RW	0x00	sli_qp slice_qp
15:11	RW	0x00	sli_cb_qp_ofst Actually this field should be configured as pps_cb_qp_offset.
10	RW	0x0	dblk_fltr_ovrd_flg deblocking_filter_override_flag
9	RW	0x0	sp_dblk_fltr_dis slice/pps_deblocking_filter_disabled_flag. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_deblocking_filter_disabled_flag. Otherwise it is pps_deblocking_filter_disabled_flag.
8	RW	0x0	sli_lp_fltr_acrs_sli slice_loop_filter_across_slices_enabled_flag
7:4	RW	0x0	sp_beta_ofst_div2 slice/pps_beta_offset_div2. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_beta_offset_div2. Otherwise it is pps_beta_offset_div2.
3:0	RW	0x0	sp_tc_ofst_div2 slice/pps_tc_offset_div2. If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_tc_offset_div2. Otherwise it is pps_tc_offset_div2.

VEPU_SYNT_SLI2_H264

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rodr_pic_num abs_diff_pic_num_minus1/long_term_pic_num
15:13	RO	0x0	reserved
12:11	RW	0x0	dis_dblk_idc disable_deblocking_filter_idc
10:7	RW	0x0	sli_alph_ofst slice_alpha_c0_offset_div2
6:3	RW	0x0	sli_beta_ofst slice_beta_offset_div2
2	RW	0x0	ref_list0_rodr ref_pic_list_reordering_flag_l0
1:0	RW	0x0	rodr_pic_idx reordering_of_pic_nums_idc

VEPU_SYNT_SLI2_HEVC

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sli_hdr_ext_len slice_segment_header_extension_length
15:0	RW	0x0000	sli_poc_lsb slice_pic_order_cnt_lsb

VEPU_SYNT_REFM0_H264

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:26	RW	0x0	mmco_type2 memory_management_control_operation[2]
25:23	RW	0x0	mmco_type1 memory_management_control_operation[1]

Bit	Attr	Reset Value	Description
22:7	RW	0x0000	mmco_parm0 MMCO parameters which have different meanings according to different mmco_parm0 valus. difference_of_pic_nums_minus1 for mmco_parm0 equals 0 or 3. long_term_pic_num for mmco_parm0 equals 2. long_term_frame_idx for mmco_parm0 equals 6. max_long_term_frame_idx_plus1 for mmco_parm0 equals 4.
6:4	RW	0x0	mmco_type0 memory_management_control_operation
3	RW	0x0	mmco4_pre A No.4 MMCO should be executed firstly if mmo4_pre is 1
2	RW	0x0	arpm_flg adaptive_ref_pic_marking_mode_flag
1	RW	0x0	ltrf_flg long_term_reference_flag
0	RW	0x0	nopp_flg no_output_of_prior_pics_flag

VEPU_SYNT_REFM0_HEVC

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	num_lt_sps num_long_term_sps
29:24	RW	0x00	st_ref_pic_idx short_term_ref_pic_set_idx
23:22	RW	0x0	num_lt_pic num_long_term_pics
21:17	RW	0x00	lt_idx_sps lt_idx_sps
16:1	RW	0x0000	poc_lsb_lt0 poc_lsb_lt[0]
0	RW	0x0	st_ref_pic_flg short_term_ref_pic_set_sps_flag

VEPU_SYNT_REFM1_H264

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mmco_parm2 MMCO parameters which have different meanings according to different mmco_parm2 valus. difference_of_pic_nums_minus1 for mmco_parm2 equals 0 or 3. long_term_pic_num for mmco_parm2 equals 2. long_term_frame_idx for mmco_parm2 equals 6. max_long_term_frame_idx_plus1 for mmco_parm2 equals 4.
15:0	RW	0x0000	mmco_parm1 MMCO parameters which have different meanings according to different mmco_parm1 valus. difference_of_pic_nums_minus1 for mmco_parm1 equals 0 or 3. long_term_pic_num for mmco_parm1 equals 2. long_term_frame_idx for mmco_parm1 equals 6. max_long_term_frame_idx_plus1 for mmco_parm1 equals 4.

VEPU_SYNT_REFM1_HEVC

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	used_by_lt_flg2 used_by_curr_pic_lt_flag[2]
30	RW	0x0	used_by_lt_flg1 used_by_curr_pic_lt_flag[1]
29	RW	0x0	used_by_lt_flg0 used_by_curr_pic_lt_flag[0]
28	RW	0x0	dlt_poc_msb_prsnt2 delta_poc_msb_present_flag[2]
27	RW	0x0	dlt_poc_msb_prsnt1 delta_poc_msb_present_flag[1]
26	RW	0x0	dlt_poc_msb_prsnt0 delta_poc_msb_present_flag[0]

Bit	Attr	Reset Value	Description
25:10	RW	0x0000	dlt_poc_msb_cycl0 delta_poc_msb_cycle_lt[0]
9:5	RW	0x00	num_negative_pics num_neg_pic
4	RW	0x0	num_pos_pic num_positive_pics
3:0	RW	0x0	used_by_s0_flg used_by_curr_pic_s0_flag

VEPU_OSD_CFG

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	osd_plt_typ OSD palette type. 1'h1: Default type. 1'h0: User defined type.
16	RW	0x0	osd_plt_cks OSD palette clock selection. 1'h0: Configure bus clock domain. 1'h1: Core clock domain.
15:8	RW	0x00	osd_lu_inv_en OSD color inverse enable of luma component, each bit controls corresponding region.
7:0	RW	0x00	osd_en OSD region enable, each bit controls corresponding OSD region.

VEPU_OSD_INV

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	osd_ithd_r7 Color inverse theshold for OSD region7.

Bit	Attr	Reset Value	Description
27:24	RW	0x0	osd_ithd_r6 Color inverse theshold for OSD region6.
23:20	RW	0x0	osd_ithd_r5 Color inverse theshold for OSD region5.
19:16	RW	0x0	osd_ithd_r4 Color inverse theshold for OSD region4.
15:12	RW	0x0	osd_ithd_r3 Color inverse theshold for OSD region3.
11:8	RW	0x0	osd_ithd_r2 Color inverse theshold for OSD region2.
7:4	RW	0x0	osd_ithd_r1 Color inverse theshold for OSD region1.
3:0	RW	0x0	osd_ithd_r0 Color inverse theshold for OSD region0.

VEPU_SYNT_REFM2

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_s0_m11 delta_poc_s0_minus1[1]
15:0	RW	0x0000	dlt_poc_s0_m10 delta_poc_s0_minus1[0]

VEPU_SYNT_REFM2_H264

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	long_term_frame_idx2 long_term_frame_idx[2] (when mmco equal 3)
7:4	RW	0x0	long_term_frame_idx1 long_term_frame_idx[1] (when mmco equal 3)

Bit	Attr	Reset Value	Description
3:0	RW	0x0	long_term_frame_idx0 long_term_frame_idx[0] (when mmco equal 3)

VEPU_SYNT_REFM3

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_poc_s0_m13 delta_poc_s0_minus1[3]
15:0	RW	0x0000	dlt_poc_s0_m12 delta_poc_s0_minus1[2]

VEPU_OSD0_POS

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd0_rb_y Y coordinate/16 of OSD region0's right-bottom point.
23:16	RW	0x00	osd0_rb_x X coordinate/16 of OSD region0's right-bottom point.
15:8	RW	0x00	osd0_lt_y Y coordinate/16 of OSD region0's left-top point.
7:0	RW	0x00	osd0_lt_x X coordinate/16 of OSD region0's left-top point.

VEPU_OSD1_POS

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd1_rb_y Y coordinate/16 of OSD region1's right-bottom point.
23:16	RW	0x00	osd1_rb_x X coordinate/16 of OSD region1's right-bottom point.
15:8	RW	0x00	osd1_lt_y Y coordinate/16 of OSD region1's left-top point.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	osd1_lt_x X coordinate/16 of OSD region1's left-top point.

VEPU_OSD2_POS

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd2_rb_y Y coordinate/16 of OSD region2's right-bottom point.
23:16	RW	0x00	osd2_rb_x X coordinate/16 of OSD region2's right-bottom point.
15:8	RW	0x00	osd2_lt_y Y coordinate/16 of OSD region2's left-top point.
7:0	RW	0x00	osd2_lt_x X coordinate/16 of OSD region2's left-top point.

VEPU_OSD3_POS

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd3_rb_y Y coordinate/16 of OSD region3's right-bottom point.
23:16	RW	0x00	osd3_rb_x X coordinate/16 of OSD region3's right-bottom point.
15:8	RW	0x00	osd3_lt_y Y coordinate/16 of OSD region3's left-top point.
7:0	RW	0x00	osd3_lt_x X coordinate/16 of OSD region3's left-top point.

VEPU_OSD4_POS

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd4_rb_y Y coordinate/16 of OSD region4's right-bottom point.

Bit	Attr	Reset Value	Description
23:16	RW	0x00	osd4_rb_x X coordinate/16 of OSD region4's right-bottom point.
15:8	RO	0x00	reserved
7:0	RW	0x00	osd4_lt_x X coordinate/16 of OSD region4's left-top point.

VEPU_OSD5_POS

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd5_rb_y Y coordinate/16 of OSD region5's right-bottom point.
23:16	RW	0x00	osd5_rb_x X coordinate/16 of OSD region5's right-bottom point.
15:8	RW	0x00	osd5_lt_y Y coordinate/16 of OSD region5's left-top point.
7:0	RW	0x00	osd5_lt_x X coordinate/16 of OSD region5's left-top point.

VEPU_OSD6_POS

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd6_rb_y Y coordinate/16 of OSD region6's right-bottom point.
23:16	RW	0x00	osd6_rb_x X coordinate/16 of OSD region6's right-bottom point.
15:8	RW	0x00	osd6_lt_y Y coordinate/16 of OSD region6's left-top point.
7:0	RW	0x00	osd6_lt_x X coordinate/16 of OSD region6's left-top point.

VEPU_OSD7_POS

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	osd7_rb_y Y coordinate/16 of OSD region7's right-bottom point.
23:16	RW	0x00	osd7_rb_x X coordinate/16 of OSD region7's right-bottom point.
15:8	RW	0x00	osd7_lt_y Y coordinate/16 of OSD region7's left-top point.
7:0	RW	0x00	osd7_lt_x X coordinate/16 of OSD region7's left-top point.

VEPU_ADR_OSD0

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd0_addr High 28 bits of base address for OSD region0, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD1

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd1_addr High 28 bits of base address for OSD region1, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD2

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd2_addr High 28 bits of base address for OSD region2, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD3

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd3_addr High 28 bits of base address for OSD region3, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD4

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd4_addr High 28 bits of base address for OSD region4, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD5

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd5_addr High 28 bits of base address for OSD region5, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD6

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd6_addr High 28 bits of base address for OSD region6, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ADR_OSD7

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	osd7_addr High 28 bits of base address for OSD region7, based on 16byte.
3:0	RO	0x0	reserved

VEPU_ST_BSL

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RO	0x0000000	bs_lgth Bit stream length for current frame.

VEPU_ST_SSE_L32

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sse_l32 Low 32 bits of encoding distortion (SSE).

VEPU_ST_SSE_QP

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	sse_h8 High bits of encoding distortion(SSE).
23:22	RO	0x0	reserved
21:0	RO	0x000000	qp_sum Sum of QP for the encoded frame.

VEPU_ST_SAO

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:12	RO	0x000	sao_ynum Number of CTUs whose LUMA component are adjusted by SAO.
11:0	RO	0x000	sao_cnum Number of CTUs whose CHROMA component are adjusted by SAO.

VEPU_ST_HEAD_BL

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rdo_head_bits Total bit length of RDO HeaderBits.

VEPU_ST_RES_BL

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rdo_res_bits Total bit length of RDO ResidualBits.

VEPU_ST_ENC

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	st_sclr Status of safe clear. 1'h0: Safe clear is finished or not started. 1'h1: VEPU is performing safe clear.
1:0	RO	0x0	st_enc VEPU working status. 2'h0: Idle. 2'h1: Working in register conifguration mode. 2'h2: Working in link table configuration mode.

VEPU_ST_LKT

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	fnum_int Number of frames has been encoded since link table mode started, updated only when corresponding link table node send interrupt (VEPU_ENC_PIC_node_int==1).
15:8	RO	0x00	fnum_cfg Number of frames has been configured since link table mode started.
7:0	RO	0x00	fnum_enc Number of frames has been encoded since link table mode started.

VEPU_ST_NADR

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	node_addr High 28 bits of the address for the processing linke table node.
3:0	RO	0x0	reserved

VEPU_ST_BSB

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bsbw_addr High 28 bits of bit stream buffer write address.
3:0	RO	0x0	reserved

VEPU_ST_BUS

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RO	0x00	axir_err AXI read error. [6]: LPF read data between tiles(AXI0_ARID==9) [5]: ROI configuration (AXI0_ARID==7) [4]: Down-sampled picture (AXI0_ARID==6) [3]: Co-located Mv (AXI0_ARID==5) [2]: Link table (AXI0_ARID==4) [1]: Reference picture (AXI0_ARID==1,2,3,8) [0]: Video source load (AXI1)
23:16	RO	0x00	axib_err AXI write response error. [7]: LPF write-back data between tiles channel(AXI0_WID==6) [6]: Reconstructed picture channel (AXI0_WID==5) [5]: ME information channel (AXI0_WID==4) [4]: Co-located Mv channel (AXI0_WID==3) [3]: Down-sampled picture channel (AXI0_WID==2) [2]: Bit stream channel (AXI0_WID==1) [1]: Link table node channel (AXI0_WID==0) [0]: Reserved
15:8	RO	0x00	axib_ovfl AXI write response outstanding overflow. [7]: LPF write-back data between tiles channel(AXI0_WID==6) [6]: Reconstructed picture channel (AXI0_WID==5) [5]: ME information channel (AXI0_WID==4) [4]: Co-located Mv channel (AXI0_WID==3) [3]: Down-sampled picture channel (AXI0_WID==2) [2]: Bit stream channel (AXI0_WID==1) [1]: Link table node channel (AXI0_WID==0) [0]: Reserved.

Bit	Attr	Reset Value	Description
7:0	RO	0x00	axib_idl AXI write response idle. [7]: LPF write-back data between tiles channel(AXI0_WID==6) [6]: Reconstructed picture channel (AXI0_WID==5) [5]: ME information channel (AXI0_WID==4) [4]: Co-located Mv channel (AXI0_WID==3) [3]: Down-sampled picture channel (AXI0_WID==2) [2]: Bit stream channel (AXI0_WID==1) [1]: Link table node channel (AXI0_WID==0) [0]: Reserved

VEPU_ST_SNUM

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	sli_num Number for slices has been encoded and not read out (by reading ST_SLEN).

VEPU_ST_SLEN

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RO	0x0000000	sli_len Byte length for the earlist encoded slice which has not been read out(by reading VEPU_ST_SLEN).

VEPU_ST_PNUM_P64

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:0	RO	0x000	pnum_p64 Number of 64x64 inter predicted blocks.

VEPU_ST_PNUM_P32

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	pnum_p32 Number of 32x32 inter predicted blocks.

VEPU_ST_PNUM_P16

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pnum_p16 Number of 16x16 inter predicted blocks.

VEPU_ST_PNUM_P8

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	pnum_p8 Number of 8x8 inter predicted blocks.

VEPU_ST_PNUM_I32

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	pnum_i32 Number of 32x32 intra predicted blocks.

VEPU_ST_PNUM_I16

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	pnum_i16 Number of 16x16 intra predicted blocks.

VEPU_ST_PNUM_I8

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	pnum_i8 Number of 8x8 intra predicted blocks.

VEPU_ST_PNUM_I4

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	pnum_i4 Number of 4x4 intra predicted blocks.

VEPU_ST_B8_QP0

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp0 Number of block8x8s with QP=0. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP1

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp1 Number of block8x8s with QP=1. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP2

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp2 Number of block8x8s with QP=2. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP3

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp3 Number of block8x8s with QP=3. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP4

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp4 Number of block8x8s with QP=4. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP5

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp5 Number of block8x8s with QP=5. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP6

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp6 Number of block8x8s with QP=6. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP7

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp7 Number of block8x8s with QP=7. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP8

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp8 Number of block8x8s with QP=8. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP9

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp9 Number of block8x8s with QP=9. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP10

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp10 Number of block8x8s with QP=10. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP11

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp11 Number of block8x8s with QP=11. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP12

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp12 Number of block8x8s with QP=12. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP13

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp13 Number of block8x8s with QP=13. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP14

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp14 Number of block8x8s with QP=14. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP15

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp15 Number of block8x8s with QP=15. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP16

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:0	RO	0x00000	b8num_qp16 Number of block8x8s with QP=16. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP17

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp17 Number of block8x8s with QP=17. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP18

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp18 Number of block8x8s with QP=18. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP19

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	b8num_qp19 Number of block8x8s with QP=19. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP20

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp20 Number of block8x8s with QP=20. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP21

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp21 Number of block8x8s with QP=21. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP22

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp22 Number of block8x8s with QP=22. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP23

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp23 Number of block8x8s with QP=23. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP24

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp24 Number of block8x8s with QP=24. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP25

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp25 Number of block8x8s with QP=25. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP26

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp26 Number of block8x8s with QP=26. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP27

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp27 Number of block8x8s with QP=27. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP28

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp28 Number of block8x8s with QP=28. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP29

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	b8num_qp29 Number of block8x8s with QP=29. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP30

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp30 Number of block8x8s with QP=30. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP31

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp31 Number of block8x8s with QP=31. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP32

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp32 Number of block8x8s with QP=32. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP33

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp33 Number of block8x8s with QP=33. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP34

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp34 Number of block8x8s with QP=34. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP35

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:0	RO	0x00000	b8num_qp35 Number of block8x8s with QP=35. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP36

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp36 Number of block8x8s with QP=36. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP37

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp37 Number of block8x8s with QP=37. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP38

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp38 Number of block8x8s with QP=38. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP39

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp39 Number of block8x8s with QP=39. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP40

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp40 Number of block8x8s with QP=40. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP41

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp41 Number of block8x8s with QP=41. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP42

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp42 Number of block8x8s with QP=42. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP43

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp43 Number of block8x8s with QP=43. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP44

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp44 Number of block8x8s with QP=44. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP45

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp45 Number of block8x8s with QP=45. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP46

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp46 Number of block8x8s with QP=46. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP47

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp47 Number of block8x8s with QP=47. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP48

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp48 Number of block8x8s with QP=48. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP49

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp49 Number of block8x8s with QP=49. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP50

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp50 Number of block8x8s with QP=50. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP51

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	b8num_qp51 Number of block8x8s with QP=51. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_CPLX_TMP

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	madp Mean absolute differences between current encoding and reference frame.

VEPU_ST_BNUM_CME

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	num_ctu Number of CTU (HEVC: 64x64; H.264: 64x16) for CME inter-frame prediction.

VEPU_ST_CPLX_SPT

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	madi Mean absolute differences for current encoding frame.

VEPU_ST_BNUM_B16

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	num_b16 Number of valid 16x16 blocks for one frame.

VEPU_ST_CPLX_MAX_B16

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	num_madi_max_b16 Number of 16x16 blocks which the value is bigger than sw_aq_thd15.

VEPU_L2CFG_ADDR

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	l2cfg_addr Level2 configuration address.

VEPU_L2CFG_WDATA

Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	l2cfg_wdata L2 configuration write data. Single access: write address to VEPU_L2CFG_ADDR then write data to VEPU_L2CFG_WDATA. Burst access: write the start address to VEPU_L2CFG_ADDR then write datas (to VEPU_L2CFG_WDATA) consecutively. Address will be auto increased after write VEPU_L2CFG_WDATA, no need to configure VEPU_L2CFG_ADDR.

VEPU_L2CFG_RDATA

Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	l2cfg_rdata L2 configuration read data. Single access: write address to VEPU_L2CFG_ADDR then read data from VEPU_L2CFG_RDATA. Burst access: write the start address to VEPU_L2CFG_ADDR then read datas (from VEPU_L2CFG_RDATA) consecutively. Address will be auto increased after read VEPU_L2CFG_RDATA, no need to configure VEPU_L2CFG_ADDR.

VEPU_OSD_PLT0

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	v V component
15:8	RW	0x00	u U component
7:0	RW	0x00	y Y component

VEPU_OSD_PLT1

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	v V component
15:8	RW	0x00	u U component
7:0	RW	0x00	y Y component

VEPU_OSD_PLT255

Address: Operational Base + offset (0x07FC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	alpha Alpha
23:16	RW	0x00	v V component
15:8	RW	0x00	u U component
7:0	RW	0x00	y Y component

VEPU_ST_WDG

Address: Operational Base + offset (0x085C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	frm_tout Frame encoding time out.
7	RO	0x0	reserved
6	RO	0x0	reserved
5	RO	0x0	reserved
4	RO	0x0	reserved
3	RO	0x0	reserved
2	RO	0x0	reserved
1	RO	0x0	reserved
0	RO	0x0	reserved

VEPU_ST_PPL

Address: Operational Base + offset (0x0860)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	frm_wrk Frame encoding is working.
7	RO	0x0	etpy_wrk Entropy is working.
6	RO	0x0	lpf_wrk Loop filter is working.
5	RO	0x0	rdo_wrk RDO is working.
4	RO	0x0	fme_wrk FME is working.
3	RO	0x0	rme_wrk RME is working.
2	RO	0x0	swn_wrk Search window load is working.
1	RO	0x0	cme_wrk CME is working.
0	RO	0x0	pp_wrk Pre-process is working.

VEPU_ST_SLI_NUM

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RO	0x000	sli_num Number of slices.

VEPU_DBG_DMA_RFPR

Address: Operational Base + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:20	RW	0x0	dfifo5_lvl Level of data FIFO5.
19:16	RW	0x0	dfifo4_lvl Level of data FIFO4.
15:12	RO	0x0	reserved
11:8	RO	0x0	reserved
7:4	RO	0x0	reserved
3:0	RO	0x0	reserved

VEPU_DBG_DMA_CH_ST

Address: Operational Base + offset (0x08E8)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	dspr_otsd DSPR channel read outstanding.
27:16	RW	0x000	rfpr_otsd RFPR channel read outstanding.
15:12	RO	0x0	reserved
11	RO	0x0	reserved
10	RO	0x0	reserved
9	RO	0x0	reserved
8	RO	0x0	reserved
7	RO	0x0	reserved
6	RO	0x0	reserved
5	RO	0x0	reserved
4	RO	0x0	reserved
3	RO	0x0	reserved
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RO	0x0	reserved

VEPU_MMU0_ADDR

Address: Operational Base + offset (0x0F00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu0_dte_addr Page table address for AXI0 MMU0.

VEPU_MMU0_ST

Address: Operational Base + offset (0x0F04)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	mmu_flt_id ID for the last MMU0 fault.
5	RO	0x0	mmu_flt_typ Type of MMU0 fault. 1'h0: Read fault. 1'h1: Write fault.
4	RO	0x0	mmu_rbly_epty MMU0 replay buffer is empty.
3	RO	0x0	mmu_idl MMU0 idle.
2	RO	0x0	mmu_stl MMU0 stall.
1	RO	0x0	mmu_flt MMU0 page fault.
0	RO	0x0	mmu_e MMU0 is enabled.

VEPU_MMU0_CMD

Address: Operational Base + offset (0x0F08)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU0 command. 3'h0: MMU mapping enable. 3'h1: MMU mapping disable. 3'h2: MMU stall enable. 3'h3: MMU stall disable. 3'h4: Zap(disable) page table cache line. 3'h5: Leave fault mode. 3'h6: MMU reset.

VEPU_MMU0_PFA

Address: Operational Base + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_pfa Address of the last page fault.

VEPU_MMU0_ZAP

Address: Operational Base + offset (0x0F10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zpa Invalid address for page table cache mapping.

VEPU_MMU0_ERR

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rb_err Read bus error.
0	RO	0x0	pf_err Page fault error.

VEPU_MMU0_INT_CLR

Address: Operational Base + offset (0x0F18)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_clr Read bus error interrupt clear.
0	RW	0x0	pfe_clr Page fault error interrupt clear.

VEPU_MMU0_INT_MSK

Address: Operational Base + offset (0x0F1C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_msk Read bus error interrupt mask.
0	RW	0x0	pfe_msk Page fault error interrupt mask.

VEPU_MMU0_INT_STA

Address: Operational Base + offset (0x0F20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rbe_sta Read bus error interrupt status.
0	RO	0x0	pfe_sta Page fault error interrupt status.

VEPU_MMU0_ACKG

Address: Operational Base + offset (0x0F24)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x1	mmu_ackg Auto clock gating enable.

VEPU_MMU1_ADDR

Address: Operational Base + offset (0x0F40)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu1_dte_addr Page table address for AXI1 MMU1.

VEPU_MMU1_ST

Address: Operational Base + offset (0x0F44)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	mmu_flt_id ID for the last MMU fault.
5	RO	0x0	mmu_flt_typ Type of MMU1 fault. 1'h0: Read fault. 1'h1: Write fault.
4	RO	0x0	mmu_rbly_epty MMU1 replay buffer is empty.
3	RO	0x0	mmu_idl MMU1 idle.
2	RO	0x0	mmu_stl MMU1 stall.
1	RO	0x0	mmu_flt MMU1 page fault.
0	RO	0x0	mmu_e MMU1 is enabled.

VEPU_MMU1_CMD

Address: Operational Base + offset (0x0F48)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU1 command. 3'h0: MMU mapping enable. 3'h1: MMU mapping disable. 3'h2: MMU stall enable. 3'h3: MMU stall disable. 3'h4: Zap(disable) page table cache line. 3'h5: Leave fault mode. 3'h6: MMU reset.

VEPU_MMU1_PFA

Address: Operational Base + offset (0x0F4C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_pfa Address of the last page fault.

VEPU_MMU1_ZAP

Address: Operational Base + offset (0x0F50)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zpa Invalid address for page table cache mapping.

VEPU_MMU1_ERR

Address: Operational Base + offset (0x0F54)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pf_err Page fault error.

VEPU_MMU1_INT_CLR

Address: Operational Base + offset (0x0F58)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_clr Read bus error interrupt clear.
0	RW	0x0	pfe_clr Page fault error interrupt clear.

VEPU_MMU1_INT_MSK

Address: Operational Base + offset (0x0F5C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_msk Read bus error interrupt mask.
0	RW	0x0	pfe_msk Page fault error interrupt mask.

VEPU_MMU1_INT_STA

Address: Operational Base + offset (0x0F60)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rbe_sta Read bus error interrupt status.
0	RO	0x0	pfe_sta Page fault error interrupt status.

VEPU_MMU1_ACKG

Address: Operational Base + offset (0x0F64)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_ackg Auto clock gating enable.

10.5.26 VEPU540 LAYER2 Register Address Mapping

Table 10-16 VEPU LAYER2 Address Mapping

Name	Offset	Size	Reset Value	Description
VEPU2_IPRD_TTHDY4_0_H264	0x0004	W	0x00000000	Texture thredsholds register0 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU2_IPRD_TTHD32_0_HEVC	0x0004	W	0x00000000	Texture thredshold register0 for HEVC 32x32 intra prediction, share address with H.264.
VEPU2_IPRD_TTHDY4_1_H264	0x0008	W	0x00000000	Texture thredsholds register1 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU2_IPRD_TTHD32_1_HEVC	0x0008	W	0x00000000	Texture thredsholds register1 for HEVC 32x32 intra prediction, share address with H.264.
VEPU2_IPRD_TTHDC8_0_H264	0x000C	W	0x00000000	Texture thredsholds register0 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU2_IPRD_TTHD16_0_HEVC	0x000C	W	0x00000000	Texture thredshold register0 for HEVC 16x16 intra prediction, share address with H.264.
VEPU2_IPRD_TTHDC8_1_H264	0x0010	W	0x00000000	Texture thredsholds register1 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU2_IPRD_TTHD16_1_HEVC	0x0010	W	0x00000000	Texture thredshold register1 for HEVC 16x16 intra prediction, share address with H.264.
VEPU2_IPRD_TTHDY8_0_H264	0x0014	W	0x00000000	Texture thredsholds register0 for H.264 LUMA 8x8 intra prediction.
VEPU2_IPRD_TTHDY8_1_H264	0x0018	W	0x00000000	texture thredsholds register1 for H.264 LUMA 8x8 intra prediction.
VEPU2_IPRD_TTHD_UL_H264	0x001C	W	0x00000000	Texture thredsholds of up and left MB for H.264 LUMA intra prediction.
VEPU2_IPRD_WGTY8_H264	0x0020	W	0x00000000	Teights of the cost for H.264 LUMA 8x8 intra prediction, share address with HEVC.

Name	Offset	Size	Reset Value	Description
VEPU2_IPRD_WGTY32_0_HEVC	0x0020	W	0x00000000	Tost weights register0 for HEVC LUMA 32x32 intra prediction, share address with H.264.
VEPU2_IPRD_WGTY4_H264	0x0024	W	0x00000000	Weights of the cost for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU2_IPRD_WGTY32_1_HEVC	0x0024	W	0x00000000	Cost weights register1 for HEVC LUMA 32x32 intra prediction, share address with H.264.
VEPU2_IPRD_WGTY16_H264	0x0028	W	0x00000000	Weights of the cost for H.264 LUMA 16x16 intra prediction, share address with HEVC.
VEPU2_IPRD_WGTY16_0_HEVC	0x0028	W	0x00000000	Cost weights register0 for HEVC LUMA 16x16 intra prediction.
VEPU2_IPRD_WGTC8_H264	0x002C	W	0x00000000	Weights of the cost for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU2_IPRD_WGTY16_1_HEVC	0x002C	W	0x00000000	Cost weights register1 for HEVC LUMA 16x16 intra prediction.
VEPU2_QNT_BIAS_COMB	0x0030	W	0x00000000	Quantization bias for H.264 and HEVC.
VEPU2_ATR_THD0_H264	0x0034	W	0x00000000	H.264 anti ringing noise threshold configuration0.
VEPU2_ATR_THD1_H264	0x0038	W	0x00000000	H.264 anti ringing noise threshold configuration1.
VEPU2_ATR_WGT16_H264	0x003C	W	0x00000000	Weights of 16x16 cost for H.264 anti ringing noise.
VEPU2_ATR_WGT8_H264	0x0040	W	0x00000000	Weights of 8x8 cost for H.264 anti ringing noise.
VEPU2_ATR_WGT4_H264	0x0044	W	0x00000000	Weights of 4x4 cost for H.264 anti ringing noise.
VEPU2_ATF_TTHD0_H264	0x0048	W	0x00000000	Texture threshold configuration0 for H.264 anti-flicker, share address with HEVC.

Name	Offset	Size	Reset Value	Description
VEPU2_ATF_TTHD_I32_HEVC	0x0048	W	0x00000000	Intra32x32 texture threshold for HEVC anti-flicker, share address with H.264.
VEPU2_ATF_TTHD1_H264	0x004C	W	0x00000000	Texture threshold configuration1 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_TTHD_I16_HEVC	0x004C	W	0x00000000	Intra16x16 texture thresholdfor HEVC anti-flicker, share address with H.264.
VEPU2_ATF_STHD0_H264	0x0050	W	0x00000000	(CME) SAD threshold configuration0 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_TTHD_P64_HEVC	0x0050	W	0x00000000	Inter64x64 texture thresholdfor HEVC anti-flicker, share address with H.264.
VEPU2_ATF_STHD1_H264	0x0054	W	0x00000000	(CME) SAD threshold configuration1 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_TTHD_P32_HEVC	0x0054	W	0x00000000	Inter32x32 texture thresholdfor HEVC anti-flicker, share address with H.264.
VEPU2_ATF_WGT0_H264	0x0058	W	0x00000000	Weight configuration0 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_TTHD_P16_HEVC	0x0058	W	0x00000000	Inter16x16 texture thresholdfor HEVC anti-flicker, share address with H.264.
VEPU2_ATF_WGT1_H264	0x005C	W	0x00000000	Weight configuration1 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_WGT0_HEVC	0x005C	W	0x00000000	Weight configuration0 for HEVC anti-flicker, share address with H.264.
VEPU2_ATF_WGT2_H264	0x0060	W	0x00000000	Weight configuration2 for H.264 anti-flicker, share address with HEVC.

Name	Offset	Size	Reset Value	Description
VEPU2_ATF_WGT1_HEVC	0x0060	W	0x00000000	Weight configuration1 for HEVC anti-flicker, share address with H.264.
VEPU2_ATF_OFST0_H264	0x0064	W	0x00000000	Offset configuration0 for H.264 anti-flicker, share address with HEVC.
VEPU2_ATF_WGT2_HEVC	0x0064	W	0x00000000	Weight configuration2 for HEVC anti-flicker, share address with H.264.
VEPU2_ATF_OFST1_H264	0x0068	W	0x00000000	Offset configuration1 for H.264 anti-flicker.
VEPU2_ATF_OFST2_H264	0x006C	W	0x00000000	Offset configuration2 for H.264 anti-flicker.
VEPU2_IPRD_WGT_QP0_HEVC	0x0070	W	0x00000000	Weight of SATD cost when QP is 0 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP1_HEVC	0x0074	W	0x00000000	Weight of SATD cost when QP is 1 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP2_HEVC	0x0078	W	0x00000000	Weight of SATD cost when QP is 2 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP3_HEVC	0x007C	W	0x00000000	Weight of SATD cost when QP is 3 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP4_HEVC	0x0080	W	0x00000000	Weight of SATD cost when QP is 4 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP5_HEVC	0x0084	W	0x00000000	Weight of SATD cost when QP is 5 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP6_HEVC	0x0088	W	0x00000000	Weight of SATD cost when QP is 6 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP7_HEVC	0x008C	W	0x00000000	Weight of SATD cost when QP is 7 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP8_HEVC	0x0090	W	0x00000000	Weight of SATD cost when QP is 8 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP9_HEVC	0x0094	W	0x00000000	Weight of SATD cost when QP is 9 for HEVC intra prediction.

Name	Offset	Size	Reset Value	Description
VEPU2_IPRD_WGT_QP10_HEVC	0x0098	W	0x00000000	Weight of SATD cost when QP is 10 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP11_HEVC	0x009C	W	0x00000000	Weight of SATD cost when QP is 11 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP12_HEVC	0x00A0	W	0x00000000	Weight of SATD cost when QP is 12 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP13_HEVC	0x00A4	W	0x00000000	Weight of SATD cost when QP is 13 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP14_HEVC	0x00A8	W	0x00000000	Weight of SATD cost when QP is 14 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP15_HEVC	0x00AC	W	0x00000000	Weight of SATD cost when QP is 15 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP16_HEVC	0x00B0	W	0x00000000	Weight of SATD cost when QP is 16 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP17_HEVC	0x00B4	W	0x00000000	Weight of SATD cost when QP is 17 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP18_HEVC	0x00B8	W	0x00000000	Weight of SATD cost when QP is 18 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP19_HEVC	0x00BC	W	0x00000000	Weight of SATD cost when QP is 19 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP20_HEVC	0x00C0	W	0x00000000	Weight of SATD cost when QP is 20 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP21_HEVC	0x00C4	W	0x00000000	Weight of SATD cost when QP is 21 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP22_HEVC	0x00C8	W	0x00000000	Weight of SATD cost when QP is 22 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP23_HEVC	0x00CC	W	0x00000000	Weight of SATD cost when QP is 23 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP24_HEVC	0x00D0	W	0x00000000	Weight of SATD cost when QP is 24 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP25_HEVC	0x00D4	W	0x00000000	Weight of SATD cost when QP is 25 for HEVC intra prediction.

Name	Offset	Size	Reset Value	Description
VEPU2_IPRD_WGT_QP26_HEVC	0x00D8	W	0x00000000	Weight of SATD cost when QP is 26 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP27_HEVC	0x00DC	W	0x00000000	Weight of SATD cost when QP is 27 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP28_HEVC	0x00E0	W	0x00000000	Weight of SATD cost when QP is 28 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP29_HEVC	0x00E4	W	0x00000000	Weight of SATD cost when QP is 29 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP30_HEVC	0x00E8	W	0x00000000	Weight of SATD cost when QP is 30 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP31_HEVC	0x00EC	W	0x00000000	Weight of SATD cost when QP is 31 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP32_HEVC	0x00F0	W	0x00000000	Weight of SATD cost when QP is 32 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP33_HEVC	0x00F4	W	0x00000000	Weight of SATD cost when QP is 33 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP34_HEVC	0x00F8	W	0x00000000	Weight of SATD cost when QP is 34 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP35_HEVC	0x00FC	W	0x00000000	Weight of SATD cost when QP is 35 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP36_HEVC	0x0100	W	0x00000000	Weight of SATD cost when QP is 36 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP37_HEVC	0x0104	W	0x00000000	Weight of SATD cost when QP is 37 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP38_HEVC	0x0108	W	0x00000000	Weight of SATD cost when QP is 38 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP39_HEVC	0x010C	W	0x00000000	Weight of SATD cost when QP is 39 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP40_HEVC	0x0110	W	0x00000000	Weight of SATD cost when QP is 40 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP41_HEVC	0x0114	W	0x00000000	Weight of SATD cost when QP is 41 for HEVC intra prediction.

Name	Offset	Size	Reset Value	Description
VEPU2_IPRD_WGT_QP42_HEVC	0x0118	W	0x00000000	Weight of SATD cost when QP is 42 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP43_HEVC	0x011C	W	0x00000000	Weight of SATD cost when QP is 43 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP44_HEVC	0x0120	W	0x00000000	Weight of SATD cost when QP is 44 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP45_HEVC	0x0124	W	0x00000000	Weight of SATD cost when QP is 45 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP46_HEVC	0x0128	W	0x00000000	Weight of SATD cost when QP is 46 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP47_HEVC	0x012C	W	0x00000000	Weight of SATD cost when QP is 47 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP48_HEVC	0x0130	W	0x00000000	Weight of SATD cost when QP is 48 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP49_HEVC	0x0134	W	0x00000000	Weight of SATD cost when QP is 49 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP50_HEVC	0x0138	W	0x00000000	Weight of SATD cost when QP is 50 for HEVC intra prediction.
VEPU2_IPRD_WGT_QP51_HEVC	0x013C	W	0x00000000	Weight of SATD cost when QP is 51 for HEVC intra prediction.
VEPU2_RDO_WGTA_QP0_COMB	0x0140	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 0.
VEPU2_RDO_WGTA_QP1_COMB	0x0144	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 1.
VEPU2_RDO_WGTA_QP2_COMB	0x0148	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 2.
VEPU2_RDO_WGTA_QP3_COMB	0x014C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 3.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTA_QP4_COMB	0x0150	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 4.
VEPU2_RDO_WGTA_QP5_COMB	0x0154	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 5.
VEPU2_RDO_WGTA_QP6_COMB	0x0158	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 6.
VEPU2_RDO_WGTA_QP7_COMB	0x015C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 7.
VEPU2_RDO_WGTA_QP8_COMB	0x0160	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 8.
VEPU2_RDO_WGTA_QP9_COMB	0x0164	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 9.
VEPU2_RDO_WGTA_QP10_COMB	0x0168	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 10.
VEPU2_RDO_WGTA_QP11_COMB	0x016C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 11.
VEPU2_RDO_WGTA_QP12_COMB	0x0170	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 12.
VEPU2_RDO_WGTA_QP13_COMB	0x0174	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 13.
VEPU2_RDO_WGTA_QP14_COMB	0x0178	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 14.
VEPU2_RDO_WGTA_QP15_COMB	0x017C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 15.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTA_QP16_COMB	0x0180	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 16.
VEPU2_RDO_WGTA_QP17_COMB	0x0184	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 17.
VEPU2_RDO_WGTA_QP18_COMB	0x0188	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 18.
VEPU2_RDO_WGTA_QP19_COMB	0x018C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 19.
VEPU2_RDO_WGTA_QP20_COMB	0x0190	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 20.
VEPU2_RDO_WGTA_QP21_COMB	0x0194	W	0x00000000	Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 21.
VEPU2_RDO_WGTA_QP22_COMB	0x0198	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 22.
VEPU2_RDO_WGTA_QP23_COMB	0x019C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 23.
VEPU2_RDO_WGTA_QP24_COMB	0x01A0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 24.
VEPU2_RDO_WGTA_QP25_COMB	0x01A4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 25.
VEPU2_RDO_WGTA_QP26_COMB	0x01A8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 26.
VEPU2_RDO_WGTA_QP27_COMB	0x01AC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 27.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTA_QP28_COMB	0x01B0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 28.
VEPU2_RDO_WGTA_QP29_COMB	0x01B4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 29.
VEPU2_RDO_WGTA_QP30_COMB	0x01B8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 30.
VEPU2_RDO_WGTA_QP31_COMB	0x01BC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 31.
VEPU2_RDO_WGTA_QP32_COMB	0x01C0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 32.
VEPU2_RDO_WGTA_QP33_COMB	0x01C4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 33.
VEPU2_RDO_WGTA_QP34_COMB	0x01C8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 34.
VEPU2_RDO_WGTA_QP35_COMB	0x01CC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 35.
VEPU2_RDO_WGTA_QP36_COMB	0x01D0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 36.
VEPU2_RDO_WGTA_QP37_COMB	0x01D4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 37.
VEPU2_RDO_WGTA_QP38_COMB	0x01D8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 38.
VEPU2_RDO_WGTA_QP39_COMB	0x01DC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 39.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTA_QP40_COMB	0x01E0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 40.
VEPU2_RDO_WGTA_QP41_COMB	0x01E4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 41.
VEPU2_RDO_WGTA_QP42_COMB	0x01E8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 42.
VEPU2_RDO_WGTA_QP43_COMB	0x01EC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 43.
VEPU2_RDO_WGTA_QP44_COMB	0x01F0	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 44.
VEPU2_RDO_WGTA_QP45_COMB	0x01F4	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 45.
VEPU2_RDO_WGTA_QP46_COMB	0x01F8	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 46.
VEPU2_RDO_WGTA_QP47_COMB	0x01FC	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 47.
VEPU2_RDO_WGTA_QP48_COMB	0x0200	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 48.
VEPU2_RDO_WGTA_QP49_COMB	0x0204	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 49.
VEPU2_RDO_WGTA_QP50_COMB	0x0208	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 50.
VEPU2_RDO_WGTA_QP51_COMB	0x020C	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 51.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTB_QP0_COMB	0x0210	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 0.
VEPU2_RDO_WGTB_QP1_COMB	0x0214	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 1.
VEPU2_RDO_WGTB_QP2_COMB	0x0218	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 2.
VEPU2_RDO_WGTB_QP3_COMB	0x021C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 3.
VEPU2_RDO_WGTB_QP4_COMB	0x0220	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 4.
VEPU2_RDO_WGTB_QP5_COMB	0x0224	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 5.
VEPU2_RDO_WGTB_QP6_COMB	0x0228	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 6.
VEPU2_RDO_WGTB_QP7_COMB	0x022C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 7.
VEPU2_RDO_WGTB_QP8_COMB	0x0230	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 8.
VEPU2_RDO_WGTB_QP9_COMB	0x0234	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 9.
VEPU2_RDO_WGTB_QP10_COMB	0x0238	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 10.
VEPU2_RDO_WGTB_QP11_COMB	0x023C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 11.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTB_QP12_COMB	0x0240	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 12.
VEPU2_RDO_WGTB_QP13_COMB	0x0244	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 13.
VEPU2_RDO_WGTB_QP14_COMB	0x0248	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 14.
VEPU2_RDO_WGTB_QP15_COMB	0x024C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 15.
VEPU2_RDO_WGTB_QP16_COMB	0x0250	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 16.
VEPU2_RDO_WGTB_QP17_COMB	0x0254	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 17.
VEPU2_RDO_WGTB_QP18_COMB	0x0258	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 18.
VEPU2_RDO_WGTB_QP19_COMB	0x025C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 19.
VEPU2_RDO_WGTB_QP20_COMB	0x0260	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 20.
VEPU2_RDO_WGTB_QP21_COMB	0x0264	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 21.
VEPU2_RDO_WGTB_QP22_COMB	0x0268	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 22.
VEPU2_RDO_WGTB_QP23_COMB	0x026C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 23.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTB_QP24_COMB	0x0270	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 24.
VEPU2_RDO_WGTB_QP25_COMB	0x0274	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 25.
VEPU2_RDO_WGTB_QP26_COMB	0x0278	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 26.
VEPU2_RDO_WGTB_QP27_COMB	0x027C	W	0x00000000	Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 27.
VEPU2_RDO_WGTB_QP28_COMB	0x0280	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 28.
VEPU2_RDO_WGTB_QP29_COMB	0x0284	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 29.
VEPU2_RDO_WGTB_QP30_COMB	0x0288	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 30.
VEPU2_RDO_WGTB_QP31_COMB	0x028C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 31.
VEPU2_RDO_WGTB_QP32_COMB	0x0290	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 32.
VEPU2_RDO_WGTB_QP33_COMB	0x0294	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 33.
VEPU2_RDO_WGTB_QP34_COMB	0x0298	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 34.
VEPU2_RDO_WGTB_QP35_COMB	0x029C	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 35.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTB_QP36_COMB	0x02A0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 36.
VEPU2_RDO_WGTB_QP37_COMB	0x02A4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 37.
VEPU2_RDO_WGTB_QP38_COMB	0x02A8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 38.
VEPU2_RDO_WGTB_QP39_COMB	0x02AC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 39.
VEPU2_RDO_WGTB_QP40_COMB	0x02B0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 40.
VEPU2_RDO_WGTB_QP41_COMB	0x02B4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 41.
VEPU2_RDO_WGTB_QP42_COMB	0x02B8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 42.
VEPU2_RDO_WGTB_QP43_COMB	0x02BC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 43.
VEPU2_RDO_WGTB_QP44_COMB	0x02C0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 44.
VEPU2_RDO_WGTB_QP45_COMB	0x02C4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 45.
VEPU2_RDO_WGTB_QP46_COMB	0x02C8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 46.
VEPU2_RDO_WGTB_QP47_COMB	0x02CC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 47.

Name	Offset	Size	Reset Value	Description
VEPU2_RDO_WGTB_QP48_COMB	0x02D0	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 48.
VEPU2_RDO_WGTB_QP49_COMB	0x02D4	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 49.
VEPU2_RDO_WGTB_QP50_COMB	0x02D8	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 50.
VEPU2_RDO_WGTB_QP51_COMB	0x02DC	W	0x00000000	Weight of group B for HEVC and H.264 RDO mode decision when QP is 51.
VEPU2_MADI_CFG	0x02E0	W	0x00000000	MADI configuration.
VEPU2_AQ_TTHD0	0x02E4	W	0x00000000	Texture threshold configuration0 for adaptive QP adjustment.
VEPU2_AQ_TTHD1	0x02E8	W	0x00000000	Texture threshold configuration1 for adaptive QP adjustment.
VEPU2_AQ_TTHD2	0x02EC	W	0x00000000	Texture threshold configuration2 for adaptive QP adjustment.
VEPU2_AQ_TTHD3	0x02F0	W	0x00000000	Texture threshold configuration3 for adaptive QP adjustment.
VEPU2_AQ_STP0	0x02F4	W	0x00000000	Adjustment step configuration0 for adaptive QP adjustment.
VEPU2_AQ_STP1	0x02F8	W	0x00000000	Adjustment step configuration1 for adaptive QP adjustment.
VEPU2_AQ_STP2	0x02FC	W	0x00000000	Adjustment step configuration2 for adaptive QP adjustment.
VEPU2_AQ_STP3	0x0300	W	0x00000000	Adjustment step configuration3 for adaptive QP adjustment.
VEPU2_RME_MVD_PNSH_H264	0x0304	W	0x00000000	RME MVD(motion vector difference) cost penalty, H.264 only.
VEPU2_ATR1_THD0_H264	0x0308	W	0x00000000	H.264 anti ringing noise threshold configuration0 of group1.

Name	Offset	Size	Reset Value	Description
VEPU2_ATR1_THD1_H264	0x030C	W	0x00000000	H.264 anti ringing noise threshold configuration1 of group1.
VEPU2_PREI_DIF_IDX00L_HEVC	0x0310	W	0x0E34C2CA	Low 30 bits of HEVC pre-intra difference idx00.
VEPU2_PREI_DIF_IDX00H_HEVC	0x0314	W	0x074083C9	High 30 bits of HEVC pre-intra difference idx00.
VEPU2_PREI_DIF_IDX01L_HEVC	0x0318	W	0x061C824A	Low 30 bits of HEVC pre-intra difference idx01.
VEPU2_PREI_DIF_IDX01H_HEVC	0x031C	W	0x0D10C14B	High 30 bits of HEVC pre-intra difference idx01.
VEPU2_PREI_DIF_IDX02L_HEVC	0x0320	W	0x0E3D0452	Low 30 bits of HEVC pre-intra difference idx02.
VEPU2_PREI_DIF_IDX02H_HEVC	0x0324	W	0x15314353	High 30 bits of HEVC pre-intra difference idx02.
VEPU2_PREI_DIF_IDX03L_HEVC	0x0328	W	0x165544D2	Low 30 bits of HEVC pre-intra difference idx03.
VEPU2_PREI_DIF_IDX03H_HEVC	0x032C	W	0x0F6105D1	High 30 bits of HEVC pre-intra difference idx03.
VEPU2_PREI_DIF_IDX04L_HEVC	0x0330	W	0x165D8699	Low 30 bits of HEVC pre-intra difference idx04.
VEPU2_PREI_DIF_IDX04H_HEVC	0x0334	W	0x1D51C55B	High 30 bits of HEVC pre-intra difference idx04.
VEPU2_PREI_DIF_IDX05L_HEVC	0x0338	W	0x1E75C69B	Low 30 bits of HEVC pre-intra difference idx05.
VEPU2_PREI_DIF_IDX05H_HEVC	0x033C	W	0x178187D9	High 30 bits of HEVC pre-intra difference idx05.
VEPU2_PREI_DIF_IDX06L_HEVC	0x0340	W	0x1E7E0862	Low 30 bits of HEVC pre-intra difference idx06.
VEPU2_PREI_DIF_IDX06H_HEVC	0x0344	W	0x04703742	High 30 bits of HEVC pre-intra difference idx06.
VEPU2_PREI_DIF_IDX07L_HEVC	0x0348	W	0x051030A2	Low 30 bits of HEVC pre-intra difference idx07.

Name	Offset	Size	Reset Value	Description
VEPU2_PREI_DIF_IDX07H_HEVC	0x034C	W	0x1F1E01A1	High 30 bits of HEVC pre-intra difference idx07.
VEPU2_PREI_DIF_IDX08L_HEVC	0x0350	W	0x0689268A	Low 30 bits of HEVC pre-intra difference idx08.
VEPU2_PREI_DIF_IDX08H_HEVC	0x0354	W	0x1809E58E	High 30 bits of HEVC pre-intra difference idx08.
VEPU2_PREI_DIF_IDX09L_HEVC	0x0358	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx09.
VEPU2_PREI_DIF_IDX09H_HEVC	0x035C	W	0x00000000	High 30 bits of HEVC pre-intra difference idx09.
VEPU2_PREI_DIF_IDX10L_HEVC	0x0360	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx10.
VEPU2_PREI_DIF_IDX10H_HEVC	0x0364	W	0x00000000	High 30 bits of HEVC pre-intra difference idx10.
VEPU2_PREI_DIF_IDX11L_HEVC	0x0368	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx11.
VEPU2_PREI_DIF_IDX11H_HEVC	0x036C	W	0x00000000	High 30 bits of HEVC pre-intra difference idx11.
VEPU2_PREI_DIF_IDX12L_HEVC	0x0370	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx12.
VEPU2_PREI_DIF_IDX12H_HEVC	0x0374	W	0x00000000	High 30 bits of HEVC pre-intra difference idx12.
VEPU2_PREI_DIF_IDX13L_HEVC	0x0378	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx13.
VEPU2_PREI_DIF_IDX13H_HEVC	0x037C	W	0x00000000	High 30 bits of HEVC pre-intra difference idx13.
VEPU2_PREI_DIF_IDX14L_HEVC	0x0380	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx14.
VEPU2_PREI_DIF_IDX14H_HEVC	0x0384	W	0x00000000	High 30 bits of HEVC pre-intra difference idx14.
VEPU2_PREI_DIF_IDX15L_HEVC	0x0388	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx15.

Name	Offset	Size	Reset Value	Description
VEPU2_PREI_DIF_IDX15H_HEVC	0x038C	W	0x00000000	High 30 bits of HEVC pre-intra difference idx15.
VEPU2_PREI_DIF_IDX16L_HEVC	0x0390	W	0x00000000	Low 30 bits of HEVC pre-intra difference idx16.
VEPU2_PREI_DIF_IDX16H_HEVC	0x0394	W	0x00000000	High 30 bits of HEVC pre-intra difference idx16.
VEPU2_RDO_CKG_H264	0x0400	W	0x00000000	H264 RDO clock-gating enable.
VEPU2_RDO_CKG_HEVC	0x0400	W	0x00000000	HEVC RDO clock-gating enable.
VEPU2_I16_SOBEL_T_HEVC	0x0410	W	0x00000000	HEVC intra cost16 adjust theshold.
VEPU2_I16_SOBEL_A_00_HEVC	0x0414	W	0x00000000	Part1 of a0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_A_01_HEVC	0x0418	W	0x00000000	Part2 of a0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_B_00_HEVC	0x041C	W	0x00000000	Part1 of b0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_B_01_HEVC	0x0420	W	0x00000000	Part2 of b0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_B_02_HEVC	0x0424	W	0x00000000	Part3 of b0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_B_03_HEVC	0x0428	W	0x00000000	Part4 of b0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_B_04_HEVC	0x042C	W	0x00000000	Part5 of b0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_C_00_HEVC	0x0430	W	0x00000000	Part1 of c0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_C_01_HEVC	0x0434	W	0x00000000	Part2 of c0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_D_00_HEVC	0x0438	W	0x00000000	Part1 of d0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_D_01_HEVC	0x043C	W	0x00000000	Part2 of d0 sobel parameter for HEVC 16x16 intra cost.

Name	Offset	Size	Reset Value	Description
VEPU2_I16_SOBEL_D_02_HEVC	0x0440	W	0x00000000	Part3 of d0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_D_03_HEVC	0x0444	W	0x00000000	Part4 of d0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_D_04_HEVC	0x0448	W	0x00000000	Part5 of d0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_00_HEVC	0x044C	W	0x00000000	Part1 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_01_HEVC	0x0450	W	0x00000000	Part2 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_02_HEVC	0x0454	W	0x00000000	Part3 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_03_HEVC	0x0458	W	0x00000000	Part4 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_04_HEVC	0x045C	W	0x00000000	Part5 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_05_HEVC	0x0460	W	0x00000000	Part6 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_06_HEVC	0x0464	W	0x00000000	Part7 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_07_HEVC	0x0468	W	0x00000000	Part8 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_08_HEVC	0x046C	W	0x00000000	Part9 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_09_HEVC	0x0470	W	0x00000000	Part10 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_10_HEVC	0x0474	W	0x00000000	Part11 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_11_HEVC	0x0478	W	0x00000000	Part12 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_12_HEVC	0x047C	W	0x00000000	Part13 of e0 sobel parameter for HEVC 16x16 intra cost.

Name	Offset	Size	Reset Value	Description
VEPU2_I16_SOBEL_E_13_HEVC	0x0480	W	0x00000000	Part14 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_14_HEVC	0x0484	W	0x00000000	Part15 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_15_HEVC	0x0488	W	0x00000000	Part16 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_16_HEVC	0x048C	W	0x00000000	Part17 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I16_SOBEL_E_17_HEVC	0x0490	W	0x00000000	Part18 of e0 sobel parameter for HEVC 16x16 intra cost.
VEPU2_I32_SOBEL_T_00_HEVC	0x0494	W	0x00000000	HEVC intra cost32 adjust theshold part1.
VEPU2_I32_SOBEL_T_01_HEVC	0x0498	W	0x00000000	HEVC intra cost32 adjust theshold part2.
VEPU2_I32_SOBEL_T_02_HEVC	0x049C	W	0x00000000	HEVC intra cost32 adjust theshold part3.
VEPU2_I32_SOBEL_A_HEVC	0x04A0	W	0x00000000	A0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_B_00_HEVC	0x04A4	W	0x00000000	Part1 of b0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_B_01_HEVC	0x04A8	W	0x00000000	Part2 of b0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_B_02_HEVC	0x04AC	W	0x00000000	Part3 of b0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_C_HEVC	0x04B0	W	0x00000000	C0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_D_00_HEVC	0x04B4	W	0x00000000	Part1 of d0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_D_01_HEVC	0x04B8	W	0x00000000	Part2 of d0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_D_02_HEVC	0x04BC	W	0x00000000	Part3 of d0 sobel parameter for HEVC 32x32 intra cost.

Name	Offset	Size	Reset Value	Description
VEPU2_I32_SOBEL_E_00_HEVC	0x04C0	W	0x00000000	Part1 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_01_HEVC	0x04C4	W	0x00000000	Part2 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_02_HEVC	0x04C8	W	0x00000000	Part3 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_03_HEVC	0x04CC	W	0x00000000	Part4 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_04_HEVC	0x04D0	W	0x00000000	Part5 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_05_HEVC	0x04D4	W	0x00000000	Part6 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_06_HEVC	0x04D8	W	0x00000000	Part7 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_07_HEVC	0x04DC	W	0x00000000	Part8 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_08_HEVC	0x04E0	W	0x00000000	Part9 of e0 sobel parameter for HEVC 32x32 intra cost.
VEPU2_I32_SOBEL_E_09_HEVC	0x04E4	W	0x00000000	Part10 of e0 sobel parameter for HEVC 32x32 intra cost.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.5.27 VEPU540 LAYER2 Detail Register Description

VEPU2_IPRD_TTHDY4_0_H264

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_1 The 2nd texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_0 The 1st texture threshold for H.264 LUMA 4x4 intra prediction.

VEPU2_IPRD_TTHD32_0_HEVC

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd32_1 The 2nd texture threshold for HEVC 32x32 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd32_0 The 1st texture threshold for HEVC 32x32 intra prediction.

VEPU2_IPRD_TTHDY4_1_H264

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_3 The 4th texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_2 The 3rd texture threshold for H.264 LUMA 4x4 intra prediction.

VEPU2_IPRD_TTHD32_1_HEVC

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd32_3 The 4th texture threshold for HEVC 32x32 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd32_2 The 3rd texture threshold for HEVC 32x32 intra prediction.

VEPU2_IPRD_TTHDC8_0_H264

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_1 The 2nd texture threshold for H.264 CHROMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_0 The 1st texture threshold for H.264 CHROMA 8x8 intra prediction.

VEPU2_IPRD_TTHD16_0_HEVC

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd16_1 The 2nd texture threshold for HEVC 16x16 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd16_0 The 1st texture threshold for HEVC 16x16 intra prediction.

VEPU2_IPRD_TTHDC8_1_H264

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_3 The 4th texture threshold for H.264 CHROMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_2 The 3rd texture threshold for H.264 CHROMA 8x8 intra prediction.

VEPU2_IPRD_TTHD16_1_HEVC

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthd16_3 The 4th texture threshold for HEVC 16x16 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthd16_2 The 3rd texture threshold for HEVC 16x16 intra prediction.

VEPU2_IPRD_TTHDY8_0_H264

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_1 The 2nd texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_0 The 1st texture threshold for H.264 LUMA 8x8 intra prediction.

VEPU2_IPRD_TTHDY8_1_H264

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_3 The 4th texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_2 The 3rd texture threshold for H.264 LUMA 8x8 intra prediction.

VEPU2_IPRD_TTHD_UL_H264

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	iprd_tthd_ul Texture thredsholds of up and left MB for H.264 LUMA intra prediction.

VEPU2_IPRD_WGTY8_H264

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty8_3 The 4th cost weight for H.264 LUMA 8x8 intra prediction
23:16	RW	0x00	iprd_wgty8_2 The 3rd cost weight for H.264 LUMA 8x8 intra prediction.
15:8	RW	0x00	iprd_wgty8_1 The 2nd cost weight for H.264 LUMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgty8_0 The 1st cost weight for H.264 LUMA 8x8 intra prediction.

VEPU2_IPRD_WGTY32_0_HEVC

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty32_3 The 4th cost weight for HEVC LUMA 32x32 intra prediction
23:16	RW	0x00	iprd_wgty32_2 The 3rd cost weight for HEVC LUMA 32x32 intra prediction.
15:8	RW	0x00	iprd_wgty32_1 The 2nd cost weight for HEVC LUMA 32x32 intra prediction.
7:0	RW	0x00	iprd_wgty32_0 The 1st cost weight for HEVC LUMA 32x32 intra prediction.

VEPU2_IPRD_WGTY4_H264

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty4_3 The 4th cost weight for H.264 LUMA 4x4 intra prediction
23:16	RW	0x00	iprd_wgty4_2 The 3rd cost weight for H.264 LUMA 4x4 intra prediction.
15:8	RW	0x00	iprd_wgty4_1 The 2nd cost weight for H.264 LUMA 4x4 intra prediction.
7:0	RW	0x00	iprd_wgty4_0 The 1st cost weight for H.264 LUMA 4x4 intra prediction.

VEPU2_IPRD_WGTY32_1_HEVC

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	iprd_wgty32_6 The 7th cost weight for HEVC LUMA 32x32 intra prediction.
15:8	RW	0x00	iprd_wgty32_5 The 6th cost weight for HEVC LUMA 32x32 intra prediction.
7:0	RW	0x00	iprd_wgty32_4 The 5th cost weight for HEVC LUMA 32x32 intra prediction.

VEPU2_IPRD_WGTY16_H264

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty16_3 The 4th cost weight for H.264 LUMA 16x16 intra prediction.
23:16	RW	0x00	iprd_wgty16_2 The 3rd cost weight for H.264 LUMA 16x16 intra prediction.
15:8	RW	0x00	iprd_wgty16_1 The 2nd cost weight for H.264 LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_0 The 1st cost weight for H.264 LUMA 16x16 intra prediction.

VEPU2_IPRD_WGTY16_0_HEVC

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty16_3 Tthe 4th cost weight for HEVC LUMA 16x16 intra prediction.
23:16	RW	0x00	iprd_wgty16_2 The 3rd cost weight for HEVC LUMA 16x16 intra prediction.
15:8	RW	0x00	iprd_wgty16_1 The 2nd cost weight for HEVC LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_0 The 1st cost weight for HEVC LUMA 16x16 intra prediction.

VEPU2_IPRD_WGTC8_H264

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgtc8_3 The 4th cost weight for H.264 CHROMA 8x8 intra prediction.
23:16	RW	0x00	iprd_wgtc8_2 The 3rd cost weight for H.264 CHROMA 8x8 intra prediction.
15:8	RW	0x00	iprd_wgtc8_1 The 2nd cost weight for H.264 CHROMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgtc8_0 The 1st cost weight for H.264 CHROMA 8x8 intra prediction.

VEPU2_IPRD_WGTY16_1_HEVC

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	iprd_wgty16_6 The 7th cost weight for HEVC LUMA 16x16 intra prediction, share address with H.264.
15:8	RW	0x00	iprd_wgty16_5 The 6th cost weight for HEVC LUMA 16x16 intra prediction.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	iprd_wgty16_4 The 5th cost weight for HEVC LUMA 16x16 intra prediction.

VEPU2_QNT_BIAS_COMB

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	qnt_bias_p Quantization bias for HEVC and H.264 P frame.
9:0	RW	0x000	qnt_bias_i Quantization bias for HEVC and H.264 I frame.

VEPU2_ATR_THD0_H264

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atr_thd1 The 2nd threshold for H.264 anti-ringing-noise.
15:12	RO	0x0	reserved
11:0	RW	0x000	atr_thd0 The 1st threshold for H.264 anti-ringing-noise.

VEPU2_ATR_THD1_H264

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atr_qp QP threshold of P frame for H.264 anti-ringing-nois.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	atr_thd2 The 3rd threshold for H.264 anti-ringing-noise.

VEPU2_ATR_WGT16_H264

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv16_wgt2 The 3rd weight for H.264 16x16 anti-ringing-noise.
15:8	RW	0x00	atr_lv16_wgt1 The 2nd weight for H.264 16x16 anti-ringing-noise.
7:0	RW	0x00	atr_lv16_wgt0 The 1st weight for H.264 16x16 anti-ringing-noise.

VEPU2_ATR_WGT8_H264

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv8_wgt2 The 3rd weight for H.264 8x8 anti-ringing-noise.
15:8	RW	0x00	atr_lv8_wgt1 The 2nd weight for H.264 8x8 anti-ringing-noise.
7:0	RW	0x00	atr_lv8_wgt0 The 1st weight for H.264 8x8 anti-ringing-noise.

VEPU2_ATR_WGT4_H264

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv4_wgt2 The 3rd weight for H.264 4x4 anti-ringing-noise.

Bit	Attr	Reset Value	Description
15:8	RW	0x00	atr_lv4_wgt1 The 2nd weight for H.264 4x4 anti-ringing-noise.
7:0	RW	0x00	atr_lv4_wgt0 The 1st weight for H.264 4x4 anti-ringing-noise.

VEPU2_ATF_TTHD0_H264

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd texture threshold for H.264 anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st texture threshold for H.264 anti-flicker.

VEPU2_ATF_TTHD_I32_HEVC

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd intra32x32 texture threshold for HEVC anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st intra32x32 texture threshold for HEVC anti-flicker.

VEPU2_ATF_TTHD1_H264

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	atf_tthd3 The 4th texture threshold for H.264 anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd2 The 3rd texture threshold for H.264 anti-flicker.

VEPU2_ATF_TTHD_I16_HEVC

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd intra16x16 texture threshold for HEVC anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st intra16x16 texture threshold for HEVC anti-flicker.

VEPU2_ATF_STHD0_H264

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_sthd_max Max (CME) SAD threshold for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_sthd_10 (CME) SAD threshold0 of texture interval1 for H.264 anti-flicker.

VEPU2_ATF_TTHD_P64_HEVC

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	atf_tthd1 The 2nd intra64x64 texture threshold for HEVC anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st inter64x64 texture threshold for HEVC anti-flicker.

VEPU2_ATF_STHD1_H264

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_sthd_20 (CME) SAD threshold0 of texture interval2 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_sthd_11 (CME) SAD threshold1 of texture interval1 for H.264 anti-flicker.

VEPU2_ATF_TTHD_P32_HEVC

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd intra32x32 texture threshold for HEVC anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st inter32x32 texture threshold for HEVC anti-flicker.

VEPU2_ATF_WGT0_H264

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

Bit	Attr	Reset Value	Description
24:16	RW	0x000	atf_wgt11 The 2nd weight in texture interval1 for H.264 anti-flicker.
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt10 The 1st weight in texture interval1 for H.264 anti-flicker.

VEPU2_ATF_TTHD_P16_HEVC

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atf_tthd1 The 2nd intra16x16 texture threshold for HEVC anti-flicker.
15:12	RO	0x0	reserved
11:0	RW	0x000	atf_tthd0 The 1st inter16x16 texture threshold for HEVC anti-flicker.

VEPU2_ATF_WGT1_H264

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	atf_wgt20 The 1st weight in texture interval2 for H.264 anti-flicker.
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt12 The 3rd weight in texture interval1 for H.264 anti-flicker.

VEPU2_ATF_WGT0_HEVC

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	atf_wgt_i32 HEVC intra32x32 anti-flicker weight.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_wgt_i16 HEVC intra16x16 anti-flicker weight.

VEPU2_ATF_WGT2_H264

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	atf_wgt30 The weight in texture interval3 for H.264 anti-flicker.
15:9	RO	0x00	reserved
8:0	RW	0x000	atf_wgt21 The 2nd weight in texture interval2 for H.264 anti-flicker.

VEPU2_ATF_WGT1_HEVC

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atf_wgt_p64 HEVC inter64x64 anti-flicker weight.
15:6	RO	0x000	reserved
5:0	RW	0x00	atf_wgt_p32 HEVC inter32x32 anti-flicker weight.

VEPU2_ATF_OFST0_H264

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:16	RW	0x0000	atf_ofst11 The 2nd offset in texture interval1 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_ofst10 The 1st offset in texture interval1 for H.264 anti-flicker.

VEPU2_ATF_WGT2_HEVC

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	atf_wgt_p16 HEVC inter16x16 anti-flicker weight.

VEPU2_ATF_OFST1_H264

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_ofst20 The 1st offset in texture interval2 for H.264 anti-flicker.
15:14	RO	0x0	reserved
13:0	RW	0x0000	atf_ofst12 The 3rd offset in texture interval1 for H.264 anti-flicker.

VEPU2_ATF_OFST2_H264

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	atf_ofst30 The offset in texture interval3 for H.264 anti-flicker.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	atf_ofst21 The 2nd offset in texture interval2 for H.264 anti-flicker.

VEPU2_IPRD_WGT_QP0_HEVC

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp0 Weight of SATD cost when QP is 0 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP1_HEVC

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp1 Weight of SATD cost when QP is 1 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP2_HEVC

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp2 Weight of SATD cost when QP is 2 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP3_HEVC

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp3 Weight of SATD cost when QP is 3 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP4_HEVC

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp4 Weight of SATD cost when QP is 4 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP5_HEVC

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp5 Weight of SATD cost when QP is 5 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP6_HEVC

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp6 Weight of SATD cost when QP is 6 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP7_HEVC

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp7 Weight of SATD cost when QP is 7 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP8_HEVC

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp8 Weight of SATD cost when QP is 8 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP9_HEVC

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp9 Weight of SATD cost when QP is 9 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP10_HEVC

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp10 Weight of SATD cost when QP is 10 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP11_HEVC

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp11 Weight of SATD cost when QP is 11 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP12_HEVC

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	wgt_qp12 Weight of SATD cost when QP is 12 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP13_HEVC

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp13 Weight of SATD cost when QP is 13 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP14_HEVC

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp14 Weight of SATD cost when QP is 14 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP15_HEVC

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp15 Weight of SATD cost when QP is 15 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP16_HEVC

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp16 Weight of SATD cost when QP is 16 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP17_HEVC

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp17 Weight of SATD cost when QP is 17 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP18_HEVC

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp18 Weight of SATD cost when QP is 18 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP19_HEVC

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp19 Weight of SATD cost when QP is 19 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP20_HEVC

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp20 Weight of SATD cost when QP is 20 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP21_HEVC

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp21 Weight of SATD cost when QP is 21 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP22_HEVC

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp2 Weight of SATD cost when QP is 2 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP23_HEVC

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp23 Weight of SATD cost when QP is 23 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP24_HEVC

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp24 Weight of SATD cost when QP is 24 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP25_HEVC

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	wgt_qp25 Weight of SATD cost when QP is 25 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP26_HEVC

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp26 Weight of SATD cost when QP is 26 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP27_HEVC

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp27 Weight of SATD cost when QP is 27 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP28_HEVC

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp28 Weight of SATD cost when QP is 28 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP29_HEVC

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp29 Weight of SATD cost when QP is 29 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP30_HEVC

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp30 Weight of SATD cost when QP is 30 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP31_HEVC

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp31 Weight of SATD cost when QP is 31 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP32_HEVC

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp32 Weight of SATD cost when QP is 32 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP33_HEVC

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp33 Weight of SATD cost when QP is 33 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP34_HEVC

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp34 Weight of SATD cost when QP is 34 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP35_HEVC

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp35 Weight of SATD cost when QP is 35 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP36_HEVC

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp36 Weight of SATD cost when QP is 36 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP37_HEVC

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp37 Weight of SATD cost when QP is 37 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP38_HEVC

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	wgt_qp38 Weight of SATD cost when QP is 38 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP39_HEVC

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp39 Weight of SATD cost when QP is 39 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP40_HEVC

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp40 Weight of SATD cost when QP is 40 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP41_HEVC

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp41 Weight of SATD cost when QP is 41 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP42_HEVC

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp42 Weight of SATD cost when QP is 42 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP43_HEVC

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp43 Weight of SATD cost when QP is 43 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP44_HEVC

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp44 Weight of SATD cost when QP is 44 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP45_HEVC

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp45 Weight of SATD cost when QP is 45 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP46_HEVC

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp46 Weight of SATD cost when QP is 46 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP47_HEVC

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp47 Weight of SATD cost when QP is 47 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP48_HEVC

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp48 Weight of SATD cost when QP is 48 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP49_HEVC

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp49 Weight of SATD cost when QP is 49 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP50_HEVC

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	wgt_qp50 Weight of SATD cost when QP is 50 for HEVC intra prediction.

VEPU2_IPRD_WGT_QP51_HEVC

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	wgt_qp51 Weight of SATD cost when QP is 51 for HEVC intra prediction.

VEPU2_RDO_WGTA_QP0_COMB

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 0.

VEPU2_RDO_WGTA_QP1_COMB

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp1_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 1.

VEPU2_RDO_WGTA_QP2_COMB

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp2_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 2.

VEPU2_RDO_WGTA_QP3_COMB

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp3_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 3.

VEPU2_RDO_WGTA_QP4_COMB

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp4_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 4.

VEPU2_RDO_WGTA_QP5_COMB

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp5_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 5.

VEPU2_RDO_WGTA_QP6_COMB

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp6_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 6.

VEPU2_RDO_WGTA_QP7_COMB

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp7_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 7.

VEPU2_RDO_WGTA_QP8_COMB

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp8_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 8.

VEPU2_RDO_WGTA_QP9_COMB

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 9.

VEPU2_RDO_WGTA_QP10_COMB

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp10_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 10.

VEPU2_RDO_WGTA_QP11_COMB

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp11_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 11.

VEPU2_RDO_WGTA_QP12_COMB

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp12_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 12.

VEPU2_RDO_WGTA_QP13_COMB

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp13_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 13.

VEPU2_RDO_WGTA_QP14_COMB

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp14_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 14.

VEPU2_RDO_WGTA_QP15_COMB

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp15_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 15.

VEPU2_RDO_WGTA_QP16_COMB

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp16_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 16.

VEPU2_RDO_WGTA_QP17_COMB

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp17_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 17.

VEPU2_RDO_WGTA_QP18_COMB

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp18_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 18.

VEPU2_RDO_WGTA_QP19_COMB

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp19_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 19.

VEPU2_RDO_WGTA_QP20_COMB

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp20_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 20.

VEPU2_RDO_WGTA_QP21_COMB

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp21_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 21.

VEPU2_RDO_WGTA_QP22_COMB

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp22_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 22.

VEPU2_RDO_WGTA_QP23_COMB

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp23_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 23.

VEPU2_RDO_WGTA_QP24_COMB

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp24_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 24.

VEPU2_RDO_WGTA_QP25_COMB

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp25_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 25.

VEPU2_RDO_WGTA_QP26_COMB

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp26_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 26.

VEPU2_RDO_WGTA_QP27_COMB

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp27_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 27.

VEPU2_RDO_WGTA_QP28_COMB

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp28_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 28.

VEPU2_RDO_WGTA_QP29_COMB

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp29_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 29.

VEPU2_RDO_WGTA_QP30_COMB

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp30_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 30.

VEPU2_RDO_WGTA_QP31_COMB

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp31_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 31.

VEPU2_RDO_WGTA_QP32_COMB

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp32_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 32.

VEPU2_RDO_WGTA_QP33_COMB

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp33_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 33.

VEPU2_RDO_WGTA_QP34_COMB

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp34_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 34.

VEPU2_RDO_WGTA_QP35_COMB

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp35_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 35.

VEPU2_RDO_WGTA_QP36_COMB

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp36_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 36.

VEPU2_RDO_WGTA_QP37_COMB

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp37_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 37.

VEPU2_RDO_WGTA_QP38_COMB

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp38_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 38.

VEPU2_RDO_WGTA_QP39_COMB

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp39_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 39.

VEPU2_RDO_WGTA_QP40_COMB

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 40.

VEPU2_RDO_WGTA_QP41_COMB

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp41_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 41.

VEPU2_RDO_WGTA_QP42_COMB

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp42_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 42.

VEPU2_RDO_WGTA_QP43_COMB

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp43_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 43.

VEPU2_RDO_WGTA_QP44_COMB

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp44_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 44.

VEPU2_RDO_WGTA_QP45_COMB

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp45_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 5.

VEPU2_RDO_WGTA_QP46_COMB

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp46_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 46.

VEPU2_RDO_WGTA_QP47_COMB

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp47_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 47.

VEPU2_RDO_WGTA_QP48_COMB

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp48_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 48.

VEPU2_RDO_WGTA_QP49_COMB

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 49.

VEPU2_RDO_WGTA_QP50_COMB

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp50_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 50.

VEPU2_RDO_WGTA_QP51_COMB

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp51_grpa Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 51.

VEPU2_RDO_WGTB_QP0_COMB

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp0_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 0.

VEPU2_RDO_WGTB_QP1_COMB

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp1_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 1.

VEPU2_RDO_WGTB_QP2_COMB

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp2_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 2.

VEPU2_RDO_WGTB_QP3_COMB

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp3_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 3.

VEPU2_RDO_WGTB_QP4_COMB

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp4_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 4.

VEPU2_RDO_WGTB_QP5_COMB

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp5_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 5.

VEPU2_RDO_WGTB_QP6_COMB

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp6_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 6.

VEPU2_RDO_WGTB_QP7_COMB

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp7_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 7.

VEPU2_RDO_WGTB_QP8_COMB

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp8_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 8.

VEPU2_RDO_WGTB_QP9_COMB

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp9_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 9.

VEPU2_RDO_WGTB_QP10_COMB

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp10_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 10.

VEPU2_RDO_WGTB_QP11_COMB

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp11_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 11.

VEPU2_RDO_WGTB_QP12_COMB

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp12_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 12.

VEPU2_RDO_WGTB_QP13_COMB

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp13_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 13.

VEPU2_RDO_WGTB_QP14_COMB

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp14_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 14.

VEPU2_RDO_WGTB_QP15_COMB

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp15_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 15.

VEPU2_RDO_WGTB_QP16_COMB

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp16_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 16.

VEPU2_RDO_WGTB_QP17_COMB

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp17_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 17.

VEPU2_RDO_WGTB_QP18_COMB

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp18_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 18.

VEPU2_RDO_WGTB_QP19_COMB

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp19_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 19.

VEPU2_RDO_WGTB_QP20_COMB

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp20_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 20.

VEPU2_RDO_WGTB_QP21_COMB

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp21_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 21.

VEPU2_RDO_WGTB_QP22_COMB

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp22_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 22.

VEPU2_RDO_WGTB_QP23_COMB

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp23_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 23.

VEPU2_RDO_WGTB_QP24_COMB

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp24_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 24.

VEPU2_RDO_WGTB_QP25_COMB

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp25_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 25.

VEPU2_RDO_WGTB_QP26_COMB

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp26_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 26.

VEPU2_RDO_WGTB_QP27_COMB

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp27_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 27.

VEPU2_RDO_WGTB_QP28_COMB

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp28_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 28.

VEPU2_RDO_WGTB_QP29_COMB

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp29_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 29.

VEPU2_RDO_WGTB_QP30_COMB

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp30_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 30.

VEPU2_RDO_WGTB_QP31_COMB

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp31_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 31.

VEPU2_RDO_WGTB_QP32_COMB

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp32_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 32.

VEPU2_RDO_WGTB_QP33_COMB

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp33_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 3.

VEPU2_RDO_WGTB_QP34_COMB

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp34_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 34.

VEPU2_RDO_WGTB_QP35_COMB

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp35_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 35.

VEPU2_RDO_WGTB_QP36_COMB

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp36_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 36.

VEPU2_RDO_WGTB_QP37_COMB

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp37_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 37.

VEPU2_RDO_WGTB_QP38_COMB

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp38_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 38.

VEPU2_RDO_WGTB_QP39_COMB

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp39_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 39.

VEPU2_RDO_WGTB_QP40_COMB

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp40_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 40.

VEPU2_RDO_WGTB_QP41_COMB

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp41_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 41.

VEPU2_RDO_WGTB_QP42_COMB

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp42_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 42.

VEPU2_RDO_WGTB_QP43_COMB

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp43_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 43.

VEPU2_RDO_WGTB_QP44_COMB

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp44_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 44.

VEPU2_RDO_WGTB_QP45_COMB

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp45_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 45.

VEPU2_RDO_WGTB_QP46_COMB

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp46_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 46.

VEPU2_RDO_WGTB_QP47_COMB

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp47_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 47.

VEPU2_RDO_WGTB_QP48_COMB

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp48_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 48.

VEPU2_RDO_WGTB_QP49_COMB

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp49_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 49.

VEPU2_RDO_WGTB_QP50_COMB

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_qp50_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 50.

VEPU2_RDO_WGTB_QP51_COMB

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_qp51_grpb Weight of gourp B for HEVC and H.264 RDO mode decision when QP is 51.

VEPU2_MADI_CFG

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	madi_thd Texture threshold for madi statistics.
15:1	RO	0x0000	reserved
0	RW	0x0	madi_mode MADI generation mode for CU32 and CU64. 1'h0: Follow 32x32 and 64x64 MADI functions. 1'h1: Calculated by the mean of corresponding CU16 MADIs.

VEPU2_AQ_TTHD0

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd3 Texture threshold3 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd2 Texture threshold2 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd1 Texture threshold1 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd0 Texture threshold0 for adaptive QP adjustment.

VEPU2_AQ_TTHD1

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd7 Texture threshold7 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd6 Texture threshold6 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd5 Texture threshold5 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd4 Texture threshold4 for adaptive QP adjustment.

VEPU2_AQ_TTHD2

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd11 Texture threshold7 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd10 Texture threshold10 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd9 Texture threshold9 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd8 Texture threshold8 for adaptive QP adjustment.

VEPU2_AQ_TTHD3

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd15 Texture threshold15 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd14 Texture threshold14 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd13 Texture threshold13 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd12 Texture threshold12 for adaptive QP adjustment.

VEPU2_AQ_STP0

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_2t3 QP adjust step when current texture strength >= aq_tthd2 and < aq_tthd3.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_1t2 QP adjust step when current texture strength >= aq_tthd1 and < aq_tthd2.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_0t1 QP adjust step when current texture strength >= aq_tthd0 and < aq_tthd1.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_s0 QP adjust step when current texture strength < aq_tthd0.

VEPU2_AQ_STP1

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_6t7 QP adjust step when current texture strength >= aq_tthd6 and < aq_tthd7.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_5t6 QP adjust step when current texture strength >= aq_tthd5 and < aq_tthd6.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x00	aq_stp_4t5 QP adjust step when current texture strength >= aq_tthd4 and < aq_tthd5.
7:6	RO	0x0	reserved
5:0	RW	0x00	ap_stp_3t4 QP adjust step when current texture strength >= aq_tthd3 and < aq_tthd4.

VEPU2_AQ_STP2

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_11t12 QP adjust step when current texture strength > aq_tthd11 and <= aq_tthd12.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_10t11 QP adjust step when current texture strength > aq_tthd10 and <= aq_tthd11.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_9t10 QP adjust step when current texture strength > aq_tthd9 and <= aq_tthd10.
7:6	RO	0x0	reserved
5:0	RW	0x00	ap_stp_8t9 QP adjust step when current texture strength > aq_tthd8 and <= aq_tthd9.

VEPU2_AQ_STP3

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x00	aq_stp_b15 QP adjust step when current texture strength > aq_tthd15.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_14t15 QP adjust step when current texture strength > aq_tthd14 and <= aq_tthd15.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_13t14 QP adjust step when current texture strength > aq_tthd13 and <= aq_tthd14.
7:6	RO	0x0	reserved
5:0	RW	0x00	ap_stp_12t13 QP adjust step when current texture strength > aq_tthd12 and <= aq_tthd13.

VEPU2_RME_MVD_PNSH_H264

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	mvd_pnsh_hthd High threshold of the MVs which should be punished.
23:20	RW	0x0	mvd_pnsh_lthd Low threshold of the MVs which should be punished.
19:6	RW	0x0000	mvd_pnsh_cnst MVD cost punishment constant.
5:1	RW	0x00	mvd_pnsh_coef MVD punishement coefficiency.
0	RW	0x0	mvd_pnsh_e MVD cost punishment enable.

VEPU2_ATR1_THD0_H264

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	atr1_thd1 The 2nd threshold for H.264 anti-ringing-noise of group1.
15:12	RO	0x0	reserved
11:0	RW	0x000	atr1_thd0 The 1st threshold for H.264 anti-ringing-noise of group1.

VEPU2_ATR1_THD1_H264

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	atr1_thd2 The 3rd threshold for H.264 anti-ringing-noise of group1.

VEPU2_PREI_DIF_IDX00L_HEVC

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x0e34c2ca	dif_idx00_low Low 30 bits of hevc pre-intra difference idx00, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX00H_HEVC

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x074083c9	dif_idx00_high High 30 bits of hevc pre-intra difference idx00, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX01L_HEVC

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x061c824a	dif_idx01_low Low 30 bits of hevc pre-intra difference idx01, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX01H_HEVC

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x0d10c14b	dif_idx01_high High 30 bits of hevc pre-intra difference idx01, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX02L_HEVC

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x0e3d0452	dif_idx02_low Low 30 bits of hevc pre-intra difference idx02, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX02H_HEVC

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x15314353	dif_idx02_high High 30 bits of hevc pre-intra difference idx02, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX03L_HEVC

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x165544d2	dif_idx03_low Low 30 bits of hevc pre-intra difference idx03, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX03H_HEVC

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x0f6105d1	dif_idx03_high High 30 bits of hevc pre-intra difference idx03, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX04L_HEVC

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x165d8699	dif_idx04_low Low 30 bits of hevc pre-intra difference idx04, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX04H_HEVC

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x1d51c55b	dif_idx04_high High 30 bits of hevc pre-intra difference idx04, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX05L_HEVC

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x1e75c69b	dif_idx05_low Low 30 bits of hevc pre-intra difference idx05, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX05H_HEVC

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x178187d9	dif_idx05_high High 30 bits of hevc pre-intra difference idx05, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX06L_HEVC

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x1e7e0862	dif_idx06_low Low 30 bits of hevc pre-intra difference idx06, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX06H_HEVC

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x04703742	dif_idx06_high High 30 bits of hevc pre-intra difference idx06, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX07L_HEVC

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x051030a2	dif_idx07_low Low 30 bits of hevc pre-intra difference idx07, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX07H_HEVC

Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x1f1e01a1	dif_idx07_high High 30 bits of hevc pre-intra difference idx07, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX08L_HEVC

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x0689268a	dif_idx08_low Low 30 bits of hevc pre-intra difference idx08, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX08H_HEVC

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x1809e58e	dif_idx08_high High 30 bits of hevc pre-intra difference idx08, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX09L_HEVC

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx09_low Low 30 bits of hevc pre-intra difference idx09, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX09H_HEVC

Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx09_high High 30 bits of hevc pre-intra difference idx09, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX10L_HEVC

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx10_low Low 30 bits of hevc pre-intra difference idx10, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX10H_HEVC

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx10_high High 30 bits of hevc pre-intra difference idx10, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX11L_HEVC

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx11_low Low 30 bits of hevc pre-intra difference idx11, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX11H_HEVC

Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx11_high High 30 bits of hevc pre-intra difference idx11, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX12L_HEVC

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx12_low Low 30 bits of hevc pre-intra difference idx12, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX12H_HEVC

Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx12_high High 30 bits of hevc pre-intra difference idx12, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX13L_HEVC

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx13_low Low 30 bits of hevc pre-intra difference idx13, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX13H_HEVC

Address: Operational Base + offset (0x037C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx13_high High 30 bits of hevc pre-intra difference idx13, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX14L_HEVC

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx14_low Low 30 bits of hevc pre-intra difference idx14, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX14H_HEVC

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx14_high High 30 bits of hevc pre-intra difference idx14, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX15L_HEVC

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx15_low Low 30 bits of hevc pre-intra difference idx15, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX15H_HEVC

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx15_high High 30 bits of hevc pre-intra difference idx15, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX16L_HEVC

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx16_low Low 30 bits of hevc pre-intra difference idx16, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_PREI_DIF_IDX16H_HEVC

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dif_idx16_high High 30 bits of hevc pre-intra difference idx16, include 5 sets of pre-intra difference, and 6 bits of per set.

VEPU2_RDO_CKG_H264

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intra4_ckg H264 RDO intra4 clock-gating enable.
8	RW	0x0	intra8_ckg H264 RDO intra8 clock-gating enable.
7	RW	0x0	inter_pred_ckg H264 RDO inter prediction clock-gating enable.
6	RW	0x0	inter_ctrl_ckg H264 RDO inter control clock-gating enable.
5	RW	0x0	inter_mode_ckg H264 RDO inter mode clock-gating enable.
4	RW	0x0	4x4_0_bits_ckg H264 RDO 4x4_0_bits clock-gating enable.
3	RW	0x0	4x4_1_bits_ckg H264 RDO 4x4_1_bits clock-gating enable.
2	RW	0x0	8x8_bits_ckg H264 RDO 8x8_bits clock-gating enable.
1	RW	0x0	tq4_ckg H264 RDO tq4 clock-gating enable.
0	RW	0x0	tq8_ckg H264 RDO tq8 clock-gating enable.

VEPU2_RDO_CKG_HEVC

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	inter_pred_ckg HEVC RDO inter prediction clock-gating enable.
23	RW	0x0	intra4_ckg HEVC RDO intra4 clock-gating enable.
22	RW	0x0	intra8_ckg HEVC RDO intra8 clock-gating enable.

Bit	Attr	Reset Value	Description
21	RW	0x0	intra16_ckg HEVC RDO intra32 clock-gating enable.
20	RW	0x0	intra32_ckg HEVC RDO intra32 clock-gating enable.
19	RW	0x0	cabac4_ckg HEVC RDO cabac4 clock-gating enable.
18	RW	0x0	t4_ckg HEVC RDO cu4 tranform clock-gating enable.
17	RW	0x0	q4_ckg HEVC RDO cu4 quantization clock-gating enable.
16	RW	0x0	iqit4_ckg HEVC RDO iqit4 clock-gating enable.
15	RW	0x0	recon4_ckg HEVC RDO recon4 clock-gating enable.
14	RW	0x0	cabac8_ckg HEVC RDO cabac8 clock-gating enable.
13	RW	0x0	t8_ckg HEVC RDO cu8 tranform clock-gating enable.
12	RW	0x0	q8_ckg HEVC RDO cu8 quantization clock-gating enable.
11	RW	0x0	iqit8_ckg HEVC RDO iqit8 clock-gating enable.
10	RW	0x0	recon8_ckg HEVC RDO recon8 clock-gating enable.
9	RW	0x0	cabac16_ckg HEVC RDO cabac16 clock-gating enable.
8	RW	0x0	t16_ckg HEVC RDO cu16 tranform clock-gating enable.
7	RW	0x0	q16_ckg HEVC RDO cu16 quantization clock-gating enable.
6	RW	0x0	iqit16_ckg HEVC RDO iqit16 clock-gating enable.

Bit	Attr	Reset Value	Description
5	RW	0x0	recon16_ckg HEVC RDO recon16 clock-gating enable.
4	RW	0x0	cabac32_ckg HEVC RDO cabac32 clock-gating enable.
3	RW	0x0	t32_ckg HEVC RDO cu32 tranform clock-gating enable.
2	RW	0x0	q32_ckg HEVC RDO cu32 quantization clock-gating enable.
1	RW	0x0	iqit32_ckg HEVC RDO iqit32 clock-gating enable.
0	RW	0x0	recon32_ckg HEVC RDO recon32 clock-gating enable.

VEPU2_I16_SOBEL_T_HEVC

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	intra_l16_sobel_t1 HEVC intra cost16 adjust theshold1.
15:12	RO	0x0	reserved
11:0	RW	0x000	intra_l16_sobel_t0 HEVC intra cost16 adjust theshold0.

VEPU2_I16_SOBEL_A_00_HEVC

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	intra_l16_sobel_a0_qp4 a0 value when qp = 42/43;
23:18	RW	0x00	intra_l16_sobel_a0_qp3 a0 value when qp = 40/41;

Bit	Attr	Reset Value	Description
17:12	RW	0x00	intra_l16_sobel_a0_qp2 a0 value when qp = 38/39;
11:6	RW	0x00	intra_l16_sobel_a0_qp1 a0 value when qp = 36/37;
5:0	RW	0x00	intra_l16_sobel_a0_qp0 a0 value when qp<36;

VEPU2_I16_SOBEL_A_01_HEVC

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x00	intra_l16_sobel_a0_qp8 a0 value when qp = 50/51;
17:12	RW	0x00	intra_l16_sobel_a0_qp7 a0 value when qp = 48/49;
11:6	RW	0x00	intra_l16_sobel_a0_qp6 a0 value when qp = 46/47;
5:0	RW	0x00	intra_l16_sobel_a0_qp5 a0 value when qp = 44/45;

VEPU2_I16_SOBEL_B_00_HEVC

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_b0_qp1
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_b0_qp0

VEPU2_I16_SOBEL_B_01_HEVC

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_b0_qp3
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_b0_qp2

VEPU2_I16_SOBEL_B_02_HEVC

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_b0_qp5
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_b0_qp4

VEPU2_I16_SOBEL_B_03_HEVC

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_b0_qp7
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_b0_qp6

VEPU2_I16_SOBEL_B_04_HEVC

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	intra_l16_sobel_b0_qp8

VEPU2_I16_SOBEL_C_00_HEVC

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	intra_l16_sobel_c0_qp4
23:18	RW	0x00	intra_l16_sobel_c0_qp3
17:12	RW	0x00	intra_l16_sobel_c0_qp2
11:6	RW	0x00	intra_l16_sobel_c0_qp1
5:0	RW	0x00	intra_l16_sobel_c0_qp0

VEPU2_I16_SOBEL_C_01_HEVC

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x00	intra_l16_sobel_c0_qp8
17:13	RO	0x00	reserved
12	RW	0x0	intra_l16_sobel_c0_qp7
11:6	RW	0x00	intra_l16_sobel_c0_qp6

Bit	Attr	Reset Value	Description
5:0	RW	0x00	intra_l16_sobel_c0_qp5

VEPU2_I16_SOBEL_D_00_HEVC

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_d0_qp1
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_d0_qp0

VEPU2_I16_SOBEL_D_01_HEVC

Address: Operational Base + offset (0x043C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_d0_qp3
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_d0_qp2

VEPU2_I16_SOBEL_D_02_HEVC

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_d0_qp5

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_d0_qp4

VEPU2_I16_SOBEL_D_03_HEVC

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l16_sobel_d0_qp7
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l16_sobel_d0_qp6

VEPU2_I16_SOBEL_D_04_HEVC

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	intra_l16_sobel_d0_qp8

VEPU2_I16_SOBEL_E_00_HEVC

Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp0_low

VEPU2_I16_SOBEL_E_01_HEVC

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp0_high

VEPU2_I16_SOBEL_E_02_HEVC

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp1_low

VEPU2_I16_SOBEL_E_03_HEVC

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp1_high

VEPU2_I16_SOBEL_E_04_HEVC

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp2_low

VEPU2_I16_SOBEL_E_05_HEVC

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp2_high

VEPU2_I16_SOBEL_E_06_HEVC

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp3_low

VEPU2_I16_SOBEL_E_07_HEVC

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp3_high

VEPU2_I16_SOBEL_E_08_HEVC

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp4_low

VEPU2_I16_SOBEL_E_09_HEVC

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp4_high

VEPU2_I16_SOBEL_E_10_HEVC

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp5_low

VEPU2_I16_SOBEL_E_11_HEVC

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp5_high

VEPU2_I16_SOBEL_E_12_HEVC

Address: Operational Base + offset (0x047C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp6_low

VEPU2_I16_SOBEL_E_13_HEVC

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp6_high

VEPU2_I16_SOBEL_E_14_HEVC

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp7_low

VEPU2_I16_SOBEL_E_15_HEVC

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	intra_l16_sobel_e0_qp7_high

VEPU2_I16_SOBEL_E_16_HEVC

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l16_sobel_e0_qp8_low

VEPU2_I16_SOBEL_E_17_HEVC

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	intra_l16_sobel_e0_qp8_high

VEPU2_I32_SOBEL_T_00_HEVC

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	intra_l32_sobel_t3
15:12	RO	0x0	reserved
11:0	RW	0x000	intra_l32_sobel_t2

VEPU2_I32_SOBEL_T_01_HEVC

Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	intra_l32_sobel_t4

VEPU2_I32_SOBEL_T_02_HEVC

Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	intra_l32_sobel_t6
15:12	RO	0x0	reserved
11:0	RW	0x000	intra_l32_sobel_t5

VEPU2_I32_SOBEL_A_HEVC

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	intra_l32_sobel_a1_qp4
23:18	RW	0x00	intra_l32_sobel_a1_qp3
17:12	RW	0x00	intra_l32_sobel_a1_qp2
11:6	RW	0x00	intra_l32_sobel_a1_qp1
5:0	RW	0x00	intra_l32_sobel_a1_qp0

VEPU2_I32_SOBEL_B_00_HEVC

Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l32_sobel_b1_qp1
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l32_sobel_b1_qp0

VEPU2_I32_SOBEL_B_01_HEVC

Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l32_sobel_b1_qp3
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l32_sobel_b1_qp2

VEPU2_I32_SOBEL_B_02_HEVC

Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	intra_l32_sobel_b1_qp4

VEPU2_I32_SOBEL_C_HEVC

Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x00	intra_l32_sobel_c1_qp4
23:18	RW	0x00	intra_l32_sobel_c1_qp3
17:12	RW	0x00	intra_l32_sobel_c1_qp2
11:6	RW	0x00	intra_l32_sobel_c1_qp1
5:0	RW	0x00	intra_l32_sobel_c1_qp0

VEPU2_I32_SOBEL_D_00_HEVC

Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l32_sobel_d1_qp2
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l32_sobel_d1_qp0

VEPU2_I32_SOBEL_D_01_HEVC

Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	intra_l32_sobel_d1_qp3
15	RO	0x0	reserved
14:0	RW	0x0000	intra_l32_sobel_d1_qp2

VEPU2_I32_SOBEL_D_02_HEVC

Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	intra_l32_sobel_d1_qp4

VEPU2_I32_SOBEL_E_00_HEVC

Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l32_sobel_e1_qp0_low

VEPU2_I32_SOBEL_E_01_HEVC

Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	intra_l32_sobel_e1_qp0_high

VEPU2_I32_SOBEL_E_02_HEVC

Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l32_sobel_e1_qp1_low

VEPU2_I32_SOBEL_E_03_HEVC

Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x000	intra_l32_sobel_e1_qp1_high

VEPU2_I32_SOBEL_E_04_HEVC

Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l32_sobel_e1_qp2_low

VEPU2_I32_SOBEL_E_05_HEVC

Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	intra_l32_sobel_e1_qp2_high

VEPU2_I32_SOBEL_E_06_HEVC

Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l32_sobel_e1_qp3_low

VEPU2_I32_SOBEL_E_07_HEVC

Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	intra_l32_sobel_e1_qp3_high

VEPU2_I32_SOBEL_E_08_HEVC

Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_l32_sobel_e1_qp4_low

VEPU2_I32_SOBEL_E_09_HEVC

Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	intra_l32_sobel_e1_qp4_high

10.6 Application Notes

10.6.1 MMU Config Flow

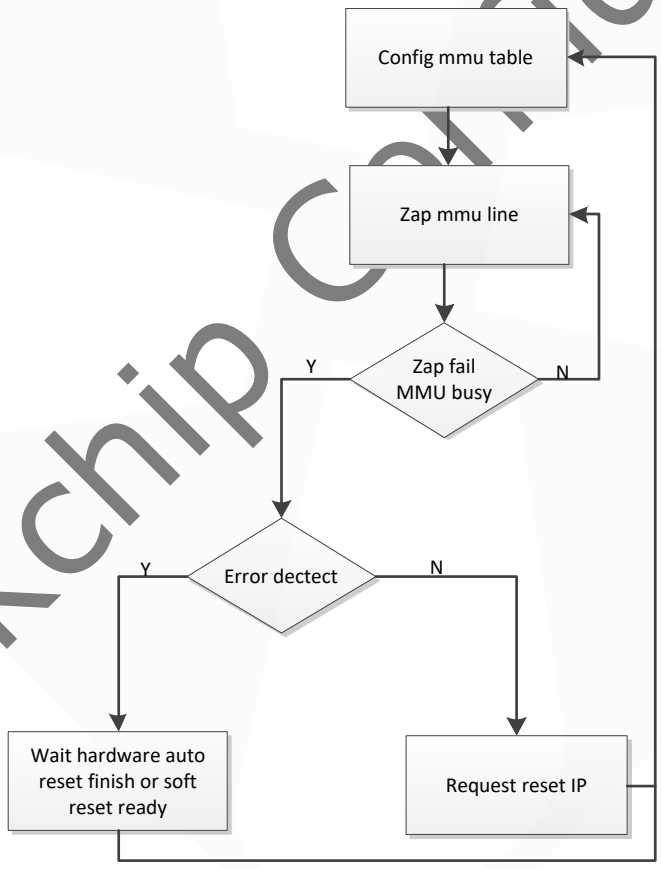


Fig. 10-12 MMU config flow

1. Prepare mmu table to ddr and config DTE address before begin to decoder.
2. If the mmu table have been changed, you will zap one mmu line.
3. If you zap successed, you can continus to zap next line.
4. If you zap fail, maybe some error happened, then you should check if there any error happen when decoding.
5. If some error happen, you should wait reset finish, and then re-start mmu config.

6. If don’t have any error find, it will still need to reset, and then re-start mmu config.

10.6.2 VDPU121 decoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. The decoder can support ref buffer mode or cacheable mode, but they can’t be both enabled. We can config the swreg57[28],swreg57[29] to enable cache and config the swreg65 to control the ref buffer.
3. You should config VDPU_SWREG57[0] as 1’b1 to enable video decoder. And config VDPU_SWREG41[0] as 1’b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG41[4] as 1’b1 and then config VDPU_SWREG57[0] as 1’b1 to enable decoder and pp.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

10.6.3 VDPU346 decoder Configuration Flow

1. Prepare the data in the DDR.
2. Set the H265 general system configuration. such as working mode in RKVDEC.swreg9, in/out endian in RKVDEC.swreg8.
3. Set the picture parameters with RKVDEC.swreg0~ RKVDEC.swreg63.
4. Set the input and output data base address and H265 reference configuration with RKVDEC.swreg64~RKVDEC.swreg204.
5. If CABAC error detection is desired, set the RKVDEC.swreg21 to enable the corresponding error detection.
6. Set the interrupt configuration with RKVDEC.swreg11 and start the H265 with RKVDEC.swreg10.
7. Wait for the frame interrupt, and then get the processed results in the target DDR.
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

10.6.4 VDPU346 Link table Pointer mode configuration flow

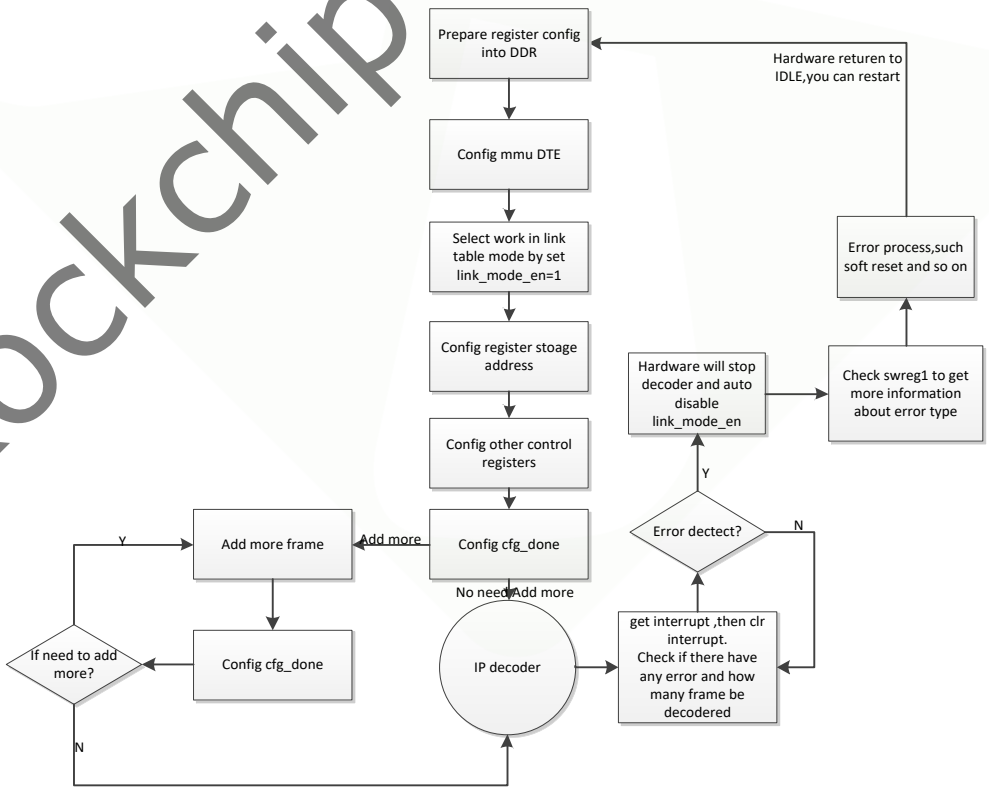


Fig. 10-13 Link table Pointer mode work flow

1. Prepare all the register config value into DDR.
2. Config mmu DTE and enable mmu before config link table mode.
3. Config link_mode_irq and other link table mode register. The register is from link_tale_swreg0~link_table_swreg2.
4. Config config_done(set link_table_swreg3[0]=1'b1) to make the link table register configuration effect, after that,hardware will begin to decoder frame by frame.
5. If you need to add more frame, you can use superaddition mode, you can add more frame when decoder at any status.
6. If all config be rdy, you should enable the working flag by config link_mode_en (link_table_swreg6[0]) to 1.
7. If all the frame be decodered, the hardware will hold the working status wait user to process, you can add more frame or set link_mode_en=0(need to set config_done=1'b1) to finish link table mode.
8. When you get interrupt, at first, you should clear the irq, and then, goto check if there have any error by check link_table_swreg4[31]=1'b1 or not. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from normal register swreg225.
9. When you get interrupt, if there doesn't have any error, you may be to check the frame number which have been decoded.
10. Please note that: Any link table register be config, you need to config swreg3[0]=1'b1 to make it effective.

10.6.5 VDPU720 JPEG decoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used.
3. You should config VDPU720_SWREG1[0] as 1'b1 to enable JPEG decoder.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

10.6.6 VEPU121 JPEG encoder Configuration flow

1. Prepare the encoder data in the DDR memory
2. Config all the registers will be used. And please notice that which be list as follows:
   - For encoder: We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac_table data. And the register VEPU_SWREG0~31 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set VEPU_SWREG103[0] to 1'b0 and VEPU_SWREG103[5:4] to 2'b10(select JPEG mode).
3. VEPU_SWREG103[0] set to 1'b1 to enable encoder.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~5 to start a new frame decoder or encoder.

10.6.7 VEPU540 Layer2 Register Access

User can access VEPU Layer2 registers through VEPU_L2CFG_ADDR(0x03f0), VEPU_L2CFG_WDATA(0x03f4) and VEPU_L2CFG_RDATA(0x03f8) in Layer1.

Example1: write "DATAx" into layer2 address "ADDRx"

- Write(VEPU_L2CFG_ADDR, "ADDRx")
- Write(VEPU_L2CFG_WDATA, "DATAx")

Example2: read back "DATAx" from layer2 register "ADDRx"

- Write(VEPU_L2CFG_ADDR, "ADDRx")
- Read(VEPU_L2CFG_RDATA, "DATAx")

To increase configuration speed, VEPU also support "burst mode" which auto increase VEPU_L2CFG_ADDR after write to VEPU_L2CFG_WDATA or read L2CFG_RDATA if VEPU_L2CFG_WDATA.burst_mode is 1.

Example3: write DATA[0~3] into layer2 address "ADDRx", "ADDRx+4", "ADDRx+8",

"ADDRx+12" continuously.

- Write(VEPU_L2CFG_ADDR, "ADDRx"|32'h1)
- Write(VEPU_L2CFG_WDATA, "DATA[0]")
- Write(VEPU_L2CFG_WDATA, "DATA[1]")
- Write(VEPU_L2CFG_WDATA, "DATA[2]")
- Write(VEPU_L2CFG_WDATA, "DATA[3]")

Example4: read 4 "DATA[0~4]" from layer2 registers with the address of "ADDRx", "ADDRx+4", "ADDRx+8" and "ADDRx+12" continuously.

- Write(VEPU_L2CFG_ADDR, "ADDRx"|32'h1)
- Read(VEPU_L2CFG_RDATA, "DATA[0]")
- Read(VEPU_L2CFG_RDATA, "DATA[1]")
- Read(VEPU_L2CFG_RDATA, "DATA[2]")
- Read(VEPU_L2CFG_RDATA, "DATA[3]")

10.6.8 VEPU540 Buffer Allocation

User should allocates the following buffers and informs VEPU before the corresponding frame encoding starts.

- Video source buffer
- (ROI) block level configuration buffer
- Reference frame buffer
- Current frame buffer
- Collocated MV buffer
- Current MV buffer
- Down-sampled reference frame buffer
- Down-sampled current frame buffer
- Motion information buffer
- Bitstream buffer

10.6.8.1 Video Source Buffer

Depending on different video source format, there're up to 3 buffers should be configured.
When video source format is BGRA8888, RGB888, RGB565, YUYV422 or UYVY422, only one buffer should be allocated and LAYER1.VEPU_ADR_SRC0(0x0118) should be set to the buffer start address.
When video source format is arm AFBC (YUV420 or YUV422), LAYER1.VEPU_ADR_SRC0 should be set to the start address of "AFBC header portion". LAYER1.VEPU_ADR_SRC1 should be set to the address of which the "AFBC body portion" offset base on (layer1.ADR_SRC0 and layer1.ADR_SRC1 are the same in most cases).
When video source format is YUV420 or YUV 422 semi-planar, LAYER1.VEPU_ADR_SRC0 should be set to the LUMA component start address, LAYER1.VEPU_ADR_SRC1 should be set to the CHROMA component start address.
Otherwise (YUV420 or YUV422 planar), LAYER1.VEPU_ADR_SRC0 should be set to the Y component start address, LAYER1.ADR_SRC1 should be set to the U component start address, and LAYER1.VEPU_ADR_SRC2 should be set to the V component start address.

10.6.8.2 Block Level Configure Buffer

This buffer should be allocated and configured when LAYER1.VEPU_ENC_PIC.roi_en is 1.
The size of block level configure buffer is:
((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+8)/8) x
((LAYER1.VEPU_ENC_RSL.pic_hd8_m1+8)/8) x 32Bytes.

10.6.8.3 Current And Reference Frame Buffer

Reference frame buffer and current frame buffer store the reconstructed frame data for motion estimation. Because of that frame buffer compression is implemented, each buffer has head portion and body portion. LAYER1.VEPU_ADR_RFPW_H and LAYER1.VEPU_ADR_RFPW_B should be set to the head portion and body portion start address of current frame buffer separately. LAYER1.VEPU_ADR_RFPR_H and LAYER1.VEPU_ADR_RFPR_B should be set to the header portion and body portion start

address of reference frame buffer.
The size of head portion of current and reference frame buffer is:
(((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+2)/2) x
((LAYER1.VEPU_ENC_RSL.pic_hd8_m1+1)x2) +15)/16 x 16Bytes.
The size of body portion of current and reference frame buffer is:
((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+2)/2) x
((LAYER1.VEPU_ENC_RSL.pic_hd8_m1+1)x2) x 96Bytes.
Note that the head and body start address should be 4K byte aligned.

10.6.8.4 Col-Mv Buffer And Cur-Mv buffer

Col-Mv buffer and Cur-Mv buffer stores the col-mv information for HEVC encoding.
When LAYER1.VEPU_ME_CFG.colmv_stor is 1, the LAYER1.VEPU_ADR_CMVW should be set to the start address of Cur-Mv buffer. VEPU will store the col-mv information of current encoding frame into Cur-Mv buffer.
When LAYER1.VEPU_ME_CFG.colmv_load is 1, the LAYER1.VEPU_ADR_CMVR should be set to the start address of Col-Mv buffer. VEPU will load the col-mv information for MVP generation.
The size of Col-Mv buffer and Cur-Mv buffer is calculated by the following function:
((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+8)/8) x
((LAYER1.VEPU_ENC_RSL.pic_hd8_m1+8)/8) x 32Bytes.
Note that the start address of col-mv and cur-mv buffer should be 1K byte aligned.

10.6.8.5 Down-sampled Current and Reference Frame Buffer

Down-sampled frame buffer is for VEPU coarse motion estimation. If current frame will be referred in subsequent encoding, the down-sampled current frame buffer should be allocated and set the start address to LAYER1.VEPU_ADR_DSPW. If current frame is P frame, a reference frame buffer should be selected and set the start address to LAYER1.VEPU_ADR_DSPR.
The size of down-sampled frame buffer is:
((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+8)/8) x
(LAYER1.VEPU_ENC_RSL.pic_hd8_m1+2)/2) x 64Bytes.
Note that the start address of down-sampled frame buffer should be 1KB aligned.

10.6.8.6 Motion Information Buffer

When LAYER1.VEPU_ENC_PIC.mei_stor is 1, the motion information buffer should be allocated and set the start address to LAYER1.VEPU_ADR_MEIW. VEPU stores best motion vector and corresponding SAD into this buffer just for user extended extraction.
The size of motion information buffer is:
((LAYER1.VEPU_ENC_RSL.pic_wd8_m1+32)/32) x
(LAYER1.VEPU_ENC_RSL.pic_hd8_m1+1)x2) x 64Bytes.

10.6.8.7 Bit Stream Buffer

VEPU stores the encoding result (bit stream) into bit stream buffer.
There are 4 address pointers for one bit stream buffer management:

- LAYER1.VEPU_ADR_BSBT: buffer top address, not included.
- LAYER1.VEPU_ADR_BSBB: buffer bottom address, included.
- LAYER1.VEPU_ADR_BSBR: buffer read address to avoid overlap.
- LAYER1.VEPU_ADR_BSBW: buffer write start address.

Two types of buffer management strategy can be implemented by configuring the four address pointers: single buffer and cyclic buffer management.
Single buffer management allocates a new buffer for each frame while cyclic buffer management allocates a shared cyclic buffer for all encoding frames.
Interrupt LAYER1.VEPU_INT_STUS.bs_ovflr will assert when write address meets read address (which indicates buffer is full) and encoding process is paused. Driver should allocated a new buffer to continue current frame encoding by setting new values to the four address pointers or change buffer read address (read out the bitstream before that), and then the encoding process will continue.

Note that LAYER1.VEPU_ADR_BSBW must be configured after the other 3 address pointers.

10.6.8.8 Cur-LPF Row Buffer and Left-LPF Row Buffer

Cur-LPF row buffer and Left-LPF row buffer stores the data between tiles for loop-filter and sao when the current picture is partitioned into several tiles for HEVC coding. If current tile is not the right tile of the picture, the cur-LPF row buffer should be allocated and set the start address to LAYER1.VEPU_ADR_LPFW. If the current tile is not the left tile of the picture, the left-LPF row buffer should be selected and set the start address to LAYER1.VEPU_ADR_LPFR.

The size of Cur-LPF Row buffer and Left-LPF Row buffer is:
(LAYER1.VEPU_TILE_CFG_HEVC.tile_h_m1+1) x 128 x 16Byte.

10.6.9 VEPU540 Link Table Mode

VEPU540 supports a batch process mode named "link table mode". It will increase the interaction efficiency between hardware and software. CPU can stores the configuration for several frames in DDR before encoding or add new frames to be encoded when VEPU is processing the previous one. This will save the time of interrupt response and register configuration and let VEPU and software process in parallel.

The struct contains one frame configuration in DDR is called node. It contains the LAYER1 register configuration and status from address 0x0030 to 0x002C. VEPU will load the node and replace corresponding LAYER1 registers automatically.

Note that only the registers between LAYER1 0x0030 to 0x002C can be re-configured in link table mode, other configurations can not be changed.

When LAYER1. VEPU_INT_EN.lkt_done_en is 1, the interrupt of LAYER1.VEPU_INT_STA.lkt_done_sta will assert after each frame encoding whose LAYER1.VEPU_ENC_PIC.node_int is 1. User can set dedicated frame interrupt such as the last node of link table. LAYER1.VEPU_ST_LKT.fnum_int contains the number of frames have been encoded when interrupt is assert.

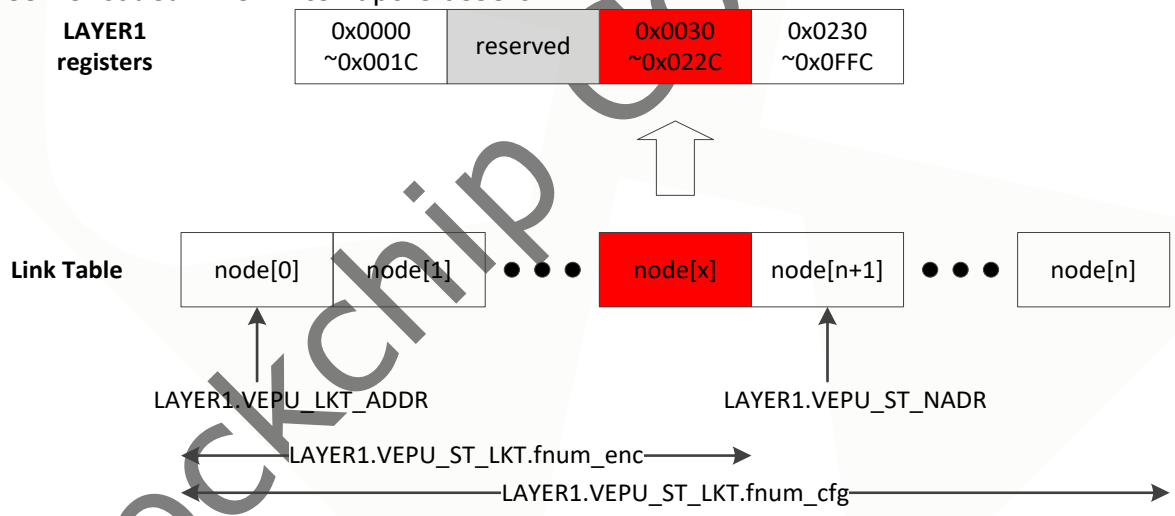


Fig. 10-14 VEPU Link Table Introduction

10.6.10 VEPU540 ROI

User can adjust QP and inter/intra selection base on 16x16 block and stores the configurations in block level configuration buffer. Each 16x16 block has 16 bits ROI configuration struct as the table listed below.

Table 10-17 ROI Configuration Structure

Bit	Field	Description
15	qp_mode	QP adjustment mode 0: absolute QP 1: relative QP

Bit	Field	Description
14:8	qp_value	QP adjustment value This field is the absolute QP when qp_mode is 0, otherwise it's the relative QP base on corresponding 16x16 block's QP
7	amap_en	Area map enable
6:4	amap_idx	Area map index. QP clip is implemented base on area map index, each map index has its dedicated threshold. ROI configuration mapping will use amap_idx to arbitrate the final configure when CU size is bigger than 16x16. Bigger amap_idx has higher priority.
3:1	reserved	Reserved
0	force_intra	Force intra encoding

The configuration structures of different blocks are stored in the order of raster scanning within a frame.

10.6.11 VEPU540 OSD

VEPU has 8 rectangular OSD areas, which insert user defined picture into encoding frames. The top left and bottom right ordinate for each OSD area is assigned by LAYER1.VEPU_OSD0~7_POS, and the materials buffer assigned by LAYER1.VEPU_ADR_OSD0~7.

VEPU's OSD material bases on palette. LAYER1.VEPU_OSD_CFG.osd_plt_typ selects the type of palette: default OSD palette has only 8 colors while user defined OSD palette (configured by LAYER1.VEPU_OSD_PLT0~255) supports up to 256 colors.

Note that LAYER1.VEPU_OSD_CFG.osd_plt_cks should be 0 when configure and be 1 when encoding.

10.6.12 VEPU540 Safe Clear

Safe Clear confirms the integrity of BUS transaction. It will discard the (AXI) transactions have not sent out and complete all outstanding ones. To implement safe clear, software should set LAYER1.VEPU_ENC_CLR to 1, and wait for LAYER1.VEPU_ST_STUS.clr_fnsh interrupt. After that pull down VEPU asynchronous reset port to perform force reset.

10.6.13 VEPU540 Large Resolution Encoding

The typical resolution supported by VEPU is 1080P while the maximum resolution is 4096x4096. When encoding the video with resolution above 1080P, large resolution encoding strategy is needed.

For HEVC encoding, TILE partition is used to support the large resolution video encoding which above 1080P. Layer1.TILE_CFG_HEVC and Layer1.TILE_POS contain the configuration of TILE size and position.

For H.264 encoding, slice line split is used to support the large resolution video encoding which above 1080P. Layer1.SLI_CFG_H264.sli_crs_en should be 0, and Layer1.SLI_SPLT set each MB line into a slice. Meanwhile, Layer1.sli_max_num_m1 should be bigger than the maximum number of MB lines in current picture.

Chapter 11 Video Capture (VICAP)

11.1 Overview

The Video Capture, receives the data from Camera via DVP/MIPI, and transfers the data into system main memory by AXI bus.

The features of VICAP are as follow:

- Support BT601 YCbCr 422 8bit input、RAW 8/10/12bit input
- Support BT656 YCbCr 422 8bit input
- Support BT1120 YCbCr 422 8bit input, single/dual-edge sampling
- Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input
- Support YUYV sequence configurable
- Support the polarity of pixel_clk, hsync and vsync configurable
- Support receiving CSI2 protocol data(up to four IDs)
- Support receiving DSI protocol data(Video mode/Command mode)
- Support window cropping
- Support virtual stride when write to DDR
- Support NV16/NV12 output for YUV data
- Support compact/non-compact output for RAW data
- Support MMU

11.2 Block Diagram

VICAP/VICAP_LITE comprises with:

- AHB Slave

Host configure the registers via the AHB Slave

- AXI Master

Transmit the data to chip memory via the AXI Master

- MMU

Map the virtual address to physical address

- INTERFACE

Translate the input video data(DVP/CSI/LVDS) into the requisite data format

- CROP

Bypass or crop the source video data to a smaller size destination

- DMA

Control the operation of AXI Master

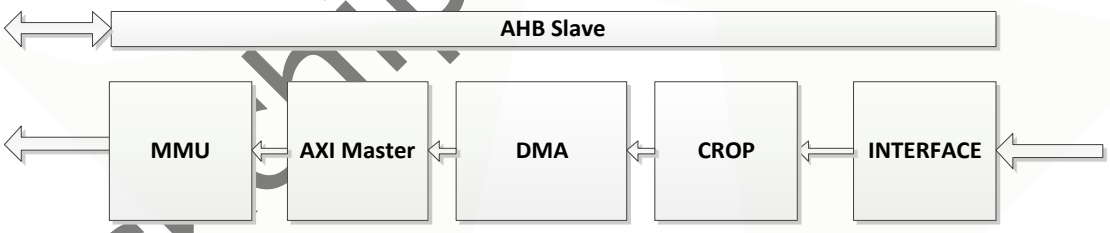


Fig. 11-1 VICAP Block Diagram

11.3 Function Description

11.3.1 Interface

Interface module is designed to receive DVP/CSI/LVDS data and transfer to pixel data.

11.3.2 Crop

Crop module is used to crop the received image.

11.3.3 DMA

The DMA is used to transfer the data from crop module to the AXI master block which will send the data to the AXI bus.

11.3.4 AXI Master

There is an AXI master in VICAP, it is responsible for transferring the DMA output data to AXI bus.

11.3.5 MMU

There is a MMU in VICAP, it is responsible for mapping the virtual address to physical address.

11.4 VICAP Register Description

11.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

11.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VICAP_DVP_CTRL	0x0000	W	0x00007000	DVP path control
VICAP_DVP_INTEN	0x0004	W	0x00000000	DVP path interrupt status
VICAP_DVP_INTSTAT	0x0008	W	0x00000000	DVP path interrupt status
VICAP_DVP_FOR	0x000C	W	0x00000000	DVP path format
VICAP_DVP_MULTI_ID	0x0010	W	0x00000000	Channel ID for multi-ID mode
VICAP_DVP_FRM0_ADDR_Y	0x0014	W	0x00000000	DVP path frame0 y address
VICAP_DVP_FRM0_ADDR_UV	0x0018	W	0x00000000	DVP path frame0 uv address
VICAP_DVP_FRM1_ADDR_Y	0x001C	W	0x00000000	DVP path frame1 y address
VICAP_DVP_FRM1_ADDR_UV	0x0020	W	0x00000000	DVP path frame1 uv address
VICAP_DVP_VIR_LINE_WIDTH	0x0024	W	0x00000000	DVP path virtual line width
VICAP_DVP_SET_SIZE	0x0028	W	0x01E002D0	The expected width and height of received image
VICAP_DVP_LINE_INT_NUM	0x002C	W	0x00000040	DVP path line interrupt number
VICAP_DVP_LINE_CNT	0x0030	W	0x00000000	DVP path line count
VICAP_DVP_CROP	0x0034	W	0x00000000	The start point of DVP path cropping
VICAP_DVP_FIFO_ENTRY	0x0038	W	0x00000000	DVP path FIFO entry
VICAP_DVP_FRAME_STATUS	0x003C	W	0x00000000	DVP path frame status
VICAP_DVP_CUR_DST	0x0040	W	0x00000000	DVP path current destination address
VICAP_DVP_LAST_LINE	0x0044	W	0x00000000	DVP path last frame line number
VICAP_DVP_LAST_PIX	0x0048	W	0x00000000	DVP path last line pixel number
VICAP_DVP_FRM0_ADDR_Y_ID1	0x0050	W	0x00000000	DVP path frame0 y address for ID1
VICAP_DVP_FRM0_ADDR_UV_ID1	0x0054	W	0x00000000	DVP path frame0 uv address for id1
VICAP_DVP_FRM1_ADDR_Y_ID1	0x0058	W	0x00000000	DVP path frame1 y address for id1
VICAP_DVP_FRM1_ADDR_UV_ID1	0x005C	W	0x00000000	DVP path frame1 uv address for id1
VICAP_DVP_FRM0_ADDR_Y_ID2	0x0060	W	0x00000000	DVP path frame0 y address for id2
VICAP_DVP_FRM0_ADDR_UV_ID2	0x0064	W	0x00000000	DVP path frame0 uv address for id2
VICAP_DVP_FRM1_ADDR_Y_ID2	0x0068	W	0x00000000	DVP path frame1 y address for id2
VICAP_DVP_FRM1_ADDR_UV_ID2	0x006C	W	0x00000000	DVP path frame1 uv address for id2

Name	Offset	Size	Reset Value	Description
VICAP_DVP_FRM0_ADDR_Y_ID3	0x0070	W	0x00000000	DVP path frame0 y address for id3
VICAP_DVP_FRM0_ADDR_UV_ID3	0x0074	W	0x00000000	DVP path frame0 uv address for id3
VICAP_DVP_FRM1_ADDR_Y_ID3	0x0078	W	0x00000000	DVP path frame1 y address for id3
VICAP_DVP_FRM1_ADDR_UV_ID3	0x007C	W	0x00000000	DVP path frame1 uv address for id3
VICAP_MIPI_ID0_CTRL0	0x0080	W	0x00000000	MIPI path id0 control0
VICAP_MIPI_ID0_CTRL1	0x0084	W	0x00000000	MIPI path id0 control1
VICAP_MIPI_ID1_CTRL0	0x0088	W	0x00000000	MIPI path id1 control0
VICAP_MIPI_ID1_CTRL1	0x008C	W	0x00000000	MIPI path id1 control1
VICAP_MIPI_ID2_CTRL0	0x0090	W	0x00000000	MIPI path id2 control0
VICAP_MIPI_ID2_CTRL1	0x0094	W	0x00000000	MIPI path id2 control1
VICAP_MIPI_ID3_CTRL0	0x0098	W	0x00000000	MIPI path id3 control0
VICAP_MIPI_ID3_CTRL1	0x009C	W	0x00000000	MIPI path id3 control1
VICAP_MIPI_CTRL	0x00A0	W	0x00000001	MIPI path control
VICAP_MIPI_FRAME0_ADDR_Y_ID0	0x00A4	W	0x00000000	First address of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI_FRAME1_ADDR_Y_ID0	0x00A8	W	0x00000000	First address of odd frame for ID0 Y path
VICAP_MIPI_FRAME0_ADDR_UV_ID0	0x00AC	W	0x00000000	First address of even frame for ID0 UV path
VICAP_MIPI_FRAME1_ADDR_UV_ID0	0x00B0	W	0x00000000	First address of odd frame for ID0 UV path
VICAP_MIPI_FRAME0_VLW_Y_ID0	0x00B4	W	0x00000000	Virtual line width of even frame for ID0 Y/RAW/RGB path
VICAP_MIPI_FRAME1_VLW_Y_ID0	0x00B8	W	0x00000000	Virtual line width of odd frame for ID0 Y/RAW/RGB path
VICAP_MIPI_FRAME0_VLW_UV_ID0	0x00BC	W	0x00000000	Virtual line width of even frame for ID0 UV path
VICAP_MIPI_FRAME1_VLW_UV_ID0	0x00C0	W	0x00000000	Virtual line width of odd frame for ID0 UV path
VICAP_MIPI_FRAME0_ADDR_Y_ID1	0x00C4	W	0x00000000	First address of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI_FRAME1_ADDR_Y_ID1	0x00C8	W	0x00000000	First address of odd frame for ID1 Y/RAW/RGB path
VICAP_MIPI_FRAME0_ADDR_UV_ID1	0x00CC	W	0x00000000	First address of even frame for ID1 UV path
VICAP_MIPI_FRAME1_ADDR_UV_ID1	0x00D0	W	0x00000000	First address of odd frame for ID1 UV path
VICAP_MIPI_FRAME0_VLW_Y_ID1	0x00D4	W	0x00000000	Virtual line width of even frame for ID1 Y/RAW/RGB path
VICAP_MIPI_FRAME1_VLW_Y_ID1	0x00D8	W	0x00000000	Virtual line width of odd frame for ID1 Y path
VICAP_MIPI_FRAME0_VLW_UV_ID1	0x00DC	W	0x00000000	Virtual line width of even frame for ID1 UV path
VICAP_MIPI_FRAME1_VLW_UV_ID1	0x00E0	W	0x00000000	Virtual line width of odd frame for ID1 UV path
VICAP_MIPI_FRAME0_ADDR_Y_ID2	0x00E4	W	0x00000000	First address of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI_FRAME1_ADDR_Y_ID2	0x00E8	W	0x00000000	First address of odd frame for ID2 Y/RAW/RGB path

Name	Offset	Size	Reset Value	Description
VICAP_MIPI_FRAME0_ADDR_UV_ID2	0x00EC	W	0x00000000	First address of even frame for ID2 UV path
VICAP_MIPI_FRAME1_ADDR_UV_ID2	0x00F0	W	0x00000000	First address of odd frame for ID2 UV path
VICAP_MIPI_FRAME0_VLW_Y_ID2	0x00F4	W	0x00000000	Virtual line width of even frame for ID2 Y/RAW/RGB path
VICAP_MIPI_FRAME1_VLW_Y_ID2	0x00F8	W	0x00000000	Virtual line width of odd frame for ID2 Y/RAW/RGB path
VICAP_MIPI_FRAME0_VLW_UV_ID2	0x00FC	W	0x00000000	Virtual line width of even frame for ID2 UV path
VICAP_MIPI_FRAME1_VLW_UV_ID2	0x0100	W	0x00000000	Virtual line width of odd frame for ID2 UV path
VICAP_MIPI_FRAME0_ADDR_Y_ID3	0x0104	W	0x00000000	First address of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI_FRAME1_ADDR_Y_ID3	0x0108	W	0x00000000	First address of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI_FRAME0_ADDR_UV_ID3	0x010C	W	0x00000000	First address of even frame for ID3 UV path
VICAP_MIPI_FRAME1_ADDR_UV_ID3	0x0110	W	0x00000000	First address of odd frame for ID3 UV path
VICAP_MIPI_FRAME0_VLW_Y_ID3	0x0114	W	0x00000000	Virtual line width of even frame for ID3 Y/RAW/RGB path
VICAP_MIPI_FRAME1_VLW_Y_ID3	0x0118	W	0x00000000	Virtual line width of odd frame for ID3 Y/RAW/RGB path
VICAP_MIPI_FRAME0_VLW_UV_ID3	0x011C	W	0x00000000	Virtual line width of even frame for ID3 UV path
VICAP_MIPI_FRAME1_VLW_UV_ID3	0x0120	W	0x00000000	Virtual line width of odd frame for ID3 UV path
VICAP_MIPI_INTEN	0x0124	W	0x00000000	MIPI path interrupt enable
VICAP_MIPI_INTSTAT	0x0128	W	0x00000000	MIPI path interrupt status
VICAP_MIPI_LINE_INT_NUM_ID0_1	0x012C	W	0x00400040	Line number of the MIPI path ID0/1 line interrupt
VICAP_MIPI_LINE_INT_NUM_ID2_3	0x0130	W	0x00400040	Line number of the MIPI path ID2/3 line interrupt
VICAP_MIPI_LINE_CNT_ID0_1	0x0134	W	0x00000000	Line count of the MIPI path ID0/1
VICAP_MIPI_LINE_CNT_ID2_3	0x0138	W	0x00000000	Line count of the MIPI path ID2/3
VICAP_MIPI_ID0_CROP_START	0x013C	W	0x00000000	The start point of MIPI ID0 cropping
VICAP_MIPI_ID1_CROP_START	0x0140	W	0x00000000	The start point of MIPI ID1 cropping
VICAP_MIPI_ID2_CROP_START	0x0144	W	0x00000000	The start point of MIPI ID2 cropping
VICAP_MIPI_ID3_CROP_START	0x0148	W	0x00000000	The start point of MIPI ID3 cropping
VICAP_MIPI_FRAME_NUM_VC0	0x014C	W	0x00000000	The frame number of virtual channel 0
VICAP_MIPI_FRAME_NUM_VC1	0x0150	W	0x00000000	The frame number of virtual channel 1
VICAP_MIPI_FRAME_NUM_VC2	0x0154	W	0x00000000	The frame number of virtual channel 2

Name	Offset	Size	Reset Value	Description
VICAP_MIPI_FRAME_NUM_VC3	0x0158	W	0x00000000	The frame number of virtual channel 3
VICAP_Y_STAT_CONTROL	0x0190	W	0x00000000	Y statistics control
VICAP_Y_STAT_VALUE	0x0194	W	0x00000000	Y statistics value
VICAP_MMU_DTE_ADDR	0x0800	W	0x00000000	MMU current page table address
VICAP_MMU_STATUS	0x0804	W	0x00000000	MMU status register
VICAP_MMU_COMMAND	0x0808	W	0x00000000	MMU command register
VICAP_MMU_PAGE_FAULT_ADDR	0x080C	W	0x00000000	MMU logical address of last page fault
VICAP_MMU_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU Zap cache line register
VICAP_MMU_INT_RAWSTAT	0x0814	W	0x00000000	MMU raw interrupt status register
VICAP_MMU_INT_CLEAR	0x0818	W	0x00000000	MMU interrupt status clear
VICAP_MMU_INT_MASK	0x081C	W	0x00000000	MMU interrupt mask
VICAP_MMU_INT_STATUS	0x0820	W	0x00000000	MMU interrupt status
VICAP_MMU_AUTO_GATING	0x0824	W	0x00000000	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

11.4.3 Detail Registers Description

VICAP_DVP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x7	axi_burst_type Burst1~16.
11:5	RO	0x00	reserved
4	RW	0x0	dma_idle_req Write 1 will stop VICAP DVP path dma. When this bit change to 0,dma is stopped really.
3	RO	0x0	reserved
2:1	RW	0x0	work_mode 2'b00: One frame stop mode 2'b01: Ping-pong mode 2'b10: Reserved 2'b11: Reserved Note: BT1120 only support ping-pong mode.
0	RW	0x0	cap_en 1'b0: Disable 1'b1: Enable

VICAP_DVP_INTEN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dma_frame_end_id3_en ID3 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
12	RW	0x0	dma_frame_end_id2_en ID2 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	dma_frame_end_id1_en ID1 dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	line_int_en The specified line end interrupt enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pst_inf_frame_end_en Frame end after interface FIFO interrupt enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pre_inf_frame_end_en Frame end before interface FIFO interrupt enable. 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	W1C	0x0	bus_err_en Axi master or ahb slave response error interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	dfifo_of_en DMA FIFO overflow interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ififo_of_en Interface FIFO overflow interrupt enable. 1'b0: Disable 1'b1: Enable
3	W1C	0x0	pix_err_en The pixel number of last line not equal to the set height interrupt enable. 1'b0: Disable 1'b1: Enable
2	W1C	0x0	line_err_en The line number of last frame not equal to the set height interrupt enable. 1'b0: Disable 1'b1: Enable
1	W1C	0x0	line_end_en Line end interrupt enable. 1'b0: Disable 1'b1: Enable
0	W1C	0x0	dma_frame_end_en Dma frame end interrupt enable. 1'b0: Disable 1'b1: Enable

VICAP_DVP_INTSTAT

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	W1C	0x0	dma_frame_end_id3 ID3 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	dma_frame_end_id2 ID2 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	dma_frame_end_id1 ID1 dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt
10	RW	0x0	line_int The specified line end interrupt. 1'b0: No interrupt 1'b1: Interrupt
9	RW	0x0	pst_inf_frame_end Frame end after interface FIFO interrupt. 1'b0: No interrupt 1'b1: Interrupt
8	RW	0x0	pre_inf_frame_end Frame end before interface FIFO interrupt. 1'b0: No interrupt 1'b1: Interrupt
7	RO	0x0	reserved
6	W1C	0x0	bus_err Axi master or ahb slave response error interrupt. 1'b0: No interrupt 1'b1: Interrupt
5	RW	0x0	dfifo_of DMA FIFO overflow interrupt. 1'b0: No interrupt 1'b1: Interrupt
4	RW	0x0	ififo_of Interface FIFO overflow interrupt. 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	pix_err The pixel number of last line not equal to the set height interrupt. 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	line_err The line number of last frame not equal to the set height interrupt. 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	line_end Line end interrupt. 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	dma_frame_end Dma frame end interrupt. 1'b0: No interrupt 1'b1: Interrupt

VICAP_DVP_FOR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_multi_id_mode 2'd0: 1to1 (ID0 will work) 2'd1: 1to2 (ID0/ID1 will work) 2'd2: 1to4 (ID0/ID1/ID2/ID3 will work) 2'd3: Reserved
29	RW	0x0	sw_multi_id_sel Only for BT1120. 1'b0: Parse the id by data[11:8] 1'b1: Parse the id by data[3:0]
28	RW	0x0	sw_multi_id_en 1'b0: Disable multi-ID bt656/bt1120 received 1'b1: Enable multi-ID bt656/bt1120 received
27	RO	0x0	reserved
26	RW	0x0	sw_yc_swap 1'b0: No swap for y and c 1'b1: Swap for y and c Only for BT1120 mode.
25	RW	0x0	sw_progress_en 1'b0: Interlace 1'b1: Progress Only for BT1120 mode.
24	RW	0x0	sw_dualedge_en 1'b0: Only use single edge of clock 1'b1: Use double edges of clock Only for BT1120 mode.
23:20	RO	0x0	reserved
19	RW	0x0	uv_store_order 1'b0: UVUV 1'b1: VUVU
18	RW	0x0	raw_end 1'b0: Little end 1'b1: Big end
17	RW	0x0	out_420_order 1'b0: UV in the even line 1'b1: UV in the odd line Note: The first line is even line(line 0).
16	RW	0x0	output_420 1'b0: Output is 422 1'b1: Output is 420
15:13	RO	0x0	reserved
12:11	RW	0x0	raw_width 2'b00: 8bit raw data 2'b01: 10bit raw data 2'b10: 12bit raw data 2'b11: Reserve
10	RO	0x0	reserved
9	RW	0x0	field_order 1'b0: Odd field first 1'b1: Even field first
8:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	yuv_in_order 2'b00: UYVY 2'b01: YVYU 2'b10: VYUY 2'b11: YUYV
4:2	RW	0x0	input_mode 3'b000: BT601 YUV422 3'b010: BT656 YUV422 3'b100: BT601 RAW 3'b101: SONY RAW 3'b111: BT1120 YUV422 others: Reserved
1	RW	0x0	href_pol 1'b0: High active 1'b1: Low active
0	RW	0x0	vsync_pol 1'b0: Low active 1'b1: High active

VICAP_DVP_MULTI_ID

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_chid_bit_en_id3 Bit enable for chid_id3. Eg: chid_id3 = 4'b1111 and chid_bit_en_id3 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
27:24	RW	0x0	sw_chid_id3 The channel id for id3.
23:20	RW	0x0	sw_chid_bit_en_id2 Bit enable for chid_id2. Eg: chid_id2 = 4'b1111 and chid_bit_en_id2 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
19:16	RW	0x0	sw_chid_id2 The channel id for id2.
15:12	RW	0x0	sw_chid_bit_en_id1 Bit enable for chid_id1. Eg: chid_id1 = 4'b1111 and chid_bit_en_id1 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
11:8	RW	0x0	sw_chid_id1 The channel id for id1.
7:4	RW	0x0	sw_chid_bit_en_id0 Bit enable for chid_id0. Eg: chid_id0 = 4'b1111 and chid_bit_en_id0 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected.
3:0	RW	0x0	sw_chid_id0 The channel id for id0.

VICAP_DVP_FRM0_ADDR_Y

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y DVP path frame0 y address.

VICAP_DVP_FRM0_ADDR_UV

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv DVP path frame0 uv address.

VICAP_DVP_FRM1_ADDR_Y

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y DVP path frame1 y address.

VICAP_DVP_FRM1_ADDR_UV

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv DVP path frame1 uv address.

VICAP_DVP_VIR_LINE_WIDTH

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	vir_line_width DVP path virtual line width.

VICAP_DVP_SET_SIZE

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x01e0	set_height The expected height of received image.
15:13	RO	0x0	reserved
12:0	RW	0x02d0	set_width The expected width of received image.

VICAP_DVP_LINE_INT_NUM

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0040	line_int_num If line_int_num=100,then vicap receive 100th line200th line300th line.....the line_int will be 1.

VICAP_DVP_LINE_CNT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	line_cnt Current line count.

VICAP_DVP_CROP

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	start_y The vertical ordinate of the start point.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	start_x The horizontal ordinate of the start point.

VICAP_DVP_FIFO_ENTRY

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	uv_fifo_entry Write 0 clear.
15:9	RO	0x00	reserved
8:0	RO	0x000	y_fifo_entry Write 0 clear.

VICAP_DVP_FRAME_STATUS

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	frame_num Completed frame number Write 0 to clear.
15:14	RO	0x0	reserved
13	RO	0x0	f1_sts_id3 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
12	RO	0x0	f0_sts_id3 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
11:10	RO	0x0	reserved
9	RO	0x0	f1_sts_id2 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
8	RO	0x0	f0_sts_id2 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
7:6	RO	0x0	reserved
5	RO	0x0	f1_sts_id1 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.
4	RO	0x0	f0_sts_id1 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.
3	RO	0x0	reserved
2	RO	0x0	idle 1'b0: Work 1'b1: Idle
1	RO	0x0	f1_sts 1'b0: Frame 1 not ready 1'b1: Frame 1 ready Write 0 clear.

Bit	Attr	Reset Value	Description
0	RO	0x0	f0_sts 1'b0: Frame 0 not ready 1'b1: Frame 0 ready Write 0 clear.

VICAP_DVP_CUR_DST

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cur_dst DVP path current destination address.

VICAP_DVP_LAST_LINE

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	last_uv_num UV line number of last frame,only for bt1120 mode.
15:13	RO	0x0	reserved
12:0	RO	0x0000	last_y_num Y line number of last frame.

VICAP_DVP_LAST_PIX

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	last_uv_num DVP path last line uv number.
15:13	RO	0x0	reserved
12:0	RO	0x0000	last_y_num DVP path last line y number.

VICAP_DVP_FRM0_ADDR_Y_ID1

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id1 DVP path frame0 y address for id1.

VICAP_DVP_FRM0_ADDR_UV_ID1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id1 DVP path frame0 uv address for id1.

VICAP_DVP_FRM1_ADDR_Y_ID1

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id1 DVP path frame1 y address for id1.

VICAP_DVP_FRM1_ADDR_UV_ID1

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id1 DVP path frame1 uv address for id1.

VICAP_DVP_FRM0_ADDR_Y_ID2

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id2 DVP path frame0 y address for id2.

VICAP_DVP_FRM0_ADDR_UV_ID2

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id2 DVP path frame0 uv address for id2.

VICAP_DVP_FRM1_ADDR_Y_ID2

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id2 DVP path frame1 y address for id2.

VICAP_DVP_FRM1_ADDR_UV_ID2

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id2 DVP path frame1 uv address for id2.

VICAP_DVP_FRM0_ADDR_Y_ID3

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_y_id3 DVP path frame0 y address for id3.

VICAP_DVP_FRM0_ADDR_UV_ID3

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm0_addr_uv_id3 DVP path frame0 uv address for id3.

VICAP_DVP_FRM1_ADDR_Y_ID3

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_y_id3 DVP path frame1 y address for id3.

VICAP_DVP_FRM1_ADDR_UV_ID3

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm1_addr_uv_id3 DVP path frame1 uv address for id3.

VICAP_MIPI_ID0_CTRL0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_align_id0 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
30:18	RO	0x0000	reserved
17:16	RW	0x0	sw_mipi_yuyv_order_id0 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
15:10	RW	0x00	sw_mipi_dt_id0 Data type for id0.
9:8	RW	0x0	sw_mipi_vc_id0 Virtual channel for id0.
7	RW	0x0	sw_mipi_uv_swap_id0 1'b0: no swap 1'b1: swap
6	RW	0x0	sw_mipi_compact_id0 1'b0: raw10/12 will occupy 16bit 1'b1: raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id0 Enable to crop for id0. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id0 Select command mode for id0. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id0 The type of id0. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id0 Enable to capture id0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI_ID0_CTRL1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id0 Height for id0.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_width_id0 Width for id0if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel). If sw_crop_en_id0 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID1_CTRL0

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_align_id1 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when non-compacted mode.
30:18	RO	0x0000	reserved
17:16	RW	0x0	sw_mipi_yuyv_order_id1 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
15:10	RW	0x00	sw_mipi_dt_id1 Data type for id1.
9:8	RW	0x0	sw_mipi_vc_id1 Virtual channel for id1.
7	RW	0x0	sw_mipi_uv_swap_id1 1'b0: no swap 1'b1: swap
6	RW	0x0	sw_mipi_compact_id1 1'b0: raw10/12 will occupy 16bit 1'b1: raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id1 Enable to crop for id1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id1 Select command mode for id1. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id1 The type of id1. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id1 Enable to capture id1. 1'b0: Disable 1'b1: Enable

VICAP_MIPI_ID1_CTRL1

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id1 Height for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id1 Width for id1if sw_wrddr_type is rgb888,then the width is equal to the number of bytes (not pixel). If sw_crop_en_id1 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID2_CTRL0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_align_id2 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when compacted mode.
30:18	RO	0x0000	reserved
17:16	RW	0x0	sw_mipi_yuyv_order_id2 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
15:10	RW	0x00	sw_mipi_dt_id2 Data type for id2.
9:8	RW	0x0	sw_mipi_vc_id2 Virtual channel for id2.
7	RW	0x0	sw_mipi_uv_swap_id2 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id2 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id2 Enable to crop for id2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id2 Select command mode for id2. 1'b0: Not command mode 1'b1: Command mode
3:1	RW	0x0	sw_mipi_wrddr_type_id2 The type of id2. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_mipi_cap_en_id2 Enable to capture id2. 1'b0: Disable 1'b1: Enable

VICAP_MIPI_ID2_CTRL1

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id2 Height for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id2 Width for id2if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel). If sw_crop_en_id2 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID3_CTRL0

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mipi_align_id3 1'b0: Low alignment(raw10/12 will in [9:0]/[11:0]) 1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4] Only be used when compacted mode.
30:18	RO	0x0000	reserved
17:16	RW	0x0	sw_mipi_yuyv_order_id3 2'b00 :UYVY(CSI-2 standard) 2'b01 :VYUY 2'b10 :YUYV 2'b11 :YVYU
15:10	RW	0x00	sw_mipi_dt_id3 Data type for id3.
9:8	RW	0x0	sw_mipi_vc_id3 Virtual channel for id3.
7	RW	0x0	sw_mipi_uv_swap_id3 1'b0: No swap 1'b1: Swap
6	RW	0x0	sw_mipi_compact_id3 1'b0: Raw10/12 will occupy 16bit 1'b1: Raw10/12 will be compacted
5	RW	0x0	sw_mipi_crop_en_id3 Enable to crop for id3. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_mipi_command_mode_en_id3 Select command mode for id3. 1'b0: Not command mode 1'b1: Command mode

Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_mipi_wrddr_type_id3 The type of id3. 3'b000: For raw8 3'b001: For raw10 3'b010: For raw12 3'b011: For rgb888 3'b100: For yuv422sp 3'b101: For yuv420sp 3'b110: For yuv400
0	RW	0x0	sw_mipi_cap_en_id3 Enable to capture id3. 1'b0: Disable 1'b1: Enable

VICAP_MIPI_ID3_CTRL1

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_height_id3 Height for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_width_id3 Width for id3if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel). If sw_crop_en_id3 is enable the width value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_CTRL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_dma_idle 1'b0: Not idle 1'b1: Idle MIPI/LVDS path dma transport
15	RO	0x0	reserved
14:13	RW	0x0	sw_press_value Press value.
12	RW	0x0	sw_press_en 1'b0: Disable press 1'b1: Enable press
11:7	RO	0x00	reserved
6:5	RW	0x0	sw_hurry_value Hurry value.
4	RW	0x0	sw_hurry_en 1'b0: Disable hurry 1'b1: Enable hurry
3	RO	0x0	reserved
2:1	RW	0x0	sw_water_line 2'b00: 75% 2'b01: 50% 2'b10: 25% 2'b11: 0%

Bit	Attr	Reset Value	Description
0	RW	0x1	sw_water_line_en 1'b0: Disable water line 1'b1: Enable water line

VICAP_MIPI_FRAME0_ADDR_Y_ID0

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id0 First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_Y_ID0

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id0 First address of odd frame for ID0 Y path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_UV_ID0

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id0 First address of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_UV_ID0

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_Y_ID0

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id0 Virtual line width of even frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_Y_ID0

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID0 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_UV_ID0

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_frame0_vlw_uv_id0 Virtual line width of even frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_UV_ID0

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id0 Virtual line width of odd frame for ID0 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_Y_ID1

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id1 First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_Y_ID1

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id1 First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_UV_ID1

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id1 First address of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_UV_ID1

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id1 First address of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_Y_ID1

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id1 Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_Y_ID1

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_frame1_vlw_y_id1 Virtual line width of odd frame for ID1 Y path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_UV_ID1

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id1 Virtual line width of even frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_UV_ID1

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id1 Virtual line width of odd frame for ID1 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_Y_ID2

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id2 First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_Y_ID2

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id2 First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_UV_ID2

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id2 First address of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_UV_ID2

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id0 First address of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_Y_ID2

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x00000	sw_frame0_vlw_y_id2 Virtual line width of even frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_Y_ID2

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id2 Virtual line width of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_UV_ID2

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id2 Virtual line width of even frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_UV_ID2

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id2 Virtual line width of odd frame for ID2 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_Y_ID3

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_y_id3 First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_Y_ID3

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_y_id3 First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_ADDR_UV_ID3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame0_addr_uv_id3 First address of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_ADDR_UV_ID3

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_frame1_addr_uv_id3 First address of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_Y_ID3

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_y_id3 Virtual line width of even frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_Y_ID3

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_y_id0 Virtual line width of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word).

VICAP_MIPI_FRAME0_VLW_UV_ID3

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame0_vlw_uv_id3 Virtual line width of even frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI_FRAME1_VLW_UV_ID3

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_frame1_vlw_uv_id3 Virtual line width of odd frame for ID3 UV path(must be aligned to double word).

VICAP_MIPI_INTEN

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	line_id3_inten 1'b0: Disable 1'b1: Enable
23	RW	0x0	line_id2_inten 1'b0: Disable 1'b1: Enable
22	RW	0x0	line_id1_inten 1'b0: Disable 1'b1: Enable
21	RW	0x0	line_id0_inten 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
20	RW	0x0	csi2rx_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
19	RW	0x0	bandwidth_lack_inten 1'b0: Disable 1'b1: Enable
18	RW	0x0	config_fifo_overflow_inten 1'b0: Disable 1'b1: Enable
17	RW	0x0	dma_uv_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path. 1'b0: Disable 1'b1: Enable
16	RW	0x0	dma_y_fifo_overflow_inten Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path. 1'b0: Disable 1'b1: Enable
15	RW	0x0	frame1_dma_end_id3_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
14	RW	0x0	frame0_dma_end_id3_inten Enable the interrupt of end of even frame for ID3. 1'b0: Disable 1'b1: Enable
13	RW	0x0	frame1_dma_end_id2_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	frame0_dma_end_id2_inten Enable the interrupt of end of even frame for ID2. 1'b0: Disable 1'b1: Enable
11	RW	0x0	frame1_dma_end_id1_inten Enable the interrupt of end of odd frame for ID1. 1'b0: Disable 1'b1: Enable
10	RW	0x0	frame0_dma_end_id1_inten Enable the interrupt of end of even frame for ID1. 1'b0: Disable 1'b1: Enable
9	RW	0x0	frame1_dma_end_id0_inten Enable the interrupt of end of odd frame for ID0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	frame0_dma_end_id0_inten Enable the interrupt of end of even frame for ID0. 1'b0: Disable 1'b1: Enable
7	RW	0x0	frame1_start_id3_inten Enable the interrupt of start of odd frame for ID3. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	frame0_start_id3_inten Enable the interrupt of start of even frame for ID3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	frame1_start_id2_inten Enable the interrupt of start of odd frame for ID2. 1'b0: Disable 1'b1: Enable
4	RW	0x0	frame0_start_id2_inten Enable the interrupt of start of even frame for ID2. 1'b0: Disable 1'b1: Enable
3	RW	0x0	frame1_start_id1_inten Enable the interrupt of start of odd frame for ID1. 1'b0: Disable 1'b1: Enable
2	RW	0x0	frame0_start_id1_inten Enable the interrupt of start of even frame for ID1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	frame1_start_id0_inten Enable the interrupt of start of odd frame for ID0. 1'b0: Disable 1'b1: Enable
0	RW	0x0	frame0_start_id0_inten Enable the interrupt of start of even frame for ID0. 1'b0: Disable 1'b1: Enable

VICAP_MIPI_INTSTAT

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	line_id3_intst 1'b0: No interrupt 1'b1: Interrupt
23	RW	0x0	line_id2_intst 1'b0: No interrupt 1'b1: Interrupt
22	RW	0x0	line_id1_intst 1'b0: No interrupt 1'b1: Interrupt
21	RW	0x0	line_id0_intst 1'b0: No interrupt 1'b1: Interrupt
20	W1C	0x0	csi2rx_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
19	W1C	0x0	bandwidth_lack_intst 1'b0: No interrupt 1'b1: Interrupt
18	W1C	0x0	config_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt

Bit	Attr	Reset Value	Description
17	W1C	0x0	dma_uv_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
16	W1C	0x0	dma_y_fifo_overflow_intst 1'b0: No interrupt 1'b1: Interrupt
15	W1C	0x0	frame1_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
14	W1C	0x0	frame0_dma_end_id3_intst 1'b0: No interrupt 1'b1: Interrupt
13	W1C	0x0	frame1_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
12	W1C	0x0	frame0_dma_end_id2_intst 1'b0: No interrupt 1'b1: Interrupt
11	W1C	0x0	frame1_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
10	W1C	0x0	frame0_dma_end_id1_intst 1'b0: No interrupt 1'b1: Interrupt
9	W1C	0x0	frame1_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
8	W1C	0x0	frame0_dma_end_id0_intst 1'b0: No interrupt 1'b1: Interrupt
7	W1C	0x0	frame1_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
6	W1C	0x0	frame0_start_id3_intst 1'b0: No interrupt 1'b1: Interrupt
5	W1C	0x0	frame1_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
4	W1C	0x0	frame0_start_id2_intst 1'b0: No interrupt 1'b1: Interrupt
3	W1C	0x0	frame1_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
2	W1C	0x0	frame0_start_id1_intst 1'b0: No interrupt 1'b1: Interrupt
1	W1C	0x0	frame1_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt
0	W1C	0x0	frame0_start_id0_intst 1'b0: No interrupt 1'b1: Interrupt

VICAP_MIPI_LINE_INT_NUM_ID0_1

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id1 If line_int_num_id1=100,then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id0 If line_int_num_id0=100,then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1.

VICAP_MIPI_LINE_INT_NUM_ID2_3

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	line_int_num_id3 If line_int_num_id3=100,then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1.
15:14	RO	0x0	reserved
13:0	RW	0x0040	line_int_num_id2 If line_int_num_id2=100,then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1.

VICAP_MIPI_LINE_CNT_ID0_1

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id1 Current line count for id1.
15:14	RO	0x0	reserved
13:0	RO	0x0000	line_cnt_id0 Current line count for id0.

VICAP_MIPI_LINE_CNT_ID2_3

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	line_cnt_id3 Current line count for id3.
15:14	RO	0x0	reserved
13:0	RO	0x0000	line_cnt_id2 Current line count for id2.

VICAP_MIPI_ID0_CROP_START

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id0 The start y coordinate for id0.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_start_x_id0 The start x coordinate for id0,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID1_CROP_START

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id1 The start y coordinate for id1.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id1 The start x coordinate for id1,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID2_CROP_START

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id2 The start y coordinate for id2.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id2 The start x coordinate for id2,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_ID3_CROP_START

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_start_y_id3 The start y coordinate for id3.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_start_x_id3 The start x coordinate for id3,if sw_wrddr_type is rgb888,then the start x is measured in byte. The start x value must be 8 aligned when sw_wrddr_type is raw8/yuv422, must be 4 aligned when sw_wrddr_type is raw10/raw12,and must be 24 aligned when sw_wrddy_type is rgb888.

VICAP_MIPI_FRAME_NUM_VC0

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc0 The frame number of frame end of virtual channel 0.
15:0	RO	0x0000	ro_frame_num_start_vc0 The frame number of frame start of virtual channel 0.

VICAP_MIPI_FRAME_NUM_VC1

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc1 The frame number of frame end of virtual channel 1.
15:0	RO	0x0000	ro_frame_num_start_vc1 The frame number of frame start of virtual channel 1.

VICAP_MIPI_FRAME_NUM_VC2

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc2 The frame number of frame end of virtual channel 2.
15:0	RO	0x0000	ro_frame_num_start_vc2 The frame number of frame start of virtual channel 2.

VICAP_MIPI_FRAME_NUM_VC3

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_frame_num_end_vc3 The frame number of frame end of virtual channel 3.
15:0	RO	0x0000	ro_frame_num_start_vc3 The frame number of frame start of virtual channel 3.

VICAP_Y_STAT_CONTROL

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:26	RW	0x00	sw_black_level_b Black level for B channel.
25:21	RW	0x00	sw_black_level_g Black level for G channel.
20:16	RW	0x00	sw_black_level_r Black level for R channel.
15:14	RO	0x0	reserved
13:12	RO	0x0	ro_block_id2 The number of block of id2.
11:10	RO	0x0	ro_block_id1 The number of block of id1.
9:8	RO	0x0	ro_block_id0 The number of block of id0.
7:6	WO	0x0	sw_y_stat_rd_block Point to the specified block.
5:4	WO	0x0	sw_y_stat_rd_id 2'b00: Point to ID0 2'b01: Point to ID1 2'b10: Point to ID2 2'b11: Reserved

Bit	Attr	Reset Value	Description
3	WO	0x0	sw_y_stat_rd Chanege the y statistics read pointer according to sw_y_stat_rd_id/sw_y_stat_rd_block.
2:1	RW	0x0	sw_bayer_pattern 2'b00: RGGB 2'b01: GRBG 2'b10: GBRG 2'b11: BGGR
0	RW	0x0	sw_y_stat_en 1'b0: Disable y statistics 1'b1: Enable y statistics

VICAP_Y_STAT_VALUE

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_y_stat_value Y statistics value.

VICAP_MMU_DTE_ADDR

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address.

VICAP_MMU_STATUS

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	paging_enabled Paging is enabled.

VICAP_MMU_COMMAND

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE

VICAP_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VICAP_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VICAP_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error.
0	RW	0x0	page_fault Page fault.

VICAP_MMU_INT_CLEAR

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error.
0	WO	0x0	page_fault Page fault.

VICAP_MMU_INT_MASK

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

VICAP_MMU_INT_STATUS

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error.

Bit	Attr	Reset Value	Description
0	RO	0x0	page_fault Page fault.

VICAP_MMU_AUTO_GATING

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self

11.5 Interface Description

Table 11-1 VICAP Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
vicap_clkout	O	CIF_CLKOUT/EBC_GDCLK/PWM11_IR_M1/GPIO4_C0_d	GRF_GPIO4C_IOMUX_L[3:0]=4'h1
vicap_clkin	I	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1/UART1_CTSn_M1/I2S2_SCLK_RX_M1/GPIO4_C1_d	GRF_GPIO4C_IOMUX_L[7:4]=4'h1
vicap_href	I	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTSn_M1/I2S2_MCLK_M1/GPIO4_B6_d	GRF_GPIO4B_IOMUX_H[11:8]=4'h1
vicap_vsync	I	CIF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1/I2S2_SCLK_TX_M1/GPIO4_B7_d	GRF_GPIO4B_IOMUX_H[15:12]=4'h1
vicap_data0	I	CIF_D0/EBC_SDDO0/SDMMC2_D0_M0/I2S1_MCLK_M1/VOP_BT656_D0_M1/GPIO3_C6_d	GRF_GPIO3C_IOMUX_H[11:8]=4'h1
vicap_data1	I	CIF_D1/EBC_SDDO1/SDMMC2_D1_M0/I2S1_SCLK_TX_M1/VOP_BT656_D1_M1/GPIO3_C7_d	GRF_GPIO3C_IOMUX_H[15:12]=4'h1
vicap_data2	I	CIF_D2/EBC_SDDO2/SDMMC2_D2_M0/I2S1_LRCK_TX_M1/VOP_BT656_D2_M1/GPIO3_D0_d	GRF_GPIO3D_IOMUX_L[3:0]=4'h1
vicap_data3	I	CIF_D3/EBC_SDDO3/SDMMC2_D3_M0/I2S1_SDO0_M1/VOP_BT656_D3_M1/GPIO3_D1_d	GRF_GPIO3D_IOMUX_L[7:4]=4'h1
vicap_data4	I	CIF_D4/EBC_SDDO4/SDMMC2_CMD_M0/I2S1_SDI0_M1/VOP_BT656_D4_M1/GPIO3_D2_d	GRF_GPIO3D_IOMUX_L[11:8]=4'h1
vicap_data5	I	CIF_D5/EBC_SDDO5/SDMMC2_CLK_M0/I2S1_SDI1_M1/VOP_BT656_D5_M1/GPIO3_D3_d	GRF_GPIO3D_IOMUX_L[15:12]=4'h1
vicap_data6	I	CIF_D6/EBC_SDDO6/SDMMC2_DET_M0/I2S1_SDI2_M1/VOP_BT656_D6_M1/GPIO3_D4_d	GRF_GPIO3D_IOMUX_H[3:0]=4'h1
vicap_data7	I	CIF_D7/EBC_SDDO7/SDMMC2_PWREN_M0/I2S1_SDI3_M1/VOP_BT656_D7_M1/GPIO3_D5_d	GRF_GPIO3D_IOMUX_H[7:4]=4'h1
vicap_data8	I	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1/UART1_TX_M1/PDM_CLK0_M1/GPIO3_D6_d	GRF_GPIO3D_IOMUX_H[11:8]=4'h1
vicap_data9	I	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M1/UART1_RX_M1/PDM_SDI0_M1/GPIO3_D7_d	GRF_GPIO3D_IOMUX_H[15:12]=4'h1
vicap_data10	I	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1/PDM_CLK1_M1/GPIO4_A0_d	GRF_GPIO4A_IOMUX_L[3:0]=4'h1

Module Pin	Dir	Pad Name	IOMUX Setting
vicap_data11	I	CIF_D11/EBC_SDDO11/GMAC1_RXD2_M1/PDM_SDI1_M1/GPIO4_A1_d	GRF_GPIO4A_IOMUX_L[7:4]=4'h1
vicap_data12	I	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1/UART7_TX_M2/PDM_SDI2_M1/GPIO4_A2_d	GRF_GPIO4A_IOMUX_L[11:8]=4'h1
vicap_data13	I	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1/UART7_RX_M2/PDM_SDI3_M1/GPIO4_A3_d	GRF_GPIO4A_IOMUX_L[15:12]=4'h1
vicap_data14	I	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	GRF_GPIO4A_IOMUX_H[3:0]=4'h1
vicap_data15	I	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	GRF_GPIO4A_IOMUX_H[7:4]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

11.6 Application Notes

11.6.1 DVP receiving Application

The most important configuration requirement of all operations is the DVP_CAP_EN bit must be set after all the mode selection is ready. The configuration order of the input/output data format, YUV order, the address, frame size/width, AXI burst length and other options do not need to care.

There are many debug registers to make it easy to read the internal operation information of VICAP. The line number of last frame and the pixel number of last line can be known by read the DVP_LAST_LINE and DVP_LAST_PIX.

If 1/2/4 mixed BT656/BT1120 is received, sw_multi_id_en/sw_multi_id_mode must be configured. And sw_chid_idx/sw_chid_bit_en_idx should be configured according the encoding rules. Eg: the different videos are distinguished by the [3:2] bits in sync code, so we can configure sw_chid_bit_en_idx=4'b1100.

If DVP data is double edge sampling, GRF_VI_CON1[9] should be configured to 1. And the user can adjust the clock phase by GRF_VI_CON1[6:0].

11.6.2 MIPI receiving Application

VICAP support receiving up to four MIPI IDs at the same time. VICAP could receive all ID value via configuring the sw_vc_id0/1/2/3 and sw_dt_id0/1/2/3, but VICAP could only transform MIPI data to RAW8/10/12, RGB888, YUV422SP, YUV420SP, YUV400 via configuring the sw_wrddr_type. The register sw_height must be same as the received image, and the register sw_width is useless when sw_crop_en is disable. If sw_wrddr_type is rgb888, then the sw_width and sw_start_x are equal to the number of bytes.

If AXI bus is too busy to transfer sensor data, you can enable sw_hurry_en/sw_press_en and sw_water_line_en.

Chapter 12 Image Signal Processing（ISP）

12.1 Introduction

12.1.1 Overview

The Image Signal Processing (ISP) is a complete video and still picture input unit which contains standard sensor picture data processing functions, such as image processing, scaling. This unit supports image sensors with integrated YCbCr processing and also simple CMOS sensors delivering RGB Bayer pattern without any integrated image processing.

Image processing contains many functions, such as HDR_MGE, HDR_DRC, RAWNR, GIC, DEBAYER and so on.Scaling is used for downsizing the sensor data for either displaying them on the LCD. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well. The camera interface provides Parallel-data and MIPI support, so that ISP can be connected to PHY devices or IP blocks directly. All data is transmitted via the memory interface to a AXI bus system using a bus master interface. Programming is done by register read/write transactions using an AHB slave interface.

ISP supports the following features:

- DVP input: ITU-R BT601/656 with raw8/raw10/raw12, YUV422; BT1120
- MIPI input: RX lane x1/x2/4; raw8/raw10/raw12; YUV422;
- Maximum input: 4096x2304
- 3A: include AE/Histogram, AF, AWB statistics output
- FPN: Fixed Pattern Noise removal
- BLC: Black Level Correction
- DPCC: Static/Dynamic defect pixel cluster correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens shading correction
- Bayer-2DNR: Spatial Bayer-raw De-noising
- Bayer-3DNR: Temporal Bayer-raw De-noising
- HDR: 2-Frame Merge into High-Dynamic Range
- DRC: HDR Dynamic Range Compression , Tone mapping
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction
- CCM/CSM: Color correction matrix; RGB2YUV etc
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and Effect enhancement
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion only in the horizontal direction
- YUV-2DNR: Spatial YUV De-noising
- Sharp: image Sharpening and boundary filtering
- Multi-sensor reuse ISP;
- BUS interface: 32 bit AHB configuration; AXI-128 RW; MMU table
- Low power, auto-gating for each block

12.1.2 Using constrains

1. If the virtual width is randomly allocated, the 30th bit of 0x00001808 must be set to the old mode. If the virtual width is equal to the real width, the virtual width is not configured or the real width is configured, at this time, the 30th bit of 0x00001808 should be set to 0, and the hardware will adaptively optimize the transmission of MI at the end of the line.
2. The auto-gating of RAWAWB need to be enabled in the default automatic 3a-gating mode, if the auto-gating is closed by software, the module will continue to count the next frame and cause an error. (only constraint for version 2.1)

3. The enable of BAY3D and the enable of BAYNR must be switched on and off together.
4. The DEHAZE on or off needs to force update its sys_itself_force_upd at the idle of frame.(only constraint for version 2.1)
5. The YNR、CNR and SHARP should be on or off at the same time. Each of these three modules has its own bypass control. If you want to bypass a module, you can turn on its bypass of the module. The bypass signal of YNR has sw_ynr_bft3x3_bypass, sw_ynr_lbft5x5_bypass, sw_ynr_lgft3x3_bypass, sw_ynr_flt1x1_bypass, sw_ynr_sft5x5_bypass, sw_ynr_flt1x1_bypass_sel to choose. The bypass signal of CNR has sw_cnr_exgain_bypass, sw_cnr_hq_bila_bypass, sw_cnr_lq_bila_bypass to choose. The bypass control of SHARP is sw_sharp_bypass.

12.2 Block Diagram

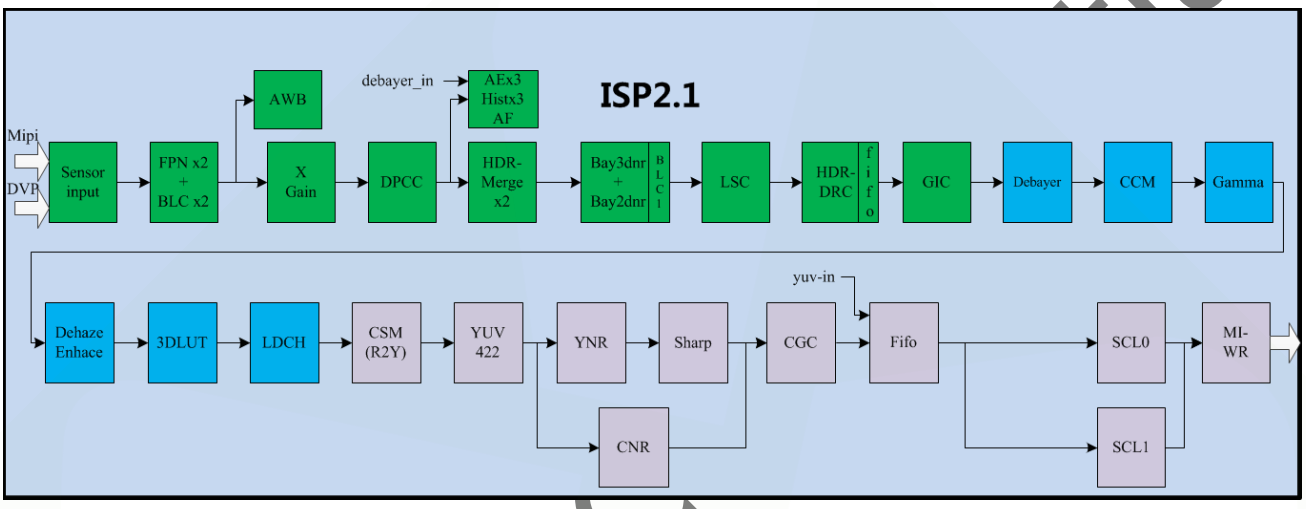


Fig. 12-1 ISP Block Diagram

ISP comprises with:

- MIPI serial camera interface(MIPI)
- RAW Processing
- RGB Processing
- YUV Processing
- Memory Interface(MI)

12.3 Function Description

12.3.1 CSI2RX(MIPI)

（1）Overview

CSI2RX is a MIPI controller, which parses raw data from D-PHY into each pixel output.

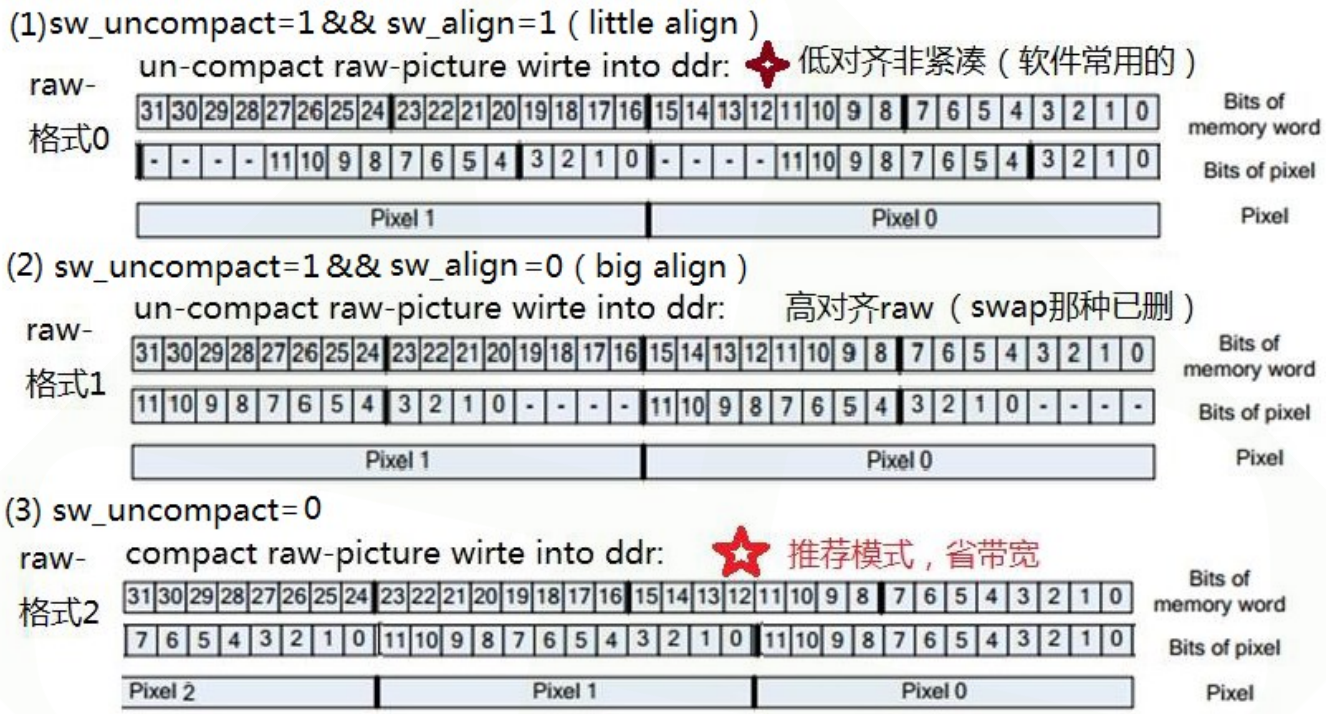
（2）Features

- Compliant with MIPI Alliance Standard for Camera Serial2(CSI2),version 1.00-29 Nov 2005
- Interface with MIPI D-PHY following PHY Protocol Interface(PPI), version 1.00-14 May 2009
- Support VC sensor, HDR sensor(AR0239, IMX327)
- Support x1/x2/x4 DPHY RX data lanes, and merge into word align
- Support RAW8,RAW10,RAW12 transfer(compatible with the old method)
- Support RAW14,RAW16 clip into RAW12, then into ISP pipeline or into DDR
- Support RAW8. RAW10,RAW12,YUV422_8 and RGB888 direct to DDR
- Support auto correct single-ecc error
- Support multiple ecc, crc error, and all phy error interrupts
- Frequency-->500Mhz pix rate
- Support four mipi_tx channels and three mipi_rx channels

- Support embed_data(RAW8/10/12/14/16 use 2byte align) into DDR & read back pixels into ISP
- Support ppi_data(word align) into DDR for debug
- Multi-ID separately into DDR and into ISP, HDR or PDAF
- Ppi_data read back, ppi2pix into ISP, low priority (save bandwidth)
- Support hdr stream: frame mode; line mode
- Support DVP data input
- Support LVDS data input
- Support MIPI raw readback framex1, framex2
- Support FPN (Fixed Pattern Noise)

12.3.1.1 Block Descriptions

Raw-picture into DDR support un-compact and compact (including swap) mode:



The function mode of csi2rx depend on the configuration of sw_ibuf_op_mode, which are shown in the following table.

Table 12-1 csi2rx function mode

Sw_ibuf_op_mode	Function	Interval mode	HDR mode	Need DDR
0	normal	NA	N	N
3	user_mode	NA/frame/line	N/Y	N/Y
4	raw_rdback_framex1	frame	N	Y
5	raw_rdback_framex2	frame	Y	Y
6	raw_rdback_framex3	frame	N	N
8	frame_x2_ddr	frame	Y	Y
9	line_x2_ddr	line	Y	Y
10	line_x2_noddr	line	Y	N
12	frame_x3_ddr	frame	N	N
13	line_x3_ddr	line	N	N

(1) frame_x2_ddr mode (2IDs--hdr mode)
The 2IDs interframe mode has L-data and S-data, which is similar to the 3IDs interframe mode.
(2) line_x2_ddr_mode (2IDs--hdr mode)
The 2IDs interline mode has L-data and S-data, which is similar to the 3IDs interline mode.
(3) line_x2_noddr mode (2IDs--hdr mode)

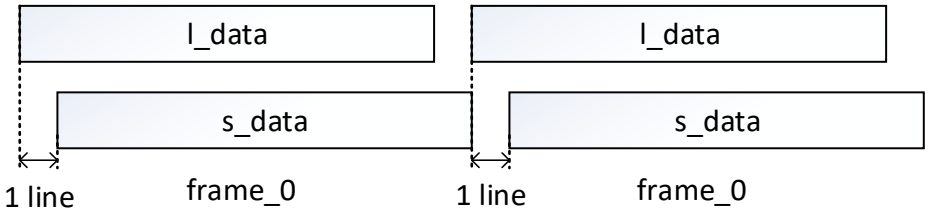


Fig. 12-2 2IDs interline mode data flow (no DDR)

In line_x2_noddr mode interline mode, both ID data are input from phy interface to csi2rx. The data of the two IDs is input at intervals of lines, and the order of L-data and S-data. When the L-data arrives, the data will not be output to DDR. After 1 line of phy's L-data is transferred, S-data is transferred. S-data is directly processed into pix data of pipeline without DDR.

(4) user mode

User defined mode. All dmatx and dmarx are available. If do not configure any dmarx, user mode is equal to normal mode.

(5) raw_rdback_framex3 mode (hdr mode)

The difference between frame_x3_ddr mode and raw_rdback_framex3 mode is that S-data also needs to go in and out of DDR. S-data is output from dmatx2 (all dmatx configurable, recommend dmatx2) to DDR. Then S-data is read back through channel dmarx2 (dmarxs). The time to start readback is up to the user. Start once, read back one frame of L-data, M-data and S-data.

(6) raw_rdback_framex2 mode (hdr mode)

The mode raw_rdback_framex2 is similar to mode frame_x2_ddr mode. It refers to raw_rdback_framex3 mode.

(7) raw_rdback_framex1 mode

Under raw_rdback_framex1 mode, S-data is processed by csi2word module and output from dmatx2 (all dmatx configurable, recommend dmatx2) to DDR. Then S-data is read back through channel dmarx2 (dmarxs). The time to start dmarxs is up to the user. Start once, read back one frame of S-data.

(8) normal mode (Single ID)

The single ID mode is the normal sensor mode. The single ID data is input to csi2rx controller through d-phy interface. Csi2rx decodes the PPI stream data of d-phy, then output pixel to ISP.

12.3.2 Memory Interface(MI)

The memory interface unit (MI) is responsible for reading/writing image data from/to the system memory(DDR). The MI has six main tasks, which can operate independently:

- Take image data from the main path, either in YCbCr or RAW format, and write it into DDR.
- Take image data from MIPI module, and take it back from the DDR to MIPI module.
- Take image data from DBR module, and take it back from the DDR to DBR module.
- Take image data of LUT data from the DDR to 3D_LUT/LDCH/LSC module.

Memory Interface is as following:

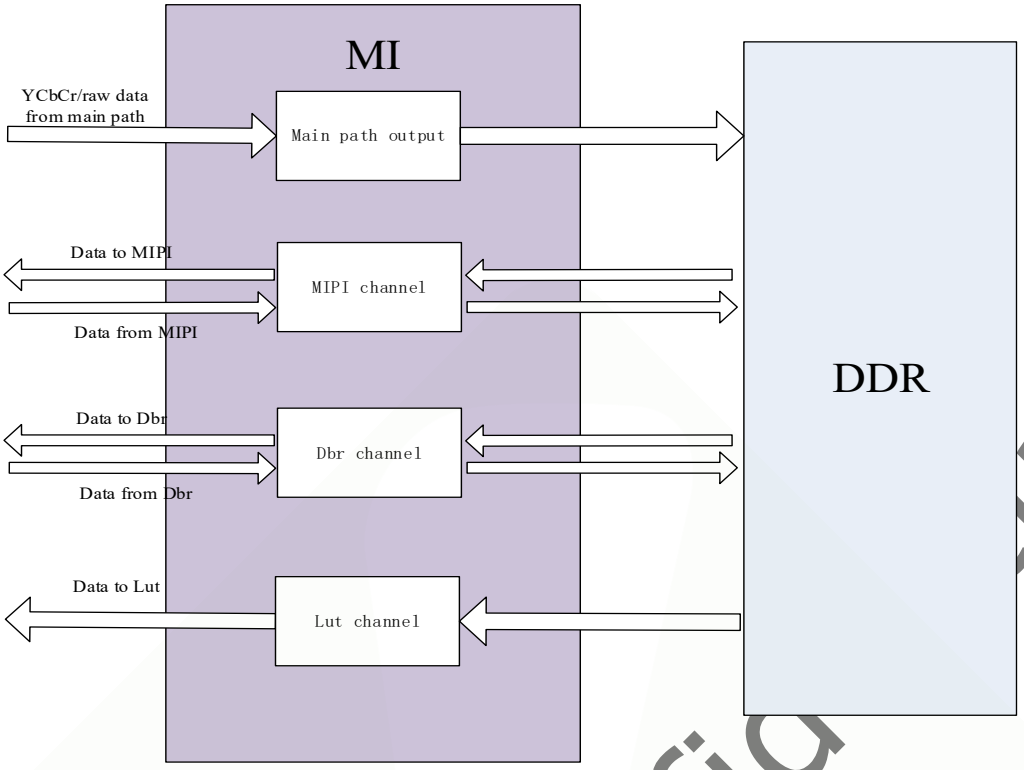


Fig. 12-3 Memory Interface

The following registers need to be configured to use different channels:

（1）Main path

The registers need to be configured are as follows(xx means Y, CB ,and CR):

- MI_MP_WR_xx_BASE

This is the base address of the memory area to use for that buffer.
This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(MI_MP_WR_xx_BASE, address_value) is equivalent to write (MI_MP_WR_xx_BASE, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is not recommended to use non-aligned address values for access. It is also not recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations.
In addition, the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL .
Set control bit init_base_en before updating so that a forced or automatic update can take effect.

- MI_MP_WR_xx_SIZE

Size of main picture ring buffer or raw data ring buffer.
Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update.
Set control bit init_base_en before updating so that a forced or automatic update can take effect.
Note: This register protects from non-aligned access.

- MI_MP_xx_OFFS_CNT_INIT

This is the initial offset (in bytes) for writing to the buffer after e.g. a soft reset. Usually, to write to the buffer from the very beginning, an offset of zero is to be programmed into this register.

- MI_MP_xx_OFFS_CNT_START

This is a read-only register, which holds the offset at which the MI had written the last processed frame. This register is updated at frame end, so at any given time, it contains always the starting offset of the last completely processed frame.

- MI_WR_CTRL

This register is a global write control register of main path, include path_enable, wr_format

and so on. Refer to MI_WR_CTRL register description for details.

(2)MIPI/DBR/LUT channel

The registers need to be configured are as follows(xx include RAW0~RAW3, LUT, and DBR):

- xx_WR_BASE

DDR write base address, similar to MI_SP_WR_xx_BASE.Refer to register description for details.

- xx_WR_SIZE

DDR write size, similar to MI_SP_WR_xx_SIZE.Refer to register description for details.

- xx_WR_LENGHT

Line length of DDR write in pixel, also known as line stride.If no line stride is used, line length must match image width.For example, raw8 mode must be a multiple of 8.

- xx_RD_BASE

Image read start address.

- xx_RD_LENGTH

Line length of DDR read in pixel, also known as line stride.

- MI_WR_CTRL2

This register is a global write control register of MIPI/DBR/LUT channel. Refer to register description for details.

- MI_RD_CTRL2

This register is a control register of MIPI/DBR/LUT channel, Refer to MI_WR_CTRL register description for details.

12.3.3 ISP_CORE

12.3.3.1 INFORM

The input formatter module is responsible for sampling data from the sensor device and providing it to the other blocks in the processing pipelines.

12.3.3.2 OUTFORM

At the output of the ISP sub module the image data may be cropped a third time.
The following figure illustrates the different possible regions which can be defined by register settings. Some of these regions may have the same size and offset (settings), if a differentiation is not needed.

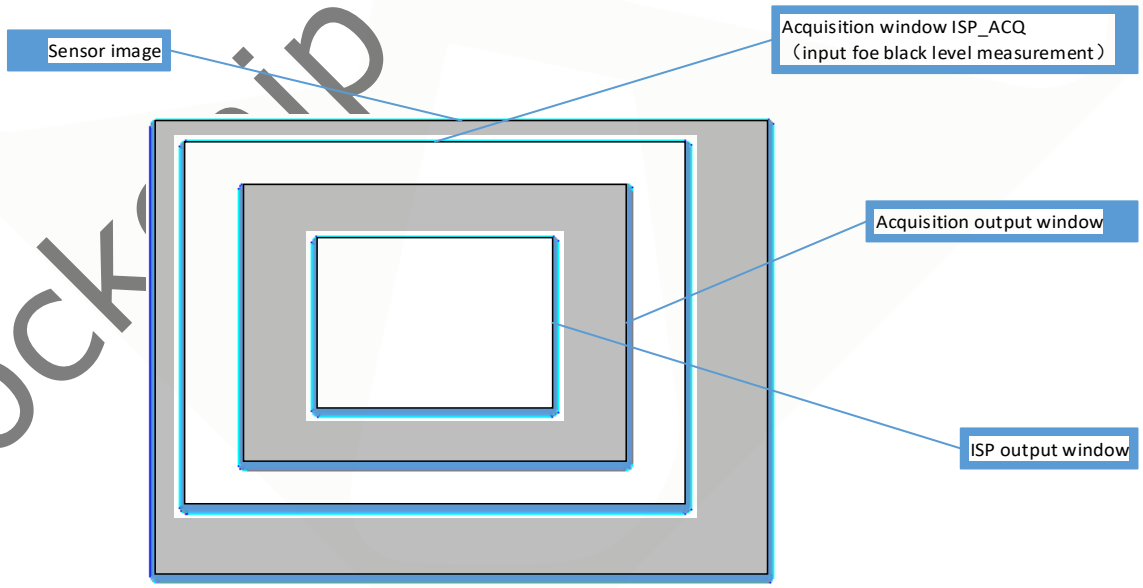


Fig. 12-4 Possible cropping regions of ISP

12.3.3.3 BLC

Black-level-control block is a function to subtract a DC offset from picture data.
A CMOS sensor always has a so-called black level shift. So that pixels with no light on them will not read out the value zero. This value varies with different setting for the exposure.
This black level can easily be detected by special pixels on the sensor that are permanently covered, i.e. they are always black.
The black level subtraction block reads out the values of these pixels, calculates their mean

value and then subtracts these values from all pixels that represent the picture frame (in automatic mode).

12.3.3.4 GAMMA_IN

The gamma_in module is used to adapt the image signal processing to the characteristics of the attached sensor device.
There are three gamma curves can be defined, one for each color component red, green, and blue.

12.3.3.5 DPCC

The DPCC (Static/Dynamic defect pixel cluster correction) module is used to correct the defect pixels of the sensor, and supports both static and dynamic DPCC. The DPCC supports detection and correction of single pixels and small cluster defects (up to 3x3 pixels). It detects and corrects single pixels and small cluster defects on raw Bayer image data. An integrated defect pixel table allows the correction of up to 2048 fix positions independently from the on-the-fly detection.

12.3.3.6 HDR

HDR(High Dynamic Range) refers to the ratio of "brightest value" and "darkest value" contained in an image, that is, the number of levels of gray scale division between "brightest" and "darkest".
Dynamic range calculation formula: Dynamic_range = 20log(MaxIntensity / MinIntensity), which means maximum brightness value.
Version 2.1 HDR*2 support 17bit, the dynamic range is 102db. The larger the dynamic range, the richer the level of representation and the wider the color space. High Dynamic Range means the ratio of "brightest" to "darkest" is very high.
HDR is composed of HDRMGE and HDR-DRC two module. HDRMGE realize the function of three/two frames synthesizing one frame. HDR-DRC realize wide dynamic compression.

12.3.3.7 Bayer-NR

Bay2DNR module mainly realizes non-local mean noise reduction of image in raw format, so as to achieve the purpose of noise removal.
Bay3DNR module mainly realizes Advanced Temporal Noise reduce noise of image in raw format, so as to achieve the purpose of noise removal.

12.3.3.8 LSC

Lens shade correction(LSC) is designed to deal the problems of lens shading and vignette. It is done during input data processing: If the lens shading correction is enabled, each pixel is processed and corrected according to the stored settings. The lens shading correction is done by multiplying each input pixel with its respective correction value. Only the correction factors at predefined sector corners as well as the sector positions are stored. The pixel position specific correction values are calculated using bilinear interpolation. The correction factors at the sector corners are calculated during a calibration process which uses one or more reference frames which have to be captured under dedicated light conditions and at a dedicated position of the sensor. The captured frames are evaluated by software and the calculated parameters for lens shading correction are stored in multiple illumination specific tables e.g. in external memory or on a flash device. The software controls the lens shading process by loading or updating the correct tables into the hardware module.
It is also possible to use different lens shading correction parameters for different environment conditions, e.g. lightness, light direction or sensor position.

12.3.3.9 GIC

GIC(Green Imbalance Correction) is a method to correct the color imbalance in captured images. The principle is that each pixel in the captured image is used to represent a set of colors, and there is a selected specific color pixel in the set of colors. The horizontal and vertical gradient data are derived from a set of pixel blocks surrounding the single pixel, and the pixel blocks are classified according to the visual characteristics of the part of the image. A compensation value based on gradient data and visual characteristics is determined, and the compensation value is applied to the pixel block.

12.3.3.10 DEBAYER

The debayer module outputs RGB data after interpolation and filtering operation of the input Bayer data. The filtering operation can be bypassed by software configuration, and debayer module can also output three RGB components of the same value in black-and-white mode.

12.3.3.11 CCM

CCM(Color Correct Matrix) is used to correct the color crosstalk because of three channel response of sensor when only one channel color input.For example,when the sensor input is red,the other two channel GB not only R is also response too.CCM is working to reduce this crosstalk to make color more bright in color.The adjustment factor is added to adjust CCM working strength.The factor is works at dark range and bright range,this two range is symmetry.

12.3.3.12 GAMMA_OUT

Because the human eye's perception of natural brightness is non-linear, the dynamic range and gray-scale budget of the medium we use to record and display the picture are limited. In this premise, gamma is produced which is the mapping relationship between the natural brightness and the subjective gray-scale experience.

12.3.3.13 DEHAZE_ENHANCE

Dehaze: The process of dehaze is that the input pixel first goes through the dark channel defogging treatment, then goes through a histogram equalization module, and finally outputs the defogging results. In addition, a dehaze gain is also output to guide the noise reduction module.The module supports two modes of parameter adaptation and parameter external configuration. The parameters of the adaptive mode are calculated by the module itself, without external intervention, and the adaptive parameters are conservative.
Enhance: Dhaz algorithm can't enhance the image effect at night, so an enhance enable is added. When the enable is turned on, it can enhance the image at night.

12.3.3.14 3DLUT

3D_LUT(3D look up table) is a technical means of color calibration. Because the 3D LUT has RGB channels for each coordinate direction, the biggest advantage of 3D LUT in color calibration can affect both gamut, color temperature and gamma(this is a 1D LUT, 2D LUT or matrix can't be achieved), and more accurate than traditional matrix calibration methods. In addition, the 3D LUT can map and process all color information, whether it is a color that exists or does not exist, or a color gamut that cannot be reached by film.

12.3.3.15 LDCH

This module achieves distortion correction under fisheye lens.
This module needs to take table from DDR through MI module. When the resolution is small, it is recommended that the image's MI configuration burst length be greater than the table's width; otherwise, the fetching will hang.https://fanyi.baidu.com/?aldtype=16047 -zh/en/javascript:void(0);

12.3.3.16 2DNR-YUV

2DNR consists of two modules, YNR and UVNR. YNR is used to filter the noise of Y component, and UVNR is used to filter the color noise.
2DNR supports the following features:
Support the independent configuration of Y component and UV component denoising intensity
Support the independent configuration of high-frequency and low-frequency noise suppression

12.3.3.17 Sharp

Sharp includes two functions: image Sharpening and boundary filtering. Sharpening can sharpen the intermediate frequency and high frequency respectively. Boundary filtering is to do another level of filtering on the Sharpening results, remove the boundary burrs, and finally add a level of general Sharpening to supplement the image details.
Sharp supports the following features:

Support image Sharpening and boundary filtering
Support Sharpening of medium-low frequency and high frequency respectively
Support adaptive filtering and specified coefficient filtering
Support detail enhancement

12.3.3.18 CSM

CSM module realizes data conversion from RGB to YUV format.

12.3.3.19 CONV422

CONV422 module change YUV444 format data to YUV422 format.

12.3.3.20 SCL-RESIZE

The Resize Modules get pictures in YCbCr 4:2:2 format, and scale them by an arbitrary factor up or down to a new format. See following Figure for a module overview:

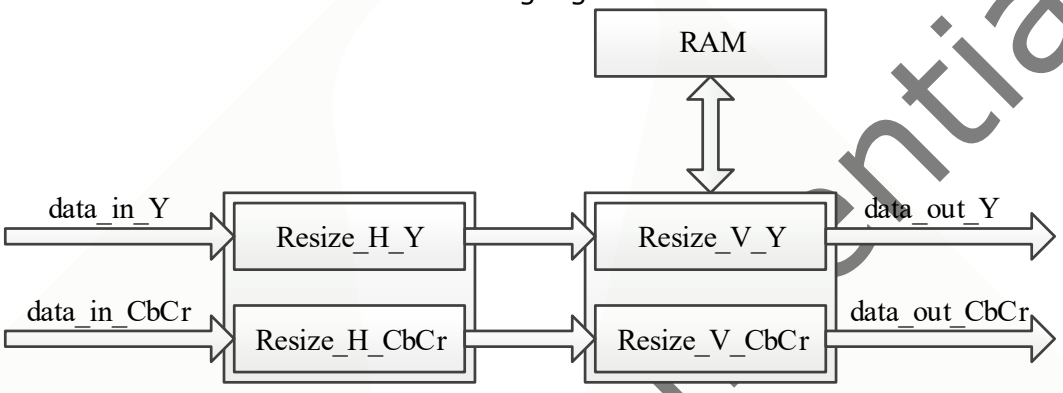


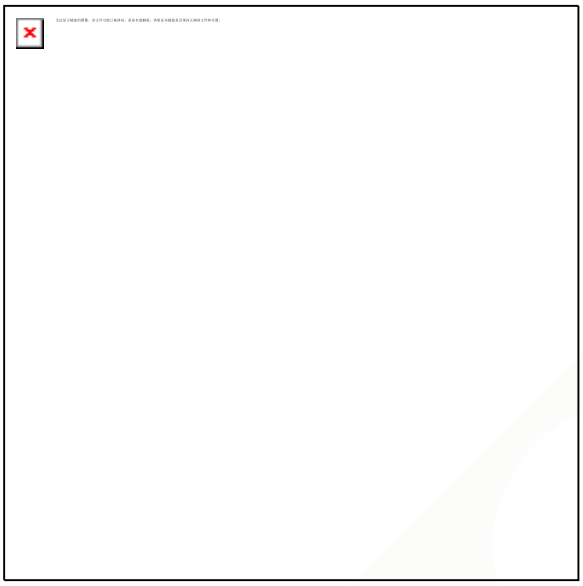
Fig. 12-5 Block Diagram of the Resize Module

The Resize module is configurable for horizontal and vertical up- or down-scaling. Discrete values for the scaling factors of the luminance and the two chrominance components allow conversion between YUV4:2:2 and YUV4:2:0 color format and support of uneven line width.
Phase shift registers are provided to shift the output pixel positions with respect to the input pixel positions. This allows for e.g. format conversion between cosited and non-cosited color schemes.
In sensor mode this block supports only down-scaling because of the sensor cannot be stopped from delivering data during one frame.
The Resize module is able to process luminance and chrominance data independently, i.e. there are separate pipelines for luminance and chrominance processing using dedicated scale factors and phase offsets. This allows format conversion to be done by the Resize block (YCbCr 4:2:2 to 4:2:0, 4:1:1, 4:1:0).

12.3.3.21 FLASH_LIGHT

The sensor interface supports triggering of a LED or tube flash light. To control a flash light device, the flash light output and the prelight output can be used. A trigger event could active both the flash light and the prelight. This event may either be a positive or negative edge from the camera or a positive edge from any other trigger source at the input port 'vds_vsync'.
Programming respective configuration register can determind the signal polarity, flash delay time and flash light time.

12.3.4 3A



12.3.4.1 AF

AF realizes the function of auto focus. The main part of auto focus control will be completed in the software: the search algorithm for the maximum definition in the image will be realized in the software, and the motion of the lens will be controlled by the software. The hardware AF module mainly realizes the measurement of image definition by configuring the configuration register. Filtering and gamma are added to facilitate the dark field processing.It supports a 15x15 size window and a separate window. Because it's input data format is raw, AF here is named RAWAF.

12.3.4.2 AE

AE realizes the function of automatic exposure processing. The input source is raw format. Two versions of AE are used here named RAWAE_BIG and RAWAE_LITE here. There are three AE modules here, two are RAWAE_BIG and one is RAWAE_LITE.The difference between RAWAE_BIG and RAWAE_LITE is that RAWAE_BIG supports 15x15 statistics window while RAWAE_LITE supports 5x5 statistics window.

12.3.4.3 AWB

The AWB module provides the white balance function, and configures the gains of the R, Gr, Gb, and B components. Because it's input data format is raw, AWB here is named RAWAWB. RAWAWB has 3 engines for finding valid white points(XY UV and 3DYUV domain).
It supports a 15x15 size window for white points or all points. It accumulates R G B channel data of all white points in XY domain for small normal and big window and for 7source lights.

12.3.4.4 HIST

Hist counts the number of pixels with the same or similar values. In general, a histogram is a graphical representation of the pattern of change that exists in the intensity value of a color or luminance plane. It is often shown as a vertical bar chart to indicate the frequency level of data collected over a specific range. The measurement can be used in different applications. The common application is to display the information of the end user, or to improve the exposure control and so on.
Two versions of HIST are named RAWHIST_BIG and RAWHIST_LITE here. Each AE follows a HIST, RAWAE_BIG follows RAWHIST_BIG, RAWAE_LITE follows RAWHIST_LITE. Both HIST have 256 bins for R G B or Y channel. The difference between RAWHIST_BIG and RAWHIST_LITE is same with AE.

12.3.4.5 PDAF

PDAF(Phase Detection Auto Focus) module here replaces the PDAF points inside the raw input data with corresponding 3x3 median data.

12.4 Register Description

The ISP uses a distributed configuration register scheme. So there is no central unit containing all programming registers, but all sub-modules contain their own programming

registers. An address space is reserved for each sub-module inside the total ISP Controller

Table 12-2 ISP module base address

Module	Description	Offset Address
BLS	Black-level-subtraction	0x3000
AWB_GAIN	Auto White Balance Gain	0x3200
DPCC	Defect Pixel Cluster Correction	0x3400
HDRMGE	High Dynamic Range Merge	0x3800
BAYNR	RAW noise reduction	0X3A00
BAY3D	Temporal noise reduction in raw space	0x3A80
LSC	Lens shade correction	0X2200
HDRTMO	High Dynamic Range Tone mapping	0x3900
GIC	Color imbalance correction	0X2F00
DEBAYER	Debayer	0X2500
CCM	Color Correct Matrix	0X0700
GAMMA_OUT	GAMMA OUT	0X0900
2DNR-YNR	filter the noise of Y component	0X2700
2DNR-CNR	filter the noise of C component	0X2800
SHARP	image Sharpening and boundary filtering	0X2900
LDCH	Lens-distortion in Horizontal	0X2B00
DHAZ	De-haze	0X3C00
3DLUT	3D look up table	0X3E00
SELF_RESIZE	main resize	0X0C00
	Scale self-resize	0X1000
ISP_Core	ISP top module	0X0400
FLASH	ISP flash light	0x0660
SHUTTER	ISP mech shutter	0x0680
CTRL	Marvin top ctrl	0X0000
RAWAF	auto focus measurement	0x4D00
RAWAE_LITE	auto exposure lite version	0x4500
RAWAE_BIG	auto exposure big version	0X4400
RAWAWB	auto white balancing	0X5000
RAWHIST_LITE	histogram calculation lite	0x4900
RAWHIST_BIG	histogram calculation big	0x4800,0x4A00,0x4B00

12.4.1 Registers Summary

12.4.1.1 MIPI

Name	Offset	Size	Reset Value	Description
CSI2RX_1C00_CTRL0	0x0000	W	0x20820000	Version of the CSI-2 host controller 0
CSI2RX_1C00_CTRL1	0x0004	W	0x00032103	Version of the CSI-2 host controller 1
CSI2RX_1C00_CTRL2	0x0008	W	0x00000000	Version of the CSI-2 host controller 2
CSI2RX_1C00_CSI2_RESETN	0x0010	W	0x00000003	CSI-2 controller reset
CSI2RX_1C00_PHY_STATE_RO	0x0014	W	0x00000000	General settings for all blocks
CSI2RX_1C00_DATA_IDS_1	0x0018	W	0x0000002b	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 0)Data IDs for which IDI reports line boundary matching errors
CSI2RX_1C00_DATA_IDS_2	0x001c	W	0x00000000	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 1)Data IDs for which IDI reports line boundary matching errors
CSI2RX_1C00_ERR_PHY	0x0020	W	0x00000000	Phy error state register
CSI2RX_1C00_ERR_PACKET	0x0024	W	0x00000000	Error of packet analysis
CSI2RX_1C00_ERR_OVERFLOW	0x0028	W	0x00000000	Error state overflow register
CSI2RX_1C00_ERR_STAT	0x002c	W	0x00000000	Error state
CSI2RX_1C00_MASK_PHY	0x0030	W	0x00000000	Phy error state register
CSI2RX_1C00_MASK_PACKET	0x0034	W	0x00000000	Error state register 2
CSI2RX_1C00_MASK_OVERFLOW	0x0038	W	0x00000000	Error state overflow register
CSI2RX_1C00_MASK_STAT	0x003c	W	0x00000000	Error state register 3
CSI2RX_1C00_RAW0_WR_CTRL	0x0040	W	0x002e0200	RAW0_WR control register. the channel that write csi pic data to ddr
CSI2RX_1C00_RAW0_WR_LINECNT_RO	0x0044	W	0x00000000	RAW0_WR line counter
CSI2RX_1C00_RAW0_WR_PIC_SIZE	0x0048	W	0x00000000	RAW0_WR picture size
CSI2RX_1C00_RAW0_WR_PIC_OFF	0x004c	W	0x00000000	RAW0_WR picture offset

CSI2RX_1C00_RAW1_WR_CTRL	0x0050	W	0x00000200	RAW1_WR control register
CSI2RX_1C00_RAW1_WR_LINECNT_RO	0x0054	W	0x00000000	RAW1_WR line counter
CSI2RX_1C00_RAW1_WR_PIC_SIZE	0x0058	W	0x00000000	RAW1_WR picture size
CSI2RX_1C00_RAW1_WR_PIC_OFF	0x005c	W	0x00000000	RAW1_WR picture offset
CSI2RX_1C00_RAW2_WR_CTRL	0x0060	W	0x00000100	RAW2_WR control register
CSI2RX_1C00_RAW2_WR_LINECNT_RO	0x0064	W	0x00000000	RAW2_WR line counter
CSI2RX_1C00_RAW2_WR_PIC_SIZE	0x0068	W	0x00000000	RAW2_WR picture size
CSI2RX_1C00_RAW2_WR_PIC_OFF	0x006c	W	0x00000000	RAW2_WR picture offset
CSI2RX_1C00_RAW3_WR_CTRL	0x0070	W	0x00000800	RAW3_WR control register
CSI2RX_1C00_RAW3_WR_LINECNT_RO	0x0074	W	0x00000000	RAW3_WR line counter
CSI2RX_1C00_RAW3_WR_PIC_SIZE	0x0078	W	0x00000000	RAW3_WR picture size
CSI2RX_1C00_RAW3_WR_PIC_OFF	0x007c	W	0x00000000	RAW3_WR picture offset
CSI2RX_1C00_RAW_RD_CTRL	0x0080	W	0x00000000	RAW_RD control register, the channel that read pic data from ddr
CSI2RX_1C00_RAW_RD_LINECNT_RO	0x0084	W	0x00000000	RAW_RD line counter
CSI2RX_1C00_RAW_RD_PIC_SIZE	0x0088	W	0x00000000	RAW_RD picture size
CSI2RX_1C00_RAW2_RD_LINECNT_RO	0x008c	W	0x00000000	RAW2_RD line counter
CSI2RX_1C00_RAWFBC_CTRL	0x0090	W	0x00000011	Raw fbc enable register
CSI2RX_1C00_ESPHDR_LCNT	0x0094	W	0x00010004	Parameter configuration of line counter mode
CSI2RX_1C00_ESPHDR_IDCD	0x0098	W	0x12121211	Parameter configuration of identification code mode
CSI2RX_1C00_ESPHDR_CTRL	0x009c	W	0x00000000	Especial HDR control
CSI2RX_1C00_VC0_FRAME_NUM_RO	0x00a0	W	0x00000000	VC0 current Frame Number
CSI2RX_1C00_VC1_FRAME_NUM_RO	0x00a4	W	0x00000000	VC1 current Frame Number

CSI2RX_1C00_VC2_FRAME_NUM_RO	0x00a8	W	0x00000000	VC2 current Frame Number
CSI2RX_1C00_VC3_FRAME_NUM_RO	0x00ac	W	0x00000000	VC3 current Frame Number
CSI2RX_1C00_ISP_LINECNT_RO	0x00b0	W	0x00000000	Current Line Counter
CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO	0x00b4	W	0x00000000	HDR ibuf status
CSI2RX_1C00_RAW_WR_IBUF3_STATUS_RO	0x00b8	W	0x00000000	HDR ibuf3 status
CSI2RX_1C00_CUR_HEADER_RO	0x00c4	W	0x00000000	Read onlysw_csi_ro_phyio_en == 1'b1 :rxdatahssw_csi_ro_phyio_en == 1'b0 :ro_csi_cur_header
CSI2RX_1C00_FPN_CTRL	0x00d0	W	0x00000000	FPN ctrl register
CSI2RX_1C00_FPN_TABLE_CTRL	0x00d4	W	0x00000001	FPN data write ctrl registerthe memory write address celars when finish
CSI2RX_1C00_FPN_TABLE_DATA	0x00d8	W	0x00000000	FPN data register to memoryFPN data to memory, the memory write address add 1 after write
CSI2RX_1C00_CSI_Y_STAT_CTRL	0x00f0	W	0x00000003	Y statistic ctrl
CSI2RX_1C00_CSI_Y_STAT_RO	0x00f4	W	0x00000000	Y statistic value read out with ahb
CSI2RX_1C00_VERSION	0x00fc	W	0x02021812	Version of the CSI-2 host controller

12.4.1.2 MI

Name	Offset	Size	Reset Value	Description
MI_1400_MI_WR_CTRL	0x0000	W	0x000a0000	Global write control register
MI_1400_MI_WR_INIT	0x0004	W	0x00000020	Control register for address init and skip function
MI_1400_MI_MP_WR_Y_BASE	0x0008	W	0x00000000	Base address for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_SIZE	0x000c	W	0x00000000	Size of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT	0x0010	W	0x00000000	Offset counter init value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_START	0x0014	W	0x00000000	Offset counter start value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS	0x0018	W	0x00000000	Fill level interrupt offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE	0x001c	W	0x00000000	Base address for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE	0x0020	W	0x00000000	Size of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT	0x0024	W	0x00000000	Offset counter init value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_START	0x0028	W	0x00000000	Offset counter start value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE	0x002c	W	0x00000000	Base address for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE	0x0030	W	0x00000000	Size of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT	0x0034	W	0x00000000	Offset counter init value for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_START	0x0038	W	0x00000000	Offset counter start value for main picture Cr component ring buffer
MI_1400_MI_SP_WR_Y_BASE	0x003c	W	0x00000000	Base address for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE	0x0040	W	0x00000000	Size of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT	0x0044	W	0x00000000	Offset counter init value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_START	0x0048	W	0x00000000	Offset counter start value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_LLENGTH	0x004c	W	0x00000000	Line length of self picture Y component
MI_1400_MI_SP_WR_CB_BASE	0x0050	W	0x00000000	Base address for self picture Cb component ring buffer

MI_1400_MI_SP_WR_CB_SIZE	0x0054	W	0x00000000	Size of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT	0x0058	W	0x00000000	Offset counter init value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_START	0x005c	W	0x00000000	Offset counter start value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE	0x0060	W	0x00000000	Base address for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE	0x0064	W	0x00000000	Size of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT	0x0068	W	0x00000000	Offset counter init value for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT_START	0x006c	W	0x00000000	Offset counter start value for self picture Cr component ring buffer
MI_1400_MI_WR_BYTE_CNT	0x0070	W	0x00000000	Counter value of JPEG or RAW data bytes
MI_1400_MI_WR_CTRL_SHD	0x0074	W	0x00000000	Global control internal shadow register
MI_1400_MI_MP_WR_Y_BASE_SHD	0x0078	W	0x00000000	Base address shadow register for main picture Y component, JPEG or raw data ring buffer
MI_1400_MI_MP_WR_Y_SIZE_SHD	0x007c	W	0x00000000	Size shadow register of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD	0x0080	W	0x00000000	Current offset counter of main picture Y component, JPEG or raw data ring buffe
MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD	0x0084	W	0x00000000	Shadow register of fill level interrupt offset value for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE_SHD	0x0088	W	0x00000000	Base address shadow register for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE_SHD	0x008c	W	0x00000000	Size shadow register of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD	0x0090	W	0x00000000	Current offset counter of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE_SHD	0x0094	W	0x00000000	Base address shadow register for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE_SHD	0x0098	W	0x00000000	Size shadow register of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD	0x009c	W	0x00000000	Current offset counter of main picture Cr component ring buffer

MI_1400_MI_SP_WR_Y_BASE_SHD	0x00a0	W	0x00000000	Base address shadow register for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE_SHD	0x00a4	W	0x00000000	Size shadow register of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD	0x00a8	W	0x00000000	Current offset counter of self picture Y component ring buffer
MI_1400_MI_SP_WR_CB_BASE_AD_SHD	0x00b0	W	0x00000000	Base address shadow register for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_SIZE_SHD	0x00b4	W	0x00000000	Size shadow register of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD	0x00b8	W	0x00000000	Current offset counter of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE_AD_SHD	0x00bc	W	0x00000000	Base address shadow register for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE_SHD	0x00c0	W	0x00000000	Size shadow register of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD	0x00c4	W	0x00000000	Current offset counter of self picture Cr component ring buffer
MI_1400_MI_RD_Y_PIC_START_AD	0x00c8	W	0x00000000	Y component image start address
MI_1400_MI_RD_Y_PIC_WIDTH	0x00cc	W	0x00000000	Y component image width
MI_1400_MI_RD_Y_LLENGTH	0x00d0	W	0x00000000	Y component original line length
MI_1400_MI_RD_Y_PIC_SIZE	0x00d4	W	0x00000000	Y component image size
MI_1400_MI_RD_CB_PIC_START_AD	0x00d8	W	0x00000000	Cb component image start address
MI_1400_MI_RD_CR_PIC_START_AD	0x00e8	W	0x00000000	Cr component image start address
MI_1400_MI_IMSC	0x00f8	W	0x00000000	Interrupt Mask ('1': interrupt active, '0': interrupt masked)
MI_1400_MI_RIS	0x00fc	W	0x00000000	Raw Interrupt Statu
MI_1400_MI_MIS	0x0100	W	0x00000000	Masked Interrupt Status
MI_1400_MI_ICR	0x0104	W	0x00000000	Interrupt Clear Register
MI_1400_MI_ISR	0x0108	W	0x00000000	Interrupt Set Register
MI_1400_MI_STATUS	0x010c	W	0x00000000	MI Status Register
MI_1400_MI_STATUS_CLR	0x0110	W	0x00000000	MI Status Clear Register
MI_1400_MI_SP_WR_Y_PIC_WIDTH	0x0114	W	0x00000000	Y component image width for self picture

MI_1400_MI_SP_WR_Y_PIC_HEIGHT	0x0118	W	0x00000000	Y component image height for self picture
MI_1400_MI_SP_WR_Y_PIC_SIZE	0x011c	W	0x00000000	Y component image size for self picture
MI_1400_MI_RD_CTRL	0x0120	W	0x00000000	DMA read control register
MI_1400_MI_RD_START	0x0124	W	0x00000000	DMA start register
MI_1400_MI_RD_STATUS	0x0128	W	0x00000000	DMA status register
MI_1400_MI_WR_PIXEL_CNT	0x012c	W	0x00000000	Counter value for defect pixel list
MI_1400_MI_MP_WR_Y_BASE2	0x0130	W	0x00000000	Base address 2 (ping pong) for main picture Y component
MI_1400_MI_MP_WR_CB_BASE2	0x0134	W	0x00000000	Base address 2 (ping pong) for main picture CB component
MI_1400_MI_MP_WR_CR_BASE2	0x0138	W	0x00000000	Base address 2 (ping pong) for main picture CR component
MI_1400_MI_SP_WR_Y_BASE2	0x013c	W	0x00000000	Base address 2 (ping pong) for self picture Y component
MI_1400_MI_SP_WR_CB_BASE2	0x0140	W	0x00000000	Base address 2 (ping pong) for self picture CB component
MI_1400_MI_SP_WR_CR_BASE2	0x0144	W	0x00000000	Base address 2 (ping pong) for self picture CR component
MI_1400_MI_WR_XTD_FORMAT_CTRL	0x0148	W	0x00000000	Extended Storage Format Control for main, self and dma read path
MI_1400_MI_WR_ID	0x0154	W	0x65432100	AXI write id group1
MI_1400_MI_MP_WR_Y_IRQ_OFFS2	0x01e0	W	0x00000000	Fill level interrupt2 offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD	0x01e4	W	0x00000000	Shadow register of fill level interrupt2 offset value for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_LLENGTH	0x01e8	W	0x00000000	Line length of main picture Y component
MI_1400_MI_WR_CTRL2	0x0400	W	0x00000000	New path control register
MI_1400_MI_WR_ID2	0x0404	W	0x00000000	AXI write id group2
MI_1400_MI_RD_CTRL2	0x0408	W	0x00250000	DMA path control register
MI_1400_MI_RD_ID	0x040c	W	0x00000000	AXI read id group
MI_1400_MI_RD_FIFO_LEVEL	0x041c	W	0x00000000	DMA read fifo level for generating hurry signal
MI_1400_RAW0_WR_BASE	0x0420	W	0x00000000	Base address for mipi raw0 tx;raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_WR_SIZE	0x0424	W	0x00000000	Size of raw0 tx dataraw write function move to VICAP, not support in ISP3.X....

MI_1400_RAW0_WR_LENGTH	0x0428	W	0x00000000	Line length of raw0 tx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_WR_BASE_SHD	0x042c	W	0x00000000	Base address shadow register for raw0 tx data ring bufferraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_WR_BASE	0x0430	W	0x00000000	Base address for mipi raw1 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_WR_SIZE	0x0434	W	0x00000000	Size of raw1 tx dataraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_WR_LENGTH	0x0438	W	0x00000000	Line length of raw1 tx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_WR_BASE_SHD	0x043c	W	0x00000000	Base address shadow register for raw1 tx data ring bufferraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW2_WR_BASE	0x0440	W	0x00000000	Base address for mipi raw2 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW2_WR_SIZE	0x0444	W	0x00000000	Size of raw2 tx dataraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW2_WR_LENGTH	0x0448	W	0x00000000	Line length of raw2 tx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW2_WR_BASE_SHD	0x044c	W	0x00000000	Base address shadow register for raw2 tx data ring bufferraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW3_WR_BASE	0x0450	W	0x00000000	Base address for mipi raw3 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW3_WR_SIZE	0x0454	W	0x00000000	Size of raw3 tx dataraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW3_WR_LENGTH	0x0458	W	0x00000000	Line length of raw3 tx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW3_WR_BASE_SHD	0x045c	W	0x00000000	Base address shadow register for raw3 tx data ring bufferraw write function move to VICAP, not support in ISP3.X....

MI_1400_RW0_WR_LAST_FRAME_ADDR	0x0460	W	0x00000000	Last address for raw0 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RW1_WR_LAST_FRAME_ADDR	0x0464	W	0x00000000	Last address for raw1 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RW2_WR_LAST_FRAME_ADDR	0x0468	W	0x00000000	Last address for raw2 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RW3_WR_LAST_FRAME_ADDR	0x046c	W	0x00000000	Last address for raw3 txraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_BASE	0x0470	W	0x00000000	Base address for mipi raw0 rxraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_LENGTH	0x0474	W	0x00000000	Line length of raw0 rx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_BASE_SHD	0x0478	W	0x00000000	Base shadow address for mipi raw0 rx. Update mode include hdr_dbg read pulse.raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_BASE	0x0480	W	0x00000000	Base address for mipi raw1 rxraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_LENGTH	0x0484	W	0x00000000	Line length of raw1 rx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_BASE_SHD	0x0488	W	0x00000000	Base shadow address for mipi raw1 rx. Update mode include hdr_dbg read pulse.raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_BASE	0x0490	W	0x00000000	Base address for mipi raws rxraw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_LENGTH	0x0494	W	0x00000000	Line length of raws rx (virtual width)raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_BASE_SHD	0x0498	W	0x00000000	Base shadow address for mipi rawsrx. Update mode include hdr_dbg read pulse.raw write function move to VICAP, not support in ISP3.X....

MI_1400_LUT_3D_RD_BASE	0x0540	W	0x00000000	Base address for 3d lut read
MI_1400_LUT_LSC_RD_BASE	0x0544	W	0x00000000	Base address for lsc lut read
MI_1400_LUT_LDCH_RD_BASE	0x0548	W	0x00000000	Base address for ldch lut read
MI_1400_LUT_3D_RD_WSIZE	0x0550	W	0x000002d9	3d lut word size
MI_1400_LUT_LSC_RD_WSIZE	0x0554	W	0x00000000	3d lut word size
MI_1400_LUT_LDCH_RD_H_WSIZE	0x0558	W	0x00000000	Ldch lut word size
MI_1400_LUT_LDCH_RD_V_SIZE	0x055c	W	0x00000000	Ldch lut v_size
MI_1400_DBR_WR_BASE	0x0560	W	0x00000000	Base address for mimux write, sws reuse
MI_1400_DBR_WR_SIZE	0x0564	W	0x00000000	Size of mimux write data
MI_1400_DBR_WR_LENGTH	0x0568	W	0x00000000	Line length of mimux write (virtual width)
MI_1400_DBR_WR_BASE_SHD	0x056c	W	0x00000000	Base address shadow register for mimux write data ring buffer
MI_1400_DBR_RD_BASE	0x0570	W	0x00000000	Base address for mimux read
MI_1400_DBR_RD_LENGTH	0x0574	W	0x00000000	Line length of mimux read (virtual width)
MI_1400_DBR_RD_BASE_SHD	0x0578	W	0x00000000	Base shadow address for mimux read
MI_1400_SWS_3A_WR_BASE	0x057c	W	0x00000000	AXI write 3A stats data to DDR address
MI_1400_GAIN_WR_BASE	0x0580	W	0x00000000	Base address for mimux write
MI_1400_GAIN_WR_SIZE	0x0584	W	0x00000000	Size of mimux write data
MI_1400_GAIN_WR_LENGTH	0x0588	W	0x00000000	Line length of mimux write (virtual width)
MI_1400_GAIN_WR_BASE2	0x058c	W	0x00000000	Base address 2 for mimux write
MI_1400_GAIN_WR_BASE_SHD	0x0590	W	0x00000000	Base address shadow register for mimux write data ring buffer
MI_1400_BAY3D_WR_BASE	0x05a0	W	0x00000000	Base address for bayer 3dnr write
MI_1400_BAY3D_WR_SIZE	0x05a4	W	0x00000000	Size of bayer 3dnr write data
MI_1400_BAY3D_WR_LENGTH	0x05a8	W	0x00000000	Line length of bayer 3dnr write (virtual width)
MI_1400_BAY3D_WR_BASE_SHD	0x05ac	W	0x00000000	Base address shadow register for bayer 3dnr write data ring buffer

MI_1400_BAY3D_RD_BASE	0x05b0	W	0x00000000	Base address for mimux read
MI_1400_BAY3D_RD_LENGTH	0x05b4	W	0x00000000	Line length of mimux read (virtual width)
MI_1400_BAY3D_RD_BASE_SHD	0x05b8	W	0x00000000	Base shadow address for mimux read

12.4.1.3 BLS

Name	Offset	Size	Reset Value	Description
ISP_BLS_3000_CTRL	0x0000	W	0x00000000	Global control register
ISP_BLS_3000_SAMPLES	0x0004	W	0x00000000	Samples register
ISP_BLS_3000_H1_START	0x0008	W	0x00000000	Window 1 horizontal start
ISP_BLS_3000_H1_STOP	0x000c	W	0x00000000	Window 1 horizontal stop
ISP_BLS_3000_V1_START	0x0010	W	0x00000000	Window 1 vertical start
ISP_BLS_3000_V1_STOP	0x0014	W	0x00000000	Window 1 vertical stop
ISP_BLS_3000_H2_START	0x0018	W	0x00000000	Window 2 horizontal start
ISP_BLS_3000_H2_STOP	0x001c	W	0x00000000	Window 2 horizontal stop
ISP_BLS_3000_V2_START	0x0020	W	0x00000000	Window 2 vertical start
ISP_BLS_3000_V2_STOP	0x0024	W	0x00000000	Window 2 vertical stop
ISP_BLS_3000_A_FIXED	0x0028	W	0x00000000	Fixed black level A
ISP_BLS_3000_B_FIXED	0x002c	W	0x00000000	Fixed black level B
ISP_BLS_3000_C_FIXED	0x0030	W	0x00000000	Fixed black level C
ISP_BLS_3000_D_FIXED	0x0034	W	0x00000000	Fixed black level D
ISP_BLS_3000_A_MEASURED	0x0038	W	0x00000000	Measured black level A
ISP_BLS_3000_B_MEASURED	0x003c	W	0x00000000	Measured black level B
ISP_BLS_3000_C_MEASURED	0x0040	W	0x00000000	Measured black level C
ISP_BLS_3000_D_MEASURED	0x0044	W	0x00000000	Measured black level D
ISP_BLS_3000_BLS1_A_FIXED	0x0048	W	0x00000000	Register0000 Description
ISP_BLS_3000_BLS1_B_FIXED	0x004c	W	0x00000000	Register0001 Description
ISP_BLS_3000_BLS1_C_FIXED	0x0050	W	0x00000000	Register0002 Description
ISP_BLS_3000_BLS1_D_FIXED	0x0054	W	0x00000000	Register0000 Description

12.4.1.4 DPCC

Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_MODE	0x0000	W	0x00000004	Mode control for DPCC detection unit
ISP_DPCC_3400_OUTPUT_MODE	0x0004	W	0x00000003	Interpolation mode for correction unit
ISP_DPCC_3400_SET_USE	0x0008	W	0x00000007	DPCC methods set usage for detection
ISP_DPCC_3400_METHODS_SET_1	0x000c	W	0x00001d1d	Methods enable bits for SET_1
ISP_DPCC_3400_METHODS_SET_2	0x0010	W	0x00000707	Methods enable bits for SET_2
ISP_DPCC_3400_METHODS_SET_3	0x0014	W	0x00001f1f	Methods enable bits for SET_3
ISP_DPCC_3400_LINE_THRESH_1	0x0018	W	0x00000808	Line threshold SET_1
ISP_DPCC_3400_LINE_MAD_FAC_1	0x001c	W	0x00000404	Mean Absolute Difference (MAD) factor for Line check set 1
ISP_DPCC_3400_PG_FAC_1	0x0020	W	0x00000403	Peak gradient factor for set 1
ISP_DPCC_3400_RND_THRESH_1	0x0024	W	0x00000a0a	Rank Neighbor Difference threshold for set 1
ISP_DPCC_3400_RG_FAC_1	0x0028	W	0x00002020	Rank gradient factor for set 1
ISP_DPCC_3400_LINE_THRESH_2	0x002c	W	0x0000100c	Line threshold set 2
ISP_DPCC_3400_LINE_MAD_FAC_2	0x0030	W	0x00001810	Mean Absolute Difference (MAD) factor for Line check set 2
ISP_DPCC_3400_PG_FAC_2	0x0034	W	0x00000403	Peak gradient factor for set 2
ISP_DPCC_3400_RND_THRESH_2	0x0038	W	0x00000808	Rank Neighbor Difference threshold for set 2
ISP_DPCC_3400_RG_FAC_2	0x003c	W	0x00000808	Rank gradient factor for set 2
ISP_DPCC_3400_LINE_THRESH_3	0x0040	W	0x00002020	Line threshold set 3
ISP_DPCC_3400_LINE_MAD_FAC_3	0x0044	W	0x00000404	Mean Absolute Difference (MAD) factor for Line check set 3
ISP_DPCC_3400_PG_FAC_3	0x0048	W	0x00000403	Peak gradient factor for set 3
ISP_DPCC_3400_RND_THRESH_3	0x004c	W	0x00000806	Rank Neighbor Difference threshold for set 3
ISP_DPCC_3400_RG_FAC_3	0x0050	W	0x00000404	Rank gradient factor for set 3

ISP_DPCC_3400_RO_LIMITS	0x0054	W	0x00000a0a	Rank Order Limits
ISP_DPCC_3400_RND_OFFS	0x0058	W	0x00000fff	Differential Rank Offsets for Rank Neighbor Difference
ISP_DPCC_3400_BPT_CTRL	0x005c	W	0x00000000	Bad pixel table settings
ISP_DPCC_3400_BPT_NUMBER	0x0060	W	0x00000000	Number of entries for bad pixel table (table based correction)
ISP_DPCC_3400_BPT_ADDR	0x0064	W	0x00000000	TABLE Start Address for table-based correction algorithm
ISP_DPCC_3400_BPT_DATA	0x0068	W	0x00000000	TABLE DATA register for read and write access of table RAM
ISP_DPCC_3400_BP_CNT	0x006c	W	0x00000000	Number of entries for bad pixel table (table based correction)
ISP_DPCC_3400_PDAF_EN	0x0070	W	0x00000000	Pdaf enable
ISP_DPCC_3400_PDAF_POINT_EN	0x0074	W	0x00000000	Enable for each pdaf point.
ISP_DPCC_3400_PDAF_OFFSET	0x0078	W	0x00000000	Pdaf point offset postion in wrapper
ISP_DPCC_3400_PDAF_WRAP	0x007c	W	0x00000000	Pdaf pattern size
ISP_DPCC_3400_PDAF_SCOPE	0x0080	W	0x00000000	The number of dpcc pattern
ISP_DPCC_3400_PDAF_POINT_0	0x0084	W	0x00000000	Point0 & point1 coordinate
ISP_DPCC_3400_PDAF_POINT_1	0x0088	W	0x00000000	Point2 & point3 coordinate
ISP_DPCC_3400_PDAF_POINT_2	0x008c	W	0x00000000	Point4 & point5 coordinate
ISP_DPCC_3400_PDAF_POINT_3	0x0090	W	0x00000000	Point6 & point7 coordinate
ISP_DPCC_3400_PDAF_POINT_4	0x0094	W	0x00000000	Point8 & point9 coordinate
ISP_DPCC_3400_PDAF_POINT_5	0x0098	W	0x00000000	Point10 & point11 coordinate
ISP_DPCC_3400_PDAF_POINT_6	0x009c	W	0x00000000	Point12 & point13 coordinate
ISP_DPCC_3400_PDAF_POINT_7	0x00a0	W	0x00000000	Point14 & point15 coordinate
ISP_DPCC_3400_PDAF_FORWARD_MED	0x00a4	W	0x00000000	Median value = center point = pdaf point , selecet forward median value or backwrad medain value to replace pdaf point

12.4.1.5 HDRMGE

Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_CTRL	0x0000	W	0x00000004	Global ctrl
ISP_HDRMGE_3800_GAIN0	0x0008	W	0x01000400	Gain0 config of S-frame
ISP_HDRMGE_3800_GAIN1	0x000c	W	0x04000100	Gain1 config of M-frame
ISP_HDRMGE_3800_GAIN2	0x0010	W	0x00000040	Gain2 config of L-frame
ISP_HDRMGE_3800_CONS_DIFF	0x0014	W	0x00ff00ff	Lightzone config
ISP_HDRMGE_3800_DIFF_Y0	0x0020	W	0x00000000	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y1	0x0024	W	0x00c900c9	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y2	0x0028	W	0x01fa01fa	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y3	0x002c	W	0x02c002c0	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y4	0x0030	W	0x032f032f	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y5	0x0034	W	0x03700370	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y6	0x0038	W	0x03970397	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y7	0x003c	W	0x03b103b1	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y8	0x0040	W	0x03c203c2	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y9	0x0044	W	0x03cf03cf	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y10	0x0048	W	0x03d803d8	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y11	0x004c	W	0x03de03de	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y12	0x0050	W	0x03e403e4	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y13	0x0054	W	0x03e803e8	Y value of L-curve0,1 config
ISP_HDRMGE_3800_DIFF_Y14	0x0058	W	0x03eb03eb	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y15	0x005c	W	0x03ee03ee	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y16	0x0060	W	0x03f003f0	Y value of L-curve0,1

ISP_HDRMGE_3800_OVER_Y0	0x0070	W	0x00000000	Y value of ES-curve
ISP_HDRMGE_3800_OVER_Y1	0x0074	W	0x00000001	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y2	0x0078	W	0x00000004	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y3	0x007c	W	0x0000000e	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y4	0x0080	W	0x00000031	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y5	0x0084	W	0x00000098	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y6	0x0088	W	0x00000183	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y7	0x008c	W	0x000002b7	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y8	0x0090	W	0x00000386	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y9	0x0094	W	0x000003da	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y10	0x0098	W	0x000003f5	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y11	0x009c	W	0x000003fd	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y12	0x00a0	W	0x000003ff	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y13	0x00a4	W	0x000003ff	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y14	0x00a8	W	0x000003ff	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y15	0x00ac	W	0x000003ff	Y value of ES-curve config
ISP_HDRMGE_3800_OVER_Y16	0x00b0	W	0x000003ff	Y value of ES-curve config

12.4.1.6 BAY2DNR

Name	Offset	Size	Reset Value	Description
ISP_BAYNR_3A00_CTRL	0x0000	W	0x00000101	rawnr state register
ISP_BAYNR_3A00_DGAIN0	0x0004	W	0x04714000	rawnr dgain parameter
ISP_BAYNR_3A00_DGAIN1	0x0008	W	0x00000400	rawnr dgain parameter
ISP_BAYNR_3A00_PIXDIFF	0x000c	W	0x00003fff	rawnr dgain parameter
ISP_BAYNR_3A00_THLD	0x0010	W	0x03ff000a	luma ration0 and luma ration1 parameter
ISP_BAYNR_3A00_W1_STRENG	0x0014	W	0x00a303ff	channel weight and bialfter streng
ISP_BAYNR_3A00_SIGMAX01	0x0018	W	0x12101010	sigma x value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAX23	0x001c	W	0x16101410	sigma x value of segment 2 and 3
ISP_BAYNR_3A00_SIGMAX45	0x0020	W	0x1c101810	sigma x value of segment 4 and 5
ISP_BAYNR_3A00_SIGMAX67	0x0024	W	0x24102010	sigma x value of segment 6 and 7
ISP_BAYNR_3A00_SIGMAX89	0x0028	W	0x2c102810	sigma x value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAX1011	0x002c	W	0x34103010	sigma x value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAX1213	0x0030	W	0x3a103810	sigma x value of segment 12 and 13
ISP_BAYNR_3A00_SIGMAX1415	0x0034	W	0x40103c10	sigma x value of segment 14 and 15
ISP_BAYNR_3A00_SIGMAY01	0x0038	W	0x03000300	sigma y value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAY23	0x003c	W	0x03000300	sigma y value of segment 2 and 3
ISP_BAYNR_3A00_SIGMAY45	0x0040	W	0x02800280	sigma y value of segment 4 and 5
ISP_BAYNR_3A00_SIGMAY67	0x0044	W	0x02800280	sigma y value of segment 6 and 7
ISP_BAYNR_3A00_SIGMAY89	0x0048	W	0x02000200	sigma y value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAY1011	0x004c	W	0x02000200	sigma y value of segment 0 and 1
ISP_BAYNR_3A00_SIGMAY1213	0x0050	W	0x02000200	sigma y value of segment 12 and 13
ISP_BAYNR_3A00_SIGMAY1415	0x0054	W	0x01800200	sigma y value of segment 14 and 15

ISP_BAYNR_3A00_WRITD	0x0058	W	0x31d9b578	space weight of blal filter

12.4.1.7 BAY3DNR

Name	Offset	Size	Reset Value	Description
BAY3D_BAY3D_CTRL	0x0080	W	0x00000010	bayer 3dnr ctrl
BAY3D_BAY3D_KALRATIO	0x0084	W	0x01000100	sigma ratio,softthreshold weight
BAY3D_BAY3D_GLBPK2	0x0088	W	0x00000800	global pk gain
BAY3D_BAY3D_KALSTR	0x008c	W	0x01000100	exp curve strength
BAY3D_BAY3D_WGTLMT	0x0090	W	0x03800380	wgt1 limit
BAY3D_BAY3D_SIG_X0	0x0094	W	0x102d002d	sigma curve coordinate x
BAY3D_BAY3D_SIG_X1	0x0098	W	0x10331031	sigma curve coordinate x
BAY3D_BAY3D_SIG_X2	0x009c	W	0x10571053	sigma curve coordinate x
BAY3D_BAY3D_SIG_X3	0x00a0	W	0x30d73057	sigma curve coordinate x
BAY3D_BAY3D_SIG_X4	0x00a4	W	0x715770d7	sigma curve coordinate x
BAY3D_BAY3D_SIG_X5	0x00a8	W	0x715d715b	sigma curve coordinate x
BAY3D_BAY3D_SIG_X6	0x00ac	W	0x72dd725d	sigma curve coordinate x
BAY3D_BAY3D_SIG_X7	0x00b0	W	0x771d76dd	sigma curve coordinate x
BAY3D_BAY3D_SIG_Y0	0x00b4	W	0x0cc608ea	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y1	0x00b8	W	0x0e620a3c	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y2	0x00bc	W	0x08600da3	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y3	0x00c0	W	0x02300460	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y4	0x00c4	W	0x086d09f0	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y5	0x00c8	W	0x03d60152	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y6	0x00cc	W	0x06c60a61	sigma curve coordinate y
BAY3D_BAY3D_SIG_Y7	0x00d0	W	0x093e0f59	sigma curve coordinate y

12.4.1.8 LSC

Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_CTRL	0x0000	W	0x00000000	Lens shade control
ISP_LSC_2200_R_TABLE_ADDR	0x0004	W	0x00000000	Table RAM Address for red component
ISP_LSC_2200_GR_TABLE_ADDR	0x0008	W	0x00000000	Table RAM Address for green (red) component
ISP_LSC_2200_B_TABLE_ADDR	0x000c	W	0x00000000	Table RAM Address for blue component
ISP_LSC_2200_GB_TABLE_ADDR	0x0010	W	0x00000000	Table RAM Address for green (blue) component
ISP_LSC_2200_R_TABLE_DATA	0x0014	W	0x00000000	Sample table red
ISP_LSC_2200_GR_TABLE_DATA	0x0018	W	0x00000000	Sample table green (red)
ISP_LSC_2200_B_TABLE_DATA	0x001c	W	0x00000000	Sample table blue
ISP_LSC_2200_GB_TABLE_DATA	0x0020	W	0x00000000	Sample table green (blue)
ISP_LSC_2200_XGRAD_01	0x0024	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_23	0x0028	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_45	0x002c	W	0x00000000	Gradient table x
ISP_LSC_2200_XGRAD_67	0x0030	W	0x00000000	Gradient table x
ISP_LSC_2200_YGRAD_01	0x0034	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_23	0x0038	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_45	0x003c	W	0x00000000	Gradient table y
ISP_LSC_2200_YGRAD_67	0x0040	W	0x00000000	Gradient table y
ISP_LSC_2200_XSIZE_01	0x0044	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_23	0x0048	W	0x00000000	ISP_LSC_XSIZE_23
ISP_LSC_2200_XSIZE_45	0x004c	W	0x00000000	Size table
ISP_LSC_2200_XSIZE_67	0x0050	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_01	0x0054	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_23	0x0058	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_45	0x005c	W	0x00000000	Size table
ISP_LSC_2200_YSIZE_67	0x0060	W	0x00000000	Size table
ISP_LSC_2200_ISP_LSC_STATUS	0x0068	W	0x00000000	Lens shade status

12.4.1.9 HDR_DRC

Name	Offset	Size	Reset Value	Description
ISP_DRC_3900_CTRL0	0x0000	W	0x00000000	Global hdr-control-0
ISP_DRC_3900_CTRL1	0x0004	W	0x83904100	hdr-drc control1
ISP_DRC_3900_LPRATIO	0x0008	W	0x40000000	lp-ratio
ISP_DRC_3900_EXPLRATIO	0x000c	W	0x60001000	exp-ratio
ISP_DRC_3900_SIGMA	0x0010	W	0x00000000	edge, motion control signals
ISP_DRC_3900_SPACESGM	0x0014	W	0x0fe40f80	space sigma
ISP_DRC_3900_RANESGM	0x0018	W	0x04000400	range sigma
ISP_DRC_3900_BILAT	0x001c	W	0x00000010	bilateral config
ISP_DRC_3900_GAIN_Y0	0x0020	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y1	0x0024	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y2	0x0028	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y3	0x002c	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y4	0x0030	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y5	0x0034	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y6	0x0038	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y7	0x003c	W	0x04000400	curve gain Y0~Y16
ISP_DRC_3900_GAIN_Y8	0x0040	W	0x00000400	curve gain Y0~Y16
ISP_DRC_3900_COMPRES_Y0	0x0044	W	0x022e0000	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y1	0x0048	W	0x0634043f	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y2	0x004c	W	0x09d3080f	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y3	0x0050	W	0x0d190b80	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y4	0x0054	W	0x11790ea0	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y5	0x0058	W	0x16771413	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y6	0x005c	W	0x1ab618ac	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y7	0x0060	W	0x1e5c1c9a	curve compress Y0~Y16
ISP_DRC_3900_COMPRES_Y8	0x0064	W	0x00002000	curve compress Y0~Y16
ISP_DRC_3900_SCALE_Y0	0x0068	W	0x00020000	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y1	0x006c	W	0x004c0014	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y2	0x0070	W	0x017d00c1	curve scale Y0~Y16

ISP_DRC_3900_SCALE_Y3	0x0074	W	0x03040277	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y4	0x0078	W	0x042a0397	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y5	0x007c	W	0x05c704bb	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y6	0x0080	W	0x074706a4	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y7	0x0084	W	0x07e807b0	curve scale Y0~Y16
ISP_DRC_3900_SCALE_Y8	0x0088	W	0x00000800	curve scale Y0~Y16
ISP_DRC_3900_IIRWG_GAIN	0x008c	W	0x00000000	drc_min_ogain, drc_iir_weight

12.4.1.10 GIC

Name	Offset	Size	Reset Value	Description
ISP_GIC_CONTROL	0x0000	W	0x00000000	control register
ISP_GIC_DIFF_PARA1	0x0004	W	0x00000000	diff_gb calculate parameter register1
ISP_GIC_DIFF_PARA2	0x0008	W	0x00000000	diff_gb calculate parameter register2
ISP_GIC_DIFF_PARA3	0x000c	W	0x00000000	diff_gb calculate parameter register3
ISP_GIC_DIFF_PARA4	0x0010	W	0x00000000	diff_gb calculate parameter register4
ISP_GIC_NOISE_PARA1	0x0014	W	0x00000000	noise calculate parameter register1
ISP_GIC_NOISE_PARA2	0x0018	W	0x00000000	noise calculate parameter register2
ISP_GIC_NOISE_PARA3	0x001c	W	0x00000000	noise calculate parameter register1
ISP_GIC_SIGMA_VALUE0	0x0044	W	0x00000000	y0 to y1 value of sigma table
ISP_GIC_SIGMA_VALUE1	0x0048	W	0x00000000	y2 to y3 value of sigma table
ISP_GIC_SIGMA_VALUE2	0x004c	W	0x00000000	y4 to y5 value of sigma table
ISP_GIC_SIGMA_VALUE3	0x0050	W	0x00000000	y6 to y7 value of sigma table
ISP_GIC_SIGMA_VALUE4	0x0054	W	0x00000000	y8 to y9 value of sigma table
ISP_GIC_SIGMA_VALUE5	0x0058	W	0x00000000	y10 to y11 value of sigma table
ISP_GIC_SIGMA_VALUE6	0x005c	W	0x00000000	y12 to y13 value of sigma table
ISP_GIC_SIGMA_VALUE7	0x0060	W	0x00000000	y14 value of sigma table

12.4.1.11 DEBAYER

Name	Offset	Size	Reset Value	Description
ISP_DEBAYER_2500_CONTROL	0x0000	W	0x00000110	DEBAYER CONTROL
ISP_DEBAYER_2500_G_INTERP	0x0004	W	0x00006389	G INTERPOLATION REGISTER
ISP_DEBAYER_2500_G_INTERP_FILTER1	0x0008	W	0x000e60a2	THIS FILTER IS FOR GETTING THE EDGE OF LOW FREQUENCY
ISP_DEBAYER_2500_G_INTERP_FILTER2	0x000c	W	0x0002c4c2	THIS FILTER IS FOR GETTING THE DETAIL OF HIGH FREQUENCY
ISP_DEBAYER_2500_OFFSET	0x0010	W	0x00800401	OFFSET REGISTER
ISP_DEBAYER_2500_C_FILTER	0x0014	W	0x00020e05	C FILTER REGISTER

12.4.1.12 CCM

Name	Offset	Size	Reset Value	Description
ISP_CCM_0700_CTRL	0x0000	W	0x00000000	ISP CCM Enable
ISP_CCM_0700_COEFF0_R	0x0004	W	0x07b70065	CCM matrix R coefficient 0 & 1
ISP_CCM_0700_COEFF1_R	0x0008	W	0x000007e4	CCM matrix R coefficient 2 & offset
ISP_CCM_0700_COEFF0_G	0x000c	W	0x005807d9	CCM matrix G coefficient 0 & 1
ISP_CCM_0700_COEFF1_G	0x0010	W	0x000007cf	CCM matrix G coefficient 2 & offset
ISP_CCM_0700_COEFF0_B	0x0014	W	0x07b70002	CCM matrix B coefficient 0&1
ISP_CCM_0700_COEFF1_B	0x0018	W	0x00000046	CCM matrix B coefficient 2 & offset
ISP_CCM_0700_COEFF0_Y	0x001c	W	0x004b0026	The R&G coeff of RGB2Y calculation
ISP_CCM_0700_COEFF1_Y	0x0020	W	0x0000000f	The B coeff of RGB2Y calculation
ISP_CCM_0700_ALP_Y0	0x0024	W	0x04000400	CCM curve definition y0 & y1
ISP_CCM_0700_ALP_Y1	0x0028	W	0x04000400	CCM curve definition y2 & y3
ISP_CCM_0700_ALP_Y2	0x002c	W	0x04000400	CCM curve definition y4 & y5
ISP_CCM_0700_ALP_Y3	0x0030	W	0x04000400	CCM curve definition y6 & y7
ISP_CCM_0700_ALP_Y4	0x0034	W	0x04000400	CCM curve definition y8 & y9
ISP_CCM_0700_ALP_Y5	0x0038	W	0x04000400	CCM curve definition y10 & y11
ISP_CCM_0700_ALP_Y6	0x003c	W	0x04000400	CCM curve definition y12 & y13
ISP_CCM_0700_ALP_Y7	0x0040	W	0x04000400	CCM curve definition y14 & y15
ISP_CCM_0700_ALP_Y8	0x0044	W	0x00000400	CCM curve definition y16
ISP_CCM_0700_bound_bit	0x0048	W	0x00000000	curve inflection point , the value is 2^bound_bit.

12.4.1.13 GAMMA_OUT

Name	Offset	Size	Reset Value	Description
ISP_GAMMA_OUT_0900_CTRL	0x0000	W	0x00000000	Global control register
ISP_GAMMA_OUT_0900_OFFSET	0x0004	W	0x00000000	Offset config register
ISP_GAMMA_OUT_0900_Y0	0x0010	W	0x00010000	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y1	0x0014	W	0x00030002	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y2	0x0018	W	0x00050004	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y3	0x001c	W	0x00070006	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y4	0x0020	W	0x000a0008	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y5	0x0024	W	0x000e000c	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y6	0x0028	W	0x00140010	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y7	0x002c	W	0x001c0018	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y8	0x0030	W	0x00280020	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y9	0x0034	W	0x00380030	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y10	0x0038	W	0x00500040	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y11	0x003c	W	0x00700060	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y12	0x0040	W	0x00a00080	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y13	0x0044	W	0x00e000c0	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y14	0x0048	W	0x01400100	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y15	0x004c	W	0x01c00180	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y16	0x0050	W	0x02800200	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y17	0x0054	W	0x03800300	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y18	0x0058	W	0x05000400	Y value of gamma_out curve config register

ISP_GAMMA_OUT_0900_Y19	0x005c	W	0x07000600	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y20	0x0060	W	0x0a000800	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y21	0x0064	W	0x0e000c00	Y value of gamma_out curve config register
ISP_GAMMA_OUT_0900_Y22	0x0068	W	0x00000fff	Y value of gamma_out curve config register

12.4.1.14 DEHAZE_ENHANCE

Name	Offset	Size	Reset Value	Description
ISP_DHAZ_3C00_CTRL	0x0000	W	0x00000110	Dehaze control
ISP_DHAZ_3C00_ADP0	0x0004	W	0x1bf9c040	Dehaze self-adaption coefficant 0
ISP_DHAZ_3C00_ADP1	0x0008	W	0x00e6f0b4	Dehaze self-adaption coefficant 1
ISP_DHAZ_3C00_ADP2	0x000c	W	0x7dfafae6	Dehaze self-adaption coefficant 2
ISP_DHAZ_3C00_ADP_TMAX	0x0010	W	0x02000066	Dehaze self-adaption tmax
ISP_DHAZ_3C00_ADP_HIST0	0x0014	W	0x00044008	Dehaze self-adaption hist0
ISP_DHAZ_3C00_ADP_HIST1	0x0018	W	0x001000e6	Dehaze self-adaption hist1
ISP_DHAZ_3C00_ENHANCE	0x001c	W	0x060004cc	Dehaze enhance value
ISP_DHAZ_3C00_IIR0	0x0020	W	0x000f0108	Dehaze iir control0
ISP_DHAZ_3C00_IIR1	0x0024	W	0x07005f08	Dehaze iir control1
ISP_DHAZ_3C00_SOFT_CFG0	0x0028	W	0x00ccd200	Dehaze user config0
ISP_DHAZ_3C00_SOFT_CFG1	0x002c	W	0x020000cc	Dehaze user config1
ISP_DHAZ_3C00_BF_SIGMA	0x0030	W	0x00804d99	bilateral filter sigma
ISP_DHAZ_3C00_BF_WET	0x0034	W	0x01000080	bilateral filter weight
ISP_DHAZ_3C00_ENH_CURVE0	0x0038	W	0x00400000	enhance curve
ISP_DHAZ_3C00_ENH_CURVE1	0x003c	W	0x00c00080	enhance curve
ISP_DHAZ_3C00_ENH_CURVE2	0x0040	W	0x01400100	enhance curve
ISP_DHAZ_3C00_ENH_CURVE3	0x0044	W	0x01c00180	enhance curve
ISP_DHAZ_3C00_ENH_CURVE4	0x0048	W	0x02400200	enhance curve
ISP_DHAZ_3C00_ENH_CURVE5	0x004c	W	0x02c00280	enhance curve
ISP_DHAZ_3C00_ENH_CURVE6	0x0050	W	0x03400300	enhance curve
ISP_DHAZ_3C00_ENH_CURVE7	0x0054	W	0x03c00380	enhance curve
ISP_DHAZ_3C00_ENH_CURVE8	0x0058	W	0x000003ff	enhance curve
ISP_DHAZ_3C00_GAUS	0x005c	W	0x00020408	The gausi smoothed coefficient, 3*3window¤ /32 normalization.(h0+4*h1+4*h2=32)

ISP_DHAZ_3C00_CTRL_SHD	0x0060	W	0x00000000	Dehaze enable shandow read only
ISP_DHAZ_3C00_ADP_RD0	0x0064	W	0x00000000	Self_adaption read only
ISP_DHAZ_3C00_ADP_RD1	0x0068	W	0x00000000	Self_adaption read only
ISP_DHAZ_3C00_HIST_REG0	0x0070	W	0x00100000	Hist_rgb_iir_1 & hist_rgb_iir_0, read only
ISP_DHAZ_3C00_HIST_REG1	0x0074	W	0x00300020	Hist_rgb_iir_3 & hist_rgb_iir_2, read only
ISP_DHAZ_3C00_HIST_REG2	0x0078	W	0x00500040	Hist_rgb_iir_5 & hist_rgb_iir_4, read only
ISP_DHAZ_3C00_HIST_REG3	0x007c	W	0x00700060	Hist_rgb_iir_7 & hist_rgb_iir_6, read only
ISP_DHAZ_3C00_HIST_REG4	0x0080	W	0x00900080	Hist_rgb_iir_9 & hist_rgb_iir_8, read only
ISP_DHAZ_3C00_HIST_REG5	0x0084	W	0x00b000a0	Hist_rgb_iir_11 & hist_rgb_iir_10, read only
ISP_DHAZ_3C00_HIST_REG6	0x0088	W	0x00d000c0	Hist_rgb_iir_13 & hist_rgb_iir_12, read only
ISP_DHAZ_3C00_HIST_REG7	0x008c	W	0x00f000e0	Hist_rgb_iir_15 & hist_rgb_iir_14, read only
ISP_DHAZ_3C00_HIST_REG8	0x0090	W	0x01100100	Hist_rgb_iir_17 & hist_rgb_iir_16, read only
ISP_DHAZ_3C00_HIST_REG9	0x0094	W	0x01300120	Hist_rgb_iir_19 & hist_rgb_iir_18, read only
ISP_DHAZ_3C00_HIST_REG10	0x0098	W	0x01500140	Hist_rgb_iir_21 & hist_rgb_iir_20, read only
ISP_DHAZ_3C00_HIST_REG11	0x009c	W	0x01700160	Hist_rgb_iir_23 & hist_rgb_iir_22, read only
ISP_DHAZ_3C00_HIST_REG12	0x00a0	W	0x01900180	Hist_rgb_iir_25 & hist_rgb_iir_24, read only
ISP_DHAZ_3C00_HIST_REG13	0x00a4	W	0x01b001a0	Hist_rgb_iir_27 & hist_rgb_iir_26, read only
ISP_DHAZ_3C00_HIST_REG14	0x00a8	W	0x01d001c0	Hist_rgb_iir_29 & hist_rgb_iir_28, read only
ISP_DHAZ_3C00_HIST_REG15	0x00ac	W	0x01f001e0	Hist_rgb_iir_31 & hist_rgb_iir_30, read only
ISP_DHAZ_3C00_HIST_REG16	0x00b0	W	0x02100200	Hist_rgb_iir_33 & hist_rgb_iir_32, read only
ISP_DHAZ_3C00_HIST_REG17	0x00b4	W	0x02300220	Hist_rgb_iir_35 & hist_rgb_iir_34, read only
ISP_DHAZ_3C00_HIST_REG18	0x00b8	W	0x02500240	Hist_rgb_iir_37 & hist_rgb_iir_36, read only

ISP_DHAZ_3C00_HIST_REG19	0x00bc	W	0x02700260	Hist_rgb_iir_39 & hist_rgb_iir_38, read only
ISP_DHAZ_3C00_HIST_REG20	0x00c0	W	0x02900280	Hist_rgb_iir_41 & hist_rgb_iir_40, read only
ISP_DHAZ_3C00_HIST_REG21	0x00c4	W	0x02b002a0	Hist_rgb_iir_43 & hist_rgb_iir_42, read only
ISP_DHAZ_3C00_HIST_REG22	0x00c8	W	0x02d002c0	Hist_rgb_iir_45 & hist_rgb_iir_44, read only
ISP_DHAZ_3C00_HIST_REG23	0x00cc	W	0x02f002e0	Hist_rgb_iir_47 & hist_rgb_iir_46, read only
ISP_DHAZ_3C00_HIST_REG24	0x00d0	W	0x03100300	Hist_rgb_iir_49 & hist_rgb_iir_48, read only
ISP_DHAZ_3C00_HIST_REG25	0x00d4	W	0x03300320	Hist_rgb_iir_51 & hist_rgb_iir_50, read only
ISP_DHAZ_3C00_HIST_REG26	0x00d8	W	0x03500340	Hist_rgb_iir_53 & hist_rgb_iir_52, read only
ISP_DHAZ_3C00_HIST_REG27	0x00dc	W	0x03700360	Hist_rgb_iir_55 & hist_rgb_iir_54, read only
ISP_DHAZ_3C00_HIST_REG28	0x00e0	W	0x03900380	Hist_rgb_iir_57 & hist_rgb_iir_56, read only
ISP_DHAZ_3C00_HIST_REG29	0x00e4	W	0x03b003a0	Hist_rgb_iir_59 & hist_rgb_iir_58, read only
ISP_DHAZ_3C00_HIST_REG30	0x00e8	W	0x03d003c0	Hist_rgb_iir_61 & hist_rgb_iir_60, read only
ISP_DHAZ_3C00_HIST_REG31	0x00ec	W	0x03f003e0	Hist_rgb_iir_63 & hist_rgb_iir_62, read only

12.4.1.15 3DLUT

Name	Offset	Size	Reset Value	Description
ISP_3DLUT_3E00_CTRL	0x0000	W	0x00000000	3DLUT control register
ISP_3DLUT_3E00_UPDATE	0x0004	W	0x00000000	3DLUT lut update register

12.4.1.16 SELF_RESIZE

Name	Offset	Size	Reset Value	Description
SELF_RESIZE_0C00_1000_CTRL	0x0000	W	0x00000000	Global control register
SELF_RESIZE_0C00_1000_SCALE_HY	0x0004	W	0x00000000	Horizontal luminance scale factor register
SELF_RESIZE_0C00_1000_SCALE_HCB	0x0008	W	0x00000000	Horizontal chrominance scale factor register
SELF_RESIZE_0C00_1000_SCALE_HCR	0x000c	W	0x00000000	Horizontal chrominance scale factor register
SELF_RESIZE_0C00_1000_SCALE_VY	0x0010	W	0x00000000	Vertical luminance scale factor register
SELF_RESIZE_0C00_1000_SCALE_VC	0x0014	W	0x00000000	Vertical chrominance scale factor register The size of the output picture is calculated as follows:(size_out - 1) / (size_in - 1)) = scale,where size_in/out is the width or heigth of the in/output picture. The values of the MRSZ_SCALEregisters then have to be int(scale x 2^14)+1
SELF_RESIZE_0C00_1000_PHASE_HY	0x0018	W	0x00000000	Horizontal luminance phase register
SELF_RESIZE_0C00_1000_PHASE_HC	0x001c	W	0x00000000	Horizontal chrominance phase register
SELF_RESIZE_0C00_1000_PHASE_VY	0x0020	W	0x00000000	Vertical luminance phase register
SELF_RESIZE_0C00_1000_PHASE_VC	0x0024	W	0x00000000	Vertical chrominance phase register
SELF_RESIZE_0C00_1000_SCALE_LUT_ADDR	0x0028	W	0x00000000	Address pointer of up-scaling look up table
SELF_RESIZE_0C00_1000_SCALE_LUT	0x002c	W	0x00000000	Entry of up-scaling look up table
SELF_RESIZE_0C00_1000_CTRL_SHD	0x0030	W	0x00000000	Global control shadow register
SELF_RESIZE_0C00_1000_SCALE_HY_SHD	0x0034	W	0x00000000	Horizontal luminance scale factor shadow register
SELF_RESIZE_0C00_1000_SCALE_HCB_SHD	0x0038	W	0x00000000	Horizontal Cb scale factor shadow register
SELF_RESIZE_0C00_1000_SCALE_HCR_SHD	0x003c	W	0x00000000	Horizontal Cr scale factor shadow register
SELF_RESIZE_0C00_1000_SCALE_VY_SHD	0x0040	W	0x00000000	Vertical luminance scale factor shadow register
SELF_RESIZE_0C00_1000_SCALE_VC_SHD	0x0044	W	0x00000000	Vertical chrominance scale factor shadow register

SELF_RESIZE_0C00_1000_PHASE_HY_SHD	0x0048	W	0x00000000	Horizontal luminance phase shadow register
SELF_RESIZE_0C00_1000_PHASE_HC_SHD	0x004c	W	0x00000000	Horizontal chrominance phase shadow register
SELF_RESIZE_0C00_1000_PHASE_VY_SHD	0x0050	W	0x00000000	Vertical luminance phase shadow register
SELF_RESIZE_0C00_1000_PHASE_VC_SHD	0x0054	W	0x00000000	Vertical chrominance phase shadow register

12.4.1.17 ISP_TOP

Name	Offset	Size	Reset Value	Description
ISP_0400_CTRL0	0x0000	W	0x00006000	Global control register
ISP_0400_CTRL1	0x0004	W	0x0f800060	ISP acquisition properties
ISP_0400_ACQ_H_OFFS	0x0008	W	0x00000000	Horizontal input offset
ISP_0400_ACQ_V_OFFS	0x000c	W	0x00000000	Vertical input offset
ISP_0400_ACQ_H_SIZE	0x0010	W	0x10001000	Horizontal input size
ISP_0400_ACQ_V_SIZE	0x0014	W	0x00000c00	Vertical input size
ISP_0400_ACQ_NR_FRAMES	0x0018	W	0x00000000	Number of frames to be captured
ISP_0400_GAMMA_DX_LO	0x001c	W	0x44444444	De-Gamma Curve definition lower x increments (sampling points)
ISP_0400_GAMMA_DX_HI	0x0020	W	0x44444444	De-Gamma Curve definition higher x increments (sampling points)
ISP_0400_GAMMA_R_Y_0	0x0024	W	0x00000000	De-Gamma Curve definition y red 0
ISP_0400_GAMMA_R_Y_1	0x0028	W	0x00000100	De-Gamma Curve definition y red 1
ISP_0400_GAMMA_R_Y_2	0x002c	W	0x00000200	De-Gamma Curve definition y red 2
ISP_0400_GAMMA_R_Y_3	0x0030	W	0x00000300	De-Gamma Curve definition y red 3
ISP_0400_GAMMA_R_Y_4	0x0034	W	0x00000400	De-Gamma Curve definition y red 4
ISP_0400_GAMMA_R_Y_5	0x0038	W	0x00000500	De-Gamma Curve definition y red 5
ISP_0400_GAMMA_R_Y_6	0x003c	W	0x00000600	De-Gamma Curve definition y red 6
ISP_0400_GAMMA_R_Y_7	0x0040	W	0x00000700	De-Gamma Curve definition y red 7
ISP_0400_GAMMA_R_Y_8	0x0044	W	0x00000800	De-Gamma Curve definition y red 8
ISP_0400_GAMMA_R_Y_9	0x0048	W	0x00000900	De-Gamma Curve definition y red 9
ISP_0400_GAMMA_R_Y_10	0x004c	W	0x00000a00	De-Gamma Curve definition y red 10
ISP_0400_GAMMA_R_Y_11	0x0050	W	0x00000b00	De-Gamma Curve definition y red 11
ISP_0400_GAMMA_R_Y_12	0x0054	W	0x00000c00	De-Gamma Curve definition y red 12
ISP_0400_GAMMA_R_Y_13	0x0058	W	0x00000d00	De-Gamma Curve definition y red 13
ISP_0400_GAMMA_R_Y_14	0x005c	W	0x00000e00	De-Gamma Curve definition y red 14

ISP_0400_GAMMA_R_Y_15	0x0060	W	0x00000f00	De-Gamma Curve definition y red 15
ISP_0400_GAMMA_R_Y_16	0x0064	W	0x00000fff	De-Gamma Curve definition y red 16
ISP_0400_GAMMA_G_Y_0	0x0068	W	0x00000000	De-Gamma Curve definition y green 0
ISP_0400_GAMMA_G_Y_1	0x006c	W	0x00000100	De-Gamma Curve definition y green 1
ISP_0400_GAMMA_G_Y_2	0x0070	W	0x00000200	De-Gamma Curve definition y green 2
ISP_0400_GAMMA_G_Y_3	0x0074	W	0x00000300	De-Gamma Curve definition y green 3
ISP_0400_GAMMA_G_Y_4	0x0078	W	0x00000400	De-Gamma Curve definition y green 4
ISP_0400_GAMMA_G_Y_5	0x007c	W	0x00000500	De-Gamma Curve definition y green 5
ISP_0400_GAMMA_G_Y_6	0x0080	W	0x00000600	De-Gamma Curve definition y green 6
ISP_0400_GAMMA_G_Y_7	0x0084	W	0x00000700	De-Gamma Curve definition y green 7
ISP_0400_GAMMA_G_Y_8	0x0088	W	0x00000800	De-Gamma Curve definition y green 8
ISP_0400_GAMMA_G_Y_9	0x008c	W	0x00000900	De-Gamma Curve definition y green 9
ISP_0400_GAMMA_G_Y_10	0x0090	W	0x00000a00	De-Gamma Curve definition y green 10
ISP_0400_GAMMA_G_Y_11	0x0094	W	0x00000b00	ISP_GAMMA_G_Y_11
ISP_0400_GAMMA_G_Y_12	0x0098	W	0x00000c00	De-Gamma Curve definition y green 12
ISP_0400_GAMMA_G_Y_13	0x009c	W	0x00000d00	De-Gamma Curve definition y green 13
ISP_0400_GAMMA_G_Y_14	0x00a0	W	0x00000e00	De-Gamma Curve definition y green 14
ISP_0400_GAMMA_G_Y_15	0x00a4	W	0x00000f00	De-Gamma Curve definition y green 15
ISP_0400_GAMMA_G_Y_16	0x00a8	W	0x00000fff	De-Gamma Curve definition y green 16
ISP_0400_GAMMA_B_Y_0	0x00ac	W	0x00000000	De-Gamma Curve definition y blue 0
ISP_0400_GAMMA_B_Y_1	0x00b0	W	0x00000100	De-Gamma Curve definition y blue 1
ISP_0400_GAMMA_B_Y_2	0x00b4	W	0x00000200	De-Gamma Curve definition y blue 2

ISP_0400_GAMMA_B_Y_3	0x00b8	W	0x00000300	De-Gamma Curve definition y blue 3
ISP_0400_GAMMA_B_Y_4	0x00bc	W	0x00000400	De-Gamma Curve definition y blue 4
ISP_0400_GAMMA_B_Y_5	0x00c0	W	0x00000500	De-Gamma Curve definition y blue 5
ISP_0400_GAMMA_B_Y_6	0x00c4	W	0x00000600	De-Gamma Curve definition y blue 6
ISP_0400_GAMMA_B_Y_7	0x00c8	W	0x00000700	De-Gamma Curve definition y blue 7
ISP_0400_GAMMA_B_Y_8	0x00cc	W	0x00000800	De-Gamma Curve definition y blue 8
ISP_0400_GAMMA_B_Y_9	0x00d0	W	0x00000900	De-Gamma Curve definition y blue 9
ISP_0400_GAMMA_B_Y_10	0x00d4	W	0x00000a00	De-Gamma Curve definition y blue 10
ISP_0400_GAMMA_B_Y_11	0x00d8	W	0x00000b00	De-Gamma Curve definition y blue 11
ISP_0400_GAMMA_B_Y_12	0x00dc	W	0x00000c00	De-Gamma Curve definition y blue 12
ISP_0400_GAMMA_B_Y_13	0x00e0	W	0x00000d00	De-Gamma Curve definition y blue 13
ISP_0400_GAMMA_B_Y_14	0x00e4	W	0x00000e00	De-Gamma Curve definition y blue 14
ISP_0400_GAMMA_B_Y_15	0x00e8	W	0x00000f00	De-Gamma Curve definition y blue 15
ISP_0400_GAMMA_B_Y_16	0x00ec	W	0x00000fff	De-Gamma Curve definition y blue 16
ISP_0400_AWB_GAIN0_G	0x0138	W	0x01000100	Auto white balance gain green for normal channel and short-expose frame
ISP_0400_AWB_GAIN0_RB	0x013c	W	0x01000100	Auto white balance gain red and blue for normal channel and short-expose frame
ISP_0400_AWB_GAIN1_G	0x0140	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB_GAIN1_RB	0x0144	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB_GAIN2_G	0x0148	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx3)
ISP_0400_AWB_GAIN2_RB	0x014c	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx3)

ISP_0400_CC_COEFF_0	0x0170	W	0x00000021	Color conversion coefficient 0
ISP_0400_CC_COEFF_1	0x0174	W	0x00000040	Color conversion coefficient 1
ISP_0400_CC_COEFF_2	0x0178	W	0x0000000d	Color conversion coefficient 2
ISP_0400_CC_COEFF_3	0x017c	W	0x000001ed	Color conversion coefficient 3
ISP_0400_CC_COEFF_4	0x0180	W	0x000001db	Color conversion coefficient 4
ISP_0400_CC_COEFF_5	0x0184	W	0x00000038	Color conversion coefficient 5
ISP_0400_CC_COEFF_6	0x0188	W	0x00000038	Color conversion coefficient 6
ISP_0400_CC_COEFF_7	0x018c	W	0x000001d1	Color conversion coefficient 7
ISP_0400_CC_COEFF_8	0x0190	W	0x000001f7	Color conversion coefficient 8
ISP_0400_OUT_H_OFFS	0x0194	W	0x00000000	Horizontal offset of output window
ISP_0400_OUT_V_OFFS	0x0198	W	0x00000000	Vertical offset of output window
ISP_0400_OUT_H_SIZE	0x019c	W	0x00001000	Output horizontal picture size
ISP_0400_OUT_V_SIZE	0x01a0	W	0x00000c00	Output vertical picture size
ISP_0400_FLAGS_SHD	0x01a8	W	0x00000000	Flags (current status) of certain signals and Shadow regs for enable signals
ISP_0400_OUT_H_OFFS_SHD	0x01ac	W	0x00000000	Current horizontal offset of output window (shadow register)
ISP_0400_OUT_V_OFFS_SHD	0x01b0	W	0x00000000	Current vertical offset of output window (shadow register)
ISP_0400_OUT_H_SIZE_SHD	0x01b4	W	0x00000000	Current output horizontal picture size (shadow register)
ISP_0400_OUT_V_SIZE_SHD	0x01b8	W	0x00000000	Current output vertical picture size (shadow register)
ISP_0400_ISP_IMSC	0x01bc	W	0x00000000	Interrupt mask
ISP_0400_ISP_RIS	0x01c0	W	0x00000000	Raw interrupt status
ISP_0400_ISP_MIS	0x01c4	W	0x00000000	Masked interrupt status
ISP_0400_ISP_ICR	0x01c8	W	0x00000000	Interrupt clear register, high clear
ISP_0400_ISP_ISR	0x01cc	W	0x00000000	Interrupt set register, high set
ISP_0400_ISP3A_IMSC	0x01d0	W	0x00000000	Interrupt mask
ISP_0400_ISP3A_RIS	0x01d4	W	0x00000000	Raw interrupt status
ISP_0400_ISP3A_MIS	0x01d8	W	0x00000000	Masked interrupt status
ISP_0400_ISP3A_ICR	0x01dc	W	0x00000000	Interrupt clear register
ISP_0400_ERR	0x023c	W	0x00000000	ISP error register
ISP_0400_ERR_CLR	0x0240	W	0x00000000	ISP error clear register
ISP_0400_FRAME_COUNT	0x0244	W	0x00000000	Frame counter
ISP_0400_DEBUG1	0x0248	W	0x00000000	RKISP_DEBUG1
ISP_0400_DEBUG2	0x024c	W	0x00000000	RKISP_DEBUG2
ISP_0400_DEBUG3	0x0250	W	0x00000000	RKISP_DEBUG3

12.4.1.18 SHUTTER

Name	Offset	Size	Reset Value	Description
ISP_SHUTTER_0680_CTRL	0x0000	W	0x00000000	Mechanical shutter control
ISP_SHUTTER_0680_PREDIV	0x0004	W	0x00000000	Mech. Shutter Counter Pre-Divider
ISP_SHUTTER_0680_DELAY	0x0008	W	0x00000000	Delay register
ISP_SHUTTER_0680_TIME	0x000c	W	0x00000000	Time register

12.4.1.19 CTRL

Name	Offset	Size	Reset Value	Description
CTRL_0000_VI_ISP_EN	0x0000	W	0x00000000	Isp_top_en ctrl
CTRL_0000_VI_ISP_PATH	0x0004	W	0x00000000	Register0000 Description
CTRL_0000_VI_ID	0x0008	W	0x02001909	Revision identification register
CTRL_0000_VI_ISP_CLK_CTRL	0x000c	W	0x00000000	Internal clock control register
CTRL_0000_VI_ICCL	0x0010	W	0x00000f7b	Internal clock control register
CTRL_0000_VI_IRCL	0x0014	W	0x00000000	Internal reset control register
CTRL_0000_VI_DPCL	0x0018	W	0x00000000	Data path control register
CTRL_0000_SWS_CFG	0x001c	W	0x00000000	Sws config
CTRL_0000_LVDS_CTRL	0x0020	W	0x00000000	LVDS control
CTRL_0000_LVDS_SAV_EAV_ACT	0x0024	W	0x00000000	SAV/EAV of act
CTRL_0000_LVDS_SAV_EAV_BLK	0x0028	W	0x00000000	SAV/EAV of blk

12.4.1.20 LDCH

Name	Offset	Size	Reset Value	Description
ISP_LDCH_3B00_STS	0x0000	W	0x00000001	LDCH state register

12.4.1.21 RAWAF

Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_CTRL	0x0000	W	0x00000006	This is the control register for RAWAF measurement unit
ISP_RAWAF_4D00_OFFSET_WINA	0x0004	W	0x00000000	Top Left corner of measure window A
ISP_RAWAF_4D00_SIZE_WINA	0x0008	W	0x00000000	Size of measure window A
ISP_RAWAF_4D00_OFFSET_WINB	0x000C	W	0x00000000	Top Left corner of measure window B

Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_SIZE_WINB	0x0010	W	0x00000000	Size of measure window B
ISP_RAWAF_4D00_INT_LINE	0x0014	W	0x000FC963	Line of window 15x15 that need to produce int signle
ISP_RAWAF_4D00_GAUS_COE	0x0018	W	0x00081020	3x3 gaus filter coe
ISP_RAWAF_4D00_THRES	0x001C	W	0x00000000	Threshold and ram_star_addr register
ISP_RAWAF_4D00_VAR_SHIFT	0x0020	W	0x00000000	Variable shift register
ISP_RAWAF_4D00_SUM_A	0x0024	W	0x00000000	Sharpness Value Status Register of Window A
ISP_RAWAF_4D00_SUM_B	0x0028	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_LUM_A	0x002C	W	0x00000000	Luminance Value Status Register of Window A
ISP_RAWAF_4D00_LUM_B	0x0030	W	0x00000000	Luminance Value Status Register of Window B
ISP_RAWAF_4D00_GAMMA_Y0	0x0034	W	0x000B0000	Include y0 and y1 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y1	0x0038	W	0x002C001B	Include y2 and y3 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y2	0x003C	W	0x0056003D	Include y4 and y5 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y3	0x0040	W	0x00720066	Include y6 and y7 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y4	0x0044	W	0x008D007D	Include y8 and y9 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y5	0x0048	W	0x00A9009B	Include y10 and y11 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y6	0x004C	W	0x00D000BD	Include y12 and y13 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y7	0x0050	W	0x00F000E0	Include y14 and y15 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y8	0x0054	W	0x000000FF	Include y16 value of gamma table
ISP_RAWAF_4D00_INT_STATE	0x0058	W	0x00000000	Int state of five line interrupt
ISP_RAWAF_4D00_RAM_DATA	0x005C	W	0x00000000	Read 15x15 sum data in ram should choose this addr, then data will be read out by ahb bus.

12.4.1.22 RAWAE

(1)RAWAE_BIG

Name	Offset	Size	Reset Value	Description
RAWAE_BIG_4400_4600_4700_CTRL	0x0000	W	0x00000000	Exposure control
RAWAE_BIG_4400_4600_4700_WND0_BLK_SIZE	0x0004	W	0x00000000	Size of one block for window0
RAWAE_BIG_4400_4600_4700_WND0_OFFSET	0x0008	W	0x00000000	Offset of one block for window0

Name	Offset	Size	Reset Value	Description
RAWAE_BIG_4400_4600_4700_RAM_CTRL	0x000C	W	0x00000000	RAM address offset
RAWAE_BIG_4400_4600_4700_WND1_SIZE	0x0010	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND1_OFFSET	0x0014	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND2_SIZE	0x0018	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND2_OFFSET	0x001C	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND3_SIZE	0x0020	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND3_OFFSET	0x0024	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND4_SIZE	0x0028	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4600_4700_WND4_OFFSET	0x002C	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMR	0x0030	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMR	0x0034	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMR	0x0038	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND4_SUMR	0x003C	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMG	0x0040	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMG	0x0044	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMG	0x0048	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND4_SUMG	0x004C	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND1_SUMB	0x0050	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND2_SUMB	0x0054	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND3_SUMB	0x0058	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_WND4_SUMB	0x005C	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4600_4700_RO_DBG1	0x0060	W	0x00000000	Just for debug
RAWAE_BIG_4400_4600_4700_RO_DBG2	0x0064	W	0x00000000	Just for debug
RAWAE_BIG_4400_4600_4700_RO_DBG3	0x0068	W	0x00000000	Just for debug
RAWAE_BIG_4400_4600_4700_RO_MEAN_BASE_ADDR	0x0080	W	0x00000000	Mean luminance value of block 00 ~ee (total 225) Read data from RAM, support burst16

(2) RAWAE_LITE

Name	Offset	Size	Reset Value	Description
ISP_RAWAE_LITE_4500_CTRL	0x0000	W	0x00000000	Exposure control
ISP_RAWAE_LITE_4500_BLK_SIZE	0x0004	W	0x00000000	Horizontal size of one block
ISP_RAWAE_LITE_4500_OFFSET	0x0008	W	0x00000000	Horizontal offset for first block
ISP_RAWAE_LITE_4500_RO_MEAN_XX	0x0010	W	0x00000000	Reg name from EXP_MEAN_00 EXP_MEAN_24
ISP_RAWAE_LITE_4500_RO_DBG1	0x0074	W	0x00000000	Just for debug
ISP_RAWAE_LITE_4500_RO_DBG2	0x0078	W	0x00000000	Just for debug

12.4.1.23 RAWAWB

Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_CTRL	0x0000	W	0x00000000	Rawawb global control register
ISP_RAWAWB_5000_SUM_BGAIN_BIG_3	0x0000	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_3	0x0003	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_BLK_CTRL	0x0004	W	0x00000000	Rawawb block control
ISP_RAWAWB_5000_WIN_OFFS	0x0008	W	0x00000000	Awb vertical and horizontal offset of measure window
ISP_RAWAWB_5000_WIN_SIZE	0x000c	W	0x00000000	Awb vertical and horizontal window size
ISP_RAWAWB_5000_LIMIT_RG_MAX	0x0010	W	0x00000000	Max red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MAX	0x0014	W	0x00000000	Max bule and luminance value in white point detection
ISP_RAWAWB_5000_LIMIT_RG_MIN	0x0018	W	0x00000000	Min red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MIN	0x001c	W	0x00000000	Min bule and luminance value in white point detection
ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL	0x0020	W	0x00000000	Weight curve ctrol
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03	0x0024	W	0x60402000	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47	0x0028	W	0xe0c0a080	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8	0x002c	W	0x000000ff	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03	0x0030	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47	0x0034	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8	0x0038	W	0x01000020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_PRE_WBGAIN_INV	0x003c	W	0x01000100	The pre wbgain operation
ISP_RAWAWB_5000_UV_DETC_VERTEX0_0	0x0040	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_0	0x0044	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_0	0x0048	W	0x00000000	UV detect, vertex 0

ISP_RAWAWB_5000_UV_DETC_VERTEX3_0	0x004c	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_0	0x0050	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_0	0x0054	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_0	0x0058	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_0	0x005c	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_1	0x0060	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_1	0x0064	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_1	0x0068	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_1	0x006c	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_1	0x0070	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_1	0x0074	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_1	0x0078	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_1	0x007c	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_2	0x0080	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_2	0x0084	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_2	0x0088	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_2	0x008c	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_2	0x0090	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_2	0x0094	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_2	0x0098	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2	0x009c	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_3	0x00a0	W	0x00000000	UV detect, vertex 0

ISP_RAWAWB_5000_UV_DETC_VERTEX1_3	0x00a4	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_3	0x00a8	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_3	0x00ac	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3	0x00b0	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3	0x00b4	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3	0x00b8	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3	0x00bc	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_4	0x00c0	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_4	0x00c4	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_4	0x00c8	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_4	0x00cc	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_4	0x00d0	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_4	0x00d4	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_4	0x00d8	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_4	0x00dc	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_5	0x00e0	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_5	0x00e4	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_5	0x00e8	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_5	0x00ec	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_5	0x00f0	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE10_5	0x00f4	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_5	0x00f8	W	0x00000000	UV detect, slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_5	0x00fc	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_VERTEX0_6	0x0100	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX1_6	0x0104	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX2_6	0x0108	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_VERTEX3_6	0x010c	W	0x00000000	UV detect, vertex 0
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_6	0x0110	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE10_6	0x0114	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_6	0x0118	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_6	0x011c	W	0x00000000	UV detect, slope inv
ISP_RAWAWB_5000_YUV_RGB2ROTY_0	0x0120	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTY_1	0x0124	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTU_0	0x0128	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTU_1	0x012c	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTV_0	0x0130	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_RGB2ROTV_1	0x0134	W	0x00000000	RGB2ROTYUV coefficient mat
ISP_RAWAWB_5000_YUV_X_COOR_Y_0	0x0140	W	0x00000000	The Y coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X_COOR_U_0	0x0144	W	0x00000000	The U coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X_COOR_V_0	0x0148	W	0x00000000	The V coordinate of point1 and vector point21 for light 0
ISP_RAWAWB_5000_YUV_X1X2_DIS_0	0x014c	W	0x00000000	The distance between point1 and point2 for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_0	0x0150	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_0	0x0154	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_0	0x0158	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_0	0x015c	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 0
ISP_RAWAWB_5000_YUV_X_COOR_Y_1	0x0160	W	0x00000000	The Y coordinate of point1 and vector point21 for light 1
ISP_RAWAWB_5000_YUV_X_COOR_U_1	0x0164	W	0x00000000	The U coordinate of point1 and vector point21 for light 1
ISP_RAWAWB_5000_YUV_X_COOR_V_1	0x0168	W	0x00000000	The V coordinate of point1 and vector point21 for light 1
ISP_RAWAWB_5000_YUV_X1X2_DIS_1	0x016c	W	0x00000000	The distance between point1 and point2 for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_1	0x0170	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_1	0x0174	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_1	0x0178	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_1	0x017c	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 1
ISP_RAWAWB_5000_YUV_X_COOR_Y_2	0x0180	W	0x00000000	The Y coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X_COOR_U_2	0x0184	W	0x00000000	The U coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X_COOR_V_2	0x0188	W	0x00000000	The V coordinate of point1 and vector point21 for light 2
ISP_RAWAWB_5000_YUV_X1X2_DIS_2	0x018c	W	0x00000000	The distance between point1 and point2 for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_2	0x0190	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_2	0x0194	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_2	0x0198	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_2	0x019c	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 2
ISP_RAWAWB_5000_YUV_X_COOR_Y_3	0x01a0	W	0x00000000	The Y coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X_COOR_U_3	0x01a4	W	0x00000000	The U coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X_COOR_V_3	0x01a8	W	0x00000000	The V coordinate of point1 and vector point21 for light 3
ISP_RAWAWB_5000_YUV_X1X2_DIS_3	0x01ac	W	0x00000000	The distance between point1 and point2 for light 3

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_3	0x01b0	W	0x00000000	The 3DYUV U interpolation curve of X coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_3	0x01b4	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_3	0x01b8	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_3	0x01bc	W	0x00000000	The 3DYUV U interpolation curve of Y coordinate for light 3
ISP_RAWAWB_5000_RGB2XY_WT01	0x01fc	W	0x00000000	RGB2XY weight matrix, coeff 01
ISP_RAWAWB_5000_RGB2XY_WT2	0x0200	W	0x00000000	RGB2XY weight matrix, coeff 2
ISP_RAWAWB_5000_RGB2XY_MAT0_XY	0x0204	W	0x00000000	RGB2XY, rotation matrix, first column xy
ISP_RAWAWB_5000_RGB2XY_MAT1_XY	0x0208	W	0x00000000	RGB2XY, rotation matrix, second column xy
ISP_RAWAWB_5000_RGB2XY_MAT2_XY	0x020c	W	0x00000000	RGB2XY, rotation matrix, third column xy
ISP_RAWAWB_5000_XY_DETC_NOR_X_0	0x0210	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_0	0x0214	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_0	0x0218	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_0	0x021c	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_1	0x0228	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_1	0x022c	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_1	0x0230	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_1	0x0234	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_2	0x0240	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_2	0x0244	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_2	0x0248	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_2	0x024c	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_3	0x0258	W	0x00000000	XY detect, x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_3	0x025c	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_3	0x0260	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_3	0x0264	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_4	0x0270	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_4	0x0274	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_4	0x0278	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_4	0x027c	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_5	0x0288	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_5	0x028c	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_5	0x0290	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_5	0x0294	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_6	0x02a0	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_6	0x02a4	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_6	0x02a8	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_6	0x02ac	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL	0x02b8	W	0x00000000	The horizontal and vertical offset of multiwiondow
ISP_RAWAWB_5000_EXC_WP_REGION0_XU	0x02fc	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION0_YV	0x0300	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION1_XU	0x0304	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION1_YV	0x0308	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION2_XU	0x030c	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION2_YV	0x0310	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range

ISP_RAWAWB_5000_EXC_WP_REGION3_XU	0x0314	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION3_YV	0x0318	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION4_XU	0x031c	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION4_YV	0x0320	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION5_XU	0x0324	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION5_YV	0x0328	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION6_XU	0x032c	W	0x00000000	The left and right boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_EXC_WP_REGION6_YV	0x0330	W	0x00000000	The top and bottom boundary of exclude region in UV or xy range
ISP_RAWAWB_5000_SUM_RGAIN_NOR_0	0x0340	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_0	0x0348	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_NOR_0	0x034c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_0	0x0350	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_0	0x0358	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_0	0x035c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_1	0x0370	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_1	0x0378	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_NOR_1	0x037c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_1	0x0380	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_1	0x0388	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_1	0x038c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_2	0x03a0	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_2	0x03a8	W	0x00000000	White point Bgain sum with yweight and blkweight

ISP_RAWAWB_5000_WP_NUM_NOR_2	0x03ac	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_2	0x03b0	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_2	0x03b8	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_2	0x03bc	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_3	0x03d0	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_3	0x03d8	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_NOR_3	0x03dc	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_3	0x03ec	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_4	0x0400	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_4	0x0408	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_NOR_4	0x040c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_4	0x0410	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_4	0x0418	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_4	0x041c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_5	0x0430	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_5	0x0438	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_NOR_5	0x043c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_5	0x0440	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_5	0x0448	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_5	0x044c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_6	0x0460	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_6	0x0468	W	0x00000000	White point Bgain sum with yweight and blkweight

ISP_RAWAWB_5000_WP_NUM_NOR_6	0x046c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_6	0x0470	W	0x00000000	White point Rgain sum with yweight and blkweight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_6	0x0478	W	0x00000000	White point Bgain sum with yweight and blkweight
ISP_RAWAWB_5000_WP_NUM_BIG_6	0x047c	W	0x00000000	White point Num sum with yweight and blkweight
ISP_RAWAWB_5000_Y_HIST01	0x0620	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST23	0x0624	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST45	0x0628	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST67	0x062c	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_RAM_CTRL	0x0650	W	0x00000000	Control of reading ram
ISP_RAWAWB_5000_WRAM_CTRL	0x0654	W	0x00000000	Control of BLK weight ram
ISP_RAWAWB_5000_WRAM_DATA_BASE	0x0660	W	0x00000000	The Weight of BLK system. The user will always config this base address 45 times for 15x15 weights.
ISP_RAWAWB_5000_RAM_DATA_BASE	0x0700	W	0x00000000	Data read from ram

12.4.1.24 RAWHIST

(1)RAWHIST_BIG

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_BIG_4800_4A00_4B00_CTRL	0x0000	W	0x20000000	Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window.
ISP_RAWHIST_BIG_4800_4A00_4B00_SIZE	0x0004	W	0x00000000	Note: hist_h_offset + hist_h_size * n should be less than input window width.
ISP_RAWHIST_BIG_4800_4A00_4B00_OFFS	0x0008	W	0x00000000	Note: Histogram measurement is done in nxn sub-windows like the exposure measurement, if histogram.
ISP_RAWHIST_BIG_4800_4A00_4B00_HRAM_CTRL	0x000C	W	0x00000000	HRAM address offset

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_BIG_4800_4A00_4B00_RAW2Y_CC	0x0010	W	0x000D2021	The offset of RAW2Y formula
ISP_RAWHIST_BIG_4800_4A00_4B00_WRAM_CTRL	0x0014	W	0x00000000	RAM offset for write or read
ISP_RAWHIST_BIG_4800_4A00_4B00_DBG1	0x0020	W	0x00000000	Just hist debug reg
ISP_RAWHIST_BIG_4800_4A00_4B00_DBG2	0x0024	W	0x00000000	Just hist debug reg
ISP_RAWHIST_BIG_4800_4A00_4B00_DBG3	0x0028	W	0x00000000	Just hist debug reg
ISP_RAWHIST_BIG_4800_4A00_4B00_WEIGHT_BASE	0x0040	W	0x00820820	Note: Allowed value range for weight factor is 0 to 32. The resulting weight is register_value/32. The host software has to limit the register value for each factor to 32.
ISP_RAWHIST_BIG_4800_4A00_4B00_RO_BASE_BIN	0x0080	W	0x00000000	Histogram measurement result bin 0~255 (total 256)

(2) RAWHIST_LIST

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_LITE_4900_CTRL	0x0000	W	0x00000000	Histogram properties
ISP_RAWHIST_LITE_4900_SIZE	0x0004	W	0x00000000	Horizontal (sub-)window size Note: hist_h_offset + hist_h_size x n should be less than input window width.
ISP_RAWHIST_LITE_4900_OFFS	0x0008	W	0x00000000	Histogram window horizontal offset for first window of nxnNote: Histogram measurement is done in nxn sub-windows like the exposure measurement, if histogram.
ISP_RAWHIST_LITE_4900_RAM_CTRL	0x000C	W	0x00000000	RAM address offset
ISP_RAWHIST_LITE_4900_RAW2Y_CC	0x0010	W	0x000D2021	The offset of RAW2Y formula
ISP_RAWHIST_LITE_4900_DBG1	0x0020	W	0x00000000	Just hist debug reg
ISP_RAWHIST_LITE_4900_DBG2	0x0024	W	0x00000000	Just hist debug reg
ISP_RAWHIST_LITE_4900_DBG3	0x0028	W	0x00000000	Just hist debug reg
ISP_RAWHIST_LITE_4900_WEIGHT_0	0x0040	W	0x20202020	Weighting factor for sub-windows total 25 factorNote: Allowed value range for weight factor is 0 to 32. The resulting weight is register_value/32. The host software has to limit the register value for each factor to 32.

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_LITE_4900_RO_BASE_BIN	0x0080	W	0x00000000	Histogram measurement result bin 0~255 (total 256)

12.4.1.25 YNR

Name	Offset	Size	Reset Value	Description
YNR_2700_GLOBAL_CTRL	0x0000	W	0x00801000	Control register
YNR_2700_RNR_MAX_R	0x0004	W	0x00003754	Control register
YNR_2700_LOWNR_CTRL_0	0x0010	W	0x01000100	Control register
YNR_2700_LOWNR_CTRL_1	0x0014	W	0x00000080	Control register
YNR_2700_LOWNR_CTRL_2	0x0018	W	0x00100007	Control register
YNR_2700_LOWNR_CTRL_3	0x001c	W	0x40640133	Control register
YNR_2700_HIGHNR_CTRL_0	0x0020	W	0x003a0080	Control register
YNR_2700_HIGHNR_CTRL_1	0x0024	W	0x006e0064	Control register
YNR_2700_HIGHNR_BASE_FILTER_WEIGHT	0x0028	W	0x00080f12	Base filter weight. The more strength of high frequency reduing noise when three signals closer.
YNR_2700_GAUSS1_COEFF	0x0030	W	0x0054200b	Gauss coeff for BFT3X3
YNR_2700_GAUSS2_COEFF	0x0034	W	0x00402010	Gauss coeff for LGFT3X3
YNR_2700_DIRECTION_W_0_3	0x0038	W	0x08080808	The bigger of signal, the more strength of reduing noise of this direction.
YNR_2700_DIRECTION_W_4_7	0x003c	W	0x04040404	Control register
YNR_2700_SGM_DX_0_1	0x0040	W	0x00400000	X increments of noise intensity cuvre
YNR_2700_SGM_DX_2_3	0x0044	W	0x00c00080	X increments of noise intensity cuvre
YNR_2700_SGM_DX_4_5	0x0048	W	0x01400100	X increments of noise intensity cuvre
YNR_2700_SGM_DX_6_7	0x004c	W	0x01c00180	X increments of noise intensity cuvre
YNR_2700_SGM_DX_8_9	0x0050	W	0x02400200	X increments of noise intensity cuvre
YNR_2700_SGM_DX_10_11	0x0055	W	0x02c00280	X increments of noise intensity cuvre
YNR_2700_SGM_DX_12_13	0x0058	W	0x03400300	X increments of noise intensity cuvre
YNR_2700_SGM_DX_14_15	0x005c	W	0x03c00380	X increments of noise intensity cuvre

YNR_2700_SGM_DX_16	0x0060	W	0x00000400	X increments of noise intensity cuvre
YNR_2700_LSGM_Y_0_1	0x0070	W	0x00a0004c	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_2_3	0x0074	W	0x00e400d0	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_4_5	0x0078	W	0x00e400e8	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_6_7	0x007c	W	0x00cc00d8	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_8_9	0x0080	W	0x00c000c4	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_10_11	0x0084	W	0x00b800bc	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_12_13	0x0088	W	0x00a400b4	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_14_15	0x008c	W	0x00540088	Noise intensity of low frequency coefficient
YNR_2700_LSGM_Y_16	0x0090	W	0x00000028	Noise intensity of low frequency coefficient
YNR_2700_HSGM_Y_0_1	0x00a0	W	0x00a0004c	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_2_3	0x00a4	W	0x00e400d0	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_4_5	0x00a8	W	0x00e400e8	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_6_7	0x00ac	W	0x00cc00d8	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_8_9	0x00b0	W	0x00c000c4	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_10_11	0x00b4	W	0x00b800bc	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_12_13	0x00b8	W	0x00a400b4	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_14_15	0x00bc	W	0x00540088	Noise intensity of high frequency coefficient
YNR_2700_HSGM_Y_16	0x00c0	W	0x00000028	Noise intensity of high frequency coefficient
YNR_2700_RNR_STRENGTH03	0x00d0	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH47	0x00d4	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH8b	0x00d8	W	0x10101010	RNR strength adjust curve

YNR_2700_RNR_STRENGTHcf	0x00dc	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH16	0x00e0	W	0x00000010	RNR strength adjust curve

12.4.1.26 CNR

Name	Offset	Size	Reset Value	Description
ISP_CNR_2800_CTRL	0x0000	W	0x00000002	Global ctrl
ISP_CNR_2800_EXGAIN	0x0004	W	0x00000080	external gain value
ISP_CNR_2800_GAIN_PARA	0x0008	W	0x00160c3c	gain cal parameter
ISP_CNR_2800_GAIN_UV_PARA	0x000c	W	0x00004030	uv gain cal paramter
ISP_CNR_2800_LMED3	0x0010	W	0x00000003	low frequence med 3x3
ISP_CNR_2800_LBF5_GAIN	0x0014	W	0x00000102	gain parameter of low frequence bialteral filter 5x5
ISP_CNR_2800_LBF5_WEITD0_3	0x0018	W	0x4d637080	lbf5x5 filter spatial weight 0 to 3
ISP_CNR_2800_LBF5_WEITD4	0x001c	W	0x0000002f	lbf5x5 filter spatial weight4
ISP_CNR_2800_HMED3	0x0020	W	0x00000003	high frequence med 3x3
ISP_CNR_2800_HBF5	0x0024	W	0x0f000438	High frequence bialteral filter parameter
ISP_CNR_2800_LBF3	0x0028	W	0x00800438	Low frequence bialteral filter3x3 parameter

12.4.1.27 Sharp

Name	Offset	Size	Reset Value	Description
SHARP_EN	0x0000	W	0x00000000	SHARP ENABLE
SHARP_RATIO	0x0004	W	0x28800033	SHARP RATIO
SHARP_□LUMA_DX	0x0008	W	0x07887766	SHARP ENABLE
SHARP_PBF_SIGMA_INV_0	0x000C	W	0x09430515	SHARP PBF SIGMA INVERSE
SHARP_PBF_SIGMA_INV_1	0x0010	W	0x07819494	SHARP PBF SIGMA INVERSE
SHARP_PBF_SIGMA_INV_2	0x0014	W	0x00025094	SHARP PBF SIGMA INVERSE
SHARP_BF_SIGMA_INV_0	0x0018	W	0x0F14EDC7	SHARP BF SIGMA INVERSE
SHARP_BF_SIGMA_INV_1	0x001C	W	0x0C3290F1	SHARP BF SIGMA INVERSE
SHARP_BF_SIGMA_INV_2	0x0020	W	0x0003C4F1	SHARP BF SIGMA INVERSE
SHARP_SIGMA_SHIFT	0x0024	W	0x00000076	SHARP PBF/BF SIGMA INVERSE SHIFT BITS
SHARP_EHF_TH_0	0x0028	W	0x08020080	SHARP EHF TH
SHARP_EHF_TH_1	0x002C	W	0x08020080	SHARP EHF TH
SHARP_EHF_TH_2	0x0030	W	0x00000440	SHARP EHF TH
SHARP_CLIP_HF_0	0x0034	W	0x08816040	SHARP CLIP HF
SHARP_CLIP_HF_1	0x0038	W	0x0E03E0B4	SHARP CLIP HF

Name	Offset	Size	Reset Value	Description
SHARP_CLIP_HF_2	0x003C	W	0x00000048	SHARP CLIP HF
SHARP_PBF_COEF	0x0040	W	0x000A1018	SHARP PBF COEF
SHARP_BF_COEF	0x0044	W	0x000A1018	SHARP BF COEF
SHARP_GAUS_COEF_0	0x0048	W	0x0006070C	SHARP RF COEF

12.4.2 Detail Register Description

12.4.2.1 MIPI

CSI2RX_1C00_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:12	RW	0x0	sw_dma_2frm_mode raw read back two/three frames mode, only the last frame valid 2'b00: Normal one frame mode 2'b01: Two frame mode 2'b10: Three frame mode 2'b11: Reserved
11:8	RW	0x0	sw_ibuf_op_mode 4'b0000: Normal_mode. All tx available, rx unavailable. 4'b0011: User mode. All tx and rx available. If do not configure any rx, user mode is equal to normal mode. 4'b0100: raw_rdback_frame1(start use sw_dma_rdback_p) 4'b0101: hdr_rdback_frame2 (start use sw_dma_rdback_p) 4'b0110: hdr_rdback_frame3 (start use sw_dma_rdback_p) 4'b0111: Reserved 4'b1000: hdr_framex2_ddr_mode 4'b1001: hdr_linex2_ddr_mode 4'b1010: hdr_linex2_noddr_mode 4'b1100: hdr_framex3_ddr_mode 4'b1101: hdr_linex3_ddr_mode
7	RW	0x0	sw_csi_ro_phyio_en force phyio to debug
6	RW	0x0	sw_csi_dbg_bypass csi bypass. Active high
5:4	RW	0x0	sw_csi_2ecc_bypass csi 2ecc bypass
3:2	RW	0x0	sw_hdr_esp_mode hdr especial mode 2'b00: Normal virtual channel mode 2'b01: Line counter mode of especial hdr (AR0239) 2'b10: Identification code mode of especial hdr (IMX327) 2'b11: Reserved
1	RW	0x0	sw_csi_pix_mode mipi word to pixel mode: 1'b0: one pixel 1'b1: two pixel
0	RW	0x0	sw_csi2rx_en_p csi rx read enable under hdr debug mode, auto-clear Note: CTRL0[0] read back is mipi readback working

CSI2RX_1C00_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	mipi_dphy_working mipi dhpy working state
30	RO	0x0	ro_csi2rx_enable mipi mode enable (~sw_dvp_mode)
29:28	RW	0x0	sw_ibuf_lvl1_sel2 ibuf2_m sel 2'b00: ibuf2_m_i 2'b01: ibuf1_l_i 2'b10: ibuf0_s_i
27:26	RW	0x0	sw_ibuf_lvl1_sel1 ibuf1_l sel 2'b00: ibuf1_l_i 2'b01: ibuf0_s_i 2'b10: ibuf2_m_i
25:24	RW	0x0	sw_ibuf_lvl1_sel0 ibuf0_s sel 2'b00: ibuf0_s_i 2'b01: ibuf1_l_i 2'b10: ibuf2_m_i
23	RW	0x0	sw_ibuf_lvl0_sel3 ibuf3_r_i sel : 1'b0: csi0_mipi[chan3_sel]; 1'b1: raw2_mipi(from ddr)
22	RW	0x0	sw_ibuf_lvl0_sel2 ibuf2_l_i sel : 1'b0: csi0_mipi[chan2_sel]; 1'b1: raw1_mipi(from ddr)
21	RW	0x0	sw_ibuf_lvl0_sel1 ibuf1_l_i sel : 1'b0: csi0_mipi[chan1_sel]; 1'b1: raw0_mipi(from ddr)
20	RW	0x0	sw_ibuf_lvl0_sel0 ibuf0_s_i sel : 1'b0: csi0_mipi[chan0_sel] 1'b1: csi1_mipi[chan0_sel]
19	RO	0x0	reserved
18:16	RW	0x3	sw_csi_chan3_sel csi0_mipi[7:0] chan3 sel
15	RO	0x0	reserved
14:12	RW	0x2	sw_csi_chan2_sel csi0_mipi[7:0] chan2 sel
11	RO	0x0	reserved
10:8	RW	0x1	sw_csi_chan1_sel csi0_mipi[7:0] chan1 sel
7	RO	0x0	reserved

6:4	RW	0x0	sw_csi_chan0_sel csi0_mipi[7:0] + csi1_mipi[7:0] chan0 sel
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_csi_lane Number of active data lanes 2'b00: 1 data lane (lane 0) 2'b01: 2 data lanes (lanes 0 and 1) 2'b10: 3 data lanes (lanes 0, 1, and 2) 2'b11: 4 data lanes (All) Can only be updated when the D-PHY lane is in Stop state. Note:Value after Reset: CSI2_HOST_NUMBER_OF_LANES-1 = 0x3

CSI2RX_1C00_CTRL2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_ibuf_hblank_count mipi in buffer hblank counter
23:20	RW	0x0	sw_rdbak_hold_diff raw readback hold diff value for pipeline full
19:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_isp_linecnt isp linecnt reach interrupt for ro_err3[15]

CSI2RX_1C00_CSI2_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	R/WSC	0x1	sw_csi_fifo_clr_n fifo clear. Active Low. auto-clr Write then clear
0	R/WSC	0x1	sw_csi_rxbyte_rst_n reset output. Active Low. auto-clr Write then clear

CSI2RX_1C00_PHY_STATE_RO

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	ro_phy_state phy state READ ONLY [11] : phy_ulpsactivenotclk [10] : phy_stopstateclk [9] : phy_rxulpsclknot [8] : phy_rxclkactivehs [7:4] : phy_stopstate [3:0] : phy_rxulpsesc

CSI2RX_1C00_DATA_IDS_1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_csi_id3 Data ID 3 dt3_vc[1:0],dt3_dt[5:0] channel 3
23:16	RW	0x00	sw_csi_id2 Data ID 2 dt2_vc[1:0],dt2_dt[5:0] channel 2
15:8	RW	0x00	sw_csi_id1 Data ID 1 dt1_vc[1:0],dt1_dt[5:0] channel 1
7:0	RW	0x2b	sw_csi_id0 Data ID 0 dt0_vc[1:0],dt0_dt[5:0] channel 0

CSI2RX_1C00_DATA_IDS_2

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_csi_id7 Data ID 7 dt7_vc[1:0],dt7_dt[5:0] cahnnel 7
23:16	RW	0x00	sw_csi_id6 Data ID 6 dt6_vc[1:0],dt6_dt[5:0] cahnnel 6
15:8	RW	0x00	sw_csi_id5 Data ID 5 dt5_vc[1:0],dt5_dt[5:0] channel 5
7:0	RW	0x00	sw_csi_id4 Data ID 4 dt5_vc[1:0],dt5_dt[5:0] channel 4

CSI2RX_1C00_ERR_PHY

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RC	0x0	phy_errcontrol phy control err
19:16	RO	0x0	reserved
15:12	RC	0x0	phy_erresc phy esc err
11:8	RC	0x0	phy_erreotsynchs phy eotsynchs err
7:4	RC	0x0	phy_errsotsynchs phy sotsynchs err
3:0	RC	0x0	phy_errsoths phy soths err

CSI2RX_1C00_ERR_PACKET

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RC	0x0	checksum_error CRC checksum error
23:21	RO	0x0	reserved
20	RC	0x0	ecc_2bit_error ecc 2bit error
19:16	RC	0x0	ecc_1bit_error ecc 1bit error
15:12	RC	0x0	err_id id err
11:8	RC	0x0	err_frame_data The frame whose fransfer is being finished had at last one CRC err detected
7:4	RC	0x0	err_f_seq The Frame Number of two consecutive packets does not follow the expcted order
3:0	RC	0x0	err_f_bndry_match Error in correspondence between Frame Starts and Frame Edns. Could be caused by: - Two consecutive Frame Starts receive for the signaled Virtual Channel, with no Frame End between them. - Two consecutive Frame Ends receive for the signaled Virtual Channel, with no Frame Start between them. - The Frame Number of a Frame End does not match the one of the Frame Start before it, for the signaled Virtual Channel

CSI2RX_1C00_ERR_OVERFLOW

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RC	0x0	y_stat_afifox3_overflow raw0~2 to y statistic afifo overflow [0] raw0 afifo overflow [1] raw1 afifo overflow [2] raw2 afifo overflow
19	RC	0x0	ibuf3r_overflow ibuf_r_fifo overflow
18:16	RC	0x0	ibufx3_overflow ibufx3 overflow [0] : ibuf_s_fifo overflow [1] : ibuf_l_fifo overflow [2] : ibuf_m_fifo overflow
15	RO	0x0	reserved
14	RC	0x0	afifo22_overflow afifo22 overflow
13	RC	0x0	afifo21_overflow afifo21 overflow
12	RC	0x0	afifo20_overflow afifo20 woverflow
11	RC	0x0	lafifo13_overflow lafifo13 overflow
10	RC	0x0	lafifo12_overflow lafifo12 overflow
9	RC	0x0	lafifo11_overflow lafifo11 overflow
8	RC	0x0	lafifo10_overflow lafifo10 overflow
7	RC	0x0	afifo13_overflow afifo13 overflow
6	RC	0x0	afifo12_overflow afifo12 overflow
5	RC	0x0	afifo11_overflow afifo11 overflow
4	RC	0x0	afifo10_overflow afifo10 overflow
3:1	RO	0x0	reserved
0	RC	0x0	afifo0_overflow afifo0 overfolw

CSI2RX_1C00_ERR_STAT

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31	RW	0x0	mipi_drop_frm mipi drop frame state
30:28	RC	0x0	y_stat_end y stat end [raw2_y_stat_end, raw1_y_stat_end, raw0_y_stat_end] Note: y_stat_end point depends on sw_y_stat_int_mode
27:24	RC	0x0	mipi_frame_end_vc mipi frame end [mipi_frame_end_vc3, mipi_frame_end_vc2, mipi_frame_end_vc1, mipi_frame_end_vc0] Note: Only on the fly mode detection
23:20	RC	0x0	mipi_frame_st_vc mipi frame start [mipi_frame_st_vc3, mipi_frame_st_vc2, mipi_frame_st_vc1, mipi_frame_st_vc0] Note: Only on the fly mode detection
19:17	RO	0x0	reserved
16	RC	0x0	mipi_linecnt line counter number reach the sw_csi_isp_linecnt
15	RC	0x0	raw3_wr_v_size_err raw3_wr data v size err
14	RC	0x0	raw2_wr_v_size_err raw2_wr data v size err
13	RC	0x0	raw1_wr_v_size_err raw1_wr data v size err
12	RC	0x0	raw0_wr_v_size_err raw0_wr data v size err
11	RC	0x0	raw3_wr_h_size_err raw3_wr data h size err
10	RC	0x0	raw2_wr_h_size_err raw2_wr data h size err
9	RC	0x0	raw1_wr_h_size_err raw1_wr data h size err
8	RC	0x0	raw0_wr_h_size_err raw0_wr data h size err
7	RO	0x0	reserved
6	RC	0x0	raw2_rd_frame_end raw2 read data frame end
5	RC	0x0	raw1_rd_frame_end raw1 read data frame end
4	RC	0x0	raw0_rd_frame_end raw0 read data frame end
3	RC	0x0	raw3_wr_frame_end raw3 write data frame end

2	RC	0x0	raw2_wr_frame_end raw2 write data frame end
1	RC	0x0	raw1_wr_frame_end raw1 write data frame end
0	RC	0x0	raw0_wr_frame_end raw0 write data frame end

CSI2RX_1C00_MASK_PHY

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	sw_imsk_phy_errcontrol Mask for phy control err
19:16	RO	0x0	reserved
15:12	RW	0x0	sw_imsk_phy_erresc Mask for phy esc err
11:8	RW	0x0	sw_imsk_phy_erreotsynchs Mask for phy eotsynchs err
7:4	RW	0x0	sw_imsk_phy_errsotsynchs Mask for phy sotsynchs err
3:0	RW	0x0	sw_imsk_phy_errsoths Mask for phy soths err

CSI2RX_1C00_MASK_PACKET

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_imsk_checksum_error Mask for CRC checksum error
23:21	RO	0x0	reserved
20	RW	0x0	sw_imsk_ecc_2bit_error Mask for ecc 2bit error
19:16	RW	0x0	sw_imsk_ecc_1bit_error Mask for ecc 1bit error
15:12	RW	0x0	sw_imsk_err_id Mask for id err
11:8	RW	0x0	sw_imsk_err_frame_data Mask for err_frame_data
7:4	RW	0x0	sw_imsk_err_f_seq Mask for err_f_seq
3:0	RW	0x0	sw_imsk_err_f_bndry_match Mask for error in correspondence between Frame Starts and Frame Edns.

CSI2RX_1C00_MASK_OVERFLOW

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RC	0x0	sw_imsk_y_stat_afifox3_overflow Mask for raw0~2 to y statistic afifo overflow [0] raw0 afifo overflow [1] raw1 afifo overflow [2] raw2 afifo overflow
19	RW	0x0	sw_imsk_ibuf3r_overflow Mask for ibuf_r_fifo overflow
18:16	RW	0x0	sw_imsk_ibufx3_overflow Mask for ibufx3 overflow [0] : ibuf_s_fifo overflow [1] : ibuf_l_fifo overflow [2] : ibuf_m_fifo overflow
15	RO	0x0	reserved
14	RW	0x0	sw_imsk_afifo22_overflow Mask for afifo22 overflow
13	RW	0x0	sw_imsk_afifo21_overflow Mask for afifo21 overflow
12	RW	0x0	sw_imsk_afifo20_overflow Mask for afifo20 woverflow
11	RW	0x0	sw_imsk_lafifo13_overflow Mask for lafifo13 overflow
10	RW	0x0	sw_imsk_lafifo12_overflow Mask for lafifo12 overflow
9	RW	0x0	sw_imsk_lafifo11_overflow Mask for lafifo11 overflow
8	RW	0x0	sw_imsk_lafifo10_overflow Mask for lafifo10 overflow
7	RW	0x0	sw_imsk_afifo13_overflow Mask for afifo13 overflow
6	RW	0x0	sw_imsk_afifo12_overflow Mask for afifo12 overflow
5	RW	0x0	sw_imsk_afifo11_overflow Mask for afifo11 overflow
4	RW	0x0	sw_imsk_afifo10_overflow Mask for afifo10 overflow
3:1	RO	0x0	reserved
0	RW	0x0	sw_imsk_afifo0_overflow Mask for afifo0 overfolw

CSI2RX_1C00_MASK_STAT

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_imsk_mipi_drop_frm Mask for mipi drop frame state
30:28	RC	0x0	sw_imsk_y_stat_end y stat end [raw2_y_stat_end, raw1_y_stat_end, raw0_y_stat_end]
27:24	RC	0x0	sw_imsk_mipi_frame_end_vc Mask for mipi frame end [mipi_frame_end_vc3, mipi_frame_end_vc2, mipi_frame_end_vc1, mipi_frame_end_vc0]
23:20	RC	0x0	sw_imsk_mipi_frame_st_vc Mask for mipi frame start [mipi_frame_st_vc3, mipi_frame_st_vc2, mipi_frame_st_vc1, mipi_frame_st_vc0]
19:17	RO	0x0	reserved
16	RW	0x0	sw_imsk_csi_isp_linecnt Mask for line counter number reach the sw_csi_isp_linecnt
15	RW	0x0	sw_imsk_raw3_wr_v_size_err Mask for raw3_wr data v size err
14	RW	0x0	sw_imsk_raw2_wr_v_size_err Mask for raw2_wr data v size err
13	RW	0x0	sw_imsk_raw1_wr_v_size_err Mask for raw1_wr data v size err
12	RW	0x0	sw_imsk_raw0_wr_v_size_err Mask for raw0_wr data v size err
11	RW	0x0	sw_imsk_raw3_wr_h_size_err Mask for raw3_wr data h size err
10	RW	0x0	sw_imsk_raw2_wr_h_size_err Mask for raw2_wr data h size err
9	RW	0x0	sw_imsk_raw1_wr_h_size_err Mask for raw1_wr data h size err
8	RW	0x0	sw_imsk_raw0_wr_h_size_err Mask for raw0_wr data h size err
7	RO	0x0	reserved
6	RW	0x0	sw_imsk_raw2_rd_frame_end Mask for raw2_rd data frame_end
5	RW	0x0	sw_imsk_raw1_rd_frame_end Mask for raw_rd1 data frame_end
4	RW	0x0	sw_imsk_raw0_rd_frame_end Mask for raw_rd0 data frame_end
3	RW	0x0	sw_imsk_raw3_wr_frame_end Mask for raw3_wr frame end
2	RW	0x0	sw_imsk_raw2_wr_frame_end Mask for raw2_wr frame end

1	RW	0x0	sw_imsk_raw1_wr_frame_end Mask for raw1_wr frame end
0	RW	0x0	sw_imsk_raw0_wr_frame_end Mask for raw0_wr frame end

CSI2RX_1C00_RAW0_WR_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_raw0self_force_upd raw0 self force update Note: If readback this register, it's sw_csi_raw0_wr_en_shd
30:22	RO	0x0	reserved
21:16	RW	0x2e	sw_csi_raw16_id set raw16 new id, data type
15:8	RW	0x02	sw_csi_raw0_wr_chan raw0_wr channel enable
7:3	RO	0x0	reserved
2	RW	0x0	sw_csi_raw0_wr_align raw0_wr pix-out align mode 1'b0: big-endian 1'b1: little-endian
1	RW	0x0	sw_csi_raw0_wr_uncompact raw0_wr pix-out uncompact mode 1'b0: uncompact 1'b1: compact
0	RW	0x0	sw_csi_raw0_wr_en_org raw0_wr enable, hold when enable The channel that write csi data to ddr. 1'b1: Enable the channel 1'b0: Disable teh channel

CSI2RX_1C00_RAW0_WR_LINECNT_RO

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw0_wr_line_cnt current raw0_wr line counter

CSI2RX_1C00_RAW0_WR_PIC_SIZE

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw0_wr_v_size_org if (sw_csi_raw0_wr_v_size_org equal 0), use regs_acq_v_size value
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw0_wr_h_size_org if (sw_csi_raw0_wr_h_size_org equal 0), use regs_acq_h_size value

CSI2RX_1C00_RAW0_WR_PIC_OFF

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw0_wr_v_off vertical sample offset of damtx0
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw0_wr_h_off horizontal sample offset of raw0_wr

CSI2RX_1C00_RAW1_WR_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_raw1self_force_upd raw1 self force update Note: If readback this register, it's sw_csi_raw1_wr_en_shd
30:16	RO	0x0	reserved
15:8	RW	0x02	sw_csi_raw1_wr_chan raw1_wr channel enable
7:3	RO	0x0	reserved
2	RW	0x0	sw_csi_raw1_wr_align raw1_wr pix-out align mode 1'b0: big-endian 1'b1: little-endian
1	RW	0x0	sw_csi_raw1_wr_uncompact raw1_wr pix-out simg_mod enable
0	RW	0x0	sw_csi_damtx1_en_org raw1_wr enable, hold when enable

CSI2RX_1C00_RAW1_WR_LINECNT_RO

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw1_wr_line_cnt current raw1_wr line counter

CSI2RX_1C00_RAW1_WR_PIC_SIZE

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw1_wr_v_size_org if (sw_csi_raw1_wr_v_size_org equal 0), use regs_acq_v_size value
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw1_wr_h_size_org if (sw_csi_raw1_wr_h_size_org equal 0), use regs_acq_h_size value

CSI2RX_1C00_RAW1_WR_PIC_OFF

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw1_wr_v_off vertical sample offset of damtx1
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw1_wr_h_off horizontal sample offset of raw1_wr

CSI2RX_1C00_RAW2_WR_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_raw2self_force_upd raw2 self force update Note: If readback this register, it's sw_csi_raw2_wr_en_shd
30:16	RO	0x0	reserved
15:8	RW	0x01	sw_csi_raw2_wr_chan raw2_wr channel enable
7:3	RO	0x0	reserved
2	RW	0x0	sw_csi_raw2_wr_align raw2_wr pix-out align mode 1'b0: big-endian 1'b1: little-endian
1	RW	0x0	sw_csi_raw2_wr_uncompact raw2_wr pix-out simg_mod enable
0	RW	0x0	sw_csi_damtx2_en_org raw2_wr enable, hold when enable

CSI2RX_1C00_RAW2_WR_LINECNT_RO

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw2_wr_line_cnt current raw2_wr line counter

CSI2RX_1C00_RAW2_WR_PIC_SIZE

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw2_wr_v_size_org if (sw_csi_raw2_wr_v_size_org equal 0), use regs_acq_v_size value
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw2_wr_h_size_org if (sw_csi_raw2_wr_h_size_org equal 0), use regs_acq_h_size value

CSI2RX_1C00_RAW2_WR_PIC_OFF

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw2_wr_v_off vertical sample offset of damtx2
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw2_wr_h_off horizontal sample offset of raw2_wr

CSI2RX_1C00_RAW3_WR_CTRL

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_raw3self_force_upd raw3 self force update Note: If readback this register, it's sw_csi_raw3_wr_en_shd
30:16	RO	0x0	reserved
15:8	RW	0x08	sw_csi_raw3_wr_chan raw3_wr channel enable
7:3	RO	0x0	reserved
2	RW	0x0	sw_csi_raw3_wr_align raw3_wr pix-out align mode 1'b0: big-endian 1'b1: little-endian
1	RW	0x0	sw_csi_raw3_wr_uncompact raw3_wr pix-out simg_mod enable
0	RW	0x0	sw_csi_damtx3_en_org raw3_wr enable, hold when enable

CSI2RX_1C00_RAW3_WR_LINECNT_RO

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw3_wr_line_cnt current raw3_wr line counter

CSI2RX_1C00_RAW3_WR_PIC_SIZE

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw3_wr_v_size_org if (sw_csi_raw3_wr_v_size_org equal 0), use regs_acq_v_size value
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw3_wr_h_size_org if (sw_csi_raw3_wr_h_size_org equal 0), use regs_acq_h_size value

CSI2RX_1C00_RAW3_WR_PIC_OFF

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw3_wr_v_off vertical sample offset of damtx3
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw3_wr_h_off horizontal sample offset of raw3_wr

CSI2RX_1C00_RAW_RD_CTRL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_rxself_force_upd All mipirx self force update Note: If readback this register, it's mipi working.
30:8	RO	0x0	reserved
7:5	RW	0x0	sw_csi_raw_rd_chan_sel raw_rd sw_csi_id_7to0 id input id-sel, default id0
4	RW	0x0	sw_csi_raw_rd_align raw_rd pix-out align mode 1'b0: big-endian 1'b1: little-endian
3	RW	0x0	sw_csi_raw_rd_uncompact raw_rd pix-out simg_mod enable
2	RW	0x0	sw_csi_raw2_rd_en_org raw_rd1 enable Auto clear when finish
1	RW	0x0	sw_csi_raw1_rd_en_org raw_rd1 enable Auto clear when finish
0	RW	0x0	sw_csi_raw0_rd_en_org raw_rd0 enable Auto clear when finish

CSI2RX_1C00_RAW_RD_LINECNT_RO

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_raw1_rd_isp_line_cnt current raw_rd1 to isp line counter
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw0_rd_isp_line_cnt current raw_rd0 to isp line counter

CSI2RX_1C00_RAW_RD_PIC_SIZE

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw_rd_v_size_org if (sw_csi_raw_rd_v_size_org equal 0), use regs_acq_v_size value
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw_rd_h_size_org if (sw_csi_raw_rd_h_size_org equal 0), use regs_acq_h_size value

CSI2RX_1C00_RAW2_RD_LINECNT_RO

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw2_rd_isp_line_cnt current raw2_rd to isp line counter

CSI2RX_1C00_RAWFBC_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:8	RW	0x0	sw_rawfbc_head_diff_num head diff num between fbce and fbcd 2'b00: Head diff num = head_burst_len (default) 2'b01: Head diff num = head_burst_len * 2 2'b10: Head diff num = head_burst_len * 4
7:5	RO	0x0	reserved
4	RW	0x1	sw_rawfbc_head_diff_en head data read ctrl en based on rawfbce and rawfbce speed 1'b1: Enable (default) 1'b0: Disable
3:2	RO	0x0	reserved
1	RW	0x0	sw_rawfbc_en fbce enable 1'b1: Enable 1'b0: Disable
0	RW	0x1	sw_raw_out_en raw output to tx 1'b1: Enable 1'b0: Disable

CSI2RX_1C00_ESPHDR_LCNT

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:12	RW	0x10	sw_csi_esp_lcnt_padnum the number needed to identify padding row
11:0	RW	0x004	sw_csi_esp_lcnt_padpix padding row payload, default value as follows: raw10: 0x1 raw12: 0x4

CSI2RX_1C00_ESPHDR_IDCD

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x12	sw_csi_esp_idcd_efpix3 identification code of Effective line, default value as follows: raw10: 0x12 raw12: 0x12
23	RO	0x0	reserved
22:16	RW	0x12	sw_csi_esp_idcd_efpix2 identification code of Effective line, default value as follows: raw10: 0x12 raw12: 0x12
15	RO	0x0	reserved
14:8	RW	0x12	sw_csi_esp_idcd_efpix1 identification code of Effective line, default value as follows: raw10: 0x12 raw12: 0x12
7	RO	0x0	reserved
6:0	RW	0x11	sw_csi_esp_idcd_efpix0 identification code of Effective line, default value as follows: raw10: 0x12 raw12: 0x12

CSI2RX_1C00_ESPHDR_CTRL

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	sw_csi_esp_short_chan Short channel enable Only on-the-fly mode is available for short-frame.

CSI2RX_1C00_VC0_FRAME_NUM_RO

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_csi_vc0_fs_num 16 bit frame number from VC0 Frame Start (FS) short packet
15:0	RO	0x0000	ro_csi_vc0_fe_num 16 bit frame number from VC0 Frame End (FE) short packet

CSI2RX_1C00_VC1_FRAME_NUM_RO

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_csi_vc1_fs_num 16 bit frame number from VC1 Frame Start (FS) short packet
15:0	RO	0x0000	ro_csi_vc1_fe_num 16 bit frame number from VC1 Frame End (FE) short packet

CSI2RX_1C00_VC2_FRAME_NUM_RO
Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_csi_vc2_fs_num 16 bit frame number from VC2 Frame Start (FS) short packet
15:0	RO	0x0000	ro_csi_vc2_fe_num 16 bit frame number from VC2 Frame End (FE) short packet

CSI2RX_1C00_VC3_FRAME_NUM_RO
Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_csi_vc3_fs_num 16 bit frame number from VC3 Frame Start (FS) short packet
15:0	RO	0x0000	ro_csi_vc3_fe_num 16 bit frame number from VC3 Frame End (FE) short packet

CSI2RX_1C00_ISP_LINECNT_RO
Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	ro_csi_isp_line_cnt current csi to isp line counter

CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO
Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	ro_r1fifo_space2full lafifo11_space2full
27:24	RO	0x0	ro_r0fifo_space2full lafifo10_space2full
23:0	RO	0x000000	ro_ibuf_debug_status ibuf working debug status, mipi_clk

CSI2RX_1C00_RAW_WR_IBUF3_STATUS_RO
Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:11	RO	0x0	ro_r3fifo_space2full lafifo13_space2full
10:7	RO	0x0	ro_r2fifo_space2full lafifo12_space2full
6:0	RO	0x00	ro_ibuf3_debug_status ibuf3 working debug status, mipi_clk, including: ro_ibuf3_debug_status[3:0]: ro_ibuf3_space2full ro_ibuf3_debug_status[4]: ibuf3r_ready ro_ibuf3_debug_status[5]: ibuf3_start_flag ro_ibuf3_debug_status[6]: ibuf3_work_end

CSI2RX_1C00_CUR_HEADER_RO

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_csi_cur_header rxbyte_clk domain current header

CSI2RX_1C00_FPN_CTRL

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	sw_fpn_bits calculate data bits selsction 2'b00: 3'b000, x; 2'b01: 2'b00, x, 1'b0; 2'b10: 1'b0, x, 2'b00; 2'b11: x, 3'b000 Note:"x" is 4 bits data, frame FPN_TABLE_DATA
1	RW	0x0	sw_cfpn_n colum fpn enable, active low 1'b0: col fpn 1'b1: row fpn
0	RW	0x0	sw_fpn_en sw_fpn_en 1'b0: Disable 1'b1: Enable

CSI2RX_1C00_FPN_TABLE_CTRL

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	sw_fpn_cfg_ing write fpn data to memory, active high 1'b0: Disable/finish config 1'b1: Write table data to memory enable

CSI2RX_1C00_FPN_TABLE_DATA

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fpn_table_data FPN data register to memory

CSI2RX_1C00_CSI_Y_STAT_CTRL

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	sw_black_level_b y statistic black level of B
23:21	RO	0x0	reserved
20:16	RW	0x00	sw_black_level_g y statistic black level of G
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_black_level_r y statistic black level of R
7:6	RW	0x0	sw_y_stat_rd_tile_id y statistic read tileline id 2'b00: Read y_stat from tileline0 offset 2'b01: Read y_stat from tileline1 offset 2'b10: Read y_stat from tileline2 offset 2'b11: Read y_stat from tileline3 offset Note: tileline0 offset, 0; tileline1 offset, 4; tileline2 offset, 8; tileline3 offset, 12
5:4	RW	0x0	sw_y_stat_rd_frm_id y statistic read frame id 2'b00: Read y_stat from raw0 start addr in sram 2'b01: Read y_stat from raw1 start addr in sram 2'b10: Read y_stat from raw2 start addr in sram 2'b11: Reserved Note: raw0 start addr, 0; raw1 start addr, 16; raw2 start addr, 32
3:2	RW	0x0	sw_y_stat_int_mode y statistic interrupt generation mode 2'b00: Each tileline generate once interrupt 2'b01: Two tileline generate once interrupt 2'b10: Frame end generate once interrupt 2'b11: Reserved Note: Each tileline including 4blocks at horizon direction
1	RW	0x1	sw_y_stat_rd_en y statistic read enable for read y_stat sram address update, auto-clear 1'b0: Disable 1'b1: Enable when the first read y_stat sram in each frame, should config sw_y_stat_rd_en = 1, give read start address in sram. Note: SRAM addr from 0 to 47; raw0, 0~15; raw1, 16~31; raw2, 32~47. read sram addr = sw_y_stat_rd_frm_id (corresponding addr) + sw_y_stat_rd_tile_id (corresponding offset)

0	RW	0x1	sw_y_stat_en y statistic enable 1'b0: Disable 1'b1: Enable Note: y statistic is based on 4x4 block, and each block size are calculated by hardware

CSI2RX_1C00_CSI_Y_STAT_RO

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_y_stat_buf_rdata y statistic read data from sram. Read according to y_stat interrupt in ERR_PACKET[30:28]

CSI2RX_1C00_VERSION

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:0	RO	0x02021812	version_id Version of the DWC_mipi_csi2_host Value after Reset: 32'h02021812 integrated in ISP (max: 02; min: 02 date: 1812)

12.4.2.2 MI

MI_1400_MI_WR_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sw_sp_wr_output_format Selects output format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 3'b111: Reserved 3'b110: RGB 888 3'b101: RGB 666 3'b100: RGB 565 3'b011: YCbCr 4:4:4 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. - For RGB output format the SP input format must be YCbCr 4:2:2
27:26	RW	0x0	sw_sp_wr_input_format Selects input format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 2'b11: YCbCr 4:4:4 2'b10: YCbCr 4:2:2 2'b01: YCbCr 4:2:0 2'b00: YCbCr 4:0:0 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
25:24	RW	0x0	sw_sp_wr_format Defines how YCbCr self picture data is written to memory. Must be set to 00 if RGB conversion is active. Note that with RGB conversion active the output format is always interleaved. 2'b00: Planar 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

23:22	RW	0x0	sw_mp_wr_format Defines how YCbCr main picture data is written to memory. Ignored if JPEG data is chosen. In YCbCr mode the following meaning is applicable 2'b00: Planar 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved In RAW data mode the following meaning is applicable 2'b00: RAW 8 bit 2'b01: Reserved 2'b10: RAW 12 bit 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.
21	RW	0x0	sw_mi_wr_init_offset_en Enables updating of the offset counters shadow registers for main and self picture to the programmed register init values. MI_MP/SP_Y/CB/CR_OFFS_CNT_INIT -> MI_MP/SP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic config update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip init mode (see bit skip in register MI_INIT).
20	RW	0x0	sw_mi_wr_init_base_en Enables updating of the base address and buffer size shadow registers for main and self picture to the programmed register init values. MI_MP/SP_Y/CB/CR_BASE_AD_INIT -> MI_MP/SP_Y/CB/CR_BASE_AD_SHD MI_MP/SP_Y/CB/CR_SIZE_INIT -> MI_MP/SP_Y/CB/CR_SIZE_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic config update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected.

19:18	RW	0x2	sw_mi_wr_burst_len_chrom_org Burst length for Cb or Cr data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. If rotation is active, then only 4-beat bursts will be generated in self path, regardless of the setting here. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
17:16	RW	0x2	sw_mi_wr_burst_len_lum_org Burst length for Y data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15	RW	0x0	sw_mi_wr_last_pixel_sig_en enables the last pixel signalization 1'b1: Enabled 1'b0: Disabled
14	RW	0x0	sw_sp_wr_auto_upd automatic update of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled
13	RW	0x0	sw_mp_wr_auto_upd automatic update of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled Note: If mp pingpong enable, it needs to be set "1".
12	WO	0x0	sw_sp_wr_pingpong_en pingpong mode of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled

11	RW	0x0	sw_mp_wr_pingpong_en pingpong mode of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled
10	RW	0x0	sw_mi_wr_422noncosited Enables self path YCbCr422non-co-sited -> YCbCr444 interpolation (M5_v6, M5_v7 only) 1'b1: YCbCr422 data are non_co-sited (Cb and Cr samples are centered between Y samples) so modified interpolation is activated 1'b0: YCbCr422 data are co-sited (Y0 Cb0 and Cr0 are sampled at the same position) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
9	RW	0x0	sw_mi_wr_cbcr_full_range Enables CbCr full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: CbCr have full range (0..255) 1'b0: CbCr have compressed range range (16..240) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
8	RW	0x0	sw_mi_wr_y_full_range Enables Y full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: Y has full range (0..255) 1'b0: Y has compressed range (16..235) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
7	RW	0x0	sw_mi_wr_byte_swap Enables change of byte order of the 32 bit output word at write port 1'b1: Byte order is mirrored but the bit order within one byte doesnt change 1'b0: No byte mirroring Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.

6	RW	0x0	sw_mi_wr_rot Rotation 90 degree counter clockwise of self picture, only in RGB mode. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For RGB 565 format the line length must be a multiple of 2. There are no restrictions for RGB 888/666. 1'b1: Enabled 1'b0: Disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. In rotation mode only 4-beat bursts are supported for self-path. not support rotation90 function in the newset version now;
5	RW	0x0	sw_mi_wr_v_flip Vertical flipping of self picture. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. 1'b1: Enabled 1'b0: Disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
4	RW	0x0	sw_mi_wr_h_flip Horizontal flipping of self picture. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. 1'b1: Enabled 1'b0: Disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

3:0	RW	0x0	sw_mi_wr_path_enable Enables data pathes of MI according to the following table: 4'b0000: Disabled, no data is transferred 4'b0001: YUV data output, mainpath only (mp_enable only) 4'b0010: Self-path only, output data format depending on other settings (sp_enable only) 4'b0011: YUV data output in mainpath and self-path image data active 4'b0100: JPEG data output, mainpath only (jpeg_enable only) 4'b0101: Not allowed 4'b0110: JPEG data output in mainpath and self-path image data active 4'b0111: Not allowed 4'b1000: RAW data output, mainpath only (raw_enable only) 4'b1001: Defect pixel data on self-path, image data on mainpath 4'b1010: Defect pixel data on mainpath, image data on self-path 4'b1011: Not allowed 4'b1100: Defect pixel data on self-path, JPEG data on mainpath 4'b1101: Defect pixel data on mainpath only 4'b1110: Defect pixel data on self-path only 4'b1111: Defect pixel data on self-path, RAW data on mainpath Programmed value becomes effective (visible in shadow register) after a soft reset, a forced software update or an automatic config update. Affects MI_IN and MI_OUT module.

MI_1400_MI_WR_INIT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	sw_mp_wr_vir_stride_old 1'b0: mp virstual stride mode 1'b1: mp no virtual stride mode
15:7	RO	0x0	reserved
6	RW	0x0	sw_mi_update_last_pixel_en If this bit set 1, MI IN and MI OUT module will update at the time of dual crop module sent out the last pixel
5	RW	0x1	sw_mi_update_mode 1'b0: Old mode 1'b1: New mode, all path will update when frame_end In new mode, all path regs of MI will be updated at right time; (not support input RAW/JEPG mode)
4	WO	0x0	sys_mi_cfg_upd Forced configuration update. Leads to an immediate update of the shadow registers. Depending on the two init enable bits in the MI_CTRL register (init_offset_en and init_base_en) the offset counter, base address and buffer size shadow registers are also updated.
3	RO	0x0	reserved

2	RW	0x0	sw_mi_skip Skip of current or next starting main picture: Aborts writing of main picture image data of the current frame to RAM (after the current burst transmission has been completed). Further main picture data up to the end of the current frame are discarded. No further makroblock line interrupt (mblk_line), no wrap around interrupt for main picture (wrap_mp_y/cb/cr) and no fill level interrupt (fill_mp_y) are generated. Skip does not affect the generation of the main path frame end interrupt (mp_frame_end). Skip does not affect the processing of self picture and its corresponding interrupts namely the self path frame end interrupt (sp_frame_end). The byte counter (register MI_WR_BYTE_CNT) is not affected. It produces the correct number of JPEG or RAW data bytes at the end of the current (skipped) frame. After a skip has been performed the offset counter for the main picture at the start of the following frame are set depending on the bit init_offset_en in register MI_WR_CTRL: - Skip restart mode (init_offset_en = 0) The offset counters of the main picture are restarted at the old start values of the previous skipped frame. - Skip init mode (init_offset_en = 1) The offset counters of the main picture are initialized with the register contents of the offset counter init registers without any additional forced software update or automatic config update.
1:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_BASE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- MI_MP_Y_BASE_AD_INIT --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(MI_MP_Y_BASE_AD_INIT, address_value) is equivalent to write(MI_MP_Y_BASE_AD_INIT, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if camerIC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_SIZE

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_size Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- MI_MP_Y_SIZE_INIT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_offs_cnt Offset counter init value of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- MI_MP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_START

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Y component, JPEG or raw data). Updated at frame end. Note: A soft reset resets the contents to the reset value. --- MI_MP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base Base address of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASEwith respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cb_size Size of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cb_offs_cnt Offset counter init value of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_START

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cb component). Updated at frame end. --- MI_MP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base Base address of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cr_size Size of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cr_offs_cnt Offset counter init value of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_START

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cr component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_y_base Base address of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_sp_wr_y_size Size of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_sp_wr_y_offs_cnt Offset counter init value of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_START

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Y component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_LLENGTH

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_sp_wr_y_llength_tmp Line length of self picture Y component or RGB picture in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_CB_BASE

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cb_base Base address of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cb_size Size of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_cb_offs_cnt_init Offset counter init value of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_START

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cb component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cr_base Base address of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cr_size Size of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cr_offs_cnt Offset counter init value of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_START

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cr component). Updated at frame end. --- MI_SP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_WR_BYTE_CNT

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	byte_cnt Counter value specifies the number of JPEG or RAW data bytes of the last transmitted frame. Updated at frame end. A soft reset will set the byte counter to zero.

MI_1400_MI_WR_CTRL_SHD

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RO	0x0	path_enable_out path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
15:4	RO	0x0	reserved
3:0	RO	0x0	path_enable_in path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)

MI_1400_MI_MP_WR_Y_BASE_SHD

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_y_base_shd Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_SIZE_SHD

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_size_shd Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_shd Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE_SHD

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cb_base_shd Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE_SHD

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_size_shd Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_shd Current offset counter of main picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE_SHD

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cr_base_shd Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE_SHD

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_size_shd Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_shd Current offset counter of main picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE_SHD

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_y_base_shd Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE_SHD

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_size_shd Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_offs_cnt_shd Current offset counter of self picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_BASE_AD_SHD

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cb_base_shd Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE_SHD

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_size_shd Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_shd Current offset counter of self picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE_AD_SHD

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cr_base_shd Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE_SHD

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_size_shd Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_shd Current offset counter of self picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_RD_Y_PIC_START_AD

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_y_pic_start_ad Image start address of the y component Note: Must be multiple of 4 in interleaved mode.

MI_1400_MI_RD_Y_PIC_WIDTH

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_mi_rd_y_pic_width Image width of the Y component in pixel. For YCbCr 4:2:x the image width must be a multiple of 2. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used.

MI_1400_MI_RD_Y_LLENGTH

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_mi_rd_y_llength Line length of the Y component of the original image in memory For an uncropped image, where lines follow each other without offset (no line stride), line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr line length is used.

MI_1400_MI_RD_Y_PIC_SIZE

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mi_rd_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (dma_y_llength * dma_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb component (which includes Cr) is assumed half for 4:2:0 and the same size for 4:2:2. In interleave mode no Cb/Cr image size is used.

MI_1400_MI_RD_CB_PIC_START_AD

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_cb_pic_start_ad Image start address of the Cb component Note: Must be multiple of 2 in semi-planar mode.

MI_1400_MI_RD_CR_PIC_START_AD

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_cr_pic_start_ad Image start address of the Cr component

MI_1400_MI_IMSC

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mpfbc_wr_frame_end Mask mpfbc write end of frame interrupt
30	RW	0x0	isp_bus_err Mask bit for isp bus error interrupt
29:23	RO	0x0	reserved
22	RW	0x0	bay3d_frame_end Mask bay3d write end of frame interrupt
21	RW	0x0	gain_wr_frame_end Mask gain write end of frame interrupt
20	RW	0x0	dbr_wr_frame_end Mask mimux write end of frame interrupt
19	RW	0x0	raw3_wr_frame_end Mask raw1 tx end of frame interrupt
18	RW	0x0	raw2_wr_frame_end Mask raw2 tx end of frame interrupt
17	RW	0x0	raw1_wr_frame_end Mask raw1 tx end of frame interrupt
16	RW	0x0	raw0_wr_frame_end Mask raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_en Mask all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_en Mask of Y12 C COMPENT picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_en Mask of Y12 Y COMPENT picture end of frame interrupt
11	RW	0x0	dma_ready Mask bit for dma ready interrupt
10	RW	0x0	fill_mp_y2 Mask bit for fill level interrupt 2 of main picture Y, JPEG or raw data
9	RW	0x0	wrap_sp_cr Mask bit for self picture Cr address wrap interrupt
8	RW	0x0	wrap_sp_cb Mask bit for self picture Cb address wrap interrupt
7	RW	0x0	wrap_sp_y Mask bit for self picture Y address wrap interrupt
6	RW	0x0	wrap_mp_cr Mask bit for main picture Cr address wrap interrupt
5	RW	0x0	wrap_mp_cb Mask bit for main picture Cb address wrap interrupt
4	RW	0x0	wrap_mp_y Mask bit for main picture Y address wrap interrupt

3	RW	0x0	fill_mp_y Mask bit for fill level interrupt of main picture Y, JPEG or raw data
2	RW	0x0	mblk_line Mask bit for makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM)
1	RW	0x0	sp_frame_end Mask self picture end of frame interrupt
0	RW	0x0	mp_frame_end Mask main picture end of frame interrupt

MI_1400_MI_RIS

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Raw status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Raw status of isp bus error interrupt
29:23	RO	0x0	reserved
22	RO	0x0	bay3d_frame_end Raw status of bay3d write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Raw status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Raw status of mimux write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Raw status of raw0 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Raw status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Raw status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Raw status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_rawsts Raw status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_rawsts Raw status of Y12 C picture end of frame interrupt
12	RO	0x0	ro_y12y_frame_end_rawsts Raw status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Raw status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Raw status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Raw status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Raw status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Raw status of self picture Y address wrap interrupt
6	RO	0x0	wrap_mp_cr Raw status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Raw status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Raw status of main picture Y address wrap interrupt

3	RO	0x0	fill_mp_y Raw status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Raw status of makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Raw status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Raw status of main picture end of frame interrupt

MI_1400_MI_MIS

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Masked status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Masked status of isp bus error interrupt
29:23	RO	0x0	reserved
22	RO	0x0	bay3d_frame_end Masked status of bay3d write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Masked status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Masked status of mimux write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Masked status of raw3 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Masked status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Masked status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Masked status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_sts Masked status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_sts Masked status of Y12 C picture end of frame interrupt
12	RO	0x0	ro_y12y_frame_end_sts Masked status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Masked status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Masked status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Masked status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Masked status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Masked status of self picture Y address wrap interrupt
6	RO	0x0	wrap_mp_cr Masked status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Masked status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Masked status of main picture Y address wrap interrupt

3	RO	0x0	fill_mp_y Masked status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Masked status of makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Masked status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Masked status of main picture end of frame interrupt

MI_1400_MI_ICR

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Clear mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Clear isp bus error interrupt
29:23	RO	0x0	reserved
22	WO	0x0	bay3d_frame_end Clear bay3d write end of frame interrupt
21	WO	0x0	gain_wr_frame_end Clear gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Clear mimux write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Clear raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Clear raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Clear raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Clear raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_clr Clear all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_clr Clear Y12 C picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_clr Clear Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Clear dma ready interrupt
10	WO	0x0	fill_mp_y2 Clear fill level interrupt 2
9	WO	0x0	wrap_sp_cr Clear self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Clear self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Clear self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Clear main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Clear main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Clear main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Clear fill level interrupt

2	WO	0x0	mblk_line Clear makroblock line interrupt
1	WO	0x0	sp_frame_end Clear self picture end of frame interrupt
0	WO	0x0	mp_frame_end Clear main picture end of frame interrupt

MI_1400_MI_ISR

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Set mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Set isp bus error interrupt
29:23	RO	0x0	reserved
22	WO	0x0	bay3d_frame_end Set bay3d write end of frame interrupt
21	WO	0x0	gain_wr_frame_end Set gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Set mimux write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Set raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Set raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Set raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Set raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_set Set all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_set Set Y12 C picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_set Set Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Set dma ready interrupt
10	WO	0x0	fill_mp_y2 Set fill level interrupt 2
9	WO	0x0	wrap_sp_cr Set self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Set self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Set self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Set main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Set main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Set main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Set fill level interrupt

2	WO	0x0	mblk_line Set makroblock line interrupt
1	WO	0x0	sp_frame_end Set self picture end of frame interrupt
0	WO	0x0	mp_frame_end Set main picture end of frame interrupt

MI_1400_MI_STATUS

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RO	0x0	bay3d_fifo_full FIFO full flag of bay3d FIFO asserted since last clear
13	RO	0x0	gain_fifo_full FIFO full flag of gain FIFO asserted since last clear
12	RO	0x0	dbr_wr_y_fifo_full FIFO full flag of Y FIFO in mimux write path asserted since last clear
11	RO	0x0	raw3_wr_y_fifo_full FIFO full flag of Y FIFO in raw3 tx path asserted since last clear
10	RO	0x0	raw2_wr_y_fifo_full FIFO full flag of Y FIFO in raw2 tx path asserted since last clear
9	RO	0x0	raw1_wr_y_fifo_full FIFO full flag of Y FIFO in raw1 tx path asserted since last clear
8	RO	0x0	raw0_wr_y_fifo_full FIFO full flag of Y FIFO in raw0 tx path asserted since last clear
7	RO	0x0	reserved
6	RO	0x0	sp_cr_fifo_full FIFO full flag of Cr FIFO in self path asserted since last clear
5	RO	0x0	sp_cb_fifo_full FIFO full flag of Cb FIFO in self path asserted since last clear
4	RO	0x0	sp_y_fifo_full FIFO full flag of Y FIFO in self path asserted since last clear
3	RO	0x0	reserved
2	RO	0x0	mp_cr_fifo_full FIFO full flag of Cr FIFO in main path asserted since last clear
1	RO	0x0	mp_cb_fifo_full FIFO full flag of Cb FIFO in main path asserted since last clear
0	RO	0x0	mp_y_fifo_full FIFO full flag of Y FIFO in main path asserted since last clear

MI_1400_MI_STATUS_CLR

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	WO	0x0	bp_cb_fifo_full Clear status of Cb FIFO full flag in bypass path
17	WO	0x0	bp_y_fifo_full Clear status of Y FIFO full flag in bypass path
16	WO	0x0	bay3d_ds_fifo_full Clear status of bay3d down scale FIFO full flag
15	WO	0x0	bay3d_cur_fifo_full Clear status of bay3d current FIFO full flag
14	WO	0x0	bay3d_iir_fifo_full Clear status of bay3d iir FIFO full flag
13	WO	0x0	gain_fifo_full Clear status of gain FIFO full flag
12	WO	0x0	dbr_wr_y_fifo_full Clear status of Y FIFO full flag in mimux write path
11	WO	0x0	raw3_wr_y_fifo_full Clear status of Y FIFO full flag in raw3 tx path
10	WO	0x0	raw2_wr_y_fifo_full Clear status of Y FIFO full flag in raw2 tx path
9	WO	0x0	raw1_wr_y_fifo_full Clear status of Y FIFO full flag in raw1 tx path
8	WO	0x0	raw0_wr_y_fifo_full Clear status of Y FIFO full flag in raw0 tx path
7	RO	0x0	reserved
6	WO	0x0	sp_cr_fifo_full Clear status of Cr FIFO full flag in self path
5	WO	0x0	sp_cb_fifo_full Clear status of Cb FIFO full flag in self path
4	WO	0x0	sp_y_fifo_full Clear status of Y FIFO full flag in self path
3	RO	0x0	reserved
2	WO	0x0	mp_cr_fifo_full Clear status of Cr FIFO full flag in main path
1	WO	0x0	mp_cb_fifo_full Clear status of Cb FIFO full flag in main path
0	WO	0x0	mp_y_fifo_full Clear status of Y FIFO full flag in main path

MI_1400_MI_SP_WR_Y_PIC_WIDTH
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_sp_wr_y_pic_width Image width of the self picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_HEIGHT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_sp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_SIZE

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:0	RW	0x0000000	sw_sp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_RD_CTRL
Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	sw_mi_rd_start_sel DMA read start mode 1'b1: sw_mi_rd_start_pre 1'b0: sw_mi_rd_start_pre toggle
13:12	RW	0x0	sw_mi_rd_rgb_format Selects RGB Bayer data of read DMA picture 2'b00: No DMA RGB Bayer data 2'b01: 8 bit RGB Bayer data 2'b10: 16 bit RGB Bayer data (12 bit used) bytes are organized MSB first and 4 lower bits of LSB remain unused: byte_even -> bayer[11:4], byte_odd[7:4] -> bayer[3:0] 2'b11: Reserved.
11	RO	0x0	reserved
10	RW	0x0	sw_mi_rd_frame_end_disable Suppresses v_end so that no frame end can be detected by following instances. Note: The dma_ready interrupt is raised as usual, but the dma_frame_end interrupt will not be generated until v_end has been enabled again.
9	RW	0x0	sw_mi_rd_continuous_en Enables continuous mode. If set the same frame is read back over and over. A start pulse on dma_start is needed only for the first time. To stop continuous mode reset this bit (takes effect after the next frame end) or execute a soft reset. This bit is intended to be used in conjunction with the Superimpose feature.
8	RW	0x0	sw_mi_rd_byte_swap Enables change of DMA byte order of the 32 bit input word at read port 1'b1: Byte order is mirrored but the bit order within one byte doesnt change 1'b0: No byte mirroring
7:6	RW	0x0	sw_mi_rd_inout_format Selects input/output format of DMA picture. 2'b11: YCbCr 4:4:4 2'b10: YCbCr 4:2:2 2'b01: YCbCr 4:2:0 2'b00: YCbCr 4:0:0
5:4	RW	0x0	sw_mi_rd_format Defines how YCbCr picture data is read from memory. 2'b00: Planar 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 and RGB only 2'b11: Reserved

3:2	RW	0x0	sw_mi_rd_burst_len_chrom Burst length for Cb or Cr data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported.
1:0	RW	0x0	sw_mi_rd_burst_len_lum Burst length for Y data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported.

MI_1400_MI_RD_START

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	sys_mi_rd_start_pre Enables DMA access. Additionally main or self path has to be enabled separately.

MI_1400_MI_RD_STATUS

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	sw_mi_rd_active If set DMA access is active.

MI_1400_MI_WR_PIXEL_CNT

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	pix_cnt Counter value specifies the number of pixels of the defect pixel list generated by DPCC of the last transmitted frame. Updated at frame end. A soft reset will set the counter to zero.

MI_1400_MI_MP_WR_Y_BASE2

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE2

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE2

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE2

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_BASE2

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE2

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_WR_XTD_FORMAT_CTRL

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	sw_mi_wr_nv21_dma_read 1'b0: DMA read path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: DMA read path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.
1	RW	0x0	sw_mi_wr_nv21_self 1'b0: Self path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Self path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.
0	RW	0x0	sw_mi_wr_nv21_main 1'b0: Main path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Main path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.

MI_1400_MI_WR_ID

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x6	sw_spcr_wr_axi_id spcr write id
27:24	RO	0x5	sw_spcb_wr_axi_id spcb write id
23:20	RO	0x4	sw_spy_wr_axi_id spy write id
19:16	RO	0x3	sw_mpcr_wr_axi_id mpcr write id
15:12	RO	0x2	sw_mpcb_wr_axi_id mpcb write id
11:8	RO	0x1	sw_mpy_wr_axi_id mpy write id
7:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs2 Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD

Address: Operational Base + offset (0x01e4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs2_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_LLENGTH

Address: Operational Base + offset (0x01e8)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	sw_mp_wr_y_llegnth Line length of main picture Y component or RGB picture in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_WR_CTRL2
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	W1C	0x0	sys_bay3d_self_force_upd force update of configuration registers for bay3dnr frame DMA write.
21	W1C	0x0	sys_gainself_force_upd force update of configuration registers for gain DMA write.
20	W1C	0x0	sys_dbrself_force_upd force update of configuration registers for debayer DMA write.
19:17	RO	0x0	reserved
16	RW	0x0	sw_bay3d_wr_auto_upd automatic update of configuration registers for bay3d write at frame end. 1'b1: Enabled 1'b0: Disabled
15:14	RO	0x0	reserved
13	RW	0x0	sw_gain_wr_auto_upd automatic update of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
12	RW	0x0	sw_gain_wr_pingpong_en pingpong mode of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
11	RO	0x0	reserved
10	RW	0x0	sw_dbr_wr_auto_upd automatic update of configuration registers for mimux write at frame end. 1'b1: Enabled 1'b0: Disabled
9	RW	0x0	sw_mimux_raw_align align mode, 32bit including two data 1'b0: big-endian 1'b1: little-endian
8	RW	0x0	sw_dbr_enable_org mimux enable for isp_hdrtmo data mux to ddr and read back to isp_debayer
7:4	RO	0x0	reserved
3	RW	0x0	sw_raw3_wr_auto_upd automatic update of configuration registers for raw3 tx at frame end. 1'b1: Enabled 1'b0: Disabled

2	RW	0x0	sw_raw2_wr_auto_upd automatic update of configuration registers for raw2 tx at frame end. 1'b1: Enabled 1'b0: Disabled
1	RW	0x0	sw_raw1_wr_auto_upd automatic update of configuration registers for raw1 tx at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_raw0_wr_auto_upd automatic update of configuration registers for raw0 tx at frame end. 1'b1: Enabled 1'b0: Disabled

MI_1400_MI_WR_ID2

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	sw_bay3d_iir_wr_axi_id bay3d iir write id, read only
27:24	RO	0x0	sw_gain_wr_axi_id gain write id, read only
23:20	RO	0x0	sw_dbr_wr_axi_id mimux write id, read only
19:16	RO	0x0	sw_raw3_wr_axi_id mipi raw3 tx id, read only
15:12	RO	0x0	sw_raw2_wr_axi_id mipi raw2 tx id, read only
11:8	RO	0x0	sw_raw1_wr_axi_id mipi raw1 tx id, read only
7:4	RO	0x0	sw_raw0_wr_axi_id mipi raw0 tx id, read only
3:0	RO	0x0	reserved

MI_1400_MI_RD_CTRL2

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_rd2_burst_dis 1'b0: self-adaption enable 1'b1: self-adaption disable
30	RW	0x0	sw_raw_rd_old old-mi read. 0: disable; 1: enable;
29:22	RO	0x0	reserved
21:20	RW	0x2	sw_raw_wr_burst_len Burst length for raw data affecting DMA write port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
19:18	RW	0x1	sw_bay3d_rd_burst_len Burst length for bay3d data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
17:16	RW	0x1	sw_lut_rd_burst_len Burst length for lut data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15:14	RW	0x0	sw_dbr_rd_burst_len Burst length for mimux read data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported.

13:12	RW	0x0	sw_raws_rd_burst_len Burst length for raw2 rx data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported.
11:10	RW	0x0	sw_raw1_rd_burst_len Burst length for raw1 rx data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported.
9:8	RW	0x0	sw_raw0_rd_burst_len Burst length for raw0 rx data affecting DMA read port. 2'b00: 16-beat bursts 2'b01: 2-beat bursts 2'b10: 4-beat bursts 2'b11: 8-beat bursts Ignored if 8- or 16-beat bursts are not supported.
7:5	RO	0x0	reserved
4	RW	0x0	sw_bay3d_rw_one_addr_en ddr address of mimux read is the same to bay3d write
3	RW	0x0	sw_dbr_rw_one_addr_en ddr address of mimux read is the same to mimux write
2	RW	0x0	sw_raws_rw_one_addr_en ddr address of raw2 rx is the same to raw2 tx
1	RW	0x0	sw_raw1_rw_one_addr_en ddr address of raw1 rx is the same to raw1 tx
0	RW	0x0	sw_raw0_rw_one_addr_en ddr address of raw0 rx is the same to raw0 tx

MI_1400_MI_RD_ID

Address: Operational Base + offset (0x040c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RO	0x0	sw_bay3d_rd_axi_id bay3d read id, read only
19:16	RO	0x0	sw_lut_rd_axi_id mipi lut read id, read only
15:12	RO	0x0	sw_dbr_rd_axi_id mipi mimux read id, read only
11:8	RO	0x0	sw_raws_rd_axi_id mipi raw2 rx id, read only
7:4	RO	0x0	sw_raw1_rd_axi_id mipi raw1 rx id, read only
3:0	RO	0x0	sw_raw0_rd_axi_id mipi raw0 rx id, read only

MI_1400_MI_RD_FIFO_LEVEL

Address: Operational Base + offset (0x041c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_lut_rd_level lut read fifo level for generating hurry signal
23:18	RW	0x00	sw_dbr_rd_level mimux read fifo level for generating hurry signal
17:12	RW	0x00	sw_raws_rd_level raw2 rx fifo level for generating hurry signal
11:6	RW	0x00	sw_raw1_rd_level raw1 rx fifo level for generating hurry signal
5	RO	0x0	reserved
4:0	RW	0x00	sw_raw0_rd_level raw0 rx fifo level for generating hurry signal

MI_1400_RAW0_WR_BASE

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw0_wr_base Base address of raw0 tx data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW0_WR_BASE --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(RAW0_WR_BASE, address_value) is equivalent to write(RAW0_WR_BASE, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if camerIC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured . Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW0_WR_SIZE

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_raw0_wr_size Size of raw0 data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW0_WR_SIZE --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW0_WR_LENGTH

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_raw0_wr_length Line length of raw0 tx in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.
3:0	RO	0x0	reserved

MI_1400_RAW0_WR_BASE_SHD

Address: Operational Base + offset (0x042c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw0_wr_base_shd Base address of raw0 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_RAW1_WR_BASE

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw1_wr_base Base address of raw1 tx data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW1_WR_BASE --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(RAW1_WR_BASE, address_value) is equivalent to write(RAW1_WR_BASE, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if camerIC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured . Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW1_WR_SIZE

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_raw1_wr_size Size of raw1 data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW1_WR_SIZE --- Note: This register protects from non-aligned access. Refer to RAW1_WR_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW1_WR_LENGTH

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_raw1_wr_length Line length of raw1 tx in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.
3:0	RO	0x0	reserved

MI_1400_RAW1_WR_BASE_SHD

Address: Operational Base + offset (0x043c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	raw1_wr_base_shd Base address of raw1 tx data ring buffer. --- RAW1_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW1_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_RAW2_WR_BASE

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw2_wr_base base address of raw1 tx data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW2_WR_BASE --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(RAW2_WR_BASE, address_value) is equivalent to write(RAW2_WR_BASE, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if camerIC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW2_WR_SIZE

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_raw2_wr_size Size of raw2 data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW2_WR_SIZE --- Note: This register protects from non-aligned access. Refer to RAW2_WR_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW2_WR_LENGTH

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_raw2_wr_length Line length of raw2 tx in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.
3:0	RO	0x0	reserved

MI_1400_RAW2_WR_BASE_SHD

Address: Operational Base + offset (0x044c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	raw2_wr_base_shd Base address of raw2 tx data ring buffer. --- RAW2_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW2_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_RAW3_WR_BASE

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw3_wr_base base address of raw1 tx data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW3_WR_BASE --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(RAW3_WR_BASE, address_value) is equivalent to write(RAW3_WR_BASE, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if camerIC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW3_WR_SIZE

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_raw3_wr_size Size of raw3 data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. --- RAW3_WR_SIZE --- Note: This register protects from non-aligned access. Refer to RAW3_WR_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_RAW3_WR_LENGTH

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_raw3_wr_length Line length of raw3 tx in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.
3:0	RO	0x0	reserved

MI_1400_RAW3_WR_BASE_SHD

Address: Operational Base + offset (0x045c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	raw3_wr_base_shd Base address of raw3 tx data ring buffer. --- RAW3_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW3_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_RW0_WR_LAST_FRAME_ADDR

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	stat_raw0_last_frame_waddr The last write ddr address of raw0 at frame end
3:0	RO	0x0	reserved

MI_1400_RW1_WR_LAST_FRAME_ADDR

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	stat_raw1_last_frame_waddr The last write ddr address of raw1 at frame end
3:0	RO	0x0	reserved

MI_1400_RW2_WR_LAST_FRAME_ADDR

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	stat_raw2_last_frame_waddr The last write ddr address of raw2 at frame end
3:0	RO	0x0	reserved

MI_1400_RW3_WR_LAST_FRAME_ADDR

Address: Operational Base + offset (0x046c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	stat_raw3_last_frame_waddr The last write ddr address of raw3 at frame end
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_BASE

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw0_rd_base Base address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_LENGTH

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_raw0_rd_length Line length of raw0 rx in pixel, also known as line stride.

MI_1400_RAW0_RD_BASE_SHD

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw0_rd_base_shd Base shadow address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_BASE

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw1_rd_base Base address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_LENGTH

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_raw1_rd_length Line length of raw1 rx in pixel, also known as line stride.

MI_1400_RAW1_RD_BASE_SHD

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw1_rd_base_shd Base shadow address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_BASE

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base Base address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_LENGTH

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_raws_rd_length Line length of raws rx in pixel, also known as line stride.

MI_1400_RAWS_RD_BASE_SHD

Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base_shd Base shadow address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_3D_RD_BASE

Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_3dlut_rd_base Base address of 3d lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LSC_RD_BASE

Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_lsclut_rd_base Base address of lsc lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LDCH_RD_BASE

Address: Operational Base + offset (0x0548)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_ldch_rd_base Base address of ldch lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_3D_RD_WSIZE

Address: Operational Base + offset (0x0550)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x2d9	sw_3d_lut_wsize 3d lut actual size, word unit

MI_1400_LUT_LSC_RD_WSIZE

Address: Operational Base + offset (0x0554)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_lsc_lut_wsize lsc lut actual size, word unit

MI_1400_LUT_LDCH_RD_H_WSIZE

Address: Operational Base + offset (0x0558)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_ldch_lut_h_wsize ldch lut h size, word unit (((pic_width+15)/16+1)+1)/2

MI_1400_LUT_LDCH_RD_V_SIZE

Address: Operational Base + offset (0x055c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_ldch_lut_v_size ldch lut v size (pic_height+7)/8+1

MI_1400_DBR_WR_BASE

Address: Operational Base + offset (0x0560)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_dbr_wr_base Base address of mimux write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_WR_SIZE

Address: Operational Base + offset (0x0564)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_dbr_wr_size Size of mimux write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_WR_LENGTH

Address: Operational Base + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:4	RW	0x000	sw_dbr_wr_length Line length of mimux write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_DBR_WR_BASE_SHD

Address: Operational Base + offset (0x056c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	dbr_wr_base_shd Base address of mimux wirte data ring buffer. --- DBR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to DBR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_DBR_RD_BASE

Address: Operational Base + offset (0x0570)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_dbr_rd_base Base address of mimux read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_DBR_RD_LENGTH

Address: Operational Base + offset (0x0574)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	sw_dbr_rd_length Line length of mimux read in pixel, also known as line stride.

MI_1400_DBR_RD_BASE_SHD

Address: Operational Base + offset (0x0578)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	dbr_rd_base_shd Base shadow address of mimux read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_SWS_3A_WR_BASE

Address: Operational Base + offset (0x057c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sws_3a_wr_base Base shadow address of mimux read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_SIZE

Address: Operational Base + offset (0x0584)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_gain_wr_size Size of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_LENGTH

Address: Operational Base + offset (0x0588)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_gain_wr_length Line length of gain write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE2

Address: Operational Base + offset (0x058c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base2 Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE_SHD

Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	gain_wr_base_shd Base address of gain wirte data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to GAIN_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_WR_BASE

Address: Operational Base + offset (0x05a0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_wr_base Base address of bayer 3dnr write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_WR_SIZE

Address: Operational Base + offset (0x05a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_wr_size Size of bayer 3dnr write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_WR_LENGTH

Address: Operational Base + offset (0x05a8)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:4	RW	0x000	sw_bay3d_wr_length Line length of bayer 3dnr write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_WR_BASE_SHD

Address: Operational Base + offset (0x05ac)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_wr_base_shd Base address of bayer 3dnr wirte data ring buffer. --- BAY3D_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_RD_BASE

Address: Operational Base + offset (0x05b0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_rd_base Base address of bayer 3dnr read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_RD_LENGTH

Address: Operational Base + offset (0x05b4)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_bay3d_rd_length Line length of bayer 3dnr read in pixel, also known as line stride.

MI_1400_BAY3D_RD_BASE_SHD

Address: Operational Base + offset (0x05b8)

Bit	Attr	Reset Value	Description
31:4	R/WSC	0x0000000	bay3d_rd_base_shd Base shadow address of bayer 3dnr read data ring buffer.
3:0	RO	0x0	reserved

12.4.2.3 BLC

ISP_BLS_3000_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_bls1_en bls1 module after bay-nr: 1: Black level subtraction is enabled 0: Bypass the black level processing
3:2	RW	0x0	sw_bls_win_en 0: No measuring is performed 1: Only window 1 is measured 2: Only window 2 is measured 3: Both windows are measured
1	RW	0x0	sw_bls_mode 1: Subtract measured values 0: Subtract fixed values
0	RW	0x0	sw_bls_en 1: Black level subtraction is enabled 0: Bypass the black level processing

ISP_BLS_3000_SAMPLES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	BLS_SAMPLES This number to the power of two gives the number of measure samples for each Bayer position. Range 0x00: 2^0=1 to 0x12: 2^18=262144. This number is also the divider for the accumulator for each Bayer position. The accumulation will be stopped, if the number of measured pixels for the current Bayer position is equal to the number of samples. The measure windows must be positioned that way that the number of included pixels of each Bayer position included by both windows is equal or greater than the number of measure samples calculated by 2^BLS_SAMPLES. NOTE: The number of pixels of one Bayer position is 1/4 of the number of all Pixels included by the measure windows.

ISP_BLS_3000_H1_START

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_H1_START Black pixel window 1 horizontal start position

ISP_BLS_3000_H1_STOP

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_H1_STOP Black pixel window 1 horizontal stop position

ISP_BLS_3000_V1_START

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_V1_START Black pixel window 1 vertical start position

ISP_BLS_3000_V1_STOP

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_V1_STOP Black pixel window 1 vertical stop position

ISP_BLS_3000_H2_START

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_H2_START Black pixel window 2 horizontal start position

ISP_BLS_3000_H2_STOP

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_H2_STOP Black pixel window 2 horizontal stop position

ISP_BLS_3000_V2_START

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_V2_START Black pixel window 2 vertical start position

ISP_BLS_3000_V2_STOP

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	BLS_V2_STOP Black pixel window 2 vertical stop position

ISP_BLS_3000_A_FIXED

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	BLS_A_FIXED Fixed black level for A pixels C signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values

ISP_BLS_3000_B_FIXED

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	BLS_B_FIXED Fixed black level for B pixels C signed two's complement, value range from -4096 to +4095

ISP_BLS_3000_C_FIXED

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	BLS_C_FIXED Fixed black level for C pixels C signed two's complement, value range from -4096 to +4095

ISP_BLS_3000_D_FIXED

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	BLS_D_FIXED Fixed black level for D pixels - signed two's complement, value range from -4096 to +4095

ISP_BLS_3000_A_MEASURED

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	BLS_A_MEASURED Measured black level for A pixels

ISP_BLS_3000_B_MEASURED

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	BLS_B_MEASURED Measured black level for B pixels

ISP_BLS_3000_C_MEASURED

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	BLS_C_MEASURED Measured black level for C pixels

ISP_BLS_3000_D_MEASURED

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	BLS_D_MEASURED Measured black level for D pixels

ISP_BLS_3000_BLS1_A_FIXED

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_bls1_a_fixed Fixed black level for A pixels C signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values

ISP_BLS_3000_BLS1_B_FIXED

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_b_fixed Fixed black level for B pixels C signed two's complement, value range from -4096 to +4095

ISP_BLS_3000_BLS1_C_FIXED

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:1	RW	0x0000	sw_bls1_c_fixed Fixed black level for C pixels C signed two's complement, value range from -4096 to +4095
0	RO	0x0	reserved

ISP_BLS_3000_BLS1_D_FIXED

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_d_fixed Fixed black level for D pixels - signed two's complement, value range from -4096 to +4095

12.4.2.4 DPCC

ISP_DPCC_3400_MODE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dpcc_working
29:3	RO	0x0000000	reserved
2	RW	0x1	STAGE1_ENABLE 1'b1: Enable stage1 *Default* 1'b0: Bypass stage1
1	RW	0x0	GRAYSCALE_MODE 1'b1: Enable gray scale data input from black and white sensors (without color filter array) 1'b0: BAYER DATA INPUT *Default*
0	RW	0x0	ISP_DPCC_enable 1'b1: Enable DPCC 1'b0: Bypass DPCC *Default*

ISP_DPCC_3400_OUTPUT_MODE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:5	RW	0x0	sw_rk_out_sel 2'b00: RK method1 2'b01: RK method2 2'b10: RK method3 2'b11: Reserved
4	RW	0x0	sw_dpcc_output_sel 1'b0: Select median mode 1'b1: Select rk output mode
3	RW	0x0	STAGE1_RB_3x3 1'b1: Stage1 red/blue 9 pixel (3x3) output median 1'b0: Stage1 red/blue 4 or 5 pixel output median *Default*
2	RW	0x0	STAGE1_G_3x3 1'b1: Stage1 green 9 pixel (3x3) output median 1'b0: Stage1 green 4 or 5 pixel output median *Default*
1	RW	0x1	STAGE1_INCL_RB_CENTER 1'b1: Stage1 include center pixel for red/blue output median 2x2+1 *Default* 1'b0: Stage1 do not include center pixel for red/blue output median 2x2
0	RW	0x1	STAGE1_INCL_GREEN_CENTER 1'b1: Stage1 include center pixel for green output median 2x2+1 *Default* 1'b0: Stage1 do not include center pixel for green output median 2x2

ISP_DPCC_3400_SET_USE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	STAGE1_USE_FIX_SET 1'b1: Stage1 use hard coded methods set *Default* 1'b0: Stage1 do not use hard coded methods set
2	RW	0x1	STAGE1_USE_SET_3 1'b1: Stage1 use methods set 3 1'b0: Stage1 do not use methods set 3 *Default*

Bit	Attr	Reset Value	Description
1	RW	0x1	STAGE1_USE_SET_2 1'b1: Stage1 use methods set 2 1'b0: Stage1 do not use methods set 2 *Default*
0	RW	0x1	STAGE1_USE_SET_1 1'b1: Stage1 use methods set 1 *Default* 1'b0: Stage1 do not use methods set 1 --- ISP_DPCC_SET_USE --- Note: Methods sets can be used in parallel for each stage and the result is the logical OR of all selected sets.

ISP_DPCC_3400_METHODS_SET_1

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_rk_red_blue1_en 1'b1: Enable RK method check for green *Default* 1'b0: Bypass RK method check for green
12	RW	0x1	RG_RED_BLUE1_ENABLE 1'b1: Enable Rank Gradient check for red_blue *Default* 1'b0: Bypass Rank Gradient check for red_blue
11	RW	0x1	RND_RED_BLUE1_ENABLE 1'b1: Enable Rank Neighbor Difference check for red_blue *Default* 1'b0: Bypass Rank Neighbor Difference check for red_blue
10	RW	0x1	RO_RED_BLUE1_ENABLE 1'b1: Enable Rank Order check for red_blue *Default* 1'b0: Bypass Rank Order check for red_blue
9	RW	0x0	LC_RED_BLUE1_ENABLE 1'b1: Enable Line check for red_blue *Default* 1'b0: Bypass Line check for red_blue
8	RW	0x1	PG_RED_BLUE1_ENABLE 1'b1: Enable Peak Gradient check for red_blue *Default* 1'b0: Bypass Peak Gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_rk_green1_en 1'b1: Enable RK method check for green *Default* 1'b0: Bypass RK method check for green
4	RW	0x1	RG_GREEN1_ENABLE 1'b1: Enable Rank Gradient check for green *Default* 1'b0: Bypass Rank Gradient check for green
3	RW	0x1	RND_GREEN1_ENABLE 1'b1: Enable Rank Neighbor Difference check for green *Default* 1'b0: Bypass Rank Neighbor Difference check for green
2	RW	0x1	RO_GREEN1_ENABLE 1'b1: Enable Rank Order check for green *Default* 1'b0: Bypass Rank Order check for green
1	RW	0x0	LC_GREEN1_ENABLE 1'b1: Enable Line check for green *Default* 1'b0: Bypass Line check for green
0	RW	0x1	PG_GREEN1_ENABLE 1'b1: Enable Peak Gradient check for green *Default* 1'b0: Bypass Peak Gradient check for green --- ISP_DPCC_METHODS_SET_1 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods.

ISP_DPCC_3400_METHODS_SET_2

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_rk_red_blue2_en 1'b1: Enable RK method check for green 1'b0: Bypass RK method check for green *Default*
12	RW	0x0	RG_RED_BLUE2_ENABLE 1'b1: Enable Rank Gradient check for red_blue *Default* 1'b0: Bypass Rank Gradient check for red_blue
11	RW	0x0	RND_RED_BLUE2_ENABLE 1'b1: Enable Rank Neighbor Difference check for red_blue *Default* 1'b0: Bypass Rank Neighbor Difference check for red_blue
10	RW	0x1	RO_RED_BLUE2_ENABLE 1'b1: Enable Rank Order check for red_blue *Default* 1'b0: Bypass Rank Order check for red_blue
9	RW	0x1	LC_RED_BLUE2_ENABLE 1'b1: Enable Line check for red_blue 1'b0: Bypass Line check for red_blue *Default*
8	RW	0x1	PG_RED_BLUE2_ENABLE 1'b1: Enable Peak Gradient check for red_blue *Default* 1'b0: Bypass Peak Gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_rk_green2_en 1'b1: Enable RK method check for green 1'b0: Bypass RK method check for green *Default*
4	RW	0x0	RG_GREEN2_ENABLE 1'b1: Enable Rank Gradient check for green *Default* 1'b0: Bypass Rank Gradient check for green
3	RW	0x0	RND_GREEN2_ENABLE 1'b1: Enable Rank Neighbor Difference check for green *Default* 1'b0: Bypass Rank Neighbor Difference check for green
2	RW	0x1	RO_GREEN2_ENABLE 1'b1: Enable Rank Order check for green *Default* 1'b0: Bypass Rank Order check for green
1	RW	0x1	LC_GREEN2_ENABLE 1'b1: Enable Line check for green 1'b0: Bypass Line check for green *Default*
0	RW	0x1	PG_GREEN2_ENABLE 1'b1: Enable Peak Gradient check for green *Default* 1'b0: Bypass Peak Gradient check for green --- ISP_DPCC_METHODS_SET_2 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods.

ISP_DPCC_3400_METHODS_SET_3

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	sw_rk_red_blue3_en 1'b1: Enable RK method check for green 1'b0: Bypass RK method check for green *Default*

Bit	Attr	Reset Value	Description
12	RW	0x1	RG_RED_BLUE3_ENABLE 1'b1: Enable Rank Gradient check for red_blue 1'b0: Bypass Rank Gradient check for red_blue *Default*
11	RW	0x1	RND_RED_BLUE3_ENABLE 1'b1: Enable Rank Neighbor Difference check for red_blue 1'b0: Bypass Rank Neighbor Difference check for red_blue *Default*
10	RW	0x1	RO_RED_BLUE3_ENABLE 1'b1: Enable Rank Order check for red_blue *Default* 1'b0: Bypass Rank Order check for red_blue
9	RW	0x1	LC_RED_BLUE3_ENABLE 1'b1: Enable Line check for red_blue *Default* 1'b0: Bypass Line check for red_blue
8	RW	0x1	PG_RED_BLUE3_ENABLE 1'b1: Enable Peak Gradient check for red_blue *Default* 1'b0: Bypass Peak Gradient check for red_blue
7:6	RO	0x0	reserved
5	RW	0x0	sw_rk_green3_en 1'b1: Enable RK method check for green 1'b0: Bypass RK method check for green *Default*
4	RW	0x1	RG_GREEN3_ENABLE 1'b1: Enable Rank Gradient check for green 1'b0: Bypass Rank Gradient check for green *Default*
3	RW	0x1	RND_GREEN3_ENABLE 1'b1: Enable Rank Neighbor Difference check for green 1'b0: Bypass Rank Neighbor Difference check for green *Default*
2	RW	0x1	RO_GREEN3_ENABLE 1'b1: Enable Rank Order check for green *Default* 1'b0: Bypass Rank Order check for green
1	RW	0x1	LC_GREEN3_ENABLE 1'b1: Enable Line check for green *Default* 1'b0: Bypass Line check for green
0	RW	0x1	PG_GREEN3_ENABLE 1'b1: Enable Peak Gradient check for green *Default* 1'b0: Bypass Peak Gradient check for green --- ISP_DPCC_METHODS_SET_3 --- Note: Different methods can be used in parallel, the result is the logical AND of all selected methods.

ISP_DPCC_3400_LINE_THRESH_1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis1_rb Min distance for set 1 red /blue
23:16	RW	0x00	sw_mindis1_g Min distance for set 1 green
15:8	RW	0x08	LINE_THR_1_RB Line threshold for set 1 red/blue
7:0	RW	0x08	LINE_THR_1_G Line threshold for set 1 green --- ISP_DPCC_LINE_THRESH_1 --- Note: All values are unsigned integer.

ISP_DPCC_3400_LINE_MAD_FAC_1

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min1
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max1
15:14	RO	0x0	reserved
13:8	RW	0x04	LINE_MAD_FAC_1_RB Line MAD factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	LINE_MAD_FAC_1_G Line MAD factor for set 1 green --- ISP_DPCC_LINE_MAD_FAC_1 --- Note: All values are unsigned integer.

ISP_DPCC_3400_PG_FAC_1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	PG_FAC_1_RB Peak gradient factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	PG_FAC_1_G Peak gradient factor for set 1 green --- ISP_DPCC_PG_FAC_1 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RND_THRESH_1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0a	RND_THR_1_RB Rank Neighbor Difference threshold for set 1 red/blue
7:0	RW	0x0a	RND_THR_1_G Rank Neighbor Difference threshold for set 1 green --- ISP_DPCC_RND_THRESH_1 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RG_FAC_1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x20	RG_FAC_1_RB Rank gradient factor for set 1 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x20	RG_FAC_1_G Rank gradient factor for set 1 green --- ISP_DPCC_RG_FAC_1 --- Note: All values are unsigned integer.

ISP_DPCC_3400_LINE_THRESH_2

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis2_rb Min distance for set 2 red /blue

Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_mindis2_g Min distance for set 2 green
15:8	RW	0x10	LINE_THR_2_RB Line threshold for set 2 red/blue
7:0	RW	0x0c	LINE_THR_2_G Line threshold for set 2 green --- ISP_DPCC_LINE_THRESH_2 --- Note: All values are unsigned integer.

ISP_DPCC_3400_LINE_MAD_FAC_2

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min2
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max2
15:14	RO	0x0	reserved
13:8	RW	0x18	LINE_MAD_FAC_2_RB Line MAD factor for set 2 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x10	LINE_MAD_FAC_2_G Line MAD factor for set 2 green --- ISP_DPCC_LINE_MAD_FAC_2 --- Note: All values are unsigned integer.

ISP_DPCC_3400_PG_FAC_2

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	PG_FAC_2_RB Peak gradient factor for set 2 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	PG_FAC_2_G Peak gradient factor for set 2 green --- ISP_DPCC_PG_FAC_2 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RND_THRESH_2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x08	RND_THR_2_RB Rank Neighbor Difference threshold for set 2 red/blue
7:0	RW	0x08	RND_THR_2_G Rank Neighbor Difference threshold for set 2 green --- ISP_DPCC_RND_THRESH_2 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RG_FAC_2

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x08	RG_FAC_2_RB Rank gradient factor for set 2 red/blue

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:0	RW	0x08	RG_FAC_2_G Rank gradient factor for set 2 green --- ISP_DPCC_RG_FAC_2 --- Note: All values are unsigned integer.

ISP_DPCC_3400_LINE_THRESH_3

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_mindis3_rb Min distance for set 3 red /blue
23:16	RW	0x00	sw_mindis3_g Min distance for set 3 green
15:8	RW	0x20	LINE_THR_3_RB Line threshold for set 3 red/blue
7:0	RW	0x20	LINE_THR_3_G Line threshold for set 3 green --- ISP_DPCC_LINE_THRESH_3 --- Note: All values are unsigned integer.

ISP_DPCC_3400_LINE_MAD_FAC_3

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dis_scale_min3
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dis_scale_max3
15:14	RO	0x0	reserved
13:8	RW	0x04	LINE_MAD_FAC_3_RB Line MAD factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	LINE_MAD_FAC_3_G Line MAD factor for set 3 green --- ISP_DPCC_LINE_MAD_FAC_3 --- Note: All values are unsigned integer.

ISP_DPCC_3400_PG_FAC_3

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	PG_FAC_3_RB Peak gradient factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x03	PG_FAC_3_G Peak gradient factor for set 3 green --- ISP_DPCC_PG_FAC_3 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RND_THRESH_3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x08	RND_THR_3_RB Rank Neighbor Difference threshold for set 3 red/blue

Bit	Attr	Reset Value	Description
7:0	RW	0x06	RND_THR_3_G Rank Neighbor Difference threshold for set 3 green --- ISP_DPCC_RND_THRESH_3 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RG_FAC_3

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	RG_FAC_3_RB Rank gradient factor for set 3 red/blue
7:6	RO	0x0	reserved
5:0	RW	0x04	RG_FAC_3_G Rank gradient factor for set 3 green --- ISP_DPCC_RG_FAC_3 --- Note: All values are unsigned integer.

ISP_DPCC_3400_RO_LIMITS

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:10	RW	0x2	RO_LIM_3_RB Rank order limit for set 3 red/blue
9:8	RW	0x2	RO_LIM_3_G Rank order limit for set 3 green
7:6	RW	0x0	RO_LIM_2_RB Rank order limit for set 2 red/blue
5:4	RW	0x0	RO_LIM_2_G Rank order limit for set 2 green
3:2	RW	0x2	RO_LIM_1_RB Rank order limit for set 1 red/blue
1:0	RW	0x2	RO_LIM_1_G Rank order limit for set 1 green --- ISP_DPCC_RO_LIMITS --- Note: All values are unsigned integer.

ISP_DPCC_3400_RND_OFFS

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:10	RW	0x3	RND_OFFS_3_RB Rank Offset to Neighbor for set 3 red/blue
9:8	RW	0x3	RND_OFFS_3_G Rank Offset to Neighbor for set 3 green
7:6	RW	0x3	RND_OFFS_2_RB Rank Offset to Neighbor for set 2 red/blue
5:4	RW	0x3	RND_OFFS_2_G Rank Offset to Neighbor for set 2 green
3:2	RW	0x3	RND_OFFS_1_RB Rank Offset to Neighbor for set 1 red/blue
1:0	RW	0x3	RND_OFFS_1_G Rank Offset to Neighbor for set 1 green --- ISP_DPCC_RND_OFFS --- Note: All values are unsigned integer.

ISP_DPCC_3400_BPT_CTRL

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	BPT_RB_3x3 1'b1: If BPT active red/blue 9 pixel (3x3) output median 1'b0: If BPT active red/blue 4 or 5 pixel output median *Default*
10	RW	0x0	BPT_G_3x3 1'b1: If BPT active green 9 pixel (3x3) output median 1'b0: If BPT active green 4 or 5 pixel output median *Default*
9	RW	0x0	BPT_INCL_RB_CENTER 1'b1: If BPT active include center pixel for red/blue output median 2x2+1 1'b0: If BPT active do not include center pixel for red/blue output median 2x2
8	RW	0x0	BPT_INCL_GREEN_CENTER 1'b1: If BPT active include center pixel for green output median 2x2+1 1'b0: If BPT active do not include center pixel for green output median 2x2
7	RW	0x0	BPT_USE_FIX_SET 1'b1: For BPT write use hard coded methods set 1'b0: For BPT write do not use hard coded methods set *Default*
6	RW	0x0	BPT_USE_SET_3 1'b1: For BPT write use methods set 3 1'b0: For BPT write do not use methods set 3 *Default*
5	RW	0x0	BPT_USE_SET_2 1'b1: For BPT write use methods set 2 1'b0: For BPT write do not use methods set 2 *Default*
4	RW	0x0	BPT_USE_SET_1 1'b1: For BPT write use methods set 1 1'b0: For BPT write do not use methods set 1 *Default*
3:2	RO	0x0	reserved
1	RW	0x0	bpt_cor_en Table based correction enable 1'b1: Table based correction is enabled; 1'b0: Table based correction is disabled.
0	RW	0x0	bpt_det_en Bad pixel detection write enable 1'b1: Bad pixel detection write to memory is enabled; 1'b0: Bad pixel detection write to memory is disabled. --- ISP_DPCC_BPT_CTRL --- Note: This register controls the behaviour of the table based bad pixel correction module. It can be switched on and off independently of the DPCC detection and correction block. Different correction algorithms for the table based correction are available and are defined by this register. The default setting after reset enables a correction algorithm with most accurate correlation to surrounding pixels. Detection for the table based correction can be configured independently from the on-the-fly DPCC detection scheme.

ISP_DPCC_3400_BPT_NUMBER

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	bp_number Number of current Bad Pixel entries in bad pixel table (BPT) --- ISP_DPCC_BPT_NUMBER --- Note: Bit width of bp_number depends on size of BP RAM which is defined during chip synthesis.

ISP_DPCC_3400_BPT_ADDR

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	bp_table_addr Table RAM start address for read or write operations. The address counter is incremented at each read or write access to the data register (auto-increment mechanism). --- ISP_DPCC_BPT_ADDR --- Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh.

ISP_DPCC_3400_BPT_DATA

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	bpt_v_addr Bad Pixel vertical address (pixel position)
15:13	RO	0x0	reserved
12:0	RW	0x0000	bpt_h_addr Bad Pixel horizontal address (pixel position) --- ISP_DPCC_BPT_DATA --- Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh. The programmed table value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits).

ISP_DPCC_3400_BP_CNT

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x000000	bp_cnt Number of current Bad Pixel Cnt

ISP_DPCC_3400_PDAF_EN

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_en 1'b1: Open pdaf point replace 1'b0: Close all pdaf points replace

ISP_DPCC_3400_PDAF_POINT_EN

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sw_pdaf_point15_en 1'b1: Open point15 replace 1'b0: Close point15 replace
14	RW	0x0	sw_pdaf_point14_en 1'b1: Open point14 replace 1'b0: Close point14 replace
13	RW	0x0	sw_pdaf_point13_en 1'b1: Open point13 replace 1'b0: Close point13 replace
12	RW	0x0	sw_pdaf_point12_en 1'b1: Open point12 replace 1'b0: Close point12 replace
11	RW	0x0	sw_pdaf_point11_en 1'b1: Open point11 replace 1'b0: Close point11 replace
10	RW	0x0	sw_pdaf_point10_en 1'b1: Open point10 replace 1'b0: Close point10 replace
9	RW	0x0	sw_pdaf_point9_en 1'b1: Open point9 replace 1'b0: Close point9 replace
8	RW	0x0	sw_pdaf_point8_en 1'b1: Open point8 replace 1'b0: Close point8 replace
7	RW	0x0	sw_pdaf_point7_en 1'b1: Open point7 replace 1'b0: Close point7 replace
6	RW	0x0	sw_pdaf_point6_en 1'b1: Open point6 replace 1'b0: Close point6 replace
5	RW	0x0	sw_pdaf_point5_en 1'b1: Open point5 replace 1'b0: Close point5 replace
4	RW	0x0	sw_pdaf_point4_en 1'b1: Open point4 replace 1'b0: Close point4 replace
3	RW	0x0	sw_pdaf_point3_en 1'b1: Open point3 replace 1'b0: Close point3 replace
2	RW	0x0	sw_pdaf_point2_en 1'b1: Open point2 replace 1'b0: Close point2 replace
1	RW	0x0	sw_pdaf_point1_en 1'b1: Open point1 replace 1'b0: Close point1 replace
0	RW	0x0	sw_pdaf_point0_en 1'b1: Open point0 replace 1'b0: Close point0 replace

ISP_DPCC_3400_PDAF_OFFSET

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_pdaf_offsety The beginning y coordinate of pdaf pattern
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_pdaf_offsetx The beginning x coordinate of pdaf pattern

ISP_DPCC_3400_PDAF_WRAP

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_pdaf_wrapy The height of pattren , 0x00 is 1, 0x0f is 16.
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_pdaf_wrapx The width of pattren , 0x00 is 1, 0x0f is 16.

ISP_DPCC_3400_PDAF_SCOPE

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_pdaf_wrapy_num The num of wrapy
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_pdaf_wrapx_num The num of wrapx

ISP_DPCC_3400_PDAF_POINT_0

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point1_y point1 y cordinate
23:16	RW	0x00	sw_pdaf_point1_x point1 x cordinate
15:8	RW	0x00	sw_pdaf_point0_y point0 y cordinate
7:0	RW	0x00	sw_pdaf_point0_x point0 x cordinate

ISP_DPCC_3400_PDAF_POINT_1

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point3_y point3 y cordinate
23:16	RW	0x00	sw_pdaf_point3_x point3 x cordinate
15:8	RW	0x00	sw_pdaf_point2_y point2 y cordinate
7:0	RW	0x00	sw_pdaf_point2_x point2 x cordinate

ISP_DPCC_3400_PDAF_POINT_2

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point5_y point5 y cordinate
23:16	RW	0x00	sw_pdaf_point5_x point5 x cordinate
15:8	RW	0x00	sw_pdaf_point4_y point4 y cordinate
7:0	RW	0x00	sw_pdaf_point4_x point4 x cordinate

ISP_DPCC_3400_PDAF_POINT_3

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point7_y point7 y cordinate
23:16	RW	0x00	sw_pdaf_point7_x point7 x cordinate
15:8	RW	0x00	sw_pdaf_point6_y point6 y cordinate
7:0	RW	0x00	sw_pdaf_point6_x point6 x cordinate

ISP_DPCC_3400_PDAF_POINT_4

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point9_y point9 y cordinate
23:16	RW	0x00	sw_pdaf_point9_x point9 x cordinate
15:8	RW	0x00	sw_pdaf_point8_y point8 y cordinate
7:0	RW	0x00	sw_pdaf_point8_x point8 x cordinate

ISP_DPCC_3400_PDAF_POINT_5

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point11_y point11 y cordinate
23:16	RW	0x00	sw_pdaf_point11_x point11 x cordinate
15:8	RW	0x00	sw_pdaf_point10_y point10 y cordinate
7:0	RW	0x00	sw_pdaf_point10_x point10 x cordinate

ISP_DPCC_3400_PDAF_POINT_6

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point13_y point13 y cordinate
23:16	RW	0x00	sw_pdaf_point13_x point13 x cordinate
15:8	RW	0x00	sw_pdaf_point12_y point12 y cordinate

Bit	Attr	Reset Value	Description
7:0	RW	0x00	sw_pdaf_point12_x point12 x cordinate

ISP_DPCC_3400_PDAF_POINT_7

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point15_y point15 y cordinate
23:16	RW	0x00	sw_pdaf_point15_x point15 x cordinate
15:8	RW	0x00	sw_pdaf_point14_y point14 y cordinate
7:0	RW	0x00	sw_pdaf_point14_x point14 x cordinate

ISP_DPCC_3400_PDAF_FORWARD_MED

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_forward_med 1'b1: Selecet forward median value to replace pdaf point 1'b0: Selecet backward median value to replace pdaf point

12.4.2.5 HDRMGE

ISP_HDRMGE_3800_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_hdrmge_en_shd rkhdr enable shadow
30	RO	0x0	ro_hdrmge_working hdrmge working status
29:4	RO	0x0	reserved
3:2	RW	0x1	sw_hdrmge_mode 2'b00:Normal 2'b01:Framex2 2'b10:Framex3
1	RO	0x0	reserved
0	RW	0x0	sw_hdrmge_en_i rkhdr function enable

ISP_HDRMGE_3800_GAIN0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_hdrmge_gain0_inv 1/short -gain, [0,12]
15:14	RO	0x0	reserved
13:0	RW	0x0400	sw_hdrmge_gain0 short -gain, [8,6]

ISP_HDRMGE_3800_GAIN1

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x400	sw_hdrmge_gain1_inv 1/middle-gain, [0,12]
15:11	RO	0x0	reserved
10:0	RW	0x100	sw_hdrmge_gain1 middle-gain, [5,6]

ISP_HDRMGE_3800_GAIN2

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x40	sw_hdrmge_gain2 long -gain, [1,6]

ISP_HDRMGE_3800_CONS_DIFF

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_hdrmge_lm_dif_0p15 lm_0p15 for diff-offset of (M*gain1-frame and L*gain2*0p9 frame)/gain1 + 0p15;
23:16	RW	0xff	sw_hdrmge_lm_dif_0p9 lm_0p9 for diff-scale of (M*gain1-frame and L*gain2*0p9 frame)/gain1 + 0p15;
15:8	RW	0x00	sw_hdrmge_ms_diff_0p15 ms_0p15 for diff-offset of (S*gain0-frame and M*gain1*0p8 frame)/gain0 + 0p15;
7:0	RW	0xff	sw_hdrmge_ms_dif_0p8 ms_0p9 for diff-scale of (S*gain0-frame and M*gain1*0p8 frame)/gain0 + 0p15;

ISP_HDRMGE_3800_DIFF_Y0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_hdrmge_l1_y0 L-curve1 maskUseCur=D of Y0
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_hdrmge_l0_y0 L-curve0 maskUseCur=D of Y0

ISP_HDRMGE_3800_DIFF_Y1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x0c9	sw_hdrmge_l1_y1 L-curve1 maskUseCur=D of Y1
15:10	RO	0x0	reserved
9:0	RW	0x0c9	sw_hdrmge_l0_y1 L-curve0 maskUseCur=D of Y1

ISP_HDRMGE_3800_DIFF_Y2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x1fa	sw_hdrmge_l1_y2 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x1fa	sw_hdrmge_l0_y2 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y3

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x2c0	sw_hdrmge_l1_y3 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x2c0	sw_hdrmge_l0_y3 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y4

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x32f	sw_hdrmge_l1_y4 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x32f	sw_hdrmge_l0_y4 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y5

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x370	sw_hdrmge_l1_y5 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x370	sw_hdrmge_l0_y5 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y6

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x397	sw_hdrmge_l1_y6 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x397	sw_hdrmge_l0_y6 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y7

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3b1	sw_hdrmge_l1_y7 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3b1	sw_hdrmge_l0_y7 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y8

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3c2	sw_hdrmge_l1_y8 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3c2	sw_hdrmge_l0_y8 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y9

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3cf	sw_hdrmge_l1_y9 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3cf	sw_hdrmge_l0_y9 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y10

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3d8	sw_hdrmge_l1_y10 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3d8	sw_hdrmge_l0_y10 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y11

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3de	sw_hdrmge_l1_y11 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3de	sw_hdrmge_l0_y11 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y12

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3e4	sw_hdrmge_l1_y12 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3e4	sw_hdrmge_l0_y12 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y13

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3e8	sw_hdrmge_l1_y13 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3e8	sw_hdrmge_l0_y13 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y14

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3eb	sw_hdrmge_l1_y14 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3eb	sw_hdrmge_l0_y14 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y15

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3ee	sw_hdrmge_l1_y15 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3ee	sw_hdrmge_l0_y15 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y16

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3f0	sw_hdrmge_l1_y16 L-curve1 maskUseCur=D
15:10	RO	0x0	reserved
9:0	RW	0x3f0	sw_hdrmge_l0_y16 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_OVER_Y0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	sw_hdrmge_e_y0 E-curve over_exp_normal of Y-0

ISP_HDRMGE_3800_OVER_Y1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x001	sw_hdrmge_e_y1 E-curve over_exp_normal of Y-1

ISP_HDRMGE_3800_OVER_Y2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x004	sw_hdrmge_e_y2 E-curve over_exp_normal of Y-2

ISP_HDRMGE_3800_OVER_Y3

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x00e	sw_hdrmge_e_y3 E-curve over_exp_normal of Y-3

ISP_HDRMGE_3800_OVER_Y4

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x031	sw_hdrmge_e_y4 E-curve over_exp_normal of Y-4

ISP_HDRMGE_3800_OVER_Y5

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x098	sw_hdrmge_e_y5 E-curve over_exp_normal of Y-5

ISP_HDRMGE_3800_OVER_Y6

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x183	sw_hdrmge_e_y6 E-curve over_exp_normal of Y-6

ISP_HDRMGE_3800_OVER_Y7

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x2b7	sw_hdrmge_e_y7 E-curve over_exp_normal of Y-7

ISP_HDRMGE_3800_OVER_Y8

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x386	sw_hdrmge_e_y8 E-curve over_exp_normal of Y-8

ISP_HDRMGE_3800_OVER_Y9

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3da	sw_hdrmge_e_y9 E-curve over_exp_normal of Y-9

ISP_HDRMGE_3800_OVER_Y10

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3f5	sw_hdrmge_e_y10 E-curve over_exp_normal of Y-10

ISP_HDRMGE_3800_OVER_Y11

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3fd	sw_hdrmge_e_y11 E-curve over_exp_normal of Y-11

ISP_HDRMGE_3800_OVER_Y12

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_hdrmge_e_y12 E-curve over_exp_normal of Y-12

ISP_HDRMGE_3800_OVER_Y13

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_hdrmge_e_y13 E-curve over_exp_normal of Y-13

ISP_HDRMGE_3800_OVER_Y14

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_hdrmge_e_y14 E-curve over_exp_normal of Y-14

ISP_HDRMGE_3800_OVER_Y15

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_hdrmge_e_y15 E-curve over_exp_normal of Y-15

ISP_HDRMGE_3800_OVER_Y16

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_hdrmge_e_y16 E-curve over_exp_normal of Y-16

12.4.2.6 BAY2DNR

ISP_BAYNR_3A00_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_baynr_en_shd rawnr enable after shadow 0:disable 1:enable
30	RO	0x0	baynr_working working state of rawnr 0: shut down 1:working
29:9	RO	0x0	reserved
8	RW	0x1	sw_baynr_gauss_en 3x3 gauss filter enable range:0~1 default:0
7:5	RO	0x0	reserved
4	RW	0x0	sw_baynr_log_bypass log convert bypass enable signal HDR mode:0 NOT HDR mode:0~1 default:0
3:1	RO	0x0	reserved
0	RW	0x1	sw_baynr_en rawnr module enable signal range:0~1 default:1

ISP_BAYNR_3A00_DGAIN0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0471	sw_baynr_dgain1 rawnr dgain1 parameter range:0~0xffff
15:0	RW	0x4000	sw_baynr_dgain0 rawnr dgain0 parameter range:0~0xffff

ISP_BAYNR_3A00_DGAIN1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0400	sw_baynr_dgain2 rawnr dgain2 parameter range:0~0xffff

ISP_BAYNR_3A00_PIXDIFF

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x3fff	sw_baynr_pix_diff 5x5 pixel diffrence uper limit

ISP_BAYNR_3A00_THLD

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3ff	sw_baynr_diff_thld sumdiff threshold of filter parameter
15:10	RO	0x0	reserved
9:0	RW	0x00a	sw_baynr_softthld final threshold of filter parameter

ISP_BAYNR_3A00_W1_STRENG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a3	sw_bltflt_streng bialflter streng
15:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_baynr_reg_w1 channel weight of filter result

ISP_BAYNR_3A00_SIGMAX01

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x1210	sw_sigma_x1 sigma x value of segment 1
15:0	RW	0x1010	sw_sigma_x0 sigma x value of segment 0

ISP_BAYNR_3A00_SIGMAX23

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:16	RW	0x1610	sw_sigma_x3 sigma x value of segment 3
15:0	RW	0x1410	sw_sigma_x2 sigma x value of segment 2

ISP_BAYNR_3A00_SIGMAX45

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x1c10	sw_sigma_x5 sigma x value of segment 5
15:0	RW	0x1810	sw_sigma_x4 sigma x value of segment 4

ISP_BAYNR_3A00_SIGMAX67

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x2410	sw_sigma_x7 sigma x value of segment 7
15:0	RW	0x2010	sw_sigma_x6 sigma x value of segment 6

ISP_BAYNR_3A00_SIGMAX89

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x2c10	sw_sigma_x9 sigma x value of segment 9
15:0	RW	0x2810	sw_sigma_x8 sigma x value of segment 8

ISP_BAYNR_3A00_SIGMAX1011

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:16	RW	0x3410	sw_sigma_x11 sigma x value of segment 11
15:0	RW	0x3010	sw_sigma_x10 sigma x value of segment 10

ISP_BAYNR_3A00_SIGMAX1213

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x3a10	sw_sigma_x13 sigma x value of segment 13
15:0	RW	0x3810	sw_sigma_x12 sigma x value of segment 12

ISP_BAYNR_3A00_SIGMAX1415

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x4010	sw_sigma_x15 sigma x value of segment 15
15:0	RW	0x3c10	sw_sigma_x14 sigma x value of segment 14

ISP_BAYNR_3A00_SIGMAY01

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0300	sw_sigma_y1 sigma y value of segment 1
15:0	RW	0x0300	sw_sigma_y0 sigma y value of segment 0

ISP_BAYNR_3A00_SIGMAY23

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0300	sw_sigma_y3 sigma y value of segment 3
15:0	RW	0x0300	sw_sigma_y2 sigma y value of segment 2

ISP_BAYNR_3A00_SIGMAY45

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0280	sw_sigma_y5 sigma y value of segment 5
15:0	RW	0x0280	sw_sigma_y4 sigma y value of segment 4

ISP_BAYNR_3A00_SIGMAY67

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0280	sw_sigma_y7 sigma y value of segment 7
15:0	RW	0x0280	sw_sigma_y6 sigma y value of segment 6

ISP_BAYNR_3A00_SIGMAY89

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	sw_sigma_y9 sigma y value of segment 9
15:0	RW	0x0200	sw_sigma_y8 sigma y value of segment 8

ISP_BAYNR_3A00_SIGMAY1011

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	sw_sigma_y11 sigma y value of segment 11
15:0	RW	0x0200	sw_sigma_y10 sigma y value of segment 10

ISP_BAYNR_3A00_SIGMAY1213

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	sw_sigma_y13 sigma y value of segment 13
15:0	RW	0x0200	sw_sigma_y12 sigma y value of segment 12

ISP_BAYNR_3A00_SIGMAY1415

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0180	sw_sigma_x15 sigma y value of segment 15
15:0	RW	0x0200	sw_sigma_x14 sigma y value of segment 14

ISP_BAYNR_3A00_WRIT_D

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x31d	weit_d2 space weight of second line second colume pix in 5x5
19:10	RW	0x26d	weit_d1 space weight of first line third colume pix in 5x5
9:0	RW	0x178	weit_d0 space weight of first line fix colume pix in 5x5

12.4.2.7 BAY3DNR

BAY3D_BAY3D_CTRL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	WO	0x0	sys_itself_force_upd_sw_bay3d_bypass_en_shd sys_itself_force_upd write only sw_bay3d_bypass_en_shd read only
30	RO	0x0	sw_bay3d_en_shd bay3d en shadow
29	RO	0x0	sw_bay3d_pk_en_shd pk gain select shadow
28	RW	0x0	bay3d_working working
27	RW	0x0	sw_bay3d_exp_sel_shd exp curve lut select shadow
26:17	RO	0x0	reserved
16	RW	0x0	sw_bay3d_exp_sel exp curve lut select 1:fixed exp curve, wgt0 = exp1(dif2/153/153/4)*sw_bay3d_str 0:unfixed exp curve, wgt0 = exp0(dif2*sw_bay3d_exp_str)
15:13	RO	0x0	reserved
12	RW	0x0	sw_bay3d_bypass_en datapath bypass 1:bypass;0:nonbypass
11:5	RO	0x0	reserved
4	RW	0x1	sw_bay3d_pk_en pk gain select 1:local pk from ddr;0:global pk from sw_bay3d_glbpk2
3:1	RO	0x0	reserved
0	RW	0x0	sw_bay3d_en_i bay3d enable

BAY3D_BAY3D_KALRATIO

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x100	sw_bay3d_softwgt softthreshold weight
15:14	RO	0x0	reserved
13:0	RW	0x0100	sw_bay3d_sigratio sigma ratio

BAY3D_BAY3D_GLBPK2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000800	sw_bay3d_glbpk2 global pk square

BAY3D_BAY3D_KALSTR

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x100	sw_bay3d_exp_str exp_curve strength wgt0 = exp(dif2*sw_bay3d_exp_str)
15:9	RO	0x0	reserved
8:0	RW	0x100	sw_bay3d_str exp_curve strength wgt0 = exp(dif2/153/153/4)*sw_bay3d_str

BAY3D_BAY3D_WGTLMT

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x380	sw_bay3d_wgtlmt_h high freq wgt1 limit
15:10	RO	0x0	reserved
9:0	RW	0x380	sw_bay3d_wgtlmt_l low freq wgt1 limit

BAY3D_BAY3D_SIG_X0

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x102d	sw_bay3d_sig_x1 sigma curve coordinate x1
15:0	RW	0x002d	sw_bay3d_sig_x0 sigma curve coordinate x0

BAY3D_BAY3D_SIG_X1

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x1033	sw_bay3d_sig_x3 sigma curve coordinate x3
15:0	RW	0x1031	sw_bay3d_sig_x2 sigma curve coordinate x2

BAY3D_BAY3D_SIG_X2

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:16	RW	0x1057	sw_bay3d_sig_x5 sigma curve coordinate x5
15:0	RW	0x1053	sw_bay3d_sig_x4 sigma curve coordinate x4

BAY3D_BAY3D_SIG_X3

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:16	RW	0x30d7	sw_bay3d_sig_x7 sigma curve coordinate x7
15:0	RW	0x3057	sw_bay3d_sig_x6 sigma curve coordinate x6

BAY3D_BAY3D_SIG_X4

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:16	RW	0x7157	sw_bay3d_sig_x9 sigma curve coordinate x9
15:0	RW	0x70d7	sw_bay3d_sig_x8 sigma curve coordinate x8

BAY3D_BAY3D_SIG_X5

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:16	RW	0x715d	sw_bay3d_sig_x11 sigma curve coordinate x11
15:0	RW	0x715b	sw_bay3d_sig_x10 sigma curve coordinate x10

BAY3D_BAY3D_SIG_X6

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:16	RW	0x72dd	sw_bay3d_sig_x13 sigma curve coordinate x13
15:0	RW	0x725d	sw_bay3d_sig_x12 sigma curve coordinate x12

BAY3D_BAY3D_SIG_X7

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:16	RW	0x771d	sw_bay3d_sig_x15 sigma curve coordinate x15
15:0	RW	0x76dd	sw_bay3d_sig_x14 sigma curve coordinate x14

BAY3D_BAY3D_SIG_Y0

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0cc6	sw_bay3d_sig_y1 sigma curve coordinate y1
15:14	RO	0x0	reserved
13:0	RW	0x08ea	sw_bay3d_sig_y0 sigma curve coordinate y0

BAY3D_BAY3D_SIG_Y1

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0e62	sw_bay3d_sig_y3 sigma curve coordinate y3
15:14	RO	0x0	reserved
13:0	RW	0x0a3c	sw_bay3d_sig_y2 sigma curve coordinate y2

BAY3D_BAY3D_SIG_Y2

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0860	sw_bay3d_sig_y5 sigma curve coordinate y5
15:14	RO	0x0	reserved
13:0	RW	0x0da3	sw_bay3d_sig_y4 sigma curve coordinate y4

BAY3D_BAY3D_SIG_Y3

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0230	sw_bay3d_sig_y7 sigma curve coordinate y7
15:14	RO	0x0	reserved
13:0	RW	0x0460	sw_bay3d_sig_y6 sigma curve coordinate y6

BAY3D_BAY3D_SIG_Y4

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x086d	sw_bay3d_sig_y9 sigma curve coordinate y9
15:14	RO	0x0	reserved
13:0	RW	0x09f0	sw_bay3d_sig_y8 sigma curve coordinate y8

BAY3D_BAY3D_SIG_Y5

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x03d6	sw_bay3d_sig_y11 sigma curve coordinate y11
15:14	RO	0x0	reserved
13:0	RW	0x0152	sw_bay3d_sig_y10 sigma curve coordinate y10

BAY3D_BAY3D_SIG_Y6

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x06c6	sw_bay3d_sig_y13 sigma curve coordinate y13
15:14	RO	0x0	reserved
13:0	RW	0x0a61	sw_bay3d_sig_y12 sigma curve coordinate y12

BAY3D_BAY3D_SIG_Y7

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x093e	sw_bay3d_sig_y15 sigma curve coordinate y15
15:14	RO	0x0	reserved
13:0	RW	0x0f59	sw_bay3d_sig_y14 sigma curve coordinate y14

12.4.2.8 LSC

ISP_LSC_2200_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	lsc_lut_en Load correction factor from DDR
0	RW	0x0	lsc_en 1'b0: Activation request for lens shading correction 1'b1: Deactivation reqeust for lens shading correction Activation/Deactivation is object of a shadowing mechnism. The current status is visible at ISP_LSC_STATUS::lsc_enable_status

ISP_LSC_2200_R_TABLE_ADDR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	r_ram_addr Table address in RAM for samples of the R color component. Will be automatically incremented by each read or write access to the table. Valid addresses are in the range 0 to 152. --- ISP_LSC_R_TABLE_ADDR --- Note: The table values are written into an internal RAM. The RAM address is generated per auto-increment. The tables values will be read back by a continuous read access to the corresponding register. The read address is auto-incremented for each read access to that register and is reset to a specific value by a write access to the ISP_LSC_TABLE_ADDR register. Table set 0 access by SW at table address 0~152. Table set 1 access at table address 153~305.

ISP_LSC_2200_GR_TABLE_ADDR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x000	gr_ram_addr Table address in RAM for samples of the G_R color component. Will be automatically incremented by each read or write access to the table. --- ISP_LSC_GR_TABLE_ADDR --- Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_B_TABLE_ADDR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	b_ram_addr Table address in RAM for samples of the B color component. Will be automatically incremented by each read or write access to the table. --- ISP_LSC_B_TABLE_ADDR --- Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_GB_TABLE_ADDR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	gb_ram_addr Table address in RAM for samples of the G_B color component. Will be automatically incremented by each read or write access to the table. --- ISP_LSC_GB_TABLE_ADDR --- Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_R_TABLE_DATA

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:13	RW	0x0000	r_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999)

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	r_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999) --- ISP_LSC_R_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_GR_TABLE_DATA

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:13	RW	0x0000	gr_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999)
12:0	RW	0x0000	gr_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999) --- ISP_LSC_GR_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_B_TABLE_DATA

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:13	RW	0x0000	b_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999)
12:0	RW	0x0000	b_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999) --- ISP_LSC_B_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_GB_TABLE_DATA

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25:13	RW	0x0000	gb_sample_1 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999)
12:0	RW	0x0000	gb_sample_0 Correction factor at sample point (fixed point number: 3 bits integer with 10-bit fractional part, range 1~7.999) --- ISP_LSC_GB_TABLE_DATA --- Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0~153. Table set 1 access at table address 154~307.

ISP_LSC_2200_XGRAD_01

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_1 Factor for x-gradient calculation of sector 1
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_0 Factor for x-gradient calculation of sector 0

ISP_LSC_2200_XGRAD_23

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_3 Factor for x-gradient calculation of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_2 Factor for x-gradient calculation of sector 2

ISP_LSC_2200_XGRAD_45

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_5 Factor for x-gradient calculation of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_4 Factor for x-gradient calculation of sector 4

ISP_LSC_2200_XGRAD_67

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	xgrad_7 Factor for x-gradient calculation of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	xgrad_6 Factor for x-gradient calculation of sector 6

ISP_LSC_2200_YGRAD_01

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_1 Factor for y-gradient calculation of sector 1
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_0 Factor for y-gradient calculation of sector 0

ISP_LSC_2200_YGRAD_23

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_3 Factor for y-gradient calculation of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_2 Factor for y-gradient calculation of sector 2

ISP_LSC_2200_YGRAD_45

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_5 Factor for y-gradient calculation of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_4 Factor for y-gradient calculation of sector 4

ISP_LSC_2200_YGRAD_67

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ygrad_7 Factor for y-gradient calculation of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	ygrad_6 Factor for y-gradient calculation of sector 6

ISP_LSC_2200_XSIZE_01

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_1 Sector size 1 in x-direction
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	x_sect_size_0 Sector size 0 in x-direction --- ISP_LSC_XSIZE_01 --- Note: The sector size in x-direction must be greater than 12 pixels. The sum of the sector sizes in x-direction must be "picture width / 2". The sum of the sector sizes in y-direction must be "picture height / 2". No interrupt is generated if above requirements are not fulfilled and the behaviour of the hardware cannot be predicted. The sector size in x-direction was defined to be 9 bits for preliminary Marvin versions.

ISP_LSC_2200_XSIZE_23

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_3 Sector size 3 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_2 Sector size 2 in x-direction --- ISP_LSC_XSIZE_23 --- Note: Minimum sector size is 10 in x direction.

ISP_LSC_2200_XSIZE_45

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_5 Sector size 5 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_4 Sector size 4in x-direction --- ISP_LSC_XSIZE_45 --- Note: Minimum sector size is 10 in x direction.

ISP_LSC_2200_XSIZE_67

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_sect_size_7 Sector size 7 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_sect_size_6 Sector size 6 in x-direction --- ISP_LSC_XSIZE_67 --- Note: Minimum sector size is 10 in x direction.

ISP_LSC_2200_YSIZE_01

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_1 Sector size 1 in y-direction

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_0 Sector size 0 in y-direction --- ISP_LSC_YSIZE_01 --- Note: Minimum sector size is 8 in y direction. The sector size in y-direction was defined to be 9 bits for preliminary Marvin versions.

ISP_LSC_2200_YSIZE_23

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_3 Sector size 3 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_2 Sector size 2 in y-direction --- ISP_LSC_YSIZE_23 --- Note: Minimum sector size is 8 in y direction.

ISP_LSC_2200_YSIZE_45

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_5 Sector size 5 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_4 Sector size 4 in y-direction --- ISP_LSC_YSIZE_45 --- Note: Minimum sector size is 8 in y direction.

ISP_LSC_2200_YSIZE_67

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_sect_size_7 Sector size 7 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_sect_size_6 Sector size 6 in y-direction --- ISP_LSC_YSIZE_67 --- Note: Minimum sector size is 8 in y direction.

ISP_LSC_2200_ISP_LSC_STATUS

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lsc_en_status 1'b0: Lens shading correction is currently off; 1'b1: Lens shading correction is currently on.

12.4.2.9 HDR_DRC

ISP_DRC_3900_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sys_itself_force_upd when write 1, it will force_upd drc module; auto-clear;
30	RO	0x0	ro_adrc_working 1'b1: adrc working
29:28	RW	0x0	sw_drc_bil_ack_mode backdoor to bilat_interp ack low 1-4 cycle
27:1	RO	0x0	reserved
0	RW	0x0	sw_hdrtmo_en rkhdr function enable, shadow reg;

ISP_DRC_3900_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RW	0x8	sw_drc_offset_pow2 log offset: indata+(1<<offset_pow2), then log2data-offset_pow2, shadow reg;
27	RO	0x0	reserved
26:14	RW	0x0e41	sw_drc_compres_scl [2,11], scale plgmax range(0~24576) for trans compress, shadow reg;
13:0	RW	0x0100	sw_drc_position [6,8], pluma scale for table index of gain2raw, shadow reg;

ISP_DRC_3900_LPRATIO

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_drc_delta_scalein [0,8], for plgt*delta_scalein into scaleTable, shadow reg;
23:12	RW	0x000	sw_drc_hpdetail_ratio [1,11], for delt=delt + gain_scl*hpdetail_ratio used, shadow reg;
11:0	RW	0x000	sw_drc_lpdetail_ratio [1,11], for delt=(lgt-nglt) + (lgt-maxl)*lpdetail_ratio used, shadow reg;

ISP_DRC_3900_EXPLRATIO

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	sw_drc_weicur_pix [4,4]<<7, bilat-weight of current pix;
23:16	RW	0x00	sw_drc_weipre_frame [0,8], bilat-weight of previous frame;
15	RO	0x0	reserved
14:0	RW	0x1000	sw_drc_expl_ratio [3,12], cur_exp_time*cur_exp_gain/(prev_exp_time*prev_exp_gain) in normal domain

ISP_DRC_3900_SIGMA

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_drc_force_sgm_inv0 [5,11], force bilat-5x5 sigma(edge+motion) value = force_sgm_inv0 if force_sgm_inv0!=0;
15:8	RW	0x00	sw_drc_motion_scl [4,4], scale motion data for bilat-diff, use when edge/motion writing into ram;
7:0	RW	0x00	sw_drc_edge_scl [4,4], scale edge data for bilat-diff, use when edge/motion writing into ram;

ISP_DRC_3900_SPACESGM

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfe4	sw_drc_space_sgm_inv1 [4,8], bil3x3 space sigma invert weight: high-4b expoent, low-8b mantissa;
15:12	RO	0x0	reserved
11:0	RW	0xf80	sw_drc_space_sgm_inv0 [4,8], bil5x5 space sigma invert weight: high-4b expoent, low-8b mantissa; (x^2+y^2)*sigma_inv;

ISP_DRC_3900_RANESGM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_range_sgm_inv1 [2,11], bil3x3 range sigma invert weight; (diff*range_sigma_inv)^2;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_range_sgm_inv0 [2,11], bil5x5 range sigma invert weight; (diff*range_sigma_inv)^2;

ISP_DRC_3900_BILAT

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	sw_drc_weig_maxl [1,4], weight for (max3x3*W + (16-W)*gas3x3) when bilateral filter in, shadow reg in rk3566;
7:5	RO	0x0	reserved
4:0	RW	0x10	sw_drc_weig_bilat [1,4], weight for (bilat*W + (16-W)*luma) when bilateral filter out, shadow reg in rk3566;

ISP_DRC_3900_GAIN_Y0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y1 [3,10], curve_gain2raw y1, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y0 [3,10], curve_gain2raw y0, shadow reg;

ISP_DRC_3900_GAIN_Y1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y3 [3,10], curve_gain2raw y3, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y2 [3,10], curve_gain2raw y2, shadow reg;

ISP_DRC_3900_GAIN_Y2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y5 [3,10], curve_gain2raw y5, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y4 [3,10], curve_gain2raw y4, shadow reg;

ISP_DRC_3900_GAIN_Y3

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y7 [3,10], curve_gain2raw y7, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y6 [3,10], curve_gain2raw y6, shadow reg;

ISP_DRC_3900_GAIN_Y4

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y9 [3,10], curve_gain2raw y9, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y8 [3,10], curve_gain2raw y8, shadow reg;

ISP_DRC_3900_GAIN_Y5

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y11 [3,10], curve_gain2raw y11, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y10 [3,10], curve_gain2raw y10, shadow reg;

ISP_DRC_3900_GAIN_Y6

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y13 [3,10], curve_gain2raw y13, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y12 [3,10], curve_gain2raw y12, shadow reg;

ISP_DRC_3900_GAIN_Y7

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	sw_drc_gain_y15 [3,10], curve_gain2raw y15, shadow reg;
15:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y14 [3,10], curve_gain2raw y14, shadow reg;

ISP_DRC_3900_GAIN_Y8

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0400	sw_drc_gain_y16 [3,10], curve_gain2raw y16, shadow reg;

ISP_DRC_3900_COMPRES_Y0

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x022e	sw_drc_compres_y1 [3,11], curve_compress y1, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_drc_compres_y0 [3,11], curve_compress y0, shadow reg;

ISP_DRC_3900_COMPRES_Y1

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0634	sw_drc_compres_y3 [3,11], curve_compress y3, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x043f	sw_drc_compres_y2 [3,11], curve_compress y2, shadow reg;

ISP_DRC_3900_COMPRES_Y2

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x09d3	sw_drc_compres_y5 [3,11], curve_compress y5, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x080f	sw_drc_compres_y4 [3,11], curve_compress y4, shadow reg;

ISP_DRC_3900_COMPRES_Y3

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0d19	sw_drc_compres_y7 [3,11], curve_compress y7, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x0b80	sw_drc_compres_y6 [3,11], curve_compress y6, shadow reg;

ISP_DRC_3900_COMPRES_Y4

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1179	sw_drc_compres_y9 [3,11], curve_compress y9, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x0ea0	sw_drc_compres_y8 [3,11], curve_compress y8, shadow reg;

ISP_DRC_3900_COMPRES_Y5

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1677	sw_drc_compres_y11 [3,11], curve_compress y11, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x1413	sw_drc_compres_y10 [3,11], curve_compress y10, shadow reg;

ISP_DRC_3900_COMPRES_Y6

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1ab6	sw_drc_compres_y13 [3,11], curve_compress y13, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x18ac	sw_drc_compres_y12 [3,11], curve_compress y12, shadow reg;

ISP_DRC_3900_COMPRES_Y7

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x1e5c	sw_drc_compres_y15 [3,11], curve_compress y15, shadow reg;
15:14	RO	0x0	reserved
13:0	RW	0x1c9a	sw_drc_compres_y14 [3,11], curve_compress y14, shadow reg;

ISP_DRC_3900_COMPRES_Y8

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x2000	sw_drc_compres_y16 [3,11], curve_compress y16, shadow reg;

ISP_DRC_3900_SCALE_Y0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x002	sw_drc_scale_y1 [1,11], curve_scale y1;
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_drc_scale_y0 [1,11], curve_scale y0;

ISP_DRC_3900_SCALE_Y1

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x04c	sw_drc_scale_y3 [1,11], curve_scale y3;
15:12	RO	0x0	reserved
11:0	RW	0x014	sw_drc_scale_y2 [1,11], curve_scale y2;

ISP_DRC_3900_SCALE_Y2

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x17d	sw_drc_scale_y5 [1,11], curve_scale y5;
15:12	RO	0x0	reserved
11:0	RW	0x0c1	sw_drc_scale_y4 [1,11], curve_scale y4;

ISP_DRC_3900_SCALE_Y3

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x304	sw_drc_scale_y7 [1,11], curve_scale y7;
15:12	RO	0x0	reserved
11:0	RW	0x277	sw_drc_scale_y6 [1,11], curve_scale y6;

ISP_DRC_3900_SCALE_Y4

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x42a	sw_drc_scale_y9 [1,11], curve_scale y9;
15:12	RO	0x0	reserved
11:0	RW	0x397	sw_drc_scale_y8 [1,11], curve_scale y8;

ISP_DRC_3900_SCALE_Y5

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x5c7	sw_drc_scale_y11 [1,11], curve_scale y11;
15:12	RO	0x0	reserved
11:0	RW	0x4bb	sw_drc_scale_y10 [1,11], curve_scale y10;

ISP_DRC_3900_SCALE_Y6

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x747	sw_drc_scale_y13 [1,11], curve_scale y13;
15:12	RO	0x0	reserved
11:0	RW	0x6a4	sw_drc_scale_y12 [1,11], curve_scale y12;

ISP_DRC_3900_SCALE_Y7

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x7e8	sw_drc_scale_y15 [1,11], curve_scale y15;
15:12	RO	0x0	reserved
11:0	RW	0x7b0	sw_drc_scale_y14 [1,11], curve_scale y14;

ISP_DRC_3900_SCALE_Y8

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x800	sw_drc_scale_y16 [1,11], curve_scale y16;

ISP_DRC_3900_IIRWG_GAIN

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x00	sw_drc_iir_weight [1,6], range 0~0x40; weight of iir_thumb mix with pre_thumb, shadow reg;
15:0	RW	0x0000	sw_drc_min_ogain [1,15], adrc_out gain clip value, shadow reg;

12.4.2.10 GIC

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_gic_en_shk 1'b1: shk is success 1'b0: shk is fail
30	RO	0x0	sw_gic_woking 1'b1: gic is woking 1'b0: gic is not woking
29:2	RO	0x0	reserved
1	RW	0x0	sw_edge_open Usually set this bit to 0,it will influence shapen result when open,but also will get a better gic effect 1'b1:open 1'b0:close
0	RW	0x0	sw_gic_en 1'b1:enable gic module 1'b0:close gic module

ISP_GIC_DIFF_PARA1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	sw_regMinGradThrDark2 The lower limit 2 of the classification threshold when in a dark environment
19:10	RW	0x040	sw_regMinGradThrDark1 The lower limit 1 of the classification threshold when in a dark ienvironment
9:0	RW	0x0a0	sw_regMinbusythre The lower limit of the gradient threshold

ISP_GIC_DIFF_PARA2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:21	RW	0x078	sw_regDarkThre Luminance judgment parameter2
20:11	RW	0x008	sw_regMaxCorVboth The value and threshold parameters of nonedge class
10:0	RW	0x0f0	sw_regDarkTthreHi Luminance judgment parameter1

ISP_GIC_DIFF_PARA3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:28	RW	0x1	sw_regKGrad2Dark The calculation parameters 1 of the classification threshold when in a dark Environment
27:24	RW	0x6	sw_regKGrad1Dark The calculation parameters 1 of the classification threshold when in a dark environment
23:16	RW	0x08	sw_regStrengthGlobal_fix Strength adjustment parameter
15:12	RW	0x9	sw_regDarkThreStep Displacement parameters of dark weight
11:8	RW	0x1	sw_regKGrad2 The calculation parameters 2 of the classification threshold
7:4	RW	0x5	sw_regKGrad1 The calculation parameters 1 of the classification threshold
3:0	RW	0x7	sw_regGbThre Displacement parameters of sum of mean values

ISP_GIC_DIFF_PARA4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x028	sw_regMaxCorv The value and threshold parameters of edge class
19:10	RW	0x020	sw_regMinGradThr2 The lower limit parameter 2 of the classification threshold
9:0	RW	0x020	sw_regMinGradThr1 The lower limit parameter 1 of the classification threshold

ISP_GIC_NOISE_PARA1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:15	RW	0x180	sw_dnLoScale Calculation parameters of lower limit of noise
14:4	RW	0x280	sw_dnHiScale Calculation parameters of upper limit of noise
3:0	RW	0x7	sw_regLumaPointsStep Calculation parameters of sigma noise

ISP_GIC_NOISE_PARA2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RW	0x500	sw_gValueLimitLo the lower limit of the difference between limits of the noise
19:8	RW	0x6e0	sw_gValueLimitHi the upper limit of the difference between limits of the noise
7:0	RW	0x09	sw_fusionRatioHiLimt1 Calculation parameters of noise factor

ISP_GIC_NOISE_PARA3

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x20	sw_regStrength_fix Noise enhancement coefficient

ISP_GIC_SIGMA_VALUE0

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x01f0	sw_sigma_y1 y1 value of sigma table
15:0	RW	0x0042	sw_sigma_y0 y0 value of sigma table

ISP_GIC_SIGMA_VALUE1

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0357	sw_sigma_y3 y3 value of sigma table
15:0	RW	0x02bb	sw_sigma_y2 y2 value of sigma table

ISP_GIC_SIGMA_VALUE2

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:16	RW	0x044f	sw_sigma_y5 y5 value of sigma table
15:0	RW	0x03db	sw_sigma_y4 y4 value of sigma table

ISP_GIC_SIGMA_VALUE3

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0518	sw_sigma_y7 y7 value of sigma table
15:0	RW	0x04b8	sw_sigma_y6 y6 value of sigma table

ISP_GIC_SIGMA_VALUE4

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x06ab	sw_sigma_y9 y9 value of sigma table
15:0	RW	0x0572	sw_sigma_y8 y8 value of sigma table

ISP_GIC_SIGMA_VALUE5

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x089b	sw_sigma_y11 y11 value of sigma table
15:0	RW	0x07b2	sw_sigma_y10 y10 value of sigma table

ISP_GIC_SIGMA_VALUE6

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0a2e	sw_sigma_y13 y13 value of sigma table
15:0	RW	0x096d	sw_sigma_y12 y12 value of sigma table

ISP_GIC_SIGMA_VALUE7

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0ae2	sw_sigma_y14 y14 value of sigma table

12.4.2.11 DEBAYER

ISP_DEBAYER_2500_CONTROL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	sw_debayer_working 1'b0: Debayer module is not working; 1'b1: Debayer module is working.

Bit	Attr	Reset Value	Description
26	RO	0x0	sw_debayer_filter_c_en_shd The shadow register of sw_debayer_filter_c_en
25	RO	0x0	sw_debayer_filter_g_en_shd The shadow register of sw_debayer_filter_g_en
24	RO	0x0	sw_debayer_en_shd The shadow register of sw_debayer_en
23:9	RO	0x0000	reserved
8	RW	0x1	sw_debayer_filter_c_en 1'b0: C filter module will bypass; 1'b1: Enable c filter module
7:5	RO	0x0	reserved
4	RW	0x1	sw_debayer_filter_g_en 1'b0: G filter module will bypass; 1'b1: Enable g filter
3:1	RO	0x0	reserved
0	RW	0x0	sw_debayer_en 1'b0: Debayer module will bypass; 1'b1: Enable debayer

ISP_DEBAYER_2500_G_INTERP

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	sw_debayer_thed1 0 is equal to 0 16 is equal to 0.5
11:8	RW	0x3	sw_debayer_thed0 0 is equal to 0 16 is equal to 0.5
7:4	RW	0x8	sw_debayer_dist_scale 0 is equal to 0 15 is equal to 1.875
3:1	RW	0x4	sw_debayer_max_ratio The level of sharp in the g interpolation 0 is the lowest level, and 7 is the highest level.
0	RW	0x1	sw_debayer_clip_en Clip enable for g interpolation If enable this bit, the interpolated g will be cliped to [Gmin,Gmax].

ISP_DEBAYER_2500_G_INTERP_FILTER1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0xe	sw_debayer_filter1_coe5 Coe5 (the most significant bit is sign bit) Value range: -8 to 7
15:12	RW	0x6	sw_debayer_filter1_coe4 Coe4 (the most significant bit is sign bit) Value range: -8 to 7
11:8	RW	0x0	sw_debayer_filter1_coe3 Coe3 (the most significant bit is sign bit) Value range: -8 to 7

Bit	Attr	Reset Value	Description
7:4	RW	0xa	sw_debayer_filter1_coe2 Coe2 (the most significant bit is sign bit) Value range: -8 to 7
3:0	RW	0x2	sw_debayer_filter1_coe1 Coe1 (the most significant bit is sign bit) Value range: -8 to 7

ISP_DEBAYER_2500_G_INTERP_FILTER2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x2	sw_debayer_filter2_coe5 Coe5 (the most significant bit is sign bit) Value range: -8 to 7
15:12	RW	0xc	sw_debayer_filter2_coe4 Coe4 (the most significant bit is sign bit) Value range: -8 to 7
11:8	RW	0x4	sw_debayer_filter2_coe3 Coe3 (the most significant bit is sign bit) Value range: -8 to 7
7:4	RW	0xc	sw_debayer_filter2_coe2 Coe2 (the most significant bit is sign bit) Value range: -8 to 7
3:0	RW	0x2	sw_debayer_filter2_coe1 Coe1 (the most significant bit is sign bit) Value range: -8 to 7

ISP_DEBAYER_2500_OFFSET

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0080	sw_debayer_hf_offset HF offset for G interp
15:12	RO	0x0	reserved
11:8	RW	0x4	sw_debayer_gain_offset Gain offset for G interp
7:5	RO	0x0	reserved
4:0	RW	0x01	sw_debayer_offset Offset for G filter

ISP_DEBAYER_2500_C_FILTER

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x2	sw_debayer_shift_num 2'b00: Left shift 1 bit 2'b01: Left shift 2 bit 2'b10: Left shift 3 bit 2'b11: Left shift 4 bit
15:13	RO	0x0	reserved
12:8	RW	0x0e	sw_debayer_order_max The max sequence number of 24 G-C in the 9*9 matrix
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_debayer_order_min The min sequence number of 24 G-C in the 9*9 matrix

12.4.2.12 CCM

ISP_CCM_0700_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	sw_ccm_highy_adjust_dis Disable CCM high Y alpha adjustment bit 1'b1: High Y alpha adjustment disable 1'b0: High Y alpha adjustment
0	RW	0x0	sw_ccm_en_i Enable CCM module 1'b1: Enable 1'b0: Disable The reset value is 1'b0

ISP_CCM_0700_COEFF0_R

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x7b7	sw_ccm_coeff1_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x065	sw_ccm_coeff0_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_R

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_r The R offset value for CCM calculation. The range of offset value is from -4096 to 4095.
15:11	RO	0x0	reserved
10:0	RW	0x7e4	sw_ccm_coeff2_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_G

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x058	sw_ccm_coeff1_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x7d9	sw_ccm_coeff0_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_G

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x7cf	sw_ccm_coeff2_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_B

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x7b7	sw_ccm_coeff1_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x002	sw_ccm_coeff0_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_B

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x046	sw_ccm_coeff2_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit frctional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff],so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_Y

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x04b	sw_ccm_coeff1_y The G coefficent value of RGB2Y calculation. The value is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x026	sw_ccm_coeff0_y The R coefficent value of RGB2Y calculation. The value is expanded 128 times.

ISP_CCM_0700_COEFF1_Y

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x00f	sw_ccm_coeff2_y The B coefficent value of RGB2Y calculation. The value is expanded 128 times.

ISP_CCM_0700_ALP_Y0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y1 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y0 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y3 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y2 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y2

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y5 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y4 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y3

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y7 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y6 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y4

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y9 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y8 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y5

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y11 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y10 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y6

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y13 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y12 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y7

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x400	sw_ccm_alp_y15 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.
15:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y14 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_ALP_Y8

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x400	sw_ccm_alp_y16 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. The value of y-axis point is expanded 128 times.

ISP_CCM_0700_bound_bit

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	sw_ccm_bound_bit CCM alpha interpolation curve's inflection point . The inflection ponit is 2^sw_ccm_bound_bit. The max value is 4'b10 because the inflection point's max value is 1024.

12.4.2.13 GAMMA_OUT

ISP_GAMMA_OUT_0900_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_gamma_out_en_shd gamma_out enable shadow
30	RO	0x0	gamma_out_working gamma_out working status
29:2	RO	0x0000000	reserved
1	RW	0x0	sw_gamma_out_equ_segm 1'b0: Division like segmentation of gamma curve (default after reset) The segmentation from 0 to 4095 (44 segments): 1111 1111 2222 4444 8888 16.16.16.16 32.32.32.32 64.64.64.64 128.128.128.128 256.256.256.256 512.512.512.512; 1'b1: Equidistant segmentation (all segments are equally)
0	RW	0x0	sw_gamma_out_en 1'b0: gamma_out disable 1'b1: gamma_out enable

ISP_GAMMA_OUT_0900_OFFSET

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_gamma_out_offset Offset value of gamma_out curve

ISP_GAMMA_OUT_0900_Y0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x001	sw_gamma_out_y1 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_out_y0 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x003	sw_gamma_out_y3 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x002	sw_gamma_out_y2 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x005	sw_gamma_out_y5 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x004	sw_gamma_out_y4 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y3

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x007	sw_gamma_out_y7 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x006	sw_gamma_out_y6 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y4

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	sw_gamma_out_y9 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x008	sw_gamma_out_y8 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y5

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00e	sw_gamma_out_y11 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x00c	sw_gamma_out_y10 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y6

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x014	sw_gamma_out_y13 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x010	sw_gamma_out_y12 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y7

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x01c	sw_gamma_out_y15 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x018	sw_gamma_out_y14 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y8

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x028	sw_gamma_out_y17 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x020	sw_gamma_out_y16 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y9

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x038	sw_gamma_out_y19 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x030	sw_gamma_out_y18 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y10

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x050	sw_gamma_out_y21 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x040	sw_gamma_out_y20 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y11

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x070	sw_gamma_out_y23 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x060	sw_gamma_out_y22 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y12

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_gamma_out_y25 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x080	sw_gamma_out_y24 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y13

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e0	sw_gamma_out_y27 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x0c0	sw_gamma_out_y26 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y14

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x140	sw_gamma_out_y29 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_out_y28 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y15

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1c0	sw_gamma_out_y31 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x180	sw_gamma_out_y30 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y16

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x280	sw_gamma_out_y33 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_out_y32 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y17

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x380	sw_gamma_out_y35 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_out_y34 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y18

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x500	sw_gamma_out_y37 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_out_y36 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y19

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x700	sw_gamma_out_y39 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x600	sw_gamma_out_y38 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y20

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xa00	sw_gamma_out_y41 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x800	sw_gamma_out_y40 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y21

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xe00	sw_gamma_out_y43 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_out_y42 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y22

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_out_y44 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

12.4.2.14 DEHAZE_ENHANCE

ISP_DHAZ_3C00_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd dhaz itself force update
30	RW	0x0	dhaz_working RO : dehaze working ; dehaze disable
29:25	RO	0x0	reserved
24	RW	0x0	sw_dhaz_ckg_dis clock gating, 1: gating disable, 0: gating enable
23:21	RO	0x0	reserved
20	RW	0x0	sw_dhaz_enhance_en 1'b0: Dehaze enhance disable; 1'b1: Dehaze enhance enable; Default: 1'b0; must shadow
19:17	RO	0x0	reserved
16	RW	0x0	sw_dhaz_air_lc_en only dehaze mode valid 1'b0: use adaption air_base; 1'b1: use (max(r,g,b),air_base); Default: 1'b0; must shadow
15:13	RO	0x0	reserved
12	RW	0x0	sw_dhaz_hpara_en 1'b1:hist parameter enable; 1'b0:hist parameter disable. Default: 1'b1; must shadow
11:9	RO	0x0	reserved
8	RW	0x1	sw_dhaz_hist_en 1'b1:hist equilibration enable; 1'b0:hist equilibration disable. Default: 1'b1; must shadow
7:5	RO	0x0	reserved
4	RW	0x1	sw_dhaz_dc_en 1'b0: Dehaze dark channel disable; 1'b1: Dehaze dark channel enable; Default: 1'b0; must shadow
3:1	RO	0x0	reserved
0	RW	0x0	sw_dhaz_en_mux Dehaze enable, 1'b1: enable; 1'b0:disable. Default:0

ISP_DHAZ_3C00_ADP0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x1b	sw_dhaz_yblk_th Y self-adaption threshold of block ratiod. Default:0.002*col_blk*row_blk, range:(0.002~0.01)*col_blk*row_blk
23:16	RW	0xf9	sw_dhaz_yhist_th Y self-adaption high light threshold. Default:249, range:170~255
15:8	RW	0xc0	sw_dhaz_dc_max_th Wt self-adaption high light threshold. Default:192, range:170~255
7:0	RW	0x40	sw_dhaz_dc_min_th Wt self-adaption min threshold. Default 64, range:16~120

ISP_DHAZ_3C00_ADP1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x0e6	sw_dhaz_wt_max Wt self-adaption max threshold. Default:0.9*256=230, range:(0.75~0.9)*256
15:8	RW	0xf0	sw_dhaz_bright_max Bright self-adaption max threshold. Default:240, range:210~250
7:0	RW	0xb4	sw_dhaz_bright_min Bright self-adaption min threshold. Default:180, range:160~200

ISP_DHAZ_3C00_ADP2

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:24	RW	0x7d	sw_dhaz_tmax_base Tmax self-adaption base valve. Default:125, range:131~105; (200(131),210(125),220(119),230(114),240(109),250(105))
23:16	RW	0xfa	sw_dhaz_dark_th Wt self-adaption min threshold. Default:250, range:230~250
15:8	RW	0xfa	sw_dhaz_air_max Air self-adaption max threshold. Default:250, range:230~250
7:0	RW	0xe6	sw_dhaz_air_min Air self-adaption min threshold. Default:200, range:200~220

ISP_DHAZ_3C00_ADP_TMAX

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x200	sw_dhaz_tmax_max Tmax self-adaption max threshold. Default:0.5*1024, range:0.1*1024~0.5*1024
15:10	RO	0x0	reserved
9:0	RW	0x066	sw_dhaz_tmax_off Tmax self-adaption offset threshold. Default:0.1*1024=102, range:0.1*1024~0.5 *1024

ISP_DHAZ_3C00_ADP_HIST0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x004	sw_dhaz_hist_min The min statistical threshold of hist. Default:0.016*256
15:8	RW	0x40	sw_dhaz_hist_th_off The statistical threshold offset of hist. Default:64
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_dhaz_hist_k Amp times of hist self-adaption. Default:2

ISP_DHAZ_3C00_ADP_HIST1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x10	sw_dhaz_hist_gratio The draw ratio of hist,5bit+3bit
15:13	RO	0x0	reserved
12:0	RW	0x00e6	sw_dhaz_hist_scale Dehaze hist scale user config while sw_dhaz_hpara_en is enabled

ISP_DHAZ_3C00_ENHANCE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0600	sw_dhaz_enhance_value The light enhance value
15:14	RO	0x0	reserved
13:0	RW	0x04cc	sw_dhaz_enhance_chroma The light enhance chroma

ISP_DHAZ_3C00_IIR0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x00f	sw_dhaz_iir_wt_sigma The coeff of inter wt iir control
15:8	RW	0x01	sw_dhaz_iir_sigma The sigma value of iir control. Default:6; max:255
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_dhaz_stab_fnum Max stable frame num

ISP_DHAZ_3C00_IIR1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x7	sw_dhaz_iir_pre_wet weight of previous down scale and current down scale, must > 0
23:19	RO	0x0	reserved
18:8	RW	0x05f	sw_dhaz_iir_tmax_sigma The coeff of inter tmax iir control
7:0	RW	0x08	sw_dhaz_iir_air_sigma The coeff of inter air iir control

ISP_DHAZ_3C00_SOFT_CFG0

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x0cc	sw_dhaz_cfg_wt Softwave config wt, range:0~256
15:8	RW	0xd2	sw_dhaz_cfg_air Softwave config airlight, range:0~255
7:0	RW	0x00	sw_dhaz_cfg_alpha The weight of cfg data. Eg:wt = ((sw_dhaz_cfg_alpha * sw_dhaz_cfg_wt + (256 - sw_dhaz_cfg_alpha) * wt_cur)/256); Range:0~255; 255 parsing to 256. Default: 0

ISP_DHAZ_3C00_SOFT_CFG1

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0200	sw_dhaz_cfg_gratio Softwave config gratio
15:10	RO	0x0	reserved
9:0	RW	0x0cc	sw_dhaz_cfg_tmax Softwave config tmax, range:0~1024

ISP_DHAZ_3C00_BF_SIGMA

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x080	sw_dhaz_range_sigma range sigma of bilateral filter
15:8	RW	0x4d	sw_dhaz_space_sigma_pre space sigma of previous bilateral filter
7:0	RW	0x99	sw_dhaz_space_sigma_cur space sigma of current bilateral filter

ISP_DHAZ_3C00_BF_WET

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x100	sw_dhaz_dc_weitcur current center weight of bilateral filter
15:9	RO	0x0	reserved
8:0	RW	0x080	sw_dhaz_bf_weight weight of bilateral filter

ISP_DHAZ_3C00_ENH_CURVE0

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x040	sw_dhaz_curve1 map curve1
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_dhaz_curve0 map curve0

ISP_DHAZ_3C00_ENH_CURVE1

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x0c0	sw_dhaz_curve3 map curve3
15:10	RO	0x0	reserved
9:0	RW	0x080	sw_dhaz_curve2 map curve2

ISP_DHAZ_3C00_ENH_CURVE2

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x140	sw_dhaz_curve5 map curve5
15:10	RO	0x0	reserved
9:0	RW	0x100	sw_dhaz_curve4 map curve4

ISP_DHAZ_3C00_ENH_CURVE3

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x1c0	sw_dhaz_curve7 map curve7
15:10	RO	0x0	reserved
9:0	RW	0x180	sw_dhaz_curve6 map curve6

ISP_DHAZ_3C00_ENH_CURVE4

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x240	sw_dhaz_curve9 map curve9
15:10	RO	0x0	reserved
9:0	RW	0x200	sw_dhaz_curve8 map curve8

ISP_DHAZ_3C00_ENH_CURVE5

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x2c0	sw_dhaz_curve11 map curve11
15:10	RO	0x0	reserved
9:0	RW	0x280	sw_dhaz_curve10 map curve10

ISP_DHAZ_3C00_ENH_CURVE6

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x340	sw_dhaz_curve13 map curve13
15:10	RO	0x0	reserved
9:0	RW	0x300	sw_dhaz_curve12 map curve12

ISP_DHAZ_3C00_ENH_CURVE7

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x3c0	sw_dhaz_curve15 map curve15
15:10	RO	0x0	reserved
9:0	RW	0x380	sw_dhaz_curve14 map curve14

ISP_DHAZ_3C00_ENH_CURVE8

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x3ff	sw_dhaz_curve16 map curve16

ISP_DHAZ_3C00_GAUS

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RW	0x02	sw_dhaz_gaus_h2 The gausi smoothed coefficient, 3*3window□ /32 normalization.(h0+4*h1+4*h2=32)
15:14	RO	0x0	reserved
13:8	RW	0x04	sw_dhaz_gaus_h1 The gausi smoothed coefficient, 3*3window□ /32 normalization.(h0+4*h1+4*h2=32)
7:6	RO	0x0	reserved
5:0	RW	0x08	sw_dhaz_gaus_h0 The gausi smoothed coefficient, 3*3window□ /32 normalization.(h0+4*h1+4*h2=32)

ISP_DHAZ_3C00_CTRL_SHD

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dhaz_gain_working Dehaze gain module working flag. 1:working; 0:not working. 3566 no use
29	RO	0x0	dhaz_hist_working Dehaze hist equlation module working flag. 1:working; 0:not working.
28	RO	0x0	dhaz_bilat_working Dehaze dark channel module working flag. 1:working; 0:not working.
27:21	RO	0x0	reserved
20	RO	0x0	sw_dhaz_enhance_en_shd Dehaze enhance enable shandow.
19:17	RO	0x0	reserved
16	RO	0x0	sw_dhaz_air_lc_shd Dehaze rgb channel separate shandow.
15:13	RO	0x0	reserved
12	RO	0x0	sw_dhaz_hpara_en_shd Dehaze hist parameter enable shandow.
11:9	RO	0x0	reserved
8	RO	0x0	sw_dhaz_hist_en_shd Dehaze hist equilibration enable shandow.
7:5	RO	0x0	reserved
4	RO	0x0	sw_dhaz_dc_en_shd Dehaze dark channel enable shandow.
3:0	RO	0x0	reserved

ISP_DHAZ_3C00_ADP_RD0

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	dhaz_adp_air_base Air_base of self-adaption
15:9	RO	0x0	reserved
8:0	RO	0x000	dhaz_adp_wt Wt of self-adaption

ISP_DHAZ_3C00_ADP_RD1

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	dhaz_adp_gratio Hist gratio of self-adaption
15:10	RO	0x0	reserved
9:0	RO	0x000	dhaz_adp_tmax Tmax of self-adaption

ISP_DHAZ_3C00_HIST_REG0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x010	h_rgb_iir1 Hist rgb iir reg 1 data
15:10	RO	0x0	reserved
9:0	RO	0x000	h_rgb_iir0 Hist rgb iir reg 0 data

ISP_DHAZ_3C00_HIST_REG1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x030	h_rgb_iir3 Hist rgb iir reg 3 data
15:10	RO	0x0	reserved
9:0	RO	0x020	h_rgb_iir2 Hist rgb iir reg 2 data

ISP_DHAZ_3C00_HIST_REG2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x050	h_rgb_iir5 Hist rgb iir reg 5 data
15:10	RO	0x0	reserved
9:0	RO	0x040	h_rgb_iir4 Hist rgb iir reg 4 data

ISP_DHAZ_3C00_HIST_REG3

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x070	h_rgb_iir7 Hist rgb iir reg 7 data
15:10	RO	0x0	reserved
9:0	RO	0x060	h_rgb_iir6 Hist rgb iir reg 6 data

ISP_DHAZ_3C00_HIST_REG4

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x090	h_rgb_iir9 Hist rgb iir reg 9 data
15:10	RO	0x0	reserved
9:0	RO	0x080	h_rgb_iir8 Hist rgb iir reg 8 data

ISP_DHAZ_3C00_HIST_REG5

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x0b0	h_rgb_iir11 Hist rgb iir reg 11 data
15:10	RO	0x0	reserved
9:0	RO	0x0a0	h_rgb_iir10 Hist rgb iir reg 10 data

ISP_DHAZ_3C00_HIST_REG6

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x0d0	h_rgb_iir13 Hist rgb iir reg 13 data
15:10	RO	0x0	reserved
9:0	RO	0x0c0	h_rgb_iir12 Hist rgb iir reg 12 data

ISP_DHAZ_3C00_HIST_REG7

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x0f0	h_rgb_iir15 Hist rgb iir reg 15 data
15:10	RO	0x0	reserved
9:0	RO	0x0e0	h_rgb_iir14 Hist rgb iir reg 14 data

ISP_DHAZ_3C00_HIST_REG8

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x110	h_rgb_iir17 Hist rgb iir reg 17 data
15:10	RO	0x0	reserved
9:0	RO	0x100	h_rgb_iir16 Hist rgb iir reg 16 data

ISP_DHAZ_3C00_HIST_REG9

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x130	h_rgb_iir19 Hist rgb iir reg 19 data
15:10	RO	0x0	reserved
9:0	RO	0x120	h_rgb_iir18 Hist rgb iir reg 18 data

ISP_DHAZ_3C00_HIST_REG10

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x150	h_rgb_iir21 Hist rgb iir reg 21 data
15:10	RO	0x0	reserved
9:0	RO	0x140	h_rgb_iir20 Hist rgb iir reg 20 data

ISP_DHAZ_3C00_HIST_REG11

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x170	h_rgb_iir23 Hist rgb iir reg 23 data
15:10	RO	0x0	reserved
9:0	RO	0x160	h_rgb_iir22 Hist rgb iir reg 22 data

ISP_DHAZ_3C00_HIST_REG12

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x190	h_rgb_iir25 Hist rgb iir reg 25 data
15:10	RO	0x0	reserved
9:0	RO	0x180	h_rgb_iir24 Hist rgb iir reg 24 data

ISP_DHAZ_3C00_HIST_REG13

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x1b0	h_rgb_iir27 Hist rgb iir reg 27 data
15:10	RO	0x0	reserved
9:0	RO	0x1a0	h_rgb_iir26 Hist rgb iir reg 26 data

ISP_DHAZ_3C00_HIST_REG14

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x1d0	h_rgb_iir29 Hist rgb iir reg 29 data
15:10	RO	0x0	reserved
9:0	RO	0x1c0	h_rgb_iir28 Hist rgb iir reg 28 data

ISP_DHAZ_3C00_HIST_REG15

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x1f0	h_rgb_iir31 Hist rgb iir reg 31 data
15:10	RO	0x0	reserved
9:0	RO	0x1e0	h_rgb_iir30 Hist rgb iir reg 30 data

ISP_DHAZ_3C00_HIST_REG16

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x210	h_rgb_iir33 Hist rgb iir reg 33 data
15:10	RO	0x0	reserved
9:0	RO	0x200	h_rgb_iir32 Hist rgb iir reg 32 data

ISP_DHAZ_3C00_HIST_REG17

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x230	h_rgb_iir35 Hist rgb iir reg 35 data
15:10	RO	0x0	reserved
9:0	RO	0x220	h_rgb_iir34 Hist rgb iir reg 34 data

ISP_DHAZ_3C00_HIST_REG18

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x250	h_rgb_iir37 Hist rgb iir reg 37 data
15:10	RO	0x0	reserved
9:0	RO	0x240	h_rgb_iir36 Hist rgb iir reg 36 data

ISP_DHAZ_3C00_HIST_REG19

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x270	h_rgb_iir39 Hist rgb iir reg 39 data
15:10	RO	0x0	reserved
9:0	RO	0x260	h_rgb_iir38 Hist rgb iir reg 38 data

ISP_DHAZ_3C00_HIST_REG20

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x290	h_rgb_iir41 Hist rgb iir reg 41 data
15:10	RO	0x0	reserved
9:0	RO	0x280	h_rgb_iir40 Hist rgb iir reg 40 data

ISP_DHAZ_3C00_HIST_REG21

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x2b0	h_rgb_iir43 Hist rgb iir reg 43 data
15:10	RO	0x0	reserved
9:0	RO	0x2a0	h_rgb_iir42 Hist rgb iir reg 42 data

ISP_DHAZ_3C00_HIST_REG22

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x2d0	h_rgb_iir45 Hist rgb iir reg 45 data
15:10	RO	0x0	reserved
9:0	RO	0x2c0	h_rgb_iir44 Hist rgb iir reg 44 data

ISP_DHAZ_3C00_HIST_REG23

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x2f0	h_rgb_iir47 Hist rgb iir reg 47 data
15:10	RO	0x0	reserved
9:0	RO	0x2e0	h_rgb_iir46 Hist rgb iir reg 46 data

ISP_DHAZ_3C00_HIST_REG24

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x310	h_rgb_iir49 Hist rgb iir reg 49 data
15:10	RO	0x0	reserved
9:0	RO	0x300	h_rgb_iir48 Hist rgb iir reg 48 data

ISP_DHAZ_3C00_HIST_REG25

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x330	h_rgb_iir51 Hist rgb iir reg 51 data
15:10	RO	0x0	reserved
9:0	RO	0x320	h_rgb_iir50 Hist rgb iir reg 50 data

ISP_DHAZ_3C00_HIST_REG26

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x350	h_rgb_iir53 Hist rgb iir reg 53 data
15:10	RO	0x0	reserved
9:0	RO	0x340	h_rgb_iir52 Hist rgb iir reg 52 data

ISP_DHAZ_3C00_HIST_REG27

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x370	h_rgb_iir55 Hist rgb iir reg 55 data
15:10	RO	0x0	reserved
9:0	RO	0x360	h_rgb_iir54 Hist rgb iir reg 54 data

ISP_DHAZ_3C00_HIST_REG28

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x390	h_rgb_iir57 Hist rgb iir reg 57 data
15:10	RO	0x0	reserved
9:0	RO	0x380	h_rgb_iir56 Hist rgb iir reg 56 data

ISP_DHAZ_3C00_HIST_REG29

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x3b0	h_rgb_iir59 Hist rgb iir reg 59 data
15:10	RO	0x0	reserved
9:0	RO	0x3a0	h_rgb_iir58 Hist rgb iir reg 58 data

ISP_DHAZ_3C00_HIST_REG30

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x3d0	h_rgb_iir61 Hist rgb iir reg 61 data
15:10	RO	0x0	reserved
9:0	RO	0x3c0	h_rgb_iir60 Hist rgb iir reg 60 data

ISP_DHAZ_3C00_HIST_REG31

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RO	0x3f0	h_rgb_iir63 Hist rgb iir reg 63 data
15:10	RO	0x0	reserved
9:0	RO	0x3e0	h_rgb_iir62 Hist rgb iir reg 62 data

12.4.2.15 3DLUT

ISP_3DLUT_3E00_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_lut3d_en_shd
30	RO	0x0	lut3d_working 1'b0: Module not working 1'b1: Module working
29:2	RO	0x0000000	reserved
1	RW	0x0	sw_lut3d_bypass_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_lut3d_en 1'b0: Disable 1'b1: Enable

ISP_3DLUT_3E00_UPDATE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_lut3d_lut_update_en LUT3D lut update pulse signal 1'b0: Disable 1'b1: Enable

12.4.2.16 SELF_RESIZE

SELF_RESIZE_0C00_1000_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	auto_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
8	RW	0x0	cfg_upd 1'b0: Nothing happens 1'b1: Update shadow registers read: Always 0
7	RW	0x0	scale_vc_up 1'b1: Vertical chrominance upscaling selected 1'b0: Vertical chrominance downscaling selected
6	RW	0x0	scale_vy_up 1'b1: Vertical luminance upscaling selected 1'b0: Vertical luminance downscaling selected

Bit	Attr	Reset Value	Description
5	RW	0x0	scale_hc_up 1'b1: Horizontal chrominance upscaling selected 1'b0: Horizontal chrominance downscaling selected
4	RW	0x0	scale_hy_up 1'b1: Horizontal luminance upscaling selected 1'b0: Horizontal luminance downscaling selected
3	RW	0x0	scale_vc_enable 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	scale_vy_enable 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	scale_hc_enable 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	scale_hy_enable 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

SELF_RESIZE_0C00_1000_SCALE_HY

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_hy This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor. --- SRSZ_SCALE_HY --- Note: The size of the output picture is calculated as follows: Upscaling: (size_in - 1) / (size_out - 1)) = scale downscaling: (size_out - 1) / (size_in - 1)) = scale, where size_in/out is the width or height of the in/output picture. The value of the respective SRSZ_SCALE register then has to be int(scale x 2^14) for upscaling and int(scale x 2^14)+1 for downscaling. For downscaling this formula has no restriction. In upscaling processes the limit is factor 5. If a format conversion is performed, the scale factors have to be different for the luminance and the chrominance component, respectively. For example, for a format conversion from 4:2:2 to 4:2:0 the scale register value for the vertical chrominance component should be half of the vertical luminance scale register value.

SELF_RESIZE_0C00_1000_SCALE_HCB

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_hcb This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.

SELF_RESIZE_0C00_1000_SCALE_HCR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	scale_hcr This register is set to the horizontal Cr downscale factor or to the reciprocal of the horizontal Cr upscale factor.

SELF_RESIZE_0C00_1000_SCALE_VY

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_vy This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.

SELF_RESIZE_0C00_1000_SCALE_VC

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	scale_vc This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.

SELF_RESIZE_0C00_1000_PHASE_HY

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_hy This register is set to the horizontal luminance phase offset.

SELF_RESIZE_0C00_1000_PHASE_HC

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_hc This register is set to the horizontal chrominance phase offset.

SELF_RESIZE_0C00_1000_PHASE_VY

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_vy This register is set to the vertical luminance phase offset.

SELF_RESIZE_0C00_1000_PHASE_VC

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	phase_vc This register is set to the vertical chrominance phase offset.

SELF_RESIZE_0C00_1000_SCALE_LUT_ADDR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	scale_lut_addr Pointer to entry of lookup table

SELF_RESIZE_0C00_1000_SCALE_LUT

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	scale_lut Entry of lookup table at position scale_lut_addr. The lookup table must be filled with appropriate values before the up- scaling functionality can be used.

SELF_RESIZE_0C00_1000_CTRL_SHD

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	scale_vc_up_shd 1'b1: Vertical chrominance upscaling selected 1'b0: Vertical chrominance downscaling selected
6	RO	0x0	scale_vy_up_shd 1'b1: Vertical luminance upscaling selected 1'b0: Vertical luminance downscaling selected
5	RO	0x0	scale_hc_up_shd 1'b1: Horizontal chrominance upscaling selected 1'b0: Horizontal chrominance downscaling selected
4	RO	0x0	scale_hy_up_shd 1'b1: Horizontal luminance upscaling selected 1'b0: Horizontal luminance downscaling selected
3	RO	0x0	scale_vc_enable_shd 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RO	0x0	scale_vy_enable_shd 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RO	0x0	scale_hc_enable_shd 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RO	0x0	scale_hy_enable_shd 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

SELF_RESIZE_0C00_1000_SCALE_HY_SHD

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hy_shd This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor.

SELF_RESIZE_0C00_1000_SCALE_HCB_SHD

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hcb_shd This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.

SELF_RESIZE_0C00_1000_SCALE_HCR_SHD

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_hcr_shd This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor.

SELF_RESIZE_0C00_1000_SCALE_VY_SHD

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_vy_shd This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.

SELF_RESIZE_0C00_1000_SCALE_VC_SHD

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	scale_vc_shd This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.

SELF_RESIZE_0C00_1000_PHASE_HY_SHD

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_hy_shd This register is set to the horizontal luminance phase offset.

SELF_RESIZE_0C00_1000_PHASE_HC_SHD

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_hc_shd This register is set to the horizontal chrominance phase offset.

SELF_RESIZE_0C00_1000_PHASE_VY_SHD

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_vy_shd This register is set to the vertical luminance phase offset.

SELF_RESIZE_0C00_1000_PHASE_VC_SHD

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	phase_vc_shd This register is set to the vertical chrominance phase offset.

12.4.2.17 ISP_TOP

ISP_0400_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_noc_hurry_value 2'b00: The Low priority 2'b01: The 3th High priority 2'b10: The 2nd High priority 2'b11: The first High priority
29	RW	0x0	sw_cgc_ratio_en cgc ratio mode: 1:ration use 219/224 ; 0 : ration use
28	RW	0x0	sw_cgc_yuv_limit yuv cgc enable: 1:limit range; 0:full range(bypass);
27:24	RW	0x0	sw_noc_hurry_w1_mode ibuf0-S RW-channel, 3bit: hurry_req assert high when left waterlevel<(hurry_w1_mode/16) fifo empty, recommended value=0x4;
23:21	RW	0x0	sw_noc_hurry_w0_mode lafifo Wr-channel, 3bit: hurry_req assert high when left waterlevel<(hurry_w1_mode/8) fifo empty, recommended value=0x4;
20:18	RW	0x0	sw_noc_hurry_r_mode lafifo wr-channel, 3bit: hurry_req assert high when left waterlevel<(hurry_w1_mode/8) fifo empty, recommended value=0x4;
17	RO	0x0	reserved
16	RW	0x0	sw_en_12bit_unpack isp_dma: raw16to12->isp(unpack csi-raw12, 8-8-4/4)
15	RW	0x0	sw_en_12bit_packed isp_dma: raw16to12->isp(pack csi-raw12, 8-8-4/4)
14	RW	0x1	sw_csm_c_range Color Space Matrix chrominance clipping range for ISP output 1'b0: CbCr range 64..960 (16..240) according to ITU-R BT.601 standard 1'b1: Full UV range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly
13	RW	0x1	sw_csm_y_range Color Space Matrix luminance clipping range for ISP output 1'b0: Y range 64..940 (16..235) according to ITU-R BT.601 standard 1'b1: Full Y range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly

12	RW	0x0	sw_flash_mode 1'b0: Sensor interface works independently from flash control unit 1'b1: One frame is captured when signaled by flash control unit
11	RO	0x0	reserved
10	WO	0x0	sys_cfg_gen_upd 1: Generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
9	WO	0x0	sys_cfg_force_upd 1: Immediately configure (update) shadow registers, write only
8	RW	0x0	sys_cfg_gen_upd_fix 1: Permanent configure (update) shadow registers on frame end
7	RW	0x0	isp_awb_enable Auto white balance ON/OFF
6	RW	0x0	sw_gamma_in_enable Sensor De-gamma ON/OFF
5	RO	0x0	reserved
4	RW	0x0	sw_inform_enable 1'b1: Input formatter enabled 1'b0: Input formatter disabled The ISP input formatter is enabled or disabled by this bit immediately, but always starts or stops acquisition frame synchronously
3:1	RW	0x0	sw_isp_mode 3'b000 - RAW picture with BT.601 sync (ISP bypass) 3'b001 - ITU-R BT.656 (YUV with embedded sync) 3'b010 - ITU-R BT.601 (YUV input with H and Vsync signals) 3'b011 - Bayer RGB processing with H and Vsync signals 3'b100 - data mode (ISP bypass, sync signals interpreted as data enable) 3'b101 - Bayer RGB processing with BT.656 synchronization 3'b110 - RAW picture with ITU-R BT.656 synchronization (ISP bypass) 3'b111 - Reserved Side effect: If RAW, BT.601, BT.656, or data mode is selected, the clock of the ISP SRAMs (ISP line buffer, Lens Shading, Bad Pixel) is switched off. Only in Bayer RGB mode the clock to the SRAMs is enabled. This further reduces power consumption

0	RW	0x0	sw_isp_enable 1'b1: ISP data output enabled 1'b0: ISP data output disabled Controls output formatter frame synchronously, if isp_gen_cfg_upd is used to activate this bit. For immediate update isp_cfg_upd must be used. --- ISP_CTRL --- Note: Partly write-only

ISP_0400_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_bigmode_mode bigmode_mode 1:use bigmode force_en 0:bigmode_auto(>2560 auto use bigmode)
28	RW	0x0	sw_bigmode_force_en bigmode force enable
27	W1C	0x1	sys_raw3d_fst_frame 3drawnr 1st_frame pulse signal
26	W1C	0x1	sys_cnr_fst_frame cnr 1st_frame pulse signal
25	W1C	0x1	sys_dhaz_fst_frame dhaz 1st_frame pulse signal
24	W1C	0x1	sys_adrc_fst_frame adrc 1st_frame pulse signal
23	W1C	0x1	sys_ynr_fst_frame ynr 1st_frame pulse signal
22	RW	0x0	sw_bt_1120_yc_swap sw_bt_1120_yc_swap old dvp for ccir656, not ues now
21	RW	0x0	sw_dualedge_en sw_dualedge_en old dvp for ccir656, not ues now
20	RW	0x0	sw_bt1120_en 1'b0: Disable bt1120 mode 1'b1: Enable bt1120 mode old dvp for ccir656, not ues now
19:17	RO	0x0	reserved
16	RW	0x0	sw_yuv_dma_sel 1'b0: Use align or conversion data for isp_is input. 1'b1: Use dma yuv read data for isp_is input
15	RW	0x0	sw_rgb_dma_sel 1'b0: Use input formatter data for latency fifo. 1'b1: Use dma rgb read data for latency fifo
14:12	RW	0x0	sw_input_selection 3'b000 - 12Bit external Interface 3'b001 - 10Bit Interface, append 2 zeroes as LSBs 3'b010 - 10Bit Interface, append 2 MSBs as LSBs 3'b011 - 8Bit Interface, append 4 zeroes as LSBs 3'b100 - 8Bit Interface, append 4 MSBs as LSBs 3'b101~111 - Reserved
11	RW	0x0	sw_field_inv 1: Swap odd and even fields 0: do not swap fields old dvp for ccir656, not ues now

10:9	RW	0x0	sw_field_selection 2'b00: Sample all fields (do not care about fields) 2'b01: Sample only even fields 2'b10: Sample only odd fields 2'b11: Reserved old dvp for ccir656, not ues now
8:7	RW	0x0	sw_ccir_seq 2'b00: YCbYCr 2'b01: YCrYCb 2'b10: CbYCrY 2'b11: CrYCbY old dvp for ccir656, not ues now
6:5	RW	0x3	sw_conv_422 2'b00 - Co-sited color subsampling Y0Cb0Cr0 –Y1 2'b01 - Interleaved color subsampling Y0Cb0 –Y1Cr1 (not recommended) 2'b10 - Non-cosited color subsampling Y0Cb(0+1)/2 – Y1Cr(0+1)/2 2'b11 - UV 1/2 sample (drop mode)
4:3	RW	0x0	sw_bayer_pat color components from sensor, starting with top left position in sampled frame (reprogram with ISP_ACQ_H_OFFS, ISP_ACQ_V_OFFS) 2'b00 - First line: RGRG..., second line: GBGB..., etc. 2'b01 - First line: GRGR..., second line: BGBG..., etc. 2'b10 - First line: GBGB..., second line: RGRG..., etc. 2'b11 - First line: BGBG..., second line: GRGR..., etc. This configuration applies for the black level area after cropping by the input formatter
2	RW	0x0	sw_vsync_pol vertical sync polarity 1'b0: High active 1'b1: Low active old dvp for ccir656, not ues now
1	RW	0x0	sw_hsync_pol horizontal sync polarity 1'b0: High active 1'b1: Low active old dvp for ccir656, not ues now
0	RO	0x0	reserved

ISP_0400_ACQ_H_OFFS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	sw_sensor_mode multi-sensor mode(outside sensor nums): 0:one sensor 1:two sensor 2:four sensor
29:28	RW	0x0	sw_sensor_index multi-sensor index used, 0:sensor0-index; 1:sensor1 index then same as sensor_id in old version
27:15	RO	0x0	reserved
14:0	RW	0x0000	sw_acq_h_offs horizontal sample offset in 8-bit samples (yuv: 4 samples=2pix)

ISP_0400_ACQ_V_OFFS

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_acq_v_offs vertical sample offset in lines

ISP_0400_ACQ_H_SIZE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	sw_acq_h_size_bay3dmi sw_acq_h_size_bay3dmi for bay3d size config, when not config, hardware will auto-calc;
15	RO	0x0	reserved
14:0	RW	0x1000	sw_acq_h_size horizontal sample size in 12-bit samples YUV input: 2 samples = 1 pixel, else 1 sample = 1 pixel; So in YUV mode ACQ_H_SIZE must be twice as large as horizontal image size horizontal image size must always be even exept in raw picture mode; If an odd size is programmed the value will be truncated to even size

ISP_0400_ACQ_V_SIZE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0c00	sw_acq_v_size vertical sample size in lines

ISP_0400_ACQ_NR_FRAMES

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	sw_acq_nr_frames number of input frames to be sampled (0 = continuous)

ISP_0400_GAMMA_DX_LO

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x4	sw_gamma_dx8 gamma curve sample point definition x-axis (input)
27	RO	0x0	reserved
26:24	RW	0x4	sw_gamma_dx7 gamma curve sample point definition x-axis (input)
23	RO	0x0	reserved
22:20	RW	0x4	sw_gamma_dx6 gamma curve sample point definition x-axis (input)
19	RO	0x0	reserved
18:16	RW	0x4	sw_gamma_dx5 gamma curve sample point definition x-axis (input)
15	RO	0x0	reserved
14:12	RW	0x4	sw_gamma_dx4 gamma curve sample point definition x-axis (input)
11	RO	0x0	reserved
10:8	RW	0x4	sw_gamma_dx3 gamma curve sample point definition x-axis (input)
7	RO	0x0	reserved
6:4	RW	0x4	sw_gamma_dx2 gamma curve sample point definition x-axis (input)
3	RO	0x0	reserved
2:0	RW	0x4	sw_gamma_dx1 gamma curve sample point definition x-axis (input)

ISP_0400_GAMMA_DX_HI

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x4	sw_gamma_dx16 gamma curve sample point definition x-axis (input)
27	RO	0x0	reserved
26:24	RW	0x4	sw_gamma_dx15 gamma curve sample point definition x-axis (input)
23	RO	0x0	reserved
22:20	RW	0x4	sw_gamma_dx14 gamma curve sample point definition x-axis (input)
19	RO	0x0	reserved
18:16	RW	0x4	sw_gamma_dx13 gamma curve sample point definition x-axis (input)
15	RO	0x0	reserved
14:12	RW	0x4	sw_gamma_dx12 gamma curve sample point definition x-axis (input)
11	RO	0x0	reserved
10:8	RW	0x4	sw_gamma_dx11 gamma curve sample point definition x-axis (input)
7	RO	0x0	reserved
6:4	RW	0x4	sw_gamma_dx10 gamma curve sample point definition x-axis (input)
3	RO	0x0	reserved
2:0	RW	0x4	sw_gamma_dx9 gamma curve sample point definition x-axis (input)

ISP_0400_GAMMA_R_Y_0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_r_y0 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_r_y1 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_2

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_r_y2 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_3

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_r_y3 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_4

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_r_y4 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_5

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x500	sw_gamma_r_y5 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_6

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x600	sw_gamma_r_y6 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_7

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x700	sw_gamma_r_y7 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_8

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x800	sw_gamma_r_y8 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_9

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x900	sw_gamma_r_y9 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_10

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xa00	sw_gamma_r_y10 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_11

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xb00	sw_gamma_r_y11 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_12

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_r_y12 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_13

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xd00	sw_gamma_r_y13 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_14

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xe00	sw_gamma_r_y14 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_15

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xf00	sw_gamma_r_y15 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_R_Y_16

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_r_y16 gamma curve point definition y-axis (output) for red RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_g_y0 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_1

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_g_y1 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_2

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_g_y2 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_3

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_g_y3 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_4

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_g_y4 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_5

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x500	sw_gamma_g_y5 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_6

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x600	sw_gamma_g_y6 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_7

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x700	sw_gamma_g_y7 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_8

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x800	sw_gamma_g_y8 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_9

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x900	sw_gamma_g_y9 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_10

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xa00	sw_gamma_g_y10 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_11

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xb00	sw_gamma_g_y11 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_12

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_g_y12 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_13

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xd00	sw_gamma_g_y13 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_14

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xe00	sw_gamma_g_y14 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_15

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xf00	sw_gamma_g_y15 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_G_Y_16

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_g_y16 gamma curve point definition y-axis (output) for green RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_0

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_b_y0 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_1

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_b_y1 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_2

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_b_y2 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_3

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_b_y3 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_4

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_b_y4 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_5

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x500	sw_gamma_b_y5 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_6

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x600	sw_gamma_b_y6 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_7

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x700	sw_gamma_b_y7 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_8

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x800	sw_gamma_b_y8 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_9

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x900	sw_gamma_b_y9 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_10

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xa00	sw_gamma_b_y10 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_11

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xb00	sw_gamma_b_y11 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_12

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_b_y12 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_13

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xd00	sw_gamma_b_y13 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_14

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xe00	sw_gamma_b_y14 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_15

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xf00	sw_gamma_b_y15 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_GAMMA_B_Y_16

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_b_y16 gamma curve point definition y-axis (output) for blue RESTRICTION: Each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed!)

ISP_0400_AWB_GAIN0_G

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0100	sw_awb_gain0_gr gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0100	sw_awb_gain0_gb gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part

ISP_0400_AWB_GAIN0_RB

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0100	sw_awb_gain0_r gain value for red component 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0100	sw_awb_gain0_b gain value for blue component 100h = 1, unsigned integer value, range 0 to 63with 8 bit fractional part

ISP_0400_AWB_GAIN1_G

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_awb_gain1_gr gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_awb_gain1_gb gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part

ISP_0400_AWB_GAIN1_RB

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_awb_gain1_r gain value for red component 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_awb_gain1_b gain value for blue component 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part

ISP_0400_AWB_GAIN2_G

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_awb_gain2_gr gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_awb_gain2_gb gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part

ISP_0400_AWB_GAIN2_RB

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_awb_gain2_r gain value for red component 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_awb_gain2_b gain value for blue component 100h = 1, unsigned integer value, range 0 to 63 with 8 bit fractional part

ISP_0400_CC_COEFF_0

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_csm_y_offset If this signal is 0, will use old function(Y = f(coe_x) + 0/16). If this signal is not 0, Y = f(coe_x) + sw_csm_y_offset
23:16	RW	0x00	sw_csm_c_offset If this signal is 0, will use old function(Cb/r = f(coe_x) + 128). If this signal is not 0, Cb/r = f(coe_x) + sw_csm_c_offset
15:9	RO	0x0	reserved
8:0	RW	0x021	sw_csm_coeff0 coefficient 0 for color space conversion --- ISP_CC_COEFF_0 --- Note: All color conversion coefficients are signed integer values with 7 bit fractional part, range -2 to 1.992

ISP_0400_CC_COEFF_1

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x040	sw_csm_coeff1 coefficient 1 for color space conversion

ISP_0400_CC_COEFF_2

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x00d	sw_csm_coeff2 coefficient 2 for color space conversion

ISP_0400_CC_COEFF_3

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x1ed	sw_csm_coeff3 coefficient 3 for color space conversion

ISP_0400_CC_COEFF_4

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x1db	sw_csm_coeff4 coefficient 4 for color space conversion

ISP_0400_CC_COEFF_5

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x038	sw_csm_coeff5 coefficient 5 for color space conversion

ISP_0400_CC_COEFF_6

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x038	sw_csm_coeff6 coefficient 6 for color space conversion

ISP_0400_CC_COEFF_7

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x1d1	sw_csm_coeff7 coefficient 7 for color space conversion

ISP_0400_CC_COEFF_8

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x1f7	sw_csm_coeff8 coefficient 8 for color space conversion

ISP_0400_OUT_H_OFFS

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_out_h_offs vertical pic offset in lines

ISP_0400_OUT_V_OFFS

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	sw_out_v_offs vertical pic offset in lines

ISP_0400_OUT_H_SIZE

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x1000	sw_out_h_size horizontal picture size in pixel if ISP_MODE is set to 3'b001: ITU-R BT.656 YUV 3'b010: ITU-R BT.601 YUV 3'b011: ITU-R BT.601 Bayer RGB 3'b101: ITU-R BT.656 Bayer RGB only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the 422 output. (If an odd size is programmed the value will be truncated to even size)

ISP_0400_OUT_V_SIZE

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0c00	sw_out_v_size vertical pic size in lines

ISP_0400_FLAGS_SHD

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31	RO	0x0	s_hsync state of ISP input port s_hsync, for test purposes
30	RO	0x0	s_vsync state of ISP input port s_vsync, for test purposes
29:28	RO	0x0	reserved
27:16	RO	0x000	s_data state of ISP input port s_data, for test purposes
15:3	RO	0x0	reserved
2	RO	0x0	inform_field current field information (0=odd, 1=even)
1	RO	0x0	isp_inform_enable_shd Input formatter enable shadow register
0	RO	0x0	isp_enable_shd ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)

ISP_0400_OUT_H_OFFS_SHD

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	isp_out_h_offs_shd current vertical pic offset in lines

ISP_0400_OUT_V_OFFS_SHD

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	isp_out_v_offs_shd current vertical pic offset in lines

ISP_0400_OUT_H_SIZE_SHD

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RO	0x0000	isp_out_h_size_shd current horizontal pic size in pixel

ISP_0400_OUT_V_SIZE_SHD

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	isp_out_v_size_shd vertical pic size in lines

ISP_0400_ISP_IMSC

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_imsc_gain_done 1, enable interrupt 0, mask out
21	RW	0x0	sw_imsc_dhaz_done 1, enable interrupt 0, mask out
20	RW	0x0	sw_imsc_hdr_done 1, enable interrupt 0, mask out
19	RW	0x0	sw_imsc_out_quarter out_size = 0.25
18	RW	0x0	sw_imsc_exp_end 1, enable interrupt 0, mask out
17	RW	0x0	sw_imsc_flash_cap 1, enable interrupt 0, mask out
16	RW	0x0	sw_imsc_lsc_lut_err 1, enable interrupt 0, mask out
15	RW	0x0	sw_imsc_hist_measure_rdy 1, enable interrupt 0, mask out
14	RW	0x0	sw_imsc_afm_fin 1, enable interrupt 0, mask out
13	RW	0x0	sw_imsc_afm_lum_of 1, enable interrupt 0, mask out
12	RW	0x0	sw_imsc_afm_sum_of 1, enable interrupt 0, mask out
11	RW	0x0	sw_imsc_shutter_off 1, enable interrupt 0, mask out
10	RW	0x0	sw_imsc_shutter_on 1, enable interrupt 0, mask out
9	RW	0x0	sw_imsc_flash_off 1, enable interrupt 0, mask out
8	RW	0x0	sw_imsc_flash_on 1, enable interrupt 0, mask out

7	RW	0x0	sw_imsc_h_start 1, enable interrupt 0, mask out
6	RW	0x0	sw_imsc_v_start 1, enable interrupt 0, mask out
5	RW	0x0	sw_imsc_frame_in 1, enable interrupt 0, mask out
4	RW	0x0	sw_imsc_awb_done 1, enable interrupt 0, mask out
3	RW	0x0	sw_imsc_pic_size_err 1, enable interrupt 0, mask out
2	RW	0x0	sw_imsc_data_loss 1, enable interrupt 0, mask out
1	RW	0x0	sw_imsc_frame 1, enable interrupt 0, mask out
0	RW	0x0	sw_imsc_isp_off 1, enable interrupt 0, mask out

ISP_0400_ISP_RIS

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RO	0x0	ris_gain_done GAIN module error flag, high valid
21	RO	0x0	ris_dhaz_done DHAZ module complete, high valid
20	RO	0x0	ris_hdr_done HDR module complete, high valid
19	RW	0x0	ris_out_quarter out_size = 0.25
18	RO	0x0	ris_exp_end Exposure measurement complete, high valid
17	RO	0x0	ris_flash_cap Signaling captured frame, high valid
16	RO	0x0	ris_lsc_lut_err LSC and RAWLSC LUT udpate error, high valid
15	RO	0x0	ris_hist_measure_rdy Histogram measurement ready. (Old or new histogram measurement), high valid
14	RO	0x0	ris_afm_fin AF measurement finished: This interrupt is set when the first complete frame is calculated after enabling the AF measurement, high valid
13	RO	0x0	ris_afm_lum_of Auto focus luminance overflow, high valid
12	RO	0x0	ris_afm_sum_of Auto focus sum overflow, high valid
11	RO	0x0	ris_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	ris_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	ris_flash_off Flash light is switched off, high valid
8	RO	0x0	ris_flash_on Flash light is switched on, high valid
7	RO	0x0	ris_h_start Start edge of h_sync, high valid
6	RO	0x0	ris_v_start Start edge of v_sync, high valid
5	RO	0x0	ris_frame_in sampled input frame is complete, high valid
4	RO	0x0	ris_awb_done White balancing measurement cycle is complete, results can be read out, high valid

3	RO	0x0	ris_pic_size_err pic size violation occurred, programming seems wrong, high valid
2	RO	0x0	ris_data_loss loss of data occurred within a line, processing failure, high valid
1	RO	0x0	ris_frame frame was completely put out, high valid
0	RO	0x0	ris_isp_off isp output was disabled (vsynced) due to f_cnt reached or manual, high valid

ISP_0400_ISP_MIS
Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RO	0x0	mis_gain_done GAIN module done flag, high valid
21	RO	0x0	mis_dhaz_done DHAZ module complete, high valid
20	RO	0x0	mis_hdr_done HDR module complete, high valid
19	RW	0x0	mis_out_quarter out_size = 0.25
18	RO	0x0	mis_exp_end Exposure measurement complete, high valid
17	RO	0x0	mis_flash_cap Captured is frame is detected, high valid
16	RO	0x0	mis_lsc_lut_err LSC and RAWLSC LUT udpate error, high valid
15	RO	0x0	mis_hist_measure_rdy Histogram measurement ready. (Old or new histogram measurement), high valid
14	RO	0x0	mis_afm_fin AF measurement finished: This interrupt is set when the first complete frame is calculated after enabling the AF measurement, high valid
13	RO	0x0	mis_afm_lum_of Luminance overflow, high valid
12	RO	0x0	mis_afm_sum_of Sum overflow, high valid
11	RO	0x0	mis_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	mis_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	mis_flash_off Flash light is switched off, high valid
8	RO	0x0	mis_flash_on Flash light is switched on, high valid
7	RO	0x0	mis_h_start Start edge of h_sync, high valid
6	RO	0x0	mis_v_start Start edge of v_sync, high valid
5	RO	0x0	mis_frame_in sampled input frame is complete, high valid
4	RO	0x0	mis_awb_done White balancing measurement cycle is complete, results can be read out, high valid

3	RO	0x0	mis_pic_size_err pic size violation occurred, programming seems wrong, high valid
2	RO	0x0	mis_data_loss loss of data occurred within a line, processing failure, high valid
1	RO	0x0	mis_frame frame was completely put out, high valid each MIS[31:0] signals high, set IRQ;
0	RO	0x0	mis_isp_off isp was turned off (vsynced) due to f_cnt reached or manual, high valid each MIS[31:0] signals high, set IRQ;

ISP_0400_ISP_ICR
Address: Operational Base + offset (0x01c8)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	sys_icr_gain_done clear interrupt
21	WO	0x0	sys_icr_dhaz_done clear interrupt
20	WO	0x0	sys_icr_hdr_done clear interrupt
19	RW	0x0	sys_icr_out_quarter clear interrupt
18	WO	0x0	sys_icr_exp_end clear interrupt
17	WO	0x0	sys_icr_flash_cap clear interrupt
16	WO	0x0	sys_icr_lsc_lut_err clear interrupt
15	WO	0x0	sys_icr_hist_measure_rdy clear interrupt
14	WO	0x0	sys_icr_afm_fin clear interrupt
13	WO	0x0	sys_icr_afm_lum_of clear interrupt
12	WO	0x0	sys_icr_afm_sum_of clear interrupt
11	WO	0x0	sys_icr_shutter_off clear interrupt
10	WO	0x0	sys_icr_shutter_on clear interrupt
9	WO	0x0	sys_icr_flash_off clear interrupt
8	WO	0x0	sys_icr_flash_on clear interrupt
7	WO	0x0	sys_icr_h_start clear interrupt
6	WO	0x0	sys_icr_v_start clear interrupt
5	WO	0x0	sys_icr_frame_in clear interrupt
4	WO	0x0	sys_icr_awb_done clear interrupt
3	WO	0x0	sys_icr_pic_size_err clear interrupt
2	WO	0x0	sys_icr_data_loss clear interrupt

1	WO	0x0	sys_icr_frame clear interrupt
0	WO	0x0	sys_icr_isp_off clear interrupt

ISP_0400_ISP_ISR

Address: Operational Base + offset (0x01cc)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	WO	0x0	sys_isr_gain_done set interrupt
21	WO	0x0	sys_isr_dhaz_done set interrupt
20	WO	0x0	sys_isr_hdr_done set interrupt
19	RW	0x0	sys_isr_out_quarter set interrupt
18	WO	0x0	sys_isr_exp_end set interrupt
17	WO	0x0	sys_isr_flash_cap set interrupt
16	WO	0x0	sys_isr_lsc_lut_err set interrupt
15	WO	0x0	sys_isr_hist_measure_rdy set interrupt
14	WO	0x0	sys_isr_afm_fin set interrupt
13	WO	0x0	sys_isr_afm_lum_of set interrupt
12	WO	0x0	sys_isr_afm_sum_of set interrupt
11	WO	0x0	sys_isr_shutter_off set interrupt
10	WO	0x0	sys_isr_shutter_on set interrupt
9	WO	0x0	sys_isr_flash_off set interrupt
8	WO	0x0	sys_isr_flash_on set interrupt
7	WO	0x0	sys_isr_h_start set interrupt
6	WO	0x0	sys_isr_v_start set interrupt
5	WO	0x0	sys_isr_frame_in set interrupt
4	WO	0x0	sys_isr_awb_done set interrupt
3	WO	0x0	sys_isr_pic_size_err set interrupt
2	WO	0x0	sys_isr_data_loss set interrupt

1	WO	0x0	sys_isr_frame set interrupt
0	WO	0x0	sys_isr_isp_off set interrupt

ISP_0400_ISP3A_IMSC

Address: Operational Base + offset (0x01d0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	sw_imsc_sws_3a_ddr_done 1, enable interrupt 0, mask out
11	RW	0x0	sw_imsc_rawawb_done 1, enable interrupt 0, mask out
10	RW	0x0	sw_imsc_rawaf_done 1, enable interrupt 0, mask out
9	RW	0x0	sw_imsc_rawaf_lum_of 1, enable interrupt 0, mask out
8	RW	0x0	sw_imsc_rawaf_sum_of 1, enable interrupt 0, mask out
7	RW	0x0	sw_imsc_rawhist_ch2_done 1, enable interrupt 0, mask out
6	RW	0x0	sw_imsc_rawhist_ch1_done 1, enable interrupt 0, mask out
5	RW	0x0	sw_imsc_rawhist_ch0_done 1, enable interrupt 0, mask out
4	RW	0x0	sw_imsc_rawhist_big_done 1, enable interrupt 0, mask out
3	RW	0x0	sw_imsc_rawae_ch2_done 1, enable interrupt 0, mask out
2	RW	0x0	sw_imsc_rawae_ch1_done 1, enable interrupt 0, mask out
1	RW	0x0	sw_imsc_rawae_ch0_done 1, enable interrupt 0, mask out
0	RW	0x0	sw_imsc_rawae_big_done 1, enable interrupt 0, mask out

ISP_0400_ISP3A_RIS

Address: Operational Base + offset (0x01d4)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	ris_sws_3a_ddr_done 3a result write to ddr done flag
11	RO	0x0	ris_rawawb_done RAWAWB module complete
10	RO	0x0	ris_rawaf_done RAWAF module complete
9	RO	0x0	ris_rawaf_lum_of Auto focus luminance overflow
8	RO	0x0	ris_rawaf_sum_of Auto focus sum overflow
7	RO	0x0	ris_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	ris_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	ris_rawhist_ch0_done RAWHIST 0channel complete
4	RO	0x0	ris_rawhist_big_mode RAWHIST BIG module complete
3	RO	0x0	ris_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	ris_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	ris_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	ris_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_MIS

Address: Operational Base + offset (0x01d8)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	mis_sws_3a_ddr_done 3a result write to ddr done flag
11	RO	0x0	mis_rawawb_done RAWAWB module complete
10	RO	0x0	mis_rawaf_done RAWAF module complete
9	RO	0x0	mis_rawaf_lum_of Auto focus luminance overflow
8	RO	0x0	mis_rawaf_sum_of Auto focus sum overflow
7	RO	0x0	mis_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	mis_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	mis_rawhist_ch0_done RAWHIST 0channel complete
4	RO	0x0	mis_rawhist_big_done RAWHIST BIG module complete
3	RO	0x0	mis_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	mis_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	mis_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	mis_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_ICR

Address: Operational Base + offset (0x01dc)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	WO	0x0	sys_icr_sws_3a_ddr_done clear interrupt
11	WO	0x0	sys_icr_rawawb_done clear interrupt
10	WO	0x0	sys_icr_rawaf_done clear interrupt
9	WO	0x0	sys_icr_rawaf_lum_of clear interrupt
8	WO	0x0	sys_icr_rawaf_sum_of clear interrupt
7	WO	0x0	sys_icr_rawhist_ch2_done clear interrupt
6	WO	0x0	sys_icr_rawhist_ch1_done clear interrupt
5	WO	0x0	sys_icr_rawhist_ch0_done clear interrupt
4	WO	0x0	sys_icr_rawhist_big_done clear interrupt
3	WO	0x0	sys_icr_rawae_ch2_done clear interrupt
2	WO	0x0	sys_icr_rawae_ch1_done clear interrupt
1	WO	0x0	sys_icr_rawae_ch0_done clear interrupt
0	WO	0x0	sys_icr_rawae_big_done clear interrupt

ISP_0400_ERR
Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	rawlsc_lut_err this error is generated by RAWLSC LUT config error
3	RO	0x0	lsc_lut_err This error is generated by LSC LUT config error. (This bit will assert high when update this LUT select from DDR mode and can not finish update at vsync period)
2	RO	0x0	outform_size_err size error is generated in outmux submodule
1	RO	0x0	is_size_err size error is generated in image stabilization submodule
0	RO	0x0	inform_size_err size error is generated in inform submodule --- ISP_ERR --- Note: For debug purposes the ISP_ERR und ISP_ERR_CLR are implemented. For the case when a PIC_SIZE_ERR interrupt is signaled the SW is able to see in which submodule this error is generated. Writing to the ISP_ERR_CLR register clears this bit

ISP_0400_ERR_CLR

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	WO	0x0	rawlsc_lut_err_clr this error is cleared
3	WO	0x0	lsc_lut_err_clr this error is cleared
2	WO	0x0	outform_size_err_clr size error is cleared
1	WO	0x0	is_size_err_clr size error is cleared
0	WO	0x0	inform_size_err_clr size error is cleared

ISP_0400_FRAME_COUNT

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RO	0x000	frame_counter Current frame count of processing --- ISP_FRAME_COUNT --- Note: In the ISP_FRAME_COUNT register the number of processed frames are displayed. For example: If a 8 is programmed into the ISP_ACQ_NR_FRAMES register, a read access to the ISP_FRAME_COUNT register during processing of the first picture shows a 7. After the entire frames are processed the ISP_OFF interrupt is generated and the ISP_FRAME_COUNT has the count zero. In case a "0" is programmed into the ISP_ACQ_NR_FRAMES register (continues mode) the ISP_FRAME_COUNT register keeps the value "0".

ISP_0400_DEBUG1

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_fifo_space2full ro_ibuf2_space2full ,ro_ibuf1_space2full ,ro_ibuf0_space2full ,ro_r2fifo_space2full,ro_r1fifo_space2full,ro_r0fifo_space2full,ro_outfifo_space2full,ro_lafifo_space2full;

ISP_0400_DEBUG2

Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	isp_out_line_counter isp_out_line_counter

ISP_0400_DEBUG3

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	isp_pipe_ack mge_val, mge_ack, rawnr_val, rawnr_ack, bay3d_val, bay3d_ack, tmo_val, tmo_ack, gic_val, gic_ack, dbr_val, dbr_ack, debayer_val, debayer_ack, ccm_val, ccm_ack, gamma_out_val, gamma_out_ack, dhaz_val, dhaz_ack, lut3d_val, lut3d_ack, ldch_val, ldch_ack, conv422_val, conv422_ack, ynr_val, ynr_ack, shp_val, shp_ack, cgc_val, cgc_ack, 4'b0, isp_out_val, isp_out_ack, isp_in_val, isp_in_ack

12.4.2.18 FLASH

ISP_FLASH_0660_CMD

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	preflash_on Preflash on 0: No effect 1: Flash delay counter is started at next trigger event. No capture event is signaled to the sensor interface block.
1	WO	0x0	flash_on Flash on 0: No effect 1: Flash delay counter is started at next trigger event. A capture event is signaled to the sensor interface block.
0	WO	0x0	prelight_on Prelight on 0: Prelight is switched off at next trigger event; 1: Prelight is switched on at next trigger event. --- ISP_FLASH_CMD --- Note: This is the command register for flash light and prelight activation. If the "rw" bits (e.g. "fl_cap_del") are re-programmed during operation, the following scheme shall be applied: i) Prelight is active (prelight_on = 1 has been set before): Every write access to this register shall use prelight_on = 1 (to prevent undesired switch off of the prelight). ii) Prelight is off: Every write access to this register shall use prelight_on = 0 (to prevent undesired switch on of the prelight).

ISP_FLASH_0660_CONFIG

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	fl_cap_del Capture delay Frame number (0 to 15) to be captured after trigger event
3	RW	0x0	fl_trig_src Trigger source for flash and prelight 0: Use "vds_vsync" for trigger event (with evaluation of vs_in_edge) 1: Use "fl_trig" for trigger event (positive edge)
2	RW	0x0	fl_pol Polarity of flash related signals 0: flash_trig, prelight_trig are high active; 1: flash_trig, prelight_trig are low active.
1	RW	0x0	vs_in_edge VSYNC edge 0: Use negative edge of "vds_vsync" if generating a trigger event 1: Use positive edge of "vds_vsync" if generating a trigger event
0	RW	0x0	prelight_mode Prelight mode 0: Prelight is switched off at begin of flash; 1: Prelight is switched off at end of flash.

ISP_FLASH_0660_PREDIV

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	fl_pre_div Pre-divider for flush/preflash counter

ISP_FLASH_0660_DELAY

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_delay Counter value for flash/preflash delay open_delay = (fl_delay + 1) * (fl_pre_div + 1) / clk_isp fl_delay = (open_delay*clk_isp) / (fl_pre_div + 1) - 1 --- ISP_FLASH_DELAY --- Note: Example: fl_delay = (10s * 100MHz) / (1023 + 1) - 1 = 976561

ISP_FLASH_0660_TIME

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_time Counter value for flash/preflash time open_time = (fl_time + 1) * (fl_pre_div + 1) / clk_isp fl_time = (open_time * clk_isp) / (fl_pre_div + 1) - 1 --- ISP_FLASH_TIME --- Note: Example: fl_time = (500ms * 100MHz) / (700 + 1) C 1 = 71530

ISP_FLASH_0660_MAXP

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	fl_maxp Maximum period value for flash or preflash max. flash/preflash period = 214 * (fl_maxp + 1) / clk_isp fl_maxp = (max_period * clk_isp) / 214 - 1 --- ISP_FLASH_MAXP --- Note: Example: fl_maxp = (10s * 100MHz) / (16384) - 1 = 61034

12.4.2.19 CTRL

CTRL_0000_VI_ISP_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	isp_ldch_en isp_ldch_en 1'b0: Disable 1'b1: Enable
27	RW	0x0	isp_gain_en isp_gain_en 1'b0: Disable 1'b1: Enable
26	RO	0x0	reserved
25	RW	0x0	isp_imp_en isp_imp_en 1'b0: Disable 1'b1: Enable
24	RW	0x0	isp_eff_en isp_eff_en 1'b0: Disable 1'b1: Enable
23	RO	0x0	reserved
22	RW	0x0	isp_rsz_en isp_rsz_en 1'b0: Disable 1'b1: Enable
21	RW	0x0	isp_cp_en isp_cp_en 1'b0: Disable 1'b1: Enable
20	RW	0x0	isp_awb_en isp_awb_en 1'b0: Disable 1'b1: Enable
19	RO	0x0	reserved
18	RW	0x0	isp_3dlut_en isp_3dlut_en 1'b0: Disable 1'b1: Enable
17	RW	0x0	isp_dhaz_en isp_dhaz_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	isp_rkwdr_en isp_rkwdr_en 1'b0: Disable 1'b1: Enable

15	RW	0x0	isp_gamma12_en isp_gamma12_en 1'b0: Disable 1'b1: Enable
14	RW	0x0	isp_ccm_en isp_ccm_en 1'b0: Disable 1'b1: Enable
13	RW	0x0	isp_debayer_en isp_debayer_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	isp_gic_en isp_gic_en 1'b0: Disable 1'b1:Enable
11	RW	0x0	isp_hdrtmo_en isp_hdrtmo_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	isp_lsc_en isp_lsc_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	isp_rawnr_en isp_rawnr_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	isp_hdrmge_en isp_hdrmge_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	isp_dpcc_en isp_dpcc_en 1'b0: Disable 1'b1: Enable
6	RW	0x0	isp_gamma_in_en isp_gamma_in_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	isp_bls_en isp_bls_en 1'b0: Disable 1'b1: Enable
4:2	RO	0x0	reserved

1	RW	0x0	isp_en_sel select top en ctrl each module 1'b0: Not select 1'b1: Select
0	RW	0x0	vi_ccl_dis isp_top enable for all marvin sub_module 1'b0: isp is disable 1'b1: isp is enable

CTRL_0000_VI_ISP_PATH

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:22	RW	0x0	sw_3a_rawae012_swap rawae(hist)0-1 swap: 2'b00: RAWAE0 for StrmCh0, RAWAE1 for StrmCh1, RAWAE2 for StrmCh2; 2'b01: RAWAE0 for StrmCh1, RAWAE1 for StrmCh0, RAWAE2 for StrmCh2; 2'b10: RAWAE0 for StrmCh2, RAWAE1 for StrmCh1, RAWAE2 for StrmCh0;
21:20	RW	0x0	sw_3a_rawawb_sel 2'b00: dpcc0 2'b01: dpcc1 2'b10: dpcc2
19:18	RW	0x0	sw_3a_rawaf_sel 2'b00: awb0 2'b01: awb1 2'b10: awb2 2'b11: debayer
17:16	RW	0x0	sw_3a_rawae3_sel 2'b00: awb0 2'b01: awb1 2'b10: awb2 2'b11: tmo
15:0	RO	0x0	reserved

CTRL_0000_VI_ID

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x02	ro_isp_version_major major version
23:16	RO	0x00	ro_isp_version_minor minor version
15:0	RO	0x1909	ro_isp_version_date release date

CTRL_0000_VI_ISP_CLK_CTRL

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31	RW	0x0	marvinmi_clk_alwayson marvin_mi processing clock control 1: marvin_mi clk always on 0: clk gate
30	RW	0x0	mipi_clk_alwayson simipi & mipi0 & mipi1 processing clock control 1: mipi clk always on 0: clk gate
29	RW	0x0	rszs_clk_alwayson rszs processing clock control 1: rszs clk always on 0: clk gate
28	RW	0x0	jpeg_clk_alwayson pjeg processing clock control 1: jpeg clk always on 0: clk gate
27	RW	0x0	dpmux_clk_alwayson dpmux processing clock control 1: dpmux clk always on 0: clk gate
26	RW	0x0	rszm_clk_alwayson rszm processing clock control 1: rszm clk always on 0: clk gate
25	RW	0x0	si_clk_alwayson si processing clock control 1: si clk always on 0: clk gate
24	RW	0x0	ie_clk_alwayson iemux & ie processing clock control 1: ie & ie clk always on 0: clk gate
23	RW	0x0	cp_clk_alwayson scp processing clock control 1: cp clk always on 0: clk gate
22	RW	0x0	mi_rawrd_clk_on isp_mi raw read path clk always on 1: Always on 0: Gated
21	RW	0x0	mi_read_clk_on isp_mi dma read clk always on 1: Always on 0: Gated

20	RW	0x0	mi_raw1_clk_on isp_mi raw1 write path clk always on 1: Always on 0: Gated
19	RW	0x0	mi_raw0_clk_on isp_mi raw0 write path clk always on 1: Always on 0: Gated
18	RW	0x0	mi_sp_clk_on isp_mi self path clk always on 1: Always on 0: Gated
17	RW	0x0	mi_y12_clk_on isp_mi y12 path clk always on 1: Always on 0: Gated
16	RW	0x0	mi_dp_clk_on isp_mi dpcc path clk always on 1: Always on 0: Gated
15	RW	0x0	mi_jpeg_clk_on isp_mi jpeg path clk always on 1: Always on 0: Gated
14	RW	0x0	mi_mp_clk_on isp_mi main path clk always on 1: Always on 0: Gated
13	RW	0x0	mi_ldc_clk_on isp_mi ldc path clk always on 1: Always on 0: Gated
12	RW	0x0	ldc_ram_clk_on ldc_ram clock control, for ram 1: ldc_ram clk always on 0: clk gate
11	RW	0x0	aclk_isp_clk_on aclk_isp clock control, for ram 1: aclk_isp clk always on 0: clk gate
10	RW	0x0	jpeg_ram_clk_on jpeg ram clock control 1: jpeg ram clk always on 0: clk gate

9	RW	0x0	rsz_ram_clk_on rsz ram clock control 1: rsz clk always on 0: clk gate
8	RW	0x0	isp_ie_ram_clk_on isp_ie_ram clock control 1: ie_ram clk always on 0: clk gate
7	RW	0x0	isp_dpcc_ram_clk_on isp_dpcc_ram clock control 1: isp_dpcc_ram clk always on 0: clk gate
6	RW	0x0	isp_dem_ram_clk_on isp_dem_ram clock control 1: isp_dem_ram clk always on 0: clk gate
5	RW	0x0	isp_fifo_ram_clk_on isp_fifo_ram clock control 1: isp_fifo_ram clk always on 0: clk gate
4	RW	0x0	mipi_ram_clk_on mipi_ram clock control 1: mipi_ram clk always on 0: clk gate
3	RW	0x0	isp_3a_clk_on 3w processing clock control 1: 3a clk always on 0: clk gate
2	RW	0x0	isp_yuv_clk_on yuv path clock control 1: yuv path clk always on 0: clk gate
1	RW	0x0	isp_rgb_clk_on rgb path clock control 1: rgb path clk always on 0: clk gate
0	RW	0x0	isp_raw_clk_on raw path clock control 1: raw path clk always on 0: clk gate

CTRL_0000_VI_ICCL
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	vi_mpfbc_clk_enable mpfbc clock enable 1: Processing mode 0: Power safe
13:12	RO	0x0	reserved
11	RW	0x1	vi_mipi_clk_enable MIPI interface clock enable 1: Processing mode 0: Power safe
10	RW	0x1	vi_smia_clk_enable SMIA interface clock enable 1: Processing mode 0: Power safe
9	RW	0x1	vi_simp_clk_enable Superimpose clock enable 1: Processing mode 0: Power safe
8	RW	0x1	vi_ie_clk_enable Image effect clock enable 1: Processing mode 0: Power safe
7	RO	0x0	reserved
6	RW	0x1	vi_mi_clk_enable memory interface clock enable 1: Processing mode 0: Power safe
5	RW	0x1	vi_jpeg_clk_enable JPEG encoder clock enable 1: Processing mode 0: Power safe
4	RW	0x1	vi_srsz_clk_enable self picture resize clock enable 1: Processing mode 0: Power safe
3	RW	0x1	vi_mrsz_clk_enable main picture resize clock enable 1: Processing mode 0: Power safe
2	RO	0x0	reserved
1	RW	0x1	vi_cp_clk_enable color processing clock enable 1: Processing mode 0: Power safe

0	RW	0x1	vi_isp_clk_enable isp processing clock enable 1: Processing mode 0: Power safe

CTRL_0000_VI_IRCL
Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	vi_3a_soft_rst 3a software reset 0: Processing mode 1: Reset state 3a can be reset by vi_isp_soft_rst too.
12	RO	0x0	reserved
11	RW	0x0	vi_mipi_soft_rst MIPI Interface software reset 0: Processing mode 1: Reset state
10	RW	0x0	vi_smia_soft_rst SMIA Interface software reset 0: Processing mode 1: Reset state
9	RW	0x0	vi_simp_soft_rst Superimpose software reset 0: Processing mode 1: Reset state
8	RW	0x0	vi_ie_soft_rst Image effect software reset 0: Processing mode 1: Reset state
7	RW	0x0	vi_marvin_rst hardware reset of entire marvin 0: Processing mode 1: Reset state
6	RW	0x0	vi_mi_soft_rst memory interface software reset 0: Processing mode 1: Reset state
5	RW	0x0	vi_jpeg_soft_rst JPEG encoder software reset 0: Processing mode 1: Reset state
4	RW	0x0	vi_srsz_soft_rst Self-picture resize software reset 0: Processing mode 1: Reset state
3	RW	0x0	vi_mrsz_soft_rst Main-picture resize software reset 0: Processing mode 1: Reset state

2	RW	0x0	vi_ycs_soft_rst y/c splitter software reset 0: Processing mode 1: Reset state
1	RW	0x0	vi_cp_soft_rst color processing software reset 0: Processing mode 1: Reset state
0	RW	0x0	vi_isp_soft_rst isp software reset 0: Processing mode 1: Reset state

CTRL_0000_VI_DPCL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	vi_mi_debug_mode vi_mi_debug_mode
13	RW	0x0	vi_old_mi_sel_rd vi_old_mi_sel_rd
12	RW	0x0	vi_old_mi_sel_wr vi_old_mi_sel_wr
11	RW	0x0	vi_dma_spmux 0: Data from camera interface to self resize 1: Data from DMA read port to self resize
10	RW	0x0	vi_dma_iemux 0: Data from camera interface to image effects 1: Data from DMA read port to image effects
9:8	RW	0x0	if_select selects input interface 0: Parallel interface 1: LVDS interface 2: MIPI1-interface 3: Reserved
7	RO	0x0	reserved
6:4	RW	0x0	vi_dma_switch DMA read data path selector 0: Path to SPMUX 1: Path to Superimpose 2: Path to Image Effects 3: Reserved 4: Path to ISP Bayer RGB 5~7: Reserved
3:2	RW	0x0	vi_chan_mode Y/C splitter channel mode 0: Disabled 1: Main path and raw data mode 2: Self path mode 3: Main and self path mode
1:0	RW	0x0	vi_mp_mux data path selector for main path 00: Data from DMA read port to JPEG encoder 01: Data from main resize to MI, uncompressed 10: Data from main resize to JPEG encoder 11: Reserved

CTRL_0000_SWS_CFG

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp2pp_hold isp2pp pipeline hold, read only
30	RO	0x0	sw_sws_en_shd sw_sws_en_shd
29	RO	0x0	sws_working sws_working
28:26	RO	0x0	reserved
25	RW	0x0	sw_mipi2isp_fifo_dis v_blank hold fifo disable
24	RW	0x0	sw_3a_ddr_write_en 3a result load to ddr enable
23:16	RW	0x00	sw_isp2pp_difx16 isp2pp lineconter diff isp_linecnt + sw_isp2pp_difx16*16 >= tnr_linecnt*128, unit=16line; hold mainisp
15:6	RO	0x0	reserved
5:4	RW	0x0	sw_sensor_id current frame sensor id from 0~3
3	RW	0x0	sw_ack_frm_pro_dis vblank optimize disable
2	RW	0x0	sw_mipi_drop_frm_dis mipi drop frame disable 1'b0: Enable, default 1'b1: Disable Note: only mipi on-the-fly mode needs to use drop frame
1	RW	0x0	sw_isp2pp_pipe_en enable pp nodrop frame, use pp_ack into mainisp output
0	RW	0x0	sw_sws_en 1'b0: sws close 1'b1: sws en

CTRL_0000_LVDS_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	sw_lvds_start_y Crop start y.
20:10	RW	0x000	sw_lvds_start_x Crop start x.
9:8	RW	0x0	sw_lvds_main_lane Choose the lane to parse the sync code
7:4	RW	0x0	sw_lvds_lane_en Lane enable for LVDS eg : 4'b0011 represent lane 0/1 is enable.
3:2	RW	0x0	sw_lvds_width 2'b00 : 8bit 2'b01 : 10bit 2'b10 : 12bit
1	RW	0x0	sw_lvds_mode There are 2 modes 1'b0 : ls-le...fs-fe or sav_act-eav_act...sav_blk-eav_blk 1'b1 : fs-le...ls-fe
0	RW	0x0	sw_lvds_cap_en Enable to capture LVDS 1'b0 : Disable 1'b1 : Enable

CTRL_0000_LVDS_SAV_EAV_ACT

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_act LVDS path sync code of eav_act
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_act LVDS path sync code of sav_act

CTRL_0000_LVDS_SAV_EAV_BLK

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_lvds_eav_blk LVDS path sync code of eav_blk
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_lvds_sav_blk LVDS path sync code of sav_blk

12.4.2.20 LDCH

ISP_LDCH_3B00_STS

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_ldch_en_shd Module ldch enable signal
30	RO	0x0	ldch_working Working state
29	RO	0x0	ldch_map_data_err LDCH error interrupt signal
28:1	RO	0x0000000	reserved
0	RW	0x1	sw_ldch_en_i Module ldch enable signal

12.4.2.21 RAWAF

ISP_RAWAF_4D00_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawaf_meas_flag When rawaf measurement is over, this bit will pulled up by hardware itself, then software could read the result of rawaf. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down.
30:3	RO	0x0000000	reserved
2	RW	0x1	sw_gaus_en 1'b0: Gaus module is disabled 1'b1: Gaus is enabled
1	RW	0x1	sw_gamma_en 1'b0: Gamma module is disabled 1'b1: Gamma is enabled
0	RW	0x0	sw_rawaf_en AF measurement enable 1'b0: AF measurement is disabled 1'b1: AF measurement is enabled Writing a 1 to this register starts a new measurement and resets the afm_fin (measurement finished) interrupt to 0.

ISP_RAWAF_4D00_OFFSET_WINA

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_a_h_l First pixel of window A (horizontal left row), value must be greater or equal 2.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_a_v_t First line of window A (vertical top line), value must be greater or equal 1.

ISP_RAWAF_4D00_SIZE_WINA

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_a_h_size Horizontal size of window A, value must be lower than (width of picture -2 -- a_h_l). This value must be an integer multiple of 15.

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_a_v_size Vertical size of window A, value must be lower than (number of lines -2 -- a_v_t). This value must be an integer multiple of 15.

ISP_RAWAF_4D00_OFFSET_WINB

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_l first pixel of window B (horizontal left row), value must be greater or equal 2.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_b_v_t First line of window B (vertical top line), value must be greater or equal 1.

ISP_RAWAF_4D00_SIZE_WINB

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_size Horizontal size of window A, value must be lower than (width of picture -2 -- a_h_l).
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_b_v_size Vertical size of window A, value must be lower than (number of lines -2 -- a_v_t).

ISP_RAWAF_4D00_INT_LINE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_int_line4_en Int line4 is valid to produle an interrupt signal at the end of the line4 number is measured. 1'b0: AF line4 interrup is disabled; 1'b1: AF line4 interrup is enabled.
30	RW	0x0	sw_int_line3_en Int line3 is valid to produle an interrupt signal at the end of the line3 number is measured. 1'b0: AF line3 interrup is disabled; 1'b1: AF line3 interrup is enabled.
29	RW	0x0	sw_int_line2_en Int line2 is valid to produle an interrupt signal at the end of the line2 number is measured. 1'b0: AF line2 interrup is disabled; 1'b1: AF line2 interrup is enabled.
28	RW	0x0	sw_int_line1_en Int line1 is valid to produle an interrupt signal at the end of the line1 number is measured. 1'b0: AF line1 interrup is disabled; 1'b1: AF line1 interrup is enabled.

Bit	Attr	Reset Value	Description
27	RW	0x0	sw_int_line0_en Int line0 is valid to produle an interrupt signal at the end of the line0 number is measured. 1'b0: AF line0 interrup is disabled; 1'b1: AF line0 interrup is enabled.
26:20	RO	0x00	reserved
19:16	RW	0xf	sw_int_line4 Fifth line number which need to produce int signal, range from 1 to 15, line4 need to be > line3, the interrupt will be produced at the at of ine_line4 - 1.
15:12	RW	0xc	sw_int_line3 Fourth line number which need to produce int signal, range from 1 to 15, line3 need to be > line2, the interrupt will be produced at the at of ine_line3 - 1.
11:8	RW	0x9	sw_int_line2 Third line number which need to produce int signal, range from 1 to 15, line2 need to be > line1, the interrupt will be produced at the at of ine_line2 - 1.
7:4	RW	0x6	sw_int_line1 Second line number which need to produce int signal, range from 1 to 15, line1 need to be > line0, the interrupt will be produced at the at of ine_line1 - 1.
3:0	RW	0x3	sw_int_line0 First line number which need to produce interrupt signal, range from 1 to 15, the interrupt will be produced at the at of ine_line0 - 1.

ISP_RAWAF_4D00_GAUS_COE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x08	sw_gaus_coe_h2 The coe of first line and first colume pix in 3x3 gaus filter
15	RO	0x0	reserved
14:8	RW	0x10	sw_gaus_coe_h1 The coe of first line and second colume pix in 3x3 gaus filter
7:0	RW	0x20	sw_gaus_coe_h0 The coe of middle pix in 3x3 gaus filter

ISP_RAWAF_4D00_THRES

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_ram_star_addr sw_ram_star_addr, if ine_line0_en is 1, it need to be small than value of (ine_line0-1)*15; Else if ine_line1_en is 1, it need to be small than value of (ine_line1-1)*15, and so on.
15:0	RW	0x0000	sw_afm_thres AF measurement threshold This register defines a threshold which can be used for minimizing the influence of noise in the measurement result.

ISP_RAWAF_4D00_VAR_SHIFT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	sw_lum_var_shift_b Variable shift for luminance summation
19	RO	0x0	reserved
18:16	RW	0x0	sw_lum_var_shift_a Variable shift for luminance summation The lum_var_shift defines the number of bits for the shift operation of the value of the current pixel before summation. The shift operation is used to avoid a luminance sum overflow.
15:7	RO	0x000	reserved
6:4	RW	0x0	sw_afm_var_shift_b Variable shift for AF measurement
3	RO	0x0	reserved
2:0	RW	0x0	sw_afm_var_shift_a Variable shift for AF measurement The afm_var_shift defines the number of bits for the shift operation at the end of the calculation chain. The shift operation is used to avoid an AF measurement sum overflow.

ISP_RAWAF_4D00_SUM_A

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	afm_sum_a Sharpness value of window A

ISP_RAWAF_4D00_SUM_B

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	afm_sum_b Sharpness value of window B

ISP_RAWAF_4D00_LUM_A

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	afm_lum_a Luminance value of window A

ISP_RAWAF_4D00_LUM_B

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	afm_lum_b Luminance value of window B

ISP_RAWAF_4D00_GAMMA_Y0

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x0b	sw_y1 Y1 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_y0 Y0 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y1

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x2c	sw_y3 Y3 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x1b	sw_y2 Y2 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y2

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x56	sw_y5 Y5 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x3d	sw_y4 Y4 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y3

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x72	sw_y7 Y7 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x66	sw_y6 Y6 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y4

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x8d	sw_y9 Y9 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x7d	sw_y8 Y8 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y5

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0xa9	sw_y11 Y11 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0x9b	sw_y10 Y10 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y6

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0xd0	sw_y13 Y13 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0xbd	sw_y12 Y12 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y7

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0xf0	sw_y15 Y15 value of gamma table
15:8	RO	0x00	reserved
7:0	RW	0xe0	sw_y14 Y14 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y8

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	sw_y16 Y16 value of gamma table

ISP_RAWAF_4D00_INT_STATE

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	int_line4_state When int_line4_en is 1 and at the end of line4 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down.
3	RW	0x0	int_line3_state When int_line3_en is 1 and at the end of line3 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down.
2	RW	0x0	int_line2_state When int_line2_en is 1 and at the end of line2 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down.

Bit	Attr	Reset Value	Description
1	RW	0x0	int_line1_state When int_line1_en is 1 and at the end of line1 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down.
0	RW	0x0	int_line0_state When int_line0_en is 1 and at the end of line0 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the begining of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down.

ISP_RAWAF_4D00_RAM_DATA

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sum_data_wndx Total 15x15 windows, each window has 32bit, if need shift , please use afm_var_shift_a.

12.4.2.22 RAWAE

(1)RAWAE_BIG

RAWAE_BIG_4400_4600_4700_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aemeas_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_working_r
29:9	RO	0x000000	reserved
8	RW	0x0	sw_aemeas_debug_en The debug signal will toggle when this bit asset.
7	RW	0x0	sw_rawae_big_wnd4_en 1'b0: Window close 1'b1: Window open
6	RW	0x0	sw_rawae_big_wnd3_en 1'b0: Window close 1'b1: Window open
5	RW	0x0	sw_rawae_big_wnd2_en 1'b0: Window close 1'b1: Window open
4	RW	0x0	sw_rawae_big_wnd1_en 1'b0: Window close 1'b1: Window open

Bit	Attr	Reset Value	Description
3	RO	0x0	ro_rd_ram_en User need assert this bit to 1 before reading back RAM data and set to 0 after read operation.
2:1	RW	0x0	sw_aemeas_wnd0_num 2'b0: 1x1 2'b1: 5x5 2'b2: 15x15 2'b3: 15x15
0	RW	0x0	sw_aemeas_en 1'b0: Disable this module 1'b1: Enable this module

RAWAE_BIG_4400_4600_4700_WND0_BLK_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size Vertical offset of first block in pixels. Note: The vertical size must be oven, and need leave 2lines at last.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size Horizontal size in pixels of one block. Note: exp_h_size*window_num must be less (not equal) than the horizontal size of the picture.

RAWAE_BIG_4400_4600_4700_WND0_OFFSET

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

RAWAE_BIG_4400_4600_4700_RAM_CTRL

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset

RAWAE_BIG_4400_4600_4700_WND1_SIZE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window Note: This signal is not this window's vertical size.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window Note: This signal is not this window's horizontal size.

RAWAE_BIG_4400_4600_4700_WND1_OFFSET

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels

RAWAE_BIG_4400_4600_4700_WND2_SIZE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window Note: This signal is not this window's vertical size.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window Note: This signal is not this window's horizontal size.

RAWAE_BIG_4400_4600_4700_WND2_OFFSET

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels

RAWAE_BIG_4400_4600_4700_WND3_SIZE

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window Note: This signal is not this window's vertical size.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window Note: This signal is not this window's horizontal size.

RAWAE_BIG_4400_4600_4700_WND3_OFFSET

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels

RAWAE_BIG_4400_4600_4700_WND4_SIZE

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window Note: This signal is not this window's vertical size.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window Note: This signal is not this window's horizontal size.

RAWAE_BIG_4400_4600_4700_WND4_OFFSET

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels

RAWAE_BIG_4400_4600_4700_WND1_SUMR

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumr

RAWAE_BIG_4400_4600_4700_WND2_SUMR

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd2_sumr

RAWAE_BIG_4400_4600_4700_WND3_SUMR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd3_sumr

RAWAE_BIG_4400_4600_4700_WND4_SUMR

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd4_sumr

RAWAE_BIG_4400_4600_4700_WND1_SUMG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd1_sumg

RAWAE_BIG_4400_4600_4700_WND2_SUMG

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd2_sumg

RAWAE_BIG_4400_4600_4700_WND3_SUMG

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd3_sumg

RAWAE_BIG_4400_4600_4700_WND4_SUMG

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd4_sumg

RAWAE_BIG_4400_4600_4700_WND1_SUMB

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumb

RAWAE_BIG_4400_4600_4700_WND2_SUMB

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd2_sumb

RAWAE_BIG_4400_4600_4700_WND3_SUMB

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd3_sumb

RAWAE_BIG_4400_4600_4700_WND4_SUMB

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd4_sumb

RAWAE_BIG_4400_4600_4700_RO_DBG1

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	ro_current_y_pos
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_current_x_pos

RAWAE_BIG_4400_4600_4700_RO_DBG2

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_wnd_val
30	RO	0x0	ro_vblk_end
29	RO	0x0	ro_vactive

Bit	Attr	Reset Value	Description
28:16	RO	0x0000	ro_v_cnt
15	RO	0x0	ro_blk_finish
14	RO	0x0	ro_hblk_end
13	RO	0x0	ro_hactive
12:0	RO	0x0000	ro_h_cnt

RAWAE_BIG_4400_4600_4700_RO_DBG3

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	ro_acc_val
22	RO	0x0	ro_mean_val
21	RO	0x0	ro_working_stored
20	RO	0x0	ro_gating
19	RO	0x0	ro_in_hend
18	RO	0x0	ro_in_vend
17	RO	0x0	ro_in_val
16	RO	0x0	ro_in_ack
15:8	RO	0x00	ro_mean_addr
7:4	RO	0x0	ro_y_current_blk
3:0	RO	0x0	ro_x_current_blk

RAWAE_BIG_4400_4600_4700_RO_MEAN_BASE_ADDR

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	ro_rawae_mean_channelr_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.
21:12	RO	0x000	ro_rawae_mean_channelb_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.
11:0	RO	0x000	ro_rawae_mean_channelg_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.

(2) RAWAE_LITE

ISP_RAWAE_LITE_4500_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aemeas_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RW	0x0	ro_working_r Field0000 Description
29:9	RO	0x000000	reserved
8	RW	0x0	sw_aemeas_debug_en The debug signal will toggle when this bit asset
7:2	RO	0x00	reserved
1	RW	0x0	sw_aemeas_wnd_num 1'b0: 1x1 1'b1: 5x5

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_aemeas_en 1'b0: No mean 1'b1: Start ae module (autoclr)

ISP_RAWAE_LITE_4500_BLK_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size Vertical offset of first block in pixels Note: The vertical size must be oven, and need leave 2lines at last.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size Horizontal size in pixels of one block Note: exp_h_size*window_num must be less (not equal) than the horizontal size of the picture.

ISP_RAWAE_LITE_4500_OFFSET

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels

ISP_RAWAE_LITE_4500_RO_MEAN_XX

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	ro_rawae_mean_channelr_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.
21:12	RO	0x000	ro_rawae_mean_channelb_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.
11:0	RO	0x000	ro_rawae_mean_channelg_xy Channel g mean luminance value of block 00~44 (x,y), x, y means x and y coordinate.

ISP_RAWAE_LITE_4500_RO_DBG1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_wnd_val
30	RO	0x0	ro_vblk_end
29	RO	0x0	ro_vactive
28:16	RO	0x0000	ro_v_cnt
15	RO	0x0	ro_blk_finish
14	RO	0x0	ro_hblk_end
13	RO	0x0	ro_hactive
12:0	RO	0x0000	ro_h_cnt

ISP_RAWAE_LITE_4500_RO_DBG2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	ro_acc_val
22	RO	0x0	ro_mean_val
21	RO	0x0	ro_working_stored
20	RO	0x0	ro_gating
19	RO	0x0	ro_in_hend
18	RO	0x0	ro_in_vend
17	RO	0x0	ro_in_val
16	RO	0x0	ro_in_ack
15:8	RO	0x00	ro_mean_addr
7:4	RO	0x0	ro_y_current_blk
3:0	RO	0x0	ro_x_current_blk

12.4.2.23 RAWAWB

ISP_RAWAWB_5000_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_meas_done when rawawb measurement is over, this bit is pulled up by hardware itself, then software could read the result of rawawb. When read is over, it should been pulled down by software, and rawawb will work again at the begining of next frame after pulled down
30	RW	0x0	ro_rawawb_working rawawb working state read bac 1'b1: Workin 1'b0: Not working
29:27	RO	0x0	reserved
26	RW	0x0	sw_rawawb_3dyuv_en1 1'b1: 3DYUV detect enable for all light and big window 1'b0: 3DYUV detect disable for all light and big window
25	RW	0x0	sw_rawawb_xy_en1 1'b1: XY detect enable for all light and big window 1'b0: XY detect disable for all light and big window
24	RW	0x0	sw_rawawb_uv_en1 1'b1: UV detect enable for all light and big window 1'b0: UV detect disable for all light and big window
23	RO	0x0	reserved
22:20	RW	0x0	sw_rawawb_light_num number of light sources, range is from 0 to 7
19	RW	0x0	sw_rawlsc_bypass_en 1'b1: rawlsc bypass enable 1'b0: rawlsc bypass disable
18	RW	0x0	sw_rawawb_wind_size raw to rgb down sample window siz 1: 8x8 windo 0: 4x4 windo If sw_rawawb_h_size > 2560, the window size would been 8x8 forced by hardware
17:16	RO	0x0	reserved
15:13	RW	0x0	sw_rawawb_3dyuv_ls_idx3 light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to supprot maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 3 . 3'd6: Light 6 for 3dyuv white point detected logic 3 3'd7: Disable for 3dyuv white point detected logic 3

12:10	RW	0x0	sw_rawawb_3dyuv_ls_idx2 light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to supprot maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 2 . 3'd6: Light 6 for 3dyuv white point detected logic 2 3'd7: Disable for 3dyuv white point detected logic 2
9:7	RW	0x0	sw_rawawb_3dyuv_ls_idx1 light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to supprot maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 1 . 3'd6: Light 6 for 3dyuv white point detected logic 1 3'd7: Disable for 3dyuv white point detected logic 1
6:4	RW	0x0	sw_rawawb_3dyuv_ls_idx0 light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to supprot maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 0 . 3'd6: Light 6 for 3dyuv white point detected logic 0 3'd7: Disable for 3dyuv white point detected logic 0
3	RW	0x0	sw_rawawb_3dyuv_en0 1'b1: 3DYUV detect enable for all light and normal window 1'b0: 3DYUV detect disable for all light and normal window
2	RW	0x0	sw_rawawb_xy_en0 1'b1: XY detect enable for all light and normal window 1'b0: XY detect disable for all light and normal window
1	RW	0x0	sw_rawawb_uv_en0 1'b1: UV detect enable for all light and normal window 1'b0: UV detect disable for all light and normal window
0	RW	0x0	sw_rawawb_en 1'b1: Rawawb enable 1'b0: Rawawb disable

ISP_RAWAWB_5000_SUM_BGAIN_BIG_3

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_3 read only : white point sum of bgain

ISP_RAWAWB_5000_SUM_RGAIN_BIG_3

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_3 read only : white point sum of rgain

ISP_RAWAWB_5000_BLK_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	sw_rawawb_blk_with_luma_wei_en Block luma weight enable bit
7	RO	0x0	reserved
6:4	RW	0x0	sw_rawawb_blk_measure_illu_idx 3'b0: Select source light 3'b1: Select source light .. 3'b7: Select all lights
3	RW	0x0	sw_rawawb_blk_rtdw_measure_en The right and down corner of block measure enable bit
2	RW	0x0	sw_rawawb_blk_measure_xytype 1'b0: Select normal windo 1'b1: Select big window
1	RW	0x0	sw_rawawb_blk_measure_mode 1'b0: Measure all pixel 1'b1: Measure real one
0	RW	0x0	sw_rawawb_blk_measure_en Block measure enable bit

ISP_RAWAWB_5000_WIN_OFFS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_v_offs awb vertical offset of crop measure windo bit16 is written to 0 by hardware to align offset to 2
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_offs awb horizontal offset of crop measure windo bit0 is written to 0 by hardware to align offset to 2

ISP_RAWAWB_5000_WIN_SIZE

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_v_size awb vertical crop window siz 8x8 down sample window: bit16 to bit18 are written to 0 by hardware to algin size to 4x4 down sample window: bit16 to bit17 are written to 0 by hardware to algin size to 4
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_size awb horizontal window siz down sample window 8x8: bit0 to bit2 are written to 0 by hardware to algin size to down sample window 4x4: bit0 to bit1 are written to 0 by hardware to algin size to 4

ISP_RAWAWB_5000_LIMIT_RG_MAX

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	sw_rawawb_g_max max green value in white point detection
15:8	RO	0x0	reserved
7:0	RW	0x00	sw_rawawb_r_max max red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MAX

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	sw_rawawb_y_max max luminance value in white point detection
15:8	RO	0x0	reserved
7:0	RW	0x00	sw_rawawb_b_max max bule value in white point detection

ISP_RAWAWB_5000_LIMIT_RG_MIN

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	sw_rawawb_g_min min green value in white point detection
15:8	RO	0x0	reserved
7:0	RW	0x00	sw_rawawb_r_min max red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MIN

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	sw_rawawb_y_min min luminance value in white point detection
15:8	RO	0x0	reserved
7:0	RW	0x00	sw_rawawb_b_min min bule value in white point detection

ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	sw_rawawb_wp_hist_xytype Sel normal or big window for YHIST 1'b0: normal windo 1'b1: big window
3	RW	0x0	sw_rawawb_wp_blk_wei_en1 Block weight enable bit for big window
2	RW	0x0	sw_rawawb_wp_blk_wei_en0 Block weight enable bit for normal window
1	RW	0x0	sw_rawawb_wp_luma_wei_en1 Y weight curve enable for big window
0	RW	0x0	sw_rawawb_wp_luma_wei_en0 Y weight curve enable for normal window

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	sw_rawawb_wp_luma_weicurve_y3 Y weight curve x coordinate
23:16	RW	0x40	sw_rawawb_wp_luma_weicurve_y2 Y weight curve x coordinate
15:8	RW	0x20	sw_rawawb_wp_luma_weicurve_y1 Y weight curve x coordinate
7:0	RW	0x00	sw_rawawb_wp_luma_weicurve_y0 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0xe0	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate
23:16	RW	0xc0	sw_rawawb_wp_luma_weicurve_y7 Y weight curve x coordinate
15:8	RW	0xa0	sw_rawawb_wp_luma_weicurve_y6 Y weight curve x coordinate
7:0	RW	0x80	sw_rawawb_wp_luma_weicurve_y5 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0xff	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w3 Y weight curve y coordinate
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w2 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w1 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w0 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w7 Y weight curve y coordinate
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w6 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w5 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w4 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x100	sw_rawawb_pre_wbgain_inv_r For some sensor has already do awbgain need do some pre wbgain operation； Or，use for rawawb dgain
15:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w8 Y weight curve y coordinate

ISP_RAWAWB_5000_PRE_WBGAIN_INV

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x100	sw_rawawb_pre_wbgain_inv_b For some sensor has already do awbgain need do some pre wbgain operation
15:11	RO	0x0	reserved
10:0	RW	0x100	sw_rawawb_pre_wbgain_inv_g For some sensor has already do awbgain need do some pre wbgain operation Or，use for rawawb dgain

ISP_RAWAWB_5000_UV_DETC_VERTEX0_0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_0 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_0 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_0

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_0 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_0 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_0

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_0 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_0 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_0

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_0 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_0 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_0 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_0
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_0 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_0
Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_0 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_0
Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_0 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_1
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_1 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_1 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_1
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_1 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_1 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_1
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_1 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_1 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_1

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_1 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_1 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_1

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_1 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_1 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_1

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_1 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_1

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_1 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_2

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_2 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_2 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_2

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_2 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_2 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_2 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_2 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_2

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_2 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_2 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_2
Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_2 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_2
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_2 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_2
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_2 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2
Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_2 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_3
Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_3 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_3 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_3
Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_3 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_3 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_3

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_3 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_3 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_3

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_3 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_3 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_3 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_3 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_3 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_3 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_4

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_4 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_4 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_4

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_4 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_4 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_4

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_4 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_4 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_4

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_4 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_4 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_4

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_4 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_4

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_4 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_4

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_4 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_4

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_4 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_5

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_5 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_5 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_5

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_5 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_5 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_5

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_5 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_5 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_5

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_5 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_5 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_5

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_5 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE10_5
Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope12_5 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_5
Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_5 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_5
Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_5 slope inv

ISP_RAWAWB_5000_UV_DETC_VERTEX0_6
Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_6 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_6 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_6
Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_6 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_6 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_6
Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_6 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_6 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_6

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_6 vertex coordinate
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_6 vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_6

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope01_6 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE10_6

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope10_6 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope23_6 slope inv

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_6

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_rawawb_islope30_6 slope inv

ISP_RAWAWB_5000_YUV_RGB2ROTY_0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_y RGB2ROTY matrix, coeff 1
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_y RGB2ROTY matrix, coeff 0

ISP_RAWAWB_5000_YUV_RGB2ROTY_1

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_y RGB2ROTY matrix, offset
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_y RGB2ROTY matrix, coeff 2

ISP_RAWAWB_5000_YUV_RGB2ROTU_0

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_u RGB2ROTU matrix, coeff 1
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_u RGB2ROTU matrix, coeff 0

ISP_RAWAWB_5000_YUV_RGB2ROTU_1

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_u RGB2ROTU matrix, offset
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_u RGB2ROTU matrix, coeff 2

ISP_RAWAWB_5000_YUV_RGB2ROTV_0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_rawawb_rgb2ryuvmat1_v RGB2ROTV matrix, coeff 1
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat0_v RGB2ROTV matrix, coeff 0

ISP_RAWAWB_5000_YUV_RGB2ROTV_1

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_rgb2ryuvofs_v RGB2ROTY matrix, offset
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_rawawb_rgb2ryuvmat2_v RGB2ROTY matrix, coeff 2

ISP_RAWAWB_5000_YUV_X_COOR_Y_0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_y signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_y unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_0

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_u signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_u unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_0

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls0_v signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls0_v unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_0
Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls0 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls0 The x coordinate of u interpolation curve
15:5	RO	0x0	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls0 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_0
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls0 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls0 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls0 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls0 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_0
Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_0
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_0

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls0 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls0 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_1

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_y signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_y unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_u signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_u unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_1

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls1_v signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls1_v unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_1

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls1 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls1 The x coordinate of u interpolation curve
15:5	RO	0x0	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls1 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_1

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls1 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls1 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls1 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls1 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_1

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_1

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_1

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls1 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls1 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_2

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_y signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_y unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_2

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_u signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_u unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls2_v signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls2_v unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_2

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls2 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls2 The x coordinate of u interpolation curve
15:5	RO	0x0	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls2 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_2

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls2 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls2 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls2 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls2 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_2

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_2

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_2

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls2 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls2 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_X_COOR_Y_3

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_y signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_y unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_U_3

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_u signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_u unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X_COOR_V_3

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_vec_x21_ls3_v signed, 8 interger and 4 fraction
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_coor_x1_ls3_v unsigned, 8 interger and 4 fraction

ISP_RAWAWB_5000_YUV_X1X2_DIS_3

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu1_ls3 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu0_ls3 The x coordinate of u interpolation curve
15:5	RO	0x0	reserved
4:0	RW	0x00	sw_rawawb_dis_x1x2_ls3 The distance between x1 and x2 (must 2^n)

ISP_RAWAWB_5000_YUV_INTERP_CURVE_UCOOR_3

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawawb_rotu5_ls3 The x coordinate of u interpolation curve
23:16	RW	0x00	sw_rawawb_rotu4_ls3 The x coordinate of u interpolation curve
15:8	RW	0x00	sw_rawawb_rotu3_ls3 The x coordinate of u interpolation curve
7:0	RW	0x00	sw_rawawb_rotu2_ls3 The x coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH0_3

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th1_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th0_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH1_3

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th3_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th2_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_YUV_INTERP_CURVE_TH2_3

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_th5_ls3 The y coordinate of u interpolation curve
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_th4_ls3 The y coordinate of u interpolation curve

ISP_RAWAWB_5000_RGB2XY_WT01

Address: Operational Base + offset (0x01fc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_wt1 RGB2XY weight matrix, coeff 1
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_wt0 RGB2XY weight matrix, coeff 0

ISP_RAWAWB_5000_RGB2XY_WT2

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_wt2 RGB2XY weight matrix, coeff 0

ISP_RAWAWB_5000_RGB2XY_MAT0_XY

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat0_y rgb2xy, rotation matrix, first column y
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat0_x rgb2xy, rotation matrix, first column x

ISP_RAWAWB_5000_RGB2XY_MAT1_XY

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat1_y rgb2xy, rotation matrix, second column y
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat1_x rgb2xy, rotation matrix, second column x

ISP_RAWAWB_5000_RGB2XY_MAT2_XY

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat2_y rgb2xy, rotation matrix, third column y
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat2_x rgb2xy, rotation matrix, third column x

ISP_RAWAWB_5000_XY_DETC_NOR_X_0

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_0 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_0 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_0

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_0 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_0 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_0

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_0 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_0 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_0
Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_0 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_0 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_1
Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_1 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_1 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_1
Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_1 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_1 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_1
Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_1 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_1 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_1
Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_1 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_1 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_2
Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_2 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_2 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_2
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_2 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_2 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_2
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_2 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_2 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_2
Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_2 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_2 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_3
Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_3 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_3 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_3
Address: Operational Base + offset (0x025c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_3 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_3 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_3
Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_3 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_3 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_3
Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_3 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_3 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_4
Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_4 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_4 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_4
Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_4 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_4 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_4
Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_4 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_4 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_4
Address: Operational Base + offset (0x027c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_4 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_4 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_5
Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_5 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_5 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_5
Address: Operational Base + offset (0x028c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_5 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_5 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_5
Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_5 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_5 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_5
Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_5 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_5 xy detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_6
Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_6 xy detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_6 xy detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_6
Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_6 xy detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_6 xy detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_6
Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_6 xy detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_6 xy detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_6

Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_6 xy detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_6 xy detect, up y boundary of big range

ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	sw_rawawb_exc_wp_region3_domain The domain of exclude regio 1'b1: xy rang 1'b0: uv range
14	RW	0x0	sw_rawawb_exc_wp_region3_measen The measurement enable of exclude region in xy or uv rang 1'b1: Enabl 1'b0: Disable
13:12	RW	0x0	sw_rawawb_exc_wp_region3_excen The exclude enable of exclude region in both xy and uv range Bit0 is for normal window and bit1 for big window
11	RW	0x0	sw_rawawb_exc_wp_region2_domain The domain of exclude regio 1'b1: xy rang 1'b0: uv range
10	RW	0x0	sw_rawawb_exc_wp_region2_measen The measurement enable of exclude region in xy or uv rang 1'b1: Enabl 1'b0: Disable
9:8	RW	0x0	sw_rawawb_exc_wp_region2_excen The exclude enable of exclude region in both xy and uv range Bit0 is for normal window and bit1 for big window
7	RW	0x0	sw_rawawb_exc_wp_region1_domain The domain of exclude regio 1'b1: xy rang 1'b0: uv range
6	RW	0x0	sw_rawawb_exc_wp_region1_measen The measurement enable of exclude region in xy or uv rang 1'b1: Enabl 1'b0: Disable
5:4	RW	0x0	sw_rawawb_exc_wp_region1_excen The exclude enable of exclude region in both xy and uv range Bit0 is for normal window and bit1 for big window
3	RW	0x0	sw_rawawb_exc_wp_region0_domain The domain of exclude regio 1'b1: xy rang 1'b0: uv range
2	RW	0x0	sw_rawawb_exc_wp_region0_measen The measurement enable of exclude region in xy or uv rang 1'b1: Enabl 1'b0: Disable
1:0	RW	0x0	sw_rawawb_exc_wp_region0_excen The exclude enable of exclude region in both xy and uv range Bit0 is for normal window and bit1 for big window

ISP_RAWAWB_5000_EXC_WP_REGION0_XU

Address: Operational Base + offset (0x02fc)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION0_YV

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_XU

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_YV

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_XU

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_YV

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region2_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_XU

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_YV

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_XU

Address: Operational Base + offset (0x031c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_YV

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_XU

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_YV

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_XU

Address: Operational Base + offset (0x032c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_YV

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_SUM_RGAIN_NOR_0

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_0 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_0

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_0 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_0

Address: Operational Base + offset (0x034c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_0 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_0

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_0 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_0

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_0 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_0

Address: Operational Base + offset (0x035c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_0 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_1

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_1 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_1

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_1 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_1

Address: Operational Base + offset (0x037c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_1 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_1

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_1 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_1

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_1 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_1

Address: Operational Base + offset (0x038c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_1 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_2

Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_2 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_2

Address: Operational Base + offset (0x03a8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_2 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_2

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_2 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_2

Address: Operational Base + offset (0x03b0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_2 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_2

Address: Operational Base + offset (0x03b8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_2 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_2

Address: Operational Base + offset (0x03bc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_2 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_3

Address: Operational Base + offset (0x03d0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_3 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_3

Address: Operational Base + offset (0x03d8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_3 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_3

Address: Operational Base + offset (0x03dc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_3 read only : white point num with weight

ISP_RAWAWB_5000_WP_NUM_BIG_3

Address: Operational Base + offset (0x03ec)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_3 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_4

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_4 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_4

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_4 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_4

Address: Operational Base + offset (0x040c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_4 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_4

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_4 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_4

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_4 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_4

Address: Operational Base + offset (0x041c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_4 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_5

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_5 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_5

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_5 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_5

Address: Operational Base + offset (0x043c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_5 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_5

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_5 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_5

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_5 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_5

Address: Operational Base + offset (0x044c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_5 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_6

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_6 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_6

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_6 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_NOR_6

Address: Operational Base + offset (0x046c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_6 read only : white point num with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_6

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_6 read only : white point sum of rgain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_6

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_6 read only : white point sum of bgain

ISP_RAWAWB_5000_WP_NUM_BIG_6

Address: Operational Base + offset (0x047c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_6 read only : white point num with weight

ISP_RAWAWB_5000_Y_HIST01

Address: Operational Base + offset (0x0620)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin1 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin0 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST23

Address: Operational Base + offset (0x0624)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin3 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin2 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST45

Address: Operational Base + offset (0x0628)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin5 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin4 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST67

Address: Operational Base + offset (0x062c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin7 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin6 The bin of YHIST

ISP_RAWAWB_5000_RAM_CTRL

Address: Operational Base + offset (0x0650)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_rd_ram_en This bit is not need configuration in normal case, software could read the ram directly when rawawb interruption is valid. But the software could read the information in the ram in case the rawawb is failed to create interruption or stuck The bit is need pulled down again before the next valid frame statistics
30:22	RW	0x000	ro_ram_rdaddr_cnt RAM real address when read 15x15 window statistics in ram, read only
21:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawawb_ram_offs The 15x15 windows statistics information is stored in ram, the real size of ram is 225x57. Each ram address is for one window. The sw_rawawb_ram_offs is ram offset address when reading, so it is meas the software could read statistics from the offset window

ISP_RAWAWB_5000_WRAM_CTRL

Address: Operational Base + offset (0x0654)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RO	0x00	ro_rawawb_ram_cnt config ram cnt
15:0	RO	0x0	reserved

ISP_RAWAWB_5000_WRAM_DATA_BASE

Address: Operational Base + offset (0x0660)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_rawawb_wp_blk_wei_w4 sub-window weight from num0 to num224
23:18	RW	0x00	sw_rawawb_wp_blk_wei_w3 sub-window weight from num0 to num224
17:12	RW	0x00	sw_rawawb_wp_blk_wei_w2 sub-window weight from num0 to num224
11:6	RW	0x00	sw_rawawb_wp_blk_wei_w1 sub-window weight from num0 to num224
5:0	RW	0x00	sw_rawawb_wp_blk_wei_w0 sub-window weight from num0 to num224

ISP_RAWAWB_5000_RAM_DATA_BASE

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_wind15x15 There is 225 window information, each information is 64bits, 18bit for each RGB channel and 10bit for white point number First word: G[13:0],B[17:0];Second word: Wpnum[9:0],R[17:0],G[17:14] The read ram address should equal this base addr each read ram option, ram address is added by hardware

12.4.2.24 RAWHIST

(1) RAWHIST_BIG

ISP_RAWHIST_BIG_4800_4A00_4B00_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aehist_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_aehist_working This module working signal
29:28	RW	0x2	sw_aehist_wnd_num 2'd0, 2'd1: 5x5 2'd2, 2'd3: 15x15
27	RO	0x0	reserved
26:24	RW	0x0	sw_aehist_data_sel 3'd0: input_data[11:4] 3'd1: input_data[10:3] 3'd2: input_data[9:2] 3'd3: input_data[8:1] 3'd4: input_data[7:0] Others: input_data[7:0]
23:12	RW	0x000	sw_aehist_waterline For region statics
11	RO	0x0	reserved
10:8	RW	0x0	sw_aehist_mode Histogram mode, luminance is taken at ISP output before output formatter, RGB is taken at xtalk output. 3'd7, 3'd6: Must not be used 3'd5: Y (luminance) histogram 3'd4: B histogram 3'd3: G histogram 3'd2: R histogram 3'd1: Reserved 3'd0: Disable, no measurements
7	RW	0x0	sw_aehist_debug_en The debug signal will toggle when this bit asset.
6:4	RO	0x0	reserved
3:1	RW	0x0	sw_aehist_stepsize Histogram predivider, process every (stepsize)th pixel, all other pixels are skipped.

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_aehist_en Module enable bit

ISP_RAWHIST_BIG_4800_4A00_4B00_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_aehist_v_size Vertical size in lines of one sub-window
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_aehist_h_size Horizontal size in pixels of one sub-window,

ISP_RAWHIST_BIG_4800_4A00_4B00_OFFS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aehist_v_offset Vertical offset of first window in pixels
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aehist_h_offset Horizontal offset of first window in pixels

ISP_RAWHIST_BIG_4800_4A00_4B00_HRAM_CTRL

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt RAM cnt for write or read
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_BIG_4800_4A00_4B00_RAW2Y_CC

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawae_off The coeffitient of RAW2Y formula
23:16	RW	0x0d	sw_rawae_bcc RAW2Y blue channel coeffitient
15:8	RW	0x20	sw_rawae_gcc RAW2Y green channel coeffitient
7:0	RW	0x21	sw_rawae_rcc RAW2Y red channel coeffitient

ISP_RAWHIST_BIG_4800_4A00_4B00_WRAM_CTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_config_wram_en Write RAM enable
30:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RO	0x00	ro_ram_cnt RAM cnt for write or read
15:6	RO	0x000	reserved
5:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_BIG_4800_4A00_4B00_DBG1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_in_val
30	RO	0x0	ro_in_hend
29	RO	0x0	ro_in_vend
28:16	RO	0x0000	ro_cur_y_pos Y cnt for current frame
15	RO	0x0	ro_hist_wnd_val
14	RO	0x0	ro_hist_framing
13	RO	0x0	ro_hist_gating
12:0	RO	0x0000	ro_cur_x_pos X cnt for current frame

ISP_RAWHIST_BIG_4800_4A00_4B00_DBG2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	ro_wram_first_rd_val
25:24	RO	0x0	ro_wram_cur_state
23:16	RO	0x00	ro_ram_clr_cnt
15:14	RO	0x0	ro_cur_state
13	RO	0x0	ro_hist_rd
12	RO	0x0	ro_hist_wr
11	RO	0x0	ro_channelx_wnd_val
10	RO	0x0	ro_channelx_val
9	RO	0x0	ro_channelx_hend
8	RO	0x0	ro_channelx_vend
7	RO	0x0	ro_vblank_val
6:4	RO	0x0	ro_hist_stepsize_y_pos Y cnt for current frame
3	RO	0x0	ro_stepsize_val
2:0	RO	0x0	ro_hist_stepsize_x_pos X cnt for current frame

ISP_RAWHIST_BIG_4800_4A00_4B00_DBG3

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x0	ro_subwindow_y
27	RO	0x0	reserved
26:16	RO	0x000	ro_hist_wnd_y_cnt Y cnt for current frame
15	RO	0x0	reserved
14:12	RO	0x0	ro_subwindow_x
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_hist_wnd_x_cnt X cnt for current frame

ISP_RAWHIST_BIG_4800_4A00_4B00_WEIGHT_BASE

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_aehist_weight_wnd4 Sub-window weight from num0 to num224
23:18	RW	0x20	sw_aehist_weight_wnd3 Sub-window weight from num0 to num224
17:12	RW	0x20	sw_aehist_weight_wnd2 Sub-window weight from num0 to num224
11:6	RW	0x20	sw_aehist_weight_wnd1 Sub-window weight from num0 to num224
5:0	RW	0x20	sw_aehist_weight_wnd0 Sub-window weight from num0 to num224

ISP_RAWHIST_BIG_4800_4A00_4B00_RO_BASE_BIN

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_aehist_bin_x Measured bin count as 28-bit unsigned integer value with 5 fractional part.

(2) RAWHIST_LITE

ISP_RAWHIST_LITE_4900_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aehist_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write 1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_aehist_working This module working signal
29:27	RO	0x0	reserved
26:24	RW	0x0	sw_aehist_data_sel 3'd0: input_data[11:4] 3'd1: input_data[10:3] 3'd2: input_data[9:2] 3'd3: input_data[8:1] 3'd4: input_data[7:0] Others: input_data[7:0]
23:12	RW	0x000	sw_aehist_waterline For region statics
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	sw_aehist_mode Histogram mode, luminance is taken at ISP output before output formatter, RGB is taken at xtalk output. Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window. 3'd7, 3'd 6: Must not be used 3'd5: Y (luminance) histogram 3'd4: B histogram 3'd3: G histogram 3'd2: R histogram 3'd1: Reserved 3'd0: Disable, no measurements
7	RW	0x0	sw_aehist_debug_en The debug signal will toggle when this bit asset.
6:4	RO	0x0	reserved
3:1	RW	0x0	sw_aehist_stepsize Histogram predivider, process every (stepsize)th pixel, all other pixels are skipped.
0	RW	0x0	sw_aehist_en Module enable bit

ISP_RAWHIST_LITE_4900_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_aehist_v_size Vertical size in lines of one sub-window
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_aehist_h_size Horizontal size in pixels of one sub-window

ISP_RAWHIST_LITE_4900_OFFS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aehist_v_offset Vertical offset of first window in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aehist_h_offset Horizontal offset of first window in pixels.

ISP_RAWHIST_LITE_4900_RAM_CTRL

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt RAM read or write cnt
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_LITE_4900_RAW2Y_CC

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawae_off The offset of RAW2Y formula
23:16	RW	0x0d	sw_rawae_bcc RAW2Y blue channel coeffitient
15:8	RW	0x20	sw_rawae_gcc RAW2Y green channel coeffitient
7:0	RW	0x21	sw_rawae_rcc RAW2Y red channel coeffitient

ISP_RAWHIST_LITE_4900_DBG1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_in_val
30	RO	0x0	ro_in_hend
29	RO	0x0	ro_in_vend
28:16	RO	0x0000	ro_cur_y_pos Y cnt for current frame
15	RO	0x0	ro_hist_wnd_val
14	RO	0x0	ro_hist_framing
13	RO	0x0	ro_hist_gating
12:0	RO	0x0000	ro_cur_x_pos X cnt for current frame

ISP_RAWHIST_LITE_4900_DBG2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_clr_cnt
15:14	RO	0x0	ro_cur_state
13	RO	0x0	ro_hist_rd
12	RO	0x0	ro_hist_wr
11	RO	0x0	ro_channelx_wnd_val
10	RO	0x0	ro_channelx_val
9	RO	0x0	ro_channelx_hend
8	RO	0x0	ro_channelx_vend
7	RO	0x0	ro_vblank_val
6:4	RO	0x0	ro_hist_stepsize_y_pos Y cnt for current frame
3	RO	0x0	ro_stepsize_val
2:0	RO	0x0	ro_hist_stepsize_x_pos X cnt for current frame

ISP_RAWHIST_LITE_4900_DBG3

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	ro_subwindow_y
27	RO	0x0	reserved
26:16	RO	0x000	ro_hist_wnd_y_cnt Y cnt for current frame
15:12	RO	0x0	ro_subwindow_x
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_hist_wnd_x_cnt X cnt for current frame

ISP_RAWHIST_LITE_4900_WEIGHT_0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_aehist_weight_wnd3 Sub-window weight from num0 to num24
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_aehist_weight_wnd2 Sub-window weight from num0 to num24
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_aehist_weight_wnd1 Sub-window weight from num0 to num24
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_aehist_weight_wnd0 Sub-window weight from num0 to num24

ISP_RAWHIST_LITE_4900_RO_BASE_BIN

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	ro_aehist_bin_x Measured bin count as 28-bit unsigned integer value with 5 fractional part.

12.4.2.25 YNR

YNR_2700_GLOBAL_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	sw_ynr_debug_en Debug signal enable bit
25	RW	0x0	sw_ynr_gate_dis A backdoor for YNR internal gating
24	RW	0x0	sw_ynr_thumb_mix_cur_en Pre thumb data mix current frame thumb data enable bit
23:20	RW	0x8	sw_ynr_global_gain_alpha Global gain alpha for YNR 1i,3f data range:[0,8]. Gain = (sw_ynr_global_gain_alpha * sw_ynr_global_gain + (8-sw_ynr_global_gain)*local_gain)>>3
19:18	RO	0x0	reserved
17:8	RW	0x010	sw_ynr_global_gain Global gain for YNR 6i,4f
7:6	RW	0x0	sw_ynr_flt1x1_bypass_sel 2'b00: lgft3x3_data 2'b01: bft3x3_data 2'b10: gauss_data
5	RW	0x0	sw_ynr_sft5x5_bypass YNR SFT5X5 bypass bit
4	RW	0x0	sw_ynr_flt1x1_bypass YNR FT1X1 bypass bit
3	RW	0x0	sw_ynr_lgft3x3_bypass YNR LGFT3X3 bypass bit
2	RW	0x0	sw_ynr_lbft5x5_bypass YNR LBFT5X5 bypass bit
1	RW	0x0	sw_ynr_bft3x3_bypass YNR BFT3X3 bypass bit
0	RW	0x0	sw_ynr_en YNR enable bit

YNR_2700_RNR_MAX_R

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x3754	sw_ynr_rnr_max_r 9 bit integer and 5 bit fraction M(9bit),E(5bit).1/R^2= M/(2^E) ,M and E will be calculated automatically by driver. Use RNR module when no exgain. RNR module will reduce the influence of LSC.

YNR_2700_LOWNR_CTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0100	sw_ynr_low_bf_inv1 5 bit integer and 9 bit fraction. This signal will adjust the strength of bilateral filtering of LBFT5X5 module.Note: this signal is reciprocal value which means the smaller of this signal, the bigger of reducing noise function.
15:14	RO	0x0	reserved
13:0	RW	0x0100	sw_ynr_low_bf_inv0 5 bit integer and 9 bit fraction. This signal will adjust the strength of bilateral filtering of BFT3X3 module. Note: this signal is reciprocal value which means the smaller of this signal, the bigger of reducing noise function.

YNR_2700_LOWNR_CTRL1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	sw_ynr_low_peak_supress 1 bit integer and 7 bit fraction. This signal will adjust restrain the big hot pixel. The bigger of this signal, the more strength of reducing the isolated big hot pixel.
15:11	RO	0x0	reserved
10:0	RW	0x080	sw_ynr_low_thred_adj 5 bit integer and 6 bit fraction. Adjust the threshold of low frequency filter. The bigger this signal, the stronger reduing noise.

YNR_2700_LOWNR_CTRL2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x010	sw_ynr_low_dist_adj 7 bit integer and 2 bit fraction. Adjust the distance weight of LBFT5X5 bilateral filter . The bigger of this sinal, the smaller of reduing noise effect.
15:10	RO	0x0	reserved
9:0	RW	0x007	sw_ynr_low_edge_adj_thresh 11 bit integer, and 0 bit fraction. Adjust the edge weight of LBFT5X5 bilateral filter . The bigger of this signal, the smaller of reduing noise effect.

YNR_2700_LOWNR_CTRL3

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	sw_ynr_low_bi_weight 1 bit integer and 7 bit fraction, use for ori ydata merge with bft3x3 outdata. The bigger of this signal, the bigger strength of low frequency reduing noise.
23:16	RW	0x64	sw_ynr_low_weight 1 bit integer and 7 bit fraction. The weight of reducing value. The bigger of this signal, the bigger strength of low frequency reducing noise.
15:11	RO	0x0	reserved
10:0	RW	0x133	sw_ynr_low_center_weight 1 bit integer and 10 bit fraction. The weight of LBFT5X5 module of center data. The bigger of this signal, the smaller strength of low frequency reduing noise.

YNR_2700_HIGHNR_CTRL0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RW	0x3a	sw_ynr_hi_min_adj 0 bit integer and 6 bit fraction. This signal is used for holding the edge of stripes. The bigger this signal, the stronger holding the edge of stripes.
15:11	RO	0x0	reserved
10:0	RW	0x080	sw_ynr_high_thred_adj 5 bit integer and 6 bit fraction. Adjust the threshold of high frequency filter. The bigger this signal, the stronger reduing noise.

YNR_2700_HIGHNR_CTRL1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x6e	sw_ynr_high_retain_weight 1 bit integer and 7 bit fraction. This signal is used for holding the high frequency noise . The bigger this signal, the smaller strength of reduing high frequency noise.
15:8	RO	0x0	reserved
7:0	RW	0x64	sw_ynr_hi_edge_thed 8 bit integer. Adjust the threshold of high frequency filter. The bigger this signal, the weaker of reduing noise.

YNR_2700_HIGHNR_BASE_FILTER_WEIGHT

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x8	sw_ynr_base_filter_weight2 0 bit integer and 4 bit fraction(max15)
15:13	RO	0x0	reserved
12:8	RW	0x0f	sw_ynr_base_filter_weight1 0 bit integer and 5 bit fraction(max31)
7	RO	0x0	reserved
6:0	RW	0x12	sw_ynr_base_filter_weight0 1 bit integer and 6 bit fraction

YNR_2700_GAUSS1_COEFF

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x054	sw_ynr_low_gauss1_coeff2 1 bit integer and 8 bit fraction
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_ynr_low_gauss1_coeff1 0 bit integer and 6 bit fraction
7:6	RO	0x0	reserved
5:0	RW	0x0b	sw_ynr_low_gauss1_coeff0 0 bit integer and 6 bit fraction

YNR_2700_GAUSS2_COEFF

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x040	sw_ynr_low_gauss2_coeff2 1 bit integer and 8 bit fraction
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_ynr_low_gauss2_coeff1 0 bit integer and 6 bit fraction
7:6	RO	0x0	reserved
5:0	RW	0x10	sw_ynr_low_gauss2_coeff0 0 bit integer and 6 bit fraction

YNR_2700_DIRECTION_W_0_3

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x08	sw_ynr_direction_weight3 1 bit integer and 4 bit fraction
23:21	RO	0x0	reserved
20:16	RW	0x08	sw_ynr_direction_weight2 1 bit integer and 4 bit fraction
15:13	RO	0x0	reserved
12:8	RW	0x08	sw_ynr_direction_weight1 1 bit integer and 4 bit fraction
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_ynr_direction_weight0 1 bit integer and 4 bit fration

YNR_2700_DIRECTION_W_4_7

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	sw_ynr_direction_weight7 1 bit integer and 4 bit fraction
23:21	RO	0x0	reserved
20:16	RW	0x04	sw_ynr_direction_weight6 1 bit integer and 4 bit fraction
15:13	RO	0x0	reserved
12:8	RW	0x04	sw_ynr_direction_weight5 1 bit integer and 4 bit fraction
7:5	RO	0x0	reserved
4:0	RW	0x04	sw_ynr_direction_weight4 1 bit integer and 4 bit fration

YNR_2700_SGM_DX_0_1

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x040	sw_ynr_luma_points_x1 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x000	sw_ynr_luma_points_x0 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_2_3

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0c0	sw_ynr_luma_points_x3 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x080	sw_ynr_luma_points_x2 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_4_5

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x140	sw_ynr_luma_points_x5 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x100	sw_ynr_luma_points_x4 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_6_7

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x1c0	sw_ynr_luma_points_x7 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x180	sw_ynr_luma_points_x6 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_8_9

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x240	sw_ynr_luma_points_x9 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x200	sw_ynr_luma_points_x8 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_10_11

Address: Operational Base + offset (0x0055)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x2c0	sw_ynr_luma_points_x11 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x280	sw_ynr_luma_points_x10 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_12_13

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x340	sw_ynr_luma_points_x13 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x300	sw_ynr_luma_points_x12 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_14_15

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x3c0	sw_ynr_luma_points_x15 Sigma point x coordinate [0-1024]
15:11	RO	0x0	reserved
10:0	RW	0x380	sw_ynr_luma_points_x14 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_16

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x400	sw_ynr_luma_points_x16 Sigma point x coordinate [0-1024]

YNR_2700_LSGM_Y_0_1

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_ynr_lsgm_y1 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x04c	sw_ynr_lsgm_y0 4bit unsigned, 9bit integer and 5bit fraction. The interval widths in x directon are defined in SGM_DX_1_8 or SGM_DX_9_16

YNR_2700_LSGM_Y_2_3

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_lsgm_y3 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0d0	sw_ynr_lsgm_y2 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_4_5

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_lsgm_y5 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0e8	sw_ynr_lsgm_y4 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_6_7

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0cc	sw_ynr_lsgm_y7 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0d8	sw_ynr_lsgm_y6 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_8_9

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0c0	sw_ynr_lsgm_y9 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0c4	sw_ynr_lsgm_y8 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_10_11

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0b8	sw_ynr_lsgm_y11 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0bc	sw_ynr_lsgm_y10 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_12_13

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a4	sw_ynr_lsgm_y13 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0b4	sw_ynr_lsgm_y12 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_14_15

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x054	sw_ynr_lsgm_y15 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x088	sw_ynr_lsgm_y14 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_LSGM_Y_16

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x028	sw_ynr_lsgm_y16 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_0_1

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_ynr_hsgm_y1 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x04c	sw_ynr_hsgm_y0 14bit unsigned, 9bit integer and 5bit fraction. The interval widths in x directon are defined in SGM_DX_1_8 or SGM_DX_9_16

YNR_2700_HSGM_Y_2_3

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_hsgm_y3 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0d0	sw_ynr_hsgm_y2 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_4_5

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	sw_ynr_hsgm_y5 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0e8	sw_ynr_hsgm_y4 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_6_7

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0cc	sw_ynr_hsgm_y7 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0d8	sw_ynr_hsgm_y6 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_8_9

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0c0	sw_ynr_hsgm_y9 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0c4	sw_ynr_hsgm_y8 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_10_11

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0b8	sw_ynr_hsgm_y11 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0bc	sw_ynr_hsgm_y10 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_12_13

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a4	sw_ynr_hsgm_y13 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x0b4	sw_ynr_hsgm_y12 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_14_15

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x054	sw_ynr_hsgm_y15 14bit unsigned, 9bit integer and 5bit fraction
15:12	RO	0x0	reserved
11:0	RW	0x088	sw_ynr_hsgm_y14 14bit unsigned, 9bit integer and 5bit fraction

YNR_2700_HSGM_Y_16

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x028	sw_ynr_hsgm_y16 14bit unsigned, 9bit intege r and 5bit fraction

YNR_2700_RNR_STRENGTH03

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength3 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength2 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength1 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength0 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH47

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength7 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength6 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength5 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength4 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH8b

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength11 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength10 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength9 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength8 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTHcf

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_ynr_rnr_strength15 4 bit integer and 4 bit fraction
23:16	RW	0x10	sw_ynr_rnr_strength14 4 bit integer and 4 bit fraction
15:8	RW	0x10	sw_ynr_rnr_strength13 4 bit integer and 4 bit fraction
7:0	RW	0x10	sw_ynr_rnr_strength12 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH16
Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x10	sw_ynr_rnr_strength16 4 bit integer and 4 bit fraction

12.4.2.26 CNR

ISP_CNR_2800_CTRL
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_cnr_en_shd Cnr enable shadow register.
30:5	RO	0x0	reserved
4	RW	0x0	sw_cnr_thumb_mix_cur_en 32SD thumb use cur frame mix last frame data enable: 1'b1:mix is enable 1'b0:mix is diable Read back is shodow register.
3	RW	0x0	sw_cnr_lq_bila_bypass low frequence bilateral 3x3 filter bypass enable signal 1'b1:bypass is enable, out_data is equal to in_data in this 3x3 fiter. 1'b0:bypass is disable. Read back is shodow register.
2	RW	0x0	sw_cnr_hq_bila_bypass high frequence bilateral 5x5 filter bypass enable signal 1'b1:bypass is enable, out_data is equal to in_data in this 5x5 fiter. 1'b0:bypass is disable. Read back is shodow register.
1	RW	0x1	sw_cnr_exgain_bypass External gain bypass enable signal 1'b1:bypass is enable, external gain value is fixed to sw_cnr_egain_mux 1'b0:bypass is disable,use external gain. Current version is not support bypass disable. Read back is shodow register.
0	RW	0x0	sw_cnr_en_i CNR enable signal 1'b1:cnr enable 1'b0:cnr disable

ISP_CNR_2800_EXGAIN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x80	sw_cnr_exgain_mux fix external gain value to sw_cnr_exgain_mux

ISP_CNR_2800_GAIN_PARA

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x16	sw_cnr_gain_iso To enlarge external gain, range from 0~128
15:13	RO	0x0	reserved
12:8	RW	0x0c	sw_cnr_gain_offset gain offset of low pass filter in gain cal, range from 0~16
7:0	RW	0x3c	sw_cnr_gain_1sigma Enlarge the output data of high pass filter in gain cal

ISP_CNR_2800_GAIN_UV_PARA

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:8	RW	0x40	sw_cnr_gain_uvgain1 uvgain parameter1
7	RO	0x0	reserved
6:0	RW	0x30	sw_cnr_gain_uvgain0 uvgain parameter0

ISP_CNR_2800_LMED3

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x03	sw_cnr_lmed3_alpha weight of in_data in low frequence median filter,range from 0~16

ISP_CNR_2800_LBF5_GAIN

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x1	sw_cnr_lbf5_gain_y y gain of lbf5x5 bialteral filter
7:6	RO	0x0	reserved
5:0	RW	0x02	sw_cnr_lbf5_gain_c uv gain of lbf5x5 bialteral filter

ISP_CNR_2800_LBF5_WEITD0_3

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x4d	sw_cnr_lbf5_weit_d3 Spatial weight of distance 4 or 5, range from 0~128
23:16	RW	0x63	sw_cnr_lbf5_weit_d2 Spatial weight of pix6,8,16,18, range from 0~128
15:8	RW	0x70	sw_cnr_lbf5_weit_d1 Spatial weight of pix7,11,13,17, range from 0~128
7:0	RW	0x80	sw_cnr_lbf5_weit_d0 Spatial weight of pix12, range from 1~128

ISP_CNR_2800_LBF5_WEITD4

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x2f	sw_cnr_lbf5_weit_d4 Spatial weight of pix0,4,20,24, range from 0~128

ISP_CNR_2800_HMED3

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x03	sw_cnr_hmed3_alpha weight of in_data in high frequence median filter, range from 0~16

ISP_CNR_2800_HBF5

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	sw_cnr_hbf5_weit_src in_data weight of hbf5x5, range from 0~128
23:16	RW	0x00	sw_cnr_hbf5_min_wgt hbf5x5 weit_r low limit
15:13	RO	0x0	reserved
12:0	RW	0x0438	sw_cnr_hbf5_sigma sigma of hbf5x5

ISP_CNR_2800_LBF3

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x80	sw_cnr_lbf5_weit_src in_data weight of lbf3x3, range from 0~128
15:13	RO	0x0	reserved
12:0	RW	0x0438	sw_cnr_lbf3_sigma sigma of hbf3x3

12.4.2.27 Sharp

SHARP_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_sharp_bypass_shd 1'b0: Not bypass 1'b1: Bypass
30	RO	0x0	ro_sharp_en_shd 1'b0: Disable 1'b1: Enable
29	RO	0x0	ro_sharp_working 1'b0: Not working 1'b1: Working
28:2	RO	0x0000000	reserved
1	RW	0x0	sw_sharp_bypass 1'b0: Not bypass 1'b1: Bypass
0	RW	0x0	sw_sharp_en 1'b0: Disable 1'b1: Enable

SHARP_RATIO

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x28	sw_sharp_sharp_ratio Sharp ratio.
23:16	RW	0x80	sw_sharp_bf_ratio Sharp bilateral filter ratio.It has to be less than or equal to 128.
15:8	RW	0x00	sw_sharp_gaus_ratio Sharp gauss ratio.It has to be less than or equal to 128.
7:0	RW	0x33	sw_sharp_pbf_ratio Sharp pre-bilateral filter ratio.It has to be less than or equal to 128.

SHARP_□LUMA_DX

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x7	sw_sharp_luma_dx7 Distance between point 6 and point 7.The actual distance is equal to 2^sw_sharp_luma_dx7.

Bit	Attr	Reset Value	Description
23:20	RW	0x8	sw_sharp_luma_dx6 Distance between point 5 and point 6.The actual distance is equal to 2^sw_sharp_luma_dx6.
19:16	RW	0x8	sw_sharp_luma_dx5 Distance between point 4 and point 5.The actual distance is equal to 2^sw_sharp_luma_dx5.
15:12	RW	0x7	sw_sharp_luma_dx4 Distance between point 3 and point 4.The actual distance is equal to 2^sw_sharp_luma_dx4.
11:8	RW	0x7	sw_sharp_luma_dx3 Distance between point 2 and point 3.The actual distance is equal to 2^sw_sharp_luma_dx3.
7:4	RW	0x6	sw_sharp_luma_dx2 Distance between point 1 and point 2.The actual distance is equal to 2^sw_sharp_luma_dx2.
3:0	RW	0x6	sw_sharp_luma_dx1 Distance between point 0 and point 1.The actual distance is equal to 2^sw_sharp_luma_dx1. Note :The total distacne must be equal to 1024.

SHARP_PBF_SIGMA_INV_0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x094	sw_sharp_pbf_sigma_inv_2 Sharp pbf sigma inverse 2.
19:10	RW	0x0c1	sw_sharp_pbf_sigma_inv_1 Sharp pbf sigma inverse 1.
9:0	RW	0x115	sw_sharp_pbf_sigma_inv_0 Sharp pbf sigma inverse 0.

SHARP_PBF_SIGMA_INV_1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x078	sw_sharp_pbf_sigma_inv_5 Sharp pbf sigma inverse 5.
19:10	RW	0x065	sw_sharp_pbf_sigma_inv_4 Sharp pbf sigma inverse 4.
9:0	RW	0x094	sw_sharp_pbf_sigma_inv_3 Sharp pbf sigma inverse 3.

SHARP_PBF_SIGMA_INV_2

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x094	sw_sharp_pbf_sigma_inv_7 Sharp pbf sigma inverse 7.
9:0	RW	0x094	sw_sharp_pbf_sigma_inv_6 Sharp pbf sigma inverse 6.

SHARP_BF_SIGMA_INV_0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0f1	sw_sharp_bf_sigma_inv_2 Sharp bf sigma inverse 2.
19:10	RW	0x13b	sw_sharp_bf_sigma_inv_1 Sharp bf sigma inverse 1.
9:0	RW	0x1c7	sw_sharp_bf_sigma_inv_0 Sharp bf sigma inverse 0.

SHARP_BF_SIGMA_INV_1

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0c3	sw_sharp_bf_sigma_inv_5 Sharp bf sigma inverse 5.
19:10	RW	0x0a4	sw_sharp_bf_sigma_inv_4 Sharp bf sigma inverse 4.
9:0	RW	0x0f1	sw_sharp_bf_sigma_inv_3 Sharp bf sigma inverse 3.

SHARP_BF_SIGMA_INV_2

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x0f1	sw_sharp_bf_sigma_inv_7 Sharp bf sigma inverse 7.
9:0	RW	0x0f1	sw_sharp_bf_sigma_inv_6 Sharp bf sigma inverse 6.

SHARP_SIGMA_SHIFT

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x7	sw_sharp_bf_sigma_shift Sharp bf sigma shift bits.
3:0	RW	0x6	sw_sharp_pbf_sigma_shift Sharp pbf sigma shift bits.

SHARP_EHF_TH_0

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x080	sw_sharp_ehf_th_2 Sharp ehf th 2.
19:10	RW	0x080	sw_sharp_ehf_th_1 Sharp ehf th 1.
9:0	RW	0x080	sw_sharp_ehf_th_0 Sharp ehf th 0.

SHARP_EHF_TH_1

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x080	sw_sharp_ehf_th_5 Sharp ehf th 5.

Bit	Attr	Reset Value	Description
19:10	RW	0x080	sw_sharp_ehf_th_4 Sharp ehf th 4.
9:0	RW	0x080	sw_sharp_ehf_th_3 Sharp ehf th 3.

SHARP_EHF_TH_2

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x001	sw_sharp_ehf_th_7 Sharp ehf th 7.
9:0	RW	0x040	sw_sharp_ehf_th_6 Sharp ehf th 6.

SHARP_CLIP_HF_0

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x088	sw_sharp_clip_hf_2 Sharp clip hf 2.
19:10	RW	0x058	sw_sharp_clip_hf_1 Sharp clip hf 1.
9:0	RW	0x040	sw_sharp_clip_hf_0 Sharp clip hf 0.

SHARP_CLIP_HF_1

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0e0	sw_sharp_clip_hf_5 Sharp clip hf 5.
19:10	RW	0x0f8	sw_sharp_clip_hf_4 Sharp clip hf 4.
9:0	RW	0x0b4	sw_sharp_clip_hf_3 Sharp clip hf 3.

SHARP_CLIP_HF_2

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	sw_sharp_clip_hf_7 Sharp clip hf 7.
9:0	RW	0x048	sw_sharp_clip_hf_6 Sharp clip hf 6.

SHARP_PBF_COEF

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x0a	sw_sharp_pbf_coef_2 Sharp pbf coefficient of corner.
15	RO	0x0	reserved
14:8	RW	0x10	sw_sharp_pbf_coef_1 Sharp pbf coefficient of up/down/left/right.

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x18	sw_sharp_pbf_coef_0 Sharp pbf coefficient of center. Note :sw_sharp_pbf_coef_0+4*sw_sharp_pbf_coef_1+4*sw_sharp_pbf_coef_2 must be equal to 128.

SHARP_BF_COEF

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x0a	sw_sharp_bf_coef_2 Sharp bf coefficient of corner.
15	RO	0x0	reserved
14:8	RW	0x10	sw_sharp_bf_coef_1 Sharp bf coefficient of up/down/left/right.
7	RO	0x0	reserved
6:0	RW	0x18	sw_sharp_bf_coef_0 Sharp bf coefficient of center. Note :sw_sharp_bf_coef_0+4*sw_sharp_bf_coef_1+4*sw_sharp_bf_coef_2 must be equal to 128.

SHARP_GAUS_COEF_0

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x06	sw_sharp_gaus_coef_2 Sharp gaus coefficient of corner.
15	RO	0x0	reserved
14:8	RW	0x07	sw_sharp_gaus_coef_1 Sharp gaus coefficient of up/down/left/right.
7	RO	0x0	reserved
6:0	RW	0x0c	sw_sharp_gaus_coef_0 Sharp gaus coefficient of center. Note :sw_sharp_gaus_coef_0+4*sw_sharp_gaus_coef_1+4*sw_sharp_gaus_coef_2 must be equal to 128.

12.5 Application Notes

12.5.1 MIPI

For register update, the signal force_update comes from ISP MI module, and achieves automatic update of channel's frame end.
Under different modes, the hardware will complete adaptive configuration for some register combinations.
Using mipi mode, configure VI_DPCL[9:8] if_select = 2 in MAIN_CONTROL (0X0000).
CSI2RX register base address is 0x1c00.
For especial HDR sensor:
Configure DATA_IDS_1.sw_csi_id0[5:0] = data_type (e.g. raw8, raw10, raw12...)
If sensor AR0239, configure sw_hdr_esp_mode = 1.
If sensor IMX327, configure sw_hdr_esp_mode = 2.
Note: all mode support especial HDR sensor.

12.5.1.1 normal mode (Single ID)

For this mode:
Configure sw_ibuf_op_mode = 0.
All dmatx are available, but all dmarx are unavailable.
For example: raw10, lanex4

CTRL0 = 0x0. (if sensor AR0239, CTRL0 = 0X4; if sensor IMX327, CTRL0 = 0X8)
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.

12.5.1.2 frame_x2_ddr mode (2IDs--hdr mode)

For this mode:
Configure sw_ibuf_op_mode = 8.
For example: raw10, lanex4
CTRL0 = 0x800.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP_MI register for address and size:
RAW0_WR_BASE = "dmatx0 base address in DDR"
RAW0_WR_SIZE = "pic_width*pic_height*1.5"

12.5.1.3 line_x2_ddr_mode (2IDs--hdr mode)

For this mode:
Configure sw_ibuf_op_mode = 9.
For example: raw10, lanex4
CTRL0 = 0x900.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP_MI register for address and size:
RAW0_WR_BASE = "dmatx0 base address in DDR"
RAW0_WR_SIZE = "pic_width*pic_height*1.5"

12.5.1.4 line_x2_noddr mode (2IDs--hdr mode)

For this mode:
Configure sw_ibuf_op_mode = 10.
For example: raw10, lanex4
CTRL0 = 0xa00.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.

12.5.1.5 user mode

For this mode:
Configure sw_ibuf_op_mode = 3.
User defined mode. All dmatx and dmarx are available.

12.5.1.6 raw_rdback_framex1 mode

For this mode:
Configure sw_ibuf_op_mode = 4.
For example: raw10, lanex4 (all dmatx configurable, recommend dmatx2)
CTRL0 = 0x400.
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.
RAW2_WR_CTRL = 0x101.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x1
RAW2_WR_BASE = "dmatx2 base address in DDR"
RAW2_WR_SIZE = "pic_width*pic_height*1.5"
RAWS_RD_BASE = RAW2_WR_BASE
Then, the time to start dmarxs is up to the user (maybe dmatx2 frame end):
Configure CTRL0 = 0x401.

12.5.1.7 raw_rdback_framex2 mode (hdr mode)

For this mode:
Configure sw_ibuf_op_mode = 5.
For example: raw10, lanex4 (all dmatx configurable, recommend dmatx2 and dmatx0)

CTRL0 = 0x500.
CTRL1 = 0x103.
DATA_IDS_1 = 0x6b2b.
RAW2_WR_CTRL = 0x101.
RAW0_WR_CTRL = 0x201.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x3
RAW2_WR_BASE = "dmatx2 base address in DDR"
RAW2_WR_SIZE = "pic_width*pic_height*1.5"
RAW0_WR_BASE = "dmatx0 base address in DDR"
RAW0_WR_SIZE = "pic_width*pic_height*1.5"
RAWS_RD_BASE = RAW2_WR_BASE
RAW0_RD_BASE = RAW0_WR_BASE
Then, the time to start dmarxs is up to the user (maybe both dmatx2 and dmatx0 frame end):
Configure CTRL0 = 0x501.

12.5.2 MI

Three are three points to note:
1) The signal sw_mi_wr_init_offset_en in MI_WR_CTRL register needs to be set to 1, otherwise, the address of MI will not be updated.
2) If output address need ping-pong, the signal sw_mp_wr_auto_upd in MI_WR_CTRL register needs to be set to 1.
3) The signal sw_mi_cfg_upd in MI_WR_INIT register needs to be set to 1 after all MI registers configuration complete when it is the first frame.
4) The respective force update(sys_dbrself_force_upd、sys_gainself_force_upd、sys_bay3dself_force_upd) is added to the register MI_WR_CTRL2, can be used to update the enable signal and shadow address.

12.5.3 HDRMGE

1) HDR-merge global register configuration：
Enable and select mode, choose gain or Anti-gain, other configurations such as curves use the default typical value.
2) Curves：
L curve: The first quarter is divided into 16 sections; other is equal to 1023.
S curve: Middle 1/2 divided into 16 sections; other is equal to 1023.
E curve: Last 1/2 divided into 16 segments; other is equal to 0.
3) Software configuration：
sw_hdr_mode: 0:noraml; 1:framex2; 2:framex3
sw_hdr_lightz =0.1*(short_gain/16)^3)
sw_hdr_gain2 =1
sw_hdr_gain1 = exposure_L÷exposure_M; (Anti-gain1 is1/gain1)
sw_hdr_gain0 = exposure_L÷exposure_S ; (Anti-gain0 is1/gain0)
sw_hdr_lightzone = 0.1*(short_gain/16)^3
light_zone = img_short > sw_hdr_lightzone= 0.1*(short_gain/16)^3

12.5.4 BayerNR

1) Configure sw_rawnr_en_i to 1 to turn on rawnr module.
2) According to HDR mode or not, configure sw_rawnr_log_bypass.
3) Except for the enable switch, all parameters are determined by ISO, and the post configuration needs to be obtained from the C_model. The parameter tables corresponding to different ISO are given below for reference. After reset, the ISO is equal to 50.

15.1.1 HDR-DRC

HDR-DRC global register configuration:
Enabling and select mode, lgscl and lgscl_inv, other configurations such as curves use the default typical value.

15.1.2 GIC

User can open GOC module through ISP top,in this case GIC will work in a usual ISO

situation with value 50 when reset.
If outside environment is too dark or too bright, then you need configure the coefficient register in the reg block from CPU. All the register value need acquire by c_model first.
Following are GIC register values (decimal system):

Table 12-3 GIC parameters

Registers	ISO100	ISO200	ISO400
sw_gic_en	1	1	1
sw_regminbusy_thre	160	160	160
sw_regmingrad_thrdark1	64	64	64
sw_regmingrad_thrdark2	32	32	32
sw_regdark_threhi	960	960	960
sw_regmaxcorv_both	80	80	80
sw_regdark_thre	480	480	480
sw_reggb_thre	7	7	6
sw_regkgrad1	5	5	5
sw_regkgrad2	1	1	1
sw_regdark_threstep	9	9	9
sw_regstrenth_global_fix	8	8	8
sw_regkgrad1_dark	6	6	6
sw_regkgrad2_dark	1	1	1
sw_regmingrad_thr1	32	32	32
sw_regmingrad_thr2	32	32	32
sw_regmaxcov	40	64	96
sw_regluma_points_step	7	7	7
sw_dnhi_scale	128	128	128
sw_dnlo_scale	102	102	102
sw_fusion_rationhi_limit	96	96	96
sw_gvalue_limit_hi	1760	1760	1760
sw_gvalue_limit_lo	1280	1280	1280
regstrength_fix	128	128	128
sw_sigma_y0	0	153	0
sw_sigma_y1	702	935	0
sw_sigma_y2	1000	1313	1947
sw_sigma_y3	1228	1605	1947
sw_sigma_y4	1420	1851	2754
sw_sigma_y5	1589	2068	2754
sw_sigma_y6	1741	2264	3374
sw_sigma_y7	1881	2445	3374
sw_sigma_y8	2012	2613	3896
sw_sigma_y9	2466	3199	3896
sw_sigma_y10	2848	3693	5511
sw_sigma_y11	3185	4128	5511
sw_sigma_y12	3490	4522	6749
sw_sigma_y13	3770	4884	6749
sw_sigma_y14	4030	5220	7794

15.1.3 DEBAYER

The debayer module has four important regiter configurations:
1) sw_debayer_en: When it is 0, it corresponds to black and white mode; when it is 1, it corresponds to RGB mode.
2) sw_debayer_filter_g_en: When it is 0, G filter module will be bypassed.
3) sw_debayer_filter_c_en: When it is 0, C filter module will be bypassed.
4) sw_debayer_clip_en: Determine whether the horizontal and vertical interpolation result will clip according to the maximum value in the window when G interpolation.
The rest of the configuration is to adjust the algorithm effect. The following points need to be noted：

1）sw_debayer_filter1_coe and sw_debayer_filter2_coe is a signed number, the value range is -8~7.
2）sw_debayer_order_max has to be bigger than sw_debayer_order_min, and the difference value has to be 3, 5, 9, 17 when sw_debayer_shift_num is 0, 1, 2, 3 respectively.
3）The step of sw_debayer_max_ratio is 1/4, the step of sw_debayer_dist_scale is 1/8, the step of sw_debayer_thed0 and sw_debayer_thed1 is 1/32.

15.1.4 CCM

1) Set sw_ccm_en_i to 1, open CCM module, otherwise, CCM moduel will be close, and data path will be bypassed.
2) Signals sw_ccm_coeff0_r [10:0]~ sw_ccm_coeff2_b[10:0] are CCM 3x3 matrix parameters. These nine parameters are all 11 bit signed numbers which have 7 bit decimal places. The range is[-8,7.992].
3) Signals sw_ccm_offset_r[11:0], sw_ccm_offset_g[11:0], and sw_ccm_offset_b[11:0] are offsets in calculation, which are 12 bit signed integers.
4) Signals sw_ccm_coeff0_y[10:0]~sw_ccm_coeff2_y[10:0] are RGB2Y parameters, which are 11bit signed number with 7bit decimal, range from -2 to 1.992.
5) Signals sw_ccm_alp_y0[10:0]~sw_ccm_alp_y16[10:0] are 17 vertices of 16 segment alpha interpolation curve.
6) Signals sw_ccm_bound_bit[4:0] is alpha power exponent configuration of inflexion of interpolation curve. The value of the inflection point is2^sw_ccm_bound_bit, range from 0 to 4.

15.1.5 GAMMA_OUT

The GAMMA_OUT module is opened when user sets sw_gamma_out_en to 1.This module is realized by interpolation.
When sw_gamma_out_equ is asserted to 1, the segment length of x orientation is equal and the curve uses 32 segments.
When sw_gamma_out_equ is asserted to 0, the segment length of x orientation is not equal and the curve uses 44 segments.

15.1.6 DHAZ

1) Set sw_dhaz_en to be 1, open dehaze module.
2) When sw_dhaz_en is 1, set sw_dhaz_dc_en to be 1, then open dark channel function.
3) When sw_dhaz_en is 1, set sw_dhaz_hist_en to be 1, turn on histogram equalization. When sw_dhaz_hist_en is 1, and sw_dhaz_hpara_en==1, the sw_dhaz_hist_scale need to be configured too.
4) When sw_dhaz_enhance_en==1, sw_dhaz_enhance_value need to be configured too.
5) Control the number of iterative frames sw_dhaz_stab_fnum for IIR, the corresponding sigma parameters can be configured according to the user's requirements, but it should not exceed the bit width and the minimum value is 1.
6) sw_dhaz_iir_pre_wet is used for dark channel IIR, the corresponding factors can be configured according to the user's requirements, but it should not exceed the bit width and the minimum value is 1.
7) If the user only needs adaptive processing, then set sw_dhaz_cfg_alpha to zero, otherwise, sw_dhaz_cfg_air, sw_dhaz_cfg_wt, sw_dhaz_cfg_tmax and sw_dhaz_cfg_gratio need to be configured by software.

15.1.7 3DLUT

The 3DLUT module is opened when user sets sw_lut3d_en to 1.
The LUT of this module is updated by setting sw_lut3d_lut_update_en to 1.

15.1.8 AF

The AF module is opened when user sets sw_rawaf_en to 1. This module includes Gamma and Gaus Filter which are opened by sw_gamma_en and sw_gaus_en separately. There are 15x15 windows here which is configurable by user, and each window statistic the AF result independently.
User needs set 1 to sw_rawaf_meas_flag to clear this signal, after one frame is finished and the statistic data is read by user.

15.1.9 AE

Two versions of AE are named RAWAE_BIG and RAWAE_LITE here. The mean of reading

back statistic is different. RAWAE_LITE uses normal method which give a address and then read back. RAWAE_BIG read the fix address RO_MEAN_BASE_ADDR 225 times. RAWAE_BIG supports 15x15 window grid, it still support 4 separated windows.
ModuleA(RAWAE_LITE or RAWAE_BIG) needs config as follows:
1) Config ModuleA window size, window offset, and other signals.
2) Set sw_ModuleA_en signal to 1.
3) Waiting for ModuleA's interruption.
4) Read back the statistics data when the interruption is 1.
5) Write 1 to sw_ModuleA_done to clear this signal.
6) Waiting for the interruption of next frame.
Here have some constraints for AE:
1) The sub window size and offset must even.
2) The Minimum of sub window is 16x4.
3) The 4 separated window config coordinate directly instead of window size.

15.1.10 AWB

1)Data Pre-Process
RAWAWB input data is 10 bit raw format and the input picture could crop by the crop module. The cropped picture should aligning at the down sample window size, 4 or 8 configurable, and the hardware would guarantee this by force.The RGB data down sampled from RAW data and y data converted from RGB data will do some limitation(the limitation is configurable) and then output to detection module.
2)White Point Detection
There are three region white point detection method, xy region, uv region and yuv region. The xy and uv region detection are used for all 7 lights, but yuv detection is only used for 4 lights. The each 4 lights number is configurable by sw_rawawb_3dyuv_ls_idx0 to sw_rawawb_3dyuv_ls_idx3. The left 3 lights white point detection are disable in yuv region and it wouldn't affect the white point detection result in uv and xy region.The enable of three detection method is configurable too.
3)Block Measurement
The down sampled picture would divide into 15x15 blocks and then accumulate the each block input data. The input data could been down sampled data, xy white point data or uv white point data and it is configured by sw_rawawb_blk_measure_mode. The block will measure three lights white point detection result too and this three lights are selected by sw_rawawb_store_wp_flag_ls_idx0 to sw_rawawb_store_wp_flag_ls_idx2.
4)Data Read Back
The all measurement information could read back to software by AHB BUS. When the measurement is over the hardware will pull up the sw_rawawb_meas_done signal. And then the software could read back all the information. The software should pull the signal down by setting this signal to 1 when read is over. The next frame measurement is valid only if the sw_rawawb_meas_done is 0 before the next frame start.

15.1.11 HIST

Two versions of HIST are named RAWHIST_BIG and RAWHIST_LITE here. The mean of reading back statistic is same for them. Both need reads the fix address RO_BASE_BIN 256 times when read back.
ModuleA(RAWHIST_LITE or RAWHIST_BIG) needs config as follows:
1) Config ModuleA window size, window offset, and other signals.
2) Set sw_ModuleA_en signal to 1.
3) Waiting for ModuleA's interruption.
4) Read back the statistics data when the interruption is 1.
5) Write 1 to sw_ModuleA_done to clear this signal.
6) Waiting for the interruption of next frame.
Here have some constraints for HIST:
1) The sub window size and offset must even.
2) When user sets the weights of RAWHIST_BIG, sw_config_wram_en bit needs set to1 ahead.
3) The coefficient sw_rawae_gcc needs half because there are two G(Gr, Gb) in the RAW2Y formula.

15.1.12 IRQ

There are three important interrupt registers in ISP. One offset address is 0x400+0x1c4, which named ISP_MIS. Another offset address is 0x400+0x1d8, which named ISP3A_MIS. The last offset address is 0x1400+0x100, which means MI_MIS.
The following chart shows the interrupt sequence between several interrupts:

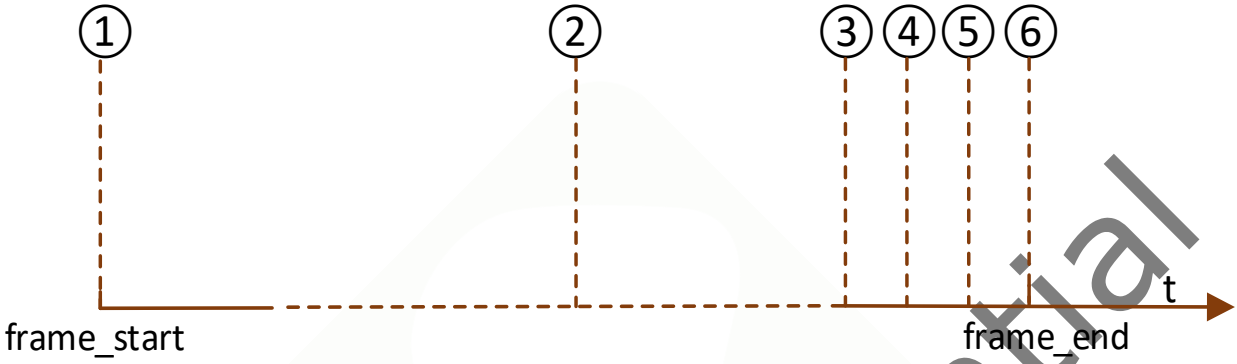


Fig. 12-6 interrupt sequence

The meanings of the above numerical symbols are as follows:

Table 12-4 meanings of IRQ

No.	Interrupt name	Registers name	Meaning
①	MIS_V_START	ISP_MIS	start edge of v_sync，pull up time is the same as first pixel valid is ISP
②	MIS_RAWXX_DONE	ISP3A_MIS	3A module done signal
③	MIS_FRAME_IN	ISP_MIS	INFORM module frame end signal
④	MIS_HDR_DONE	ISP_MIS	HDR module frame end signal
⑤	MIS_FRAME_OUT	ISP_MIS	ISP module frame end signal
⑥	mp_frame_end/mpfbc_wr_frame_end	MI_MIS	MI module frame end signal

MIS_RAWXX_DONE of above table indicates different 3A interrupts, which interrupt time are determined by the size of the window in different 3A module.
The No.6 choose mp_frame_end or mpfbc_wr_frame_end is determined by whether the MPFBC module is open. If MPFBC is open, then the end of one frame flag is mpfbc_wr_frame_end.

15.1.13 SHD_REG

All shadow register are list in following table:

Signal	In which module	Registers addr	Bit	Meaning
sw_csi_raw0_wr_en_shd	MIPI	0X1C40	31	Raw0_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to ddr. 1'b1: Enable the channel 1'b0: Disable teh channel
sw_csi_raw1_wr_en_shd	MIPI	0X1C50	31	Raw1_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to ddr. 1'b1: Enable the channel

Signal	In which module	Registers addr	Bit	Meaning
				1'b0: Disable teh channel
sw_csi_raw2_wr_en_shd	MIPI	0X1C60	31	Raw2_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to ddr. 1'b1: Enable the channel 1'b0: Disable teh channel
sw_csi_raw3_wr_en_shd	MIPI	0X1C70	31	Raw3_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to ddr. 1'b1: Enable the channel 1'b0: Disable teh channel
path_enable_in	MI	0x1474	3:0	path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)
path_enable_out	MI	0x1474	19:16	path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
sw_mp_wr_y_base_shd	MI	0x1478	31:4	Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_size_shd	MI	0X147C	28:4	Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_y_offs_cnt_shd	MI	0x1480	28:4	Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_y_irq_offs_shd	MI	0x1484	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_base_shd	MI	0x1488	31:4	Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-

Signal	In which module	Registers addr	Bit	Meaning
				aligned access.
sw_mp_wr_cb_size_shd	MI	0x148C	27:4	Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_offs_cnt_shd	MI	0x1490	27:4	Current offset counter of main picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_base_shd	MI	0x1494	31:4	Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_size_shd	MI	0x1498	27:4	Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_offs_cnt_shd	MI	0x149C	27:4	Current offset counter of main picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_base_shd	MI	0x14A0	31:4	Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_size_shd	MI	0x14A4	28:4	Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_offs_cnt_shd	MI	0x14A8	28:4	Current offset counter of self picture Y component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_base_shd	MI	0x14B0	31:4	Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access.

Signal	In which module	Registers addr	Bit	Meaning
sw_sp_wr_cb_size_shd	MI	0x14B4	27:4	Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_offs_cnt_shd	MI	0x14B8	27:4	Current offset counter of self picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_base_shd	MI	0x14BC	31:4	Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_size_shd	MI	0x14C0	27:4	Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_offs_cnt_shd	MI	0x14C4	27:4	Current offset counter of self picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_irq_offs2_shd	MI	0x15E4	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_raw0_wr_base_shd	MI	0x182C	31:4	Base address of raw0 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw1_wr_base_shd	MI	0x183C	31:4	Base address of raw1 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-

Signal	In which module	Registers addr	Bit	Meaning
				aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw2_wr_base_shd	MI	0x184C	31:4	Base address of raw2 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw3_wr_base_shd	MI	0x185C	31:4	Base address of raw3 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw0_rd_base_shd	MI	0x1878	31:4	Base shadow address of raw0 rx data ring buffer
sw_raw1_rd_base_shd	MI	0x1888	31:4	Base shadow address of raw1 rx data ring buffer
sw_raws_rd_base_shd	MI	0x1898	31:4	Base shadow address of raws rx data ring buffer
dbr_wr_base_shd	MI	0x196C	31:4	Base address of mimux wirte data ring buffer. -- DBR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to DBR_WR_BASE register description for details.
dbr_rd_base_shd	MI	0x1978	31:4	Base shadow address of mimux read data ring buffer
gain_wr_base_shd	MI	0x1990	31:4	Base address of gain wirte data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to GAIN_WR_BASE register description for details.
bay3d_wr_base_shd	MI	0x19ac	31:4	Base address of bayer 3dnr wirte data ring buffer. --- BAY3D_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_WR_BASE register description for details.
bay3d_rd_base_shd	MI	0x19b8	31:4	Base shadow address of bayer 3dnr read data ring buffer.
sw_hdrmge_en_shd	HDRMGE	0x3800	31	HDRMGE enable shadow
sw_baynr_en_shd	BayerNR	0x3A00	31	BayerNR enable after shadow 1'b0: Disable 1'b1: Enable
sw_bay3d_en_shd	BAY3D	0x3A80	30	bay3d en shadow
sw_bay3d_exp_s	BAY3D	0x3A80	27	exp curve lut select shadow

Signal	In which module	Registers addr	Bit	Meaning
el_shd				
sw_bay3d_pk_en_shd	BAY3D	0x3A80	29	pk gain select shadow
sw_bay3d_bypass_en_shd	BAY3D	0x3A80	31	sw_bay3d_bypass_en_shd
sw_hdrdrc_en_shd	HDRDRC	0x3900	31	HDRTMO enable shadow, read back
sw_drc_position	HDRDRC	0x3904	13:0	[6,8], pluma scale for table index of gain2raw
sw_adrc_compress_scl	HDRDRC	0x3904	26:14	[2,11] scale plgmax range(0~24576) for trans compress
sw_drc_offset_pow2	HDRDRC	0x3904	31:28	log offset: indata+(1<<offset_pow2), then log2data-offset_pow2
sw_drc_lpdetail_ratio	HDRDRC	0x3908	11:0	[1,11], for delt=(lgt-nglt) + (lgt-maxl)*lpdetail_ratio used
sw_drc_hpdetail_ratio	HDRDRC	0x3908	23:12	[1,11], for delt=delt + gain_scl*hpdetail_ratio used
sw_drc_delta_scalein	HDRDRC	0x3908	31:24	[0,8], for plgt*delta_scalein into scaleTable
sw_drc_weig_bilat	HDRDRC	0x391c	4:0	[1,4], weight for (bilat*W + (16-W)*luma) when bilateral filter out
sw_drc_weig_maxl	HDRDRC	0x391c	12:8	[1,4], weight for (max3x3*W + (16-W)*gas3x3) when bilateral filter in
sw_adrc_gain_y0~g16	HDRDRC	0x3920	31:0	curve_gain2raw y0~y16, {3,10}
sw_adrc_compress_y0~y16	HDRDRC	0x3944	31:0	curve_compress y0~y16
sw_adrc_scale_y0~y16	HDRDRC	0x3968	31:0	curve_scale y0~y16
sw_gic_en_shk	GIC	0x2F00	31	The shadow register of sw_gic_en
sw_debayer_en_shd	DEBAYER	0x2500	24	The shadow register of sw_debayer_en
sw_debayer_filter_g_en_shd	DEBAYER	0x2500	25	The shadow register of sw_debayer_filter_g_en
sw_debayer_filter_c_en_shd	DEBAYER	0x2500	26	The shadow register of sw_debayer_filter_c_en
sw_gamma_out_en_shd	GAMMA_OUT	0x0900	31	sw_gamma_out_en_shd
sw_dhaz_en_shd	DHAZ	0x3C00	31	Dehaze enable shandow
sw_dhaz_dc_en_shd	DHAZ	0x3C60	4	Dehaze dark channel enable shandow
sw_dhaz_hist_en_shd	DHAZ	0x3C60	8	Dehaze hist equilibration enable shandow
sw_dhaz_hpara_en_shd	DHAZ	0x3C60	12	Dehaze hist parameter enable shandow
sw_dhaz_air_lc_shd	DHAZ	0x3C60	16	Dehaze rgb channel separate shandow
sw_dhaz_enhance_en_shd	DHAZ	0x3C60	20	Dehaze enhance enable shandow
sw_lut3d_en_shd	3DLUT	0x3E00	31	sw_lut3d_en_shd

Signal	In which module	Registers addr	Bit	Meaning
scale_hy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	0	1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit
scale_hc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	1	1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
scale_vy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	2	1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
scale_vc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	3	1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
scale_hy_up_shd	SELF_RESIZE	0x0C30, 0x1030	4	1'b1: Horizontal luminance upscaling selected 1'b0: Horizontal luminance downscaling selected
scale_hc_up_shd	SELF_RESIZE	0x0C30, 0x1030	5	1'b1: Horizontal chrominance upscaling selected 1'b0: Horizontal chrominance downscaling selected
scale_vy_up_shd	SELF_RESIZE	0x0C30, 0x1030	6	1'b1: Vertical luminance upscaling selected 1'b0: Vertical luminance downscaling selected
scale_vc_up_shd	SELF_RESIZE	0x0C30, 0x1030	7	1'b1: Vertical chrominance upscaling selected 1'b0: Vertical chrominance downscaling selected
scale_hy_shd	SELF_RESIZE	0x0C34, 0x1034	15:0	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor.
scale_hcb_shd	SELF_RESIZE	0x0C38, 0x1038	15:0	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.
scale_hcr_shd	SELF_RESIZE	0x0C3C, 0x103C	15:0	This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor.
scale_vy_shd	SELF_RESIZE	0x0C40, 0x1040	15:0	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.
scale_vc_shd	SELF_RESIZE	0x0C44, 0x1044	15:0	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.
phase_hy_shd	SELF_RESIZE	0x0C48, 0x1048	15:0	This register is set to the horizontal luminance phase offset
phase_hc_shd	SELF_RESIZE	0x0C4C, 0x104C	15:0	This register is set to the horizontal chrominance phase offset.

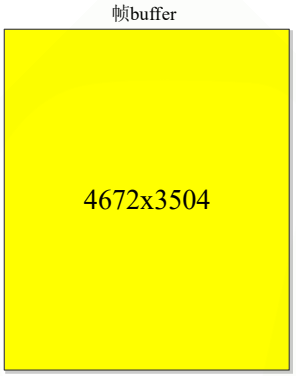
Signal	In which module	Registers addr	Bit	Meaning
phase_vy_shd	SELF_RESIZE	0x0C50, 0x1050	15:0	This register is set to the vertical luminance phase offset.
phase_vc_shd	SELF_RESIZE	0x0C54, 0x1054	15:0	This register is set to the vertical chrominance phase offset.
isp_enable_shd	ISP_CTRL	0x5A8	0	ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)
isp_inform_enable_shd	ISP_CTRL	0x5A8	1	Input formatter enable shadow register
isp_out_h_offs_shd	ISP_CTRL	0x5AC	13:0	Current vertical pic offset in lines
isp_out_v_offs_shd	ISP_CTRL	0x5B0	13:0	Current vertical pic offset in lines
isp_out_h_size_shd	ISP_CTRL	0x5B4	14:0	Current horizontal pic size in pixel
isp_out_v_size_shd	ISP_CTRL	0x5B8	13:0	Vertical pic size in lines
sw_sws_en_shd	SWS	0x1C	30	sw_sws_en_shd
sw_ldch_en_shd	LDCH	0X3B00	31	Module ldch enable signal,shadow.
sw_ynr_en_shd	YNR	0X2700	0	
sw_ynr_bft3x3_bypass_shd	YNR	0X2700	1	bft3x3_bypass enable
sw_ynr_lbft5x5_bypass_shd	YNR	0X2700	2	ynr lbft5x5 bypass
sw_ynr_lgft3x3_bypass_shd	YNR	0X2700	3	ynr lgft3x3_bypass
sw_ynr_flt1x1_bypass_shd	YNR	0X2700	4	ynr flt1x1_bypass
sw_ynr_sft5x5_bypass_shd	YNR	0X2700	5	ynr sft5x5_bypass
sw_cnr_en_shd	CNR	0X2800	0	Cnr enable
sw_cnr_exgain_bypass_shd	CNR	0X2800	1	cnr exgain_bypass
sw_cnr_hq_bila_bypass_shd	CNR	0X2800	2	cnr hq_bila_bypass
sw_cnr_lq_bila_bypass_shd	CNR	0X2800	3	cnr lq_bila_bypass
sw_cnr_thumb_mix_cur_en_shd	CNR	0X2800	4	cnr thumb_mix_cur_en
sw_sharp_en_shd	Sharp	0X2900	30	Sharp enable
sw_sharp_bypass_shd	Sharp	0X2900	31	Sharp bypass

How to update the shaow register:
You can choose to update through forced_upd and frame end update.
The forced UPD is generally used before the start of a frame. The configuration mode is to enable ISP Ctrl, which is the 9th bit of 0x400.
If you need to enable the end of frame update, you need to pull up the 8th bit of 0x400, otherwise it will not be updated by default.
10th bit of 0x400 can update shadow registers only one time while frame_end is coming.

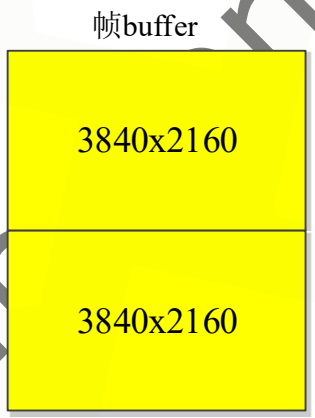
15.1.14 Multi-Sensor

Multi-sensor mainly uses the frame buffers to cache the data of the previous frame to solve the problem of previous frame data caching. The maximum resolution of frame buffer with different sensors is supported as follows.

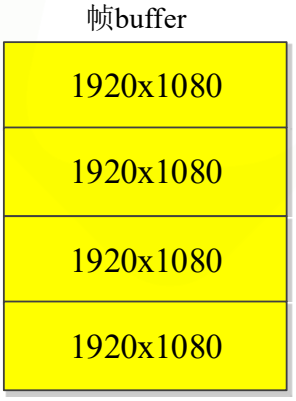
（1）single sensor: the maximum resolution is 4672x3504



（2）dual sensor: The previous frame data is stored by dividing the frame buffer in two, and the storage space is reduced by half. In normal mode, the maximum resolution is 1920x1080, In big mode, the maximum resolution is 3840x2160.



（3）four sensor: The previous frame data is stored by quartering the frame buffer, and the storage space is reduced to one fourth of the original one. In normal mode, the maximum resolution is 960x540, In big mode, the maximum resolution is 1920x1080.



Multi-sensor register configuration at 0X408, and there are two registers to cnfigure:

（1）sw_sensor_mode: used to configure the number of sensor

0:one sensor；
1:two sensor；
2:four sensor.

（2）sw_sensor_index: sensor ID of the current sensor. software is required to number and configure each sensor.

Switching parameters between different sensors need to be configured at the end of current and before of next frame. The shadow register can be configured using force_upd or frame end update. Note：different sensor switch need set first_frame register(0x404) in mult-sensor mode.

CHAPTER 13 VOP

13.1 Overview

VOP2 is the display interface from memory frame buffer to display device. VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface.VOP2 supports the following features:

- Display interface
  - 1 HDMI
    - Max support 4096x2160@60Hz
    - Support RGB/YUV420(up to 10bit) format
  - 1 LVDS
    - Max support 1280x800@60Hz
    - Support RGB(up to 8bit) format
  - 1 EDP
    - Max support 2560x1600@60Hz
    - Support RGB(up to 10bit) format
  - 2 MIPI
    - Max support 1920x1080@60Hz per channel
    - Support RGB(up to 8bit) format
    - Support dual MIPI: left-right mode.
    - Dual MIPI support 2048x1536@60Hz
  - 1 BT656
    - support PAL and NTSC
    - Support RGB(up to 8bit) format
  - 1 RGB/BT1120
    - Max support 1920x1080@60Hz
    - Support RGB(up to 8bit) format

- BUS
  - One 32bit AHB Slave to configure registers
  - Two 128bit AXI read bus
  - One 128bit AXI write bus
- Video ports
  - Video port0
    - Resolution
      - Max output resolution: 4096x2304@60Hz
      - Bits per component: 10
    - Color bar
      - Horizontal mode
      - Vertical mode
    - BCSH(10bit)
      - Brightness(8bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
    - 3D_LUT
      - Support 9x9x9(12bit) LUT
    - CSC
      - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
      - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
    - Gamma
    - Dither down
      - Allegro
      - FRC
    - Post scale down for TV over_scanning
      - Horizontal scale down using bilinear, 0.5~1.0
      - Vertical scale down using bilinear, 0.5~1.0
    - Post LB mode
      - 4096pixelx4 mode

        - 2048pixelx8 mode
      - Display mode
        - P2I/Interlace display
        - X-mirror
        - Blank display
        - Black display
        - Standby mode
  - Video port1/2
    - Resolution
      Max output resolution: 1920x1080@60Hz
        - Bits per component: 8
    - Color bar
      - Horizontal mode
      - Vertical mode
    - BCSH(8bit)
      - Brightness(6bit), Contrast(9bit), Saturation(10bit), Hue adjustment(9bit)
    - CSC
      - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
      - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
    - Gamma
    - Dither down
      - Allegro
      - FRC
    - Post scale down for TV over_scan
      - Horizontal scale down using bilinear, 0.5~1.0
      - Vertical scale down using bilinear, 0.5~1.0
    - Post LB mode
      - 2048pixelx4 mode
      - 1024pixelx8 mode
    - Display mode
      - P2I/Interlace display
      - X-mirror
      - Blank display
      - Black display
      - Standby mode
- Cluster0/1
  - Resolution
    - Max input resolution: 4096x2304
    - Max output resolution: 4096x2304
  - Data format
    - AFBCD: RGBA8888/RGB888/RGB565/RGBA1010102/ YUV420/YUV422 8bit/10bit
  - Image
    - Support virtual width(max 8k word)
    - Support active offset
    - Support display offset
    - Support Y-mirror/x-mirror/rotation-90/rotation-270
      - If rotation-90 or rotation-270 is enable, the maximum height of the source image is 2048
    - Swap: RB/UV swap
    - Support YUV clip
  - Cluster mode
    - Mode0: 4k layer mode
    - Mode1: 2*2048 layer mode
    - Mode2: rotation 2048 layer mode
  - Support Gauss filter
  - Scale

        - Scale down
            - Support scale rate 1/4~1
            - Scale mode: bilinear
        - Scale up
            - Support scale rate 1~4
            - Scale mode: bilinear
    - CSC
        - YUV2RGB: bt601-f / bt709-l/bt601-l/bt2020
        - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
- ESMART0/1
    - Resolution
        - Max input resolution: 4096x2304
        - Max output resolution: 4096x2304
    - Data format
        - RGB: ARGB8888/RGB888/RGB565
        - YUV: YUV420/YUV422/YUV444 8bit/10bit
        - YUYV: YUYV422/420; UYVY420/422
        - BPP:8BPP
    - Image
        - Support virtual width(max 8k word)
        - Support active offset
        - Support display offset
        - Support Y-mirror
        - Swap: alpha/RB/UV swap
        - Support YUV clip
    - Multi-region
        - Only one region at one line
        - All regions are RGB or YUV format
        - Up to 4 regions
    - Scale
        - Scale down
            - Support scale rate 1/8~1
            - Scale mode: nearest/bilinear/average
        - Scale up
            - Support scale rate 1~8
            - Scale mode: nearest/bilinear/bicubic
    - CSC
        - YUV2RGB: bt601-f/bt709-l/bt601-l/bt2020
        - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020
- SMART0/1
    - Resolution
        - Max input resolution:4096x2304
        - Max output resolution:4096x2304
    - Data format
        - RGB:ARGB8888/RGB888/RGB565
        - ABPP:ABPP08/26/44/62
    - Image
        - Support virtual width(max 8k word)
        - Support active offset
        - Support display offset
        - Support Y-mirror
        - Swap: alpha/RB swap
    - Multi-region
        - Only one region at one line
        - Up to 4 regions
    - CSC
        - RGB2YUV: bt601-f/bt709-l/bt601-l/bt2020

- Overlay
  - Support MAX 6 layers overlay: 2 Cluster/2ESMART/2SMART
  - Support RGB/YUV domain overlay
  - Support layers mux
  - Support per-pixel/global alpha
  - Support HDR10
    - Support one layer HDR2SDR
    - Support SDR2HDR
- Write back

Format: ARGB8888/RGB888/RGB565/YUV420
Max resolution: 1920x1080

- Interrupt
  - Vop_intr
    - System0 interrupt
      - Axi0 bus error
      - Axi0 dma finish
      - Write back UV fifo overflow
      - Write back YRGB fifo overflow
      - Write back dma finish
      - MMU0 interrupt
      - System1 interrupt
      - Axi1 bus error
      - Axi1 dma finish
      - MMU1 interrupt
    - Video port0/1/2 interrupt
      - Frame start interrupt
      - Line flag0 interrupt
      - Line flag1 interrupt
      - Post empty interrupt
      - Field start interrupt
      - Display hold interrupt
      - Video front porch interrupt
      - Post almost full interrupt
    - AFBCD interrupt
      - Cluster0 win0 decode error interrupt
      - Cluster0 win0 axi response error interrupt
      - Cluster0 win1 decode error interrupt
      - Cluster0 win1 axi response error interrupt
      - Cluster1 win0 decode error interrupt
      - Cluster1 win0 axi response error interrupt
      - Cluster1 win1 decode error interrupt
      - Cluster1 win1 axi response error interrupt
  - Vop_intr_ddr
    - Axi0 dma finish
    - Axi1 dma finish
    - Write back dma finish
    - Line flag0 interrupt
    - Line flag1 interrupt
  - Vop_intr_lb
    - Video port0 post almost full
    - Video port1 post almost full
    - Video port2 post almost full

13.2 Block Diagram

The following diagram shows the VOP2 architecture.

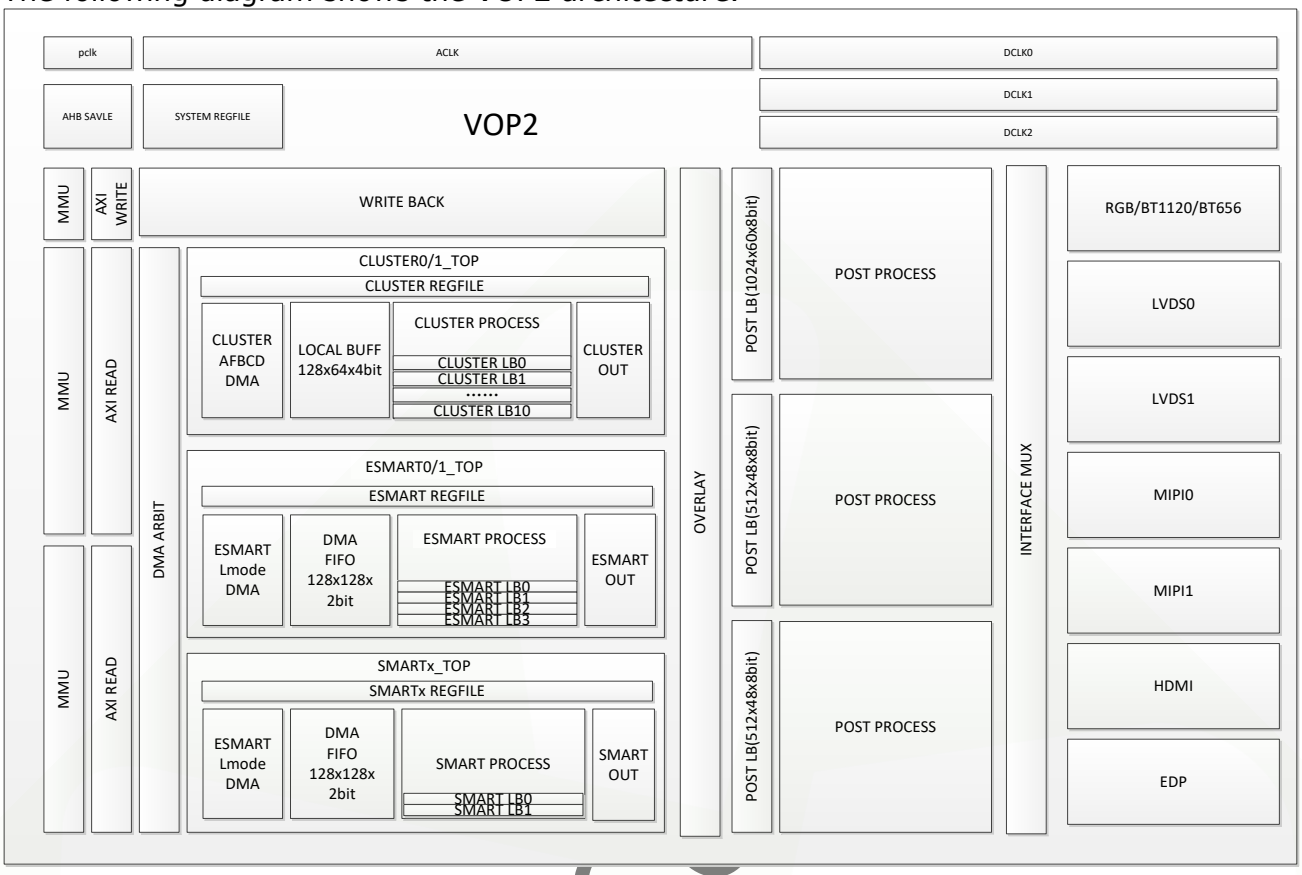


Fig. 13-1 VOP2 Architecture

13.3 Function Description

13.3.1 Pixel format

The pixel stored in memory is shown as follows, usually the data is very compact. The Y and UV component of YUV are stored in different storage location. Even though the number of odd and even rows data of YUYV420 is different, they have the same amount of storage.

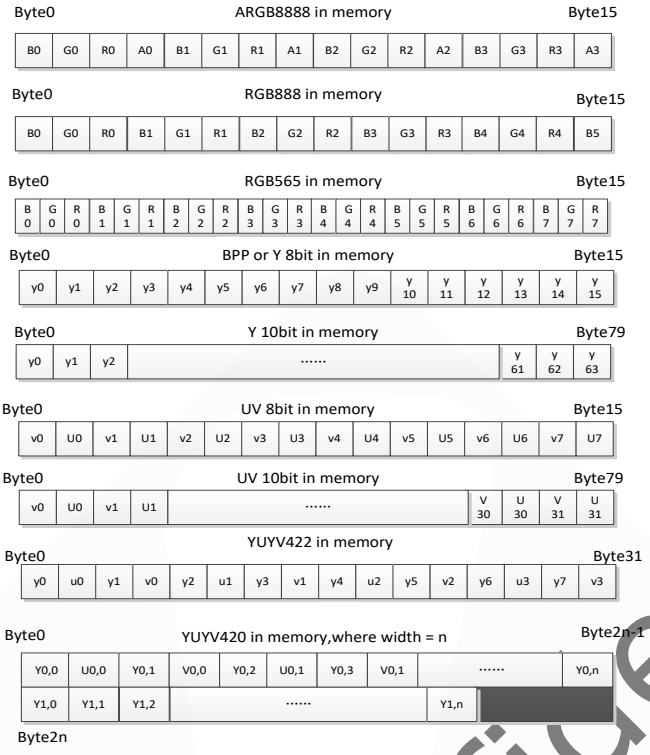


Fig.13-2 VOP2 data format

13.3.2 Virtual display

When in virtual display, the active image is part of the virtual (original) image in frame buffer memory as shown below. The virtual width is indicated by setting VIR_STRIDE for different data format. Note that RGB/BPP has one stride (yrgb_vir_stride), YCbCr has two virtual stride (yrgb_vir_stride and cbcr_vir_stride).For RGB-8bit and YUV-8bit，the stride should be multiples of word (32-bit), with dummy bytes in the end of virtual line if the original width is not 32-bit aligned.

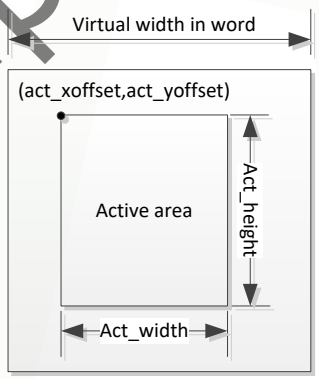


Fig.13-3 virtual width

13.3.3 AFBCD

This compression format is designed to be used for textures and frame buffers. It has been optimized to decrease external bandwidth as well as being random access and decodable at line speed for the texture cache.

Random access is available to individual 16x16 blocks, which in turn index individual 4x4 blocks. This is done using a structure where a header block is stored for each 16x16 block at a predictable memory address in what is referred to as the header buffer. If the horizontal size is given by "width" and A is the start address of the head buff, the address of the header for the 16x16 block containing a given pixel at position x, y is given by A+16*(x/16+((y/16)*(width/16))). A consequence of the 16x16 block structure is that only multiples of 16 are allowed as width and height as shown below.

The data that is used to store the individual 4x4 blocks in a 16x16 block is referred to as the payload data for that block. It is stored continuously in body buff from the offset that is supplied in the header. Each section in the body buffer contains payload data which is used to decode a 16x16 block. The header contains an offset to the payload that resides inside of the body buffer, which is typically allocated after allocated after the header buffer in the memory. The offset to the payload data is relative to the start of the header buffer. In some cases it may sense to store payload data inside the header buffer, such as when encoding blocks that are less than 16x16 in size and not all sub block sizes are used in a header.

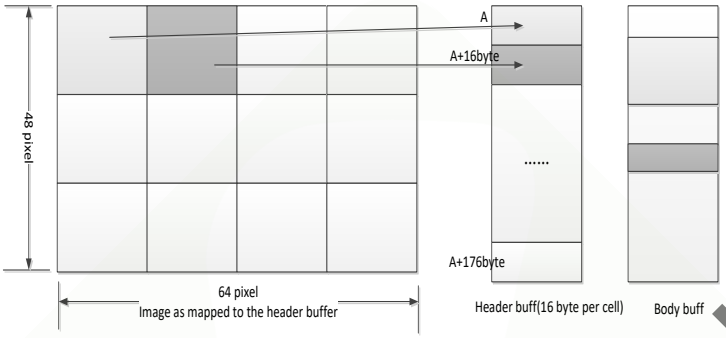


Fig. 13-5 An example of 16x16 pixel blocks with header and body buffer

13.3.3.1 Half block mode

In the full block decoding mode, the decoder fetches full payload of 16x16 blocks and sends then to the decode core, which decodes and outputs 16x16 pixel blocks. In the half block decoding mode, the decoder fetches half of the payload at each time. The decoder output in the half mode is in 16x8 blocks. The half block mode is designed to support custom hardware with limited buffer size, for example a typical display controller with 8-line buffers.

13.3.4 Scale

With all various video resolutions, scaling is usually needed in almost every solution. Average interpolation is used in scaling down and bicubic interpolation is used in scaling up besides nearest neighbor and bilinear interpolation. The summary of scaling factor calculation is shown as follows:

$$scale\_down\_bli\_factor = (src-1)/(dst-1)*2^{12}$$

$$scale\_down\_avg\_factor = (dst-1)/(src-1)*2^{16}$$

$$scale\_up\_bli\_factor = (src-1)/(dst-1)*2^{16}$$

$$scale\_up\_bic\_factor = (src-1)/(dst-1)*2^{16}$$

Where vertical scale_down_bli_factor range is 1~2. If dst_height/src_height >= 2 and bilnear scaling down is enable, line dropping must be enable. If gt2 is enable , src_height = src_height/2. If gt4 is enable, src_height = src_height/4.

13.3.5 Post scale down

Post scale down after overlay is supported to fix panel over_scanning, that draws the border of the image beyond the normal visible area on the screen(see below figure). The scale factor range is 1 to 2.

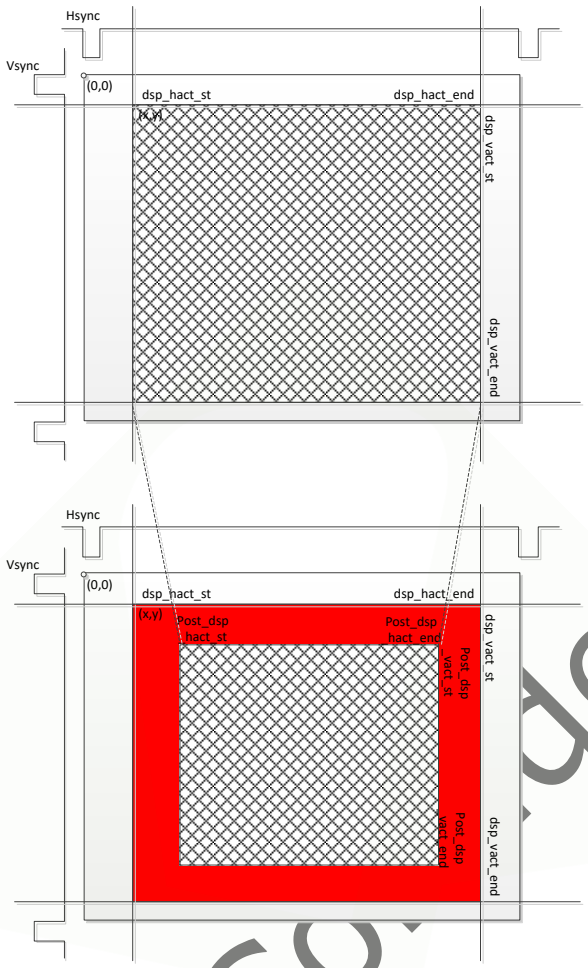


Fig. 13-6 Post scaling

13.3.6 CSC

The red, green, and blue(RGB) color space is widely used for computer graphics and displays. Red, green and blue are three primary additive colors. The YCbCr color space is used by the PAL and NTSC composite color video standards. The black-and-white system used only luma(Y) information. Color information(Cb and Cr) was added in such a way that a black-and-white receiver would still display a normal black-and-white picture. Color receivers decoded the additional color information to display a color picture.

There are four equations used to convert between RGB and YCbCr space.

YUV2RGB:

1.yuv to rgb (BT601L)

R = 1.164(Y-16) + 1.596(V-128)

G = 1.164(Y-16) - 0.391(U-128) - 0.813(V-128)

B = 1.164(Y-16) + 2.018(U-128)

2.yuv to rgb (BT601F)

R = (Y-16) + 1.402(V-128)

G = (Y-16) - 0.344(U-128) - 0.714(V-128)

B = (Y-16) + 1.772(U-128)

3. yuv to rgb (BT709L)

R = 1.164(Y-16) + 1.793(V-128)

G = 1.164(Y-16) - 0.213(U-128) - 0.534(V-128)

B = 1.164(Y-16) + 2.115(U-128)

yuv to rgb(BT2020)

R = 1.1636(Y-64) + 1.6778(V-512)

G = 1.1636(Y-64) - 0.1872(U-512) - 0.6501(V-512)

B = 1.1636(Y-64) + 2.1406(U-512)

RGB2YUV:

1. rgb to yuv(BT601L)
Y = 0.257R + 0.504G + 0.098B + 16
Cb =-0.148R - 0.291G + 0.439B + 128
Cr = 0.439R - 0.368G - 0.071B + 128
2. rgb to yuv(BT601F)
Y = 0.299R + 0.5870G + 0.1140B + 0
Cb = -0.1687R - 0.3313G + 0.5000B + 512
Cr = 0.500R - 0.4187G - 0.0813B + 512
3. rgb to yuv(BT709L)
Y = 0.183R + 0.614G + 0.062B + 16
Cb =-0.101R - 0.338G + 0.439B + 128
Cr = 0.439R - 0.399G - 0.040B + 128
4.rgb to yuv(BT2020)
Y = 0.2250R + 0.5807G + 0.0508B + 64
Cb = -0.1223R - 0.3157G + 0.4380B + 512
Cr = 0.4380R - 0.4028G - 0.0352B + 512

13.3.7 BCSH

Working in YCbCr color space simplifies the implementation of brightness, contrast, saturation, and hue controls, as shown below. Also illustrated are multiplexers to allow the output of black screen, blue screen, and color bars.
The contrast control is implemented by multiplying the YCbCr data by a constant. If Cb and Cr are not adjusted, a color shift will result whenever the contrast is changed. A typical 8-bit contrast adjustment range is 0~1.992x.
The brightness control is implemented by adding or subtracting from the Y data. Brightness is done after the contrast to avoid introducing a vary DC offset due to adjusting the contrast. A typical 8-bit brightness adjusting range is -128 to + 127.
The hue control is implemented by mixing the Cb and Cr data:

$$Cb' = Cb * \cos\theta + Cr * \sin\theta$$

$$Cr' = Cr * \cos\theta - Cb * \sin\theta$$

Where θ is the desired hue angle. A typical 8-bit hue adjustment range is -30° to +30°.
The saturation control is implemented by multiplying both Cb and Cr by a constant. A typical 8-bit saturation adjustment range is 0~1.992x.

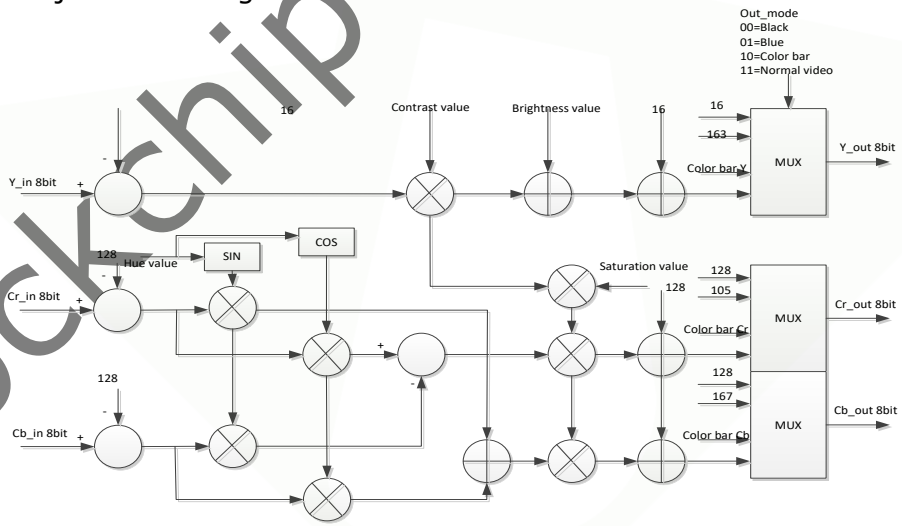


Fig. 13-7 BCSH structure when inputs are 8bit

13.3.8 Gamma

The transfer function of many displays produces an intensity that is proportional to some power of the signal amplitude. As a results, high-intensity ranges are expanded and low-intensity ranges are compressed. This is an advantage in combatting noise, as the eye is approximately sensitive to equally relative intensity changes. By gamma correcting the video signals before transmission, the intensity output of the display is roughly linear. We assume a transform at the display with a gamma of 2.2. To compensate for the nonlinear display, linear

RGB was gamma-corrected prior to transmission by the inverse transform:

$$R' = (R/1024)^{2.2} * 1024, R = 0,1...,1023$$

$$G' = (G/1024)^{2.2} * 1024, G = 0,1...,1023$$

$$B' = (B/1024)^{2.2} * 1024, B = 0,1...,1023$$

13.3.9 3D_LUT

Color space transformation using a 9-level 3D lookup table with trilinear interpolation is used to correlate the source and destination color values in the lattice points of a 3D table, where non-lattice points are interpolated by using the nearest lattice points. The 3D table which consists of 729 points data is stored in memory. Then, it's fetched by AXI master. The rule for 3D table data alignment is shown as below.

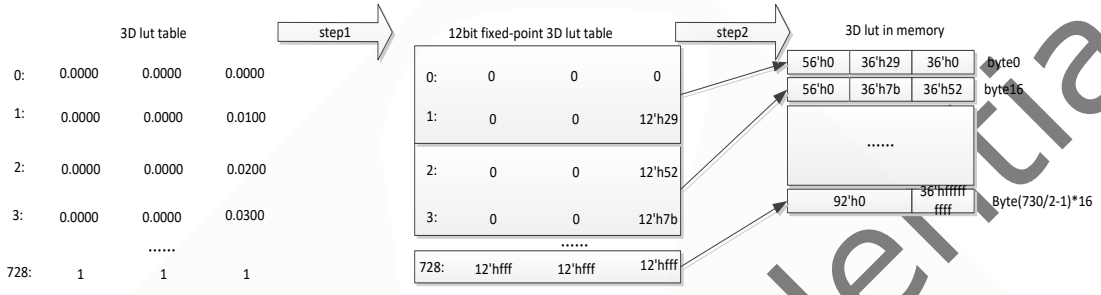


Fig. 13-8 3D LUT table in memory

13.3.10 Write back

The data which is mixed in overlay and send to post-processing module can be wrote back to memory with AXI master. The data format can be ARGB8888, RGB888, RGB565 or YUV420. The max size is 1920x1080. Note that wb_fifo_thold * 16 must be equal or greater than the byte number of one line data. Otherwise, it may causes WB dma fifo overflow and results in some data errors. For example, the size is 1920x1080 and the format is ARGB8888, wb_fifo_thold can be set to 480.

13.3.11 Overlay

Mixing video signals maybe as simple as switching between two video sources. For most other applications, a technique known as alpha blending should be used to overlay computer-generated text and graphics on to a video signal. The figure illustrates mixing 8 layers in VOP.

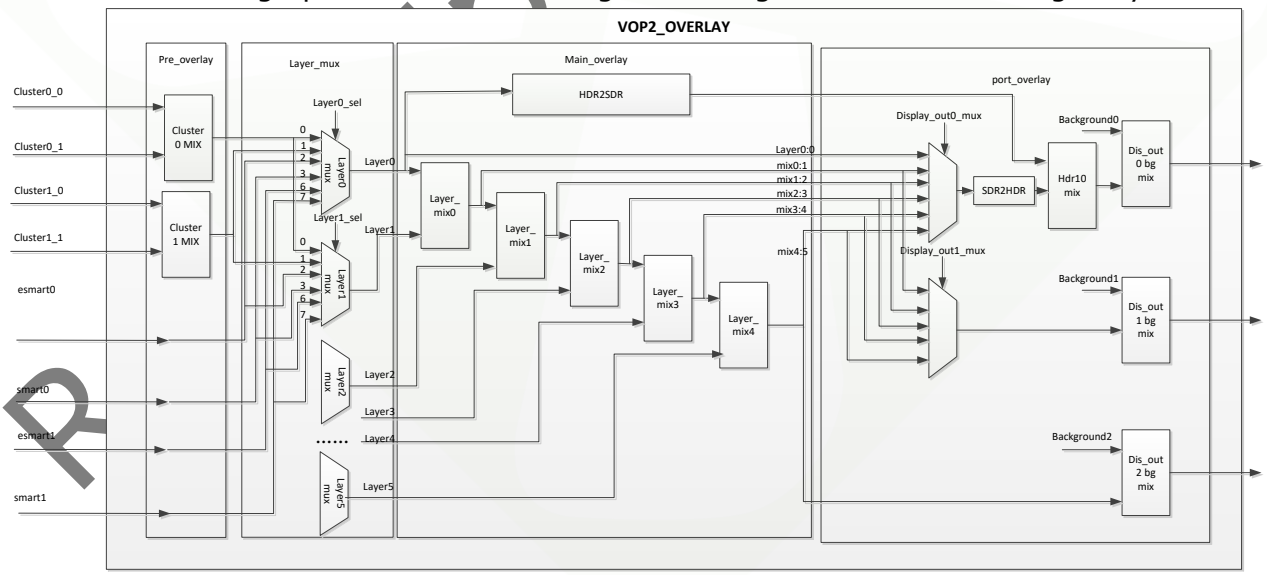


Fig. 13-9 VOP2 overlay structure

It consists of pre_overlay, layer_mux, main_overlay and post_overlay. The pre_overlay is implemented to mix the two windows from the same cluster. The layer_mux is implemented to distribute windows to layers which have the same number of windows. The main_overlay is used to mix layers one by one. The post_overly is added to distribute different layers to different display outputs in different applications. Finally, before the mixed data gets through display outputs, it is mixed with a background color. In addition, only display output0 supports

HDR10.

13.3.11.1 Alpha mixing

Every two layer that one is called source layer and another is called destination layer are mixed by alpha mixing. They are proportionally multiplied and added together. Mathematically, with normalized to have value of 0~1, data mixing is implemented as:

$$Ad * Cd = As' * Cs' + (1 - As') * Cd' * Ad'$$

$$Ad = As' + Ad' - As' * Ad'$$

Where A is alpha and C is color data. Implementation block diagram is given as below.

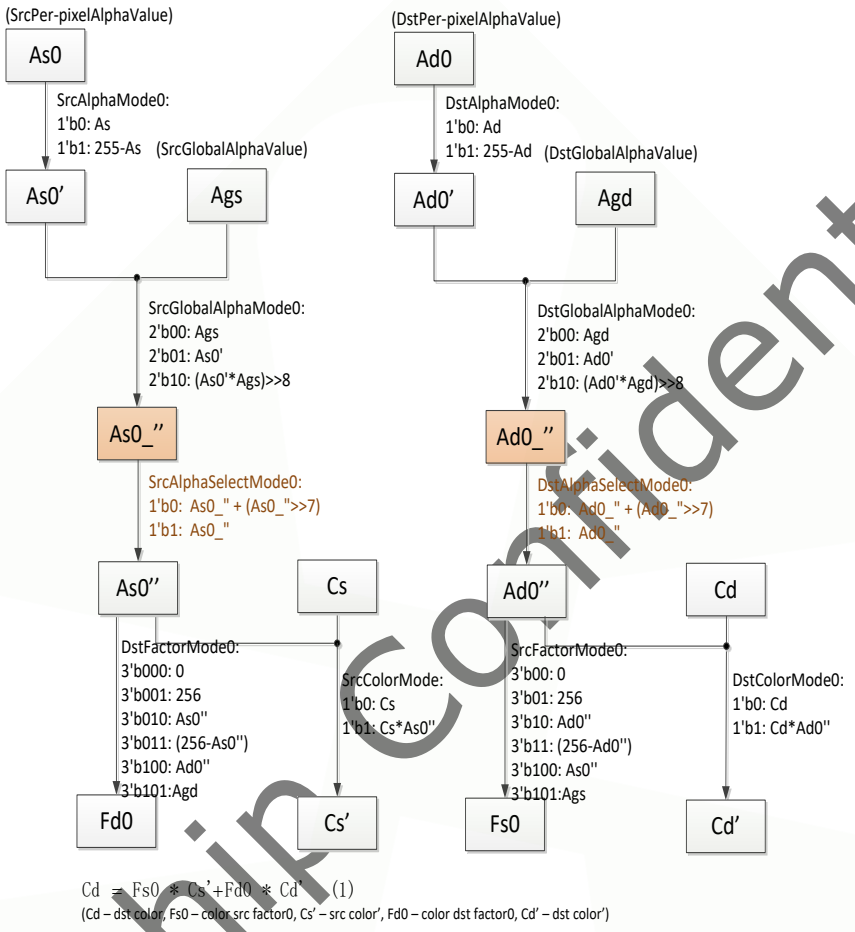


Fig. 13-10 Data calculation flow

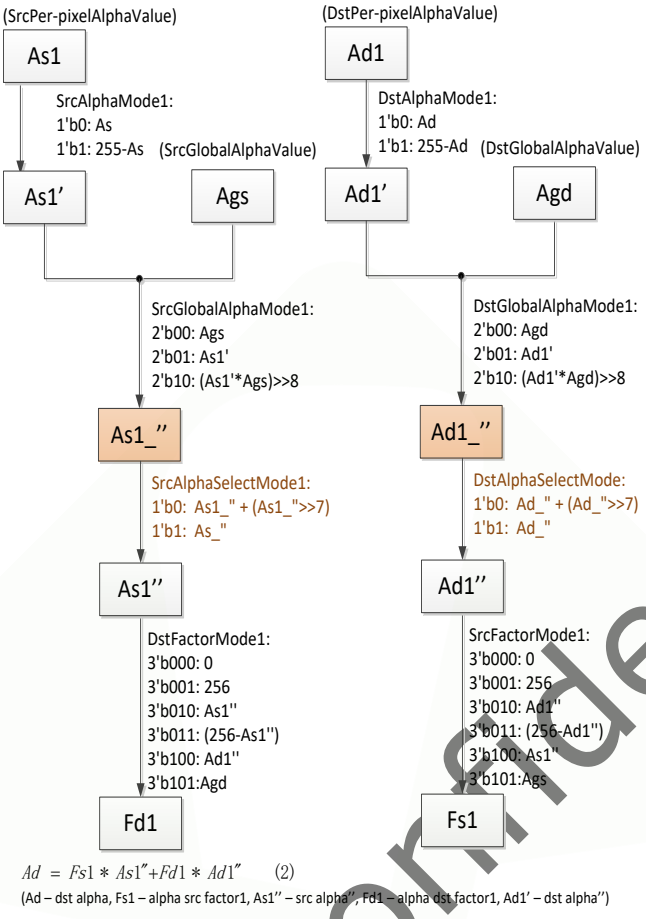


Fig. 13-11 Alpha calculation flow

13.3.11.2 Background mixing

It's known that the alpha of the background is 1. A simplified formula is used as shown below:

$$Cd = As'*Cs'+(1-As')*Cd'$$

Where Cd' is background data, Cs' is mixing video and graphic data. It's implemented as fellows.

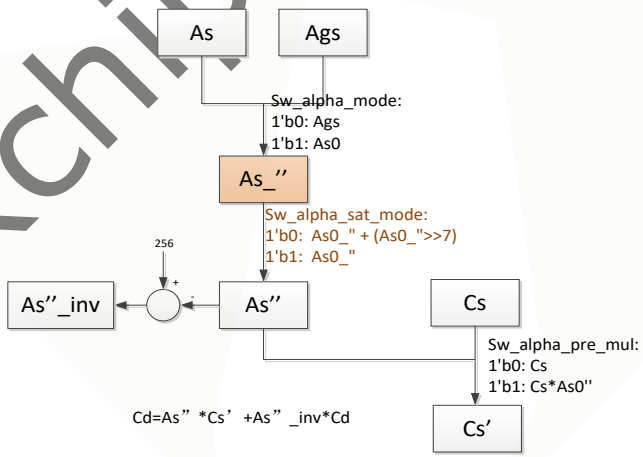


Fig. 13-12 Background alpha blending

13.3.12 HDR10

A high-dynamic-range(HDR) system is able to transmit the camera-captured dynamic range of luminance levels from the production process all the way to the consumer end without any degradation in this dynamic range. But due to the technological limitations of conventional displays, current standard-dynamic-range(SDR) production restricts luminance levels to a maximum of 100 cd/m^2 and supports only the ITU-R BT.709 standard color space. It's necessary to implement HDR2SDR to improve display quality in the system that HDR image is send to a low-luminance display. Similarly SDR2HDR is implemented in the system that a high-luminance panel displays a SDR image. HDR2SDR and SDR2HDR can be achieved using

appropriate transfer functions(OETF/EOTF). In order to decrease registers, now the registers used to configure transfer functions are stored in memory as shown below.

byte0	eetf_oetf_y0	eetf_oetf_y1	eetf_oetf_y2	eetf_oetf_y3
Byte16*1	eetf_oetf_y4	eetf_oetf_y5	eetf_oetf_y6	eetf_oetf_y7
.....	.....			
Byte16*8	Eetf_oetf_y32	96'h0		
Byte16*9	Sat_y0	Sat_y1	.....	Sat_y7
Byte16*10	Sat_y8	112'h0		
Byte16*11	eotf_oetf_y0	eotf_oetf_y1	eotf_oetf_y2	eotf_oetf_y3
.....	.....			
Byte16*27	eotf_oetf_y64	96'h0		
Byte16*28	oetf_dx_dxpow1	oetf_dx_dxpow2	oetf_dx_dxpow3	oetf_dx_dxpow4
.....	.....			
Byte16*43	oetf_dx_dxpow61	oetf_dx_dxpow62	oetf_dx_dxpow63	oetf_dx_dxpow64
Byte16*44	oetf_xn1	oetf_xn2	oetf_xn3	oetf_xn4
.....	.....			
Byte16*59	oetf_xn61	oetf_xn62	oetf_xn63	32'h0

Fig. 13-13 Configures for HDR10 transfer function in memory

13.3.13 Mirror display

Mirror display is necessary for the panel with mirror timing interface. There are two types of mirror mode: horizontal mirror(X-mirror) and vertical mirror(Y-mirror). If Y-mirror is enable, set the MST of window to the beginning of the last line.

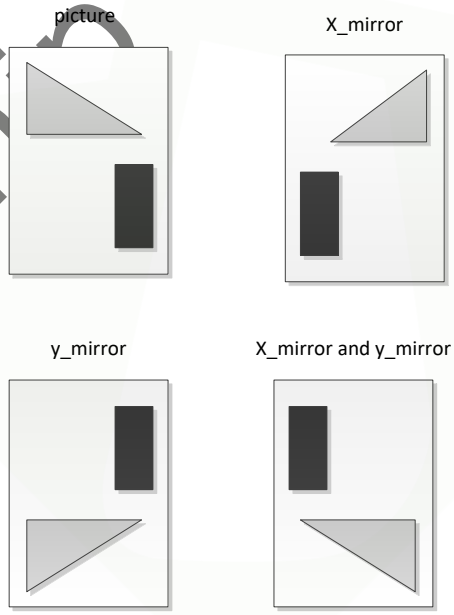


Fig.13-4 Mirror

13.3.14 Display outputs

VOP2 can output video in 4K with up to 30-bit color mode. The video data output mapping is defined by dsp_out_mode as shown below.

Table 13-1 Output data mapping

Output format			Output data		
Color Space	Color depth	dsp_out_mode	data_o[29:20]	data_o[19:10]	data_o[9:0]
RGB4:4:4	24-bit	0	{R[7:0],2'b0}	{G[7:0],2'b0}	{B[7:0],2'b0}
	30-bit	15	R[9:0]	G[9:0]	B[9:0]
YUV4:4:4	24-bit	0	{V[7:0],2'b0}	{Y[7:0],2'b0}	{U[7:0],2'b0}
	30-bit	15	V[9:0]	Y[9:0]	U[9:0]
YUV4:2:0	30-bit	14	V(L)(n)[9:0]	Y(L)(n)[9:0]	Y(L)(n+1)[9:0]
			V(L+1)(n)[9:0]	Y(L+1)(n)[9:0]	Y(L+1)(n+1)[9:0]

13.4 Register Description

13.4.1 System Register description

13.4.1.1 Registers Summary

The base address of system registers is 0x0000.

Name	Offset	Size	Reset Value	Description
VOP2_SYS_REG_CFG_DONE	0x0000	W	0x00008000	Register configure done flag.
VOP2_SYS_VERSION_INFO	0x0004	W	0x40158588	RTL version.
VOP2_SYS_AUTO_GATING_CTRL_IMD	0x0008	W	0x80000000	To control auto-gating.
VOP2_SYS_RESVERD	0x000C	W	0x00000000	RESERVED
VOP2_SYS_AXI_CTRL0_IMD	0x0010	W	0x00000A00	To control AXI.
VOP2_SYS_AXI_HURRY_CTRL0_IMD	0x0014	W	0x00000000	To control AXI0 hurry mode.
VOP2_SYS_AXI_HURRY_CTRL1_IMD	0x0018	W	0x00000000	To control AXI1 hurry mode.
VOP2_SYS_AXI_OUTSTANDING_CTRL0_IMD	0x001C	W	0x00000000	To control AXI outstanding number.
VOP2_SYS_AXI_OUTSTANDING_CTRL1_IMD	0x0020	W	0x00000000	To control AXI outstanding number.
VOP2_SYS_AXI_LUT_CTRL_IMD	0x0024	W	0x00000000	To control the DMA of fetching LUT.
VOP2_SYS_DSP_INFACE_EN	0x0028	W	0x00000000	To enable display interface.
VOP2_SYS_DSP_INFACE_CTRL	0x002C	W	0x00000000	To configure bt656 and bt1120.
VOP2_SYS_DSP_INFACE_POL	0x0030	W	0x00000000	To control the polarity of interface
VOP2_SYS_WB_CTRL0	0x0040	W	0x70680000	To control WB.
VOP2_SYS_WB_XSPD_FACTOR	0x0044	W	0x00000000	To configure the scale factor of WB.

Name	Offset	Size	Reset Value	Description
VOP2_SYS_WB_YRGB_MST	0x0048	W	0x00000000	WB YRGB memory starting address.
VOP2_SYS_WB_CBR_MST	0x004C	W	0x00000000	WB CbCr memory starting address.
VOP2_SYS_OTP_WIN_EN_IMD	0x0050	W	0x00000000	To enable optional function.
VOP2_SYS_LUT_PORT_SEL	0x0058	W	0x00000000	To select the video port for LUT.
VOP2_SYS_STATUS0	0x0060	W	0x00000000	The system status of video port0.
VOP2_SYS_STATUS1	0x0064	W	0x00000000	The system status of video port1.
VOP2_SYS_STATUS2	0x0068	W	0x00000000	The system status of video port2.
VOP2_SYS_RESERVED	0x006C	W	0x00000000	RESERVED
VOP2_SYS_LINE_FLAG0	0x0070	W	0x00000000	To set the line flag of video port0.
VOP2_SYS_LINE_FLAG1	0x0074	W	0x00000000	To set the line flag of video port1.
VOP2_SYS_LINE_FLAG2	0x0078	W	0x00000000	To set the line flag of video port2.
VOP2_SYS0_INTR_EN	0x0080	W	0x00000000	To enable system0 interrupt.
VOP2_SYS0_INTR_CLR	0x0084	W	0x00000000	To clear system0 interrupt.
VOP2_SYS0_INTR_STATUS	0x0088	W	0x00000000	System0 interrupt status.
VOP2_SYS0_INTR_RAW_STATUS	0x008C	W	0x00000000	System0 interrupt raw status.
VOP2_SYS1_INTR_EN	0x0090	W	0x00000000	To enable system1 interrupt.
VOP2_SYS1_INTR_CLR_SYS	0x0094	W	0x00000000	To clear system1 interrupt.
VOP2_SYS1_INTR_STATUS	0x0098	W	0x00000000	System1 interrupt status.
VOP2_SYS1_INTR_RAW_STATUS	0x009C	W	0x00000000	System1 interrupt raw status.
VOP2_PORT0_INTR_EN	0x00A0	W	0x00000000	To enable video port0 interrupt.
VOP2_PORT0_INTR_CLR	0x00A4	W	0x00000000	To clear video port0 interrupt.
VOP2_PORT0_INTR_STATUS	0x00A8	W	0x00000000	video port0 interrupt status.
VOP2_PORT0_INTR_RAW_STATUS	0x00AC	W	0x00000000	video port0 interrupt raw status.
VOP2_PORT1_INTR_EN	0x00B0	W	0x00000000	To enable video port1 interrupt.
VOP2_PORT1_INTR_CLR	0x00B4	W	0x00000000	To clear video port1 interrupt.
VOP2_PORT1_INTR_STATUS	0x00B8	W	0x00000000	video port1 interrupt status.
VOP2_PORT1_INTR_RAW_STATUS	0x00BC	W	0x00000000	video port1 interrupt raw status.
VOP2_PORT2_INTR_EN	0x00C0	W	0x00000000	To enable video port2 interrupt.
VOP2_PORT2_INTR_CLR	0x00C4	W	0x00000000	To clear video port2 interrupt.
VOP2_PORT2_INTR_STATUS	0x00C8	W	0x00000000	video port2 interrupt status.
VOP2_PORT2_INTR_RAW_STATUS	0x00CC	W	0x00000000	video port2 interrupt raw status.
VOP2_AFBCD_INTR_EN	0x00E0	W	0x00000000	To enable afbcd interrupts.
VOP2_AFBCD_INTR_CLR	0x00E4	W	0x00000000	To clear afbcd interrupts.
VOP2_AFBCD_INTR_STATUS	0x00E8	W	0x00000000	Afbcd interrupt status.
VOP2_AFBCD_INTR_RAW_STATUS	0x00EC	W	0x00000000	Afbcd interrupt raw status.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Double WORD (64 bits) access

13.4.1.2 Detail Registers Description

VOP2_SYS_REG_CFG_DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit. When every bit LOW, don't care the writing corresponding bit.
15	RW	0x1	sw_global_regdone_en Global regdone enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	reg_load_wb_en In the first setting of the register, the new value was saved into the mirror register.When all the wb register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
13	RW	0x0	reg_load_smart1_en In the first setting of the register, the new value was saved into the mirror register.When all the smart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
12	RW	0x0	reg_load_smart0_en In the first setting of the register, the new value was saved into the mirror register. When all the smart0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
11	RW	0x0	reg_load_esmart1_en In the first setting of the register, the new value was saved into the mirror register.When all the esmart1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
10	RW	0x0	reg_load_esmart0_en In the first setting of the register, the new value was saved into the mirror register.When all the esmart0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
9:8	RO	0x0	reserved
7	RW	0x0	reg_load_cluster1_en In the first setting of the register, the new value was saved into the mirror register.When all the cluster1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_cluster0_en In the first setting of the register, the new value was saved into the mirror register.When all the cluster0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

Bit	Attr	Reset Value	Description
5	RW	0x0	reg_load_sys2_en In the first setting of the register, the new value was saved into the mirror register.When all the system2 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_sys1_en In the first setting of the register, the new value was saved into the mirror register.When all the system1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3	RW	0x0	reg_load_sys0_en In the first setting of the register, the new value was saved into the mirror register.When all the system0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
2	RW	0x0	reg_load_global2_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
1	RW	0x0	reg_load_global1_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	RW	0x0	reg_load_global0_en In the first setting of the register, the new value was saved into the mirror register.When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

VOP2_SYS_VERSION_INFO

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major Used for IP structure.
23:16	RW	0x00	minor Big feature change under same structure.
15:0	RW	0x0000	svnbuild RTL current svn number.

VOP2_SYS_AUTO_GATING_CTRL_IMD

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x1	auto_gating_en 1'b0: Disable auto gating 1'b1: Enable auto gating default auto gating enable
30:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	prescan_aclk_gating_en 1'b0: Disable 1'b1: Enable
12	RW	0x0	pwm_pwmclk_gating_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	wb_aclk_gating_en 1'b0: Disable 1'b1: Enable
10	RW	0x0	cabc_dclk_gating_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	gamma_dclk_gating_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	overlay_aclk_gating_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	smart1_aclk_gating_en 1'b0: Disable 1'b1: Enable
6	RW	0x0	smart0_aclk_gating_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	esmart1_aclk_gating_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	esmart0_aclk_gating_en 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	cluster1_aclk_gating_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	cluster0_aclk_gating_en 1'b0: Disable 1'b1: Enable

VOP2_SYS_RESVERD

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

VOP2_SYS_AXI_CTRL0_IMD

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	lut_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
11	RW	0x1	smart1_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
10	RW	0x0	smart0_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
9	RW	0x1	esmart1_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
8	RW	0x0	esmart0_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5	RW	0x0	cluster1_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cluster0_use_axi1 Select axi1. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	axi1_dma_stop Stop axi1 dma. 1'b0: Disable 1'b1: Enable
0	RW	0x0	axi0_dma_stop Stop axi0 dma. 1'b0: Disable 1'b1: Enable

VOP2_SYS_AXI_HURRY_CTRL0_IMD

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	axi0_qos_value Noc qos value
12	RW	0x0	axi0_qos_en Noc qos enable.
11	RW	0x0	axi0_hurry_threshold Noc hurry threshold value.
10:9	RW	0x0	axi0_hurry_value Noc hurry value.
8	RW	0x0	axi0_hurry_en Noc hurry enable.
7:5	RO	0x0	reserved
4:3	RW	0x0	axi0_hurry_w_mode 2'b00: noc_hurry_w disable 2'b01: left 1/4 fifo empty 2'b10: left 1/2 fifo empty 2'b11: left 3/4 fifo empty
2:1	RW	0x0	axi0_hurry_w_value Noc hurry value. 2'b00: low priority 2'b11: high priority

Bit	Attr	Reset Value	Description
0	RW	0x0	axi0_hurry_w_en Noc hurry enable.

VOP2_SYS_AXI_HURRY_CTRL1_IMD

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:13	RW	0x0	axi1_qos_value Noc qos value.
12	RW	0x0	axi1_qos_en Noc qos enable.
11	RW	0x0	axi1_hurry_threshold Noc hurry threshold value.
10:9	RW	0x0	axi1_hurry_value Noc hurry value.
8	RW	0x0	axi1_hurry_en Noc hurry enable.
7:5	RO	0x0	reserved
4:3	RW	0x0	axi1_hurry_w_mode 2'b00: noc_hurry_w disable. 2'b01: left 1/4 fifo empty 2'b10: left 1/2 fifo empty 2'b11: left 3/4 fifo empty
2:1	RW	0x0	axi1_hurry_w_value Noc hurry value. 2'b00: low priority 2'b11: high priority
0	RW	0x0	axi1_hurry_w_en Noc hurry enable.

VOP2_SYS_AXI_OUTSTANDING_CTRL0_IMD

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	cluster1_outstanding_num Cluster1 max outstanding number.
19:16	RW	0x0	cluster0_outstanding_num Cluster0 max outstanding number.
15	RO	0x0	reserved
14:11	RW	0x0	axi1_outstanding_num Axi0 bus max outstanding number.
10:9	RO	0x0	reserved
8	RW	0x0	axi1_outstanding_en Axi1 bus max outstanding enable. 1'b0: Disable 1'b1: Enable
7:3	RW	0x00	axi0_outstanding_num Axi0 bus max outstanding number.
2:1	RO	0x0	reserved
0	RW	0x0	axi0_outstanding_en Axi0 bus max outstanding enable. 1'b0: Disable 1'b1: Enable

VOP2_SYS_AXI_OUTSTANDING_CTRL1_IMD

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	smart1_outstanding_num Smart1 max outstanding number.
11:8	RW	0x0	smart0_outstanding_num Smart0 max outstanding number.
7:4	RW	0x0	esmart1_outstanding_num Esmart1 max outstanding number.
3:0	RW	0x0	esmart0_outstanding_num Esmart0 max outstanding number.

VOP2_SYS_AXI_LUT_CTRL_IMD

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_bypass_en If axi rid > 0xa , bypass mmu. 1'b0: Disable 1'b1: Enable
30:24	RO	0x00	reserved
23:22	RW	0x0	mmu1_regdone_sel Select mmu1 regdone. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
21:20	RO	0x0	reserved
19:18	RW	0x0	mmu0_regdone_sel Select mmu0 regdone. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
17:15	RO	0x0	reserved
14	RW	0x0	vp2_interlace_frm_reg_done video port1 reg done framed valid. 1'b0: reg done every field for interlace. 1'b1: reg done every frame for interlace.
13	RW	0x0	vp1_interlace_frm_reg_done video port1 reg done framed valid. 1'b0: reg done every field for interlace. 1'b1: reg done every frame for interlace.
12	RW	0x0	vp0_interlace_frm_reg_done video port0 reg done framed valid. 1'b0: reg done every field for interlace. 1'b1: reg done every frame for interlace.
11:8	RO	0x0	reserved
7:4	RW	0x0	lut_dma_rid LUT axi read id.
3:2	RW	0x0	lut_dma_rlen LUT axi read brust. 2'b00: Burst16 2'b01: Burst8 2'b1x: Burst4

Bit	Attr	Reset Value	Description
1	RW	0x0	lut_dma_stop Stop LUT dma. 1'b0: Disable 1'b1: Enable
0	RW	0x0	lut_dma_en Enable LUT dma. 1'b0: Disable 1'b1: Enable

VOP2_SYS_DSP_INFACE_EN

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:23	RO	0x00	reserved
22:21	RW	0x0	mipi1_inface_mux Select the display output of MIPI1 interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
20	RW	0x0	mipi1_out_en 1'b0: gating output clk, data and control signal 1'b1: mipi1 interface enable
19:18	RW	0x0	lvds_inface_mux Select the display output of LVDS interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
17:16	RW	0x0	mipi_inface_mux Select the display output of MIPI interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
15:14	RW	0x0	edp_inface_mux Select the display output of EDP interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
13:12	RO	0x0	reserved
11:10	RW	0x0	hdmi_inface_mux Select the display output of HDMI interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
9:8	RW	0x0	rgb_inface_mux Select the display output of RGB interface. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
7	RW	0x0	bt656_out_en 1'b0: gating output clk, data and control signal 1'b1: bt656 interface enable
6	RW	0x0	bt1120_out_en 1'b0: gating output clk, data and control signal 1'b1: bt1120 interface enable

Bit	Attr	Reset Value	Description
5	RW	0x0	lvds_out_en 1'b0: gating output clk, data and control signal 1'b1: lvds interface enable
4	RW	0x0	mipi_out_en 1'b0: gating output clk, data and control signal 1'b1: mipi interface enable
3	RW	0x0	edp_out_en 1'b0: gating output clk, data and control signal 1'b1: edp interface enable
2	RO	0x0	reserved
1	RW	0x0	hdmi_out_en 1'b0: gating output clk, data and control signal 1'b1: hdmi interface enable
0	RW	0x0	rgb_out_en 1'b0: gating output clk, data and control signal 1'b1: rgb interface enable

VOP2_SYS_DSP_INFACE_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	dsp_inface_regdone_sel 2'b00: video port0 2'b01: video port1 2'b1x: video port2
28	RW	0x0	dsp_inface_regdone_imd_en 1'b0: Disable 1'b1: Enable
27:11	RO	0x00000	reserved
10	RW	0x0	bt1120_dclk_pol 1'b0: Normal 1'b1: Invert
9	RW	0x0	bt1120_yc_swap Swap gray and color component. 1'b0: Disable 1'b1: Enable
8	RW	0x0	bt1120_uv_swap Swap U and V component. 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	RW	0x0	bt656_dclk_pol 1'b0: Negative 1'b1: Positive
5	RW	0x0	bt656_yc_swap Swap GRAY and COLOR component of BT656.
4	RW	0x0	bt656_uv_swap Swap U and V component of BT656.
3:0	RO	0x0	reserved

VOP2_SYS_DSP_INFACE_POL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	regdone_sel Select interface control register regdone. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
29	RO	0x0	reserved
28	RW	0x0	regdone_imd_en Enable interface control register regdone immediately.
27:20	RO	0x00	reserved
19	RW	0x0	mipi_dclk_pol 1'b0: Normal 1'b1: Invert
18	RW	0x0	mipi_den_pol 1'b0: Negative 1'b1: Positive
17	RW	0x0	mipi_vsync_pol 1'b0: Negative 1'b1: Positive
16	RW	0x0	mipi_hsync_pol 1'b0: Negative 1'b1: Positive
15	RW	0x0	edp_dclk_pol 1'b0: normal 1'b1: invert
14	RW	0x0	edp_den_pol 1'b0: Negative 1'b1: Positive
13	RW	0x0	edp_vsync_pol 1'b0: Negative 1'b1: Positive
12	RW	0x0	edp_hsync_pol 1'b0: Negative 1'b1: Positive
11:8	RO	0x0	reserved
7	RW	0x0	hdmi_dclk_pol 1'b0: Normal 1'b1: Invert
6	RW	0x0	hdmi_den_pol 1'b0: Negative 1'b1: Positive
5	RW	0x0	hdmi_vsync_pol 1'b0: negative 1'b1: positive
4	RW	0x0	hdmi_hsync_pol 1'b0: negative 1'b1: positive
3	RW	0x0	rgb_lvds_clk_pol 1'b0: Normal 1'b1: Invert
2	RW	0x0	rgb_lvds_den_pol 1'b0: Negative 1'b1: Positive
1	RW	0x0	rgb_lvds_vsync_pol 1'b0: Negative 1'b1: Positive

Bit	Attr	Reset Value	Description
0	RW	0x0	rgb_lvds_hsync_pol 1'b0: Negative 1'b1: Positive

VOP2_SYS_WB_CTRL0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0xe	wb_uv_id Use default 0xe.
26:23	RO	0x0	reserved
22:19	RW	0xd	wb_yrgb_id Use default 0xd.
18:12	RO	0x00	reserved
11	RW	0x0	wb_handshake_mode 1'b0: full handshake 1'b1: half handshake
10	RO	0x0	reserved
9	RW	0x0	wb_ythrow_mode 1'b0: throw odd line 1'b1: throw even line
8	RW	0x0	wb_ythrow_en 1'b0: disable 1'b1: enable
7	RW	0x0	wb_xpsd_bil_en 1'b0: enable scale 1'b1: disable scale
6	RW	0x0	wb_rgb2yuv_mode 1'b0: BT601 1'b1: BT709
5	RW	0x0	wb_rgb2yuv_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	wb_dither_en When wb_fmt is RGB565. 1'b0: no dither, RGB888 clip to RGB565 1'b1: with dither, RGB888 dither to RGB565
3:1	RW	0x0	wb_fmt 3'b000: ARGB888 3'b001: RGB888 3'b010: RGB565 3'b100: YcbCr420 other: reserved
0	RW	0x0	wb_en 1'b0: Disable 1'b1: Enable

VOP2_SYS_WB_XSPD_FACTOR

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	wb_xpsd_bil_factor Factor=((src_width[11:0])/(dst_width[11:0]))*2^12.
15:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	fifo_thold When wb_fifo_wcnt < fifo_thold, hold the pre_scan timing. fifo_thold = wb_width * fmt_byte / 16. 3'b000: ARGB888,fmt_byte = 4 3'b001: RGB888,fmt_byte = 3 3'b010: RGB565,fmt_byte = 2 3'b100: YcbCr420,fmt_byte = 1

VOP2_SYS_WB_YRGB_MST

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_yrgb_mst YRGB mst address.

VOP2_SYS_WB_CBR_MST

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_cbr_mst CBR mst address.

VOP2_SYS_OTP_WIN_EN_IMD

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	otp_en 1'b0: Disable 1'b1: Enable

VOP2_SYS_LUT_PORT_SEL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	wb_port_sel Select WB display output. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
7:5	RW	0x0	bpp_win_sel Select 8BPP lut esmart num. 2'b00: Esmart0 2'b01: Esmart1 2'b10: Smart0 2'b11: Smart1
4	RW	0x0	bpp_lut_en Enable 8BPP LUT. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	gamma_port_sel Select Gamma lut display output. 2'b00: video port0 2'b01: video port1 2'b1x: video port2

VOP2_SYS_STATUS0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt0 Read the video port0 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu0_idle MMU0 idle status.
0	RW	0x0	dma_stop_valid0 AXI0 dma stop status.

VOP2_SYS_STATUS1

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt1 Read the video port1 vertical counter.
15:2	RO	0x0000	reserved
1	RW	0x0	mmu1_idle MMU1 idle status.
0	RW	0x0	dma_stop_valid1 AXI1 dma stop status.

VOP2_SYS_STATUS2

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vcnt2 Read the video port2 vertical counter.
15:0	RO	0x0000	reserved

VOP2_SYS_RESERVED

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	Field0000

VOP2_SYS_LINE_FLAG0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

VOP2_SYS_LINE_FLAG1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

VOP2_SYS_LINE_FLAG2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	dsp_almost_full_thold If the number of post full lb >= dsp_almost_full_thold + 1, intr_raw_post_full is asserted.
28:16	RW	0x0000	dsp_line_flag_num_1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

VOP2_SYS0_INTR_EN

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu0 1'b0: Disable 1'b1: Enable
6	RO	0x0	reserved
5	RW	0x0	int_en_wb0_finish 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_wb0_yrgb_fifo_full 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_wb0_uv_fifo_full 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_dma0_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus0_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

VOP2_SYS0_INTR_CLR

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu0 Interrupt clear(Auto clear).
6	RO	0x0	reserved
5	RW	0x0	intr_clr_wb_dma_finish WB_DMA finish interrupt clear(Auto clear).
4	RW	0x0	intr_clr_wb_yrgb_fifo_full Interrupt clear(Auto clear).
3	RW	0x0	intr_clr_wb_uv_fifo_full Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear(Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear(Auto clear).
0	RO	0x0	reserved

VOP2_SYS0_INTR_STATUS

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu0 Interrupt status of MMU0.
6	RO	0x0	reserved
5	RW	0x0	intr_status_wb_dma_finish Interrupt status.
4	RW	0x0	intr_status_wb_yrgb_fifo_full Interrupt status.
3	RW	0x0	intr_status_wb_uv_fifo_full Interrupt status.
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt clear status.
0	RO	0x0	reserved

VOP2_SYS0_INTR_RAW_STATUS

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_mmu0 Interrupt of MMU0 raw status.
6	RO	0x0	reserved
5	RW	0x0	intr_raw_status_wb_dma_finish Interrupt raw status.
4	RW	0x0	intr_raw_status_wb_yrgb_fifo_full Interrupt raw status.
3	RW	0x0	intr_raw_status_wb_uv_fifo_full Interrupt raw status.
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw status.

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_SYS1_INTR_EN

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_en_mmu1 1'b0: Disable 1'b1: Enable
6:3	RO	0x0	reserved
2	RW	0x0	intr_en_dma1_finish 1'b0: Disable 1'b1: Enable
1	RW	0x0	intr_en_bus1_error 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

VOP2_SYS1_INTR_CLR_SYS

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	intr_clr_mmu1 Interrupt clear(Auto clear).
6:3	RO	0x0	reserved
2	RW	0x0	intr_clr_dma_finish DMA finish interrupt clear(Auto clear).
1	RW	0x0	intr_clr_bus_error Bus error Interrupt clear(Auto clear).
0	RO	0x0	reserved

VOP2_SYS1_INTR_STATUS

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_status_mmu1 Interrupt status.
6:3	RO	0x0	reserved
2	RW	0x0	intr_status_dma_finish DMA finish interrupt status.
1	RW	0x0	intr_status_bus_error Bus error Interrupt status.
0	RO	0x0	reserved

VOP2_SYS1_INTR_RAW_STATUS

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	intr_raw_status_mmu1 Interrupt raw_status.

Bit	Attr	Reset Value	Description
6:3	RO	0x0	reserved
2	RW	0x0	intr_raw_status_dma_finish DMA finish interrupt raw_status.
1	RW	0x0	intr_raw_status_bus_error Bus error Interrupt raw_status.
0	RO	0x0	reserved

VOP2_PORT0_INTR_EN

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

VOP2_PORT0_INTR_CLR

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).

Bit	Attr	Reset Value	Description
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RW	0x0	intr_clr_fs_new Frame new start interrupt clear (Auto clear).
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

VOP2_PORT0_INTR_STATUS

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

VOP2_PORT0_INTR_RAW_STATUS

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.

Bit	Attr	Reset Value	Description
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

VOP2_PORT1_INTR_EN

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

VOP2_PORT1_INTR_CLR

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).

Bit	Attr	Reset Value	Description
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

VOP2_PORT1_INTR_STATUS

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

VOP2_PORT1_INTR_RAW_STATUS

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

VOP2_PORT2_INTR_EN

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask
15:10	RO	0x00	reserved
9	RW	0x0	intr_en_post_full 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	intr_en_vfp 1'b0: Disable 1'b1: Enable
6	RW	0x0	intr_en_dsp_hold_valid 1'b0: Disable 1'b1: Enable
5	RW	0x0	intr_en_fs_field 1'b0: Disable 1'b1: Enable
4	RW	0x0	intr_en_post_buf_empty 1'b0: Disable 1'b1: Enable
3	RW	0x0	intr_en_line_flag1 1'b0: Disable 1'b1: Enable
2	RW	0x0	intr_en_line_flag0 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	intr_en_fs 1'b0: Disable 1'b1: Enable

VOP2_PORT2_INTR_CLR

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:10	RO	0x00	reserved
9	RW	0x0	intr_clr_post_full Post buffer almost full interrupt clear(Auto clear).
8	RO	0x0	reserved
7	RW	0x0	intr_clr_vfp Display vfp interrupt clear(Auto clear).
6	RW	0x0	intr_clr_dsp_hold_valid Display hold valid interrupt clear(Auto clear).
5	RW	0x0	intr_clr_fs_field Field start interrupt clear (Auto clear).
4	RW	0x0	intr_clr_post_buf_empty Post buffer empty interrupt clear(Auto clear).
3	RW	0x0	intr_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear).

Bit	Attr	Reset Value	Description
2	RW	0x0	intr_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear).
1	RO	0x0	reserved
0	RW	0x0	intr_clr_fs Frame start interrupt clear (Auto clear).

VOP2_PORT2_INTR_STATUS

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_status_post_full Post buffer almost full interrupt status.
8	RO	0x0	reserved
7	RW	0x0	intr_status_vfp Display vfp interrupt status.
6	RW	0x0	intr_status_dsp_hold_valid Display hold valid interrupt status.
5	RW	0x0	intr_status_fs_field Field start interrupt status.
4	RW	0x0	intr_status_post_buf_empty Post buffer empty interrupt status.
3	RW	0x0	intr_status_line_flag1 Line flag 1 interrupt status.
2	RW	0x0	intr_status_line_flag0 Line flag 0 Interrupt status.
1	RO	0x0	reserved
0	RW	0x0	intr_status_fs Frame start interrupt status.

VOP2_PORT2_INTR_RAW_STATUS

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intr_raw_status_post_full Post buffer almost full interrupt raw status.
8	RO	0x0	reserved
7	RW	0x0	intr_raw_status_vfp Display vfp interrupt raw status.
6	RW	0x0	intr_raw_status_dsp_hold_valid Display hold valid interrupt raw status.
5	RW	0x0	intr_raw_status_fs_field Field start interrupt craw status.
4	RW	0x0	intr_raw_status_post_buf_empty Post buffer empty interrupt raw status.
3	RW	0x0	intr_raw_status_line_flag1 Line flag 1 Interrupt raw status.
2	RW	0x0	intr_raw_status_line_flag0 Line flag 0 Interrupt raw status.
1	RO	0x0	reserved
0	RW	0x0	intr_raw_status_fs Frame start interrupt raw status.

VOP2_AFBCD_INTR_EN

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	int_en_afbcd3_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
6	RW	0x0	int_en_afbcd3_hreg_dec_resp 1'b0: Disable 1'b1: Enable
5	RW	0x0	int_en_afbcd2_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_en_afbcd2_hreg_dec_resp 1'b0: Disable 1'b1: Enable
3	RW	0x0	int_en_afbcd1_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
2	RW	0x0	int_en_afbcd1_hreg_dec_resp 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_en_afbcd0_hreg_axi_rresp 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en_afbcd0_hreg_dec_resp 1'b0: Disable 1'b1: Enable

VOP2_AFBCD_INTR_CLR

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask The write mask bits.
15:8	RO	0x00	reserved
7	RW	0x0	int_clr_afbcd3_hreg_axi_rresp Interrupt clear (Auto clear).
6	RW	0x0	int_clr_afbcd3_hreg_dec_resp Interrupt clear (Auto clear).
5	RW	0x0	int_clr_afbcd2_hreg_axi_rresp Interrupt clear (Auto clear).
4	RW	0x0	int_clr_afbcd2_hreg_dec_resp Interrupt clear (Auto clear).
3	RW	0x0	int_clr_afbcd1_hreg_axi_rresp Interrupt clear (Auto clear).
2	RW	0x0	int_clr_afbcd1_hreg_dec_resp Interrupt clear (Auto clear).
1	RW	0x0	int_clr_afbcd0_hreg_axi_rresp Interrupt clear (Auto clear).
0	RW	0x0	int_clr_afbcd0_hreg_dec_resp Interrupt clear (Auto clear).

VOP2_AFBCD_INTR_STATUS

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	int_status_afbcd3_hreg_axi_rresp Interrupt status.
6	RW	0x0	int_status_afbcd3_hreg_dec_resp Interrupt status.
5	RW	0x0	int_status_afbcd2_hreg_axi_rresp Interrupt status.
4	RW	0x0	int_status_afbcd2_hreg_dec_resp Interrupt status.
3	RW	0x0	int_status_afbcd1_hreg_axi_rresp Interrupt status.
2	RW	0x0	int_status_afbcd1_hreg_dec_resp Interrupt status.
1	RW	0x0	int_status_afbcd0_hreg_axi_rresp Interrupt status.
0	RW	0x0	int_status_afbcd0_hreg_dec_resp Interrupt status.

VOP2_AFBCD_INTR_RAW_STATUS

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	int_raw_status_afbcd3_hreg_axi_rresp Interrupt raw status.
6	RW	0x0	int_raw_status_afbcd3_hreg_dec_resp Interrupt raw status.
5	RW	0x0	int_raw_status_afbcd2_hreg_axi_rresp Interrupt raw status.
4	RW	0x0	int_raw_status_afbcd2_hreg_dec_resp Interrupt raw status.
3	RW	0x0	int_raw_status_afbcd1_hreg_axi_rresp Interrupt raw status.
2	RW	0x0	int_raw_status_afbcd1_hreg_dec_resp Interrupt raw status.
1	RW	0x0	int_raw_status_afbcd0_hreg_axi_rresp Interrupt raw status.
0	RW	0x0	int_raw_status_afbcd0_hreg_dec_resp Interrupt raw status.

13.4.2 Overlay register description

13.4.2.1 Registers Summary

The base address of overlay registers is 0x0600.

Name	Offset	Size	Reset Value	Description
VOP2_OVERLAY_CTRL	0x0000	W	0x00000000	OVERLAY control register.
VOP2_LAYER_SEL	0x0004	W	0x00763210	OVERLAY layer select.
VOP2_PORT_SEL	0x0008	W	0x84000743	OVERLAY port select.
VOP2_CLUSTER0_MIX_SRC_COLOR_CTRL	0x0010	W	0x00000000	To configure the source color of cluster0 MIX.
VOP2_CLUSTER0_MIX_DST_COLOR_CTRL	0x0014	W	0x00000000	To configure the destination color of cluster0 MIX.

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER0_MIX_SRC_ALPHA_CTRL	0x0018	W	0x00000000	To configure the source alpha of cluster0 MIX.
VOP2_CLUSTER0_MIX_DST_ALPHA_CTRL	0x001C	W	0x00000000	To configure the destination alpha of cluster0 MIX.
VOP2_CLUSTER1_MIX_SRC_COLOR_CTRL	0x0020	W	0x00000000	To configure the source color of cluster1 MIX.
VOP2_CLUSTER1_MIX_DST_COLOR_CTRL	0x0024	W	0x00000000	To configure the destination color of cluster1 MIX.
VOP2_CLUSTER1_MIX_SRC_ALPHA_CTRL	0x0028	W	0x00000000	To configure the source alpha of cluster1 MIX.
VOP2_CLUSTER1_MIX_DST_ALPHA_CTRL	0x002C	W	0x00000000	To configure the destination alpha of cluster1 MIX.
VOP2_MIX0_SRC_COLOR_CTRL	0x0050	W	0x00000000	To configure the source color of MIX0.
VOP2_MIX0_DST_COLOR_CTRL	0x0054	W	0x00000000	To configure the destination color of MIX0.
VOP2_MIX0_SRC_ALPHA_CTRL	0x0058	W	0x00000000	To configure the source alpha of MIX0.
VOP2_MIX0_DST_ALPHA_CTRL	0x005C	W	0x00000000	To configure the destination alpha of MIX0.
VOP2_MIX1_SRC_COLOR_CTRL	0x0060	W	0x00000000	To configure the source color of MIX1.
VOP2_MIX1_DST_COLOR_CTRL	0x0064	W	0x00000000	To configure the destination color of MIX1.
VOP2_MIX1_SRC_ALPHA_CTRL	0x0068	W	0x00000000	To configure the source alpha of MIX1.
VOP2_MIX1_DST_ALPHA_CTRL	0x006C	W	0x00000000	To configure the destination alpha of MIX1.
VOP2_MIX2_SRC_COLOR_CTRL	0x0070	W	0x00000000	To configure the source color of MIX2.
VOP2_MIX2_DST_COLOR_CTRL	0x0074	W	0x00000000	To configure the destination color of MIX2.
VOP2_MIX2_SRC_ALPHA_CTRL	0x0078	W	0x00000000	To configure the source alpha of MIX2.
VOP2_MIX2_DST_ALPHA_CTRL	0x007C	W	0x00000000	To configure the destination alpha of MIX2.
VOP2_MIX3_SRC_COLOR_CTRL	0x0080	W	0x00000000	To configure the source color of MIX3.
VOP2_MIX3_DST_COLOR_CTRL	0x0084	W	0x00000000	To configure the destination color of MIX3.
VOP2_MIX3_SRC_ALPHA_CTRL	0x0088	W	0x00000000	To configure the source alpha of MIX3.
VOP2_MIX3_DST_ALPHA_CTRL	0x008C	W	0x00000000	To configure the destination alpha of MIX3.
VOP2_MIX4_SRC_COLOR_CTRL	0x0090	W	0x00000000	To configure the source color of MIX4.
VOP2_MIX4_DST_COLOR_CTRL	0x0094	W	0x00000000	To configure the destination color of MIX4.
VOP2_MIX4_SRC_ALPHA_CTRL	0x0098	W	0x00000000	To configure the source alpha of MIX4.
VOP2_MIX4_DST_ALPHA_CTRL	0x009C	W	0x00000000	To configure the destination alpha of MIX4.

Name	Offset	Size	Reset Value	Description
VOP2_MIX5_SRC_COLOR_CTRL	0x00A0	W	0x00000000	To configure the source color of MIX5.
VOP2_MIX5_DST_COLOR_CTRL	0x00A4	W	0x00000000	To configure the destination color of MIX5.
VOP2_MIX5_SRC_ALPHA_CTRL	0x00A8	W	0x00000000	To configure the source alpha of MIX5.
VOP2_MIX5_DST_ALPHA_CTRL	0x00AC	W	0x00000000	To configure the destination alpha of MIX5.
VOP2_MIX6_SRC_COLOR_CTRL	0x00B0	W	0x00000000	To configure the source color of MIX6.
VOP2_MIX6_DST_COLOR_CTRL	0x00B4	W	0x00000000	To configure the destination color of MIX6.
VOP2_MIX6_SRC_ALPHA_CTRL	0x00B8	W	0x00000000	To configure the source alpha of MIX6.
VOP2_MIX6_DST_ALPHA_CTRL	0x00BC	W	0x00000000	To configure the destination alpha of MIX6.
VOP2_HDR0_MIX_SRC_COLOR_CTRL	0x00C0	W	0x00000000	To configure the source color of HDR0 MIX.
VOP2_HDR0_MIX_DST_COLOR_CTRL	0x00C4	W	0x00000000	To configure the destination color of HDR0 MIX.
VOP2_HDR0_MIX_SRC_ALPHA_CTRL	0x00C8	W	0x00000000	To configure the source alpha of HDR0 MIX.
VOP2_HDR0_MIX_DST_ALPHA_CTRL	0x00CC	W	0x00000000	To configure the destination alpha of HDR0 MIX.
VOP2_DP0_BG_MIX_CTRL	0x00E0	W	0x26000000	To contro the background MIX of video port0.
VOP2_DP1_BG_MIX_CTRL	0x00E4	W	0x26000000	To contro the background MIX of video port1.
VOP2_DP2_BG_MIX_CTRL	0x00E8	W	0x26000000	To contro the background MIX of video port2.
VOP2_Cluster_DLY_NUM	0x00F0	W	0x00000000	To configure the delay cycle of cluster.
VOP2_SMART_DLY_NUM	0x00F8	W	0x14141414	To configure the delay cycle of esmart.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.2.2 Detail Registers Description

VOP2_OVERLAY_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	layer_sel_regdone_sel_imd Select overlay_layer_sel and overlay_port_sel regdone. 2'b00: video port0 2'b01: video port1 2'b1x: video port2
29	RO	0x0	reserved
28	RW	0x0	layer_sel_regdone_imd Enable interface control register regdone immediately.
27:6	RO	0x000000	reserved
5	RW	0x0	sdr2hdr_path_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	hdr10_path_en 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	vp2_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
1	RW	0x0	vp1_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
0	RW	0x0	vp0_overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay

VOP2_LAYER_SEL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x7	layer5_sel layer5 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1
19	RO	0x0	reserved
18:16	RW	0x6	layer4_sel layer4 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1
15	RO	0x0	reserved
14:12	RW	0x3	layer3_sel layer3 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x2	layer2_sel layer2 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1
7	RO	0x0	reserved
6:4	RW	0x1	layer1_sel layer1 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1
3	RO	0x0	reserved
2:0	RW	0x0	layer0_sel layer0 select port. 3'b000: cluster0 3'b001: cluster1 3'b010: esmart0 3'b011: smart0 3'b100: reserved 3'b101: reserved 3'b110: esmart1 3'b111: smart1

VOP2_PORT_SEL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RW	0x2	smart1_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved
29:28	RW	0x0	smart0_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved
27:26	RW	0x1	esmart1_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	esmart0_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved
23:20	RO	0x0	reserved
19:18	RW	0x0	cluster1_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved
17:16	RW	0x0	cluster0_sel_port 2'b00: Video port0 2'b01: Video port1 2'b10: Video port2 2'b11: reserved
15:11	RO	0x00	reserved
11:8	RW	0x7	port2_mux port2 output mux is selected according to the layer number. Note that port2_mux >= port1_mux. 4'b0010: 3 - port0_layer_number - port1_layer_number 4'b0011: 4 - port0_layer_number - port1_layer_number 4'b0100: 5 - port0_layer_number - port1_layer_number 4'b0101: 6 - port0_layer_number - port1_layer_number
7:4	RW	0x4	port1_mux port1 output mux is selected according to the layer number. Note that port1_mux >= port0_mux. 4'b0001: 2 - port0_layer_number 4'b0010: 3 - port0_layer_number 4'b0011: 4 - port0_layer_number 4'b0100: 5 - port0_layer_number 4'b0101: 6 - port0_layer_number 4'b1000: 0 layers
3:0	RW	0x3	port0_mux port0 output mux is selected according to the layer number . 4'b0000: 1 layer 4'b0001: 2 layers 4'b0010: 3 layers 4'b0011: 4 layers 4'b0100: 5 layers 4'b0101: 6 layers 4'b1000: 0 layers

VOP2_CLUSTER0_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster0_mix_src_global_alpha0 Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster0_mix_src_dst_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	cluster0_mix_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster0_mix_src_factor_mode0 Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster0_mix_src_alpha_cal_mode0 Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster0_mix_src_blend_mode0 Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster0_mix_src_alpha_mode0 Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster0_mix_src_color_mode0 Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_CLUSTER0_MIX_DST_COLOR_CTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster0_mix_dst_global_alpha0 Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster0_mix_dst_factor_mode0 Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster0_mix_dst_alpha_cal_mode0 Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster0_mix_dst_blend_mode0 Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	cluster0_mix_dst_alpha_mode0 Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster0_mix_dst_color_mode0 Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_CLUSTER0_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster0_mix_src_factor_mode1 Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster0_mix_src_alpha_cal_mode1 Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster0_mix_src_blend_mode1 Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster0_mix_src_alpha_mode1 Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_CLUSTER0_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster0_mix_dst_factor_mode1 Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster0_mix_dst_alpha_cal_mode1 Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	cluster0_mix_dst_blend_mode1 Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster0_mix_dst_alpha_mode1 Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_CLUSTER1_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster1_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	cluster1_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cluster1_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	cluster1_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster1_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster1_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster1_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	cluster1_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_CLUSTER1_MIX_DST_COLOR_CTRL

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cluster1_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	cluster1_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster1_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster1_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster1_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	cluster1_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_CLUSTER1_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster1_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	cluster1_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	cluster1_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	cluster1_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_CLUSTER1_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	cluster1_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	cluster1_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	cluster1_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	cluster1_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX0_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix0_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix0_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix0_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix0_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix0_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix0_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix0_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix0_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX0_DST_COLOR_CTRL

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix0_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix0_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix0_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix0_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix0_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix0_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX0_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix0_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix0_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix0_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix0_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX0_DST_ALPHA_CTRL

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix0_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix0_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix0_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix0_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX1_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	mix1_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix1_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix1_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix1_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix1_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix1_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix1_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix1_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX1_DST_COLOR_CTRL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix1_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix1_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads

Bit	Attr	Reset Value	Description
4	RW	0x0	mix1_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix1_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix1_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix1_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX1_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix1_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix1_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix1_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix1_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX1_DST_ALPHA_CTRL

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix1_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix1_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix1_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix1_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX2_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix2_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix2_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix2_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix2_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix2_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix2_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix2_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix2_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX2_DST_COLOR_CTRL

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix2_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix2_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix2_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix2_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix2_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix2_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX2_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix2_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix2_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix2_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix2_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX2_DST_ALPHA_CTRL

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix2_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix2_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix2_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix2_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX3_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix3_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix3_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	mix3_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix3_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix3_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix3_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix3_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix3_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX3_DST_COLOR_CTRL

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix3_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix3_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix3_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix3_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	mix3_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix3_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX3_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix3_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix3_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix3_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix3_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX3_DST_ALPHA_CTRL

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix3_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix3_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"

Bit	Attr	Reset Value	Description
3:2	RW	0x0	mix3_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix3_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX4_SRC_COLOR_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix4_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix4_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix4_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix4_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix4_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix4_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix4_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix4_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX4_DST_COLOR_CTRL

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix4_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix4_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix4_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix4_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix4_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix4_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX4_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix4_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix4_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix4_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix4_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As

Bit	Attr	Reset Value	Description
0	RO	0x0	reserved

VOP2_MIX4_DST_ALPHA_CTRL

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix4_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix4_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix4_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix4_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX5_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix5_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix5_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix5_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix5_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	mix5_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix5_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix5_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix5_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX5_DST_COLOR_CTRL

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix5_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix5_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix5_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix5_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix5_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix5_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX5_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix5_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix5_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix5_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix5_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX5_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix5_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix5_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix5_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix5_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_MIX6_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	mix6_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	mix6_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mix6_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	mix6_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix6_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix6_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix6_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	mix6_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_MIX6_DST_COLOR_CTRL

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	mix6_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	mix6_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads

Bit	Attr	Reset Value	Description
4	RW	0x0	mix6_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix6_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix6_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	mix6_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_MIX6_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	mix6_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	mix6_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	mix6_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	mix6_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_MIX6_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x0	mix6_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	mix6_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	mix6_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	mix6_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_HDR0_MIX_SRC_COLOR_CTRL

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr0_mix_src_global_alpha Source global alpha value(Ags).
15:10	RO	0x00	reserved
9	RW	0x0	hdr0_mix_src_top_swap Swap top and bottom layer. 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdr0_mix_src_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable
7:5	RW	0x0	hdr0_mix_src_factor_mode Source factor of color channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags
4	RW	0x0	hdr0_mix_src_alpha_cal_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr0_mix_src_blend_mode Source alpha blending mode of color channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8

Bit	Attr	Reset Value	Description
1	RW	0x0	hdr0_mix_src_alpha_mode Source alpha mode of color channel. 1'b0: As 1'b1: 255-As
0	RW	0x0	hdr0_mix_src_color_mode Source color mode. 1'b0: Cs 1'b1: Cs*As0"

VOP2_HDR0_MIX_DST_COLOR_CTRL

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hdr0_mix_dst_global_alpha Destination global alpha value(Agd).
15:8	RO	0x00	reserved
7:5	RW	0x0	hdr0_mix_dst_factor_mode Destination factor of color channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr0_mix_dst_alpha_cal_mode Destination alpha select mode of color channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr0_mix_dst_blend_mode Destination alpha blending mode of color channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr0_mix_dst_alpha_mode Destination alpha mode of color channel. 1'b0: Ad 1'b1: 255-Ad
0	RW	0x0	hdr0_mix_dst_color_mode Destination color mode. 1'b0: Cd 1'b1: Cd*Ad0"

VOP2_HDR0_MIX_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	hdr0_mix_src_factor_mode Source factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: Ad0" 3'b011: 256-Ad0" 3'b100: As0" 3'b101: Ags

Bit	Attr	Reset Value	Description
4	RW	0x0	hdr0_mix_src_alpha_cal_mode Source alpha select mode of alpha channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
3:2	RW	0x0	hdr0_mix_src_blend_mode Source alpha blending mode of alpha channel. 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8
1	RW	0x0	hdr0_mix_src_alpha_mode Source alpha mode of alpha channel. 1'b0: As 1'b1: 255-As
0	RO	0x0	reserved

VOP2_HDR0_MIX_DST_ALPHA_CTRL

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	hdr0_mix_dst_factor_mode Destination factor of alpha channel. 3'b000: 0 3'b001: 256 3'b010: As0" 3'b011: 256-As0" 3'b100: Ad0" 3'b101: Ads
4	RW	0x0	hdr0_mix_dst_alpha_cal_mode Destination alpha select mode of alpha channel. 1'b0: Ad0_"+Ad0_">>7 1'b1: Ad0_"
3:2	RW	0x0	hdr0_mix_dst_blend_mode Destination alpha blending mode of alpha channel. 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8
1	RW	0x0	hdr0_mix_dst_alpha_mode Destination alpha mode of alpha channel. 1'b0: Ad 1'b1: 255-Ad
0	RO	0x0	reserved

VOP2_DP0_BG_MIX_CTRL

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:24	RW	0x26	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"

Bit	Attr	Reset Value	Description
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_DP1_BG_MIX_CTRL

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x26	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_DP2_BG_MIX_CTRL

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x26	dp_bg_dly_num BG delay cycle number.
23:16	RO	0x00	reserved
15:8	RW	0x00	dp_bg_global_alpha Source global alpha value(Ags).
7:4	RO	0x0	reserved
3	RW	0x0	dp_bg_alpha_sat_mode Source alpha select mode of color channel. 1'b0: As0_"+As0_">>7 1'b1: As0_"

Bit	Attr	Reset Value	Description
2	RW	0x0	dp_bg_alpha_pre_mul Source color mode. 1'b0: Cs 1'b1: Cs*As0"
1	RW	0x0	dp_bg_alpha_mode Select source alpha. 1'b0: per_pixel alpha 1'b1: global alpha
0	RW	0x0	dp_bg_alpha_en Enable alpha blending. 1'b0: Disable 1'b1: Enable

VOP2_Cluster_DLY_NUM

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cluster1_1_dly_num Cluster1_1 delay cycle number.
23:16	RW	0x00	cluster1_0_dly_num Cluster1_0 delay cycle number.
15:8	RW	0x00	cluster0_1_dly_num Cluster0_1 delay cycle number.
7:0	RW	0x00	cluster0_0_dly_num Cluster0_0 delay cycle number.

VOP2_SMART_DLY_NUM

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:24	RW	0x14	smart1_dly_num Smart0 delay cycle number.
23:16	RW	0x14	smart0_dly_num Smart0 delay cycle number.
15:8	RW	0x14	esmart1_dly_num Esmart1 delay cycle number.
7:0	RW	0x14	esmart0_dly_num Esmart0 delay cycle number.

13.4.3 Post-process0 register description

13.4.3.1 Registers Summary

The base address of post-process0 registers is 0x0c00.

Name	Offset	Size	Reset Value	Description
VOP2_POST0_DSP_CTRL	0x0000	W	0x8000000F	To control the display mode of video port0.
VOP2_POST0_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video port0.
VOP2_POST0_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
VOP2_POST0_RESERVED2	0x000C	W	0x00000000	Register0000 Description
VOP2_POST0_3D_LUT_CTRL	0x0010	W	0x00000000	To control 3D LUT.
VOP2_POST0_3D_LUT_R	0x0014	W	0x00000000	To configure the red component of 3D LUT.

Name	Offset	Size	Reset Value	Description
VOP2_POST0_3D_LUT_G	0x0018	W	0x00000000	To configure the green component of 3D LUT.
VOP2_POST0_3D_LUT_B	0x001C	W	0x00000000	To configure the blue component of 3D LUT.
VOP2_POST0_3DLUT_MST	0x0020	W	0x00000000	To configure the starting address of 3D LUT in memory.
VOP2_POST0_DSP_BG	0x002C	W	0x00000000	To configure the background color of video port0.
VOP2_POST0_PRE_SCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video port0.
VOP2_POST0_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video port0.
VOP2_POST0_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video port0.
VOP2_POST0_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the scaling factor of post-process.
VOP2_POST0_SCL_CTRL	0x0040	W	0x00000000	To enable the scaling of post-process.
VOP2_POST0_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST0_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST0_DSP_HACT_ST_END	0x004C	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST0_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST0_DSP_VACT_ST_END	0x0054	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST0_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST0_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST0_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH.
VOP2_POST0_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH.
VOP2_POST0_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH.
VOP2_POST0_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH.
VOP2_POST0_FRC_LOWER01_0	0x00A0	W	0x12844821	To configure the filter coefficients of FRC.
VOP2_POST0_FRC_LOWER01_1	0x00A4	W	0x21488412	To configure the filter coefficients of FRC.
VOP2_POST0_FRC_LOWER10_0	0x00A8	W	0xA55A9696	To configure the filter coefficients of FRC.
VOP2_POST0_FRC_LOWER10_1	0x00AC	W	0x5AA56969	To configure the filter coefficients of FRC.
VOP2_POST0_FRC_LOWER11_0	0x00B0	W	0xDEB77BED	To configure the filter coefficients of FRC.
VOP2_POST0_FRC_LOWER11_1	0x00B4	W	0xED7BB7DE	To configure the filter coefficients of FRC.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3.2 Detail Registers Description

VOP2_POST0_DSP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x1	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: normal output 1'b1: all output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RW	0x0	post_lb_mode 1'b0: 4x4096 1'b1: 8x2048 if post_act_width > 2048 post_lb_mode =0;else config 0 or 1
22:21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RW	0x0	dsp_win_bypass If all layer are closed,enable dsp_win_bypass.
14	RW	0x0	dsp_y_mir_en 1'b0: no y_mirror 1'b1: y_mirror
13	RW	0x0	dsp_x_mir_en 1'b0: no x_mirror 1'b1: x_mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display chapter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: normal 1'b1: invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsp_core_dclk_sel If panel is 480i or 576i, it's enable. 1'b0: dclk_core sel dclk 1'b1: dclk_core sel dclk div2
3:0	RW	0xf	dsp_out_mode 4'b0000: Parallel 24-bit output {R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output {R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output {R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'b1110: YUV420 output for HDMI 4'b1111: Parallel 30-bit RGBaaa output {R[9:0],G[9:0],B[9:0]} Others: Reserved

VOP2_POST0_MIPI_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: new frame is started by te. 1'b1: new frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	dual_channel_overlap_num 4'h0: overlap num 0 4'h1: overlap num 2 4'h2: overlap num 4 4'h3: overlap num 6 4'h4: overlap num 8 4'h5: overlap num 10 4'h6: overlap num 12 4'h7: overlap num 14 4'h8: overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	dual_channel_swap Swap two channel data of MIPI.
20	RW	0x0	dual_channel_en Enable mipi dual channel. 1'b0: Disable 1'b1: Enable
19:6	RO	0x00000	reserved
5:4	RW	0x0	dclk_out_ddr_ctrl 2'b00: normal 2'b01: dclk_out is ddr clk Others: reserved
3:0	RO	0x0	reserved

VOP2_POST0_COLOR_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: horizontal mode 1'b1: vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

VOP2_POST0_RESERVED2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Field0000 x'bxxx(bits < 4), x'hxxxx(bits >= 4)

VOP2_POST0_3D_LUT_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dsp_3dlut_addr AHB write or read lut address of 3d_lut.
15:4	RO	0x000	reserved
3	RW	0x0	dsp_3dlut_mode 1'b0: lut is fetched by axi 1'b1: lut is fetched by ahb
2	RW	0x0	dsp_3dlut_update_en Update the lut of 3d_lut. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dsp_3dlut_bypass_en Bypass 3d_lut function. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dsp_3dlut_en 1'b0: Disable 1'b1: Enable

VOP2_POST0_3D_LUT_R

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_r_comp 3D_lut red component.

VOP2_POST0_3D_LUT_G

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_g_comp 3D_lut green component.

VOP2_POST0_3D_LUT_B

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	lut_3d_b_comp 3D_lut blue component.

VOP2_POST0_3DLUT_MST

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	post_3dlut_mst 3D_lut memory start address.

VOP2_POST0_DSP_BG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

VOP2_POST0_PRE_SCAN_HTIMING

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

VOP2_POST0_DSP_HACT_INFO

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point.

VOP2_POST0_DSP_VACT_INFO

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

VOP2_POST0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12.
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12.

VOP2_POST0_SCL_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	post0_ver_sd_en 1'b0: post ver scl down disable 1'b1: post ver scl down enable

Bit	Attr	Reset Value	Description
0	RW	0x0	post0_hor_sd_en 1'b0: post hor scl down disable 1'b1: post hor scl down enable

VOP2_POST0_DSP_VACT_INFO_F1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

VOP2_POST0_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

VOP2_POST0_DSP_HACT_ST_END

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

VOP2_POST0_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

VOP2_POST0_DSP_VACT_ST_END

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

VOP2_POST0_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

VOP2_POST0_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

VOP2_POST0_BCSH_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Disable 1'b1: Enable

VOP2_POST0_BCSH_BCS

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

VOP2_POST0_BCSH_H

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

VOP2_POST0_BCSH_COLOR_BAR

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

VOP2_POST0_FRC_LOWER01_0

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 FRC parameter lowerbit = 2'b01, frm1.
15:0	RW	0x4821	lower01_frm0 FRC parameter lowerbit = 2'b01, frm0.

VOP2_POST0_FRC_LOWER01_1

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 FRC parameter lowerbit = 2'b01, frm3.
15:0	RW	0x8412	lower01_frm2 FRC parameter lowerbit = 2'b01, frm2.

VOP2_POST0_FRC_LOWER10_0

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 FRC parameter lowerbit = 2'b10, frm1.
15:0	RW	0x9696	lower10_frm0 FRC parameter lowerbit = 2'b10, frm0.

VOP2_POST0_FRC_LOWER10_1

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 FRC parameter lowerbit = 2'b10, frm3.
15:0	RW	0x6969	lower10_frm2 FRC parameter lowerbit = 2'b10, frm2.

VOP2_POST0_FRC_LOWER11_0

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 FRC parameter lowerbit = 2'b11, frm1.
15:0	RW	0x7bed	lower11_frm0 FRC parameter lowerbit = 2'b11, frm0.

VOP2_POST0_FRC_LOWER11_1

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 FRC parameter lowerbit = 2'b11, frm3.
15:0	RW	0xb7de	lower11_frm2 FRC parameter lowerbit = 2'b11, frm2.

13.4.4 Post-process1 register description

13.4.4.1 Registers Summary

The base address of post-process1 registers is 0x0d00.

Name	Offset	Size	Reset Value	Description
VOP2_POST1_DSP_CTRL	0x0000	W	0x00000000	To control the display mode of video port0.
VOP2_POST1_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video port0.
VOP2_POST1_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
VOP2_POST1_RESERVED2	0x000C	W	0x00000000	Register0000 Description
VOP2_POST1_DSP_BG	0x002C	W	0x00000000	To configure the background color of video port0.
VOP2_POST1_PRE_SCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video port0.
VOP2_POST1_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video port0.
VOP2_POST1_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video port0.
VOP2_POST1_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the scaling factor of post-process.

Name	Offset	Size	Reset Value	Description
VOP2_POST1_SCL_CTRL	0x0040	W	0x00000000	To enable the scaling of post-process.
VOP2_POST1_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST1_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST1_DSP_HACT_ST_END	0x004C	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST1_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST1_DSP_VACT_ST_END	0x0054	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST1_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST1_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST1_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH.
VOP2_POST1_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH.
VOP2_POST1_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH.
VOP2_POST1_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH.
VOP2_POST1_CABC_CTRL_0	0x0070	W	0x00000000	To control CABC.
VOP2_POST1_CABC_CTRL_1	0x0074	W	0x00000000	To enable CABC LUT.
VOP2_POST1_CABC_CTRL_2	0x0078	W	0x00000000	To configure the stage of CABC.
VOP2_POST1_CABC_CTRL_3	0x007C	W	0x00000000	To configure the limited global value of CABC.
VOP2_POST1_CABC_GAUSS_LINE0_0	0x0080	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_CABC_GAUSS_LINE0_1	0x0084	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_CABC_GAUSS_LINE1_0	0x0088	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_CABC_GAUSS_LINE1_1	0x008C	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_CABC_GAUSS_LINE2_0	0x0090	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_CABC_GAUSS_LINE2_1	0x0094	W	0x00000000	To configure the filter coefficients of CABC.
VOP2_POST1_PWM_CTRL	0x00C0	W	0x0000200A	The register provides the cotrol of PWM.
VOP2_POST1_PWM_PERIOD_HPR	0x00C4	W	0x00000000	To configure the period of the output waveform.
VOP2_POST1_PWM_DUTY_LPR	0x00C8	W	0x00000000	To configure the duty cycle of the output waveform.
VOP2_POST1_PWM_CNT	0x00CC	W	0x00000000	The register indicates the status of PWM.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.4.2 Detail Registers Description

VOP2_POST1_DSP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: normal output 1'b1: all output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RW	0x0	post_lb_mode 1'b0: 4x4096 1'b1: 8x2048 if post_act_width > 2048 post_lb_mode =0; else config 0 or 1
22:21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RW	0x0	dsp_win_bypass If all layer are closed,enable dsp_win_bypass.
14	RW	0x0	dsp_y_mir_en 1'b0: no y_mirror 1'b1: y_mirror
13	RW	0x0	dsp_x_mir_en 1'b0: no x_mirror 1'b1: x_mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: Disable 1'b1: Enable *See detail description in Delta display charpter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: normal 1'b1: invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsp_core_dclk_sel If panel is 480i or 576i, it's enable. 1'b0: dclk_core sel dclk 1'b1: dclk_core sel dclk div2
3:0	RW	0x0	dsp_out_mode 4'b0000: Parallel 24-bit output {R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output {R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output {R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'b1110: YUV420 output for HDMI 4'b1111: Parallel 30-bit RGBaaa output {R[9:0],G[9:0],B[9:0]} Others: Reserved

VOP2_POST1_MIPI_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: new frame is started by te. 1'b1: new frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	dual_channel_overlap_num 4'h0: overlap num 0 4'h1: overlap num 2 4'h2: overlap num 4 4'h3: overlap num 6 4'h4: overlap num 8 4'h5: overlap num 10 4'h6: overlap num 12 4'h7: overlap num 14 4'h8: overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	dual_channel_swap Swap two channel data of MIPI.
20	RW	0x0	dual_channel_en Enable mipi dual channel. 1'b0: Disable 1'b1: Enable
19:6	RO	0x00000	reserved
5:4	RW	0x0	dclk_out_ddr_ctrl 2'b00: normal 2'b01: dclk_out is ddr clk Others: reserved
3:0	RO	0x0	reserved

VOP2_POST1_COLOR_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: horizontal mode 1'b1: vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

VOP2_POST1_RESERVED2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Field0000

VOP2_POST1_DSP_BG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

VOP2_POST1_PRE_SCAN_HTIMING

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

VOP2_POST1_DSP_HACT_INFO

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point.

VOP2_POST1_DSP_VACT_INFO

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

VOP2_POST1_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12.
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12.

VOP2_POST1_SCL_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	post0_ver_sd_en 1'b0: post ver scl down disable 1'b1: post ver scl down enable
0	RW	0x0	post0_hor_sd_en 1'b0: post hor scl down disable 1'b1: post hor scl down enable

VOP2_POST1_DSP_VACT_INFO_F1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

VOP2_POST1_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

VOP2_POST1_DSP_HACT_ST_END

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

VOP2_POST1_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: valid after frame start 1'b1: valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

VOP2_POST1_DSP_VACT_ST_END

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

VOP2_POST1_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

VOP2_POST1_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

VOP2_POST1_BCSH_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	bcsh_y2r_en 1'b0: Disable 1'b1: Enable

VOP2_POST1_BCSH_BCS

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:6	RO	0x0	reserved
5:0	RW	0x00	brightness Brightness: {-32,31}.

VOP2_POST1_BCSH_H

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

VOP2_POST1_BCSH_COLOR_BAR

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

VOP2_POST1_CABC_CTRL0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	cabc_calc_pixel_num CABC calc pixel numbers = x % * cabc_total_num
3	RW	0x0	cabc_handle_en CABC control pwm

Bit	Attr	Reset Value	Description
2:1	RW	0x0	pwm_config_mode 2'b00: last frame pwm value 2'b01: cur frame pwm value 2'b1x: stage by stage
0	RW	0x0	cabc_en 1'b0: Disable 1'b1: Enable

VOP2_POST1_CABC_CTRL1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:4	RW	0x000000	cabc_total_num CABC totala numbers = h_vd * v_vd
3:1	RO	0x0	reserved
0	RW	0x0	cabc_lut_en CABC pwm lut enable

VOP2_POST1_CABC_CTRL2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31	RW	0x0	max_scale_cfg_enable
30:29	RO	0x0	reserved
28:20	RW	0x000	max_scale_cfg_value
19	RW	0x0	cabc_stage_up_mode 1'b0: mul mode 1'b1: add mode
18:17	RO	0x0	reserved
16:8	RW	0x000	cabc_stage_up when mul mode ,scale stage up (1~1.5 * 256). when add mode ,scale stage up (0x00~0xff)
7:0	RW	0x00	cabc_stage_down when mul mode ,scale stage down (0.667~1 * 256) when add mode ,scale stage down (0x00~0xff)

VOP2_POST1_CABC_CTRL3

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	cabc_global_dn_limit_en CABC global scale down limit enable
7:0	RW	0x00	cabc_global_dn CABC global scale down value

VOP2_POST1_CABC_GAUSS_LINE0_0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line0_3 Gauss parameter t_line0_3
23:16	RW	0x00	t_line0_2 Gauss parameter t_line0_2
15:8	RW	0x00	t_line0_1 Gauss parameter t_line0_1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_line0_0 Gauss parameter t_line0_0

VOP2_POST1_CABC_GAUSS_LINE0_1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_line0_6 Gauss parameter t_line0_6
15:8	RW	0x00	t_line0_5 Gauss parameter t_line0_5
7:0	RW	0x00	t_line0_4 Gauss parameter t_line0_4

VOP2_POST1_CABC_GAUSS_LINE1_0

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line1_3 Gauss parameter t_line1_3
23:16	RW	0x00	t_line1_2 Gauss parameter t_line1_2
15:8	RW	0x00	t_line1_1 Gauss parameter t_line1_1
7:0	RW	0x00	t_line1_0 Gauss parameter t_line1_0

VOP2_POST1_CABC_GAUSS_LINE1_1

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	t_line1_6 Gauss parameter t_line1_6
15:8	RW	0x00	t_line1_5 Gauss parameter t_line1_5
7:0	RW	0x00	t_line1_4 Gauss parameter t_line1_4

VOP2_POST1_CABC_GAUSS_LINE2_0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line2_3 Gauss parameter t_line2_3
23:16	RW	0x00	t_line2_2 Gauss parameter t_line2_2
15:8	RW	0x00	t_line2_1 Gauss parameter t_line2_1
7:0	RW	0x00	t_line2_0 Gauss parameter t_line2_0

VOP2_POST1_CABC_GAUSS_LINE2_1

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	t_line2_6 Gauss parameter t_line2_6
15:8	RW	0x00	t_line2_5 Gauss parameter t_line2_5
7:0	RW	0x00	t_line2_4 Gauss parameter t_line2_4

VOP2_POST1_PWM_CTRL

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods
23:16	RW	0x00	scale This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256)
15	RO	0x0	reserved
14:12	RW	0x2	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel 1'b0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1'b1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en 1'b0: Disable 1'b1: Enable When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption
7:6	RO	0x0	reserved
5	RW	0x0	output_mode 1'b0: left aligned mode 1'b1: center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: negative 1'b1: positive
3	RW	0x1	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: negative 1'b1: positive

Bit	Attr	Reset Value	Description
2:1	RW	0x1	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 2'b01: Continuous mode. PWM produces the waveform continuously 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: reserved
0	RW	0x0	pwm_en 1'b0: Disable 1'b1: Enable If the PWM is worked the one-shot mode, this bit will be cleared at the end of operation

VOP2_POST1_PWM_PERIOD_HPR

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_period If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1)

VOP2_POST1_PWM_DUTY_LPR

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_duty If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1)

VOP2_POST1_PWM_CNT

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_cnt The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1)

13.4.5 Post-process2 register description

13.4.5.1 Registers Summary

The base address of post-process2 registers is 0x0e00.

Name	Offset	Size	Reset Value	Description
VOP2_POST2_DSP_CTRL	0x0000	W	0x00000000	To control the display mode of video port0.
VOP2_POST2_MIPI_CTRL	0x0004	W	0x00000000	To control the MIPI display of video port0.
VOP2_POST2_COLOR_CTRL	0x0008	W	0x00000000	To control color bar.
VOP2_POST2_RESERVED2	0x000C	W	0x00000000	Register0000 Description
VOP2_POST2_DSP_BG	0x002C	W	0x00000000	To configure the background color of video port0.
VOP2_POST2_PRE_SCAN_HTIMING	0x0030	W	0x00000000	To configure the pre-process timing of video port0.
VOP2_POST2_DSP_HACT_INFO	0x0034	W	0x00000000	To configure the post-process horizontal timing of video port0.
VOP2_POST2_DSP_VACT_INFO	0x0038	W	0x00000000	To configure the post-process vertical timing of video port0.
VOP2_POST2_SCL_FACTOR_YRGB	0x003C	W	0x00000000	To configure the scaling factor of post-process.
VOP2_POST2_SCL_CTRL	0x0040	W	0x00000000	To enable the scaling of post-process.
VOP2_POST2_DSP_VACT_INFO_F1	0x0044	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST2_DSP_HTOTAL_HS_END	0x0048	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST2_DSP_HACT_ST_END	0x004C	W	0x00000000	To configure the horizontal timing of video port0.
VOP2_POST2_DSP_VTOTAL_VS_END	0x0050	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST2_DSP_VACT_ST_END	0x0054	W	0x00000000	To configure the vertical timing of video port0.
VOP2_POST2_DSP_VS_ST_END_F1	0x0058	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST2_DSP_VACT_ST_END_F1	0x005C	W	0x00000000	To configure the interlace vertical timing of video port0.
VOP2_POST2_BCSH_CTRL	0x0060	W	0x00000000	To control BCSH.
VOP2_POST2_BCSH_BCS	0x0064	W	0x00000000	To configure the brightness, contrast, sat and output mode of BCSH.
VOP2_POST2_BCSH_H	0x0068	W	0x00000000	To configure the hue of BCSH.
VOP2_POST2_BCSH_COLOR_BAR	0x006C	W	0x00000000	To enable BCSH.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.5.2 Detail Registers Description

VOP2_POST2_DSP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	vop_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
30	RW	0x0	vop_fp_standby_en_imd Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0: Disable 1'b1: Enable * Black display is recommended before setting standby mode enable.
29	RO	0x0	reserved
28	RW	0x0	dsp_lut_en 1'b0: Disable 1'b1: Enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.
27	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black(0x000000).
26	RW	0x0	dsp_out_zero 1'b0: normal output 1'b1: all output '0'
25	RO	0x0	reserved
24	RW	0x0	dsp_blank_en When this bit enable, the Hsync/Vsync/Den output is blank.
23	RW	0x0	post_lb_mode 1'b0: 4x4096 1'b1: 8x2048 if post_act_width > 2048 post_lb_mode =0; else config 0 or 1
22:21	RO	0x0	reserved
20	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
19:18	RW	0x0	dither_down_sel 2'b0: Allegro 2'b1: FRC
17	RW	0x0	dither_down_en 1'b0: Disable 1'b1: Enable
16	RW	0x0	pre_dither_down_en 10bit->8bit (allegro).
15	RW	0x0	dsp_win_bypass If all layer are closed,enable dsp_win_bypass.

Bit	Attr	Reset Value	Description
14	RW	0x0	dsp_y_mir_en 1'b0: no y_mirror 1'b1: y_mirror
13	RW	0x0	dsp_x_mir_en 1'b0: no x_mirror 1'b1: x_mirror
12	RW	0x0	dsp_dummy_swap 1'b0: B+G+R+dummy 1'b1: dummy+B+G+R
11	RW	0x0	dsp_delta_swap 1'b0: disable 1'b1: enable *See detail description in Delta display charpter
10	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
9	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
8	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
7	RW	0x0	dsp_interlace 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsp_filed_pol 1'b0: Normal 1'b1: Invert
5	RW	0x0	dsp_p2i_en Enable p2i. 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsp_core_dclk_sel If panel is 480i or 576i, it's enable. 1'b0: dclk_core sel dclk 1'b1: dclk_core sel dclk div2
3:0	RW	0x0	dsp_out_mode 4'b0000: Parallel 24-bit output {R[7:0],2'b0,G[7:0],2'b0,B[7:0],2'b0} 4'b0001: Parallel 18-bit RGB666 output {R[5:0],4'b0,G[5:0],4'b0,B[5:0],4'b0} 4'b0010: Parallel 16-bit RGB565 output {R[4:0],5'b0,G[5:0],4'b0,B[4:0],5'b0} 4'b1110: YUV420 output for HDMI 4'b1111: Parallel 30-bit RGBaaa output {R[9:0],G[9:0],B[9:0]} Others: Reserved

VOP2_POST2_MIPI_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	edpi_wms_fs Frame start in hold mode. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
30	RW	0x0	edpi_wms_hold_en Enable hold mode. 1'b0: Disable 1'b1: Enable
29	RW	0x0	edpi_te_mode 1'b0: New frame is started by te. 1'b1: New frame is started by te and wms_fs.
28	RW	0x0	edpi_te_en Enable MIPI TE. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	dual_channel_overlap_num 4'h0: Overlap num 0 4'h1: Overlap num 2 4'h2: Overlap num 4 4'h3: Overlap num 6 4'h4: Overlap num 8 4'h5: Overlap num 10 4'h6: Overlap num 12 4'h7: Overlap num 14 4'h8: Overlap num 16
23:22	RO	0x0	reserved
21	RW	0x0	dual_channel_swap Swap two channel data of MIPI.
20	RW	0x0	dual_channel_en Enable mipi dual channel. 1'b0: Disable 1'b1: Enable
19:6	RO	0x00000	reserved
5:4	RW	0x0	dclk_out_ddr_ctrl 2'b00: normal 2'b01: dclk_out is ddr clk Others: reserved
3:0	RO	0x0	reserved

VOP2_POST2_COLOR_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	color_bar_mode Select color bar mode. 1'b0: Horizontal mode 1'b1: Vertical mode
0	RW	0x0	color_bar_en Enable color bar. 1'b0: Disable 1'b1: Enable

VOP2_POST2_RESERVED2

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Field0000

VOP2_POST2_DSP_BG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	dsp_bg_red 10bit red color of background.
19:10	RW	0x000	dsp_bg_blue 10bit blue color of background.
9:0	RW	0x000	dsp_bg_green 10bit green color of background.

VOP2_POST2_PRE_SCAN_HTIMING

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	pre_scan_hactive Pre_scan horizontal active pixel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	pre_scan_hblank Pre_scan horizontal blank pixel.

VOP2_POST2_DSP_HACT_INFO

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end_post Panel display scanning horizontal active end point.

VOP2_POST2_DSP_VACT_INFO

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post Panel display scanning horizontal active end point.

VOP2_POST2_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	post_vs_factor Factor=((src_height[31:16])/(dst_height[31:16]))*2^12.
15:0	RW	0x0000	post_hs_factor Factor=((src_width[15:0])/(dst_width[15:0]))*2^12.

VOP2_POST2_SCL_CTRL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	post0_ver_sd_en 1'b0: Post ver scl down disable 1'b1: Post ver scl down enable

Bit	Attr	Reset Value	Description
0	RW	0x0	post0_hor_sd_en 1'b0: Post hor scl down disable 1'b1: Post hor scl down enable

VOP2_POST2_DSP_VACT_INFO_F1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_post_f1 Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_post_f1 Panel display scanning horizontal active end point.

VOP2_POST2_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_htotal Panel display scanning horizontal period.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hs_end Panel display scanning hsync pulse width.

VOP2_POST2_DSP_HACT_ST_END

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_hact_st Panel display scanning horizontal active start point.
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_hact_end Panel display scanning horizontal active end point.

VOP2_POST2_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd Dsp vtotal number valid immediately enable. 1'b0: Valid after frame start 1'b1: Valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end Panel display scanning vsync pulse width.

VOP2_POST2_DSP_VACT_ST_END

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st Panel display scanning vertical active start point.

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end Panel display scanning vertical active end point.

VOP2_POST2_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode).

VOP2_POST2_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode).

VOP2_POST2_BCSH_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0: Disable 1'b1: Enable

VOP2_POST2_BCSH_BCS

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	out_mode 2'b00: Black 2'b01: Blue 2'b10: Color bar 2'b11: Normal video
29:20	RW	0x000	sat_con Saturation*Contrast*256: {0,1.992*1.992}.
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256: {0,1.992}.
7:0	RW	0x00	brightness Brightness: {-32,31}.

VOP2_POST2_BCSH_H

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	cos_hue Cos hue value.
15:9	RO	0x00	reserved
8:0	RW	0x000	sin_hue Sin hue value.

VOP2_POST2_BCSH_COLOR_BAR

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	bcsh_en 1'b0: Bcsh bypass 1'b1: Bcsh enable
30	RO	0x0	reserved
29:20	RW	0x000	color_bar_v V component value of BCSH color bar.
19:10	RW	0x000	color_bar_u U component value of BCSH color bar.
9:0	RW	0x000	color_bar_y Y component value of BCSH color bar.

13.4.6 Cluster register description

13.4.6.1 Registers Summary

The base address of cluster0 registers is 0x1000.
The base address of cluster1 registers is 0x1200.

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER_WIN0_CTRL0	0x0000	W	0x00000000	WIN0 control register0.
VOP2_CLUSTER_WIN0_CTRL1	0x0004	W	0x00000000	WIN0 control register1.
VOP2_CLUSTER_WIN0_CTRL2	0x0008	W	0x00000000	WIN0 control register2.
VOP2_CLUSTER_WIN0_YRGB_MST	0x0010	W	0x00000000	WIN0 YRGB memory starting.

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER_WIN0_VIR	0x0018	W	0x00000000	WIN0 virtual width.
VOP2_CLUSTER_WIN0_ACT_INFO	0x0020	W	0x00000000	WIN0 actual information.
VOP2_CLUSTER_WIN0_DSP_INFO	0x0024	W	0x00000000	WIN0 display information.
VOP2_CLUSTER_WIN0_DSP_ST	0x0028	W	0x00000000	WIN0 display start.
VOP2_CLUSTER_WIN0_DSP_BG	0x002C	W	0x00000000	WIN0 display background.
VOP2_CLUSTER_WIN0_SCL_FACTOR_YRGB	0x0030	W	0x00000000	WIN0 yrgb scale factor.
VOP2_CLUSTER_WIN0_SCL_OFFSET	0x0038	W	0x00000000	WIN0 scale offset.
VOP2_CLUSTER_WIN0_TRANSFORMED_OFFSET	0x003C	W	0x00000000	WIN0 transformed offset
VOP2_CLUSTER_WIN0_AFBCD_OUTPUT_CTRL	0x0050	W	0x00000000	WIN0 afbcd control register.
VOP2_CLUSTER_WIN0_AFBCD_MODE	0x0054	W	0x00000000	WIN0 afbcd mode
VOP2_CLUSTER_WIN0_AFBCD_HDR_PTR	0x0058	W	0x00000000	WIN0 afbcd hdr pointer.
VOP2_CLUSTER_WIN0_AFBCD_VIR_WIDTH	0x005C	W	0x00000000	WIN0 afbcd virtual width.
VOP2_CLUSTER_WIN0_AFBCD_SIZE	0x0060	W	0x00000000	WIN0 afbcd size.
VOP2_CLUSTER_WIN0_AFBCD_PIC_OFFSET	0x0064	W	0x00000000	WIN0 afbcd picture offset.
VOP2_CLUSTER_WIN0_AFBCD_DIS_OFFSET	0x0068	W	0x00000000	WIN0 afbcd display offset.
VOP2_CLUSTER_WIN0_AFBCD_CTRL	0x006C	W	0x00000000	WIN0 afbcd control.
VOP2_CLUSTER_WIN1_CTRL0	0x0080	W	0x00000000	WIN1 control register0.
VOP2_CLUSTER_WIN1_CTRL1	0x0084	W	0x00000000	WIN1 control register1.
VOP2_CLUSTER_WIN1_CTRL2	0x0088	W	0x00000000	WIN1 control register2.
VOP2_CLUSTER_WIN1_YRGB_MST	0x0090	W	0x00000000	WIN1 YRGB memory starting.
VOP2_CLUSTER_WIN1_VIR	0x0098	W	0x00000000	WIN1 virtual width.
VOP2_CLUSTER_WIN1_ACT_INFO	0x00A0	W	0x00000000	WIN1 actual information.
VOP2_CLUSTER_WIN1_DSP_INFO	0x00A4	W	0x00000000	WIN1 display information.
VOP2_CLUSTER_WIN1_DSP_ST	0x00A8	W	0x00000000	WIN1 display start.
VOP2_CLUSTER_WIN1_DSP_BG	0x00AC	W	0x00000000	WIN1 display background.
VOP2_CLUSTER_WIN1_SCL_FACTOR_YRGB	0x00B0	W	0x00000000	WIN1 yrgb scale factor.

Name	Offset	Size	Reset Value	Description
VOP2_CLUSTER_WIN1_SCL_OFFSET	0x00B8	W	0x00000000	WIN1 scale offset.
VOP2_CLUSTER_WIN0_TRANSFORMED_OFFSET	0x00BC	W	0x00000000	WIN1 transformed offset
VOP2_CLUSTER_WIN1_AFBCD_OUTPUT_CTRL	0x00D0	W	0x00000000	WIN1 afbcd control register.
VOP2_CLUSTER_WIN1_AFBCD_MODE	0x00D4	W	0x00000000	WIN1 afbcd mode
VOP2_CLUSTER_WIN1_AFBCD_HDR_PTR	0x00D8	W	0x00000000	WIN1 afbcd hdr pointer.
VOP2_CLUSTER_WIN1_AFBCD_VIR_WIDTH	0x00DC	W	0x00000000	WIN1 afbcd virtual width.
VOP2_CLUSTER_WIN1_AFBCD_SIZE	0x00E0	W	0x00000000	WIN1 afbcd size.
VOP2_CLUSTER_WIN1_AFBCD_PIC_OFFSET	0x00E4	W	0x00000000	WIN1 afbcd picture offset.
VOP2_CLUSTER_WIN1_AFBCD_DIS_OFFSET	0x00E8	W	0x00000000	WIN1 afbcd display offset.
VOP2_CLUSTER_WIN1_AFBCD_CTRL	0x00EC	W	0x00000000	WIN1 afbcd control.
VOP2_CLUSTER_CTRL	0x0100	W	0x00000000	CLUSTER control register.
VOP2_CLUSTER_LG_COE0	0x0110	W	0x00000000	CLUSTER low gauss coefficient.
VOP2_CLUSTER_LG_COE1	0x0114	W	0x00000000	CLUSTER low gauss coefficient.
VOP2_CLUSTER_LG_COE2	0x0118	W	0x00000000	CLUSTER low gauss coefficient.
VOP2_CLUSTER_HG_COE0	0x0120	W	0x00000000	CLUSTER high gauss coefficient.
VOP2_CLUSTER_HG_COE1	0x0124	W	0x00000000	CLUSTER high gauss coefficient.
VOP2_CLUSTER_HG_COE2	0x0128	W	0x00000000	CLUSTER high gauss coefficient.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.6.2 Detail Registers Description

VOP2_CLUSTER_WIN0_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	win0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win0_dither_up_en 1'b0: Disable 1'b1: Enable
17:15	RO	0x0	reserved
14	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	win0_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RW	0x0	win0_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win0_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_no_outstanding 1'b0: Disable 1'b1: Enable
6	RW	0x0	win0_hw_pre_mul_en 1'b0: No hardware pre multiply mode 1'b1: Hardware pre multiply mode
5:1	RW	0x00	win0_data_fmt 5'b00000: ARGB888 5'b00001: RGB888 5'b00010: RGB565 5'b00011: RGB101010 5'b00100: YCbCr420 5'b00101: YCbCr422 5'b00110: YCbCr444 5'b10000: YCbCr420_101010 5'b10001: YCbCr422_101010 5'b10010: YCbCr444_101010
0	RW	0x0	win0_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER_WIN0_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	win0_yrgb_vsd_gt4 If win0 yrgb_act_height/yrgb_dsp_height > 4,win0_yrgb_vsd_gt4 must be enable.
28	RW	0x0	win0_yrgb_vsd_gt2 If win0 yrgb_act_height/yrgb_dsp_height > 2,win0_yrgb_vsd_gt2 must be enable.
27:20	RO	0x00	reserved
19	RW	0x0	win0_yrgb_vsd_mode 1'b0: Bilinear2
18	RW	0x0	win0_yrgb_vsu_mode 1'b0: Bilinear2
17	RO	0x0	reserved
16	RW	0x0	win0_yrgb_hsd_mode 1'b0: Bilinear2

Bit	Attr	Reset Value	Description
15:14	RW	0x0	win0_yrgb_ver_scl_mode 2'b00: no scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
13:12	RW	0x0	win0_yrgb_hor_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
11:4	RO	0x00	reserved
3:2	RW	0x0	win0_bic_coe_sel 2'b00: PRECISE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHELL
1	RO	0x0	reserved
0	RW	0x0	win0_yrgb_axi_gather_en Win0 axi bus yrgb data gather transfer enable.

VOP2_CLUSTER_WIN0_CTRL2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:5	RW	0x0	win0_rid_cbr Axi read id of win0 cbr channel
4	RO	0x0	reserved
3:0	RW	0x0	win0_rid_yrgb Axi read id of win0 yrgb channel

VOP2_CLUSTER_WIN0_YRGB_MST

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst Win0 YRGB frame buffer memory start address.

VOP2_CLUSTER_WIN0_VIR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win0_vir_stride Number of words of Win0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_CLUSTER_WIN0_ACT_INFO

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	win0_act_height win_act_height = (win0 vertical size -1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_act_width win_act_width = (win0 horizontal size -1).

VOP2_CLUSTER_WIN0_DSP_INFO

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win0_dsp_height win0_dsp_height = (win0 vertical size -1).
15:12	RO	0x0	reserved
11:0	RW	0x000	win0_dsp_width win0_dsp_width = (win0 horizontal size -1).

VOP2_CLUSTER_WIN0_DSP_ST

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win0_dsp_yst Win0 vertical start point(y) of the display region.
15:13	RO	0x0	reserved
12:0	RW	0x0000	win0_dsp_xst Win0 horizontal start point(x) of the display region.

VOP2_CLUSTER_WIN0_DSP_BG

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win0_dsp_bg_red Win0 layer Background Red color.
19:10	RW	0x000	win0_dsp_bg_green Win0 layer Background Green color.
9:0	RW	0x000	win0_dsp_bg_blue Win0 layer Background Blue color.

VOP2_CLUSTER_WIN0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_vs_factor_yrgb factor=((LCDC_WIN0_ACT_INFO[31:16]) / (LCDC_WIN0_DSP_INFO[31:16]))*2^12.
15:0	RW	0x0000	win0_hs_factor_yrgb factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_CLUSTER_WIN0_SCL_OFFSET

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

VOP2_CLUSTER_WIN0_TRANSFORMED_OFFSET

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

VOP2_CLUSTER_WIN0_AFBCD_OUTPUT_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x1	win0_afbcd_gating_en win0 afbcd gating enable
0	RW	0x0	win0_afbcd_output_mask_en 1'b0: AFBCD output must be aligned to 16 width/height 1'b1: AFBCD output can be random integer yuv420 width/height is even, yuv422 width is even.

VOP2_CLUSTER_WIN0_AFBCD_MODE

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win0_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when afbcd output
2	RW	0x0	win0_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when afbcd output
1	RW	0x0	win0_rot270_en 1'b0: Rotation 270 disable 1'b1: Rotation 270 angle, when afbcd output
0	RW	0x0	win0_rot90_en 1'b0: Rotation 90 disable 1'b1: Enable, rotation 90 angle when afbcd output

VOP2_CLUSTER_WIN0_AFBCD_HDR_PTR

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_afbcd_hdr_ptr AFBC encode stream starting address in DDR.

VOP2_CLUSTER_WIN0_AFBCD_VIR_WIDTH

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_tail_num header/payload arbiter tail number.
15:0	RW	0x0000	win0_afbcd_pic_vir_width Number of bytes of AFBCD header virtual width. when afbcd mode is x_mirror/rot90/rot270, it must be aligned to 64pixels, or it must be aligned to 16 pixels.

VOP2_CLUSTER_WIN0_AFBCD_SIZE

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_height When win0_afbcd_output_mask_en is 1, it can be random,or it must be aligned to 16bit. Real - 1
15:0	RW	0x0000	win0_afbcd_pic_width When win0_afbcd_output_mask_en is 1, it can be random,or it must be aligned to 16bit. Real - 1

VOP2_CLUSTER_WIN0_AFBCD_PIC_OFFSET

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_pic_yoffset Display image vertical offset in DDR. When win0_afbcd_output_mask_en is 1, it can be random, or it must be aligned to 16bit.
15:0	RW	0x0000	win0_afbcd_pic_xoffset Display image horizon offset in DDR. When win0_afbcd_output_mask_en is 1, it can be random, or it must be aligned to 16bit.

VOP2_CLUSTER_WIN0_AFBCD_DIS_OFFSET

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win0_afbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win0_afbcd_dis_xoffset Display image horizon offset in panel. it can be random.

VOP2_CLUSTER_WIN0_AFBCD_CTRL

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	win0_afbcd_uv_swap_en win0 afbcd mode uv swap enable
9	RW	0x0	win0_afbcd_rb_swap_en win0 afbcd mode rb swap enable
8	RW	0x0	win0_afbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win0_afbcd_half_block 1'b0: Afbcd full mode, 16 line one tail line 1'b1: Afbcd half mode, 8 line one tail line

Bit	Attr	Reset Value	Description
6:2	RW	0x00	win0_afbcd_pixel_packing_fmt AFBCD data format. 4'h0: RGB565 4'h2: RGBA1010102 4'h3: YUV420_101010 4'h4: RGB888 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: color transform 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	win0_afbcd_video_top_crop video top crop. 2'b00: 0 2'b01: 4 2'b10: 8 others: Reserved

VOP2_CLUSTER_WIN1_CTRL0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	win1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
18	RW	0x0	win1_dither_up_en 1'b0: Disable 1'b1: Enable
17:15	RO	0x0	reserved
14	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
13:12	RO	0x0	reserved
11:10	RW	0x0	win1_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RW	0x0	win1_csc_r2y_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	win1_csc_y2r_en 1'b0: Disable 1'b1: Enable
7	RW	0x0	win1_no_outstanding 1'b0: Disable 1'b1: Enable
6	RW	0x0	win1_hw_pre_mul_en 1'b0: No hardware pre multiply mode 1'b1: Hardware pre multiply mode

Bit	Attr	Reset Value	Description
5:1	RW	0x00	win1_data_fmt 5'b00000: ARGB888 5'b00001: RGB888 5'b00010: RGB565 5'b00011: RGB101010 5'b00100: YCbCr420 5'b00101: YCbCr422 5'b00110: YCbCr444 5'b10000: YCbCr420_101010 5'b10001: YCbCr422_101010 5'b10010: YCbCr444_101010
0	RW	0x0	win1_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER_WIN1_CTRL1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	win1_yrgb_vsd_gt4 If win1 yrgb_act_height/yrgb_dsp_height > 4, win1_yrgb_vsd_gt4 must be enable.
28	RW	0x0	win1_yrgb_vsd_gt2 If win1 yrgb_act_height/yrgb_dsp_height > 2, win1_yrgb_vsd_gt2 must be enable.
27:20	RO	0x00	reserved
19	RW	0x0	win1_yrgb_vsd_mode 1'b0: bilinear2
18	RW	0x0	win1_yrgb_vsu_mode 1'b0: bilinear2
17	RO	0x0	reserved
16	RW	0x0	win1_yrgb_hsd_mode 1'b0: bilinear2
15:14	RW	0x0	win1_yrgb_ver_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
13:12	RW	0x0	win1_yrgb_hor_scl_mode 2'b00: No scale 2'b01: Scale up 2'b10: Scale down 2'b11: No scale
11:4	RO	0x00	reserved
3:2	RW	0x0	win1_bic_coe_sel 2'b00: PRECISE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHELL
1	RO	0x0	reserved
0	RW	0x0	win1_yrgb_axi_gather_en win1 axi bus yrgb data gather transfer enable.

VOP2_CLUSTER_WIN1_CTRL2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:5	RW	0x0	win1_rid_cbr Axi read id of win1 cbr channel
4	RO	0x0	reserved
3:0	RW	0x0	win1_rid_yrgb Axi read id of win1 yrgb channel

VOP2_CLUSTER_WIN1_YRGB_MST

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst Win1 YRGB frame buffer memory start address.

VOP2_CLUSTER_WIN1_VIR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	win1_vir_stride Number of words of win1 yrgb Virtual width. ARGB888: win1_vir_width RGB888: (win1_vir_width*3/4) + (win1_vir_width%3) RGB565: ceil(win1_vir_width/2) YUV: ceil(win1_vir_width/4) YUV tile: ceil(win1_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win1_vir_width/4)

VOP2_CLUSTER_WIN1_ACT_INFO

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_act_height win_act_height = (win1 vertical size -1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	win1_act_width win_act_width = (win1 horizontal size -1).

VOP2_CLUSTER_WIN1_DSP_INFO

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	win1_dsp_height win1_dsp_height = (win1 vertical size -1).
15:12	RO	0x0	reserved
11:0	RW	0x000	win1_dsp_width win1_dsp_width = (win1 horizontal size -1).

VOP2_CLUSTER_WIN1_DSP_ST

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	win1_dsp_yst win1 vertical start point(y) of the display region.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	win1_dsp_xst win1 horizontal start point(x) of the display region.

VOP2_CLUSTER_WIN1_DSP_BG

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	win1_dsp_bg_red win1 layer Background Red color.
19:10	RW	0x000	win1_dsp_bg_green win1 layer Background Green color.
9:0	RW	0x000	win1_dsp_bg_blue win1 layer Background Blue color.

VOP2_CLUSTER_WIN1_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_vs_factor_yrgb factor=((LCDC_win1_ACT_INFO[31:16]) / (LCDC_win1_DSP_INFO[31:16]))*2^12.
15:0	RW	0x0000	win1_hs_factor_yrgb factor=((LCDC_win1_ACT_INFO[15:0]) / (LCDC_win1_DSP_INFO[15:0]))*2^12.

VOP2_CLUSTER_WIN1_SCL_OFFSET

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	win1_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.
15:8	RO	0x00	reserved
7:0	RW	0x00	win1_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99.

VOP2_CLUSTER_WIN1_TRANSFORMED_OFFSET

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	transformed_yoffset The y_offset between the first acitve pixel and the first pixel of column.
15:4	RO	0x000	reserved
3:0	RW	0x0	transformed_xoffset The x_offset between the first acitve pixel and the first pixel of line.

VOP2_CLUSTER_WIN1_AFBCD_OUTPUT_CTRL

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x1	win1_afbcd_gating_en win1 afbcd gating enable
0	RW	0x0	win1_afbcd_output_mask_en 1'b0: AFBCD output must be aligned to 16 width/height 1'b1: AFBCD output can be random integer yuv420 width/height is even, yuv422 width is even.

VOP2_CLUSTER_WIN1_AFBCD_MODE

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	win1_ymir_en 1'b0: Ymirror disable 1'b1: Ymirror when afbcd output
2	RW	0x0	win1_xmir_en 1'b0: Xmirror disable 1'b1: Xmirror when afbcd output
1	RW	0x0	win1_rot270_en 1'b0: Rotation 270 disable 1'b1: Rotation 270 angle, when afbcd output
0	RW	0x0	win1_rot90_en 1'b0: Rotation 90 disable 1'b1: Enable, rotation 90 angle when afbcd output

VOP2_CLUSTER_WIN1_AFBCD_HDR_PTR

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_afbcd_hdr_ptr AFBC encode stream starting address in DDR.

VOP2_CLUSTER_WIN1_AFBCD_VIR_WIDTH

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_afbcd_tail_num Header/payload arbiter tail number.
15:0	RW	0x0000	win1_afbcd_pic_vir_width Number of bytes of AFBCD header virtual width. When afbcd mode is x_mirror/rot90/rot270, it must be aligned to 64 pixels, or it must be aligned to 16pixels.

VOP2_CLUSTER_WIN1_AFBCD_SIZE

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_afbcd_pic_height When win1_afbcd_output_mask_en is 1, it can be random, or it must be aligned to 16bit. Real - 1
15:0	RW	0x0000	win1_afbcd_pic_width When win1_afbcd_output_mask_en is 1, it can be random, or it must be aligned to 16bit. Real - 1

VOP2_CLUSTER_WIN1_AFBCD_PIC_OFFSET

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_afbcd_pic_yoffset Display image vertical offset in DDR. When win1_afbcd_output_mask_en is 1, it can be random,or it must be aligned to 16bit.
15:0	RW	0x0000	win1_afbcd_pic_xoffset Display image horizon offset in DDR. When win1_afbcd_output_mask_en is 1, it can be random,or it must be aligned to 16bit.

VOP2_CLUSTER_WIN1_AFBCD_DIS_OFFSET

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win1_afbcd_dis_yoffset Display image vertical offset in panel. it can be random.
15:0	RW	0x0000	win1_afbcd_dis_xoffset Display image horizon offset in panel. it can be random.

VOP2_CLUSTER_WIN1_AFBCD_CTRL

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	win1_afbcd_uv_swap_en Win1 afbcd mode uv swap enable
9	RW	0x0	win1_afbcd_rb_swap_en Win1 afbcd mode rb swap enable
8	RW	0x0	win1_afbcd_block_split 1'b0: Disable 1'b1: Enable
7	RW	0x0	win1_afbcd_half_block 1'b0: Afbcd full mode, 16 line one tail line 1'b1: Afbcd half mode, 8 line one tail line
6:2	RW	0x00	win1_afbcd_pixel_packing_fmt AFBCD data format. 4'h0: RGB565 4'h2: RGBA1010102 4'h3: YUV420_101010 4'h4: RGB888 4'h5: RGBA8888 4'h9: YUV420_888 4'hb: YUV422_888 4'he: YUV422_101010 Others: Reserved [4]: color transform 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	win1_afbcd_video_top_crop video top crop. 2'b00: 0 2'b01: 4 2'b10: 8 others: reserved

VOP2_CLUSTER_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	cluster_filter_en 1'b0: Disable 1'b1: Enable
7:4	RW	0x0	cluster_lb_mode CLUSTER line buffer mode, calculated by driver. 2'b00: One window,max width is 4096, afbcd is half_block mode 2'b01: Two window, max width is 2048, afbcd is half_block mode 2'b10: One window, max width is 2048, afbcd is full mode
3	RW	0x0	win1_en_status Win1 enable status.
2	RW	0x0	win0_en_status Win0 enable status.
1	RW	0x0	cluster_afbcd_en 1'b0: win0 and win1 afbcd disable 1'b1: win0 and win1 afbcd enable
0	RW	0x0	cluster_en 1'b0: Disable 1'b1: Enable

VOP2_CLUSTER_LG_COE0

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe0 Coefficient of 3x3 matrix.

VOP2_CLUSTER_LG_COE1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe1 Coefficient of 3x3 matrix.

VOP2_CLUSTER_LG_COE2

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_lg_coe2 Coefficient of 3x3 matrix.

VOP2_CLUSTER_HG_COE0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe0 Coefficient of 3x3 matrix.

VOP2_CLUSTER_HG_COE1

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe1 Coefficient of 3x3 matrix.

VOP2_CLUSTER_HG_COE2

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cluster_hg_coe2 Coefficient of 3x3 matrix.

13.4.7 Esmart register description

13.4.7.1 Registers Summary

The base address of esmart0 registers is 0x1800.
The base address of esmart1 registers is 0x1a00.

Name	Offset	Size	Reset Value	Description
VOP2_ESMART_CTRL0	0x0000	W	0x00000000	To enable the color space conversion of esmart.
VOP2_ESMART_CTRL1	0x0004	W	0x0000B0A0	To control the dma of esmart.
VOP2_ESMART_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
VOP2_ESMART_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_ESMART_REGION0_MST_CBCR	0x0018	W	0x00000000	To configure the starting address of CBCR in memory.
VOP2_ESMART_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_ESMART_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data .
VOP2_ESMART_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the display size of data .
VOP2_ESMART_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the display offset of data .
VOP2_ESMART_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
VOP2_ESMART_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x10001000	To configure the scaling factor of YRGB.
VOP2_ESMART_REGION0_SCL_FACTOR_CBCR	0x0038	W	0x10001000	To configure the scaling factor of CBCR.
VOP2_ESMART_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_ESMART_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
VOP2_ESMART_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_ESMART_REGION1_MST_CBCR	0x0048	W	0x00000000	To configure the starting address of CBCR in memory.
VOP2_ESMART_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_ESMART_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data .
VOP2_ESMART_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the display size of data .
VOP2_ESMART_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the display offset of data .
VOP2_ESMART_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.
VOP2_ESMART_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x10001000	To configure the scaling factor of YRGB.

Name	Offset	Size	Reset Value	Description
VOP2_ESMART_REGION1_SCL_FACTOR_CBCR	0x0068	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_ESMART_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
VOP2_ESMART_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_ESMART_REGION2_MST_CBCR	0x0078	W	0x00000000	To configure the starting address of CBCR in memory.
VOP2_ESMART_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_ESMART_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data .
VOP2_ESMART_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the dsiplay size of data .
VOP2_ESMART_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the dsiplay offset of data .
VOP2_ESMART_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
VOP2_ESMART_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x10001000	To configure the scaling factor of YRGB.
VOP2_ESMART_REGION2_SCL_FACTOR_CBCR	0x0098	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_ESMART_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
VOP2_ESMART_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_ESMART_REGION3_MST_CBCR	0x00A8	W	0x00000000	To configure the starting address of CBCR in memory.
VOP2_ESMART_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
VOP2_ESMART_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data .
VOP2_ESMART_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the display size of data .
VOP2_ESMART_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the display offset of data .
VOP2_ESMART_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
VOP2_ESMART_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x10001000	To configure the scaling factor of YRGB.
VOP2_ESMART_REGION3_SCL_FACTOR_CBCR	0x00C8	W	0x10001000	To configure the scaling factor of CBCR
VOP2_ESMART_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
VOP2_ESMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
VOP2_ESMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.

13.4.7.2 Detail Registers Description

VOP2_ESMART_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	esmart_yuv2rgb_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: Axi addr add vstep 1'b1: Axi addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold , dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:20	RW	0x0	esmart_yrgb_gather_num The gather number of YRGB.
19:16	RO	0x0	reserved
15:12	RW	0xb	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:8	RO	0x0	reserved
7:4	RW	0xa	esmart_yrgb_rid AXI read id of esmart yrgb channel.
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RW	0x0	esmart_yrgb_gather_en To enable YRGB gather transfer.
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

VOP2_ESMART_REGION0_MST_CTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region0_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region0_uv_swap Swap U and V component.
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region0_cbcr_gt4 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_gt4 must be enable.
10	RW	0x0	region0_cbcr_gt2 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_gt2 must be enable.
9	RW	0x0	region0_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region0_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B

Bit	Attr	Reset Value	Description
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION0_MST_YRGB

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_ESMART_REGION0_MST_CBCR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART_REGION0_VIR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region0_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART_REGION0_ACT_INFO

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth Esmart0_act_height = Esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width Win_act_width = (win0 horizontal size -1).

VOP2_ESMART_REGION0_DSP_INFO

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height Dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width Dsp_width = horizontal size -1.

VOP2_ESMART_REGION0_DSP_OFFSET

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART_REGION0_SCL_CTRL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region0_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region0_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
15:14	RW	0x0	region0_cbcr_yscl_mode when cbcr_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when cbcr_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region0_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable
12	RW	0x0	region0_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region0_cbcr_xscl_mode when cbcr_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when cbcr_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale

Bit	Attr	Reset Value	Description
9	RW	0x0	region0_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region0_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	region0_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x1000	region0_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION0_SCL_FACTOR_CBCR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region0_cbcr_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region0_cbcr_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION0_SCL_OFFSET

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region0_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region0_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART_REGION1_MST_CTL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region1_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region1_uv_swap Swap U and V component.

Bit	Attr	Reset Value	Description
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region1_cbcr_gt4 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_gt4 must be enable.
10	RW	0x0	region1_cbcr_gt2 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_gt2 must be enable.
9	RW	0x0	region1_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region1_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION1_MST_YRGB

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_ESMART_REGION1_MST_CBCR

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART_REGION1_VIR

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region1_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART_REGION1_ACT_INFO

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth esmart0_act_height = esmart0 vertical size - 1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width win_act_width = (win0 horizontal size - 1).

VOP2_ESMART_REGION1_DSP_INFO

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART_REGION1_DSP_OFFSET

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART_REGION1_SCL_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:18	RW	0x0	region1_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region1_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11 :MITCHEL
15:14	RW	0x0	region1_cbcr_yscl_mode when cbcr_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when cbcr_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region1_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable
12	RW	0x0	region1_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region1_cbcr_xscl_mode when cbcr_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when cbcr_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region1_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region1_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region1_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION1_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	region1_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION1_SCL_FACTOR_CBCR

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region1_cbcr_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region1_cbcr_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION1_SCL_OFFSET

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region1_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region1_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART_REGION2_MST_CTL

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region2_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region2_uv_swap Swap U and V component.
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR

Bit	Attr	Reset Value	Description
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region2_cbcr_gt4 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_gt4 must be enable.
10	RW	0x0	region2_cbcr_gt2 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_gt2 must be enable.
9	RW	0x0	region2_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region2_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION2_MST_YRGB

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region0 YRGB frame buffer memory start address.

VOP2_ESMART_REGION2_MST_CBCR

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART_REGION2_VIR

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region2_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART_REGION2_ACT_INFO

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART_REGION2_DSP_INFO

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART_REGION2_DSP_OFFSET

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART_REGION2_SCL_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:18	RW	0x0	region2_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region2_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11 :MITCHEL
15:14	RW	0x0	region2_cbcr_yscl_mode when cbcr_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when cbcr_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
13	RW	0x0	region2_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable
12	RW	0x0	region2_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region2_cbcr_xscl_mode when cbcr_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when cbcr_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
9	RW	0x0	region2_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region2_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region2_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: Not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: Not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION2_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	region2_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION2_SCL_FACTOR_CBCR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region2_cbcr_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region2_cbcr_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION2_SCL_OFFSET

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region2_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region2_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART_REGION3_MST_CTL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	region3_yuv_clip 1'b0: Disable, YCbCr no clip 1'b1: Enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
16	RW	0x0	region3_uv_swap Swap U and V component.
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR

Bit	Attr	Reset Value	Description
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11	RW	0x0	region3_cbcr_gt4 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 4, esmart_cbcr_gt4 must be enable.
10	RW	0x0	region3_cbcr_gt2 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_gt2 must be enable.
9	RW	0x0	region3_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region3_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h04: YUV420 5'h05: YUV422 5'h06: YUV444 5'h08: YVYU422 5'h09: YVYU420 5'h0a: VYUY422 5'h0b: VYUY420 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64 5'h14: YUV420_10B 5'h15: YUV422_10B 5'h16: YUV444_10B
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION3_MST_YRGB

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_ESMART_REGION3_MST_CBCR

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_cbcr_mst Esmart region0 CBCR frame buffer memory start address

VOP2_ESMART_REGION3_VIR

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_vir_stride_uv Number of words of Mst0 uv Virtual width.
15:0	RW	0x0000	region3_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_ESMART_REGION3_ACT_INFO

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_act_width win_act_width = (win0 horizontal size -1).

VOP2_ESMART_REGION3_DSP_INFO

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height esmart0_dsp_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width dsp_width = horizontal size -1.

VOP2_ESMART_REGION3_DSP_OFFSET

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

VOP2_ESMART_REGION3_SCL_CTRL

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:18	RW	0x0	region3_ysu_bic_mode Vertical bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11: MITCHEL
17:16	RW	0x0	region3_xsu_bic_mode Horizontal bicubic scale up mode. 2'b00: PRECESE 2'b01: SPLINE 2'b10: CATROM 2'b11 :MITCHEL
15:14	RW	0x0	region3_cbcr_yscl_mode when cbcr_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: not ysu_scale when cbcr_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other:not ysd_scale
13	RW	0x0	region3_cbcr_ysd_en Enable CBCR vertical scale down. 1'b0: Disable 1'b1: Enable
12	RW	0x0	region3_cbcr_ysu_en Enable CBCR vertical scale up. 1'b0: Disable 1'b1: Enable
11:10	RW	0x0	region3_cbcr_xscl_mode when cbcr_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: not xsu_scale when cbcr_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: not xsd_scale
9	RW	0x0	region3_cbcr_xsd_en Enable CBCR horizontal scale down. 1'b0: Disable 1'b1: Enable
8	RW	0x0	region3_cbcr_xsu_en Enable CBCR horizontal scale up. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7:6	RW	0x0	region3_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Bicubic other: not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear 2'b10: Average other: not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_ESMART_REGION3_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	region3_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION3_SCL_FACTOR_CBCR

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	region3_cbcr_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16 when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12
15:0	RW	0x1000	region3_cbcr_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_ESMART_REGION3_SCL_OFFSET

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	region3_cbcr_yscl_offset Esmart cbcr vertical scale offset.
23:16	RW	0x00	region3_cbcr_xscl_offset Esmart cbcr horizontal scale offset.
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_ESMART_KEY_CTRL

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

VOP2_ESMART_BG_EN

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

13.4.8 Smart register description

13.4.8.1 Registers Summary

The base address of smart0 registers is 0x1c00.
The base address of smart1 registers is 0x1e00.

Name	Offset	Size	Reset Value	Description
VOP2_SMART_CTRL0	0x0000	W	0x00000000	To enable the color space conversion of esmart.
VOP2_SMART_CTRL1	0x0004	W	0x0000D000	To control the dma of esmart.
VOP2_SMART_REGION0_MST_CTL	0x0010	W	0x00000000	To enable the region0 of esmart.
VOP2_SMART_REGION0_MST_YRGB	0x0014	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_SMART_REGION0_VIR	0x001C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_SMART_REGION0_ACT_INFO	0x0020	W	0x00000000	To configure the active size of data .
VOP2_SMART_REGION0_DSP_INFO	0x0024	W	0x00000000	To configure the display size of data .
VOP2_SMART_REGION0_DSP_OFFSET	0x0028	W	0x00000000	To configure the display offset of data .
VOP2_SMART_REGION0_SCL_CTRL	0x0030	W	0x00000000	To enable the scaling of esmart.
VOP2_SMART_REGION0_SCL_FACTOR_YRGB	0x0034	W	0x00000000	To configure the scaling factor of YRGB.
VOP2_SMART_REGION0_SCL_OFFSET	0x003C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_SMART_REGION1_MST_CTL	0x0040	W	0x00000000	To enable the region1 of esmart.
VOP2_SMART_REGION1_MST_YRGB	0x0044	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_SMART_REGION1_VIR	0x004C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_SMART_REGION1_ACT_INFO	0x0050	W	0x00000000	To configure the active size of data .
VOP2_SMART_REGION1_DSP_INFO	0x0054	W	0x00000000	To configure the display size of data .
VOP2_SMART_REGION1_DSP_OFFSET	0x0058	W	0x00000000	To configure the display offset of data .
VOP2_SMART_REGION1_SCL_CTRL	0x0060	W	0x00000000	To enable the scaling of esmart.

Name	Offset	Size	Reset Value	Description
VOP2_SMART_REGION1_SCL_FACTOR_YRGB	0x0064	W	0x00000000	To configure the scaling factor of YRGB.
VOP2_SMART_REGION1_SCL_OFFSET	0x006C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_SMART_REGION2_MST_CTL	0x0070	W	0x00000000	To enable the region2 of esmart.
VOP2_SMART_REGION2_MST_YRGB	0x0074	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_SMART_REGION2_VIR	0x007C	W	0x00000000	To configure the virtual width of data in memory.
VOP2_SMART_REGION2_ACT_INFO	0x0080	W	0x00000000	To configure the active size of data .
VOP2_SMART_REGION2_DSP_INFO	0x0084	W	0x00000000	To configure the display size of data .
VOP2_SMART_REGION2_DSP_OFFSET	0x0088	W	0x00000000	To configure the display offset of data .
VOP2_SMART_REGION2_SCL_CTRL	0x0090	W	0x00000000	To enable the scaling of esmart.
VOP2_SMART_REGION2_SCL_FACTOR_YRGB	0x0094	W	0x00000000	To configure the scaling factor of YRGB.
VOP2_SMART_REGION2_SCL_OFFSET	0x009C	W	0x00000000	To configure the scaling offset of esmart.
VOP2_SMART_REGION3_MST_CTL	0x00A0	W	0x00000000	To enable the region3 of esmart.
VOP2_SMART_REGION3_MST_YRGB	0x00A4	W	0x00000000	To configure the starting address of YRGB in memory.
VOP2_SMART_REGION3_VIR	0x00AC	W	0x00000000	To configure the virtual width of data in memory.
VOP2_SMART_REGION3_ACT_INFO	0x00B0	W	0x00000000	To configure the active size of data .
VOP2_SMART_REGION3_DSP_INFO	0x00B4	W	0x00000000	To configure the display size of data .
VOP2_SMART_REGION3_DSP_OFFSET	0x00B8	W	0x00000000	To configure the display offset of data .
VOP2_SMART_REGION3_SCL_CTRL	0x00C0	W	0x00000000	To enable the scaling of esmart.
VOP2_SMART_REGION3_SCL_FACTOR_YRGB	0x00C4	W	0x00000000	To configure the scaling factor of YRGB.
VOP2_SMART_REGION3_SCL_OFFSET	0x00CC	W	0x00000000	To configure the scaling offset of esmart.
VOP2_SMART_KEY_CTRL	0x00D0	W	0x00000000	To configure the color key of esmart.
VOP2_SMART_BG_EN	0x00D4	W	0x00000000	To enable the background of esmart.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.8.2 Detail Registers Description

VOP2_SMART_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	esmart_8bpp_lut_en To enable 8bpp LUT.
3:2	RW	0x0	esmart_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	esmart_rgb2yuv_en 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

VOP2_SMART_CTRL1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_ymir_en 1'b0: Axi addr add vstep 1'b1: Axi addr sub vstep
30:29	RW	0x0	esmart_dma_rreq_thold Esmart dma hurry read request thold. If esmart empty lb number >= esmart_dma_rreq_thold , dma_rreq_hurry is asserted.
28	RW	0x0	esmart_dma_rreq_hurry_en Enable esmart dma hurry read request. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	esmart_cbcr_gather_num The gather number of CBCR.
23:16	RO	0x00	reserved
15:12	RW	0xd	esmart_cbcr_rid AXI read id of esmart cbcr channel.
11:4	RO	0x00	reserved
3	RW	0x0	esmart_cbcr_gather_en To enable CBCR gather transfer.
2	RO	0x0	reserved
1:0	RW	0x0	esmart_esmart_axi_rlen 2'b00: Burst16 (burst 15 in rgb888 pack mode) 2'b01: Burst8 (burst 12 in rgb888 pack mode) 2'b10: Burst4 (burst 6 in rgb888 pack mode) 2'b11: Reserved

VOP2_SMART_REGION0_MST_CTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	region0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region0_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region0_alpha_swap 1'b0: ARGB 1'b1: RGBA

Bit	Attr	Reset Value	Description
12	RW	0x0	region0_dither_up_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	region0_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region0_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region0_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64
0	RW	0x0	region0_mst_en 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION0_MST_YRGB

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region0_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_SMART_REGION0_VIR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	region0_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_SMART_REGION0_ACT_INFO

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_act_width win_act_width = (win0 horizontal size -1).

VOP2_SMART_REGION0_DSP_INFO

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_width dsp_width = horizontal size -1.

VOP2_SMART_REGION0_DSP_OFFSET

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region0_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region0_dsp_xoff Display image horizon offset in panel.

VOP2_SMART_REGION0_SCL_CTRL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	region0_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysd_scale
5	RW	0x0	region0_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region0_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region0_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsd_scale
1	RW	0x0	region0_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	region0_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region0_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x0000	region0_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_SMART_REGION0_SCL_OFFSET

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region0_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region0_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_SMART_REGION1_MST_CTL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	region1_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region1_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region1_dither_up_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	region1_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.

Bit	Attr	Reset Value	Description
8	RW	0x0	region1_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved
5:1	RW	0x00	region1_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64
0	RW	0x0	region1_mst_en 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION1_MST_YRGB

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region1_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_SMART_REGION1_VIR

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	region1_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_SMART_REGION1_ACT_INFO

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_act_width win_act_width = (win0 horizontal size -1).

VOP2_SMART_REGION1_DSP_INFO

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	region1_dsp_width dsp_width = horizontal size -1.

VOP2_SMART_REGION1_DSP_OFFSET

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region1_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region1_dsp_xoff Display image horizon offset in panel.

VOP2_SMART_REGION1_SCL_CTRL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	region1_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysd_scale
5	RW	0x0	region1_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region1_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region1_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsd_scale
1	RW	0x0	region1_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region1_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION1_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region1_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x0000	region1_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_SMART_REGION1_SCL_OFFSET

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region1_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region1_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_SMART_REGION2_MST_CTL

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	region2_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region2_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region2_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region2_dither_up_en 1'b0: Disable 1'b1: Enable
11	RO	0x0	reserved
10	RW	0x0	region2_cbcr_gt2 If esmart_cbcr_ysd_enc, bilinear is enable and cbcr_act_height/cbcr_dsp_height > 2, esmart_cbcr_gt2 must be enable.
9	RO	0x0	reserved
8	RW	0x0	region2_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region2_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64
0	RW	0x0	region2_mst_en 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION2_MST_YRGB

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region2_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_SMART_REGION2_VIR

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	region2_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_SMART_REGION2_ACT_INFO

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_act_width win_act_width = (win0 horizontal size -1).

VOP2_SMART_REGION2_DSP_INFO

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_height dsp_height = vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_width dsp_width = horizontal size -1.

VOP2_SMART_REGION2_DSP_OFFSET

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region2_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region2_dsp_xoff Display image horizon offset in panel.

VOP2_SMART_REGION2_SCL_CTRL

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	region2_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysd_scale
5	RW	0x0	region2_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region2_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region2_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsd_scale
1	RW	0x0	region2_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region2_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION2_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region2_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x0000	region2_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_SMART_REGION2_SCL_OFFSET

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region2_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region2_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_SMART_REGION3_MST_CTL

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	region3_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
14	RW	0x0	region3_rb_swap 1'b0: RGB 1'b1: BGR
13	RW	0x0	region3_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	region3_dither_up_en 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	region3_yrgb_gt4 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 4, esmart_yrgb_gt4 must be enable.
8	RW	0x0	region3_yrgb_gt2 If esmart_yrgb_ysd_enc, bilinear is enable and yrgb_act_height/yrgb_dsp_height > 2, esmart_yrgb_gt2 must be enable.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:1	RW	0x00	region3_data_fmt 5'h00: ARGB8888 5'h01: RGB888 5'h02: RGB565 5'h10: BPP08 5'h11: BPP26 5'h12: BPP44 5'h13: BPP64
0	RW	0x0	region3_mst_en 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION3_MST_YRGB

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	region3_yrgb_mst Esmart region0 YRGB frame buffer memory start address .

VOP2_SMART_REGION3_VIR

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	region3_vir_stride Number of words of Mst0 yrgb Virtual width. ARGB888: win0_vir_width RGB888: (win0_vir_width*3/4) + (win0_vir_width%3) RGB565: ceil(win0_vir_width/2) YUV: ceil(win0_vir_width/4) YUV tile: ceil(win0_vir_width/4) YUYV,YVYU,UYVY,VYUY: ceil(win0_vir_width/4)

VOP2_SMART_REGION3_ACT_INFO

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_act_heigth esmart0_act_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_act_width win_act_width = (win0 horizontal size -1).

VOP2_SMART_REGION3_DSP_INFO

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_height esmart0_dsp_height = esmart0 vertical size -1.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_width dsp_width = horizontal size -1.

VOP2_SMART_REGION3_DSP_OFFSET

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	region3_dsp_yoff Display image vertical offset in panel.
15:13	RO	0x0	reserved
12:0	RW	0x0000	region3_dsp_xoff Display image horizon offset in panel.

VOP2_SMART_REGION3_SCL_CTRL

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	region3_yrgb_yscl_mode when yrgb_ysu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysu_scale when yrgb_ysd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not ysd_scale
5	RW	0x0	region3_yrgb_ysd_en Enable YRGB vertical scale down. 1'b0: Disable 1'b1: Enable
4	RW	0x0	region3_yrgb_ysu_en Enable YRGB vertical scale up. 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	region3_yrgb_xscl_mode when yrgb_xsu_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsu_scale when yrgb_xsd_en is enable. 2'b00: Best-neigh 2'b01: Bilinear other: not xsd_scale
1	RW	0x0	region3_yrgb_xsd_en Enable YRGB horizontal scale down. 1'b0: Disable 1'b1: Enable
0	RW	0x0	region3_yrgb_xsu_en Enable YRGB horizontal scale up. 1'b0: Disable 1'b1: Enable

VOP2_SMART_REGION3_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	region3_yrgb_yfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.
15:0	RW	0x0000	region3_yrgb_xfactor when yrgb_xsu: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^16. when yrgb_xsd: factor=((LCDC_WIN0_ACT_INFO[15:0]) / (LCDC_WIN0_DSP_INFO[15:0]))*2^12.

VOP2_SMART_REGION3_SCL_OFFSET

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	region3_yrgb_yscl_offset Esmart yrgb vertical scale offset.
7:0	RW	0x00	region3_yrgb_xscl_offset Esmart yrgb horizontal scale offset.

VOP2_SMART_KEY_CTRL

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_key_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_key_value Esmart RED color key.
19:10	RW	0x000	esmart_g_key_value Esmart GREEN color key.
9:0	RW	0x000	esmart_b_key_value Esmart Blue color key.

VOP2_SMART_BG_EN

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31	RW	0x0	esmart_bg_en 1'b0: Disable 1'b1: Enable
30	RO	0x0	reserved
29:20	RW	0x000	esmart_r_value Esmart Background Red color.
19:10	RW	0x000	esmart_g_value Esmart Background Green color.
9:0	RW	0x000	esmart_b_value Esmart Background Blue color.

13.4.9 HDR10 register description

13.4.9.1 Registers Summary

The base address of HDR10 registers is 0x2000.

Name	Offset	Size	Reset Value	Description
VOP2_HDR10_LUT_CTRL	0x0000	W	0x00000000	To control the fetching of HDR10 LUT.
VOP2_HDR10_LUT_MST	0x0004	W	0x00000000	To control the fetching of HDR10 LUT.
VOP2_SDR2HDR_CTRL	0x0010	W	0x00000000	To enable the SDR2HDR of HDR10.
VOP2_HDR2SDR_CTRL	0x0020	W	0x00000000	To enable the HDR2SDR of HDR10.
VOP2_HDR2SDR_SRC_RANGE	0x0024	W	0x00000000	To configure the source luminance of HDR10.
VOP2_HDR2SDR_NORFACEETF	0x0028	W	0x00000000	To configure the normalized factor of EETF.
VOP2_HDR2SDR_DST_RANGE	0x002C	W	0x00000000	To configure the destination luminance of HDR10.
VOP2_HDR2SDR_NORMFACCGAMMA	0x0030	W	0x00000000	To configure the normalized factor of GAMMA.
VOP2_EETF_OETF0	0x003C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF1	0x0040	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF2	0x0044	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF3	0x0048	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF4	0x004C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF5	0x0050	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF6	0x0054	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF7	0x0058	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF8	0x005C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF9	0x0060	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF10	0x0064	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF11	0x0068	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF12	0x006C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF13	0x0070	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF14	0x0074	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF15	0x0078	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF16	0x007C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_EETF_OETF17	0x0080	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF18	0x0084	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF19	0x0088	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF20	0x008C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF21	0x0090	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF22	0x0094	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF23	0x0098	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF24	0x009C	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF25	0x00A0	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF26	0x00A4	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF27	0x00A8	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF28	0x00AC	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF29	0x00B0	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF30	0x00B4	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF31	0x00B8	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_EETF_OETF32	0x00BC	W	0x00000000	To configure the Y value of BT1886_OETF and EETF curve.
VOP2_SAT_Y0	0x00C0	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y1	0x00C4	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y2	0x00C8	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y3	0x00CC	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y4	0x00D0	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y5	0x00D4	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y6	0x00D8	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y7	0x00DC	W	0x00000000	To configure the Y value of square root curve.
VOP2_SAT_Y8	0x00E0	W	0x00000000	To configure the Y value of square root curve.
VOP2_EOTF_OETF_Y0	0x00F0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_EOTF_OETF_Y1	0x00F4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y2	0x00F8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y3	0x00FC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y4	0x0100	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y5	0x0104	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y6	0x0108	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y7	0x010C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y8	0x0110	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y9	0x0114	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y10	0x0118	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y11	0x011C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y12	0x0120	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y13	0x0124	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y14	0x0128	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y15	0x012C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y16	0x0130	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y17	0x0134	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y18	0x0138	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_EOTF_OETF_Y19	0x013C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y20	0x0140	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y21	0x0144	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y22	0x0148	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y23	0x014C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y24	0x0150	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y25	0x0154	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y26	0x0158	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y27	0x015C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y28	0x0160	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y29	0x0164	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y30	0x0168	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y31	0x016C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y32	0x0170	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y33	0x0174	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y34	0x0178	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y35	0x017C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y36	0x0180	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_EOTF_OETF_Y37	0x0184	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y38	0x0188	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y39	0x018C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y40	0x0190	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y41	0x0194	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y42	0x0198	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y43	0x019C	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y44	0x01A0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y45	0x01A4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y46	0x01A8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y47	0x01AC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y48	0x01B0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y49	0x01B4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y50	0x01B8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y51	0x01BC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y52	0x01C0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y53	0x01C4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y54	0x01C8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_EOTF_OETF_Y55	0x01CC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y56	0x01D0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y57	0x01D4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y58	0x01D8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y59	0x01DC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y60	0x01E0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y61	0x01E4	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y62	0x01E8	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y63	0x01EC	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_EOTF_OETF_Y64	0x01F0	W	0x00000000	To configure the Y value of BT1886_EOTF and ST2048_OETF curve.
VOP2_OETF_DX_DXPOW1	0x0200	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW2	0x0204	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW3	0x0208	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW4	0x020C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW5	0x0210	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW6	0x0214	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW7	0x0218	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW8	0x021C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW9	0x0220	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW10	0x0224	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW11	0x0228	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW12	0x022C	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_OETF_DX_DXPOW13	0x0230	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW14	0x0234	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW15	0x0238	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW16	0x023C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW17	0x0240	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW18	0x0244	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW19	0x0248	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW20	0x024C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW21	0x0250	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW22	0x0254	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW23	0x0258	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW24	0x025C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW25	0x0260	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW26	0x0264	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW27	0x0268	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW28	0x026C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW29	0x0270	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW30	0x0274	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW31	0x0278	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW32	0x027C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW33	0x0280	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW34	0x0284	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW35	0x0288	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW36	0x028C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW37	0x0290	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW38	0x0294	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_OETF_DX_DXPOW39	0x0298	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW40	0x029C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW41	0x02A0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW42	0x02A4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW43	0x02A8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW44	0x02AC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW45	0x02B0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW46	0x02B4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW47	0x02B8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW48	0x02BC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW49	0x02C0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW50	0x02C4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW51	0x02C8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW52	0x02CC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW53	0x02D0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW54	0x02D4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW55	0x02D8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW56	0x02DC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW57	0x02E0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW58	0x02E4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW59	0x02E8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW60	0x02EC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW61	0x02F0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW62	0x02F4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW63	0x02F8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_DX_DXPOW64	0x02FC	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_OETF_XN1	0x0300	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN2	0x0304	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN3	0x0308	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN4	0x030C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN5	0x0310	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN6	0x0314	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN7	0x0318	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN8	0x031C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN9	0x0320	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN10	0x0324	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN11	0x0328	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN12	0x032C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN13	0x0330	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN14	0x0334	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN15	0x0338	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN16	0x033C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN17	0x0340	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN18	0x0344	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN19	0x0348	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN20	0x034C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN21	0x0350	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN22	0x0354	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN23	0x0358	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN24	0x035C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN25	0x0360	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN26	0x0364	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_OETF_XN27	0x0368	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN28	0x036C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN29	0x0370	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN30	0x0374	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN31	0x0378	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN32	0x037C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN33	0x0380	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN34	0x0384	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN35	0x0388	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN36	0x038C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN37	0x0390	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN38	0x0394	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN39	0x0398	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN40	0x039C	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN41	0x03A0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN42	0x03A4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN43	0x03A8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN44	0x03AC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN45	0x03B0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN46	0x03B4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN47	0x03B8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN48	0x03BC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN49	0x03C0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN50	0x03C4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN51	0x03C8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN52	0x03CC	W	0x00000000	To configure the X value of ST2048_OETF curve.

Name	Offset	Size	Reset Value	Description
VOP2_OETF_XN53	0x03D0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN54	0x03D4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN55	0x03D8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN56	0x03DC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN57	0x03E0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN58	0x03E4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN59	0x03E8	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN60	0x03EC	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN61	0x03F0	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN62	0x03F4	W	0x00000000	To configure the X value of ST2048_OETF curve.
VOP2_OETF_XN63	0x03F8	W	0x00000000	To configure the X value of ST2048_OETF curve.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.9.2 Detail Registers Description

VOP2_HDR10_LUT_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	hdr10_lut_mode Configure HDR10 register mode. 1'b0: AXI 1'b1: AHB
0	RW	0x0	hdr10_lut_update_en Update HDR10 configure. 1'b0: disable 1'b1: enable

VOP2_HDR10_LUT_MST

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hdr10_lut_mst HDR10 configure's start address in memory.

VOP2_SDR2HDR_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sdr2hdr_gating_en Enable SDR2HDR auto-gating. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
8	RW	0x0	sdr2hdr_bypass_en Bypass SDR2HDR function. 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3	RW	0x0	sdr2hdr_oetf_en Enable OETF curve. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sdr2hdr_r2r_mode Select R2R mode. 1'b0: RGB709TORGB2020 1'b1: RGB2020TORGB709
1	RW	0x0	sdr2hdr_r2r_en Enable R2R convert. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sdr2hdr_eotf_en Enable EOTF curve. 1'b0: Disable 1'b1: Enable

VOP2_HDR2SDR_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x00000000	reserved
9	RW	0x0	hdr2sdr_gating_en 1'b0: Disable 1'b1: Enable
8	RW	0x0	hdr2sdr_bypass_en 1'b0: Disable 1'b1: Enable
7:1	RO	0x0	reserved
0	RW	0x0	hdr2sdr_en 1'b0: Disable 1'b1: Enable

VOP2_HDR2SDR_SRC_RANGE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	src_max Source max luminance.
15:14	RO	0x0	reserved
13:0	RW	0x0000	src_min Source min luminance.

VOP2_HDR2SDR_NORFACEETF

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x000	normfaceetf Normalization eetf factor.

VOP2_HDR2SDR_DST_RANGE

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dst_max Destination max luminance.
15:0	RW	0x0000	dst_min Destination min luminance.

VOP2_HDR2SDR_NORMFACCGAMMA

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	normfaccgamma Normalization gamma factor.

VOP2_EETF_OETF0

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF1

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF3

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF4

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF5

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF6

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF7

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF8

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF9

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF10

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF11

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF12

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF13

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF14

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF15

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF16

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF17

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF18

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF19

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF20

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF21

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF22

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF23

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF24

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF25

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF26

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF27

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF28

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF29

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF30

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF31

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_EETF_OETF32

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	bt1886oetf_y bt1886oetf y.
15:14	RO	0x0	reserved
13:0	RW	0x0000	eetf_y eetf y.

VOP2_SAT_Y0

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y1

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y2

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y3

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y4

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y5

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y6

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y7

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_SAT_Y8

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sat_y sat y.

VOP2_EOTF_OETF_Y0

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y1

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y2

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y3

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y4

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y5

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y6

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y7

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y8

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y9

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y10

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y11

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y12

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y13

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y14

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y15

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y16

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y17

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y18

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y19

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y20

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y21

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y22

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y23

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y24

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y25

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y26

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y27

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y28

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y29

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y30

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.

Bit	Attr	Reset Value	Description
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y31

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y32

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y33

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y34

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y35

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y36

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y37

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y38

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y39

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y40

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y41

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y42

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y43

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y44

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y45

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y46

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y47

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y48

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y49

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y50

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y51

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y52

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y53

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y54

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y55

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y56

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y57

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y58

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y59

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y60

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y61

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y62

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y63

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_EOTF_OETF_Y64

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	st2084oetf_y st20840etf y.

Bit	Attr	Reset Value	Description
17:0	RW	0x00000	bt1886eotf_y bt1886eotf y.

VOP2_OETF_DX_DXPOW1

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW2

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW3

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW4

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW5

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW6

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW7

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW8

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW9

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW10

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW11

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW12

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW13

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW14

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW15

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW16

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW17

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW18

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW19

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW20

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW21

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW22

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW23

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW24

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW25

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW26

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW27

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW28

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW29

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW30

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW31

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW32

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW33

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW34

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW35

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW36

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW37

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW38

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW39

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW40

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW41

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW42

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW43

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW44

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW45

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW46

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW47

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW48

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW49

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW50

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW51

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW52

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW53

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW54

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW55

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW56

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW57

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW58

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW59

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW60

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW61

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW62

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW63

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_DX_DXPOW64

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	oetf_dxpow st2084oetf dx power.
15:0	RW	0x0000	oetf_dx st2084oetf dx.

VOP2_OETF_XN1

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN2

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN3

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN4

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN5

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN6

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN7

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN8

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN9

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN10

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN11

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN12

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN13

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN14

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN15

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN16

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN17

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN18

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN19

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN20

Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN21

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN22

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN23

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN24

Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN25

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN26

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN27

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN28

Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN29

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN30

Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN31

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN32

Address: Operational Base + offset (0x037C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN33

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN34

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN35

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN36

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN37

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN38

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN39

Address: Operational Base + offset (0x0398)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN40

Address: Operational Base + offset (0x039C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN41

Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN42

Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN43

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN44

Address: Operational Base + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN45

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN46

Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN47

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN48

Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN49

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN50

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN51

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN52

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN53

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN54

Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN55

Address: Operational Base + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN56

Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN57

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN58

Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN59

Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN60

Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN61

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN62

Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

VOP2_OETF_XN63

Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	eotf_xn st2084 x.

13.4.10 MMU register description

13.4.10.1 Registers Summary

The base address of MMU0 registers is 0x3e00.

The base address of MMU1 registers is 0x3f00.

Name	Offset	Size	Reset Value	Description
VOP2_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address.
VOP2_MMU_STATUS	0x0004	W	0x00000000	MMU status register.
VOP2_MMU_COMMAND	0x0008	W	0x00000000	MMU command register.

Name	Offset	Size	Reset Value	Description
VOP2_MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault.
VOP2_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register.
VOP2_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register.
VOP2_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register.
VOP2_MMU_INT_MASK	0x001C	W	0x00000000	MMU interrupt mask register.
VOP2_MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register.
VOP2_MMU_AUTO_GATING	0x0024	W	0x00000000	MMU auto gating.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access*

13.4.10.2 Detail Registers Description

VOP2_MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dte_addr Current page table address.

VOP2_MMU_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	page_fault_bus_id Index of master responsible for last page fault.
5	RW	0x0	page_fault_is_write The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RW	0x0	replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RW	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	paging_en Paging is enabled. 1'b0: Disable 1'b1: Enable

VOP2_MMU_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd This can be: 3'd0: MMU_ENABLE_PAGING 3'd1: MMU_DISABLE_PAGING 3'd2: MMU_ENABLE_STALL 3'd3: MMU_DISABLE_STALL 3'd4: MMU_ZAP_CACHE 3'd5: MMU_PAGE_FAULT_DONE 3'd6: MMU_FORCE_RESET Others: Reserved

VOP2_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	page_fault_addr Address of last page fault.

VOP2_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

VOP2_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rawst_bus_error Raw interrupt status of read bus error.
0	RW	0x0	rawst_page_fault Raw interrupt status of page fault.

VOP2_MMU_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	clr_bus_error Clear interrupt of bus error.
0	RW	0x0	clr_page_fault Clear interrupt of page fault.

VOP2_MMU_INT_MASK

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mask_bus_error Mask interrupt of bus error.
0	RW	0x0	mask_page_fault Mask interrupt of page fault.

VOP2_MMU_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	st_bus_error Interrupt status of bus error.
0	RW	0x0	st_page_fault Interrupt status of page fault.

VOP2_MMU_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	mmu_cfg_mode 1'b0: Regdone when frame start 1'b1: Regdone immediately
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

13.4.11 LUT address summary

The base address of GAMMA LUT is 0x4000, it's size is 0x1000. The base address of BPP LUT is 0x5000, it's size is 0x0400.

13.5 Application Note

13.5.1 Cluster application note

1. The vir_width and vir_height of the afbcd image is a multiple of 16.
2. If rotation_90 or rotation_270 is enable, afbcd_full_mode must be enable and lb_mode must be 2. Rotation_90 and rotation_270 can't be enable at the same time.
3. The height of the rotated image must be less than 2048.
4. If the afbcd image width is greater than 2048, half mode must be 1 and lb_mode must be 0.
5. If cluster is used to display two pictures, lb_mode and afbcd_half_block must be 1 and the picture width can't be greater than 2048.
6. The active width of the afbcd image must be a multiple of 4.
7. The scale factor must be less than 4. Otherwise, there is not enough AXI bandwidth to cause some display error.
8. The active width must be a multiple of 4.

13.5.2 Smart application note

1. The active width and display width of the image is a multiple of 2.
2. If YUYV420 is enable, the scale mode can't be 2.
3. If YUV-10 is enable, the active width of the image must be a multiple of 4.
4. The maximum gather number of smart is 4.

13.5.3 HDR10 application note

1. Only one HDR10 image is supported. If hdr2sdr is enable, hdr10_path_en must be 1.
2. If the display panel is HDR and the image is SDR, sdr2hdr and sdr2sdr_path_en must be enable.
3. The delay between the input and the output of HDR2SDR is 37. The delay between the input and the output of SDR2HDR is 10.

13.5.4 CABC application note

1. Post-process1 is support CABC. If CABC is enable, the post_lb_mode must be 1 and the display with is less than 1024.

13.5.5 Interlace application note

1. If interlace is enable, p2i_en must be enable.
2. If the resolution of the display panel is 480i or 576i, dsp_core_dclk_sel must be enable.

13.5.6 Write back application note

1. The maximum resolution of the wrote back image is 1920x1080. If the wrote back image resolution is greater than 1080p, scale down must be enable.
2. The wb_fifo_thold must be greater than the amount of data in row.

13.5.7 The delay number of overlay application note

The delay number used in different application scenarios is shown as below.

Tcases	Win	Delay number	Max delay number
SDR Input and SDR output	CLUSTERx	0	42
	SMARTx	20	
	Vp0_bg	42	
	Vp1_bg	40	
	Vp2_bg	40	
HDR input and SDR output	CLUSTER0(HDR10)	0	69
	CLUSTER1(SDR)	27	
	SMARTx(SDR)	47	
	Vp0_bg	69	
HDR input and SDR output	CLUSTERx(SDR)	27	69
	SMART0(HDR)	20	
	SMARTx(SDR)	47	
	Vp0_bg	69	
SDR input and HDR output	CLUSTERx	0	53
	ESMATx	20	
	Vp0_bg	53	
HDR input and HDR output	CLUSTER0(HDR10)	21	53
	CLUSTER1(SDR)	0	
	SMARTx(SDR)	20	
	Vp0_bg	53	
HDR input and HDR output	CLUSTERx(SDR)	0	53
	SMART0(HDR)	41	
	SMARTx(SDR)	20	
	Vp0_bg	53	

13.5.8 HDR10 application note

If HDR10 is enable, overlay_mode must be RGB.

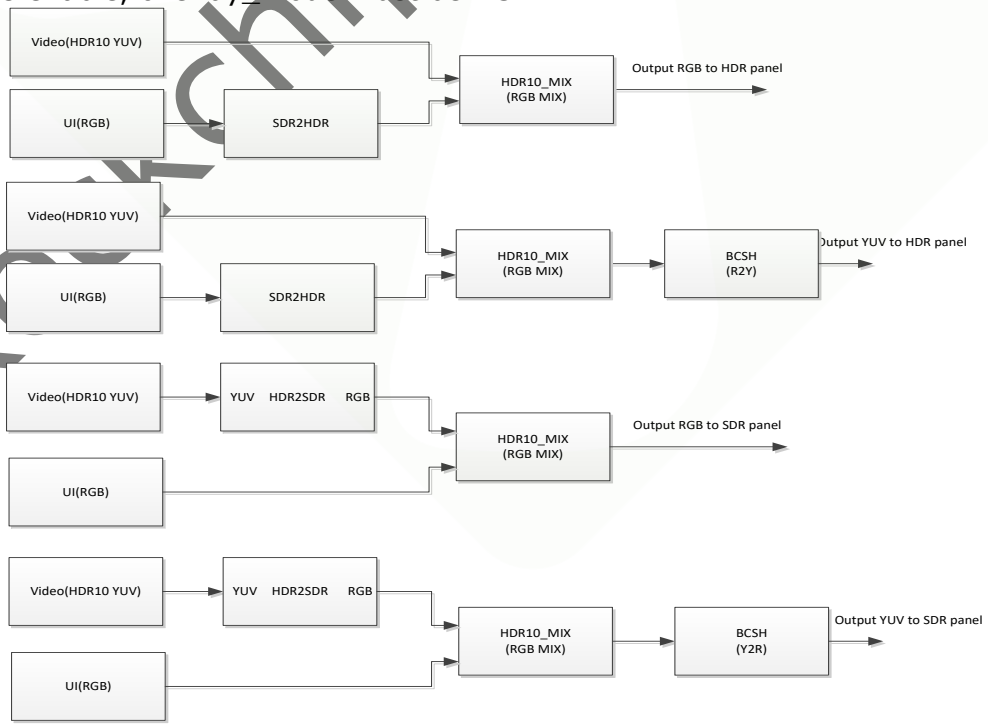


Fig.13-5 HDR10 application

Chapter 14 Raster Graphic Acceleration (RGA2)

14.1 Overview

RGA2 is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending.

14.2 Features

- **Data format**
  - Input data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YVYU422/YVYU420/YUV422SP10bit/YUV420SP10bit
  - Output data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551
    - YUV420/YUV422/YUV400/Y4/YVYU422/YVYU420
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio，from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT:
  - A+B=B only BitBLT, A support rotate&scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- **Others**
  - Support NN quantize (CLIP((source + offset) * scale) for RGB channel)
  - Floyd–Steinberg dither (RGB888 or 565 TO Y4 ; RGB888 or 565 DITHER TO Y4)
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

Constrain：

(1) YUV420/422-8bit virtual stride need 8byte align，xoff/yoff need 2byte algin；
(2) YUV420/422-10bit virtual stride need 16byte align，not support xoff/yoff；
(3) Vertical scale down or not && Horizontal bi-cubic scale up src0 width<=2048；
Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928；
(4) Vertical scale down or not && Horizontal bilinear scale up src0 width<=4096；
Vertical scale up && Horizontal bilinear scale up src0 width<=3856；

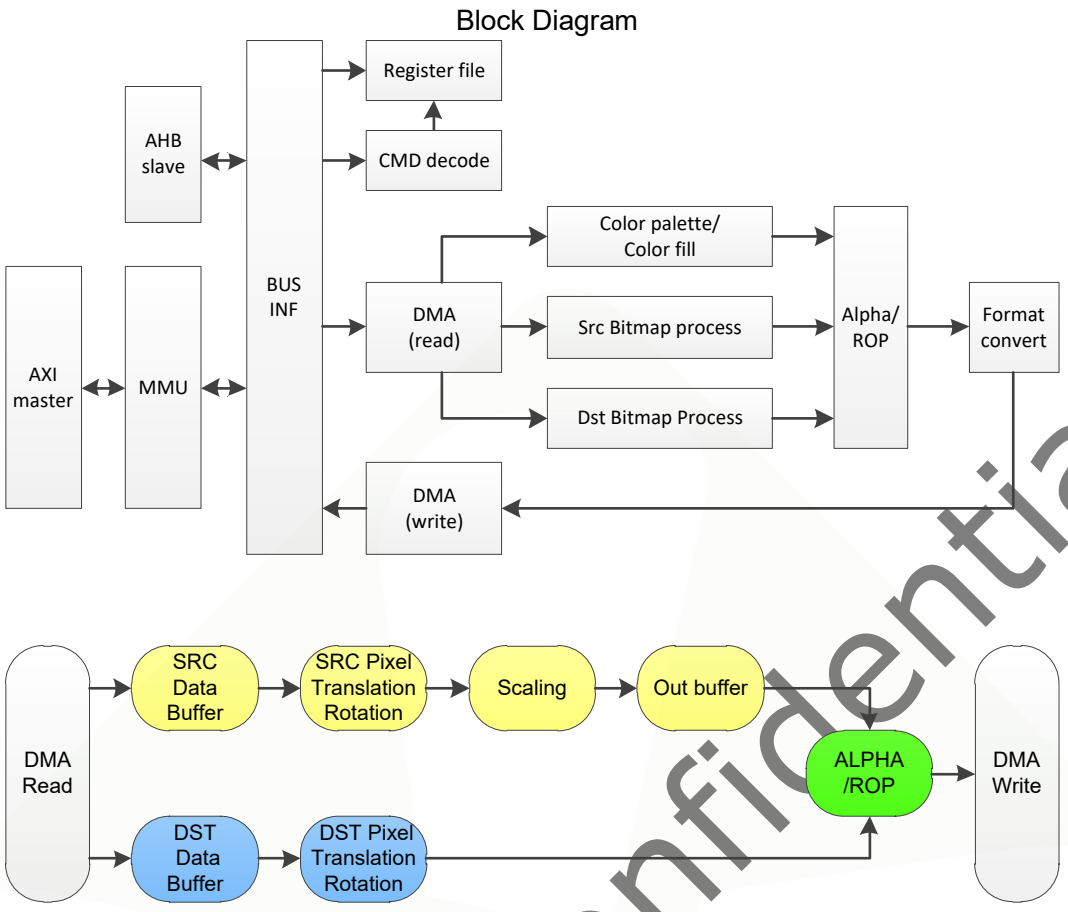


Fig. 14-1 RGA2 Block Diagram

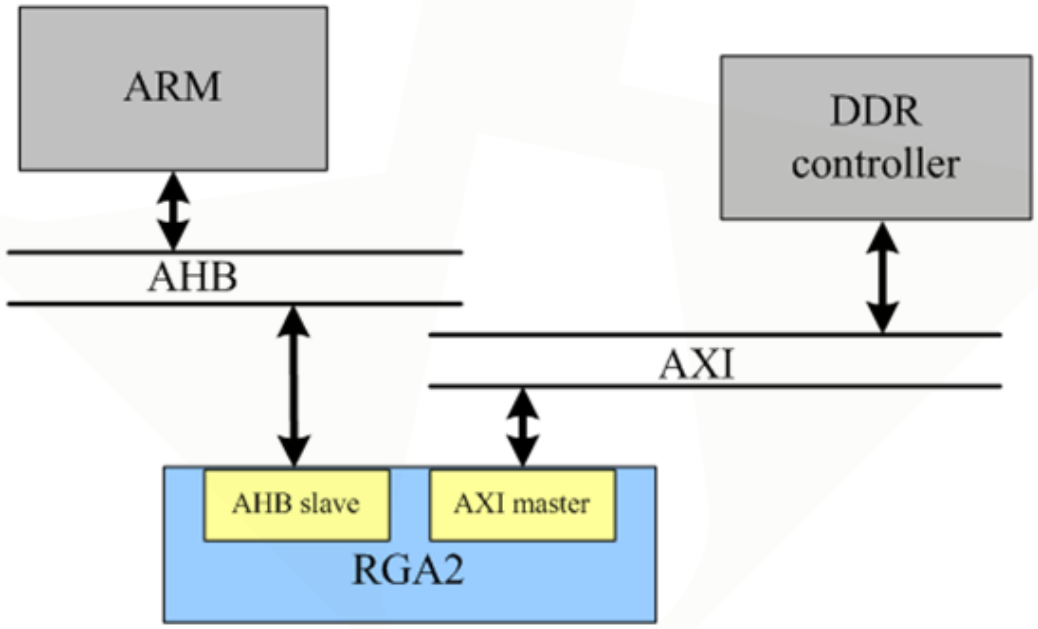


Fig. 14-2 RGA2 in SOC

14.3 Function Description

14.3.1 Data Format

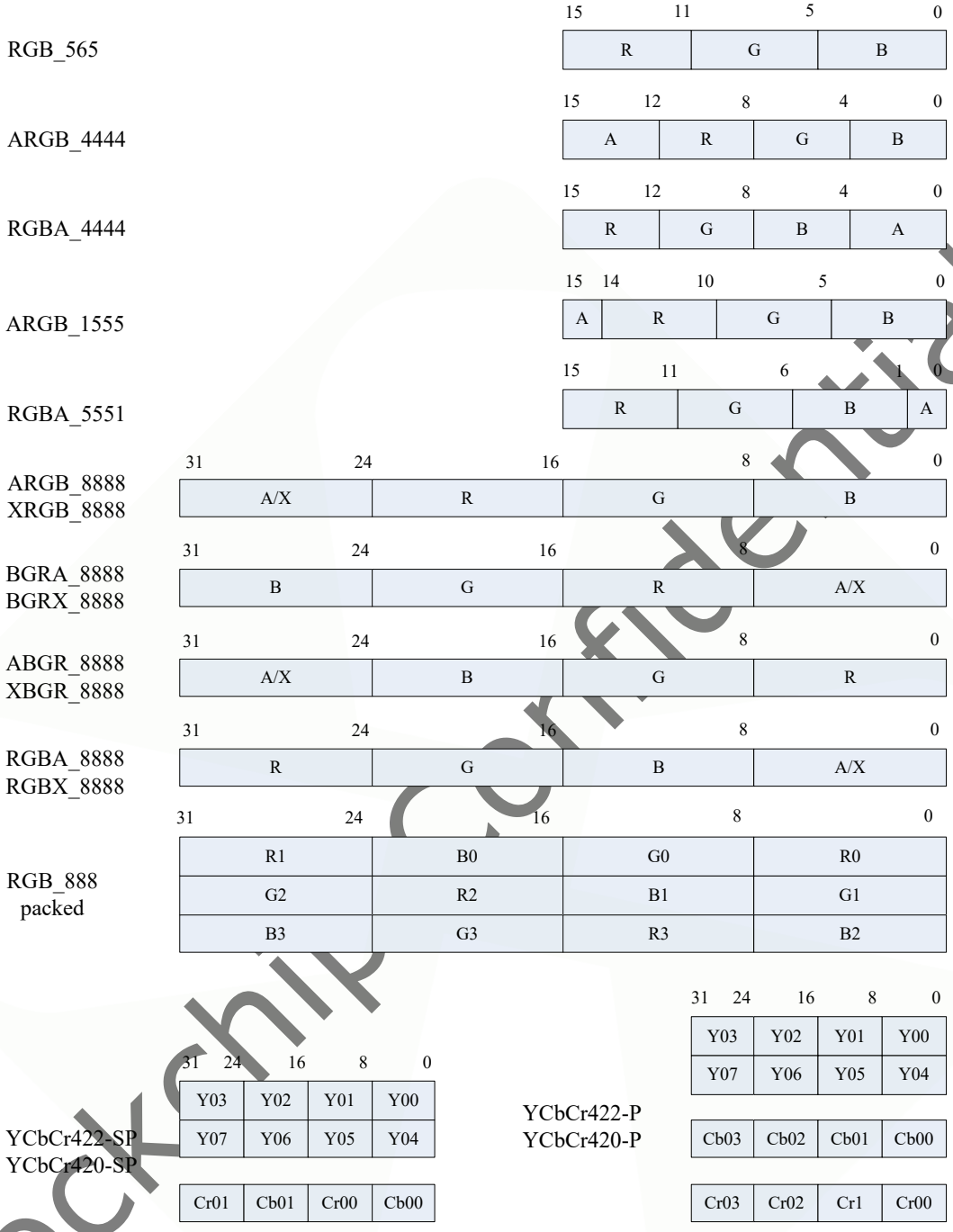


Fig. 14-3 RGA Input Data Format

All input data (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

14.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

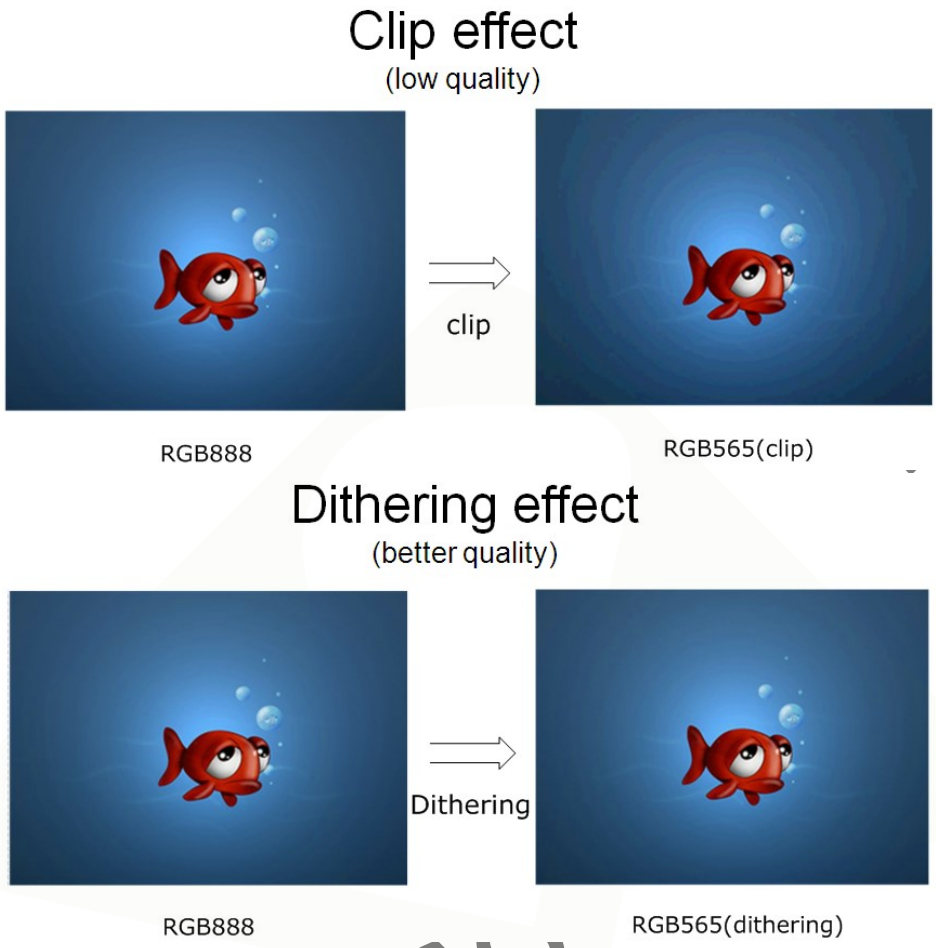
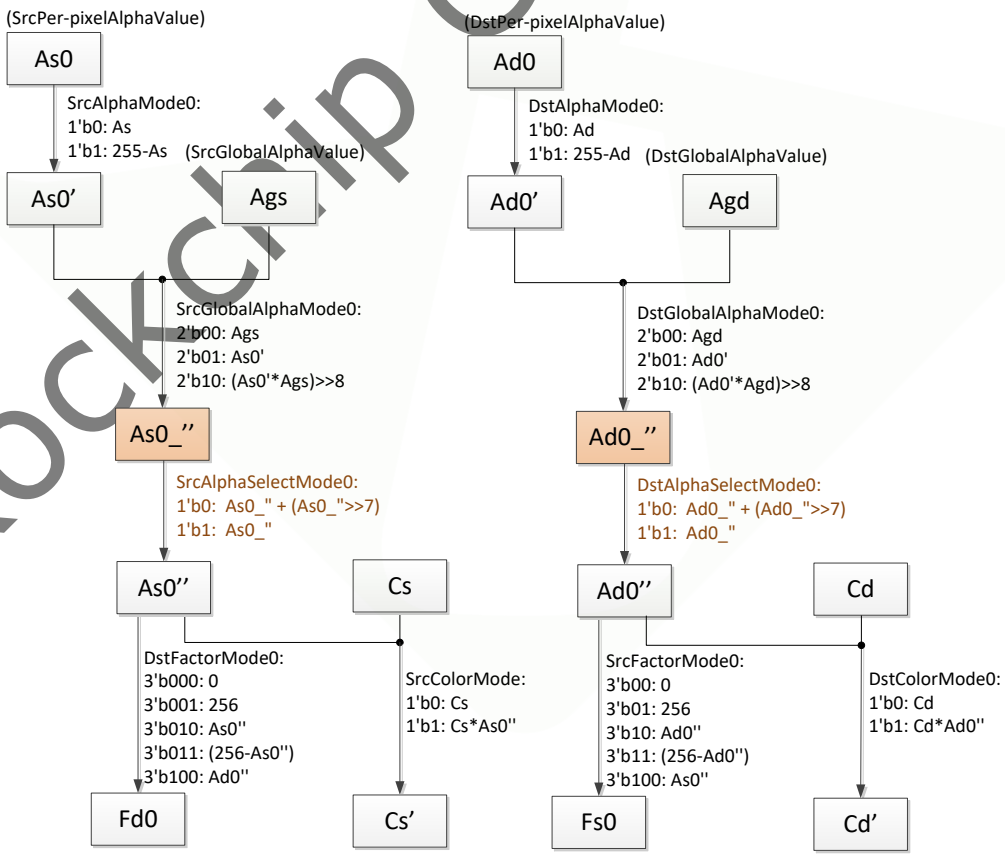


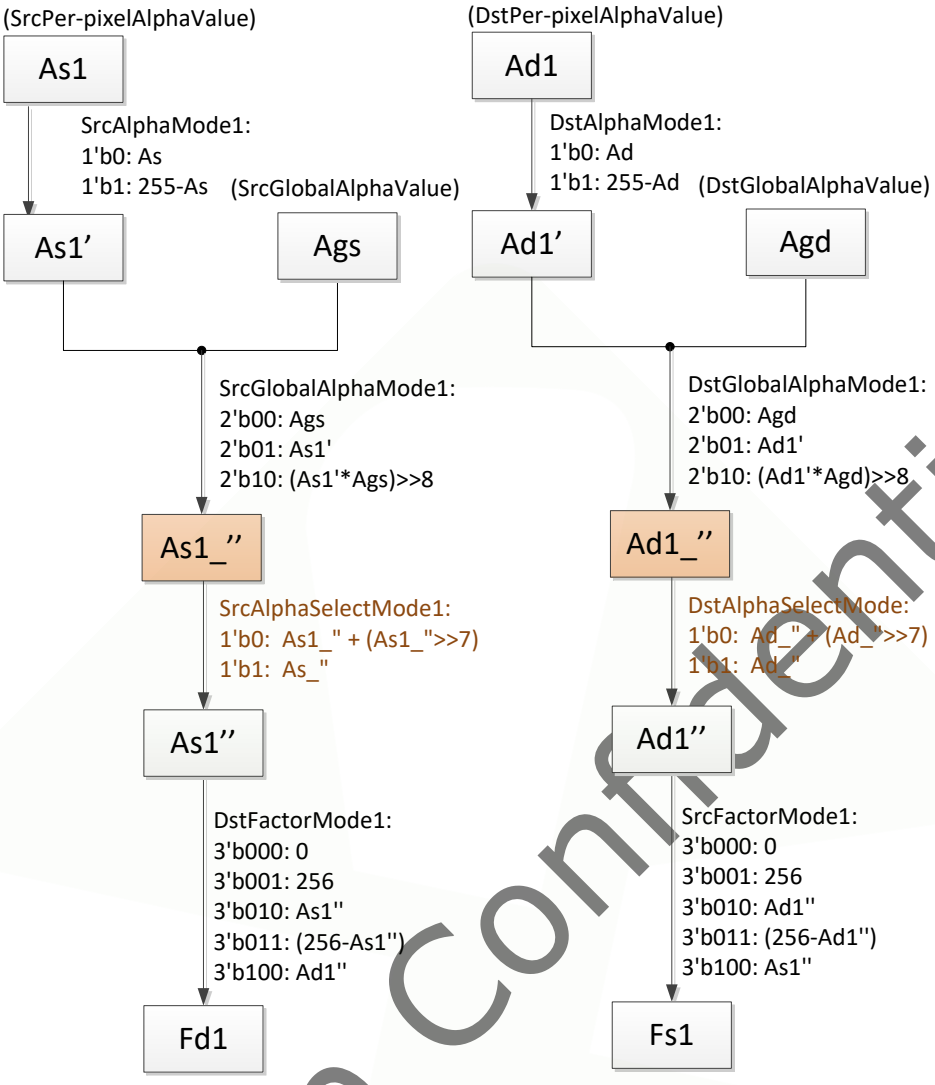
Fig. 14-4 RGA Dither effect

14.3.3 Alpha mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 14-5 alpha mode configure description

14.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

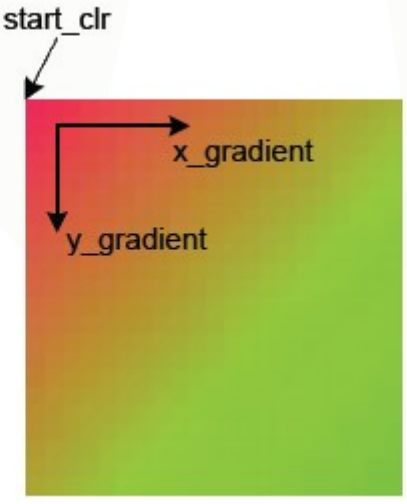


Fig. 14-6 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different

coordinary.
A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;
A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

14.3.5 Scaling

The scaling operation is the imageresizing processing of source image. Scaling is done base on ARGB8888 format.
There are three sampling modes: scale down (Average); scale up(Bi-cubic).

14.3.6 NN quantize

The NN quantize is for NN pre_process using. The function is CLIP((source + offset) * scale) for R G B channel. When use this function, the signal sw_dst_nn_quantize_en and reg NN_QUANTIZE_SCALE, NN_QUANTIZE_OFFSET need be configured.

14.3.7 Y4 output format and Floyd–Steinberg dither

The Y4 output format and Floyd–Steinberg dither is used for Eink panel. RGA supports RGB888 or 565 to Y4 directly. In this mode, signal sw_dst_fmt_y4_en needs set to 1. There is a 16 segments LUT could be used in Y4 output mode (reg is RGA2_DST_Y4MAP_LUT0 and RGA2_DST_Y4MAP_LUT1).

RGA also supports RGB888 or 565 dither to Y4. In this mode, the signals sw_dst_fmt_y4_en, sw_dither_down, sw_dither_mode need be configured.
note: If sw_dither_mode is set Y8 to Y1 mode, the output format is still Y4 format.

14.4 Register description

14.4.1 Register Summary

Slave address can be divided into different length for different usage, which is shown as follows.

Name	Offset	Size	Reset Value	Description
RGA2_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA2_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_CMD_BASE	0x0008	W	0x00000000	RGA command codes base address register
RGA2_STATUS1	0x000C	W	0x00000000	RGA status register
RGA2_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_MMU_CMD_BASE	0x0018	W	0x00000000	Register0000 Description
RGA2_STATUS2	0x001C	W	0x00000000	RGA status register
RGA2_WORK_CNT	0x0020	W	0x00000000	RGA work counter
RGA2_VERSION_INFO	0x0028	W	0x03256726	RTL version and FPGA version information
RGA2_PERF_LATENCY_CTRL0	0x0040	W	0x00000024	Axi performance latency module control register0
RGA2_PERF_LATENCY_CTRL1	0x0044	W	0x00000021	Axi performance latency module control register1
RGA2_PERF_RD_MAX_LATENCY_NUM0	0x0048	W	0x00000000	Read max latency number
RGA2_PERF_RD_LATENCY_SAMP_NUM	0x004C	W	0x00000000	The number of bigger than configured threshold value
RGA2_PERF_RD_LATENCY_ACC_SUM	0x0050	W	0x00000000	Total sample number
RGA2_PERF_RD_AXI_TOTAL_BYTE	0x0054	W	0x00000000	perf_rd_axi_total_byte
RGA2_PERF_WR_AXI_TOTAL_BYTE	0x0058	W	0x00000000	perf_wr_axi_total_byte
RGA2_PERF_WORKING_CNT	0x005C	W	0x00000000	perf_working_cnt
RGA2_DST_CSC_00	0x0060	W	0x000000bc	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_01	0x0064	W	0x00000274	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_02	0x0068	W	0x00000040	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF0	0x006C	W	0x00004200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_10	0x0070	W	0x00000798	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_11	0x0074	W	0x000006a4	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_12	0x0078	W	0x000001c0	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF1	0x007C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_20	0x0080	W	0x000001c0	sw_dst_csc_mode[2]=1'b1 used csc factor

Name	Offset	Size	Reset Value	Description
RGA2_DST_CSC_21	0x0084	W	0x00000668	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_22	0x0088	W	0x000007d8	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_DST_CSC_OFF2	0x008C	W	0x00020200	sw_dst_csc_mode[2]=1'b1 used csc factor
RGA2_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_SRC_BASE0	0x0108	W	0x00000000	RGA source image Y/RGB base address register
RGA2_SRC_BASE1	0x010C	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register
RGA2_SRC_ACT_INFO	0x011C	W	0x00000000	RGA source image active width/height register
RGA2_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_SRC_FG_COLOR	0x012C	W	0x00000000	RGA source image foreground color
RGA2_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_CP_GR_A	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_SRC_TR_COLOR1	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_CP_GR_B	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_DST_BASE0	0x013C	W	0x00000000	RGA destination image base address 0 register
RGA2_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_DST_ACT_INFO	0x014C	W	0x00000000	RGA destination image active width/height register
RGA2_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Description
RGA2_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_PAT_CON	0x015C	W	0x00000000	Pattern size/offset register
RGA2_ROP_CON0	0x0160	W	0x76543210	ROP code 0 control register

Name	Offset	Size	Reset Value	Description
RGA2_CP_GR_G	0x0160	W	0x76543210	RGA color gradient fill step register (color fill mode)
RGA2_DST_Y4MAP_LUT0	0x0160	W	0x76543210	Y4MAP LUT REGS from lut0 to lut7
RGA2_NN_QUANTIZE_SCALE	0x0160	W	0x36543210	Quantize scale of RGB (2bit integer+8bit fraction, 0~3.99)
RGA2_NN_QUANTIZE_OFFSET	0x0164	W	0x00000000	Quantize offset of RGB (1bit signed + 8bit integer)
RGA2_CP_GR_R	0x0164	W	0xfedcba98	RGA color gradient fill step register (color fill mode)
RGA2_DST_Y4MAP_LUT1	0x0164	W	0xfedcba98	Y4MAP LUT REGS from lut8 to lut15
RGA2_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_MMU_CTRL1	0x016C	W	0x00000000	RGA MMU control register 1
RGA2_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_MMU_ELS_BASE	0x017C	W	0x00000000	RGA ELSE MMU TLB base address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access **DW**-Double WORD (64 bits) access*

14.4.2 Detail Register Description

RGA2_SYS_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	sw_rst_handsave_p It would save protect-rstn into initial status if long time dead in protect-rstn status(auto clear into '0').
6	RW	0x1	sw_rst_protect_e Protect-rstn mode enable. It would be ensure all axi write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst It would auto-resetn after one frame finish. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 1'b0: Disable 1'b1: Enable
1	WO	0x0	sw_cmd_mode RGA command mode 1'b0: Slave mode 1'b1: Master mode
0	W1C	0x0	sw_cmd_op_st_p Only used in passive (slave) control mode

RGA2_CMD_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total command number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total command number would reset to RGA_INCR_CMD_NUM.

RGA2_CMD_BASE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cmd_base RGA command codes base address

RGA2_STATUS1

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 1'b0: Idle 1'b1: Working

RGA2_INT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

RGA2_MMU_CTRL0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved
10:9	RW	0x0	sw_els_ch_priority The priority of this channnel
8:7	RW	0x0	sw_dst_ch_priority The priority of this channnel
6:5	RW	0x0	sw_src1_ch_priority The priority of this channnel
4:3	RW	0x0	sw_src_ch_priority The priority of this channnel
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 1'b0: 4KB page 1'b1: 64KB page

RGA2_MMU_CMD_BASE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_STATUS2

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	Reserved
12:11	RO	0x0	rpp_mkram_rready Rpp mkram rready
10:6	RO	0x00	dstrpp_outbuf_rready Dstrpp outbuf rready
5:2	RO	0x0	srcrpp_outbuf_rready Srcrpp outbuf rready
1	RO	0x0	bus_error Bus error status
0	RO	0x0	rpp_error RPP error status

RGA2_WORK_CNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

RGA2_VERSION_INFO

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x03	major Used for IP structure version infomation
23:20	RW	0x2	minor Big feature change under same structure
19:0	RW	0x56726	svnbuild Rtl current svn number

RGA2_PERF_LATENCY_CTRL0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x2	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type
2	RW	0x1	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enalbe
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

RGA2_PERF_LATENCY_CTRL1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id
7:4	RW	0x2	sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type

RGA2_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 Read max latency value of channel 0

RGA2_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 Read latency thr number channel 0

RGA2_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

RGA2_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte

RGA2_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte

RGA2_PERF_WORKING_CNT

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt

RGA2_DST_CSC_00

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x0bc	sw_dst_coe_00 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_01

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x274	sw_dst_coe_01 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_02

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x040	sw_dst_coe_02 1bit signed+8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_OFF0

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x04200	sw_dst_coe_off0 1bit signed+8.8bit factor Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0

RGA2_DST_CSC_10

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x798	sw_dst_coe_10 1bit signed+8bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_11

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x6a4	sw_dst_coe_11 1bit signed+8bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_12

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x1c0	sw_dst_coe_12 1bit signed+8bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_OFF1

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x20200	sw_dst_coe_off1 1bit signed+8.8bit factor U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1

RGA2_DST_CSC_20

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x1c0	sw_dst_coe_20 1bit signed+8bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_21

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x668	sw_dst_coe_21 1bit signed+8bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_22

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x7d8	sw_dst_coe_22 1bit signed+8bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_DST_CSC_OFF2

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x20200	sw_dst_coe_off2 1bit signed+8.8bit factor V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2

RGA2_MODE_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 1'b0:Clip 1'b1:Not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key. 1'b0: Disable 1'b1: Enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 1'b0: Solid color 1'b1: Pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 1'b0: SRC + DST => DST 1'b1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 3'b000: Bitblt 3'b001: Color palette 3'b010: Rectangle fill 3'b011: Update palette LUT/pattern ram

RGA2_SRC_INFO

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src_yuv10_round_e This bit valid when RGA2E/2L support yuv 10bit picture input 1'b0: Yuv 10bit to 8bit round disable 1'b1: Yuv 10bit to 8bit round enable
27	RW	0x0	sw_src_yuv10_e This bit valid when RGA2E/2L support yuv 10bit picture input. 1'b0: Yuv 10bit disable 1'b1: Yuv 10bit enalbe
26	RW	0x0	sw_vsp_mode 1'b0:By-cubic 1'b1:Bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC bicubic scaling coefficient select 2'b00: CATROM 2'b01: MITCHELL 2'b10: HERMITE 2'b11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 1'b0: Disable 1'b1: Enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 1'b0: Normal stencil test (color key) 1'b1: Inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 2'b00：No scaling 2'b01: Down-scaling 2'b10: Up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 2'b00：No scaling 2'b01: Down-scaling 2'b10: Up-scaling

13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 2'b00: No mirror 2'b01: X mirror 2'b10: Y mirror 2'b11: X mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 2'b00: 0 degree 2'b01: 90 degree 2'b10: 180 degree 2'b11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 2'b00: Bypass 2'b01: BT.601-range0(limit range) 2'b10: BT.601-range1(full range) 2'b11: BT.709-range0(limit range)
7	RW	0x0	sw_cp_endian Source Color palette endian swap 1'b0: Big endian 1'b1: Little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 1'b0: CrCb 1'b1: CbCr For YVYU422 mode, UV swap 1'b0: YVYU422(U LSB) 1'b1: YUYV422(V LSB)
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 1'b0: BGR 1'b1: RGB For YVYU422 mode, YC swap 1'b0: YVYU422(U LSB) 1'b1: VYUY422(Y LSB)

3:0	RW	0x0	sw_src_fmt Source bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 4'b0111: YVYU422(U LSB) 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P 4'b1100: 1BPP (color palette) 4'b1101: 2BPP (color palette) 4'b1110: 4BPP (color palette) 4'b1111: 8BPP (color palette)

RGA2_SRC_BASE0

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 Source image Y/RGB base address

RGA2_SRC_BASE1

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 Source image Cb base address (YUV422/420-P) Source image Cb/Cr base address (YU,V422/420-SP)

RGA2_SRC_BASE2

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base2 Source image Cr base address (YUV422/420-P)

RGA2_SRC_BASE3

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base3 Source image 1 RGB base address(source bitblt mode1)

RGA2_SRC_VIR_INFO

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride Mask image virtual stride (words)
15	RW	0x0	Reserved Reserved
14:0	RW	0x0000	sw_src_vir_stride Src image virtual stride (words)

RGA2_SRC_ACT_INFO

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:16	RW	0x0000	sw_src_act_height Source image active height
15:13	RW	0x0	Reserved1 Reserved
12:0	RW	0x0000	sw_src_act_width Source image active width

RGA2_SRC_X_FACTOR

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =((SRC_ACT_WIDTH-1)/(DST_ACT_WIDTH-1)) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(DST_ACT_WIDTH/(SRC_ACT_WIDTH) * 65536 + 1

RGA2_SRC_Y_FACTOR

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor =((SRC_ACT_ HEIGHT -1)/(DST_ACT_ HEIGHT -1)) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor =(DST_ACT_ HEIGHT /(SRC_ACT_ HEIGHT) * 65536 + 1

RGA2_SRC_BG_COLOR

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_SRC_FG_COLOR

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_SRC_TR_COLOR0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin Source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin Source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin Source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin Source image transparency color R min value

RGA2_CP_GR_A

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_SRC_TR_COLOR1

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax Source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax Source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax Source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax Source image transparency color R max value

RGA2_CP_GR_B

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_DST_INFO

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	sw_dst_nn_quantize_en Destination output RGB quantize calculate 1'b0: Quantize calculate disable 1'b1: Quantize calculate enable
25	RW	0x0	sw_dst_fmt_y4_en Destination output Y channel 4bit and UV 0bit 1'b0: Y4 out disable 1'b1: Y4 out enable
24	RW	0x0	sw_dst_fmt_yuv400_en Destination Cb-Cr ouput disable (valid for YUV420/2 P/SP format) 1'b0: CbCr output normal 1'b1: CbCr output disable
23	RO	0x0	reserved
22	RW	0x0	sw_src1_csc_clip Src1 read BGR2YUV Clip mode(RGB from 0~255 clip to 36~235) 1'b0: Unclip 1'b1: Clip enable
21:20	RW	0x0	sw_src1_csc_mode SRC1 read bitmap RGB2YUV conversion mode 2'b00: Bypass 2'b01: BT.601-range0,BT601_l, Y00,255, UV00,255 2'b10: BT.601-range1,BT601_f, Y16,235, UV19,237 2'b11: BT.709-range0,BT709_l, Y16,255, UV16,237
19	RW	0x0	sw_dst_csc_mode_2 sw_dst_csc_mode[2]+sw_dst_csc_mode[1:0]; DST read bitmap CSC(r2y/y2y) conversion mode under sw_dst_csc_mode[2]=1'b0: 3'b10x: Y: sw_dst_coe_00*R + sw_dst_coe_01*G + sw_dst_coe_02*B + sw_dst_coe_off0 U: sw_dst_coe_10*R + sw_dst_coe_11*G + sw_dst_coe_12*B + sw_dst_coe_off1 V: sw_dst_coe_20*R + sw_dst_coe_21*G + sw_dst_coe_22*B + sw_dst_coe_off2 without clip 3'b110: Defulat BT.709-range1,BT601_f,Y16,235,UV16,240 clip 3'b111: Defulat BT.709-range1,BT601_f,Y16,235,UV16,237 clip
18	RW	0x0	sw_dst_csc_clip Dst write RGB2YUV Clip mode(RGB from 0~255 clip to 16~235) 1'b1: Clip enable 1'b0: Unclip

17:16	RW	0x0	sw_dst_csc_mode_01 sw_dst_csc_mode[1:0] under sw_dst_csc_mode[2]=1'b0: DST read bitmap RGB2YUV conversion mode 3'b000: Bypass 3'b001: BT.601-range0,BT601_l,Y00,255,UV00,255 3'b010: BT.601-range1,BT601_f,Y16,235,UV19,237 3'b011: BT.709-range0,BT709_l,Y16,255,UV16,237
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 2'b00: 888 to 666 2'b01: 888 to 565 2'b10: 888 to 555 2'b11: 888 to 444 DST YUV dither down bit mode 2'b00: Y8 to Y4 others:Y8 to Y1
13	RW	0x0	sw_dither_down DST dither down enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 1'b0: BGR 1'b1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 3'b000: ABGR888 3'b001: XBGR888 3'b010: BGR packed 3'b100: RGB565 3'b101: ARGB1555 3'b110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 1'b0: CrCb 1'b1: CbCr

5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 1'b0: ABGR 1'b1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 1'b0: BGR 1'b1: RGB
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 4'b0000: ABGR888 4'b0001: XBGR888 4'b0010: BGR packed 4'b0100: RGB565 4'b0101: ARGB1555 4'b0110: ARGB4444 when sw_dst_fmt_yuv400_en=1, YUV420/2 P/SP format will change to YUV400: 4'b1000: YUV422SP 4'b1001: YUV422P 4'b1010: YUV420SP 4'b1011: YUV420P only RGA2E has yuyv output format feature: 4'b1100: YVYU422(U, LSB) 4'b1101: YVYU420(U, LSB) 4'b1110: VYUY422(Y, LSB) 4'b1111: VYUY420(Y, LSB)

RGA2_DST_BASE0

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 Destination image Y/RGB base address

RGA2_DST_BASE1

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 Destination image Cb/CbCr base address

RGA2_DST_BASE2

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 Destination image Cr base address

RGA2_DST_VIR_INFO

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_src1_vir_stride Source image 1 virtual stride (words)
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_vir_stride Destination image virtual stride(words)

RGA2_DST_ACT_INFO

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_ALPHA_CTRL0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 1'b0: Big endian 1'b1: Little endian
19:12	RW	0x00	sw_dst_global_alpha Global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha Global alpha value of SRC(Ags) Fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 2'b00: ROP 2 2'b01: ROP 3 2'b10: ROP 4
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 1'b0: Alpha 1'b1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 1'b0: Disable 1'b1: Enable

RGA2_ALPHA_CTRL1

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 1'b0: As 1'b1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 1'b0: Ad 1'b1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1_'') 2'b00: Ags 2'b01: As1' 2'b10: (As1'*Ags)>>8 2'b11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1_'') 2'b00: Agd 2'b01: Ad1' 2'b10: (Ad1'*Agd)>>8 2'b11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1'') 1'b0: As1''= As1_''+ (As1_''>>7) 1'b1: As1''= As1 _''
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1'') 1'b0: Ad1''= Ad1_'' + (Ad1_''>>7) 1'b1: Ad1''= Ad1_''
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 3'b000: 0 3'b001: 256 3'b010: Ad1'' 3'b011: 256-Ad1'' 3'b100: As1''
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 3'b000: 0 3'b001: 256 3'b010: As1'' 3'b011: 256-As1'' 3'b100: Ad1''

15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0') 1'b0: As 1'b1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0') 1'b0: Ad 1'b1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_'') 2'b00: Ags 2'b01: As0' 2'b10: (As0'*Ags)>>8 2'b11: Reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_'') 2'b00: Agd 2'b01: Ad0' 2'b10: (Ad0'*Agd)>>8 2'b11: Reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0'') 1'b0: As0''= As0_''+ (As0_''>>7) 1'b1: As0''= As0 _''
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0'') 1'b0: Ad0''= Ad0_'' + (Ad0_''>>7) 1'b1: Ad0''= Ad0_''
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 3'b000: 0 3'b001: 256 3'b010: Ad0'' 3'b011: 256-Ad0'' 3'b100: As0''
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 3'b000: 0 3'b001: 256 3'b010: As0'' 3'b011: 256-As0'' 3'b100: Ad0''
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 1'b0: Cs 1'b1: Cs * As0''

0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 1'b0: Cd 1'b1: Cd * Ad0''

RGA2_FADING_CTRL

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_PAT_CON

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_ROP_CON0

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:25	RW	0x3b	Reserved Reserved
24:0	RW	0x0543210	sw_rop3_code0 Rop3 code 0 control bits

RGA2_CP_GR_G

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x7654	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x3210	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_DST_Y4MAP_LUT0

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x76543210	sw_dst_y4map_lut0 Y4 lut from lut0 to lut7

RGA2_NN_QUANTIZE_SCALE

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x365	sw_nn_quantize_scale_b Quantize scale of Blue (2bit integer+8bit fraction, 0--3.99)
19:10	RW	0x10c	sw_nn_quantize_scale_g Quantize scale of Green (2bit integer+8bit fraction, 0--3.99)
9:0	RW	0x210	sw_nn_quantize_scale_r Quantize scale of Red (2bit integer+8bit fraction, 0--3.99)

RGA2_NN_QUANTIZE_OFFSET

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_nn_quantize_offset_b Quantize offset of Blue(1bit signed + 8bit integer)
19	RO	0x0	reserved
18:10	RW	0x000	sw_nn_quantize_offset_g Quantize offset of Green (1bit signed + 8bit integer)
9	RO	0x0	reserved
8:0	RW	0x000	sw_nn_quantize_offset_r Quantize offset of Red(1bit signed + 8bit integer)

RGA2_CP_GR_R

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0xfedc	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0xba98	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_DST_Y4MAP_LUT1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0xfedcba98	sw_dst_y4map_lut1 Y4 lut from lut8 to lut15

RGA2_ROP_CON1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:25	RW	0x7f	Reserved Reserved
24:0	RW	0x0dcba98	sw_rop3_code1 Rop3 code 1 control bits

RGA2_MASK_BASE

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base Mask base address in ROP4 mode LUT/ pattern load base address

RGA2_MMU_CTRL1

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	sw_dst_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
10	RW	0x0	sw_dst_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
6	RW	0x0	sw_src1_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	sw_src_mmu_prefetch_dir 1'b0: Forward 1'b1: Backward
2	RW	0x0	sw_src_mmu_prefetch_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush Set 1 to this bit to flush MMU TLB, auto clear.

0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 1'b0: Disable 1'b1: Enable

RGA2_MMU_SRC_BASE

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

RGA2_MMU_SRC1_BASE

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

RGA2_MMU_DST_BASE

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

RGA2_MMU_ELS_BASE

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

14.5 Application Notes

14.5.1 Register Partition

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

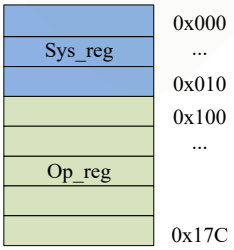


Fig. 14-7 RGA software main register-region

14.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to '1'. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing '1' to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write '1' to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1).

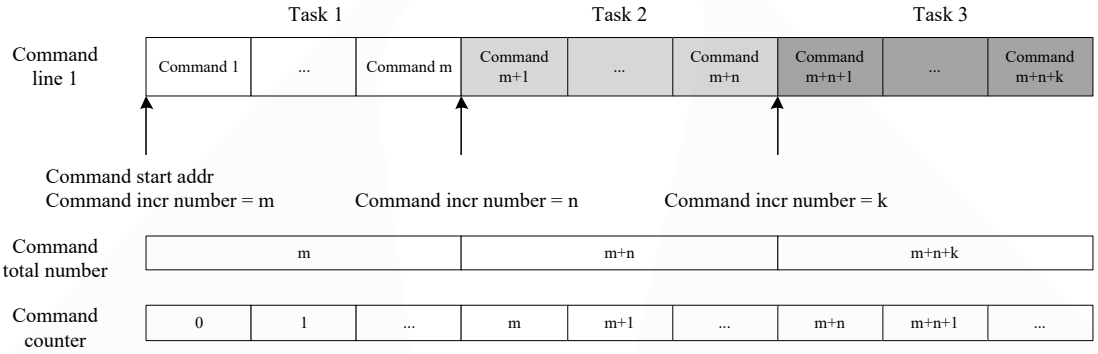


Fig. 14-8 RGA command line and command counter

14.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the current_cmd_int (sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

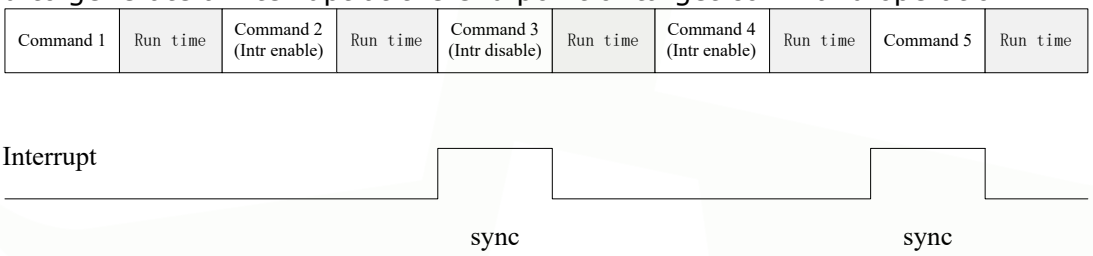


Fig. 14-9 RGA command sync generation

14.5.4 ColorPalette Application Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL.
2. ColorPalette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update.

14.5.5 Some special application constraint

1. The algorithm of vertical scale up: must select bicubic algorithm when source picture is smaller or equal to 2k and must select bilinear when bigger than 2k.
2. The effects that The output's definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as:2048x32→2008x64).
3. At the scenario A+B->C, the size among the A B C has some constraints:

A's size must be equal to C. C's size must equal to B when A+C is no rotation. C's rotation (90degree)size must equal to B1 when A+C is rotation 90 degree.

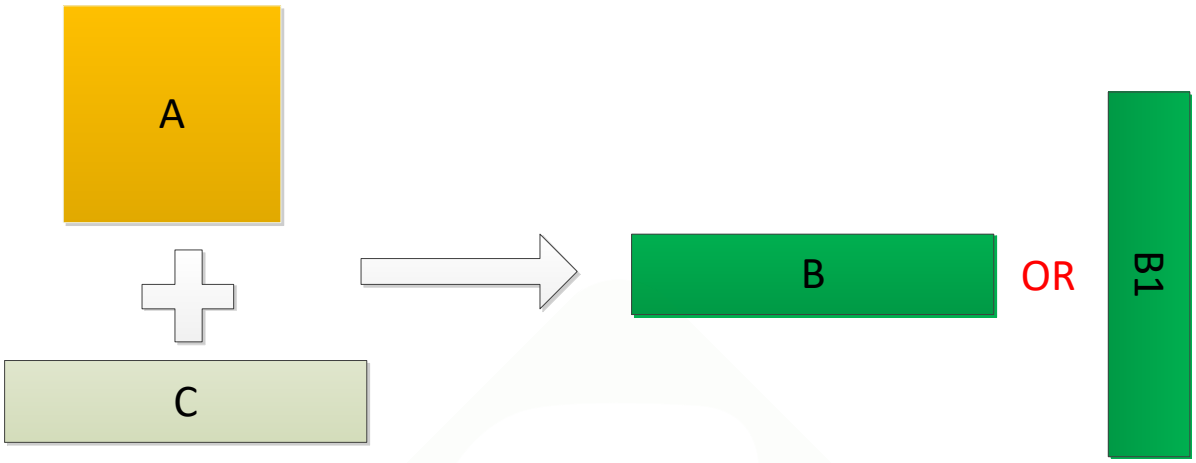


Fig. 14-10 The size constraint among A B C

4. YUV420/422-8bit virtual stride need 8byte align, xoff/yoff need 2byte align.
5. YUV420/422-10bit virtual stride need 16byte align，not support xoff/yoff.
6. Vertical scale down or not && Horizontal bi-cubic scale up src0 width<=2048.
Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928.
7. Vertical scale down or not && Horizontal bilinear scale up src0 width<=4096.
Vertical scale up && Horizontal bilinear scale up src0 width<=3856.

Chapter 15 Image Enhancement Processor（IEP）

15.1 Overview

The Image Enhancement Processor (IEP) receives data from system main memory and transmits data to system main memory by AXI bus.

The features of IEP are as follows:

- **Image format**
  - Input data: YUV420/YUV422; semi-planar/planar; UV swap
  - Output data: YUV420/YUV422; semi-planar; UV swap; Tile mode
  - YUV down sampling conversion from 422 to 420
  - Max resolution for dynamic image up to 1920x1080
- **De-interlace**
  - **I5O2**: Input 5 Fields Output 2 frames mode
  - **I5O1T**: Input 5 Fields Output 1 Top frame mode
  - **I5O1B**: Input 5 Fields Output 1 Bottom frame mode
  - **I2O2**: Input 2 Fields Output 2 frames mode
  - **I1O1T**: Input 1 Field Output 1 Top frame mode
  - **I1O1B**: Input 1 Field Output 1 Bottom frame mode
  - **PULLDOWN_REC**: Pull down Recovery mode
  - **DETECT_ONLY**: Detect Only mode
  - **MVHIST**: De-interlace MV Histogram
  - **MD**: Motion Detection
  - **ME**: Motion Estimate
  - **MC**: Motion Compensation
  - **EEDI**: Enhanced Edge based Interpolation
  - **OSD DETECT**: On-Screen Display Detection
  - **FF DETECT**: Frame Field Detection
  - **FO DETECT**: Field Order Detection
  - **PD DETECT**: Pull down Detection
  - **CC**: Combining Check
- **Interface**
  - 32bit AHB bus slave
  - 128bit AXI bus master
  - Combined interrupt output

15.2 Block Diagram

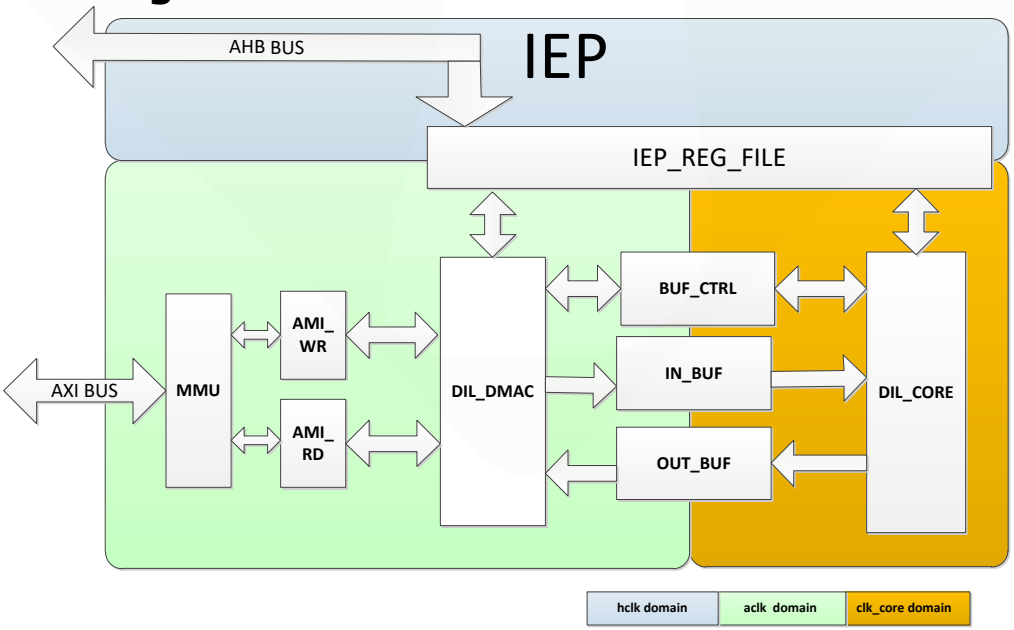


Fig.15-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

Deinterlace Core Processing

There are eight deinterlace modes (refer to feature description above) in the DIL_CORE block. Some important functions for deinterlace are in this module such as MD, ME, MC, EEDI.

DMA

DMA block responses for reading interlaced video data from DDR and writing frame data to DDR.

REG FILE

All configurable signals will be configured in this block and send to other function modules for using. Detect data and MVHIST data will be read back to user in this module by AHB bus.

15.3 Function Description

Deinterlace

There are eight deinterlace modes including I5O2, I5O1B, I5O1T, I2O2, I1O1B, I1O1T and detect only mode in the deinterlace block.

I5O2 mode

The I5O2 mode represents for 5 fields of input images and 2 frames of output images. This mode is the most frequently used. The input source images are stored as interlaced mode which means top field and bottom field are stored by the method that one top field line follows one bottom field or conversely. So, current, next and preview input frame address (SRC_ADDR_CURY, SRC_ADDR_NXTY and SRC_ADDR_PERY for Y channel) need to be configured. Top frame and bottom frame address (DST_ADDR_TOPY, DST_ADDR_BOTY for Y channel) need to be configured for output 2 frames.

I5O1B/T mode

The I5O1B and I5O1T mode have the same input images as the I4O2 mode, but only one frame output is generated once which means only need configure one output frame address(top frame address for I5O1T mode and bottom frame address for I5O1B mode).

I2O2 mode

The I2O2 mode only need current input source frame, output is the same as I5O2 mode. This mode is the fastest and the most bandwidth saving.

I1O1B/T mode

The I1O1B and I1O1T mode have the same input as I2O2 mode and the same output as I5O1B and I5O1T mode.

Bypass mode

If bypass mode is selected, there are not any deinterlace operations.

Pulldown Recovery mode

If the Pulldown Detection block detects the current source is pulldown interlace video. IEP supports Pulldown Recovery by setting this mode.

Detect Only mode

This mode has no output frames for saving power and bandwidth. All of the detection results will be read back though AHB bus.

15.4 Register Description

15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
IEP2_FRM_START	0x0000	W	0x00000000	Frame start and frame state register
IEP2_IEP_CONFIG0	0x0004	W	0x00000303	IEP configuration register0
IEP2_GATING_CTRL	0x0010	W	0x00000800	IEP auto gating register
IEP2_STATUS	0x0014	W	0x00000000	IEP status
IEP2_INT_EN	0x0020	W	0x00000011	IEP interrupt enable
IEP2_INT_CLR	0x0024	W	0x00000000	IEP interrupt clear
IEP2_INT_STS	0x0028	W	0x00000000	IEP interrupt status
IEP2_INT_RAW_STS	0x002C	W	0x00000000	IEP int raw status

Name	Offset	Size	Reset Value	Description
IEP2_VIR_SRC_IMG_WIDTH	0x0030	W	0x00000000	Source Image virtual width
IEP2_VIR_DST_IMG_WIDTH	0x0034	W	0x00000000	Destination Image virtual width
IEP2_SRC_IMG_SIZE	0x0038	W	0x00000000	Source image size
IEP2_DIL_CONFIG0	0x0040	W	0x00029F01	Deinterlace config register0
IEP2_IEP_TIMEOUT_CFG	0x0050	W	0x0065B9AA	Timeout config
IEP2_IEP_VERSION_INFO	0x0054	W	0x20056471	IEP version info
IEP2_DBG_FRM_CNT	0x0058	W	0x00000000	Frame counter
IEP2_DBG_TIMEOUT_CNT	0x005C	W	0x00000000	Timeout cnt
IEP2_SRC_ADDR_CURY	0x0060	W	0x00000000	Start address of source current image(Y), frame addr
IEP2_SRC_ADDR_NXTY	0x0064	W	0x00000000	Start address of source next image(Y), frame addr
IEP2_SRC_ADDR_PREY	0x0068	W	0x00000000	Start address of source previous image(Y), frame addr
IEP2_SRC_ADDR_CURUV	0x006C	W	0x00000000	Start address of source current image(UV), SP MODE UV frame or U PMODE frame addr
IEP2_SRC_ADDR_CURV	0x0070	W	0x00000000	Start address of source current image(V), P MODE V frame addr
IEP2_SRC_ADDR_NXTUV	0x0074	W	0x00000000	Start address of source next image(UV), SP MODE UV frame or U PMODE frame addr
IEP2_SRC_ADDR_NXTV	0x0078	W	0x00000000	Start address of source next image(V), P MODE V frame addr
IEP2_SRC_ADDR_PREUV	0x007C	W	0x00000000	Start address of source previous image(UV), SP MODE UV frame addr or U PMODE frame addr
IEP2_SRC_ADDR_PREV	0x0080	W	0x00000000	Start address of source previous image(V), P MODE V frame addr
IEP2_SRC_ADDR_MD	0x0084	W	0x00000000	MD LOAD ADDR BASE register0
IEP2_SRC_ADDR_MV	0x0088	W	0x00000000	MV LOAD ADDR BASE register0
IEP2_ROI_ADDR	0x008C	W	0x00000000	ROI ADDR register
IEP2_DST_ADDR_TOPY	0x00B0	W	0x00000000	DST TOP FRAME LUMA ADDR Register
IEP2_DST_ADDR_BOTY	0x00B4	W	0x00000000	DST BOT FRAME LUMA ADDR Register
IEP2_DST_ADDR_TOPC	0x00B8	W	0x00000000	DST TOP FRAME CHROMA ADDR Register
IEP2_DST_ADDR_BOTC	0x00BC	W	0x00000000	DST BOT FRAME CHROMA ADDR Register
IEP2_DST_ADDR_MD	0x00C0	W	0x00000000	MD SAVE ADDR BASE register0
IEP2_DST_ADDR_MV	0x00C4	W	0x00000000	MV SAVE ADDR BASE register0
IEP2_MD_CONFIG0	0x00E0	W	0x00000044	Motion dect config
IEP2_DECT_CONFIG0	0x00E4	W	0x3C3C001E	Frame field dect, pulldown dect, OSD dect, comb dect
IEP2_OSD_LIMIT_CONFIG	0x00F0	W	0x00000000	OSD limite area dect config
IEP2_OSD_LIMIT_AREA0	0x00F4	W	0x00000000	OSD limite area 0
IEP2_OSD_LIMIT_AREA1	0x00F8	W	0x00000000	OSD limite area 1
IEP2_OSD_CONFIG0	0x00FC	W	0x00020032	OSD dect config
IEP2_OSD_AREA_CONF0	0x0100	W	0x00000000	OSD area 0
IEP2_OSD_AREA_CONF1	0x0104	W	0x00000000	OSD area 1

Name	Offset	Size	Reset Value	Description
IEP2_OSD_AREA_CONF2	0x0108	W	0x00000000	OSD area 2
IEP2_OSD_AREA_CONF3	0x010C	W	0x00000000	OSD area 3
IEP2_OSD_AREA_CONF4	0x0110	W	0x00000000	OSD area 4
IEP2_OSD_AREA_CONF5	0x0114	W	0x00000000	OSD area 5
IEP2_OSD_AREA_CONF6	0x0118	W	0x00000000	OSD area 6
IEP2_OSD_AREA_CONF7	0x011C	W	0x00000000	OSD area 7
IEP2_ME_CONFIG0	0x0120	W	0x001443A4	ME search config
IEP2_ME_LIMIT_CONFIG	0x0124	W	0x00001B25	ME SERACH LIMITE
IEP2_MV_TRU_LIST0	0x0128	W	0x00000000	MV trust list0~3
IEP2_MV_TRU_LIST1	0x012C	W	0x00000000	MV trust list4~7
IEP2_EEDI_CONFIG0	0x0130	W	0x0000000C	EEDI CONFIG register0
IEP2_BLE_CONFIG0	0x0134	W	0x00000001	BLE CONFIG register0
IEP2_COMB_CONFIG0	0x0138	W	0x001004FF	COMB DECT CONFIG register0
IEP2_DIL_MTN_TAB0	0x0140	W	0x00000000	DIL_MTN_TAB0 table value
IEP2_DIL_MTN_TAB1	0x0144	W	0x00000000	DIL_MTN_TAB1 table value
IEP2_DIL_MTN_TAB2	0x0148	W	0x00000000	DIL_MTN_TAB2 table value
IEP2_DIL_MTN_TAB3	0x014C	W	0x00000000	DIL_MTN_TAB3 table value
IEP2_DIL_MTN_TAB4	0x0150	W	0x01010000	DIL_MTN_TAB4 table value
IEP2_DIL_MTN_TAB5	0x0154	W	0x06050302	DIL_MTN_TAB5 table value
IEP2_DIL_MTN_TAB6	0x0158	W	0x0F0D0A08	DIL_MTN_TAB6 table value
IEP2_DIL_MTN_TAB7	0x015C	W	0x1C191512	DIL_MTN_TAB7 table value
IEP2_DIL_MTN_TAB8	0x0160	W	0x2B282420	DIL_MTN_TAB8 table value
IEP2_DIL_MTN_TAB9	0x0164	W	0x3634312E	DIL_MTN_TAB9 table value
IEP2_DIL_MTN_TAB10	0x0168	W	0x3D3C3A38	DIL_MTN_TAB10 table value
IEP2_DIL_MTN_TAB11	0x016C	W	0x40403F3E	DIL_MTN_TAB11 table value
IEP2_DIL_MTN_TAB12	0x0170	W	0x40404040	DIL_MTN_TAB12 table value
IEP2_DIL_MTN_TAB13	0x0174	W	0x40404040	DIL_MTN_TAB13 table value
IEP2_DIL_MTN_TAB14	0x0178	W	0x40404040	DIL_MTN_TAB14 table value
IEP2_DIL_MTN_TAB15	0x017C	W	0x40404040	DIL_MTN_TAB15 table value
IEP2_RO_PD_TCNT	0x0400	W	0x00000000	Pulldown dect top field cnt
IEP2_RO_PD_BCNT	0x0404	W	0x00000000	Pulldown dect bot field cnt
IEP2_RO_FF_CUR_TCNT	0x0408	W	0x00000000	Frame field dect current frame top field cnt
IEP2_RO_FF_CUR_BCNT	0x040C	W	0x00000000	Frame field dect current frame bot field cnt
IEP2_RO_FF_NXT_TCNT	0x0410	W	0x00000000	Frame field dect next frame top field cnt
IEP2_RO_FF_NXT_BCNT	0x0414	W	0x00000000	Frame field dect next frame bot field cnt
IEP2_RO_FF_BLE_TCNT	0x0418	W	0x00000000	Frame field dect current and next frame blend top field cnt
IEP2_RO_FF_BLE_BCNT	0x041C	W	0x00000000	Frame field dect current and next frame blend bot field cnt
IEP2_RO_FF_COMB_NZ	0x0420	W	0x00000000	Frame field dect current frame comb dect none zero num
IEP2_RO_FF_COMB_F	0x0424	W	0x00000000	Frame field dect current frame comb dect num
IEP2_RO_OSD_NUM	0x0428	W	0x00000000	OSD area dect number
IEP2_RO_OUT_COMB_CNT	0x042C	W	0x00000000	Deinterlace output comb dect
IEP2_RO_FF_GRADT_TCNT	0x0430	W	0x00000000	Frame field dect, gradt top field cnt

Name	Offset	Size	Reset Value	Description
IEP2_RO_FF_GRADT_BCNT	0x0434	W	0x00000000	Frame field dect, gradt bot field cnt
IEP2_RO_MC_VLD_CNT	0x0438	W	0x00000000	MC valid cnt
IEP2_RO_OSD_AREA0_X	0x0440	W	0x00000000	OSD area dect area0 x
IEP2_RO_OSD_AREA0_Y	0x0444	W	0x00000000	OSD area dect area0 y
IEP2_RO_OSD_AREA1_X	0x0448	W	0x00000000	OSD area dect area1 x
IEP2_RO_OSD_AREA1_Y	0x044C	W	0x00000000	OSD area dect area1 y
IEP2_RO_OSD_AREA2_X	0x0450	W	0x00000000	OSD area dect area2 x
IEP2_RO_OSD_AREA2_Y	0x0454	W	0x00000000	OSD area dect area2 y
IEP2_RO_OSD_AREA3_X	0x0458	W	0x00000000	OSD area dect area3 x
IEP2_RO_OSD_AREA3_Y	0x045C	W	0x00000000	OSD area dect area3 y
IEP2_RO_OSD_AREA4_X	0x0460	W	0x00000000	OSD area dect area4 x
IEP2_RO_OSD_AREA4_Y	0x0464	W	0x00000000	OSD area dect area4 y
IEP2_RO_OSD_AREA5_X	0x0468	W	0x00000000	OSD area dect area5 x
IEP2_RO_OSD_AREA5_Y	0x046C	W	0x00000000	OSD area dect area5 y
IEP2_RO_OSD_AREA6_X	0x0470	W	0x00000000	OSD area dect area6 x
IEP2_RO_OSD_AREA6_Y	0x0474	W	0x00000000	OSD area dect area6 y
IEP2_RO_OSD_AREA7_X	0x0478	W	0x00000000	OSD area dect area7 x
IEP2_RO_OSD_AREA7_Y	0x047C	W	0x00000000	OSD area dect area7 y
IEP2_RO_MV_HIST_BIN0	0x0480	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN1	0x0484	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN2	0x0488	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN3	0x048C	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN4	0x0490	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN5	0x0494	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN6	0x0498	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN7	0x049C	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN8	0x04A0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN9	0x04A4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN10	0x04A8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN11	0x04AC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN12	0x04B0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN13	0x04B4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN14	0x04B8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN15	0x04BC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN16	0x04C0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN17	0x04C4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN18	0x04C8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN19	0x04CC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN20	0x04D0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN21	0x04D4	W	0x00000000	MV histogram

Name	Offset	Size	Reset Value	Description
IEP2_RO_MV_HIST_BIN22	0x04D8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN23	0x04DC	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN24	0x04E0	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN25	0x04E4	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN26	0x04E8	W	0x00000000	MV histogram
IEP2_RO_MV_HIST_BIN27	0x04EC	W	0x00000000	MV histogram
IEP2_PERF_LATENCY_CTRL0	0x0600	W	0x00000010	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_LATENCY_CTRL1	0x0604	W	0x00000011	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_MAX_LATENCY_NUM0	0x0608	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_LATENCY_SAMP_NUM	0x060C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_LATENCY_ACC_SUM	0x0610	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_WR_AXI_TOTAL_BYTE	0x0614	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_WORKING_CNT	0x0618	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_PERF_RD_AXI_TOTAL_BYTE	0x061C	W	0x00000000	Only exist when this IP has axi_performance monitor feature
IEP2_MMU_DTE_ADDR	0x0800	W	0x00000000	MMU DTE address
IEP2_MMU_STATUS	0x0804	W	0x00000018	MMU status
IEP2_MMU_CMD	0x0808	W	0x00000000	MMU command
IEP2_MMU_PAGE_FAULT_ADDR	0x080C	W	0x00000000	Page fault address
IEP2_MMU_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU zap one line
IEP2_MMU_INT_RAWSTAT	0x0814	W	0x00000000	MMU interruption raw status
IEP2_MMU_INT_CLEAR	0x0818	W	0x00000000	MMU interruption clear
IEP2_MMU_INT_MASK	0x081C	W	0x00000000	MMU interruption mask
IEP2_MMU_INT_STATUS	0x0820	W	0x00000000	MMU interruption status
IEP2_MMU_AUTO_GATING	0x0824	W	0x00000001	MMU auto gating config
IEP2_MMU_ID	0x0828	W	0x00000000	MMU ID

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access **DW**-Double WORD (64 bits) access*

15.4.2 Detail Register Description

IEP2_FRM_START

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_iep_frm_en Frame start, Write 1, frame work enable, frame end self clear

IEP2_IEP_CONFIG0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_iep_init_dis 1'b1: Frame start not init 1'b0: Frame start initial
21	W1C	0x0	sw_iep_sreset_p Write 1 to global reset iep, auto clear
20	RW	0x0	sw_iep_rst_protect_dis Dma bus error, default protect soft reset,1'b0:Protect reset;1'b1: Direct reset;
19:17	RO	0x0	reserved
16	RW	0x0	sw_iep_debug_data_en If assert this bit, the debug signals will have data(just for power saving).
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_iep_dst_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10,2'b11: Reserved
11:10	RO	0x0	reserved
9:8	RW	0x3	sw_iep_dst_fmt 2'b00,2'b01: Reserved 2'b10: YUV422 2'b11: YUV420
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_iep_src_yuv_swap 2'b00: SP UV 2'b01: SP VU 2'b10, 2'b11: P
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_iep_src_fmt 2'b00,2'b01: Reserved 2'b10: YUV422 2'b11: YUV420

IEP2_GATING_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_reg_clk_on Reg clk is auto gating,if write 1, clk always on, not gating, also control by sw_iep_clk_on.
10	RW	0x0	sw_dma_clk_on Aclk is auto gating,if write 1, clk always on, not gating, also control by sw_iep_clk_on.
9	RW	0x0	sw_ram_clk_on All ram clk always on 1'b0: Clk gating 1'b1: Clk always on
8	RW	0x0	sw_ctrl_clk_on CTRL clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
7	RW	0x0	sw_out_clk_on OUT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.

Bit	Attr	Reset Value	Description
6	RW	0x0	sw_ble_clk_on BLE clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
5	RW	0x0	sw_eedi_clk_on EEDI clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
4	RW	0x0	sw_mc_clk_on MC clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
3	RW	0x0	sw_me_clk_on ME clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
2	RW	0x0	sw_dect_clk_on DECT clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
1	RW	0x0	sw_md_clk_on MD clk is auto gating, if write 1, clk always on, not gating, also control by sw_iep_clk_on.
0	RW	0x0	sw_iep_clk_on IEP clk is auto gating, if write 1, clk always on, not gating.

IEP2_STATUS

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	ro_arst_finish_done IEP protect safety reset success status, write 1 clear or frame start clear.

IEP2_INT_EN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sw_iep_timeout_int_en Timeout int enable
4	RW	0x1	sw_iep_bus_error_en Bus error int enable
3:2	RO	0x0	reserved
1	RW	0x0	sw_iep_osd_max_en Frame process OSD dect done interrupt 1'b0: Inactive 1'b1: Active
0	RW	0x1	sw_iep_frm_done_en Frame process done interrupt 1'b0: Inactive 1'b1: Active

IEP2_INT_CLR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	W1C	0x0	sw_iep_timeout_int_clr Time out interruption clear
4	W1C	0x0	sw_iep_bus_error_clr Bus error interruption clear

Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	W1C	0x0	sw_iep_osd_max_clr OSD max interruption clear
0	W1C	0x0	sw_iep_frm_done_clr Frame process done interrupt clear

IEP2_INT_STS

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_sts Timeout error int status
4	RO	0x0	ro_bus_error_sts Bus error interruption status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_sts Frame process OSD dect done interrupt status
0	RO	0x0	ro_frm_done_sts Frame process done interrupt status

IEP2_INT_RAW_STS

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ro_timeout_raw Timeout int raw status
4	RO	0x0	ro_bus_error_raw Bus error int raw status
3:2	RO	0x0	reserved
1	RO	0x0	ro_osd_max_raw OSD max int raw status
0	RO	0x0	ro_frm_done_raw Frame done int raw status

IEP2_VIR_SRC_IMG_WIDTH

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_iep_src_vir_uv_stride Source uv virtual image width(word align)
15:0	RW	0x0000	sw_iep_src_vir_y_stride Source y virtual image width(word align)

IEP2_VIR_DST_IMG_WIDTH

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_iep_dst_vir_stride Destination virtual image width(word align)

IEP2_SRC_IMG_SIZE

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_iep_src_pic_height Source and destination image height(pixel align and need minus 1, for example 1080 need config 1079)
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_iep_src_pic_width Source and destination image width(pixel align and need minus 1, for example 1920 need config 1919)

IEP2_DIL_CONFIG0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x1	sw_dil_mv_hist_en Deinterlace MV histogram enable. 1'b1: Deinterlace need MV histogram 1'b0: MV histogram not work
16	RW	0x0	sw_dil_roi_en Deinterlace roi enable 1'b1: Deinterlace use roi mode 1'b0: ROI not work When ROI mode enable, each tile has 4bit for ROI mode 4'b0000: Normal mode 4'b0001: Bypass mode 4'b0010: EEDI only mode 4'b0011: Ma only mode 4'b0100: Ma mc mode(no cc) 4'b0101: Mc EEDI mode 4'b0110:4'b0111:Reserved 4'b1xxx: Mc only mode(MC's MV will be appointed by global MV based on roi[2:0])
15	RW	0x1	sw_dil_comb_en Deinterlace output result comb dect, if is comb block back to original data, else select deinterlace result. 1'b1: Output data comb dect enable 1'b0: Output data not comb dect
14:13	RO	0x0	reserved
12	RW	0x1	sw_dil_memc_en Deinterlace use me, mc result. 1'b1: ME, MC work enable 1'b0: ME, MC not work enable
11	RW	0x1	sw_dil_osd_en On screen display dect enable. 1'b1: OSD dect enable 1'b0: OSD not dect
10	RW	0x1	sw_dil_pd_en Pulldown dect enable. 1'b1: Pulldown dect enable 1'b0: Pulldown not dect
9	RW	0x1	sw_dil_ff_en Frame field dect work enable. 1'b1: Frame field dect enable 1'b0: Frame field not dect
8	RW	0x1	sw_dil_md_pre_en 1'b1: MD use previous frame data enable 1'b0: MD only use current frame data to calc md

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5	RW	0x0	sw_dil_field_order Field display order. 1'b0: TFF, top field display first 1'b1: BFF, bot field display first
4	RW	0x0	sw_dil_out_mode Output deinterlace result to DDR, line mode or tile mode. 1'b0: LINE mode 1'b1: TILE mode
3:0	RW	0x1	sw_dil_mode 4'b0000: DIL DISABLE 4'b0001: I5O2 mode 4'b0010: I5O1T mode 4'b0011: I5O1B mode 4'b0100: I2O2 mode 4'b0101: I1O1T mode 4'b0110: I1O1B mode 4'b0111: Pulldown recovery mode 4'b1000: Bypass mode 4'b1001: Dectect only mode other,reserved

IEP2_IEP_TIMEOUT_CFG

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_iep_timeout_en IEP timeout enable
30:0	RW	0x0065b9aa	sw_iep_timeout_cnt When sw_iep_timeout_en ==1, timeout_cnt == sw_iep_timeout_cnt, iep timeout

IEP2_IEP_VERSION_INFO

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x2	major Used for IP structure version information
27:20	RO	0x00	minor Big feature change under same structure
19:0	RO	0x56471	svnbuild Rtl current svn number

IEP2_DBG_FRM_CNT

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	dbg_frm_cnt Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

IEP2_DBG_TIMEOUT_CNT

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	dbg_timeout_cnt When sw_iep_timeout_en==1, frame cnt, frame start auto clear.

IEP2_SRC_ADDR_CURY

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_cury Current frame luma addr, frame addr

IEP2_SRC_ADDR_NXTY

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxty Next frame luma addr, frame addr

IEP2_SRC_ADDR_PREY

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_prey Start address of source previous image(Y), frame addr

IEP2_SRC_ADDR_CURUV

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curuv Start address of source current image(UV), SP MODE UV frame addr or U PMODE frame addr

IEP2_SRC_ADDR_CURV

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_curv Start address of source current image(V), P MODE V frame addr

IEP2_SRC_ADDR_NXTUV

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtuv Start address of source next image(UV), SP MODE UV frame addr or U PMODE frame addr

IEP2_SRC_ADDR_NXTV

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_nxtv Start address of source next image(V), P MODE V frame addr

IEP2_SRC_ADDR_PREUV

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_preuv Start address of source previous image(UV),SP MODE UV frame addr or U PMODE frame addr

IEP2_SRC_ADDR_PREV

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_prev Start address of source previous image(V), P MODE V frame addr

IEP2_SRC_ADDR_MD

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_md Md addr, save previous frame md gradt

IEP2_SRC_ADDR_MV

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_src_addr_MV Md addr, save previous frame MV

IEP2_ROI_ADDR

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_addr_roi ROI addr base

IEP2_DST_ADDR_TOPY

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topy Dst top frame luma start addr

IEP2_DST_ADDR_BOTY

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_boty Dst bot frame luma start addr

IEP2_DST_ADDR_TOPC

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_topc Dst top frame chroma start addr, uv save together

IEP2_DST_ADDR_BOTC

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_botc Dst bot frame chroma start addr, uv save together

IEP2_DST_ADDR_MD

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_md MD addr, save previous frame md gradt, and also save current frame md grad

IEP2_DST_ADDR_MV

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_iep_dst_addr_MV Output MV addr, save previous frame MV and also save current frame MV

IEP2_MD_CONFIG0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	sw_md_theta GRADtc = CLIP(GRADtf -sw_md_theta,0,255);
7:4	RW	0x4	sw_md_r Gradtf *md_r*63/(gradtf*md_r*63 + gradv)
3:0	RW	0x4	sw_md_lambda Current grad * md_lambda/8 + pre grad*(8-md_lambda)/8, value range from 0~8

IEP2_DECT_CONFIG0

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x3c	sw_osd_gradv_thr Origial data grad compare with gradv thr, if more than gradv_thr, may be OSD area.
23:16	RW	0x3c	sw_osd_gradh_thr Origial data grad compare with gradh thr, if more than gradh_thr, may be OSD area.
15:12	RO	0x0	reserved
11:8	RW	0x0	sw_osd_area_num OSD area number, frame field dect, pulldown not dect this area, comb dect also use this value, 0~8.
7:0	RW	0x1e	sw_dect_resi_thr For resi to bin, frame field, pulldown, OSD dect use this value.

IEP2_OSD_LIMIT_CONFIG

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_osd_pos_limit_num OSD constrain area dect num, real value = OSD_pos_num+1
3:1	RO	0x0	reserved
0	RW	0x0	sw_osd_pos_limit_en OSD area constrain dect enable

IEP2_OSD_LIMIT_AREA0

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area0 OSD constrain area 0 [6:0]: OSD constrain area0 x start, 16pixel num [13:7]: OSD constrain area0 x end, 16pixel num [22:14]: OSD constrain area0 y start, 4 pixel num [31:23]: OSD constrain area0 y end, 4 pixel num

IEP2_OSD_LIMIT_AREA1

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_osd_limit_area1 OSD limite area 1 [6:0]: OSD constrain area0 x start, 16pixel num [13:7]: OSD constrain area0 x end, 16pixel num [22:14]: OSD constrain area0 y start, 4 pixel num [31:23]: OSD constrain area0 y end, 4 pixel num

IEP2_OSD_CONFIG0

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x002	sw_osd_line_num Dect line num should more than OSD_line_num*4, this lines may be OSD area.
15:11	RO	0x00	reserved
10:0	RW	0x032	sw_osd_pec_thr A line should more than OSD_per_thr, this line may be OSD area.

IEP2_OSD_AREA_CONF0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end0 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta0 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end0 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta0 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end1 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta1 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end1 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta1 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end2 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta2 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end2 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta2 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end3 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta3 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end3 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta3 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end4 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta4 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end4 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta4 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end5 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta5 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end5 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta5 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end6 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta6 OSD area y start, 4 pixel num
13:7	RW	0x00	sw_osd_x_end6 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta6 OSD area x start, 16pixel num

IEP2_OSD_AREA_CONF7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:23	RW	0x000	sw_osd_y_end7 OSD area y end, 4 pixel num
22:14	RW	0x000	sw_osd_y_sta7 OSD area y start, 4 pixel num

Bit	Attr	Reset Value	Description
13:7	RW	0x00	sw_osd_x_end7 OSD area x end, 16pixel num
6:0	RW	0x00	sw_osd_x_sta7 OSD area x start, 16pixel num

IEP2_ME_CONFIG0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x14	sw_me_thr_offset me_thr = me_thr(from md module) - sw_me_thr_offset. This signal is signed from(-128 ~127).
15:12	RW	0x4	sw_mv_similar_num_thr0 MV similar check result = MV_similar_invld_num < sw_mv_similar_num_thr0
11:8	RW	0x3	sw_mv_similar_thr surround MV similar = |cur_MV - surround_MV| < sw_mv_similar_thr
7:4	RW	0xa	sw_mv_bonus MVc calc MV,the same MV range value
3:0	RW	0x4	sw_me_pena balance resi and grad, grad*me_pena/8, me_pena value range from 0~8

IEP2_ME_LIMIT_CONFIG

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x1b	sw_mv_right_limt MV right range limit, from 0~27, default 27
7:6	RO	0x0	reserved
5:0	RW	0x25	sw_mv_left_limt MV left range limit, from -27~0, default-27

IEP2_MV_TRU_LIST0

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list3_mv MV trust list MV3
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list3_vld MV trust list MV3 vld
23:18	RW	0x00	sw_mv_tru_list2_mv MV trust list MV2
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list2_vld MV trust list MV2 vld
15:10	RW	0x00	sw_mv_tru_list1_mv MV trust list MV1
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list1_vld MV trust list MV1 vld
7:2	RW	0x00	sw_mv_tru_list0_mv MV trust list MV0

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list0_vld MV trust list MV0 vld

IEP2_MV_TRU_LIST1

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	sw_mv_tru_list7_mv MV trust list MV7
25	RO	0x0	reserved
24	RW	0x0	sw_mv_tru_list7_vld MV trust list MV7 vld
23:18	RW	0x00	sw_mv_tru_list6_mv MV trust list MV6
17	RO	0x0	reserved
16	RW	0x0	sw_mv_tru_list6_vld MV trust list MV6 vld
15:10	RW	0x00	sw_mv_tru_list5_mv MV trust list MV5
9	RO	0x0	reserved
8	RW	0x0	sw_mv_tru_list5_vld MV trust list MV5 vld
7:2	RW	0x00	sw_mv_tru_list4_mv MV trust list MV4
1	RO	0x0	reserved
0	RW	0x0	sw_mv_tru_list4_vld MV trust list MV4 vld

IEP2_EEDI_CONFIG0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x0c	sw_eedi_thr0 EEDI thr0

IEP2_BLE_CONFIG0

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x1	sw_ble_backtoma_num Left and right colum of frame will back to ma, give up mc.

IEP2_COMB_CONFIG0

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	sw_comb_cnt_thr Top or bot frame comb dect compare with original comb dect
23:22	RO	0x0	reserved
21:16	RW	0x10	sw_comb_feature_thr Top or bot frame comb dect compare with original comb dect
15:8	RW	0x04	sw_comb_t_thr Different line compare use comb_t_thr

Bit	Attr	Reset Value	Description
7:0	RW	0xff	sw_comb_osd_vld OSD area dect comb block back to original [0] area0,[1]area1....[7]area7 1'b1: Back to original 1'b0: Not back to original

IEP2_DIL_MTN_TAB0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab03 sw_mtn_sub_tab03
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab02 sw_mtn_sub_tab02
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab01 sw_mtn_sub_tab01
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab00 sw_mtn_sub_tab00

IEP2_DIL_MTN_TAB1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab07 sw_mtn_sub_tab07
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab06 sw_mtn_sub_tab06
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab05 sw_mtn_sub_tab05
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab04 sw_mtn_sub_tab04

IEP2_DIL_MTN_TAB2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab11 sw_mtn_sub_tab11
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab10 sw_mtn_sub_tab10
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab09 sw_mtn_sub_tab09
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab08 sw_mtn_sub_tab08

IEP2_DIL_MTN_TAB3

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	sw_mtn_sub_tab15 sw_mtn_sub_tab15
23	RO	0x0	reserved
22:16	RW	0x00	sw_mtn_sub_tab14 sw_mtn_sub_tab14
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab13 sw_mtn_sub_tab13
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab12 sw_mtn_sub_tab12

IEP2_DIL_MTN_TAB4

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x01	sw_mtn_sub_tab19 sw_mtn_sub_tab19
23	RO	0x0	reserved
22:16	RW	0x01	sw_mtn_sub_tab18 sw_mtn_sub_tab18
15	RO	0x0	reserved
14:8	RW	0x00	sw_mtn_sub_tab17 sw_mtn_sub_tab17
7	RO	0x0	reserved
6:0	RW	0x00	sw_mtn_sub_tab16 sw_mtn_sub_tab16

IEP2_DIL_MTN_TAB5

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	sw_mtn_sub_tab23 sw_mtn_sub_tab23
23	RO	0x0	reserved
22:16	RW	0x05	sw_mtn_sub_tab22 sw_mtn_sub_tab22
15	RO	0x0	reserved
14:8	RW	0x03	sw_mtn_sub_tab21 sw_mtn_sub_tab21
7	RO	0x0	reserved
6:0	RW	0x02	sw_mtn_sub_tab20 sw_mtn_sub_tab20

IEP2_DIL_MTN_TAB6

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x0f	sw_mtn_sub_tab27 sw_mtn_sub_tab27
23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:16	RW	0x0d	sw_mtn_sub_tab26 sw_mtn_sub_tab26
15	RO	0x0	reserved
14:8	RW	0x0a	sw_mtn_sub_tab25 sw_mtn_sub_tab25
7	RO	0x0	reserved
6:0	RW	0x08	sw_mtn_sub_tab24 sw_mtn_sub_tab24

IEP2_DIL_MTN_TAB7

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	sw_mtn_sub_tab31 sw_mtn_sub_tab31
23	RO	0x0	reserved
22:16	RW	0x19	sw_mtn_sub_tab30 sw_mtn_sub_tab30
15	RO	0x0	reserved
14:8	RW	0x15	sw_mtn_sub_tab29 sw_mtn_sub_tab29
7	RO	0x0	reserved
6:0	RW	0x12	sw_mtn_sub_tab28 sw_mtn_sub_tab28

IEP2_DIL_MTN_TAB8

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x2b	sw_mtn_sub_tab35 sw_mtn_sub_tab35
23	RO	0x0	reserved
22:16	RW	0x28	sw_mtn_sub_tab34 sw_mtn_sub_tab34
15	RO	0x0	reserved
14:8	RW	0x24	sw_mtn_sub_tab33 sw_mtn_sub_tab33
7	RO	0x0	reserved
6:0	RW	0x20	sw_mtn_sub_tab32 sw_mtn_sub_tab32

IEP2_DIL_MTN_TAB9

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x36	sw_mtn_sub_tab39 sw_mtn_sub_tab39
23	RO	0x0	reserved
22:16	RW	0x34	sw_mtn_sub_tab38 sw_mtn_sub_tab38
15	RO	0x0	reserved
14:8	RW	0x31	sw_mtn_sub_tab37 sw_mtn_sub_tab37
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x2e	sw_mtn_sub_tab36 sw_mtn_sub_tab36

IEP2_DIL_MTN_TAB10

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x3d	sw_mtn_sub_tab43 sw_mtn_sub_tab43
23	RO	0x0	reserved
22:16	RW	0x3c	sw_mtn_sub_tab42 sw_mtn_sub_tab42
15	RO	0x0	reserved
14:8	RW	0x3a	sw_mtn_sub_tab41 sw_mtn_sub_tab41
7	RO	0x0	reserved
6:0	RW	0x38	sw_mtn_sub_tab40 sw_mtn_sub_tab40

IEP2_DIL_MTN_TAB11

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab47 sw_mtn_sub_tab47
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab46 sw_mtn_sub_tab46
15	RO	0x0	reserved
14:8	RW	0x3f	sw_mtn_sub_tab45 sw_mtn_sub_tab45
7	RO	0x0	reserved
6:0	RW	0x3e	sw_mtn_sub_tab44 sw_mtn_sub_tab44

IEP2_DIL_MTN_TAB12

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab51 sw_mtn_sub_tab51
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab50 sw_mtn_sub_tab50
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab49 sw_mtn_sub_tab49
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab48 sw_mtn_sub_tab48

IEP2_DIL_MTN_TAB13

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab55 sw_mtn_sub_tab55
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab54 sw_mtn_sub_tab54
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab53 sw_mtn_sub_tab53
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab52 sw_mtn_sub_tab52

IEP2_DIL_MTN_TAB14

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab59 sw_mtn_sub_tab59
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab58 sw_mtn_sub_tab58
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab57 sw_mtn_sub_tab57
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab56 sw_mtn_sub_tab56

IEP2_DIL_MTN_TAB15

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x40	sw_mtn_sub_tab63 sw_mtn_sub_tab63
23	RO	0x0	reserved
22:16	RW	0x40	sw_mtn_sub_tab62 sw_mtn_sub_tab62
15	RO	0x0	reserved
14:8	RW	0x40	sw_mtn_sub_tab61 sw_mtn_sub_tab61
7	RO	0x0	reserved
6:0	RW	0x40	sw_mtn_sub_tab60 sw_mtn_sub_tab60

IEP2_RO_PD_TCNT

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_tcnt Pulldown dect top field cnt

IEP2_RO_PD_BCNT

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	ro_dect_pd_bcnt Pulldown dect bot field cnt

IEP2_RO_FF_CUR_TCNT

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_tcnt Frame field dect current frame top field cnt

IEP2_RO_FF_CUR_BCNT

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_cur_bcnt Frame field dect current frame bot field cnt

IEP2_RO_FF_NXT_TCNT

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_tcnt Frame field dect next frame top field cnt

IEP2_RO_FF_NXT_BCNT

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_nxt_bcnt Frame field dect next frame bot field cnt

IEP2_RO_FF_BLE_TCNT

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_tcnt Frame field dect current and next frame blend top field cnt

IEP2_RO_FF_BLE_BCNT

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_dect_ff_ble_bcnt Frame field dect current and next frame blend bot field cnt

IEP2_RO_FF_COMB_NZ

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_nz Frame field dect current frame none zero num

IEP2_RO_FF_COMB_F

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	ro_dect_ff_comb_f Frame field dect current frame comb dect num

IEP2_RO_OSD_NUM

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ro_dect_osd_cnt OSD area dect number

IEP2_RO_OUT_COMB_CNT

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_out_osd_comb_cnt Top frame and bot frame OSD area comb num
15:0	RO	0x0000	ro_out_comb_cnt Top frame and bot frame comb num

IEP2_RO_FF_GRADT_TCNT

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_tcnt Frame field dect, gradt top field cnt

IEP2_RO_FF_GRADT_BCNT

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_ff_gradt_bcnt Frame field dect, gradt bot field cnt

IEP2_RO_MC_VLD_CNT

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	ro_mc_vld_cnt OSD area dect number

IEP2_RO_OSD_AREA0_X

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta0 1 pixel

IEP2_RO_OSD_AREA0_Y

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end0 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta0 1 pixel

IEP2_RO_OSD_AREA1_X

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta1 1 pixel

IEP2_RO_OSD_AREA1_Y

Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end1 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta1 1 pixel

IEP2_RO_OSD_AREA2_X

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta2 1 pixel

IEP2_RO_OSD_AREA2_Y

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end2 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta2 1 pixel

IEP2_RO_OSD_AREA3_X

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta3 1 pixel

IEP2_RO_OSD_AREA3_Y

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

Bit	Attr	Reset Value	Description
26:16	RO	0x000	ro_y_end3 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta3 1 pixel

IEP2_RO_OSD_AREA4_X

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta4 1 pixel

IEP2_RO_OSD_AREA4_Y

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end4 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta4 1 pixel

IEP2_RO_OSD_AREA5_X

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta5 1 pixel

IEP2_RO_OSD_AREA5_Y

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end5 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta5 1 pixel

IEP2_RO_OSD_AREA6_X

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end6 1 pixel
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:0	RO	0x000	ro_x_sta6 1 pixel

IEP2_RO_OSD_AREA6_Y

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end6 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta6 1 pixel

IEP2_RO_OSD_AREA7_X

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_x_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_x_sta7 1 pixel

IEP2_RO_OSD_AREA7_Y

Address: Operational Base + offset (0x047C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	ro_y_end7 1 pixel
15:11	RO	0x00	reserved
10:0	RO	0x000	ro_y_sta7 1 pixel

IEP2_RO_MV_HIST_BIN0

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist01 Mv_histogram01
15:0	RO	0x0000	ro_mv_hist00 Mv_histogram00

IEP2_RO_MV_HIST_BIN1

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist03 Mv_histogram03
15:0	RO	0x0000	ro_mv_hist02 Mv_histogram02

IEP2_RO_MV_HIST_BIN2

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist05 Mv_histogram05

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ro_mv_hist04 Mv_histogram04

IEP2_RO_MV_HIST_BIN3

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist07 Mv_histogram07
15:0	RO	0x0000	ro_mv_hist06 Mv_histogram06

IEP2_RO_MV_HIST_BIN4

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist09 Mv_histogram09
15:0	RO	0x0000	ro_mv_hist08 Mv_histogram08

IEP2_RO_MV_HIST_BIN5

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist11 Mv_histogram11
15:0	RO	0x0000	ro_mv_hist10 Mv_histogram10

IEP2_RO_MV_HIST_BIN6

Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist13 Mv_histogram13
15:0	RO	0x0000	ro_mv_hist12 Mv_histogram12

IEP2_RO_MV_HIST_BIN7

Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist15 Mv_histogram15
15:0	RO	0x0000	ro_mv_hist14 Mv_histogram14

IEP2_RO_MV_HIST_BIN8

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist17 Mv_histogram17
15:0	RO	0x0000	ro_mv_hist16 Mv_histogram16

IEP2_RO_MV_HIST_BIN9

Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist19 Mv_histogram19
15:0	RO	0x0000	ro_mv_hist18 Mv_histogram18

IEP2_RO_MV_HIST_BIN10

Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist21 Mv_histogram21
15:0	RO	0x0000	ro_mv_hist20 Mv_histogram20

IEP2_RO_MV_HIST_BIN11

Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist23 Mv_histogram23
15:0	RO	0x0000	ro_mv_hist22 Mv_histogram22

IEP2_RO_MV_HIST_BIN12

Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist25 Mv_histogram25
15:0	RO	0x0000	ro_mv_hist24 Mv_histogram24

IEP2_RO_MV_HIST_BIN13

Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist27 Mv_histogram27
15:0	RO	0x0000	ro_mv_hist26 Mv_histogram26

IEP2_RO_MV_HIST_BIN14

Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist29 Mv_histogram29
15:0	RO	0x0000	ro_mv_hist28 Mv_histogram28

IEP2_RO_MV_HIST_BIN15

Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist31 Mv_histogram31
15:0	RO	0x0000	ro_mv_hist30 Mv_histogram30

IEP2_RO_MV_HIST_BIN16

Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist33 Mv_histogram33
15:0	RO	0x0000	ro_mv_hist32 Mv_histogram32

IEP2_RO_MV_HIST_BIN17

Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist35 Mv_histogram35
15:0	RO	0x0000	ro_mv_hist34 Mv_histogram34

IEP2_RO_MV_HIST_BIN18

Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist37 Mv_histogram37
15:0	RO	0x0000	ro_mv_hist36 Mv_histogram36

IEP2_RO_MV_HIST_BIN19

Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist39 Mv_histogram39
15:0	RO	0x0000	ro_mv_hist38 Mv_histogram38

IEP2_RO_MV_HIST_BIN20

Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist41 Mv_histogram41
15:0	RO	0x0000	ro_mv_hist40 Mv_histogram40

IEP2_RO_MV_HIST_BIN21

Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist43 Mv_histogram43
15:0	RO	0x0000	ro_mv_hist42 Mv_histogram42

IEP2_RO_MV_HIST_BIN22

Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist45 Mv_histogram45
15:0	RO	0x0000	ro_mv_hist44 Mv_histogram44

IEP2_RO_MV_HIST_BIN23

Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist47 Mv_histogram47
15:0	RO	0x0000	ro_mv_hist46 Mv_histogram46

IEP2_RO_MV_HIST_BIN24

Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist49 Mv_histogram49
15:0	RO	0x0000	ro_mv_hist48 Mv_histogram48

IEP2_RO_MV_HIST_BIN25

Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist51 Mv_histogram51
15:0	RO	0x0000	ro_mv_hist50 Mv_histogram50

IEP2_RO_MV_HIST_BIN26

Address: Operational Base + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist53 Mv_histogram54
15:0	RO	0x0000	ro_mv_hist52 Mv_histogram53

IEP2_RO_MV_HIST_BIN27

Address: Operational Base + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_mv_hist55 Mv_histogram55
15:0	RO	0x0000	ro_mv_hist54 Mv_histogram54

IEP2_PERF_LATENCY_CTRL0

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr sw_rd_latency_thr
7:4	RW	0x1	sw_rd_latency_id sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by software configuration 1'b1: Clear by frame end

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enable
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

IEP2_PERF_LATENCY_CTRL1

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x1	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type sw_addr_align_type

IEP2_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 rd_max_latency_num_ch0

IEP2_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 rd_latency_thr_num_ch0

IEP2_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum rd_latency_acc_sum

IEP2_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

IEP2_PERF_WORKING_CNT

Address: Operational Base + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

IEP2_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

IEP2_MMU_DTE_ADDR

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU dte addr

IEP2_MMU_STATUS

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault. 1'b0: Read 1'b1: Write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x1	mmu_idle The MMU is idle when accesses are being translated and there is no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: The MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled. The mode is enabled by command.
0	RW	0x0	mmu_paging_enabled MMU page enable

IEP2_MMU_CMD

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled. 3'b000: Enable paging 3'b001: Disable paging 3'b010: Turn on stall mode 3'b011: Turn off stall mode 3'b100: Zap the entire page table cache 3'b101: Leave page fault mode 3'b110: Reset the MMU

IEP2_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr mmu_page_fault_addr

IEP2_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mmu_zap_one_line Address to be invalidated from the page table cache

IEP2_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

IEP2_MMU_INT_CLEAR

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_clear Read bus error interrupt clear. Write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear Page fault interrupt clear. Write 1 to this register can clear page fault interrupt.

IEP2_MMU_INT_MASK

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error_int_en MMU read bus error int enable
0	RW	0x0	page_fault_int_en PAGE fault int enable

IEP2_MMU_INT_STATUS

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error MMU read bus error
0	RW	0x0	page_fault Page fault

IEP2_MMU_AUTO_GATING

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_auto_gating When it is 1, the MMU will auto gating itself

IEP2_MMU_ID

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	mmu_axi_id
3:1	RO	0x0	reserved
0	RW	0x0	reg_load_mmu_en

15.5 Application Notes

Input source definition constant

The input source definition must be 16x4 aligned, which means the image width 16 aligned and image height 4 aligned.

Normal configuration flow

- Set IEP2 related signals based on current video source information and deinterlace mode (must open frame done interruption by asserting the sw_iep_frm_done_en signal)
- Set frame start by letting sw_iep_frm_en = 1
- Wait for IEP frame done interruption
- Read back many kinds of Detection data and MVHIST, analyze these data, get the global MV, OSD information etc
- Configure the MV, OSD information back
- Set frame start for deinterlace loop

Chapter 16 USB2.0 Host

16.1 Overview

There are two USB2.0 host controller, each USB2.0 host controller supports fully USB2.0 functions with one EHCI host controller and one OHCI host controller, and each host controller has one USB port. OHCI host controller only supports full-speed and low-speed mode and is used for full-speed devices and low-speed devices. EHCI only supports high-speed mode and is used for high-speed devices. OHCI host controller and EHCI host controller shares the same USB port, EHCI host controller will auto select the owner (OHCI or EHCI) of this USB port depending on the speed mode of attached devices, when selecting OHCI as owner, OHCI host controller will serve for the attached device; when selecting EHCI as owner, EHCI host controller will serve for the attached device.

USB2.0 Host Controller supports the following features:

- Compatible Specifications
  - Universal Serial Bus Specification, Revision 2.0
  - Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Open Host Controller Interface Specification (OHCI), Revision 1.0a

Support High-speed (480Mbps), Full-speed (12Mbps) and Low-speed (1.5Mbps)

16.2 Block Diagram

USB2.0 Host Controller comprises with:

- EHCI Host Controller: Perform High-speed transactions
- OHCI Host Controller: Perform full/low-speed transactions
- Port Routing Control: Select EHCI Host Controller or OHCI Host Controller

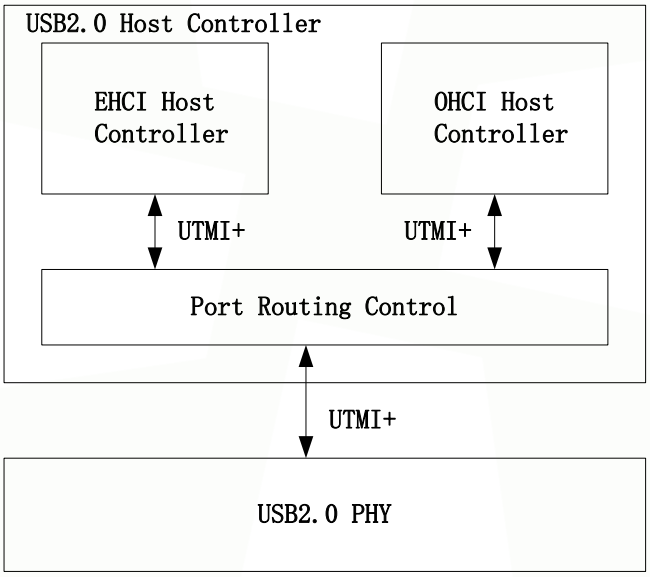


Fig. 16-1 USB2.0 Host Controller Block Diagram

16.3 Function Description

16.3.1 EHCI Host Controller

It performs descriptors and data read or write from or to system memory and packs or unpack USB transactions from or to UTMI+ interface defined in EHCI specification for high-speed data transmission.

16.3.2 OHCI Host Controller

It performs descriptors and data read/write from/to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in OHCI specification for full-speed or low-speed data transmission.

16.3.3 Port Routing Control

As part of logic in the EHCI host controller, it is used to auto-select EHCI or OHCI host controller to serve the attached device depending on the speed of the attached device.

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 16-1 USB2.0 Host Controller Address Mapping

Base Address[16]	Device	Address Length	Offset Address Range
1'b0	EHCI	64K BYTE	0x00000 ~ 0x0ffff
1'b1	OHCI	64K BYTE	0x10000 ~ 0x1ffff

EHCI and OHCI register definitions, please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

16.5 Interface Description

Table 16-2 USB2.0 PHY Interface Description

Module Pin	Direction	Pin Name	Descriptions
DP0	I/O	HOST0_DP	USB differential signal IO, positive end
DM0	I/O	HOST0_DM	USB differential signal IO, negative end
DP1	I/O	HOST1_DP	USB differential signal IO, positive end
DM1	I/O	HOST1_DM	USB differential signal IO, negative end
VCCA18	I/O	HOST_AVDD_1V8	1.8V power supply
RREF	I/O	HOST_EXTR	External 200ohm Bias Resistance, this is the 200ohm external resistance pin for termination.
AGND	I/O	VSS	Ground IO for both 3.3V, 1.8V and 0.8V
ACCA33	I/O	USB_AVDD3V3	3.3 V power supply(only Full speed driver)
VDDA	I/O	USB_AVDD_0V8	0.8 V power supply

16.6 Application Notes

16.6.1 Some Settings and Description About USB PHY

Here list some usbhost phy configure register of TOP_GRF in detail.

- GRF_USBPHY_CON2

Table 16-3 GRF_USBPHY_CON2 Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usbhost_id_pull_up Software configure for HOSTPHY id_pull_up Enable ID pin sample. Signal that enables the sampling of the analog ID line. 1'b0: Sampling of ID pin is disabled (IDDIG force to low). 1'b1: Sampling of ID pin is enabled.

Bit	Attr	Reset Value	Description
14	RW	0x0	usbhost_dischrgvbus Software configure for HOSTPHY dischrgvbus Discharge VBUS18. The signal enables discharging VBUS18. 1'b0: do not discharge VBUS18 through a resistor 1'b1: discharge VBUS18 through a resistor (this has to be active for at least 50ms)
13	RW	0x0	usbhost_chrgvbus Software configure for HOSTPHY chrgvbus Charge VBUS18. The signal enables charging VBUS18. 1'b0: do not charge VBUS18 through a resistor 1'b1: charge VBUS18 through a resistor (this has to be active for at least 30ms)
12	RW	0x0	usbhost_txbitstuff_enable Software configure for HOSTPHY txbitstuff_enable TX BITSTUFF ENABLE. Indicates if the data on the DATA_OUT[15:0]lines need to be bit stuffed or not. 1'b0: Bit stuffing is disabled 1'b1: Bit stuffing is enabled This signal is only used when OP_MODE[1:0] is set to 11b.
11	RW	0x1	usbhost_otg_suspendm Software configure for HOSTPHY suspend This signal is used for VBUS negotiation in OTG application and HOST disconnect in HOST application, in DEVICE mode this signal should be tie to 0. In OTG/HOST application this signal should be connected to 1. In HOST application, IDDIG is not valid, OTG_SUSPENDM must be set to 1 and OTG_SUSPENDM_BYPS must set to 1. In DEVICE application, IDDIG is not valid, OTG_SUSPENDM must be set to 0 and OTG_SUSPENDM_BYPS must set to 1.
10	RW	0x1	usbhost_data_bus16_8 Software configure for HOSTPHY data_bus16_8 Selects between 8 and 16-bit data transfer. 1'b1: 16-bit data path operation enabled, CLK60_30 = 30 MHz. 1'b0: 8-bit data path operation enabled, CLK60_30 = 60 MHz. This signal is sampled by USB PHY IP macro cell only when RESET becomes low. Default is 16-bit model and not suggest to configure this bit.
9	RW	0x0	usbhost_pll_en Software configure for HOSTPHY pll_en PLL enable signal, internal PLL start to work when this signal is set to high, otherwise PLL is disabled and PHY IP stop working. This bit must be set to high before usb function.

Bit	Attr	Reset Value	Description
8	RW	0x1	usbhost_chg_rst Software configure for HOSTPHY chg_rst Charge detector reset signal, active high, asynchronous. 1'b0: charge detector is normal operation 1'b1: charge detector is reset to initial
7	RW	0x0	usbhost_chg_en Software configure for HOSTPHY chg_en Charge detector enable signal. 1'b0: charging detect is off, IP is configured as SDP in HOST application or is configured as standard device in DEVICE application 1'b1: charging detect is on, IP is configured as CDP in HOST application or is configured as portable device in DEVICE application
6	RW	0x1	usbhost_termselect Software configure for HOSTPHY termselect Termination Select. This signal selects between the FS and HS terminations: 1'b0: HS termination enabled 1'b1: FS termination enabled In default this is controlled by hardware.
5:4	RW	0x1	usbhost_xcvrselect Software configure for HOSTPHY xcvrselect Transceiver Select. 2'b00: HS Transceiver enabled 2'b01: FS Transceiver enabled 2'b10: LS Transceiver enabled 2'b11: Reserved In default this is controlled by hardware.
3:2	RW	0x0	usbhost_opmode Software configure for HOSTPHY opmode Operational Mode. These signals select between various operational modes: 2'b00: Normal operation 2'b01: Non-driving. Transmitter buffer is in high impedance and pull-up/down resistors are disconnected 2'b10: Disable bit stuffing and NRZI encoding 2'b11: Reserved In default this is controlled by hardware.

Bit	Attr	Reset Value	Description
1	RW	0x0	usbhost_suspend_n Software configure for HOSTPHY suspend_n Active low, asynchronous. When enabled, drive IP into suspend mode and consume minimal current from power supply. 1'b0: IP in suspend mode, only those circuit that serve for resume function is still active 1'b1: IP in normal operation In default this is controlled by hardware.
0	RW	0x0	hostphy_input_sel HOSTPHY input selection. 1'b0: Hardware input 1'b1: Software input

16.6.2 USB Host Reset Sequence

In USB function mode, the recommended reset sequence is in figure1-2. 'RST' is the reset signal of USB controller and 'CLK' is the main clock of USB controller. At first, 'RST' is set to 1 and USB controller starts to work; secondly, USB controller outputs 'SUSPENDM'. 'RESET' is the reset of the usb phy. Both 'RST' and 'RESET' are controlled by CRU model.
'SUSPENDM' is set to 1 firstly to enable PLL, PLL starts to work and frequency starts locking, 'RESET' is set to 0 to enable clock lock detector, and 'CLK60_30' is valid when frequency is stable. PLL lock time(Tlock) is about 500us including the time of bandgap building, PLL locking and so on, Tlock also includes the PVT range.
'CLK_480' is controlled by 'PLL_EN', and 'CLK_480' is not valid when 'PLL_EN' is 0. Because 'PLL_EN' is the reset signal of delay control cell, so there must be a rise edge of 'PLL_EN' to make delay control cell to work correctly. Tdelay is the time of 'PLL_EN' rise edge to 'CLK_480' transmitting 480MHz clock, the value is greater than 200us and less than 500us.

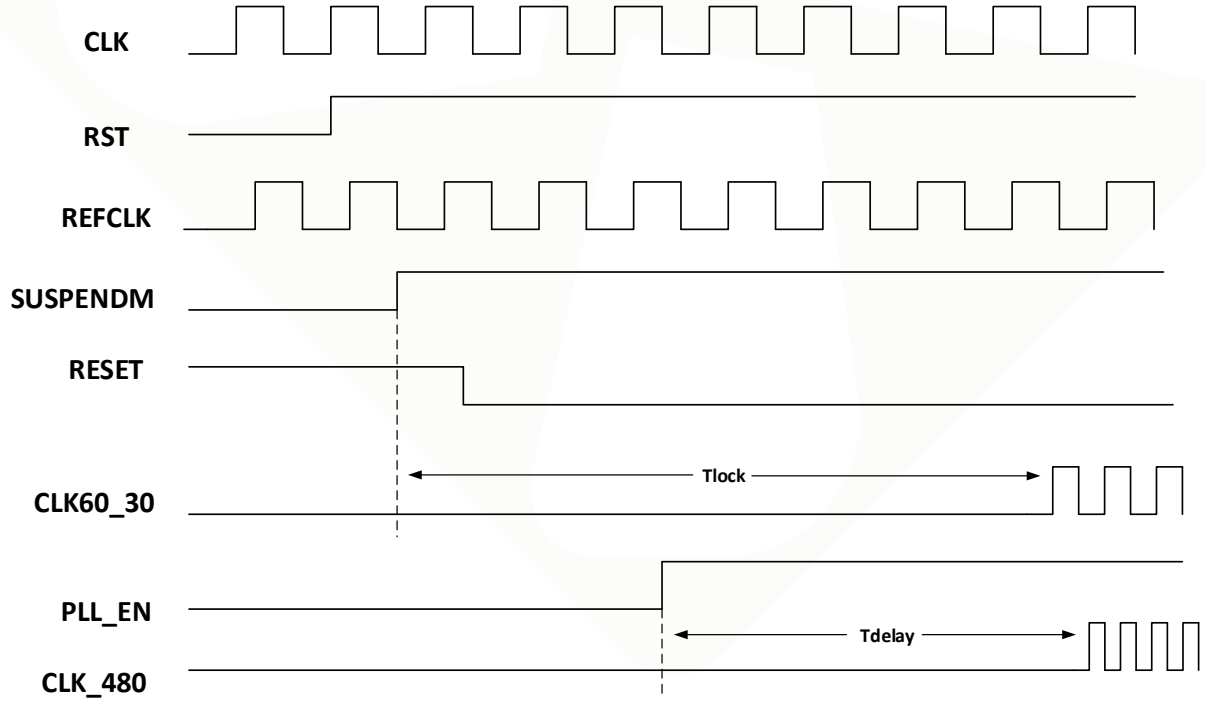


Fig. 16-2 USB2.0 Host reset sequence

16.6.3 Host Charge Detect Sequence

There are three steps in charge detector sequence including data contact detection, primary

detection and secondary detection. Data contact detection is judging DEVICE are connected or not, primary detection is judging whether the charger is connected or not, secondary detection is judging whether the charger is DCP or CDP.
When 'CHG_EN' is set to 1, 'CHG_RST' is set to 0 to start charge detection. This two signal can be control by GRF_USBPHY_CON2. During the detection, 'RESET' must be set to 1, the PHY function is disable before 'PHY_CONNECT' changes to 1. Tdelay is greater than 1ms.

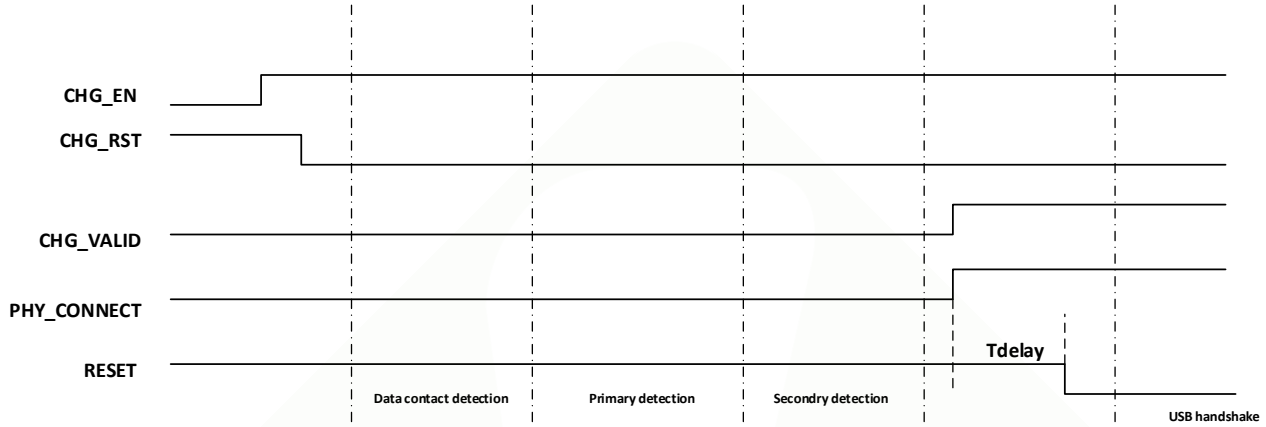


Fig. 16-3 USB2.0 Host charge sequence

Table 1-4 and the description about charge model. Host can be configured as DCP, CDP and SDP.

Table 16-4 Charge Description in host model

Host Port	Device Port	CHG_VALID	PHY_CONNECT
DCP	support charge	1	0
DCP	not support charge	0	0
CDP	support charge	1	1
CDP	not support charge	0	1
SDP	-	0	1

16.6.4 Program Flow

Please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

Chapter 17 USB3.0 Controller

17.1 Overview

There are two USB3.0 Controllers, one can use as USB3.0 OTG Controller, another one can use as USB3.0 Host Controller only. USB3.0 OTG Controller can act as static host, static device, USB2.0/3.0 OTG A device or B device basing on the status of input ID from USB2.0 PHY. It can perform data transmission between host and device as host or device for Super-Speed / High-Speed / Full-Speed / Low-Speed.

USB3.0 OTG controller supports the following features:

- General Features
  1. Compatible Specification
     - Universal Serial Bus 3.0 Specification, Revision 1.0
     - Universal Serial Bus Specification, Revision 2.0
     - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  2. Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  3. Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  4. Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  5. LPM protocol in USB 2.0 and U0, U1, U2, and U3 states for USB 3.0
  6. Dynamic FIFO memory allocation for endpoints
  7. Keep-Alive feature in LS mode and (micro-)SOFs in HS/FS modes
  8. Low MIPS requirement
     - Driver involved only in setting up transfers and high-level error recovery
     - Hardware handles data packing and routing to a specific pipe
- Application Interface Features
  1. AHB Slave interface
  2. AXI Master interface
     - Programmable burst lengths up to 16
     - Handle fixed burst address alignment
     - Programmable number of outstanding read/write requests up to 16
     - Concurrent read/write to get best performance of USB3.0 duplex operation
- USB3.0 Device Features
  1. Up to 10 IN endpoints, including control endpoint 0
  2. Up to 6 OUT endpoints, including control endpoint 0
  3. Up to 16 endpoint transfer resources, each one for each endpoint
  4. Flexible endpoint configuration for multiple applications/USB set-configuration modes
  5. Hardware handles ERDY and burst
  6. Stream-based bulk endpoints with controller automatically initiating data movement
  7. Isochronous endpoints with isochronous data in data buffers
  8. Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB Class-Specific Device Features
  1. Stream support for UASP application
  2. Gathering of scattered packet to support Ethernet Over USB
  3. Scheduling of multiple Ethernet packets without interrupt
  4. Variable FIFO buffer allocation for each endpoint
  5. For isochronous applications, scheduling of variable-length payloads for each microframe
  6. Microframe precise scheduling for isochronous applications
  7. Configurable endpoint type selection and dynamic FIFO allocation to facilitate multi-function/composite device implementation. During set-config or alternate-setting, device resources are reconfigured to meet the configuration or alternate setting requirements.
- USB 3.0 xHCI Host Features
  1. Support up to 64 devices
  2. Support 1 interrupter

3. Support 1 USB2.0 port and 1 Super-Speed port
4. Concurrent USB3.0/USB2.0 traffic, up to 8.48Gbps bandwidth
5. Support standard or open-source xHCI and class driver

- USB 3.0 Dual-Role Device (DRD) Features
  1. Static Device Operation
  2. Static Host Operation
  3. USB3.0/USB2.0 OTG A device and B device basing on ID
  4. Not support USB3.0/USB2.0 OTG session request protocol(SRP), host negotiation protocol(HNP) and Role Swap Protocol(RSP)

17.2 Block Diagram

USB3.0 OTG Controller comprises with:

- Bus Interface/List Management: Register Interface/Data and Descriptors DMA management
- HS/FS/LS MAC : USB2.0 part logic
- SS MAC : SS part logic
- USB2.0 PHY: UTMI+ interface USB2.0 PHY
- SS PHY: Pipe Interface Super-Speed PHY

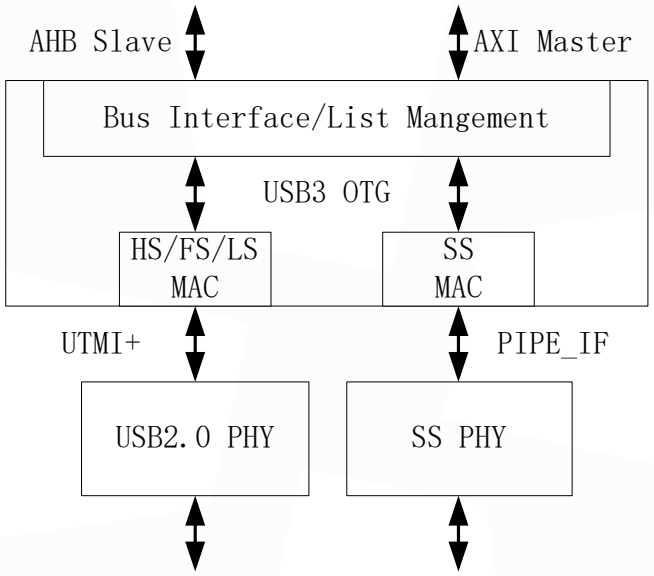


Fig.17-1USB3.0 OTG Block Diagram

17.3 Function Description

As a USB3.0 OTG controller, it can act as static xHCI host controller, static device controller, USB3.0/2.0 OTG A device or B device basing on ID of USB2.0 PHY.

As device controller, it can work on either USB2.0 speed or Super-Speed basing on speed of host attached to, and process USB tractions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of PCIE&SS PHY.

As host controller, it can work on USB2.0 speed, Super-Speed or both basing on speed or type of attached device, and process USB tractions described in the descriptors (read back from external memory by AXI master) to/from UTMI+ interface and Pipe Interface of SS PHY.

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 17-1USB3 Address Mapping

Offset Address Range	Register Type

0x00000 ~ 0x07FFF	xHCI Registers, see xHCI spec.
0x0C100 ~ 0x0C6FF	Global Registers
0x0C700 ~ 0x0CBFF	Device Controller Registers
0x0CC00 ~ 0x0CFFF	Unused/Reserved
0x40000 ~ 0x7FFFF	Internal RAM0 – Debug Access (256KB)
0x80000 ~ 0xBFFFF	Internal RAM1 – Debug Access (256KB)
0xC0000 ~ 0xFFFFF	Internal RAM2 – Debug Access (256KB)

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
usb3otg_GSBUSCFG0	0xC100	W	0x00000001	Global SoC Bus Configuration Register 0
usb3otg_GSBUSCFG1	0xC104	W	0x00000300	Global SoC Bus Configuration Register 1
usb3otg_GTXTHRCFG	0xC108	W	0x00000000	Global Tx Threshold Control Register
usb3otg_GRXTHRCFG	0xC10C	W	0x00000000	Global Rx Threshold Control Register
usb3otg_GCTL	0xC110	W	0x13512004	Global Core Control Register
usb3otg_GSTS	0xC118	W	0x7E800000	Global Status Register
usb3otg_GUCTL1	0xC11C	W	0x0004018A	Global User Control Register 1
usb3otg_GSNPSID	0xC120	W	0x5533300A	Global SNPS ID Register
usb3otg_GGPIO	0xC124	W	0x00000000	Global General Purpose Input/Output Register
usb3otg_GUID	0xC128	W	0x20190520	Global User ID Register
usb3otg_GUCTL	0xC12C	W	0x02008010	Global User Control Register
usb3otg_GBUSERRADDRLO	0xC130	W	0x00000000	Global SoC Bus Error Address Register - Low
usb3otg_GBUSERRADDRHI	0xC134	W	0x00000000	Global SoC Bus Error Address Register - High
usb3otg_GPRTBIMAPLO	0xC138	W	0x00000000	Global SS Port to Bus Instance Mapping Register
usb3otg_GHWPARAMS0	0xC140	W	0x2020400A	Global Hardware Parameters Register 0
usb3otg_GHWPARAMS1	0xC144	W	0x0120C93B	Global Hardware Parameters Register 1
usb3otg_GHWPARAMS2	0xC148	W	0x20190520	Global Hardware Parameters Register 2
usb3otg_GHWPARAMS3	0xC14C	W	0x069CD084	Global Hardware Parameters Register 3
usb3otg_GHWPARAMS4	0xC150	W	0x47822010	Global Hardware Parameters Register 4
usb3otg_GHWPARAMS5	0xC154	W	0x04204018	Global Hardware Parameters Register 5

Name	Offset	Size	Reset Value	Description
usb3otg_GHWPARAMS6	0xC158	W	0x09D78020	Global Hardware Parameters Register 6
usb3otg_GHWPARAMS7	0xC15C	W	0x00000000	Global Hardware Parameters Register 7
usb3otg_GDBGFIFOSPACE	0xC160	W	0x000A0000	Global Debug Queue/FIFO Space Available Register
usb3otg_GDBGLNMCC	0xC168	W	0x00000000	Global Debug LNMCC Register
usb3otg_GDBGBMU	0xC16C	W	0x00000000	Global Debug BMU Register
usb3otg_GDBGLSPMUX	0xC170	W	0x003F0000	Global Debug LSP MUX Register - Device
usb3otg_GDBGLSP	0xC174	W	0x00000000	Global Debug LSP Register
usb3otg_GDBGEPINFO0	0xC178	W	0x00000000	Global Debug Endpoint Information Register 0
usb3otg_GDBGEPINFO1	0xC17C	W	0x00800000	Global Debug Endpoint Information Register 1
usb3otg_GPRTBIMAP_HSLO	0xC180	W	0x00000000	Global High-Speed Port to Bus Instance Mapping Register - Low
usb3otg_GPRTBIMAP_FSLO	0xC188	W	0x00000000	Global Full-Speed Port to Bus Instance Mapping Register - Low
usb3otg_GUSB2PHYCFG0	0xC200	W	0x40102400	Global USB2 PHY Configuration Register 0
usb3otg_GUSB3PIPECTL0	0xC2C0	W	0x00000000	
usb3otg_GTXFIFOSIZn	0xC300	W	0x00000042	Global Transmit FIFO Size Register n, offset (0xc300 + 4*n), n=0~6
usb3otg_GRXFIFOSIZn	0xC380	W	0x03340185	Global Receive FIFO Size Register n,
usb3otg_GEVNTADRLO0	0xC400	W	0x00000000	Global Event Buffer Address (Low) Register 0
usb3otg_GEVNTADRHI0	0xC404	W	0x00000000	Global Event Buffer Address (High) Register 0
usb3otg_GEVNTSIZ0	0xC408	W	0x00000000	Global Event Buffer Size Register 0
usb3otg_GEVNTCOUNT0	0xC40C	W	0x00000000	Global Event Buffer Count Register 0
usb3otg_GHWPARAMS8	0xC600	W	0x0000047C	Global Hardware Parameters Register 8
usb3otg_GTXFIFOPRIDEV	0xC610	W	0x00000000	Global Device TX FIFO DMA Priority Register
usb3otg_GTXFIFOPRIHST	0xC618	W	0x00000000	Global Host TX FIFO DMA Priority Register
usb3otg_GRXFIFOPRIHST	0xC61C	W	0x00000000	Global Host RX FIFO DMA Priority Register

Name	Offset	Size	Reset Value	Description
usb3otg_GFIFOPRIDBC	0xC620	W	0x00000000	Global Host Debug Capability DMA Priority Register
usb3otg_GDMAHLRATIO	0xC624	W	0x00000000	Global Host FIFO DMA High-Low Priority Ratio Register
usb3otg_GFLADJ	0xC630	W	0x00000000	Global Frame Length Adjustment Register
usb3otg_DCFG	0xC700	W	0x00080000	Device Configuration Register
usb3otg_DCTL	0xC704	W	0x00F00000	Device Control Register
usb3otg_DEVTEN	0xC708	W	0x00000000	Device Event Enable Register
usb3otg_DSTS	0xC70C	W	0x00520000	Device Status Register
usb3otg_DGCMDPAR	0xC710	W	0x00000000	Device Generic Command Parameter Register
usb3otg_DGCMD	0xC714	W	0x00000000	Device Generic Command Register
usb3otg_DALEPENA	0xC720	W	0x00000000	Device Active USB Endpoint Enable Register
usb3otg_DEPnCMDPAR2	0xC800	W	0x00000000	Device Physical Endpoint-n Command Parameter 2 Register, offset (0xc800 + 4*n), n=0~12
usb3otg_DEPnCMDPAR1	0xC804	W	0x00000000	Device Physical Endpoint-n Command Parameter 1 Register, offset (0xc804 + 4*n), n=0~12
usb3otg_DEPnCMDPAR0	0xC808	W	0x00000000	Device Physical Endpoint-n Command Parameter 0 Register, offset (0xc808 + 4*n), n=0~12
usb3otg_DEPnCMD	0xC80C	W	0x00000000	Device Physical Endpoint-n Command Register, offset (0xc80c + 4*n), n=0~12

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

usb3otg_GSBUSCFG0

Address: Operational Base + offset (0xC100)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	datrdreqinfo AXI-cache for Data Read (DatRdReqInfo).
27:24	RW	0x0	desrdreqinfo AXI-cache for Descriptor Read (DesRdReqInfo).
23:20	RW	0x0	datwrreqinfo AXI-cache for Data Write (DatWrReqInfo).
19:16	RW	0x0	deswrreqinfo AXI-cache for Descriptor Write (DesWrReqInfo).
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	datbigend This bit controls the endian mode for data accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
10	RW	0x0	desbigend This bit controls the endian mode for descriptor accesses. 1'b0: Little-endian (default) 1'b1: Big-endian
9:8	RO	0x0	reserved
7	RW	0x0	incr256brstena If software set this bit to 1, the AXI master uses INCR to do the 256-beat burst.
6	RW	0x0	incr128brstena If software set this bit to 1, the AXI master uses INCR to do the 128-beat burst.
5	RW	0x0	incr64brstena If software set this bit to 1, AXI master uses INCR to do the 64-beat burst.
4	RW	0x0	incr32brstena If software set this bit to 1, the AXI master uses INCR to do the 32-beat burst.
3	RW	0x0	incr16brstena If software set this bit to 1, the AXI master uses INCR to do the 16-beat burst.
2	RW	0x0	incr8brstena If software set this bit to 1, the AXI master uses INCR to do the 8-beat burst.
1	RW	0x0	incr4brstena When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers.

Bit	Attr	Reset Value	Description
0	RW	0x1	incrbrstena This bit determines the set of burst lengths the master interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables(INCR256/128/64/32/16/8/4). 0: INCRX burst mode ARLEN/AWLEN do not use INCR. They use only the following burst lengths: 1; 4 (if GSBUSCFG0.INCR4BrstEna = 1); 8 (if GSBUSCFG0.INCR8BrstEna = 1); 16 (if GSBUSCFG0.INCR16BrstEna = 1); 32 (if GSBUSCFG0.INCR32BrstEna = 1); 64 (if GSBUSCFG0.INCR64BrstEna = 1); 128 (if GSBUSCFG0.INCR128BrstEna = 1); 256 (if GSBUSCFG0.INCR256BrstEna = 1); 1: INCR (undefined length) burst mode; ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR4/8/16/32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the master interface uses only power-of-2 burst lengths (as enabled via GSBUSCFG0[7:0]).

usb3otg_GSBUSCFG1

Address: Operational Base + offset (0xC104)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	en1kpage 1K Page Boundary Enable. By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	RW	0x3	pipe_trans_limit AXI Pipelined Transfers Burst Request Limit. The field controls the number of outstanding pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 0: 1 request 1: 2 requests 2: 3 requests 3: 4 requests ... F: 16 requests

Bit	Attr	Reset Value	Description
7:0	RO	0x00	reserved

usb3otg_GTXTHRCFG

Address: Operational Base + offset (0xC108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	USBTxPktCntSel This field enables/disables the USB transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled; the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	RO	0x0	reserved
27:24	RW	0x0	USBTxPktCnt This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15. Note: This field must be less than or equal to the USB Maximum TX Burst Size field.
23:16	RW	0x00	USBMaxTxBurstSize
15:0	RO	0x0000	reserved reserved

usb3otg_GRXTHRCFG

Address: Operational Base + offset (0xC10C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	usb_rx_pkt_cntsel USB ReceivePacket Count Enable. This field enables/disables the USB reception multi-packet thresholding: 1'b0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. 1'b1: Not applied. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
28:13	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x0000	resvl_socout_spc Space reserved in rx fifo for ISOC OUT. In host mode, this field is not applicable and must be programmed to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped, If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of rx fifo is 8192. Therefore, this field is 13 bits wide. For HS/FS, the space reservation is the actual value.

usb3otg_GCTL

Address: Operational Base + offset (0xC110)

Bit	Attr	Reset Value	Description
31:19	RW	0x026a	pwrdnscale Not applied.
18	RW	0x0	masterfiltbypass Master Filter Bypass When this bit is set to 1'b1, all the filters are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0.
17	RW	0x0	bypassetaddr Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device core uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device core respond to a new address. Note: You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0.
16	RW	0x1	u2rstecn Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. Note: This bit is applicable only in device mode.

Bit	Attr	Reset Value	Description
15:14	RW	0x0	frmscldwn This field scales down device view of a SOF/USOF duration. For HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be 125us For FS mode, the scale-down value is multiplied by 8. This field also scales down the MaxPacketSize of the IN and OUT bulk endpoint to allow more traffic during simulation. It can only be changed from a non-zero value during simulation. 2'h0: 1024 bytes 2'h1: 512 bytes 2'h2: 256 bytes 2'h3: 128 bytes
13:12	RW	0x2	prtcapdir PRTCAPDIR: Port Capability Direction (PrtCapDir) 2'b01: for Host configurations 2'b10: for Device configurations SW should base on IDDIG input to set usb controller as an OTG 2.0 device with A-device or B-device.
11	RW	0x0	coresoftreset Core Soft Reset (CoreSoftReset) 1'b0: No soft reset; 1'b1: Soft reset to core Clears the interrupts and all the CSRs except the following registers: GCTL; GUCTL; GSTS; GSNPSID; GGPIO; GUID; GUSB2PHYCFGn registers; GUSB3PIPECTLn registers; DCFG; DCTL; DEVTEN; DSTS.
10	RW	0x0	sofitpsync Not applied.
9	RW	0x0	u1u2_timescale Not applied.
8	RW	0x0	debugattach Debug Attach. Not applied.

Bit	Attr	Reset Value	Description
7:6	RW	0x0	ramclksel RAM Clock Select (RAMClkSel) 2'b00: bus clock 2'b01: pipe clock (Only used in device mode) 2'b10: In device mode, pipe/2 clock. In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2 ports 2'b11: In device mode, selects mac2_clk as ram_clk (when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode); In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00.
5:4	RW	0x0	scaledown Scale-Down Mode (ScaleDown) When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes: 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	RW	0x0	disscramble Disable Scrambling (DisScramble) Transmit request to Link Partner on next transition to Recovery or Polling.
2	RW	0x1	u2exit_lfps If this bit is: 1'b0: the link treats 248ns LFPS as a valid U2 exit. 1'b1: the link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third party host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller.

Bit	Attr	Reset Value	Description
1	RO	0x0	gbl_hibernation_en This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	RW	0x0	dsblclkgtng Disable Clock Gating. This bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

usb3otg_GSTS

Address: Operational Base + offset (0xC118)

Bit	Attr	Reset Value	Description
31:20	RO	0x7e8	cbelt Current BELT Value. In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:12	RO	0x00	reserved
11	RO	0x0	SSIC_IP Not applied.
10	RO	0x0	OTG_IP OTG Interrupt Pending. This field indicates that there is a pending interrupt pertaining to OTG in OEVT register.
9	RO	0x0	bc_ip Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
8	RO	0x0	adp_ip ADP Interrupt Pending. This field indicates that there is a pending interrupt pertaining to ADP in ADPEVT register.
7	RO	0x0	host_ip Host Interrupt Pending. This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	RO	0x0	device_ip Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.

Bit	Attr	Reset Value	Description
5	W1C	0x0	csr_timeout When this bit is 1'b1, it indicates that the software performed a write or read to a core register that could not be completed within DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: h1FFFF).
4	W1C	0x0	buserraddrvld us Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	RO	0x0	reserved
1:0	RO	0x0	curmod Current Mode of Operation.

usb3otg_GUCTL1

Address: Operational Base + offset (0xC11C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	filter_se0_fsls_eop 1'b0: Default behaviour, no change in Linestate check for SE0 detection in FS/LS. 1'b1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP. This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the linestate is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM hanshake, the core will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the core will ignore single SE0 glitch on the linestate during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the LineState has SE0 glitches during transmission. This bit is quasi-static, i.e., should not be changed during device operation.

Bit	Attr	Reset Value	Description
28	RW	0x0	tx_ipgap_linecheck_dis 1'b0: Default behaviour, no change in Linestate check. 1'b1: Feature enabled, 2.0 MAC disables Linestate check during HS transmit. This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI Linestate during the transmit of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the Linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the core will ignore the linestate after TX and wait for a fixed clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between (tkn to tkn/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state (J) during transmission. This bit is quasi-static, i.e., should not be changed during device operation.
27	RW	0x0	dev_trb_out_spr_ind 1'b0: Default behaviour, no change in TRB status dword. 1'b1: Feature enabled, OUT TRB status indicates Short Packet. This bit is applicable for device mode only (and ignored in host mode). If the device application (SW/HW) wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the trbstatus, RSVD, SPR,PCM1, bufsize dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, i.e., should not be changed during device operation.
26	RW	0x0	dve_force_20clk_for_30clk Not applied.
25	RW	0x0	p3_in_u2 Not applied.

Bit	Attr	Reset Value	Description
24	RW	0x0	dev_l1_exit_by_hw 1'b0: Default behaviour, disables device L1 hardware exit logic. 1'b1: feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wkp signalling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This HW remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, i.e., should not be changed during device operation.
23:21	RW	0x0	ip_gap_add_on This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC.
20	RW	0x0	dev_lsp_tail_lock_dis 1'b0: Default behaviour, enables device lsp lock logic for tail TRB update. 1'b1: Fix disabled This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times.

Bit	Attr	Reset Value	Description
19	RW	0x0	nak_per_enh_fs 1'b1: Enables performance enhancement for FS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers.
18	RW	0x1	nak_per_enh_hs 1'b1: Enables performance enhancement for HS async endpoints in the presence of NAKs. 1'b0: Enhancement not applied. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other High Speed bulk endpoint which is ACked by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers.
17	RW	0x0	parkmode_disbale_ss Not applied.

Bit	Attr	Reset Value	Description
16	RW	0x0	parkmode_disable_hs This bit is used only in host mode. When this bit is set to 1 all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few high speed devices (such as Sandisk Cruzer Blade 4GB VID: 1921, PID: 21863 and Flex Drive VID: 3744, PID: 8552) when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices.
15	RW	0x0	parkmod_disavale_fsls This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all FS/LS bus instances in park mode disabled.
14:9	RO	0x00	reserved
8	RW	0x1	l1_susp_thrld_en_for_host This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals (see LPM Interface Signals table in the Databook) as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.

Bit	Attr	Reset Value	Description
7:4	RW	0x8	l1_susp_thrld_for_host This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit.
3	RW	0x1	hc_errata_enable Not applied.
2	RW	0x0	hc_parchk_disable Host Parameter Check Disable. When this bit is set to 0 (by default), the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating PARAMETER ERROR. When the bit is set to 1, the xHC does not perform parameter checks and does not generate PARAMETER ERROR completion code.
1	RW	0x1	ovrld_l1_susp_com If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition.
0	RW	0x0	loa_filter_en If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. Note: This bit is valid only in host mode.

usb3otg_GSNPSID

Address: Operational Base + offset (0xC120)

Bit	Attr	Reset Value	Description
31:0	RO	0x5533300a	snpsid SNPSID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 (DWC_usb3). SNPSID[15:0] indicates the release number. Current Release is 3.00a. Software uses this register to configure release-specific features in the driver.

usb3otg_GGPIO

Address: Operational Base + offset (0xC124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	gpo General Purpose Output This field's value is driven out on the gp_out[15:0] core output port.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	gpi General Purpose Input This field's read value reflects the gp_in[15:0] core input value.

usb3otg_GUID

Address: Operational Base + offset (0xC128)

Bit	Attr	Reset Value	Description
31:0	RW	0x20190520	userid Application-programmable ID field.

usb3otg_GUCTL

Address: Operational Base + offset (0xC12C)

Bit	Attr	Reset Value	Description
31:22	RW	0x008	refclkper This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 (8ns/125 MHz). This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to 0 at any time. If you never plan to use this feature, then set this field to 'h8, the default value.
21	RW	0x0	no_extr_di No Extra Delay Between SOF and the First. Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	sprs_ctrl_trans_en Sparse Control Transaction Enable. Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.
16	RW	0x0	res_bw_hs_esp Reserving 85% Bandwidth for HS Periodic EPs. By default, HC reserves 80% of the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices (HD Webcams) are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 payload per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
15	RW	0x1	cm_dev_addr Compliance Mode for Device Address. When this bit is 1'b1, Slot ID may have different value than Device Address if max_slot_enabled < 128. 1'b1: Increment Device Address on each Address Device command. 1'b0: Device Address is equal to Slot ID. The xHCI compliance requires this bit to be set to 1. The 0 mode is for debug purpose only. This allows you to easily identify a device connected to a port in the Lecroy or Eliisys trace during hardware debug. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
14	RW	0x0	usb_host_in_auto_retry_en Host IN Auto Retry. 1'b0: Auto Retry Disabled 1'b1: Auto Retry Enabled Note: This bit is also applicable to the device mode.
13	RW	0x0	en_overlap_chk Not applied.

Bit	Attr	Reset Value	Description
12	RW	0x0	ext_cap_suppt_en External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the core. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in Debug Capability returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer' field. This indicates there are no more capabilities.
11	RW	0x0	insrt_extr_fsbodi Insert Extra Delay Between FS Bulk OUT. Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. Note: Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices.

Bit	Attr	Reset Value	Description
10:9	RW	0x0	dtct Device Timeout Coarse Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The core first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: 2'b00: 0 usec -> use DTFT value instead 2'b01: 500 usec 2'b10: 1.5 msec 2'b11: 6.5 msec
8:0	RW	0x010	ctft Device Timeout Fine Tuning. This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) Quick Reference: if DTFT = 0x2, 2*256*8 = 4usec timeout if DTFT = 0x5, 5*256*8 = 10usec timeout if DTFT = 0xA, 10*256*8 = 20usec timeout if DTFT = 0x10, 16*256*8 = 32usec timeout if DTFT = 0x19, 25*256*8 = 51usec timeout if DTFT = 0x31, 49*256*8 = 100usec timeout if DTFT = 0x62, 98*256*8 = 200usec timeout

usb3otg_GBUSERRADDRLO

Address: Operational Base + offset (0xC130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	buserraddr Bus Address - Low. This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

usb3otg_GBUSERRADDRHI

Address: Operational Base + offset (0xC134)

Bit	Attr	Reset Value	Description
31:0	RU	0x00000000	buserraddr Bus Address - High. This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core. Note: Only supported in AHB and AXI configurations.

usb3otg_GPRTBIMAPLO

Address: Operational Base + offset (0xC138)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	BINUM1 SS USB Instance Number for Port 1 Application-programmable ID field.

usb3otg_GHWPARAMS0

Address: Operational Base + offset (0xC140)

Bit	Attr	Reset Value	Description
31:0	RO	0x2020400a	ghwparams0 Global Hardware Parameters Register 0.

usb3otg_GHWPARAMS1

Address: Operational Base + offset (0xC144)

Bit	Attr	Reset Value	Description
31:0	RO	0x0120c93b	ghwparams1 Global Hardware Parameters Register 1.

usb3otg_GHWPARAMS2

Address: Operational Base + offset (0xC148)

Bit	Attr	Reset Value	Description
31:0	RO	0x20190520	ghwparams2 Global Hardware Parameters Register 2.

usb3otg_GHWPARAMS3

Address: Operational Base + offset (0xC14C)

Bit	Attr	Reset Value	Description
31:0	RO	0x069cd084	ghwparams3 Global Hardware Parameters Register 3.

usb3otg_GHWPARAMS4

Address: Operational Base + offset (0xC150)

Bit	Attr	Reset Value	Description
31:0	RO	0x47822010	ghwparams4 Global Hardware Parameters Register 4.

usb3otg_GHWPARAMS5

Address: Operational Base + offset (0xC154)

Bit	Attr	Reset Value	Description
31:0	RO	0x04204018	ghwparams5 Global Hardware Parameters Register 5.

usb3otg_GHWPARAMS6

Address: Operational Base + offset (0xC158)

Bit	Attr	Reset Value	Description
31:0	RO	0x09d78020	ghwparams6 Global Hardware Parameters Register 6.

usb3otg_GHWPARAMS7

Address: Operational Base + offset (0xC15C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ghwparams7 Global Hardware Parameters Register 7.

usb3otg_GDBGFIFOSPACE

Address: Operational Base + offset (0xC160)

Bit	Attr	Reset Value	Description
31:16	RO	0x000a	space_available Space Available.
15:9	RO	0x00	reserved
8:0	RW	0x000	fifo_queue_select FIFO/Queue Select (or) Port-Select. FIFO/Queue Select[8:5] indicates the FIFO/Queue Type. FIFO/Queue Select[4:0] indicates the FIFO/Queue Number. Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register.

usb3otg_GDBGLNMCC

Address: Operational Base + offset (0xC168)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	lnmcc_berc This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only.

usb3otg_GDBGBMU

Address: Operational Base + offset (0xC16C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bmu_bcu BMU_BCU Debug information.
7:4	RO	0x0	bmu_dcu BMU_DCU Debug information.
3:0	RO	0x0	bmu_ccu BMU_CCU Debug information.

usb3otg_GDBGLSPMUX

Address: Operational Base + offset (0xC170)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x3f	logic_analyzer_trace Logic Analyzer Trace Port MUX Select. Currently only bits[21:16] are used. A value of 6'h3F drives "0"s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	RW	0x0	endbc Enable debugging of Debug capability LSP in Host mode. Use HostSelect to select DbC LSP debug information presented in the GDBGLSP register.
14	RO	0x0	reserved
13:8	RW	0x00	hostselect Host LSP Select. Selects the LSP debug information presented in the GDBGLSP register in host mode.
7:4	RW	0x0	devselect Device LSP Select. Selects the LSP debug information presented in the GDBGLSP register in device mode. Or bit[7:4] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.
3:0	RW	0x0	epselect Device Endpoint Select. Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode. Or bit[3:0] of HOSTSELECT, Selects the LSP debug information presented in the GDBGLSP register in host mode.

usb3otg_GDBGLSP

Address: Operational Base + offset (0xC174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	lspdebug LSP Debug Information.

usb3otg_GDBGEPINFO0

Address: Operational Base + offset (0xC178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	epdebug Endpoint Debug Information Low 32-bit.

usb3otg_GDBGEPINFO1

Address: Operational Base + offset (0xC17C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00800000	epdebug Endpoint Debug Information High 32-bit.

usb3otg_GPRTBIMAP_HSLO

Address: Operational Base + offset (0xC180)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 HS USB Instance Number for Port 1. Application-programmable ID field.

usb3otg_GPRTBIMAP_FSLO

Address: Operational Base + offset (0xC188)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	binum1 FS USB Instance Number for Port 1. Application-programmable ID field.

usb3otg_GUSB2PHYCFG0

Address: Operational Base + offset (0xC200)

Bit	Attr	Reset Value	Description
31	RW	0x0	physoftrst UTMI PHY Soft Reset. Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl. Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset).

Bit	Attr	Reset Value	Description
30	RW	0x1	u2_freeclk_exists Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The core uses the Port-0 clock for generating the internal mac2 clock. 1'b0: USB 2.0 free clock does not exist 1'b1: USB 2.0 free clock exists Note: When the core is configured as device-only, do not set this bit to 1.
29:25	RO	0x00	reserved
24:22	RW	0x0	lstrd LS Turnaround Time. This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h0 (2 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly.

Bit	Attr	Reset Value	Description
21:19	RW	0x2	lsipd LS Inter-Packet Time. This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 3'h0: 2 bit times 3'h1: 2.5 bit times 3'h2: 3 bit times 3'h3: 3.5 bit times 3'h4: 4 bit times 3'h5: 4.5 bit times 3'h6: 5 bit times 3'h7: 5.5 bit times Note: This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h2 (3 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly.
18:14	RO	0x00	reserved
13:10	RW	0x9	usbtrdim USB 2.0 Turnaround Time. Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. Note: This field is valid only in device mode.

Bit	Attr	Reset Value	Description
9	RW	0x0	xcvrdly Transceiver Delay. Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device core comes out of power-off, you must re-initialize this bit with the appropriate value because the core does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	RW	0x0	enblslpm Enable utmi_sleep_n and utmi_l1_suspend_n. The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. Note: This bit must be set high for Port0 if SNPS PHY is used. In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
7	RO	0x0	physel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY. 1'b1: USB 1.1 full-speed serial transceiver.

Bit	Attr	Reset Value	Description
6	RW	0x0	suspendusb20 Suspend USB2.0 HS/FS/LS PHY. When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD/OTG configurations, it is recommended that this bit is set to 0 during coreConsultant configuration. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the core initialization completes. For all other configurations, this bit can be set to 1 during core configuration. Note: In host mode, on reset, this bit is set to 1. Software can override this bit after reset. In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
5	RO	0x0	reserved
4	RO	0x0	ulpi_utmi_sel ULPI or UTMI+ Select. 1'b0: UTMI+ Interface 1'b1: ULPI Interface
3	RW	0x0	phyif If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. 1'b0: 8 bits 1'b1: 16 bits

Bit	Attr	Reset Value	Description
2:0	RW	0x0	tout_cal HS/FS Timeout Calibration. The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times

usb3otg_GUSB3PIPECTL0

Address: Operational Base + offset (0xC2C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	PHYSoftRst USB3 PHY Soft Reset After setting this bit to 1, the software needs to clear this bit.
30	RW	0x0	HstPrtCmpl
29	RW	0x0	U2SSInactP3ok
28	RW	0x0	DisRxDetP3 Disabled receiver detection in P3 0: If PHY is in P3 and Core needs to perform receiver detection, The core performs receiver detection in P3. (Default) 1: If PHY is in P3 and Core needs to perform receiver detection, The core changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3.
27	RW	0x0	Ux_exit_in_Px

Bit	Attr	Reset Value	Description
26	RW	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for the downstream port only. Note: This bit is used by third-party SS PHY. It must be set to 0 for SNPS PHY.
25	RW	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.
24	RW	0x0	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change. Note: This bit must be set to 1 for SNPS PHY. For third-party SS PHY, check with your PHY vendor.
23	RW	0x0	StartRxDetU3RxDet
22	RW	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. DWC_USB3_GUSB3PIPECTL_INIT[23] must be used to start receiver detection manually. This bit can only be used for the downstream port. This bit must be set to 0 for Upstream ports. This feature must not be enabled for normal operation. If you have to use this feature, contact SNPS.
21:19	RW	0x0	DelayP1P2P3 Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.

Bit	Attr	Reset Value	Description
18	RW	0x0	DELAYP1TRANS DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. 1'b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 1'b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit must be set to '1' for SNPS PHY. It is also used by third-party SS PHY.
17	RW	0x0	SUSPENDENABLE
16:15	RW	0x0	DATWIDTH
14	RW	0x0	AbortRxDetInU2
13	RW	0x0	SkipRxDet
12	RW	0x0	LFPSP0Algn LFPS P0 Align When set: 1. The core deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. 2. The core requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with SNPS PHY. For other USB 3.0 Host, Device, and DRD cores, this bit is not required.
11	RW	0x0	P3P2TranOK
10	RW	0x0	P3ExSigP2 P3 Exit Signal in P2 When this bit is set, the core always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some non-SNPS PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It must be set to '0' for SNPS PHY.

Bit	Attr	Reset Value	Description
9	RW	0x0	LFPSFILTER LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.
8	RW	0x0	RX_DETECT_to_Polling_L RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active (VTX-CM-ACPP_ACTIVE <100mv) if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us.
7	RO	0x0	reserved
6	RW	0x0	TX_SWING
5:3	RW	0x0	TX_MARGIN
2:1	RW	0x0	TX_DE_EPPHASIS Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.
0	RW	0x0	ELASTIC_BUFFER_MODE

usb3otg_GTXFIFOSIZn

Address: Operational Base + offset (0xC300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	txfstaddr_n Transmit FIFOn RAM Start Address. This field contains the memory start address for TxFIFOn in 64-bit words.
15:0	RW	0x0042	txfdep_n TxFIFO Depth. This field contains the depth of TxFIFOn in 64-bit words. Minimum value: 32; Maximum value: 32,768.

usb3otg_GRXFIFOSIZn

Address: Operational Base + offset (0xC380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0334	rxfstaddr_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.
15:0	RW	0x0185	rxfdep_n RxFIFOn RAM Start Address. This field contains the memory start address for RxFIFOn in 64-bit words.

usb3otg_GEVNTADRLO0

Address: Operational Base + offset (0xC400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrlo Event Buffer Address. Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

usb3otg_GEVNTADRHI0

Address: Operational Base + offset (0xC404)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	evntadrhi Event Buffer Address. Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

usb3otg_GEVNTSIZ0

Address: Operational Base + offset (0xC408)

Bit	Attr	Reset Value	Description
31	RW	0x0	evntintrptmask Event Interrupt Mask. When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	RO	0x0000	reserved
15:0	RW	0x0000	eventsiz Event Buffer Size in bytes. Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes.

usb3otg_GEVNTCOUNT0

Address: Operational Base + offset (0xC40C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	evntcount Event Count. When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

usb3otg_GHWPARAMS8

Address: Operational Base + offset (0xC600)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000047c	ghwparams8_32_0 ghwparams8

usb3otg_GTXFIFOPRIDEV

Address: Operational Base + offset (0xC610)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	gtxfifopridev Device TxFIFO priority. This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the core is configured to operate in the device mode. The register size corresponds to the number of Device IN endpoints.

usb3otg_GTXFIFOPRIHST

Address: Operational Base + offset (0xC618)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	gtxfifoprihst Host TxFIFO priority. This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

usb3otg_GRXFIFOPRIHST

Address: Operational Base + offset (0xC61C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	grxfifoprihst Host RxFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the core is configured to operate in the host mode (includes DRD and OTG modes). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 2 USB bus instances (1 HS, and 1 FSLS).

usb3otg_GFIFOPRIDBC

Address: Operational Base + offset (0xC620)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	gfifopridbc Host DbC DMA priority. This register specifies the relative priority of the RXFIFOs and TXFIFOs associated with the DbC mode. It overrides the priority assigned in the corresponding indexes of the Host RXFIFO and TXFIFO DMA priority registers, when the DbC mode is enabled.

usb3otg_GDMAHLRATIO

Address: Operational Base + offset (0xC624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:8	RW	0x0000	hstrxfifo Host RXFIFO DMA High-Low Priority.

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4:0	RW	0x00	hsttxfifo Host TXFIFO DMA High-Low Priority.

usb3otg_GFLADJ

Address: Operational Base + offset (0xC630)

Bit	Attr	Reset Value	Description
31	RW	0x0	gfladj_refclk_240mhzdecr_pls1 This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk. Set this bit to a 1 only if GFLADJ_REFCLK_LPM_SEL is set to 1 and the fractional component of 240/ref_frequency is greater than or equal to 0.5. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/24) = 10 3. GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0
30:24	RW	0x00	gfladj_refclk_240mhz_decr This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1. The value is derived as follows: GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10
23	RW	0x0	gfladj_refclk_lpm_sel This bit enables the functionality of running SOF counters on the ref_clk. This bit must not be set to 1 if GCTL.SOFITPSYNC bit is set to 1. Similarly, if GFLADJ_REFCLK_LPM_SEL set to 1, GCTL.SOFITPSYNC must not be set to 1. Note that the ref_clk frequencies supported in this mode are 16/17/19.2/20/24/39.7/40 MHz. The utmi_clk[0] signal of the core must be connected to the FREECLK of the PHY. Note: If you set this bit to 1, the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to 0.
22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21:8	RW	0x0000	gfladj_refclk_fladj This field indicates the frame length adjustment to be applied when SOF counter is running on the ref_clk. SOF interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1 or GCTL.SOFITPSYNC is set to 1. The value is derived as follows: FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer)-(125000/ref_clk_period)) * ref_clk_period where: 1. The ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal (fractional) value that is programmed in the GUCTL.REF_CLK_PERIOD field. 2. The ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then 1. GUCTL.REF_CLK_PERIOD = 41 2. GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/41)-(125000/41.6666))*41.6666 = 2032 (ignoring the fractional value).
7	RW	0x0	gfladj_30mhz_sdbnd_sel This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF. When this bit is set to: 1'b1: the controller uses the register field GFLADJ.GFLADJ_30MHZ value 1'b0: the controller uses the input signal fladj_30mhz_reg value.
6	RO	0x0	reserved
5:0	RW	0x00	gfadj_30mhz This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid. For details on how to set this value, refer to section 5.2.4, "Frame Length Adjustment Register (FLADJ)," of the xHCI Specification.

usb3otg_DCFG

Address: Operational Base + offset (0xC700)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	ignstrmpp This bit only affects stream-capable bulk endpoints. Not applied.

Bit	Attr	Reset Value	Description
22	RW	0x0	lpmcap LPM Capable. Not applied.
21:17	RW	0x04	nump Number of Receive Buffers. Not applied.
16:12	RW	0x00	intrnum Interrupt number. Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts (see DEVT) are generated.
11:10	RO	0x0	reserved
9:3	RW	0x00	devaddr Device Address. The application must perform the following: 1. Program this field after every SetAddress request. 2. Reset this field to zero after USB reset.
2:0	RW	0x0	devspd Device Speed. Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

usb3otg_DCTL

Address: Operational Base + offset (0xC704)

Bit	Attr	Reset Value	Description
31	RW	0x0	run_stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1. After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2. The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. 3. When the USB is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. Note: The following is the minimum duration under various conditions for which the soft disconnect (SftDiscon) bit must be set for the USB host to detect a device disconnect: 10ms: For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions); For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions). To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration.

Bit	Attr	Reset Value	Description
30	R/WSC	0x0	csftrst Core Soft Reset. Reset all clock domains as follows: 1. This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. 2. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. 3. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core, which may take several clocks depending on the core's current state. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain (synchronization delay). Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	RO	0x0	reserved
28:24	RW	0x00	hirdthres HIRD Threshold. The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: 1. HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] 2. HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: 1. If the HIRD value is less than HIRD_Thres[3:0] or 2. HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.

Bit	Attr	Reset Value	Description
23:20	RW	0xf	lpm_nyet_thres LPM NYET Threshold Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The core always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The core responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: 1. There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). 2. No data is pending in the Transmit FIFO and OUT endpoints not in flow controlled state (else NYET). 3. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0].
19	RW	0x0	keep_connect When 1, this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to 0. The device core disconnects from the host when DCTL.RunStop is set to 0. This bit indicates whether to preserve this behavior (0), or if the core must not disconnect when RunStop is set to 0 (1).
18	RW	0x0	l1_hibernation_en When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	RW	0x0	crs Controller Restore State. This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to 1, the controller immediately sets DSTS.RSS to 1. When the controller has finished the restore process, it sets DSTS.RSS to 0. Note: When read, this field always returns 0.

Bit	Attr	Reset Value	Description
16	RW	0x0	css Controller Save State. This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to 1, the controller immediately sets DSTS.SSS to 1. When the controller has finished the save process, it sets DSTS.SSS to 0. Note: When read, this field always returns 0.
15:13	RO	0x0	reserved
12	RW	0x0	initu2ena Not applied.
11	RW	0x0	acceptu2ena Not applied.
10	RW	0x0	initu1ena Not applied.
9	RW	0x0	acceptu1ena Not applied.
8:5	RW	0x0	ulstchngreq Software writes this field to issue a USB state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. In HS/FS/LS mode: Value: Requested USB state transition 8: Remote wakeup request Others: Reserved The Remote wakeup request must be issued 2us after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software must write 8 (Recovery) into this field to confirm exit from the suspended state.
4:1	RW	0x0	tstctl Test Control. 4'b000: Test mode disabled 4'b001: Test_J mode 4'b010: Test_K mode 4'b011: Test_SE0_NAK mode 4'b100: Test_Packet mode 4'b101: Test_Force_Enable Others: Reserved
0	RO	0x0	reserved

usb3otg_DEVTEN

Address: Operational Base + offset (0xC708)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	vendevtstrcvden Vendor Device Test LMP Received Event. 1'b0: Disable this event 1'b1: Enable this event
11:10	RO	0x0	reserved
9	RW	0x0	errticerrevten Erratic Error Event Enable. 1'b0: Disable this event 1'b1: Enable this event
8	RO	0x0	reserved
7	RW	0x0	softevten Start of (u)frame Event Enable. 1'b0: Disable this event 1'b1: Enable this event
6	RW	0x0	u3l2l1_susp_en U3/L2-L1 Suspend Event Enable. 1'b0: Disable this event 1'b1: Enable this event
5	RW	0x0	hibernation_req_evt_en Hibernation Request Event Enable. 1'b0: Disable this event 1'b1: Enable this event
4	RW	0x0	wkupevten Resume/Remote Wakeup Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event
3	RW	0x0	ulstcngen USB State Change Event Enable. 1'b0: Disable this event 1'b1: Enable this event
2	RW	0x0	connectdoneevten Connection Done Event Enable. 1'b0: Disable this event 1'b1: Enable this event
1	RW	0x0	usbrstevten USB Reset Event Enable. 1'b0: Disable this event 1'b1: Enable this event

Bit	Attr	Reset Value	Description
0	RW	0x0	disconnevten Disconnect Detected Event Enable. 1'b0: Disable this event 1'b1: Enable this event

usb3otg_DSTS

Address: Operational Base + offset (0xC70C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	dcnrd Device Controller Not Ready. The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to 1 and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt.
28:26	RO	0x0	reserved
25	RW	0x0	rss Restore State Status. This bit is similar to the USBSTS.RSS in host mode. When the controller finishes the restore process, it completes the command by setting DSTS.RSS to 0.
24	RO	0x0	sss Save State Status. This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to 0.
23	RO	0x0	coreidle Core Idle. The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.

Bit	Attr	Reset Value	Description
22	RO	0x1	devctrlhlt Device Controller Halted. This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to 0, the core is idle and the lower layer finishes the disconnect process. When Halted=1, the core does not generate Device events. Note: The core does not set this bit to 1 if GEVNTCOUNTn has some valid value. Software needs to acknowledge the events that are generated (by writing to GEVNTCOUNTn) while it is waiting for this bit to be set to 1.
21:18	RO	0x4	usblnkst In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state (Default state) 4'h5: Early Suspend state (valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0) 4'he: Reset (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) 4'hf: Resume (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) The link state Resume/Reset indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write 8 (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to 1 and DSTS[29].DCNRD = 0.
17	RO	0x1	rx_fifo_empty Rx Fifo Empty.
16:3	RO	0x0000	reserved
2:0	RU	0x0	connectspd Connected Speed. Indicates the speed at which the DWC_usb3 core has come up after speed detection through a chirp sequence. 3'b000: High-speed (PHY clock is running at 30 or 60 MHz) 3'b001: Full-speed (PHY clock is running at 30 or 60 MHz)

usb3otg_DGCMDPAR

Address: Operational Base + offset (0xC710)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the device command parameter. This must be programmed before or along with the device command. The available device commands are listed in DGCMD register.

usb3otg_DGCMD

Address: Operational Base + offset (0xC714)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	cmdstatus Command Status: 1'b1: CmdErr: Indicates that the device controller encountered an error while processing the command. 1'b0: Indicates command success
11:10	RO	0x0	reserved
9	R/WSC	0x0	cmdact Command Active. The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:0	RW	0x00	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 8'h0: Reserved 8'h1: Set Endpoint Configuration - 64 or 96-bit Parameter 8'h2: Set Endpoint Transfer Resource Configuration - 32-bit Parameter 8'h3: Get Endpoint State - No Parameter Needed 8'h4: Clear Stall (see Set Stall) - No Parameter Needed 8'h5: Start Transfer - 64-bit Parameter 8'h6: Update Transfer - No Parameter Needed 8'h7: End Transfer - No Parameter Needed 8'h8 Start New Configuration - No Parameter Needed

usb3otg_DALEPENA

Address: Operational Base + offset (0xC720)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbactep USB Active Endpoints. This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0~15 and OUT endpoints 0~15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Hardware clears these bits for all endpoints (other than EP0-OUT and EP0-IN) after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits.

usb3otg_DEPnCMDPAR2

Address: Operational Base + offset (0xC800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

usb3otg_DEPnCMDPAR1

Address: Operational Base + offset (0xC804)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

usb3otg_DEPnCMDPAR0

Address: Operational Base + offset (0xC808)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	parameter This register indicates the physical endpoint command Parameter 0. It must be programmed before issuing the command.

usb3otg_DEPnCMD

Address: Operational Base + offset (0xC80C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	commandparam Command Parameters or Event Parameters when this register is written: For Start Transfer command: The 16-bit StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: StartMicroFramNum, Indicates the (micro) frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. Event Parameters (EventParam), when this register is read.
15:12	RW	0x0	cmdstatus Command Completion Status. The information is in the same format as bits 15:12 of the Endpoint Command Complete event.
11	RW	0x0	hipri_forcerm HighPriority: Only valid for Start Transfer command. ForceRM: Only valid for End Transfer command. ClearPendIN: Only valid for Clear Stall command. Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	RW	0x0	cmdact Command Active. Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	RO	0x0	reserved
8	RW	0x0	cmdioc Command Interrupt on Complete. When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to 1 if the DCTL.RunStop field is 0.
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	cmdtyp Command Type. Specifies the type of command the software driver is requesting the core to perform. 4'h0: Reserved 4'h1: Set Endpoint Configuration - -64 or 96-bit Parameter 4'h2: Set Endpoint Transfer Resource Configuration - 32-bitparameter 4'h3: Get Endpoint State - No Parameter Needed 4'h4: Set Stall - No Parameter Needed 4'h5: Clear Stall (see Set Stall) - No Parameter Needed 4'h6: Start Transfer - 64-bit Parameter 4'h7: Update Transfer - No Parameter Needed 4'h8: End Transfer - No Parameter Needed 4'h9: Start New Configuration - No Parameter Needed

17.5 Interface Description

Table 17-1 USB2.0 PHY and SS PHY Interface Description

Module Pin	Dir.	Pin Name	Descriptions
USB0ID	I/O	USB3OTG_ID	USB3 OTG usb2 part pad
USB0PN	I/O	USB3OTG_DM	USB3 OTG usb2 part pad
USB0PP	I/O	USB3OTG_DP	USB3 OTG usb2 part pad
VBUS	I/O	USB3OTG_VBUS	USB3 OTG usb2 part pad
PIPE0TXP	I/O	USB3OTG_TXP	USB3 OTG usb3 part pad
PIPE0TXN	I/O	USB3OTG_TXN	USB3 OTG usb3 part pad
PIPE0RXP	I/O	USB3OTG_RXP	USB3 OTG usb3 part pad
PIPE0RXN	I/O	USB3OTG_RXN	USB3 OTG usb3 part pad
USB1PN	I/O	USB3HOST_DM	USB3 Host usb2 part pad
USB1PP	I/O	USB3HOST_DP	USB3 Host usb2 part pad
PIPE1TXP	I/O	USB3HOST_TXP	USB3 Host usb3 part pad
PIPE1TXN	I/O	USB3HOST_TXN	USB3 Host usb3 part pad
PIPE1RXP	I/O	USB3HOST_RXP	USB3 Host usb3 part pad
PIPE1RXN	I/O	USB3HOST_RXN	USB3 Host usb3 part pad

17.6 Application Notes

17.6.1 Some Special Settings before Initialization

Set USB3.0 OTG controller AXI master secure setting.
Set PHYIF to 1 to use 16-bit UTMI+ interface (see register GUSB2PHYCFG0)
Clear ENBLSLPM to 0 to disable sleep and l1 suspend (see register GUSB2PHYCFG0)
Clear U2_FREECLK_EXITSTS to 0 (see register GUSB2PHYCFG0)
Clear DEV_FORCE_20_CLK_FOR_30_CLK to 0 (see register GUCTL1)
Clear DELAYP1TRANS to 0 (see register GUSB3PIPECTL0)
Hold USB3.0 controller in resetting during USB3PHY initialization

17.6.2 OTG Programming Model

When detect ID change event (see USBPHY_GRF) or VBUS change event (see USBPHY_GRF) after disconnect, it means a USB3/2 OTG A device or B device may connect, then check status of ID(see USBPHY_GRF). If ID==0, it will work as A device, then follow host programming flow; if ID==1, it will work as B device, then it follows device programming flow.
Note: USB3.0 OTG doesn’t support host/device mode swapping through HNP and RSP.
Note: SS PHY is combo PHY, it may share with other protocol PHY, when other protocol PHY is on, USB3.0 OTG can only work on usb2.0 mode.

Chapter 18 PCIe Controller

18.1 Overview

The PCI Express (PCIe) is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. The PCIe designed to be used as a general-purpose serial I/O interconnect in multiple market segments, including desktop, mobile, server, storage, and embedded communications. It is compliant with PCI Express Specifications 1.1, 2.1. The PCIe subsystem is consist of three Controllers, one 2-lane Gen3 PHY with bifurcation, and one 1-lane Gen2 PHY combo with SATA/PCS.
PCIe subsystem supports the following features:

- Compatible with PCI Express Base Specification Revision 3.0
- Support 1 DM (Dual-Mode) 2-lane PCIe 3.0 Gen3 controller: Root Complex (RC) and Endpoint (EP)
- Support 1 RC only mode 1-lane PCIe 3.0 Gen3 controller: Root Complex (RC)
- Support 1 RC only mode 1-lane PCIe 3.0 Gen2 controller: Root Complex (RC)
- Maximum link width is 2, single bi-directional Link interface
- Maximum Payload Size of 256 bytes
- Maximum 32 Non-Posted outstanding transactions
- Support 2.5GT/s, 5.0 GT/s, 8.0GT/s serial data transmission rate per lane per direction
- Support 100MHz differential clock output (optional with SSC) for system application
- Embedded DMA with Hardware Flow Control in DM controller
- Support Latency Tolerance Reporting (LTR)
- Support Optimized Buffer Flush and Fill (OBFF)
- Support Resizable BAR Capability
- Support Single Physical PCI Function in Endpoint Mode
- Support Legacy Interrupt
- Support MSI with Per-Vector Masking (PVM) and 32 multiple MSI
- Support MSI-X with Per-Vector Masking (PVM) and 64 MSI-X table size
- Support ECRC Generation and Checking
- Support Outbound and Inbound address translation
- Support Dynamic Power Allocation Capability (DPA)
- Support PCI Express Active State Power Management (ASPM) state L0s and L1
- Support L1 Power Management Substate
- Support PCI Function power states D0, D1 and D3, and the corresponding link power states L0, L1 and L2
- Support RAS DES (Debug, Error Injection, and Statistics)
- Support Automatic Lane Reversal
- Support PCI Express Advanced Error Reporting (AER) with Header Logging

18.2 Block Diagram

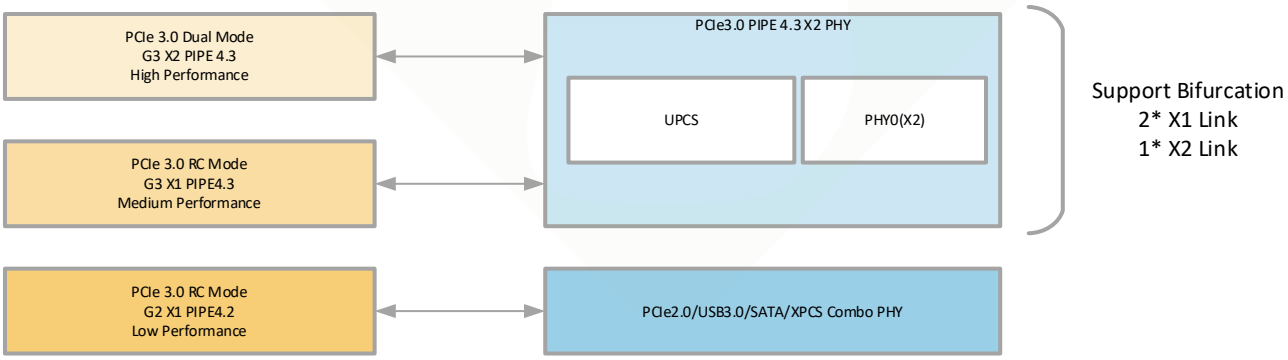


Fig. 18-1 PCIe Block Diagram

18.3 Function Description

18.3.1 Application Interface and AXI Bridge

Application Interface comprises with four standard interfaces: one AXI master interface, two AXI slave interface and one APB interface. These interface bridging capability for directly adding a PCI Express link to an AXI system fabric.

The AXI bridge module acts as a bridge between the standard AXI interfaces and the PCIe controller native interfaces. The bridge interconnects the AXI interfaces within an AXI-embedded system with a remote PCIe link, as either a root complex port or as an endpoint port.

The AXI master interfaces enable a remote PCIe device to read and write to an AXI slave connected to the AXI bridge. The AXI link slave interface enables an AXI master to read and write through the AXI bridge to a remote PCIe device. The DBI slave enables an AXI master to access the controller's registers. The APB enables Application to access the client registers.

18.3.2 Client Logic

Client Logic Consists of some additional logic used for application to interact with PCIe Controller. For example, applications can access client registers to send/receive PCIe Message, request to enter/exit PM state, deal with interrupts, configure some basic operation mode, read some basic debug information, and so on. For more details, please refer to client registers description and application notes for more information.

18.3.3 Embedded DMA

The RC system CPU, or the EP application CPU, can offload the transferring of large blocks of data to the embedded DMA controller, leaving the CPU free to perform other tasks. The embedded DMA have one read channel and one write channel. It can simultaneously perform the two types of memory transactions:

DMA write: Transfer (copy) of a block of data from local (application) memory to remote (link partner) memory.

DMA read: Transfer (copy) of a block of data from remote (link partner) memory to local (application) memory.

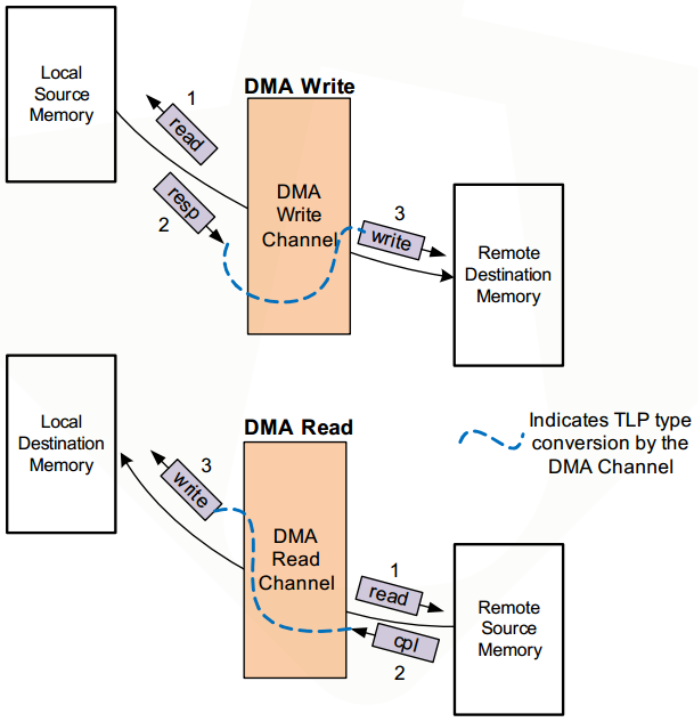


Fig. 18-2 System Level View of PCIe EDMA

Therefore, the EDMA supports full duplex operation, processing read and write transfers at the same time, and in parallel with normal (non-DMA) traffic. Upon completion of a DMA transfer or an error, the DMA optionally interrupts the local CPU or sends an interrupt MWr (Memory Write) to the remote CPU. The DMA is highly configurable and can be programed

by using the local DBI AXI Slave interface.
The EDMA provides a linked list (LL) mode to efficiently move data from source to destination with minimal intervention from the local CPU. For details, please refer to DMA Registers Description and Application notes for more information.

18.3.4 PCIe Core

PCIe Core deal with the PCIe protocol, and consists of three main modules:

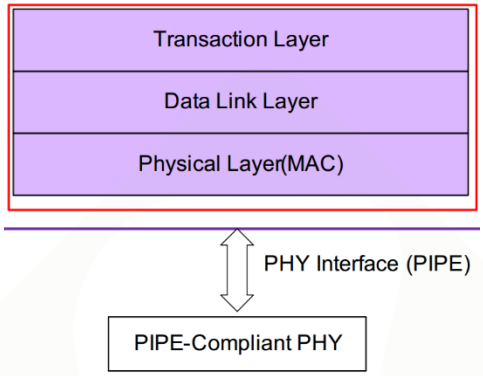


Fig. 18-3 PCIe Core Architecture Overview

The PCIe Core implements the basic functionality for the PCI Express physical, link, and transaction layers. This module implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The Core connects to the external PHY through the standard PIPE interface.

18.3.5 Power Management

PCIe Controller support PCIe ASPM, L1 Substate and PCI PM. For proper understanding of PCIe Power Management, you should be familiar with Chapter 5, Power Management of the PCI Express Base Specification, and PCI-SIG Engineering Change Notice ECN L1 Substates with CLKREQ#. For application details, please refer to Application Notes for more information.

18.3.6 PCIe 2.0 PHY

PCIe Controller shares a combo PHY with USB 3.0 Controller. The PCIe PHY, which consists of Physical Coding Sub-layer(PCS) and Physical Media Attachment Layer(PMA), includes all circuitry for interface operation, including 8/10 encoding/decoding, driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. The PHY provides standard PIPE interface with the Media Access Layer for exchanging information. This PHY is responsible for converting information received from the PCIe Core into an appropriate serialized format and transmitting it across the PCIe Link at a frequency and width compatible with the device connected to the other side of the Link.

18.4 Register Description

PCIe Registers can be accessed by either local CPU through AXI Dbi bus or remote RC device through PCIe link or both. The way through local CPU will be mentioned as 'Dbi' and the way through PCIe link will be mentioned as 'wire' in this section.
Some read-only registers can be made temporarily R/W when you write 1 to the DBI_RO_WR_EN bit of the MISC_CONTROL_1_OFF register. These registers will be specifically mentioned in their description if they have this feature.

18.4.1 Internal Address Mapping

PCIe local address mapping is discussed in this section.

Table 18-1 PCIe X2 DM G3 Client and Core Register Address Mapping

Base Address	Device	Address Length	Offset Address Range
0xF6000000	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF0000000	PCIe Outbound	32M BYTE	0x0000000~0x1ffffff

	Memory		
0xFE280000	Client Register	64K BYTE	0x0000~0xffff
0xFDC50000	PD PIPE GRF	64K BYTE	0x0000~0xffff
0xFDCB8000	PHY GRF	32K BYTE	0x0000~0x7fff
0xFE8C0000	PHY Register	128K BYTE	0x0000~0x1ffff

Table 18-2 PCIe X1 RC G3 Client and Core Register Address Mapping

Base Address	Device	Address Length	Offset Address Range
0xF6400000	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF2000000	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0xFE270000	Client Register	64K BYTE	0x0000~0xffff
0xFDC50000	PD PIPE GRF	64K BYTE	0x0000~0xffff
0xFDCB8000	PHY GRF	32K BYTE	0x0000~0x7fff
0xFE8C0000	PHY Register	128K BYTE	0x0000~0x1ffff

Table 18-3 PCIe X1 RC G2 Client and Core Register Address Mapping

Base Address	Device	Address Length	Offset Address Range
0xF6800000	Core Register	4M BYTE	0x00000 ~ 0x3fffff
0xF4000000	PCIe Outbound Memory	32M BYTE	0x0000000~0x1ffffff
0xFE260000	Client Register	64K BYTE	0x0000~0xffff
0xFDC50000	PD PIPE GRF	64K BYTE	0x0000~0xffff
0xFDC90000	PHY GRF	64K BYTE	0x0000~0xffff
0xFE840000	PHY Register	64K BYTE	0x0000~0xffff

Core Register map is as follows:
RC mode:

Table 18-4 PCIe Core Register Map in RC mode

Offset Address Range	Register Block	Description
0x0000~0x003c	TYPE1_HDR	PCI-Compatible Configuration Space Header Type1
0x0040~0x0044	PM_CAP	PCI Power Management Capability Structure
0x0050~0x0064	MSI_CAP	MSI Capability Structure
0x0070~0x00a0	PCIE_CAP	PCI Express Capability Structure
0x00b0~0x00b8	MSIX_CAP	MSI-X Capability Structure
0x0100~0x0144	AER_CAP	Advanced Error Reporting Capability Structure
0x0148~0x0154	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0160~0x016c	L1SUB_CAP	L1 Substates Capability Structure
0x01a0~0x0288	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x0700~0x0b90	PORT_LOGIC	Port Logic
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability

		Structure
0x300000~0x301f14	ATU_CAP	ATU Port Logic Structure
0x380000~0x380320	DMA_CAP	DMA Port Logic Structure

EP mode:

Table 18-5 PCIe Core Register Map in EP mode

Offset Address Range	Register Block	Description
0x0000~0x003c	TYPE0_HDR	PCI-Compatible Configuration Space Header Type0
0x0040~0x0044	PM_CAP	PCI Power Management Capability Structure
0x0050~0x0064	MSI_CAP	MSI Capability Structure
0x0070~0x00a0	PCIE_CAP	PCI Express Capability Structure
0x00b0~0x00b8	MSIX_CAP	MSI-X Capability Structure
0x0100~0x0144	AER_CAP	Advanced Error Reporting Capability Structure
0x0148~0x0154	SPCIE_CAP	Secondary PCI Express Capability Structure
0x0158~0x015c	LTR_CAP	Latency Tolerance Reporting Capability Structure
0x0160~0x016c	L1SUB_CAP	L1 Substates Capability Structure
0x0170~0x0184	DPA_CAP	DPA Capability Structure
0x01a0~0x0288	RAS_DES_CAP	RAS D.E.S. Capability Structure
0x02a0~0x02d0	RESBAR_CAP	Resizable BAR Capability Structure
0x0700~0x0b90	PORT_LOGIC	Port Logic
0x1000b0	MSIX_CAP_DBI2	Shadow Block: MSI-X Capability
0x300000~0x301f14	ATU_CAP	ATU Port Logic Structure
0x380000~0x380320	DMA_CAP	DMA Port Logic Structure

18.4.2 PCIe Client Registers Summary

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_GENERAL_CON	0x0000	W	0x00000000	General Control Register
PCIE_CLIENT_INTR_STATUS_MSG_RX	0x0004	W	0x00000000	Interrupt Status Register Related to Message Reception
PCIE_CLIENT_INTR_STATUS_LEGACY	0x0008	W	0x00000000	Interrupt Status Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_STATUS_ERR	0x000C	W	0x00000000	Interrupt Status Register Related to Error Detection
PCIE_CLIENT_INTR_STATUS_MISC	0x0010	W	0x00000000	Interrupt Status Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_STATUS_PMC	0x0014	W	0x00000000	Interrupt Status Register Related Power Management Control
PCIE_CLIENT_INTR_MASK_MSG_RX	0x0018	W	0x00007737	Interrupt Mask Register Related to Message Reception
PCIE_CLIENT_INTR_MASK_LEGACY	0x001C	W	0x000000FF	Interrupt Mask Register Related to Legacy Interrupt
PCIE_CLIENT_INTR_MASK_ERR	0x0020	W	0x0000177F	Interrupt Mask Register Related to Error Detection
PCIE_CLIENT_INTR_MASK_MISC	0x0024	W	0x00007FFF	Interrupt Mask Register Related to Miscellaneous Operation
PCIE_CLIENT_INTR_MASK_PMC	0x0028	W	0x000001FF	Interrupt Mask Register Related Power Management Control

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_POWER_CON	0x002C	W	0x00000008	Power Management Control Register
PCIE_CLIENT_POWER_STATUS	0x0030	W	0x00000000	Power Management Status Register
PCIE_CLIENT_MSG_GEN_CON	0x0034	W	0x00000000	Message Generation Control Register
PCIE_CLIENT_MSI_GEN_CON	0x0038	W	0x00000000	MSI Generation Control Register
PCIE_CLIENT_MSI_GEN_FNUM_TC	0x0040	W	0x00000000	MSI Function Number and TC set Register
PCIE_CLIENT_RBAR_SIZE_INFO0	0x0044	W	0x00000000	Resizable BAR2 to BAR0 Size Information Register
PCIE_CLIENT_RBAR_SIZE_INFO1	0x0048	W	0x00000000	Resizable BAR5 to BAR3 Size Information Register
PCIE_CLIENT_DMA_HSHAKE_TOGG	0x004C	W	0x00000000	DMA Handshake Toggle Register
PCIE_CLIENT_VEN_MSG_RX_INFO0	0x0050	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO1	0x0054	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_RX_INFO2	0x0058	W	0x00000000	Register That Contains Header Information of Vendor Message That Controller Received
PCIE_CLIENT_VEN_MSG_TX_CFG0	0x005C	W	0x00000000	Vendor Message Transmit Configuration Register 0
PCIE_CLIENT_VEN_MSG_TX_CFG1	0x0060	W	0x00000000	Vendor Message Transmit Configuration Register 1
PCIE_CLIENT_VEN_MSG_TX_CFG2	0x0064	W	0x00000000	Vendor Message Transmit Configuration Register 2
PCIE_CLIENT_LTR_MSG_TX_INFO	0x0068	W	0x00000000	LTR Message Transmit Data Register
PCIE_CLIENT_APP_ERR_RPT_INFO0	0x006C	W	0x00000000	Application Error Report Information Register 0
PCIE_CLIENT_APP_ERR_RPT_INFO1	0x0070	W	0x00000000	Application Error Report Information Register 1
PCIE_CLIENT_APP_ERR_RPT_INFO2	0x0074	W	0x00000000	Application Error Report Information Register 2
PCIE_CLIENT_APP_ERR_RPT_INFO3	0x0078	W	0x00000000	Application Error Report Information Register 3
PCIE_CLIENT_APP_ERR_RPT_INFO4	0x007C	W	0x00000000	Application Error Report Information Register 4
PCIE_CLIENT_OBFF_WAKE_ELE_CFG	0x0080	W	0xB4F05064	OBFF Wake Configuration Register
PCIE_CLIENT_OBFF_WAKE_DEBUG	0x0084	W	0x00000000	OBFF Wake Decoder Debug Register
PCIE_CLIENT_RX_CPL_TIME_OUT_INFO	0x0088	W	0x00000000	RX CPL Timeout Information
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0	0x008C	W	0x00000000	RX CPL Timeout Information 0
PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1	0x0090	W	0x00000000	RX CPL Timeout Information 1

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_LOCAL_CRU_CTRL	0x009C	W	0x00000000	Local Clock and Reset Control Register
PCIE_CLIENT_GENERAL_DEBUG_CON	0x0100	W	0x00000000	General Debug Control Register
PCIE_CLIENT_GENERAL_DEBUG_INFO	0x0104	W	0x00000000	General Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_COMMON	0x0108	W	0x00000000	Common Silicon Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_LN	0x010C	W	0x00000000	Lane N Silicon Debug Information Register
PCIE_CLIENT_SLC_DEBUG_INFO_V0	0x0114	W	0x00000000	Virtual Channel 0 Silicon Debug Information Register
PCIE_CLIENT_DIAG_STATUS_BUS_SEL	0x0118	W	0x00000000	Diagnostic Status Bus Select Register
PCIE_CLIENT_DIAG_STATUS_BUS_INFO	0x011C	W	0x00000000	Diagnostic Status Bus Information Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CON	0x0140	W	0x00000000	CDM RASDES Control Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN	0x0144	W	0x00000000	CDM RASDES Information Common Data Register
PCIE_CLIENT_CDM_RASDES_EC_INFO_LN	0x0148	W	0x00000000	Lane N CDM RASDES Information Register
PCIE_CLIENT_CDM_RASDES_TBA_CON	0x0150	W	0x00000000	CDM RASDES TBA Control Register
PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN	0x0154	W	0x00000000	CDM RASDES TBA Common Information Register
PCIE_CLIENT_HOT_RESET_CTRL	0x0180	W	0x00000000	Hot Reset Control Register
PCIE_CLIENT_AXI_MSTR_MISC_CON	0x0200	W	0x00000000	AXI Master Sideband Signals Control Register
PCIE_CLIENT_AXI_SLV_ATU_BYPASS	0x0204	W	0x00000000	Address Translate Unit Bypass set Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR	0x0208	W	0x00000000	AXI Slave Write Address Sideband Signals HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR3	0x020C	W	0x00000000	AXI Slave Write Address Sideband Signals 3rd HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_HDR4	0x0210	W	0x00000000	AXI Slave Write Address Sideband Signals 4th HDR Register
PCIE_CLIENT_AXI_SLV_AWMISC_TAG	0x0214	W	0x00000000	AXI Slave Write Request Tag Register
PCIE_CLIENT_AXI_SLV_MISC_INFO	0x0218	W	0x00000000	AXI Slave Read Address and Write Data Sideband Signals Control Register
PCIE_CLIENT_DBI_MISC_CON	0x0270	W	0x00000000	DBI Miscellaneous Control Register
PCIE_CLIENT_PORT_BDF	0x0274	W	0x00000000	Port BDF Register
PCIE_CLIENT_LTSSM_STATUS	0x0300	W	0x00000000	LTSSM Status Register
PCIE_CLIENT_DBG_FIFO_MODE_CON	0x0310	W	0x00000000	Debug FIFO Mode Control Register
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0	0x0320	W	0x00000000	Debug FIFO Pattern hit Data Register 0

Name	Offset	Size	Reset Value	Description
PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1	0x0324	W	0x00000000	Debug FIFO Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0	0x0328	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 0
PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1	0x032C	W	0x00000000	Debug FIFO Transition Pattern hit Data Register 1
PCIE_CLIENT_DBG_FIFO_STATUS	0x0350	W	0x00000000	Debug FIFO Status Register
PCIE_CLIENT_CFG_ERR_STATUS	0x0354	W	0x00000000	Configuration Error Status
PCIE_CLIENT_CLIENT_VER	0x0800	W	0x0000C5A8	Client Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 PCIe Client Detail Registers Description

PCIE_CLIENT_GENERAL_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	link_req_rst_grt_sel Link down reset request grant control select: 1'b1: From client grf GENERAL_CON bit 3 1'b0: From pcie grf PCIE_CON0 bit 2
12	WO	0x0	app_err_repot Set 1 to repor application error to controller. It is a self-clear bit to generate a pulse to controller. Application should provide error information in VEN_ERR_INFOx registers before setting this bit.
11	RW	0x0	app_sris_mode SRIS operating mode 1'b0: non-SRIS mode 1'b1: SRIS mode
10	RW	0x0	app_dbi_ro_wr_disable 1'b0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1'b1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only
9	RW	0x0	tx_lane_flip_en Performs manual lane reversal for transmit lanes. Used when automatic lane reversal does not occur. 1'b1: enable 1'b1: disable
8	RW	0x0	rx_lane_flip_en Performs manual lane reversal for receive lanes. Used when automatic lane reversal does not occur. 1'b1: enable 1'b1: disable

Bit	Attr	Reset Value	Description
7:4	RW	0x0	device_type Device/port type. Indicates the specific type of this PCI Express function. It is also used to set the 'Device/Port Type' field of the 'PCI Express Capabilities Register'. The controller uses this input to determine the operating mode of the controller at run time. Defined encodings are: 4'b0000: PCI Express endpoint 4'b0001: Legacy PCI Express endpoint 4'b0100: Root port of PCI Express root complex
3	RW	0x0	link_req_rst_grt Link down reset request grant control. 1'b1: enable link down reset request grant 1'b0: disable link down reset request grant
2	RW	0x0	ltssm_enable Driven low by your application after cold, warm, or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to delay hot resetting of the controller until you have read out any register status.
1	RW	0x0	app_req_retry_en Provides a capability to defer incoming configuration requests until initialization is complete. When app_req_retry_en is asserted, the controller completes incoming configuration requests with a configuration request retry status. Other incoming requests complete normally.
0	RW	0x0	app_init_rst Set "1" to send a hot reset to link partner. It is a self-clear bit to generate a hot reset pulse to controller. Only used in RC mode.

PCIE_CLIENT_INTR_STATUS_MSG_RX

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	W1C	0x0	obff_cpu_active_int Interrupt indicates that the controller received an 'CPU Active' OBFF message. 1'b0: no interrupt 1'b1: interrupt EP only.
13	W1C	0x0	obff_obff_int Interrupt indicates that the controller received an 'OBFF' OBFF message. 1'b0: no interrupt 1'b1: interrupt EP only.
12	W1C	0x0	obff_idle_int Interrupt indicates that the controller received an 'IDLE' OBFF message. 1'b0: no interrupt 1'b1: interrupt EP only.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	W1C	0x0	pm_turnoff_int Interrupt indicates that the controller received a PME Turnoff message. 1'b0: no interrupt 1'b1: interrupt EP mode only.
9	W1C	0x0	pm_to_ack_int Interrupt indicates that the controller received a PME_TO_Ack message. 1'b0: no interrupt 1'b1: interrupt RC mode only.
8	W1C	0x0	pm_pme_int Interrupt indicates that the controller received a PM_PME message. 1'b0: no interrupt 1'b1: interrupt RC mode only.
7:6	RO	0x0	reserved
5	W1C	0x0	pme_msi Asserted when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. The PME Interrupt Enable bit in Root Control register is set to 1. 3. The PME Status bit in Root Status register is set to 1. Note the difference between pme_msi and pme_int is that aer_rc_err_int is read only and rc_err_msi can be wroten 1 to clear.
4	RO	0x0	pme_int Asserted when all of the following conditions are true: The INTx Assertion Disable bit in the Command register is 0. The PME Interrupt Enable bit in the Root Control register is set to 1. The PME Status bit in the Root Status register is set to 1. This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.
3	RO	0x0	reserved
2	W1C	0x0	ltr_msg_int Interrupt that indicates the controller received a LTR message. The LTR message information is available in PL_LTR_LATENCY_OFF registers. 1'b0: no interrupt 1'b1: interrupt
1	W1C	0x0	unlock_int Interrupt indicates that the controller received an Unlock message. 1'b0: no interrupt 1'b1: interrupt
0	W1C	0x0	ven_msg_int Interrupt that indicates the controller received a vendor-defined message. The message header is available in VEN_MSG_RX_INFO registers. 1'b0: no interrupt 1'b1: interrupt

PCIE_CLIENT_INTR_STATUS_LEGACY

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	tx_intd_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTD Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTD Message to the upstream device. EP mode only.
6	RO	0x0	tx_intc_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTC Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTC Message to the upstream device. EP mode only.
5	RO	0x0	tx_intb_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTB Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTB Message to the upstream device. EP mode only.
4	RO	0x0	tx_inta_int Emulation of sending the legacy PCI Interrupts. 1'b0 to 1'b1: The controller has sent an Assert_INTA Message to the upstream device. 1'b1 to 1'b0: The controller has sent an Deassert_INTA Message to the upstream device. EP mode only.
3	RO	0x0	rx_intd_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTD Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTD Message from the downstream device. RC mode only.
2	RO	0x0	rx_intc_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTC Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTC Message from the downstream device. RC mode only.
1	RO	0x0	rx_intb_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTB Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTB Message from the downstream device. RC mode only.

Bit	Attr	Reset Value	Description
0	RO	0x0	rx_inta_int Emulation of reception of the legacy PCI Interrupts. RC mode only. 1'b0 to 1'b1: The controller received an Assert_INTA Message from the downstream device. 1'b1 to 1'b0: The controller received an Deassert_INTA Message from the downstream device. RC mode only.

PCIE_CLIENT_INTR_STATUS_ERR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	radm_qoverflow_int Interrupt indicates that one or more of the P/NP/CPL receive queues have overflowed. 1'b0: no interrupt 1'b1: interrupt
11	RO	0x0	reserved
10	W1C	0x0	f_err_rx_int Interrupt indicates that the controller received an ERR_FATAL message. 1'b0: no interrupt 1'b1: interrupt EP mode only.
9	W1C	0x0	nf_err_rx_int Interrupt indicates that the controller received an ERR_NONFATAL message. 1'b0: no interrupt 1'b1: interrupt EP mode only.
8	W1C	0x0	cor_err_rx_int Interrupt indicates that the controller received an ERR_COR message. 1'b0: no interrupt 1'b1: interrupt EP mode only.
7	RO	0x0	reserved
6	W1C	0x0	f_err_sent_int EP has sent a message towards the Root Complex indicating that the EP has received a TLP that contained a fatal error. 1'b0: no interrupt 1'b1: interrupt EP mode only.
5	W1C	0x0	nf_err_sent_int EP has sent a message towards the Root Complex indicating that the EP has received a TLP that contained a non-fatal error. 1'b0: no interrupt 1'b1: interrupt
4	W1C	0x0	cor_err_sent_int EP has sent a message towards the Root Complex indicating that the EP has received a TLP that contained a correctable error. 1'b0: no interrupt 1'b1: interrupt

Bit	Attr	Reset Value	Description
3	W1C	0x0	tx_cpl_timeout_int Interrupt indicates that the application has not generated a completion for an incoming request within the required time interval. The default completion timeout value is approximately 10 ms.
2	W1C	0x0	rx_cpl_timeout_int Interrupt indicates that the completion TLP for a request has not been received within the expected time window. 1'b0: no interrupt 1'b1: interrupt You can find the timed out completion information in RX_CPL_TIME_OUT_INFO register.
1	W1C	0x0	aer_rc_err_msi Interrupt asserted cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: 1. MSI or MSI-X is enabled. 2. A reported error condition causes a bit to be set in the Root Error Status register. 3. The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector is unmasked. Note the difference between aer_rc_err_msi and aer_rc_err_int is that aer_rc_err_int is read only and rc_err_msi can be wroten 1 to clear. RC mode only.
0	RO	0x0	aer_rc_err_int Interrupt sserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi. RC mode only.

PCIE_CLIENT_INTR_STATUS_MISC

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ep_elbi_app_int Interrupt generated by ELBI app. 1'b1: interrupt 1'b0: no interrupt
14	RO	0x0	link_eq_req_int Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set. 1'b1: interrupt 1'b0: no interrupt

Bit	Attr	Reset Value	Description
13	W1C	0x0	rbar_updata_int Interrupt indicates that a resizable BAR control register has been updated. 1'b1: interrupt 1'b0: no interrupt
12	W1C	0x0	dpa_sub_upd_int Interrupt asserted when the Substate Control field of the DPA Control Register has been updated with a new value. The controller asserts it when the updated value of the Substate Control field does not match the Substate Status field of the Status Register when the Substate Control Enable bit field of the Status Register is set to "1".
11	RO	0x0	edma_rd_int DMA read channel interrupt. Indicates that the DMA read transfer has completed or that an error has occurred. 1'b0: no interrupt 1'b1: interrupt
10	RO	0x0	edma_wr_int DMA write channel interrupt. Indicates that the DMA write transfer has completed or that an error has occurred. 1'b0: no interrupt 1'b1: interrupt
9	W1C	0x0	bw_mgt_msi Interrupt asserted when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated 3. The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. RC mode only.
8	RO	0x0	bw_mgt_int Interrupt asserted when all the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0 2. The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1 3. The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. RC mode only.
7	W1C	0x0	link_auto_bw_msi The controller sets this pin when following conditions are true: 1. MSI or MSI-X is enabled. 2. The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. 3. The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. RC mode only.

Bit	Attr	Reset Value	Description
6	RO	0x0	link_auto_bw_int Interrupt asserted when all the following conditions are true: 1. The INTx assertion disable bit in the Command register is 0, and 2. The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and 3. The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. RC mode only.
5	W1C	0x0	hp_msi Interrupt asserted when following conditions are true: 1. MSI or MSI-X is enabled. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. RC mode only.
4	RO	0x0	hp_int Interrupt asserted when all the following conditions are true: 1. The INTx Assertion Disable bit in the Command register is 0. 2. Hot-Plug interrupts are enabled in the Slot Control register. 3. Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. hp_int stays asserted if the status bit is set. RC mode only.
3	W1C	0x0	hp_pme_int Interrupt asserted when all the following conditions are true: 1. The PME Enable bit in the Power Management Control and Status register is set to 1. 2. Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. In addition, it asserts hp_pme only if PME is enabled, but it does not matter if hot-plug interrupts are enabled. RC mode only.
2	W1C	0x0	link_req_rst_not_int Interrupt for reset request because the link has gone down, or the controller received a hot-reset request. 1'b1: interrupt 1'b0: no interrupt
1	W1C	0x0	dll_link_up_int Data link layer up/down status interrupt: 1'b1: Data link layer is up 1'b0: Data link layer is down
0	W1C	0x0	phy_link_up_int PHY Link up/down status interrupt: 1'b1: Link is up 1'b0: Link is down

PCIE_CLIENT_INTR_STATUS_PMC

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1C	0x0	pm_dstate_update_int Interrupt indicates that the current power management D-state have changed. 1'b1: interrupt 1'b0: no interrupt
7	W1C	0x0	linkst_out_l0s_int Interrupt that indicates link has left L0s state (falling edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
6	W1C	0x0	linkst_out_l2_int Interrupt that indicates link has left L2 state (falling edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
5	W1C	0x0	linkst_out_l1_int Interrupt that indicates link has left L1 state (falling edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
4	W1C	0x0	linkst_out_l1sub_int Interrupt that indicates link has left L1 substate (falling edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
3	W1C	0x0	linkst_in_l0s_int Interrupt that indicates link has entered L0s state (rising edge detected of pm_linkst_in_l0s in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
2	W1C	0x0	linkst_in_l2_int Interrupt that indicates link has entered L2 state (rising edge detected of pm_linkst_in_l2 in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
1	W1C	0x0	linkst_in_l1_int Interrupt that indicates link has entered L1 state (rising edge detected of pm_linkst_in_l1 in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt
0	W1C	0x0	linkst_in_l1sub_int Interrupt that indicates link has entered L1 substate (rising edge detected of pm_linkst_in_l1sub in POWER_STATUS register). 1'b0: no interrupt 1'b1: interrupt

PCIE_CLIENT_INTR_MASK_MSG_RX

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x1	obff_cpu_active_int_mask Mask bit of the CPU Active OBFF message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
13	RW	0x1	obff_obff_int_mask Mask bit of the OBFF OBFF message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
12	RW	0x1	obff_idle_int_mask Mask bit of the OBFF IDLE message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
11	RO	0x0	reserved
10	RW	0x1	pm_turnoff_int_mask Mask bit of the pm_turnoff_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
9	RW	0x1	pm_to_ack_int_mask Mask bit of the pm_to_ack_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
8	RW	0x1	pm_pme_int_mask Mask bit of the pm_pme_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
7:6	RO	0x0	reserved
5	RW	0x1	pme_msi_mask Mask bit of the pme_msi interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
4	RW	0x1	pme_int_mask Mask bit of the pme_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
3	RO	0x0	reserved
2	RW	0x1	ltr_msg_int_mask Mask bit of the LTR message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
1	RW	0x1	unlock_int_mask Mask bit of the unlock message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
0	RW	0x1	ven_msg_int_mask Mask bit of the vendor-defined message reception interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

PCIE_CLIENT_INTR_MASK_LEGACY

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x1	tx_intd_int_mask Mask bit of the tx_intd_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
6	RW	0x1	tx_intc_int_mask Mask bit of the tx_intc_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
5	RW	0x1	tx_intb_int_mask Mask bit of the tx_intb_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
4	RW	0x1	tx_inta_int_mask Mask bit of the tx_inta_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
3	RW	0x1	rx_intd_int_mask Mask bit of the rx_intd_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
2	RW	0x1	rx_intc_int_mask Mask bit of the rx_intc_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
1	RW	0x1	rx_intb_int_mask Mask bit of the rx_intb_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
0	RW	0x1	rx_inta_int_mask Mask bit of the rx_inta_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

PCIE_CLIENT_INTR_MASK_ERR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	radm_qoverflow_mask Mask bit of the radm_qoverflow_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
11	RO	0x0	reserved
10	RW	0x1	f_err_rx_int_mask Mask bit of the f_err_rx_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
9	RW	0x1	nf_err_rx_int_mask Mask bit of the nf_err_rx_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

Bit	Attr	Reset Value	Description
8	RW	0x1	cor_err_rx_int_mask Mask bit of the cor_err_rx_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
7	RO	0x0	reserved
6	RW	0x1	f_err_sent_int_mask Mask bit of the f_err_sent_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
5	RW	0x1	nf_err_sent_int_mask Mask bit of the nf_err_sent_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
4	RW	0x1	cor_err_sent_int_mask Mask bit of the cor_err_sent_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
3	RW	0x1	tx_cpl_timeout_int_mask Mask bit of the tx_cpl_timeout_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
2	RW	0x1	rx_cpl_timeout_int_mask Mask bit of the rx_cpl_timeout_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
1	RW	0x1	aer_rc_err_msi_mask Mask bit of the aer_rc_err_msi interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
0	RW	0x1	aer_rc_err_int_mask Mask bit of the aer_rc_err_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

PCIE_CLIENT_INTR_MASK_MISC

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ep_elbi_app_int_mask Mask bit of the ep_elbi_app_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
14	RW	0x1	link_eq_req_int_mask Mask bit of the link_eq_req_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
13	RW	0x1	rbar_updata_int_mask Mask bit of the rbar_updata_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

Bit	Attr	Reset Value	Description
12	RW	0x1	dpa_sub_upd_int_mask Mask bit of the dpa_sub_upd_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
11	RW	0x1	edma_rd_int_mask Mask bit of the edma_rd_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
10	RW	0x1	edma_wr_int_mask Mask bit of the edma_wr_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
9	RW	0x1	bw_mgt_msi_mask Mask bit of the bw_mgt_msi interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
8	RW	0x1	bw_mgt_int_mask Mask bit of the bw_mgt_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
7	RW	0x1	link_auto_bw_msi_mask Mask bit of the link_auto_bw_msi interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
6	RW	0x1	link_auto_bw_int_mask Mask bit of the link_auto_bw_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
5	RW	0x1	hp_msi_mask Mask bit of the hp_msi interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
4	RW	0x1	hp_int_mask Mask bit of the hp_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
3	RW	0x1	hp_pme_int_mask Mask bit of the hp_pme_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
2	RW	0x1	link_req_rst_not_int_mask Mask bit of the link_req_rst_not_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
1	RW	0x1	dll_link_up_int_mask Mask bit of the dll_link_up_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask
0	RW	0x1	phy_link_up_int_mask Mask bit of the phy_link_up_int interrupt. 1'b0: interrupt unmask 1'b1: interrupt mask

PCIE_CLIENT_INTR_MASK_PMC

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	pm_dstate_update_int_mask Mask bit of the pm_dstate_update_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
7	RW	0x1	linkst_out_l0s_int_mask Mask bit of the linkst_out_l0s_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
6	RW	0x1	linkst_out_l2_int_mask Mask bit of the linkst_out_l2_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
5	RW	0x1	linkst_out_l1_int_mask Mask bit of the linkst_out_l1_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
4	RW	0x1	linkst_out_l1sub_int_mask Mask bit of the linkst_out_l1sub_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
3	RW	0x1	linkst_in_l0s_int_mask Mask bit of the linkst_in_l0s_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
2	RW	0x1	linkst_in_l2_int_mask Mask bit of the linkst_in_l2_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
1	RW	0x1	linkst_in_l1_int_mask Mask bit of the linkst_in_l1_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask
0	RW	0x1	linkst_in_l1sub_int_mask Mask bit of the linkst_in_l1sub_int interrupt in INTR_STATUS_PMC register. 1'b0: interrupt unmask 1'b1: interrupt mask

PCIE_CLIENT_POWER_CON

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_req_n_con Valid when clk_req_n_bypass set to 1. 1'b1: tristate CLKREQ# 1'b0: pull down CLKREQ#
12	RW	0x0	clk_req_n_bypass 1'b1: clk_req_n bypass, CLKREQ# driven by bit 13 of POWER_CON 1'b0: clk_req_n does not bypass, CLKREQ# driven by controller
11:10	RW	0x0	p2_cpm_disable 2'b00: when phy in P2 power state, enable clock PM for both L1 and L2. 2'b01: when phy in P2 power state, enable clock PM for L2 but disable for L1. 2'b10: when phy in P2 power state, disable clock PM for L2 but enable for L1. 2'b11: when phy in P2 power state, disable clock PM for both L1 and L2.
9	RW	0x0	app_clk_pm_en Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register.
8	RW	0x0	sys_aux_pwr_det Indicates if auxiliary power is present. 1'b1: Auxiliary power is present 1'b0: Auxiliary power is not present
7	RO	0x0	reserved
6	RW	0x0	app_l1sub_disable The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register
5	RW	0x0	app_xfer_pending Indicates that your application has transfers pending. 1'b1: There are transactions outside the controller that the controller needs to transmit. For EP mode, prevents generation of requests to enter L1. Triggers exit if already in L1. For RC mode, triggers exit if already in L1. 1'b0: There are no transactions outside the controller.
4	RW	0x0	app_req_exit_l1 1'b1: Application request to Exit L1. 1'b0: Self clear to generate a pulse to controller. Request from your application to exit L1. It is only effective when L1 is enabled.

Bit	Attr	Reset Value	Description
3	RW	0x1	app_ready_entr_l23 1'b1: Application ready to enter L23. 1'b0: Application not ready to enter L23. Indication application that it is ready to enter the L23 state. The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. EP mode only.
2	RW	0x0	app_req_entr_l1 Application request to Enter L1 ASPM state. 1'b1: Application request to enter L1 state 1'b0: Self clear to generate a pulse to controller This bit is used by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. EP mode only.
1	RW	0x0	app_pm_xmt_pme Request controller to send PME message. Self clear to generate a pulse to controller. If PME is enabled and PME support is configured for current PMCSR D-state asserting this signal will cause the controller to wake from either L1 or L2 state. When the controller has transitioned back to the L0 state it will transmit a PME message and set the PME_Status. Upon receiving the PME message the root complex should clear the PME_Status and change the D-state back to D0. This bit de-asserted when D-state back to D0. EP mode only.
0	RW	0x0	app_clk_req_n Indicates that the application is ready to have reference clock removed. 1'b0: Application does not want to remove reference clock 1'b1: Application is ready to have reference clock removed

PCIE_CLIENT_POWER_STATUS

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	pm_clkreq_in Status of wire CLKREQ#
27	RW	0x0	pm_clkreq_out Status of CLKREQ# drive signal
26	RO	0x0	pm_wake_in Status of wire WAKE#
25	RO	0x0	pm_wake_out 1'b1: Controller assert WAKE# signal to request to make link back to L0 1'b0: Controller is not in wake process or Link already back to L0 EP only.
24	RO	0x0	pm_linkst_in_l0s 1'b1: Power management is in L0s. 1'b0: Power management is not in L0s.

Bit	Attr	Reset Value	Description
23	RO	0x0	pm_linkst_in_l2 1'b1: Power management is in L2. 1'b0: Power management is not in L2.
22	RO	0x0	pm_linkst_in_l1 1'b1: Power management is in L1. 1'b0: Power management is not in L1.
21	RO	0x0	pm_linkst_in_l1sub 1'b1: Power management is in L1 substate. 1'b0: Power management is not in L1 substate.
20	RO	0x0	reserved
19:17	RO	0x0	pm_l1sub_state Power management L1 sub-states FSM state. For debugging purposes, not for system operation.
16:15	RO	0x0	reserved
14:10	RO	0x00	pm_slave_state Power management slave FSM state. For debugging purposes, not for system operation.
9	RO	0x0	reserved
8:4	RO	0x00	pm_master_state Power management master FSM state. For debugging purposes, not for system operation.
3	RO	0x0	reserved
2:0	RO	0x0	pm_curnt_state Indicates the current power state. For debugging purposes, not for system operation.

PCIE_CLIENT_MSG_GEN_CON

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	obff_cpu_active_msg_req Request controller to generate a "CPU Active" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
13	RW	0x0	obff_obff_msg_req Request controller to generate a "OBFF" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
12	RW	0x0	obff_idle_msg_req Request controller to generate a "IDLE" OBFF message. This bit clears automatically when request has been sent. Only usable in a downstream port. When application sets OBFF Enable bit in Device Control 2 Register to choose to use OBFF message or WAKE# signaling.
11:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	ltr_msg_req Set to request controller to send a LTR Message. This bit clears automatically when request is granted by controller. Application should put LTR message information ready in LTR_MSG_TX_INFO register before setting this bit.
7:6	RO	0x0	reserved
5	RW	0x0	xmt_unlock_req Request controller to generate an Unlock message. This bit clears automatically when request has been sent.
4	RW	0x0	xmt_turnoff_req Request controller to generate a PM_Turn_Off message. This bit clears automatically when request has been sent.
3:2	RO	0x0	reserved
1	RW	0x0	legacy_int_req This bit is intended to request controller to generate messages that emulates the legacy PCI Interrupts. When this bit goes from low to high, the controller generates an Assert_INTx Message. When this bit goes from high to low, the controller generates a Deassert_INTx Message. The Interrupt Pin register for the corresponding function determines which INTx Message the controller generates (INTA, INTB, INTC, or INTD).
0	RW	0x0	ven_msg_req Set to request controller to send a vendor-defined Message. This bit clears automatically when request is granted by controller. Application should put vendor message information ready in VEN_MSG_TX_CFGx registers before setting this bit.

PCIE_CLIENT_MSI_GEN_CON

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	msi_gen_req 32 bits write only MSI generation request signals. MSB has the highest priority and LSB has the lowest priority. Write 1 to a certain bit request the controller send a MSI interrupt. Software should use MSI capability register to access MSI mask or pending status.

PCIE_CLIENT_MSI_GEN_FNUM_TC

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	msi_tc Traffic Class of the MSI request. Reserved for future use.
3	RO	0x0	reserved
2:0	RW	0x0	msi_func_num The function number of the MSI request. Reserved for future use.

PCIE_CLIENT_RBAR_SIZE_INFO0

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	bar2_size_info BAR2 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.
15:14	RO	0x0	reserved
13:8	RW	0x00	bar1_size_info BAR1 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.
7:6	RO	0x0	reserved
5:0	RW	0x00	bar0_size_info BAR0 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.

PCIE_CLIENT_RBAR_SIZE_INFO1

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	bar5_size_info BAR5 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.
15:14	RO	0x0	reserved
13:8	RW	0x00	bar4_size_info BAR4 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.
7:6	RO	0x0	reserved
5:0	RW	0x00	bar3_size_info BAR3 size information, same with BAR0 size field from the resizable BAR control register. Updated when rbar_updata_int interrupt occur.

PCIE_CLIENT_DMA_HSHAKE_TOGG

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	rdxfer_done_togg DMA read engine descriptor transfer done toggle signal. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles
11:8	RO	0x0	wdxfer_done_togg DMA write engine descriptor transfer done toggle signal. After a doorbell command, this signal is de-asserted. When a channel is operating in non-linked list mode this signal does not toggles
7:4	RW	0x0	rdxfer_go_togg DMA read engine descriptor transfer go toggle signal. This signal is ignored whenever a DMA channel operates in non-linked mode.
3:0	RW	0x0	wdxfer_go_togg DMA Write engine descriptor transfer go toggle signal. This signal is ignored whenever a DMA channel operates in non-linked mode.

PCIE_CLIENT_VEN_MSG_RX_INFO0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	ven_msg_req_id The requester ID of the received Message. [15:8]: Bus number [7:3]: Device number [2:0]: Function number

PCIE_CLIENT_VEN_MSG_RX_INFO1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_l The third double word of the Vendor Defined Message header.

PCIE_CLIENT_VEN_MSG_RX_INFO2

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ven_msg_header_h The fourth double word of the Vendor Defined Message header.

PCIE_CLIENT_VEN_MSG_TX_CFG0

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	ven_msg_code The Message Code for the vendor-defined Message TLP.
23:16	RW	0x00	ven_msg_tag Tag for the vendor-defined Message TLP.
15:11	RO	0x00	reserved
10:9	RW	0x0	ven_msg_attr The Attributes field for the vendor-defined Message TLP. bit1: Relaxed ordering. bit0: No snoop.
8	RW	0x0	ven_msg_ep The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
7:5	RW	0x0	ven_msg_tc The Traffic Class field for the vendor-defined Message TLP.
4:0	RW	0x00	ven_msg_type The TYPE field for the vendor-defined Message TLP.

PCIE_CLIENT_VEN_MSG_TX_CFG1

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_l The third double word of the Vendor Defined Message header.

PCIE_CLIENT_VEN_MSG_TX_CFG2

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ven_msg_data_h The fourth double word of the Vendor Defined Message header.

PCIE_CLIENT_LTR_MSG_TX_INFO

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ltr_msg_latency 32 bits latency information in LTR message that application wants to send. Please refer to PCI Express Specification for message format.

PCIE_CLIENT_APP_ERR_RPT_INFO0

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	err_hdr_log0 The header (bit 0 to bit 31) of the TLP that contained the error.

PCIE_CLIENT_APP_ERR_RPT_INFO1

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	err_hdr_log1 The header (bit 32 to bit 63) of the TLP that contained the error.

PCIE_CLIENT_APP_ERR_RPT_INFO2

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	err_hdr_log2 The header (bit 64 to bit 95) of the TLP that contained the error.

PCIE_CLIENT_APP_ERR_RPT_INFO3

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	err_hdr_log3 The header (bit 96 to bit 127) of the TLP that contained the error.

PCIE_CLIENT_APP_ERR_RPT_INFO4

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	err_advisory 1'b1: application error is an advisory error. 1'b0: application error is not an advisory error.
15:13	RO	0x0	reserved
12:0	RW	0x0000	err_bus The type of error that application detected. The controller combines the values err_bus bits with the internally detected error signals to set the corresponding bit in the Uncorrectable or Correctable Error Status Registers, [0]: Malformed TLP [1]: Receiver Overflow [2]: Unexpected completion [3]: Completer abort [4]: Completion Timeout [5]: Unsupported request [6]: ECRC Check Failed [7]: Poisoned TLP received [8]: AtomicOp Egress Blocked [9]: Uncorrectable Internal Error [10]: Corrected Internal Error [11]: TLP Prefix Blocked Error Status [12]: ACS Violation

PCIE_CLIENT_OBFF_WAKE_ELE_CFG

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0xb4	wk_min_f2f_wdt Configure the minimum falling edge to falling edge width. The minimum value Specification define is 700ns. Application set this value equals to wk_min_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
23:16	RW	0xf0	wk_max_f2f_wdt Configure the maximum falling edge to falling edge width. The maximum value Specification define is 1000ns. Application set this value equals to wk_max_f2f_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
15:8	RW	0x50	wk_mim_pls_wdt Configure the minimum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The minimum value Specification define is 300ns. Application set this value equals to wk_mim_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2).
7:0	RW	0x64	wk_max_pls_wdt Configure the maximum WAKE# pulse width for both active-inactive-active and inactive-active-inactive pulse. The maximum value Specification define is 500ns. Application set this value equals to wk_max_pls_wdt * core_clock_period(8ns in gen1 and 4ns in gen2). Setting this value less than 50% of {wk_max_f2f_wdt * core_clock_period}.

PCIE_CLIENT_OBFF_WAKE_DEBUG

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	obff_wake_dec_err Error state of OBFF decoder FSM, used for debug.
7:4	RW	0x0	obff_wake_dec_state Current state of OBFF decoder FSM, used for debug.
3	RW	0x0	obff_wake_dec_cpu 1'b1: initialize the OBFF decoder to CPU ACTIVE state when obff_wake_dec_init is set 1'b0: do not initialize to CPU ACTIVE state
2	RW	0x0	obff_wake_dec_obff 1'b1: initialize the OBFF decoder to OBFF state when obff_wake_dec_init is set 1'b0: do not initialize to OBFF state
1	RW	0x0	obff_wake_dec_idle 1'b1: initialize the OBFF decoder to IDLE state when obff_wake_dec_init is set 1'b0: do not initialize to IDLE state
0	RW	0x0	obff_wake_dec_init 1'b1: initialize the OBFF decoder 1'b0: do not initialize the OBFF decoder

PCIE_CLIENT_RX_CPL_TIME_OUT_INFO

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	rx_timeout_cpl_tag The Tag field of the timeout completion.
23:12	RO	0x000	rx_timeout_cpl_len Length (in bytes) of the timeout completion. For a split completion, it indicates the number of bytes remaining to be delivered when the completion timeout.
11:10	RO	0x0	reserved
9:8	RO	0x0	rx_timeout_cpl_attr The Attributes field of the timeout completion.
7	RO	0x0	reserved
6:4	RO	0x0	rx_timeout_cpl_tc The Traffic Class of the timeout completion.
3	RO	0x0	reserved
2:0	RO	0x0	rx_timeout_func_num The function Number of the timeout completion.

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO0

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	tx_timeout_cpl_len The Length of the timeout completion.
11:10	RO	0x0	reserved
9:8	RO	0x0	tx_timeout_cpl_attr The Attributes value of the timeout completion.
7	RO	0x0	reserved
6:4	RO	0x0	tx_timeout_cpl_tc The TC of the timeout completion.
3	RO	0x0	reserved
2:0	RO	0x0	tx_timeout_func_num The function number of the timeout completion.

PCIE_CLIENT_TX_CPL_TIME_OUT_INFO1

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	trgt_lookup_empty Indicates that the target completion LUT is not full
15:8	RW	0x00	trgt_lookup_id The target completion LUT lookup ID for the incoming request TLP. When using the optional target completion lookup table feature, the application must save the lookup ID and assert the same lookup ID client0/1/2_cpl_lookup_id when generating a completion for the request.
7:0	RW	0x00	trgt_timeout_lookup_id The target completion LUT lookup ID of the timeout completion

PCIE_CLIENT_LOCAL_CRU_CTRL

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	radm_gate_disable Disable the radm_clk gating in local cru.
12	RW	0x0	aux_gate_disable Disable the aux_clk gating in local cru.
11	RW	0x0	link_down_gate_disable Disable the link down clock gating in local cru.
10	RW	0x0	dbi_aclk_gate_disable Disable the dbi_aclk gating in local cru.
9	RW	0x0	slv_aclk_gate_disable Disable the slv_aclk gating in local cru.
8	RW	0x0	mstr_aclk_gate_disable Disable the mstr_aclk gating in local cru.
7:4	RO	0x0	reserved
3	RW	0x0	pcie_pm_phy_req_disable Mask the phy reset request from controller pm.
2	RW	0x0	pcie_pm_srst_req_disable Mask the sticky reset request from controller pm.
1	RW	0x0	pcie_pm_nsrst_req_disable Mask the non-sticky reset request from controller pm.
0	RW	0x0	pcie_pm_crst_req_disable Mask the core reset request from controller pm.

PCIE_CLIENT_GENERAL_DEBUG_CON

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	sd_hold_ltssm 1'b1: Hold LTSSM 1'b0: Release LTSSM
5	RW	0x0	dbg_pba MSIX PBA RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the PBA.
4	RW	0x0	dbg_table MSIX Table RAM Debug Mode. Use this input to activate the debug mode and allow direct read/write access to the Table.
3	RO	0x0	reserved
2:0	RW	0x0	diag_ctrl_bus The rising edge of these two signals ([1:0]) enable the controller to assert an LCRC or ECRC to the packet that it currently being transferred: 3'bx01: Insert LCRC error by inverting the LSB of LCRC 3'bx10: Insert ECRC error by inverting the LSB of ECRC 3'b1xx: Select Fast Link Mode, simulation only

PCIE_CLIENT_GENERAL_DEBUG_INFO

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RO	0x00	smlh_ltssm_state Current state of the LTSSM
9	RO	0x0	reserved
8	RO	0x0	radm_q_not_empty 1'b1: receive queues contain TLP header/data 1'b0: receive queues do not contain TLP header/data.
7	RO	0x0	radm_xfer_pending 1'b1: receive TLP requests are pending 1'b0: receive TLP requests are not pending
6	RO	0x0	edma_xfer_pending 1'b1: EDMA transfer pending 1'b0: EDMA DBI transfer not pending
5	RO	0x0	brdg_dbi_xfer_pending 1'b1: AXI Slave DBI transfer pending 1'b0: AXI Slave DBI transfer not pending
4	RO	0x0	brdg_slv_xfer_pending 1'b1: AXI Slave non-DBI transfer pending 1'b0: AXI Slave non-DBI transfer not pending
3	RO	0x0	reserved
2	RO	0x0	radm_idle 1'b1: RADM is in idle status 1'b0: RADM is not idle in status
1	RW	0x0	rdlh_link_up 1'b1: data link layer up 1'b1: data link layer down
0	RW	0x0	smlh_link_up 1'b1: PHY link is up 1'b0: PHY link is down

PCIE_CLIENT_SLC_DEBUG_INFO_COMMON

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16 of total 78 bit of common silicon debug information: 3'b000: select bit 15 to 0 3'b001: select bit 31 to 16 3'b010: select bit 47 to 32 3'b011: select bit 63 to 48 3'b100: select bit 77 to 64 other: reserved
27:16	RO	0x000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	sd_info_common 16 of total 78-bit common silicon debug information, selected by bus_select field. [77:75]: l1sub_state: Level: L1 sub state [74]: init_eq_pending_g4: Level: Equalization sequence Gen4 [73]: init_eq_pending: Level: Equalization sequence Gen3 [72:61]: xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# [60:49]: rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# [48]: rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 [47]: rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 [46:45]: rdlh_dlcntrl_state [1:0]: Level: DLCM [44:37]: latched_ts_nfts[7:0]: Level: Latched NFTS [36:34]: ltssm_powerdown[1:0]: Level: PIPE: Power Down [33:18]: smlh_ltssm_variable [15:0]: Level: LTSSM Variable [17]: pm_pme_resend_flag: Pulse: PME Re-Send flag [16]: smlh_lane_reversed: Level: Lane Reversal Operation [15:9]: rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer [8:5]: pm_slave_state[3:0]: Level: PM Internal State (Slave) [4:0]: pm_master_state[4:0]: Level: PM Internal State (Master)

PCIE_CLIENT_SLC_DEBUG_INFO_LN

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16 of total 78 bit of l0 silicon debug information: 3'b000: select bit 15 to 0 3'b001: select bit 31 to 16 3'b010: select bit 47 to 32 3'b011: select bit 63 to 48 3'b100: select bit 77 to 64 other: reserved
27:24	RW	0x0	lane_sel sd_info_ln source selects 4'h0: Lane 0 4'h1: Lane 1 4'h2: Lane 2 4'h3: Lane 3
23:16	RO	0x00	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	sd_info_ln 16 of total 78-bit l0 silicon debug information, selected by bus_select field. [77:76]: eq_convergence_sts [1:0]: Level: Equalization convergence information Gen3 [75]: eqpa_violate_rule_123[2]: Level: Rule C Violation Event Status Gen3 [74]: eqpa_violate_rule_123[1]: Level: Rule B Violation Event Status Gen3 [73]: eqpa_violate_rule_123[0]: Level: Rule A Violation Event Status Gen3 [72]: mac_cdm_ras_des_reject_rtx: Level: Receive Reject Coefficient Event status Gen3 [71:64]: phy_cdm_ras_des_fomfeedback: Level: Current Figure of Merit Gen3 [63:61]: mac_cdm_ras_des_pset_lrx: Level: Current Local Receiver Preset Hint Gen3 [60:55]: mac_cdm_ras_des_coef_ltx[5:0]: Level: Current Local Transmitter Pre Cursor coefficient Gen3 [54:49]: mac_cdm_ras_des_coef_ltx[11:6]: Level: Current Local Transmitter Cursor coefficient Gen3 [48:43]: mac_cdm_ras_des_coef_ltx[17:12]: Level: Current Local Transmitter Post Cursor coefficient Gen3 [42:37]: mac_cdm_ras_des_coef_rtx[5:0]: Level: Current Remote Transmitter Pre Cursor coefficient Gen3 [36:31]: mac_cdm_ras_des_coef_rtx[11:6]: Level: Current Remote Transmitter Cursor coefficient Gen3 [30:25]: mac_cdm_ras_des_coef_rtx[17:12]: Level: Current Remote Transmitter Post Cursor coefficient Gen3 [24:19]: mac_cdm_ras_des_lf: Level: Remote Device LF Gen3 [18:13]: mac_cdm_ras_des_fs: Level: Remote Device FS Gen3 [12:5]: rmlh_deskew_fifo_ptr: Level: Deskew Pointer [4]: mac_phy_rxpolarity: Level: PIPE: RxPolarity [3]: latched_rxdetected: Level: PIPE: Detect Lane [2]: phy_mac_rxvalid_rxburst: Level: PIPE: RxValid/RxBurst [1]: phy_mac_rxelec_rxh8exit: Level: PIPE: RxElecIdle/RxHibern8ExitType1 [0]: mac_phy_txelec_txburst: Level: PIPE: TxElecIdle/TxBurst

PCIE_CLIENT_SLC_DEBUG_INFO_V0

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	bus_select Select the 16 of total 240 bit of virtual channel 0 silicon debug information: 4'd0: select bit 15 to 0 4'd1: select bit 31 to 16 ... 4'd14: select bit 239 to bit 224 other: reserved
27:16	RO	0x000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	sd_info_v0 16 of total 240-bit l1 silicon debug information, selected by bus_select field. [239:228]: rtlh_fc_allctd_cpld: Level: Credit Allocated (CD) [227:220]: rtlh_fc_allctd_cplh: Level: Credit Allocated (CH) [219:208]: rtlh_fc_allctd_npd: Level: Credit Allocated (ND) [207:200]: rtlh_fc_allctd_nph: Level: Credit Allocated (NH) [199:188]: rtlh_fc_allctd_pd: Level: Credit Allocated (PD) [187:180]: rtlh_fc_allctd_ph: Level: Credit Allocated (PH) [179:168]: rtlh_fc_rcvd_cpld: Level: Credit Received (CD) [167:160]: rtlh_fc_rcvd_cplh: Level: Credit Received (CH) [159:148]: rtlh_fc_rcvd_npd: Level: Credit Received (ND) [147:140]: rtlh_fc_rcvd_nph: Level: Credit Received (NH) [139:128]: rtlh_fc_rcvd_pd: Level: Credit Received (PD) [127:120]: rtlh_fc_rcvd_ph: Level: Credit Received (PH) [119:108]: xadm_fc_limit_cpld: Level: Credit Limit (CD) [107:100]: xadm_fc_limit_cplh: Level: Credit Limit (CH) [99:88]: xadm_fc_limit_npd: Level: Credit Limit (ND) [87:80]: xadm_fc_limit_nph: Level: Credit Limit (NH) [79:68]: xadm_fc_limit_pd: Level: Credit Limit (PD) [67:60]: xadm_fc_limit_ph: Level: Credit Limit (PH) [59:48]: xadm_fc_cnsmd_cpld: Level: Credit Consumed (CD) [47:40]: xadm_fc_cnsmd_cplh: Level: Credit Consumed (CH) [39:28]: xadm_fc_cnsmd_npd: Level: Credit Consumed (ND) [27:20]: xadm_fc_cnsmd_nph: Level: Credit Consumed (NH) [19:8]: xadm_fc_cnsmd_pd: Level: Credit Consumed (PD) [7:0]: xadm_fc_cnsmd_ph: Level: Credit Consumed (PH)

PCIE_CLIENT_DIAG_STATUS_BUS_SEL

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	diag_bus_sel Select the 32 of total 488 bit of diag_status_bus that present on register DIAG_STATUS_BUS_INFO. 5'd0: bit 31 to 0 5'd1: bit 63 to 32 ... 5'd31: bit 1023 to 992

PCIE_CLIENT_DIAG_STATUS_BUS_INFO

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	diag_status_bus 32 bit of total 1024 bit width diag_status_bus. Selected by DIAG_STATUS_BUS_SEL register. Contains all the important status signals from each controller module.

PCIE_CLIENT_CDM_RASDES_EC_INFO_CON

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	cdm_rasdes_ec_info_lane_sel cdm_rasdes_ec_info_lane_sel

Bit	Attr	Reset Value	Description
3:0	RW	0x0	cdm_rasdes_ec_info_con cdm_rasdes_ec_info_con

PCIE_CLIENT_CDM_RASDES_EC_INFO_CMN

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rasdes_ec_info_cmn

PCIE_CLIENT_CDM_RASDES_EC_INFO_LN

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	rasdes_ec_info_ln rasdes_ec_info_ln

PCIE_CLIENT_CDM_RASDES_TBA_CON

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	app_ras_des_tba_ctrl Controls the start/end of time-based analysis. You must only set the pins to the required value for the duration of one clock cycle. This signal must be 2'b00 while the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register is controlled by the DBI interface or the accesses from the wire side. 2'b00: No action 2'b01: Start 2'b10: End. This setting is only used when the TIME_BASED_DURATION_ SELECT field of TIME_BASED_ANALYSIS_CONTROL_REG is set to "manual control". 2'b11: Reserved These pins also set the contents of the TIMER_START field in TIME_BASED_ANALYSIS_CONTROL_REG register.

PCIE_CLIENT_CDM_RASDES_TBA_INFO_CMN

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	rasdes_tba_info_cmn rasdes_tba_info_cmn

PCIE_CLIENT_HOT_RESET_CTRL

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	app_ltssm_enable_enhance Set "1" to enable ltssm_enbale enhance mode.
3	RW	0x0	app_dly2_done Set "1" to end the delaying of the link training after Hot Reset. This bit is self-cleared.

Bit	Attr	Reset Value	Description
2	RW	0x0	app_dly1_done Set "1" to end the delaying of the controller Hot Reset. This bit is self-cleared.
1	RW	0x0	app_dly2_en Set "1" to enable delaying the link training after Hot Reset
0	RW	0x0	app_dly1_en Set "1" to enable delaying the controller Hot Reset

PCIE_CLIENT_AXI_MSTR_MISC_CON

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	mstr_rmisc_ep EP bit of read cpl TLP
3:2	RW	0x0	mstr_rmisc_cpl_status AXI Master Read Response selection bus. This bus controls the response sent on the PCIe wire in the case of successful read requests. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion)
1:0	RW	0x0	mstr_bmisc_cpl_status AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. 2'b00: SC (Successful Completion) 2'b01: CA (Completer Abort) 2'b10: UR (Unsupported Request) 2'b11: SC (Successful Completion)

PCIE_CLIENT_AXI_SLV_ATU_BYPASS

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	slv_ar_atu_bypass 1'b1: AXI slave read address ATU bypass 1'b0: not bypass
0	RW	0x0	slv_aw_atu_bypass 1'b1: AXI slave write address ATU bypass 1'b0: not bypass

PCIE_CLIENT_AXI_SLV_AWMISC_HDR

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21:0	RW	0x000000	slv_awmisc_info [4:0]: TLP's TYPE [5]: Reserved [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's Function number.

PCIE_CLIENT_AXI_SLV_AWMISC_HDR3

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_3dw AXI Slave 3rd header DWs. The application drives this with the 3rd Header DWs it intends to send on a PCIe Msg/MsgD.

PCIE_CLIENT_AXI_SLV_AWMISC_HDR4

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	slv_awmisc_info_hdr_4dw AXI Slave 4th header DWs. The application drives this with the 4th Header DWs it intends to send on a PCIe Msg/MsgD.

PCIE_CLIENT_AXI_SLV_AWMISC_TAG

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	slv_awmisc_tag AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your application normally sets this to '0' except when generating ATS invalidate requests.

PCIE_CLIENT_AXI_SLV_MISC_INFO

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	slv_wmisc_info When asserted, the controller sets the Poisoned TLP (EP) bit in the TLP header of the current and subsequent Write Data transactions.

Bit	Attr	Reset Value	Description
21:0	RW	0x000000	slv_armisc_info Provide readTLP header information [4:0]: TLP's TYPE [5]: Reserved [6]: TLP's EP bit [7]: Reserved [8]: TLP's NS bit [9]: TLP's RO bit [12:10]: TLP's TC bits [20:13]: TLP's MSG code [21]: AXI transaction is a DBI access. This is for SHARED DBI mode only. [24:22]: TLP's function number.

PCIE_CLIENT_DBI_MISC_CON

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dbi_msi_dbg_sel Control the bit 30 of the DBI awaddr.

PCIE_CLIENT_PORT_BDF

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:7	RW	0x00	bus_dev Bus number. Your application must drive this signal to set the bus number in the Requester ID for RC port and Switch DSP port
6:3	RW	0x0	dev_num Device number. Your application must drive this signal to set the device number in the Requester ID for RC port and Switch DSP port
2:0	RO	0x0	reserved

PCIE_CLIENT_LTSSM_STATUS

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	pm_current_data_rate pm_current_data_rate
19:18	RO	0x0	reserved
17	RW	0x0	rdlh_link_up rdlh_link_up
16	RW	0x0	smlh_link_up smlh_link_up
15:11	RO	0x00	reserved
10:8	RW	0x0	l1sub_state l1sub_state
7:6	RO	0x0	reserved
5:0	RW	0x00	smlh_ltssm_state smlh_ltssm_state

PCIE_CLIENT_DBG_FIFO_MODE_CON

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	dbg_fifo_hit_mode dbg_fifo_hit_mode
7:6	RO	0x0	reserved
5:4	RW	0x0	dbg_fifo_mode dbg_fifo_mode
3	RO	0x0	reserved
2	RW	0x0	dbg_fifo_l1sub_en dbg_fifo_l1sub_en
1	RW	0x0	dbg_fifo_ltssm_en dbg_fifo_ltssm_en
0	RW	0x0	dbg_fifo_en dbg_fifo_en

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA0

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data0 Hit mode data pattern 0

PCIE_CLIENT_DBG_FIFO_PTN_HIT_DATA1

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ptn_hit_data1 Hit mode data pattern 1

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA0

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data0 Transition state data 0

PCIE_CLIENT_DBG_FIFO_TRN_HIT_DATA1

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	trn_hit_data1 Transition state data 1

PCIE_CLIENT_DBG_FIFO_STATUS

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	dbg_space2empty dbg_space2empty
15	RO	0x0	reserved
14	RW	0x0	dbg_fifo_wr_overfollow dbg_fifo_wr_overfollow
13	RW	0x0	dbg_fifo_full dbg_fifo_full

Bit	Attr	Reset Value	Description
12	RW	0x0	dgb_fifo_empty dgb_fifo_empty
11	RO	0x0	reserved
10:8	RW	0x0	dbg_fifo_l1sub_state dbg_fifo_l1sub_state
7:6	RO	0x0	reserved
5:0	RW	0x00	dbg_fifo_ltssm_state dbg_fifo_ltssm_state

PCIE_CLIENT_CFG_ERR_STATUS

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cfg_uncor_internal_err_sts cfg_uncor_internal_err_sts
11	RW	0x0	cfg_rcvr_overflow_err_sts cfg_rcvr_overflow_err_sts
10	RW	0x0	cfg_fc_protocol_err_sts cfg_fc_protocol_err_sts
9	RW	0x0	cfg_mlf_tlp_err_sts cfg_mlf_tlp_err_sts
8	RW	0x0	cfg_surprise_down_err_sts cfg_surprise_down_err_sts
7	RW	0x0	cfg_dl_protocol_err_sts cfg_dl_protocol_err_sts
6	RW	0x0	cfg_ecrc_err_sts cfg_ecrc_err_sts
5	RW	0x0	cfg_corrected_internal_err_sts cfg_corrected_internal_err_sts
4	RW	0x0	cfg_replay_number_rollover_err_sts cfg_replay_number_rollover_err_sts
3	RW	0x0	cfg_replay_timer_timeout_err_sts cfg_replay_timer_timeout_err_sts
2	RW	0x0	cfg_bad_dllp_err_sts cfg_bad_dllp_err_sts
1	RW	0x0	cfg_bad_tlp_err_sts cfg_bad_tlp_err_sts
0	RW	0x0	cfg_rcvr_err_sts cfg_rcvr_err_sts

PCIE_CLIENT_CLIENT_VER

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RO	0x00050600	version Client version ID

18.4.4 DMA Registers Summary

Name	Offset	Size	Reset Value	Description
DMA_CTRL_DATA_ARB_PRIOR_OFF	0x0000	W	0x00000688	DMA Arbitration Scheme for TRGT1 Interface.
DMA_CTRL_OFF	0x0008	W	0x00010001	DMA Number of Channels Register.

Name	Offset	Size	Reset Value	Description
DMA_WRITE_ENGINE_EN_OFF	0x000C	W	0x00000000	DMA Write Engine Enable Register.
DMA_WRITE_DOORBELL_OFF	0x0010	W	0x00000000	DMA Write Doorbell Register.
DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0018	W	0x00008421	DMA Write Engine Channel Arbitration Weight Low Register.
DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x001C	W	0x00000000	DMA Write Engine Channel Arbitration Weight High Register.
DMA_READ_ENGINE_EN_OFF	0x002C	W	0x00000000	DMA Read Engine Enable Register.
DMA_READ_DOORBELL_OFF	0x0030	W	0x00000000	DMA Read Doorbell Register.
DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF	0x0038	W	0x00008421	DMA Read Engine Channel Arbitration Weight Low Register.
DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF	0x003C	W	0x00008421	DMA Read Engine Channel Arbitration Weight High Register.
DMA_WRITE_INT_STATUS_OFF	0x004C	W	0x00000000	DMA Write Interrupt Status Register.
DMA_WRITE_INT_MASK_OFF	0x0054	W	0x00010001	DMA Write Interrupt Mask Register.
DMA_WRITE_INT_CLEAR_OFF	0x0058	W	0x00000000	DMA Write Interrupt Clear Register.
DMA_WRITE_ERR_STATUS_OFF	0x005C	W	0x00000000	DMA Write Error Status Register
DMA_WRITE_DONE_IMWR_LOW_OFF	0x0060	W	0x00000000	DMA Write Done IMWr Address Low Register.
DMA_WRITE_DONE_IMWR_HIGH_OFF	0x0064	W	0x00000000	DMA Write Done IMWr Interrupt Address High Register.
DMA_WRITE_ABORT_IMWR_LOW_OFF	0x0068	W	0x00000000	DMA Write Abort IMWr Address Low Register.
DMA_WRITE_ABORT_IMWR_HIGH_OFF	0x006C	W	0x00000000	DMA Write Abort IMWr Address High Register.
DMA_WRITE_CH01_IMWR_DATA_OFF	0x0070	W	0x00000000	DMA Write Channel 1 and 0 IMWr Data Register.
DMA_WRITE_CH23_IMWR_DATA_OFF	0x0074	W	0x00000000	DMA Write Channel 3 and 2 IMWr Data Register.
DMA_WRITE_CH45_IMWR_DATA_OFF	0x0078	W	0x00000000	DMA Write Channel 5 and 4 IMWr Data Register.
DMA_WRITE_CH67_IMWR_DATA_OFF	0x007C	W	0x00000000	DMA Write Channel 7 and 6 IMWr Data Register.
DMA_WRITE_LINKED_LIST_ERR_EN_OFF	0x0090	W	0x00000000	DMA Write Linked List Error Enable Register.
DMA_READ_INT_STATUS_OFF	0x00A0	W	0x00000000	DMA Read Interrupt Status Register.
DMA_READ_INT_MASK_OFF	0x00A8	W	0x00010001	DMA Read Interrupt Mask Register.
DMA_READ_INT_CLEAR_OFF	0x00AC	W	0x00000000	DMA Read Interrupt Clear Register.
DMA_READ_ERR_STATUS_LOW_OFF	0x00B4	W	0x00000000	DMA Read Error Status Low Register.
DMA_READ_ERR_STATUS_HIGH_OFF	0x00B8	W	0x00000000	DMA Read Error Status High Register.

Name	Offset	Size	Reset Value	Description
DMA_READ_LINKED_LIST_ERR_EN_OFF	0x00C4	W	0x00000000	DMA Read Linked List Error Enable Register.
DMA_READ_DONE_IMWR_LOW_OFF	0x00CC	W	0x00000000	DMA Read Done IMWr Address Low Register.
DMA_READ_DONE_IMWR_HIGH_OFF	0x00D0	W	0x00000000	DMA Read Done IMWr Address High Register.
DMA_READ_ABORT_IMWR_LOW_OFF	0x00D4	W	0x00000000	DMA Read Abort IMWr Address Low Register.
DMA_READ_ABORT_IMWR_HIGH_OFF	0x00D8	W	0x00000000	DMA Read Abort IMWr Address High Register.
DMA_READ_CH01_IMWR_DATA_OFF	0x00DC	W	0x00000000	DMA Read Channel 1 and 0 IMWr Data Register.
DMA_READ_CH23_IMWR_DATA_OFF	0x00E0	W	0x00000000	DMA Read Channel 3 and 2 IMWr Data Register.
DMA_READ_CH45_IMWR_DATA_OFF	0x00E4	W	0x00000000	DMA Read Channel 5 and 4 IMWr Data Register.
DMA_READ_CH67_IMWR_DATA_OFF	0x00E8	W	0x00000000	DMA Read Channel 7 and 6 IMWr Data Register.
DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF	0x0108	W	0x00000000	DMA Write Engine Handshake Counter Channel 0/1/2/3 Register.
DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF	0x010C	W	0x00000000	DMA Write Engine Handshake Counter Channel 4/5/6/7 Register.
DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF	0x0118	W	0x00000000	DMA Read Engine Handshake Counter Channel 0/1/2/3 Register.
DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF	0x011C	W	0x00000000	DMA Read Engine Handshake Counter Channel 4/5/6/7 Register.
DMA_CH_CONTROL1_OFF_WRCH_0	0x0200	W	0x00000000	DMA Write Channel Control 1 Register.
DMA_TRANSFER_SIZE_OFF_WRCH_0	0x0208	W	0x00000000	DMA Write Transfer Size Register.
DMA_SAR_LOW_OFF_WRCH_0	0x020C	W	0x00000000	DMA Write SAR Low Register.
DMA_SAR_HIGH_OFF_WRCH_0	0x0210	W	0x00000000	DMA Write SAR High Register.
DMA_DAR_LOW_OFF_WRCH_0	0x0214	W	0x00000000	DMA Write DAR Low Register.
DMA_DAR_HIGH_OFF_WRCH_0	0x0218	W	0x00000000	DMA Write DAR High Register.
DMA_LLP_LOW_OFF_WRCH_0	0x021C	W	0x00000000	DMA Write Linked List Pointer Low Register.
DMA_LLP_HIGH_OFF_WRCH_0	0x0220	W	0x00000000	DMA Write Linked List Pointer High Register.
DMA_CH_CONTROL1_OFF_RDCH_0	0x0300	W	0x00000000	DMA Read Channel Control 1 Register.
DMA_TRANSFER_SIZE_OFF_RDCH_0	0x0308	W	0x00000000	DMA Read Transfer Size Register.
DMA_SAR_LOW_OFF_RDCH_0	0x030C	W	0x00000000	DMA Read SAR Low Register.
DMA_SAR_HIGH_OFF_RDCH_0	0x0310	W	0x00000000	DMA Read SAR High Register.
DMA_DAR_LOW_OFF_RDCH_0	0x0314	W	0x00000000	DMA Read DAR Low Register.

Name	Offset	Size	Reset Value	Description
DMA_DAR_HIGH_OFF_RDCH_0	0x0318	W	0x00000000	DMA Read DAR High Register.
DMA_LLP_LOW_OFF_RDCH_0	0x031C	W	0x00000000	DMA Read Linked List Pointer Low Register.
DMA_LLP_HIGH_OFF_RDCH_0	0x0320	W	0x00000000	DMA Read Linked List Pointer High Register.

18.4.5 DMA Detail Registers Description

DMA_CTRL_DATA_ARB_PRIOR_OFF

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:9	RW	0x3	RDBUFF_TRGT_WEIGHT DMA Read Channel MWr Requests. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
8:6	RW	0x2	RD_CTRL_TRGT_WEIGHT DMA Read Channel MRd Requests. For LL element/descriptor access. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
5:3	RW	0x1	WR_CTRL_TRGT_WEIGHT DMA Write Channel MRd Requests. For DMA data requests and LL element/descriptor access. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
2:0	RW	0x0	RTRGT1_WEIGHT Non-DMA Rx Requests. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_CTRL_OFF

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	DIS_C2W_CACHE_RD Disable DMA Read Channels "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
24	RW	0x0	DIS_C2W_CACHE_WR Disable DMA Write Channels "completion to memory write" context cache pre-fetch function. Note: For internal debugging only. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	RO	0x1	NUM_DMA_RD_CHAN Number of Read Channels. You can read this register to determine the number of read channels the DMA controller has been configured to support.
15:4	RO	0x000	reserved
3:0	RO	0x1	NUM_DMA_WR_CHAN Number of Write Channels. You can read this register to determine the number of write channels the DMA controller has been configured to support.

DMA_WRITE_ENGINE_EN_OFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Write Engine Channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
22	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Write Engine Channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
21	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Write Engine Channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
20	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Write Engine Channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
19	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Write Engine Channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
18	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Write Engine Channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
17	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Write Engine Channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
16	RW	0x0	DMA_WRITE_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Write Engine Channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	DMA_WRITE_ENGINE DMA Write Engine Enable. 1: Enable 0: Disable (Soft Reset) For normal operation, you must initially set this bit to "1", before any other software setup actions. You do not need to toggle or rewrite to this bit during normal operation. You should set this bit to "0" when you want to "Soft Reset" the DMA controller write logic. There are three possible reasons for resetting the DMA controller write logic: The "Abort Interrupt Status" bit is set (in the "DMA Write Interrupt Status Register" DMA_WRITE_INT_STATUS_OFF), and any of the bits is in the "DMA Write Error Status Register" (DMA_WRITE_ERR_STATUS_OFF) are set. Resetting the DMA controller write logic re-initializes the control logic, ensuring that the next DMA write transfer is executed successfully. You have executed the procedure outlined in "Stop Bit" , after which, the "Abort Interrupt Status" bit is set and the Channel Status field (CS) of the DMA write "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_WRCH_0) is set to "Stopped." Resetting the DMA controller write logic re-initializes the control logic ensuring that the next DMA write transfer is executed successfully. During software development, when you incorrectly program the DMA write engine. To "Soft Reset" the DMA controller write logic, you must: De-assert the DMA write engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA write engine enable bit returns a "0". Assert the DMA write engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA write transfer does not start until you write to the "DMA Write Doorbell Register" (DMA_WRITE_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_DOORBELL_OFF

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	WR_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA write channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_WRCH_0) to ensure that the write channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)." Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
30:3	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	WR_DOORBELL_NUM Doorbell Number. You must write the channel number to this register to start the DMA write transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. You do not need to toggle or write any other value to this register to start a new transfer. The range of this field is 0x0 to 0x7, and 0x0 corresponds to channel 0. Also note that a write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CHANNEL_ARB_WEIGHT_LOW_OFF

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x01	WRITE_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
14:10	RW	0x01	WRITE_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
9:5	RW	0x01	WRITE_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
4:0	RW	0x01	WRITE_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	WRITE_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
14:10	RW	0x00	WRITE_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
9:5	RW	0x00	WRITE_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
4:0	RW	0x00	WRITE_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. A value of '0' means that one TLP is issued before moving to the next channel. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_ENGINE_EN_OFF

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH7 Enable Handshake for DMA Read Engine Channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
22	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH6 Enable Handshake for DMA Read Engine Channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
21	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH5 Enable Handshake for DMA Read Engine Channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
20	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH4 Enable Handshake for DMA Read Engine Channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
19	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH3 Enable Handshake for DMA Read Engine Channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
18	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH2 Enable Handshake for DMA Read Engine Channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
17	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH1 Enable Handshake for DMA Read Engine Channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
16	RW	0x0	DMA_READ_ENGINE_EN_HSHAKE_CH0 Enable Handshake for DMA Read Engine Channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	DMA_READ_ENGINE DMA Read Engine Enable. 1: Enable 0: Disable (Soft Reset) For normal operation, you must initially set this bit to "1", before any other software setup actions. You do not need to toggle or rewrite to this bit during normal operation. You should set this field to "0" when you want to "Soft Reset" the DMA controller read logic. There are three possible reasons for resetting the DMA controller read logic: The "Abort Interrupt Status" bit is set (in the "DMA Read Interrupt Status Register" (DMA_READ_INT_STATUS_OFF), and any of the bits in the "DMA Read Error Status Low Register" (DMA_READ_ERR_STATUS_LOW_OFF) is set. Resetting the DMA controller read logic re-initializes the control logic, ensuring that the next DMA read transfer is executed successfully. You have executed the procedure outlined in "Stop Bit", after which, the "Abort Interrupt Status" bit is set and the channel Status field (CS) of the DMA read "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_WRCH_0) is set to "Stopped". Resetting the DMA controller read logic re-initializes the control logic ensuring that the next DMA read transfer is executed successfully. During software development, when you incorrectly program the DMA read engine. To "Soft Reset" the DMA controller read logic, you must: De-assert the DMA read engine enable bit. Wait for the DMA to complete any in-progress TLP transfer, by waiting until a read on the DMA read engine enable bit returns a "0". Assert the DMA read engine enable bit. This "Soft Reset" does not clear the DMA configuration registers. The DMA read transfer does not start until you write to the "DMA Read Doorbell Register" (DMA_READ_DOORBELL_OFF). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_DOORBELL_OFF

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31	RW	0x0	RD_STOP Stop. Set in conjunction with the Doorbell Number field. The DMA read channel stops issuing requests, sets the channel status to "Stopped", and asserts the "Abort" interrupt if it is enabled. Before setting the Stop bit, you must read the channel Status field (CS) of the "DMA Channel Control 1 Register " (DMA_CH_CONTROL1_OFF_RDCH_0) to ensure that the read channel is "Running" (transferring data). For more information, see "Stopping the DMA Transfer (Software Stop)". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
30:3	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	RD_DOORBELL_NUM Doorbell Number. You must write 0x0 to this register to start the DMA read transfer for that channel. The DMA detects a write to this register field even if the value of this field does not change. The range of this field is 0x0 to 0x7, and 0x0 corresponds to channel 0. Also note that a write to this field triggers the controller to exit L1 substates. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CHANNEL_ARB_WEIGHT_LOW_OFF

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x01	READ_CHANNEL3_WEIGHT Channel 3 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
14:10	RW	0x01	READ_CHANNEL2_WEIGHT Channel 2 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
9:5	RW	0x01	READ_CHANNEL1_WEIGHT Channel 1 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
4:0	RW	0x01	READ_CHANNEL0_WEIGHT Channel 0 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CHANNEL_ARB_WEIGHT_HIGH_OFF

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x01	READ_CHANNEL7_WEIGHT Channel 7 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
14:10	RW	0x01	READ_CHANNEL6_WEIGHT Channel 6 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
9:5	RW	0x01	READ_CHANNEL5_WEIGHT Channel 5 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
4:0	RW	0x01	READ_CHANNEL4_WEIGHT Channel 4 Weight. The weight is initialized by software before ringing the doorbell. The value is used by the channel weighted round robin arbiter to select the next channel read request. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_INT_STATUS_OFF

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	WR_ABORT_INT_STATUS Abort Interrupt Status. The DMA write channel has detected an error, or you manually stopped the transfer as described in "Error Handling Assistance by Remote Software". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	WR_DONE_INT_STATUS Done Interrupt Status. The DMA write channel has successfully completed the DMA transfer. For more details, see "Interrupts and Error Handling". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA write interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_INT_MASK_OFF

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	WR_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved
0	RW	0x1	WR_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA write interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_INT_CLEAR_OFF

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	WR_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a "0".
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	WO	0x0	WR_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA write interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a "0".

DMA_WRITE_ERR_STATUS_OFF

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	LINKLIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Write Interrupt Clear Register" (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit. Value After Reset: 0x0
15:8	RO	0x00	reserved
7:0	RO	0x00	APP_READ_ERR_DETECT Application Read Error Detected. The DMA write channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while reading data from it. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA write interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Write Interrupt Clear Register" (DMA_WRITE_INT_CLEAR_OFF) to clear this error bit.

DMA_WRITE_DONE_IMWR_LOW_OFF

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Done IMWr TLP. Bits [1:0] must be "00" as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_DONE_IMWR_HIGH_OFF

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_DONE_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_ABORT_IMWR_LOW_OFF

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_WRITE_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP it generates. Bits [1:0] must be "00" as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_ABORT_IMWR_HIGH_OFF

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_WRITE_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CH01_IMWR_DATA_OFF

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	WR_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CH23_IMWR_DATA_OFF

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	WR_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CH45_IMWR_DATA_OFF

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	WR_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_CH67_IMWR_DATA_OFF

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	WR_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	WR_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for write channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_LINKED_LIST_ERR_EN_OFF

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	WR_CHANNEL_LLLAIE Write Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the write channel local abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	WR_CHANNEL_LLRAIE Write Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the write channel remote abort interrupt through this bit. The LIE and RIE bits in the LL element enable the write channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_INT_STATUS_OFF

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	RD_ABORT_INT_STATUS Abort Interrupt Status. The DMA read channel has detected an error, or you manually stopped the transfer as described in "Stopping the DMA Transfer (Software Stop)". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. You can read the "DMA Read Error Status Low Register" (DMA_READ_ERR_STATUS_LOW_OFF) and "DMA Read Error Status High Register" (DMA_READ_ERR_STATUS_HIGH_OFF) to determine the source of the error. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:8	RO	0x00	reserved
7:0	RW	0x00	RD_DONE_INT_STATUS Done Interrupt Status. The DMA read channel has successfully completed the DMA read transfer. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the DMA read interrupt Clear register to clear this interrupt bit. Note: You can write to this register to emulate interrupt generation, during software or hardware testing. A write to the address triggers an interrupt, but the DMA does not set the Done or Abort bits in this register. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_INT_MASK_OFF

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	RD_ABORT_INT_MASK Abort Interrupt Mask. Prevents the Abort interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved
0	RW	0x1	RD_DONE_INT_MASK Done Interrupt Mask. Prevents the Done interrupt status field in the DMA read interrupt status register from asserting the edma_int output. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_INT_CLEAR_OFF

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	WO	0x00	RD_ABORT_INT_CLEAR Abort Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Abort interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a "0".
15:8	RO	0x00	reserved
7:0	WO	0x00	RD_DONE_INT_CLEAR Done Interrupt Clear. You must write a 1'b1 to clear the corresponding bit in the Done interrupt status field of the DMA read interrupt status register. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Note: Reading from this self-clearing register field always returns a "0".

DMA_READ_ERR_STATUS_LOW_OFF

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RO	0x00	LINK_LIST_ELEMENT_FETCH_ERR_DETECT Linked List Element Fetch Error Detected. The DMA read channel has received an error response from the AXI bus while reading a linked list element from local memory. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF).
15:8	RO	0x00	reserved
7:0	RO	0x00	APP_WR_ERR_DETECT Application Write Error Detected. The DMA read channel has received an error response from the AXI bus (or TRGT1 interface when the AXI Bridge is not used) while writing data to it. This error is fatal. You must restart the transfer from the beginning, as the channel context is corrupted, and the transfer is not rolled back. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this clears all bits in this register, and also the DMA Read Error Status High register (DMA_READ_ERR_STATUS_HIGH_OFF).

DMA_READ_ERR_STATUS_HIGH_OFF

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	DATA_POISIONING Data Poisoning. The DMA read channel has detected data poisoning in the completion from the remote device (in response to the MRd request). The DMA read channel will drop the completion and then be halted. The CX_FLT_MASK_UR_POIS filter rule does not affect this behavior. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register.

Bit	Attr	Reset Value	Description
23:16	RO	0x00	CPL_TIMEOUT Completion Time Out. The DMA read channel has timed-out while waiting for the remote device to respond to the MRd request, or a malformed CplD has been received. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling" . Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register.
15:8	RO	0x00	CPL_ABORT Completer Abort. The DMA read channel has received a PCIe completer abort completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register.
7:0	RO	0x00	UNSUPPORTED_REQ Unsupported Request. The DMA read channel has received a PCIe unsupported request completion status from the remote device in response to the MRd request. For more details, see "Linked List Mode". Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Enabling: For details, see "Interrupts and Error Handling". Masking: The DMA read interrupt Mask register has no effect on this register. Clearing: You must write a 1'b1 to the corresponding channel bit in the Abort interrupt field of the "DMA Read Interrupt Clear Register" (DMA_READ_INT_CLEAR_OFF) to clear this error bit. Note, this also clears the other error bits for the same channel in this register and in the DMA Read Error Status Low register.

DMA_READ_LINKED_LIST_ERR_EN_OFF

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	RD_CHANNEL_LLLAIE Read Channel LL Local Abort Interrupt Enable (LLLAIE). You enable the read channel Local Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:1	RO	0x0000	reserved
0	RW	0x0	RD_CHANNEL_LLRAIE Read Channel LL Remote Abort Interrupt Enable (LLRAIE). You enable the read channel Remote Abort interrupt through this bit. The LIE and RIE bits in the LL element enable the read channel done interrupts. Each bit corresponds to a DMA channel. Bit [0] corresponds to channel 0. Used in linked list mode only. For more details, see "Interrupt Handling". Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_DONE_IMWR_LOW_OFF

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Done IMWr TLP. Bits [1:0] must be "00" as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_DONE_IMWR_HIGH_OFF

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_DONE_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Done IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_ABORT_IMWR_LOW_OFF

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_LOW_REG The DMA uses this field to generate bits [31:0] of the address field for the Abort IMWr TLP. Bits [1:0] must be "00" as this address must be dword aligned. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_ABORT_IMWR_HIGH_OFF

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_READ_ABORT_HIGH_REG The DMA uses this field to generate bits [63:32] of the address field for the Abort IMWr TLP. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CH01_IMWR_DATA_OFF

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_1_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 1. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	RD_CHANNEL_0_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 0. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CH23_IMWR_DATA_OFF

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_3_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 3. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	RD_CHANNEL_2_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 2. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CH45_IMWR_DATA_OFF

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_5_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 5. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	RD_CHANNEL_4_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 4. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_READ_CH67_IMWR_DATA_OFF

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	RD_CHANNEL_7_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 7. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
15:0	RW	0x0000	RD_CHANNEL_6_DATA The DMA uses this field to generate the data field for the Done or Abort IMWr TLPs it generates for read channel 6. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_WRITE_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH3 DMA handshake counter for DMA Write Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Write Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Write Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Write Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.

DMA_WRITE_ENGINE_HSHAKE_CNT_HIGH_OFF

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Write Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Write Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Write Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_WRITE_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Write Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.

DMA_READ_ENGINE_HSHAKE_CNT_LOW_OFF

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Read Engine Channel 3. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH2 DMA handshake counter for DMA Read Engine Channel 2. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH1 DMA handshake counter for DMA Read Engine Channel 1. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
7:5	RO	0x0	reserved
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH0 DMA handshake counter for DMA Read Engine Channel 0. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.

DMA_READ_ENGINE_HSHAKE_CNT_HIGH_OFF

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH7 DMA handshake counter for DMA Read Engine Channel 7. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
23:21	RO	0x0	reserved
20:16	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH6 DMA handshake counter for DMA Read Engine Channel 6. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
15:13	RO	0x0	reserved
12:8	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH5 DMA handshake counter for DMA Read Engine Channel 5. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RO	0x00	DMA_READ_ENGINE_HSHAKE_CNT_CH4 DMA handshake counter for DMA Read Engine Channel 4. If CC_DMA_HSHAKE =1, the data transfer in Linked List mode starts only when the counter is non-zero.

DMA_CH_CONTROL1_OFF_WRCH_0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit (DMA_NS_SRC). The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit (DMA_NS_DST). The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
22:17	RO	0x00	reserved
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the "DMA Write Channel Control 2 Register" (DMA_CH_CONTROL2_OFF_WRCH_0). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
11:10	RO	0x0	reserved
9	RW	0x0	LLE Linked List Enable (LLE). 0: Disable linked list operation 1: Enable linked list operation Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
7	RO	0x0	reserved
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: 00: Reserved 01: Running. This channel is active and transferring data. 10: Halted. An error condition has been detected, and the DMA has stopped this channel. 11: Stopped. The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the "DMA Write Doorbell Register" (DMA_WRITE_DOORBELL_OFF) or "DMA Read Doorbell Register" (DMA_READ_DOORBELL_OFF).
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. this field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_TRANSFER_SIZE_OFF_WRCH_0

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA write channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_SAR_LOW_OFF_WRCH_0

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (Lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Write: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_SAR_HIGH_OFF_WRCH_0

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_DAR_LOW_OFF_WRCH_0

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (Lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Write: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_DAR_HIGH_OFF_WRCH_0

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_LLP_LOW_OFF_WRCH_0

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_LLP_HIGH_OFF_WRCH_0

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Upper 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_CH_CONTROL1_OFF_RDCH_0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	DMA_AT Address Translation TLP Header Bit (AT) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
29:27	RW	0x0	DMA_TC Traffic Class TLP Header Bit (TC) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
26	RO	0x0	reserved
25	RW	0x0	DMA_RO Relaxed Ordering TLP Header Bit (RO) The DMA uses this TLP header field when generating MRd/MWr (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
24	RW	0x0	DMA_NS_SRC Source No Snoop TLP Header Bit (DMA_NS_SRC). The DMA uses this TLP header field when generating MRd (SAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
23	RW	0x0	DMA_NS_DST Destination No Snoop TLP Header Bit (DMA_NS_DST). The DMA uses this TLP header field when generating MWr (DAR addressing space) (not IMWr) TLPs. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
22:17	RO	0x00	reserved
16:12	RW	0x00	DMA_FUNC_NUM Function Number (FN). The controller uses this field when generating the requester ID for the MRd/MWr DMA TLP. When you have enabled SR-IOV, then this field is ignored if you have set the VFE field in the "DMA Read Channel Control 2 Register" (DMA_CH_CONTROL2_OFF_RDCH_0). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
11:10	RO	0x0	reserved
9	RW	0x0	LLE Linked List Enable (LLE). 0: Disable linked list operation 1: Enable linked list operation Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
8	RW	0x0	CCS Consumer Cycle State (CCS). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". You must initialize this bit. The DMA updates this bit during linked list operation. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RO	0x0	CS Channel Status (CS). The channel status bits identify the current operational state of the DMA channel. The operation state encoding for each DMA channel is a s follows: 00: Reserved 01: Running. This channel is active and transferring data. 10: Halted. An error condition has been detected, and the DMA has stopped this channel. 11: Stopped. The DMA has transferred all data for this channel, or you have prematurely stopped this channel by writing to the Stop field of the "DMA Read Doorbell Register" (DMA_WRITE_DOORBELL_OFF) or "DMA Read Doorbell Register" (DMA_READ_DOORBELL_OFF).
4	RW	0x0	RIE Remote Interrupt Enable (RIE). You must set this bit to enable the generation of the Done or Abort Remote interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the RIE of the LL element. The RIE bit in a LL element only enables the Done interrupt. In non-LL mode, the RIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
3	RW	0x0	LIE Local Interrupt Enable (LIE). You must set this bit to enable the generation of the Done or Abort Local interrupts. For more details, see "Interrupts and Error Handling". In LL mode, the DMA overwrites this with the LIE of the LL element. The LIE bit in a LL element only enables the Done interrupt. In non-LL mode, the LIE bit enables the Done and Abort interrupts. This field is not defined in a link LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
2	RW	0x0	LLP Load Link Pointer (LLP). Used in linked list mode only. Indicates that this linked list element is a link element, and its LL element pointer dwords are pointing to the next (non-contiguous) element. The DMA loads this field with the LLP of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W
1	RW	0x0	TCB Toggle Cycle Bit (TCB). Indicates to the DMA to toggle its interpretation of the CB. Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the TCB of the linked list element. this field is not defined in a data LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

Bit	Attr	Reset Value	Description
0	RW	0x0	CB Cycle Bit (CB). Used in linked list mode only. It is used to synchronize the producer (software) and the consumer (DMA). For more details, see "PCS-CCS-CB-TCB Producer-Consumer Synchronization". The DMA loads this field with the CB of the linked list element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_TRANSFER_SIZE_OFF_RDCH_0

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_TRANSFER_SIZE DMA Transfer Size. You program this register with the size of the DMA transfer. The maximum DMA transfer size is 4Gbytes. The minimum transfer size is one byte (0x1). This field is automatically decremented by the DMA as the DMA read channel transfer progresses. This field indicates the number bytes remaining to be transferred. When all bytes are successfully transferred the current transfer size is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element. You can read this register to monitor the transfer progress, however in some scenarios this register is updated after a delay. For example, when less than 3 channels are doorbelled, this register is updated only after a descriptor finishes(linked list mode), or the transfer ends (non-linked list mode). Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_SAR_LOW_OFF_RDCH_0

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_LOW Source Address Register (Lower 32 bits). Indicates the next address to be read from. The DMA increments the SAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The SAR is the address of the remote memory. DMA Read: The SAR is the address of the local memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_SAR_HIGH_OFF_RDCH_0

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRC_ADDR_REG_HIGH Source Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_DAR_LOW_OFF_RDCH_0

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_LOW Destination Address Register (Lower 32 bits). Indicates the next address to be written to. The DMA increments the DAR as the DMA transfer progresses. In LL mode, the DMA overwrites this with the corresponding dword of the LL element. DMA Read: The DAR is the address of the local memory. DMA Read: The DAR is the address of the remote memory. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_DAR_HIGH_OFF_RDCH_0

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DST_ADDR_REG_HIGH Destination Address Register (Higher 32 bits). In LL mode, the DMA overwrites this with the corresponding dword of the LL element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_LLP_LOW_OFF_RDCH_0

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_LOW Lower bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list after the previous element is consumed. When the current element is a data element; this field is incremented by 6 DWORDS. When the current element is a link element; this field is overwritten by the LL Element Pointer of the element. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

DMA_LLP_HIGH_OFF_RDCH_0

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LLP_HIGH Upper 32 bits of the address of the linked list transfer list in local memory. Used in linked list mode only. Updated by the DMA to point to the next element in the transfer list as elements are consumed. Note: The access attributes of this field are as follows: Wire: R/W Dbi: R/W

18.4.6 ATU Registers Summary

Name	Offset	Size	Reset Value	Description
IATU_REGION_CTRL_1_OFF_OUTBOUND_i	0x0000	W	0x00000000	iATU Region Control 1 Register. (for i = 0; i <= 15)
IATU_REGION_CTRL_2_OFF_OUTBOUND_i	0x0004	W	0x00000000	iATU Region Control 2 Register. (for i = 0; i <= 15)
IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i	0x0008	W	0x00000000	iATU Lower Base Address Register. (for i = 0; i <= 15)
IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i	0x000C	W	0x00000000	iATU Upper Base Address Register. (for i = 0; i <= 15)
IATU_LIMIT_ADDR_OFF_OUTBOUND_i	0x0010	W	0x0000FFFF	iATU Limit Address Register. (for i = 0; i <= 15)
IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i	0x0014	W	0x00000000	iATU Lower Target Address Register. (for i = 0; i <= 15)
IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i	0x0018	W	0x00000000	iATU Upper Target Address Register. (for i = 0; i <= 15)
IATU_REGION_CTRL_1_OFF_INBOUND_i	0x0100	W	0x00000000	iATU Region Control 1 Register. (for i = 0; i <= 15)
IATU_REGION_CTRL_2_OFF_INBOUND_i	0x0104	W	0x00000000	iATU Region Control 2 Register. (for i = 0; i <= 15)
IATU_LWR_BASE_ADDR_OFF_INBOUND_i	0x0108	W	0x00000000	iATU Lower Base Address Register. (for i = 0; i <= 15)
IATU_UPPER_BASE_ADDR_OFF_INBOUND_i	0x010C	W	0x00000000	iATU Upper Base Address Register. (for i = 0; i <= 15)
IATU_LIMIT_ADDR_OFF_INBOUND_i	0x0110	W	0x0000FFFF	iATU Limit Address Register. (for i = 0; i <= 15)
IATU_LWR_TARGET_ADDR_OFF_INBOUND_i	0x0114	W	0x00000000	iATU Lower Target Address Register. (for i = 0; i <= 15)

18.4.7 ATU Detail Registers Description

IATU_REGION_CTRL_1_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register. Note: This register field is sticky.
8	RW	0x0	TD This is a reserved field. Do not use.

Bit	Attr	Reset Value	Description
7:5	RW	0x0	TC When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. Note: This register field is sticky.

IATU_REGION_CTRL_2_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RO	0x0	reserved
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. The iATU uses bits [27:12] of the untranslated address (on the XALI0/1/2 interface or AXI slave interface address) to form the BDF number of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism (Section 7.2.2 of the PCI Express Base 3.1 Specification, revision 1.0) by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space. Note: This register field is sticky.
27	RW	0x0	DMA_BYPASS DMA Bypass Mode. Allows request TLPs which are initiated by the DMA controller to pass through the iATU untranslated. Note: This register field is sticky.
26:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	HEADER_SUBSTITUTE_EN Header Substitute Enable. When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. 1: LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register is used to fill bytes 8-to-11 (for 3 DWORD header) or bytes 12-to-15 (for 4 DWORD header) of the translated TLP header. 0: LWR_TARGET_RW in the iATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i register forms the new address of the translated region. Note: This register field is sticky.
22	RW	0x0	INHIBIT_PAYLOAD Inhibit TLP Payload Data for TLP's in Matched Region; assign iATU region to be TLP without data. When enabled and region address is matched, the iATU marks all TLPs as having no payload data by forcing the TLP header Fmt[1] bit =0, regardless of the application inputs such as slv_wstrb. 1: Fmt[1] =0 so that only TLP type without data is sent. For example, a Msg instead of MsgD will be sent. 0: Fmt[1] =0/1 so that TLPs with or without data can be sent. Note: This register field is sticky.
21	RO	0x0	reserved
20	RW	0x0	SNP Serialize Non-Posted Requests. In this mode, when the AXI Bridge is populated, same AXI ID Non-Posted Read/Write Requests are transmitted on the wire if there are no other same ID Non-Posted Requests outstanding. Note: This register field is sticky.
19	RW	0x0	FUNC_BYPASS Function Number Translation Bypass. In this mode, the function number of the translated TLP is taken from your application transmit interface and not from the CTRL_1_FUNC_NUM field of the "iATU Control 1 Register" or the VF_NUMBER field of the "iATU Control 3 Register." Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	TAG_SUBSTITUTE_EN TAG Substitute Enable. When enabled and region address is matched, the iATU substitutes the TAG field of the outbound TLP header with the contents of the TAG field in this register. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Note: This register field is sticky.
15:8	RW	0x00	TAG TAG. The substituted TAG field (byte 6) in the outgoing TLP header when TAG_SUBSTITUTE_EN is set. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	MSG_CODE MSG TLPs (Message Code). When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the message field of the TLP is changed to the value in this register. Note: This register field is sticky.

IATU_LWR_BASE_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

IATU_UPPER_BASE_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. In systems with a 32-bit address space, this register is not used and therefore writing to this register has no effect. Note: This register field is sticky.

IATU_LIMIT_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:0	RW	0xffff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller.

IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LWR_TARGET_RW_OUTBOUND When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_ is '0' (normal operation): LWR_TARGET_RW[31:n] forms MSB's of the Lower Target part of the new address of the translated region; LWR_TARGET_RW[n-1:0] are not used. (The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so the lower bits of the start address of the new address of the translated region (bits n-1:0) are always '0'). n is log2(CX_ATU_MIN_REGION_SIZE). When HEADER_SUBSTITUTE_EN in IATU_REGION_CTRL_2_OFF_OUTBOUND_i is '1': LWR_TARGET_RW[31:0] forms bytes 8-11 (for 3 dword header) or bytes 12-15 (for 4 dword header) of the outbound TLP header. Usage scenarios include the transmission of Vendor Defined Messages where the controller determines the content of bytes 12 to 15 of the TLP header. Note: This register field is sticky.

IATU_UPPER_TARGET_ADDR_OFF_OUTBOUND_i

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_TARGET_RW Forms bits [63:32] of the start address (Upper Target part) of the new address of the translated region. Note: This register field is sticky.

IATU_REGION_CTRL_1_OFF_INBOUND_i

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	CTRL_1_FUNC_NUM Function Number. Note: This register field is sticky.
19:14	RO	0x00	reserved
13	RW	0x0	INCREASE_REGION_SIZE Increase the maximum ATU Region size. When set, the maximum ATU Region size is determined by CX_ATU_MAX_REGION_SIZE. When clear, the maximum ATU Region size is 4 GB (default). Note: This register field is sticky.
12:11	RO	0x0	reserved
10:9	RW	0x0	ATTR When the ATTR field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "ATTR Match Enable" bit of the "iATU Control 2 Register" is set. Note: This register field is sticky.
8	RW	0x0	TD When the TD field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TD Match Enable" bit of the "iATU Control 2 Register" is set. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
7:5	RW	0x0	TC When the TC field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "TC Match Enable" bit of the "iATU Control 2 Register" is set. Note: This register field is sticky.
4:0	RW	0x00	TYPE When the TYPE field of an inbound TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). Note: This register field is sticky.

IATU_REGION_CTRL_2_OFF_INBOUND_i

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	REGION_EN Region Enable. This bit must be set to '1' for address translation to take place. Note: This register field is sticky.
30	RW	0x0	MATCH_MODE Match Mode. Determines Inbound matching mode for TLPs. The mode depends on the type of TLP that is received as follows: For MEM-I/O TLPs, this field is interpreted as follows: 0: Address Match Mode. The iATU operates using addresses as in the outbound direction. The Region Base and Limit Registers must be setup. 1:BAR Match Mode. BAR matching is used. The "BAR Number" field is relevant. Not used for RC. For CFG0 TLPs, this field is interpreted as follows: 0: Routing ID Match Mode. The iATU interprets the Routing ID (Bytes 8 to 11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM-I/O transactions. The Routing ID of the TLP must be within the base and limit of the iATU region for matching to proceed. 1: Accept Mode. The iATU accepts all CFG0 transactions as address matches. The routing ID in the CFG0 TLP is ignored. This is useful as all received CFG0 TLPs should be processed regardless of the Bus number. For MSG/MSGD TLPs, this field is interpreted as follows: 0: Address Match Mode. The iATU treats the third dword and fourth dword of the inbound MSG/MSGD TLP as an address and it is matched against the Region Base and Limit Registers. 1: Vendor ID Match Mode. This mode is relevant for ID-routed Vendor Defined Messages. The iATU ignores the Routing ID (Bus, Device, Function) in bits [31:16] of the third dword of the TLP header, but matches against the Vendor ID in bits [15:0] of the third dword of the TLP header. Bits [15:0] of the Region Upper Base register should be programmed with the required Vendor ID. The lower Base and Limit Register should be programmed to translate TLPs based on vendor specific information in the fourth dword of the TLP header.

Bit	Attr	Reset Value	Description
29	RW	0x0	INVERT_MODE Invert Mode. When set the address matching region is inverted. Therefore, an address match occurs when the untranslated address is in the region outside the defined range (Base Address to Limit Address). Note: This register field is sticky.
28	RW	0x0	CFG_SHIFT_MODE CFG Shift Mode. This is useful for CFG transactions where the PCIe configuration mechanism maps bits [27:12] of the address to the bus/device and function number. This allows a CFG configuration space to be located in any 256MB window of your application memory space using a 28-bit effective address. Shifts bits [31:16] of the untranslated address to form bits [27:12] of the translated address. Note: This register field is sticky.
27	RW	0x0	FUZZY_TYPE_MATCH_CODE Fuzzy Type Match Mode. When enabled, the iATU relaxes the matching of the TLP TYPE field against the expected TYPE field so that CfgRd0 and CfgRd1 TLPs are seen as identical. Similarly with CfgWr0 and CfgWr1. MWr, MRd and MRdLk TLPs are seen as identical The Routing field of Msg/MsgD TLPs is ignored FetchAdd, Swap and CAS are seen as identical. For example, CFG0 in the TYPE field in the "iATU Control 1 Register" matches against an inbound CfgRd0, CfgRd1, CfgWr0 or CfgWr1 TLP. Note: This register field is sticky.
26	RO	0x0	reserved
25:24	RW	0x0	RESPONSE_CODE Response Code. Defines the type of response to give for accesses matching this region. This overrides the normal RADM filter response. Note that this feature is not available for any region where Single Address Location Translate is enabled. 00 - Normal RADM filter response is used. 01 - Unsupported request (UR) 10 - Completer abort (CA) 11 - Not used / undefined / reserved. Note: This register field is sticky.
23	RW	0x0	SINGLE_ADDR_LOC_TRANS_EN Single Address Location Translate Enable. When enabled, Rx TLPs can be translated to a single address location as determined by the target address register of the iATU region. The main usage scenario is translation of Messages (such as Vendor Defined or ATS Messages) to MWr TLPs when the AXI bridge is enabled. Note: This register field is sticky.
22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21	RW	0x0	MSG_CODE_MATCH_EN Message Code Match Enable (Msg TLPS). Ensures that a successful message Code TLP field comparison match (see Message Code field of the "iATU Control 2 Register") occurs (in MSG transactions) for address translation to proceed. ST Match Enable (Mem TLPs). Ensures that a successful ST TLP field comparison match (see ST field of the "iATU Control 2 Register") occurs (in MEM transactions) for address translation to proceed. Only Valid when the CX_TPH_ENABLE configuration parameter is 1 Note: This register field is sticky.
20	RO	0x0	reserved
19	RW	0x0	FUNC_NUM_MATCH_EN Function Number Match Enable. Ensures that a successful Function Number TLP field comparison match (see Function Number field of the "iATU Control 1 Register") occurs (in MEM-I/O and CFG0/CFG1 transactions) for address translation to proceed. Note: This register field is sticky.
18:17	RO	0x0	reserved
16	RW	0x0	ATTR_MATCH_EN ATTR Match Enable. Ensures that a successful ATTR TLP field comparison match (see ATTR field of the "iATU Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
15	RW	0x0	TD_MATCH_EN TD Match Enable. Ensures that a successful TD TLP field comparison match (see TD field of the "iATU Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
14	RW	0x0	TC_MATCH_EN TC Match Enable. Ensures that a successful TC TLP field comparison match (see TC field of the "iATU Control 1 Register") occurs for address translation to proceed. Note: This register field is sticky.
13	RW	0x0	MSG_TYPE_MATCH_MODE Message Type Match Mode. When enabled, and if single address location translate enable is set, then inbound TLPs of type MSG/MSGd which match the type field of the iatu_region_ctrl_1_OFF_inbound register (=>TYPE[4:3]=2'b10) will be translated. Message type match mode overrides any value of MATCH_MODE field in this register. Usage scenarios for this are translation of VDM or ATS messages when AXI bridge is configured on client interface. Note: This register field is sticky.
12:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	BAR_NUM BAR Number. When the BAR number of an inbound MEM or IO TLP " that is matched by the normal internal BAR address matching mechanism " is the same as this field, address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Match Mode" bit of the "iATU Control 2 Register" is set. 000b - BAR0 001b - BAR1 010b - BAR2 011b - BAR3 100b - BAR4 101b - BAR5 110b - ROM 111b - reserved IO translation would require either 00100b or 00101b in the inbound TLP TYPE; the BAR Number set in the range 000b - 101b and that BAR configured as an IO BAR. Note: This register field is sticky.
7:0	RW	0x00	MSG_CODE MSG TLPs: (Message Code). When the TYPE field of an inbound Msg/MsgD TLP is matched to this value, then address translation proceeds (when all other enabled field-matches are successful). This check is only performed if the "Message Code Match Enable" bit of the "iATU Control 2 Register" is set. Note: This register field is sticky.

IATU_LWR_BASE_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_BASE_RW Forms bits [31:n] of the start address of the address region to be translated. n is log2(CX_ATU_MIN_REGION_SIZE) Note: This register field is sticky.
15:0	RO	0x0000	LWR_BASE_HW Forms bits [n-1:0] of the start address of the address region to be translated. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always 0. A write to this location is ignored by the PCIe controller. n is log2(CX_ATU_MIN_REGION_SIZE)

IATU_UPPER_BASE_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UPPER_BASE_RW Forms bits [63:32] of the start (and end) address of the address region to be translated. Note: This register field is sticky.

IATU_LIMIT_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LIMIT_ADDR_RW Forms upper bits of the end address of the address region to be translated. Note: This register field is sticky.
15:0	RO	0xffff	LIMIT_ADDR_HW Forms lower bits of the end address of the address region to be translated. The end address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary, so these bits are always all ones. A write to this location is ignored by the PCIe controller.

IATU_LWR_TARGET_ADDR_OFF_INBOUND_i

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	LWR_TARGET_RW Forms MSB's of the Lower Target part of the new address of the translated region. These bits are always '0'. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode. Note: This register field is sticky.
15:0	RO	0x0000	LWR_TARGET_HW Forms the LSB's of the Lower Target part of the new address of the translated region. The start address must be aligned to a CX_ATU_MIN_REGION_SIZE kB boundary (in address match mode); and to the Bar size boundary (in BAR match mode) so that these bits are always '0'. If the BAR is smaller than the iATU region size, then the iATU target address must align to the iATU region size; otherwise it must align to the BAR size. A write to this location is ignored by the PCIe controller. Field size depends on log2(CX_ATU_MIN_REGION_SIZE) in address match mode. Field size depends on log2(BAR_MASK+1) in BAR match mode.

18.4.8 Port Logic Registers Summary

Name	Offset	Size	Reset Value	Description
PL_ACK_LATENCY_TIMER_OFF	0x0700	W	0x18460817	Ack Latency Timer and Replay Timer Register.
PL_VENDOR_SPEC_DLLP_OFF	0x0704	W	0xFFFFFFFF	Vendor Specific DLLP Register.
PL_PORT_FORCE_OFF	0x0708	W	0x00000004	PORT_FORCE_OFF
PL_ACK_F_ASPM_CTRL_OFF	0x070C	W	0x1BFFFF00	Ack Frequency and L0-L1 ASPM Control Register.
PL_PORT_LINK_CTRL_OFF	0x0710	W	0x00030120	Port Link Control Register.
PL_LANE_SKEW_OFF	0x0714	W	0x08000000	Lane Skew Register.
PL_TIMER_CTRL_MAX_FUNC_NUM_OFF	0x0718	W	0x00000000	Timer Control and Max Function Number Register.
PL_SYMBOL_TIMER_FILTER_1_OFF	0x071C	W	0x00000280	Symbol Timer Register and Filter Mask 1 Register. The Filter Mask 1 Register modifies the RADM filtering and error handling rules. For more details, see the "Receive Filtering" section.

Name	Offset	Size	Reset Value	Description
PL_FILTER_MASK_2_OFF	0x0720	W	0x00000000	Filter Mask 2 Register. This register modifies the RADM filtering and error handling rules.
PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF	0x0724	W	0x00000001	AMBA Multiple Outbound Decomposed NP SubRequests Control Register.
PL_PL_DEBUG0_OFF	0x0728	W	0x00000000	Debug Register 0
PL_PL_DEBUG1_OFF	0x072C	W	0x00000000	Debug Register 1
PL_TX_P_FC_CREDIT_STATUS_OFF	0x0730	W	0x00000000	Transmit Posted FC Credit Status
PL_TX_NP_FC_CREDIT_STATUS_OFF	0x0734	W	0x00000000	TX_NP_FC_CREDIT_STATUS_OFF
PL_TX_CPL_FC_CREDIT_STATUS_OFF	0x0738	W	0x00000000	Transmit Completion FC Credit Status
PL_QUEUE_STATUS_OFF	0x073C	W	0x00000000	Queue Status
PL_VC_TX_ARBI_1_OFF	0x0740	W	0x0000000F	VC Transmit Arbitration Register 1
PL_VC_TX_ARBI_2_OFF	0x0744	W	0x00000000	VC Transmit Arbitration Register 2
PL_VC0_P_RX_Q_CTRL_OFF	0x0748	W	0x45027048	Segmented-Buffer VC0 Posted Receive Queue Control.
PL_VC0_NP_RX_Q_CTRL_OFF	0x074C	W	0x05027009	Segmented-Buffer VC0 Non-Posted Receive Queue Control.
PL_VC0_CPL_RX_Q_CTRL_OFF	0x0750	W	0x05000000	Segmented-Buffer VC0 Completion Receive Queue Control.
PL_GEN2_CTRL_OFF	0x080C	W	0x000102FF	Link Width and Speed Change Control Register.
PL_PHY_STATUS_OFF	0x0810	W	0x00000000	PHY Status Register. Memory mapped register from phy_cfg_status GPIO input pins.
PL_PHY_CONTROL_OFF	0x0814	W	0x00000000	PHY Control Register. Memory mapped register to cfg_phy_control GPIO output pins.
PL_TRGT_MAP_CTRL_OFF	0x081C	W	0x00000047	Programmable Target Map Control Register.
PL_CLOCK_GATING_CTRL_OFF	0x088C	W	0x00000001	RADM clock gating enable control register.
PL_GEN3_RELATED_OFF	0x0890	W	0x00000000	Gen3 Control Register. This register is reserved for future use.
PL_GEN3_EQ_CONTROL_OFF	0x08A8	W	0x04059F61	Gen3 EQ Control Register.
PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF	0x08AC	W	0x00000040	Gen3 EQ Direction Change Feedback Mode Control Register.
PL_ORDER_RULE_CTRL_OFF	0x08B4	W	0x00000000	Order Rule Control Register.
PL_PIPE_LOOPBACK_CONTROL_OFF	0x08B8	W	0x00000003	PIPE Loopback Control Register.
PL_MISC_CONTROL_1_OFF	0x08BC	W	0x00000000	DBI Read-Only Write Enable Register.
PL_MULTI_LANE_CONTROL_OFF	0x08C0	W	0x00000080	UpConfigure Multi-lane Control Register.
PL_PHY_INTEROP_CTRL_OFF	0x08C4	W	0x0000003F	PHY Interoperability Control Register.

Name	Offset	Size	Reset Value	Description
PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF	0x08C8	W	0x00000000	TRGT_CPL_LUT Delete Entry Control register.
PL_LINK_FLUSH_CONTROL_OFF	0x08CC	W	0x00000000	Link Reset Request Flush Control Register.
PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF	0x08D0	W	0x00009C00	AXI Bridge Slave Error Response Register.
PL_AMBA_LINK_TIMEOUT_OFF	0x08D4	W	0x00000032	Link Down AXI Bridge Slave Timeout Register.
PL_AMBA_ORDERING_CTRL_OFF	0x08D8	W	0x00000000	AMBA Ordering Control.
PL_COHERENCY_CONTROL_1_OFF	0x08E0	W	0x00000000	ACE Cache Coherency Control Register 1
PL_COHERENCY_CONTROL_2_OFF	0x08E4	W	0x00000000	ACE Cache Coherency Control Register 2
PL_COHERENCY_CONTROL_3_OFF	0x08E8	W	0x00000000	ACE Cache Coherency Control Register 3
PL_AXI_MSTR_MSG_ADDR_LOW_OFF	0x08F0	W	0x00000000	Lower 20 bits of the programmable AXI address where Messages coming from wire are mapped to.
PL_AXI_MSTR_MSG_ADDR_HIGH_OFF	0x08F4	W	0x00000000	Register0000 Description
PL_PCIE_VERSION_NUMBER_OFF	0x08F8	W	0x3531302A	PCIe Controller IIP Release Version Number.
PL_PCIE_VERSION_TYPE_OFF	0x08FC	W	0x67612A2A	PCIe Controller IIP Release Version Type.
PL_MSIX_ADDRESS_MATCH_LOW_OFF	0x0940	W	0x00000000	MSI-X Address Match Low Register.
PL_MSIX_ADDRESS_MATCH_HIGH_OFF	0x0944	W	0x00000000	MSI-X Address Match High Register.
PL_MSIX_DOORBELL_OFF	0x0948	W	0x00000000	MSI-X Doorbell Register.
PL_MSIX_RAM_CTRL_OFF	0x094C	W	0x00000000	MSI-X RAM power mode and debug control register.
PL_LTR_LATENCY_OFF	0x0B30	W	0x00000000	LTR Latency Register.
PL_AUX_CLK_FREQ_OFF	0x0B40	W	0x00000018	Auxiliary Clock Frequency Control Register.
PL_L1_SUBSTATES_OFF	0x0B44	W	0x000000D2	L1 Substates Timing Register.
PL_PIPE_RELATED_OFF	0x0B90	W	0x00000000	PIPE Related Register.

18.4.9 Port Logic Detail Registers Description

PL_ACK_LATENCY_TIMER_OFF

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:16	RW	0x1846	REPLAY_TIME_LIMIT Replay Timer Limit. The replay timer expires when it reaches this limit. The controller initiates a replay upon reception of a NAK or when the replay timer expires. For more details, see "Transmit Replay". You can modify the effective timer limit with the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-4, 3-5, and 3-6 of the PCIe 3.0 specification. If there is a change in the payload size or link speed, the controller will override any value that you have written to this register field, and reset the field back to the specification-defined value. It will not change the value in the TIMER_MOD_REPLAY_TIMER field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.
15:0	RW	0x0817	ROUND_TRIP_LATENCY_TIME_LIMIT Ack Latency Timer Limit. The Ack latency timer expires when it reaches this limit. For more details, see "Ack Scheduling". You can modify the effective timer limit with the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register. After reset, the controller updates the default according to the Negotiated Link Width, Max_Payload_Size, and speed. The value is determined from Tables 3-7, 3-8, and 3-9 of the PCIe 3.0 specification. The limit must reflect the round trip latency from requester to completer. If there is a change in the payload size or link width, the controller will override any value that you have written to this register field, and reset the field back to the specification-defined value. It will not change the value in the TIMER_MOD_ACK_NAK field of the TIMER_CTRL_MAX_FUNC_NUM_OFF register.

PL_VENDOR_SPEC_DLLP_OFF

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	VENDOR_SPEC_DLLP Vendor Specific DLLP Register. Used to send a specific PCI Express DLLP. Your application writes the 8-bit DLLP Type and 24-bits of Payload data into this register, then sets the field VENDOR_SPECIFIC_DLLP_REQ of PORT_LINK_CTRL_OFF to send the DLLP. [7:0] = Type [31:8] = Payload (24 bits) The dllp type is in bits [7:0] while the remainder is the vendor defined payload. Note: This register field is sticky.

PL_PORT_FORCE_OFF

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	DO_DESKEW_FOR_SRIS Use the transitions from TS2 to Logical Idle Symbol, SKP OS to Logical Idle Symbol, and FTS Sequence to SKP OS to do deskew for SRIS instead of using received SKP OS if DO_DESKEW_FOR_SRIS is set to 1. Note: This register field is sticky.
22	RO	0x0	reserved
21:16	RW	0x00	LINK_STATE Forced LTSSM State. The LTSSM state that the controller is forced to when you set the FORCE_EN bit (Force Link). LTSSM state encoding is defined by the lts_state variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
15	WO	0x0	FORCE_EN Force Link. The controller supports a testing and debug capability to allow your software to force the LTSSM state machine into a specific state, and to force the controller to transmit a specific Link Command. Asserting this bit triggers the following actions: Forces the LTSSM to the state specified by the Forced LTSSM State field. Forces the controller to transmit the command specified by the Forced Link Command field. This is a self-clearing register field. Reading from this register field always returns a "0".
14:12	RO	0x0	reserved
11:8	RW	0x0	FORCED_LTSSM Forced Link Command. The link command that the controller is forced to transmit when you set FORCE_EN bit (Force Link). Link command encoding is defined by the ltssm_cmd variable in workspace/src/Layer1/smlh_ltssm.v. Note: This register field is sticky.
7:0	RW	0x04	LINK_NUM Link Number. Not used for endpoint. Note: This register field is sticky.

PL_ACK_F_ASPM_CTRL_OFF

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	ENTER_ASPM ASPM L1 Entry Control. 1: Core enters ASPM L1 after a period in which it has been idle. 0: Core enters ASPM L1 only after idle period during which both receive and transmit are in L0s. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
29:27	RW	0x3	L1_ENTRANCE_LATENCY L1 Entrance Latency. Value range is: 000: 1 us 001: 2 us 010: 4 us 011: 8 us 100: 16 us 101: 32 us 110 or 111: 64 us Note: Programming this timer with a value greater that 32us has no effect unless extended sync is used, or all of the credits are infinite. Note: This register field is sticky.
26:24	RW	0x3	L0S_ENTRANCE_LATENCY L0s Entrance Latency. Values correspond to: 000: 1 us 001: 2 us 010: 3 us 011: 4 us 100: 5 us 101: 6 us 110 or 111: 7 us Note: This register field is sticky.
23:16	RO	0xff	COMMON_CLK_N_FTS Common Clock N_FTS. This is the N_FTS when common clock is used. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. The maximum number of FTS ordered-sets that a component can request is 255. This field is only writable (sticky) when all of the following configuration parameter equations are true: CX_NFTS !=CX_COMM_NFTS DEFAULT_L0S_EXIT_LATENCY !=DEFAULT_COMM_L0S_EXIT_LATENCY DEFAULT_L1_EXIT_LATENCY !=DEFAULT_COMM_L1_EXIT_LATENCY The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. Note: The access attributes of this field are as follows: Wire: R Dbi: R
15:8	RW	0xff	ACK_N_FTS N_FTS. The number of Fast Training Sequence ordered sets to be transmitted when transitioning from L0s to L0. The maximum number of FTS ordered-sets that a component can request is 255. The controller does not support a value of zero; a value of zero can cause the LTSSM to go into the recovery state when exiting from L0s. This field is reserved (fixed to '0') for M-PCIe. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ACK_FREQ Ack Frequency. The controller accumulates the number of pending ACKs specified here (up to 255) before scheduling an ACK DLLP. 0: Indicates that this Ack Frequency Counter feature is turned off. The controller generates a low-priority ACK request for every TLP that it receives. The controller waits until the ACK Latency Timer expires, then converts the current low-priority ACK request to a high-priority ACK request and schedules the DLLP for transmission to the remote link partner. 1-255: Indicates that the controller will schedule a high-priority ACK after receiving this number of TLPs. It might schedule the ACK before receiving this number of TLPs if the ACK Latency Timer expires, but never later. For a typical system, you do not have to modify the default setting. For more details, see "ACK/NAK Scheduling". Note: This register field is sticky.

PL_PORT_LINK_CTRL_OFF

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	TRANSMIT_LANE_REVERSALE_ENABLE TRANSMIT_LANE_REVERSALE_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
26	RW	0x0	EXTENDED_SYNCH EXTENDED_SYNCH is an internally reserved field. Do not use. Note: This register field is sticky.
25	RW	0x0	CORRUPT_LCRC_ENABLE CORRUPT_LCRC_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
24	RW	0x0	BEACON_ENABLE BEACON_ENABLE is an internally reserved field. Do not use. Note: This register field is sticky.
23:22	RO	0x0	reserved
21:16	RW	0x03	LINK_CAPABLE Link Mode Enable. Sets the number of lanes in the link that you want to connect to the link partner. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Predetermined Number of Lanes" field of the "Link Width and Speed Change Control Register". For more information, see "How to Tie Off Unused Lanes". For information on upsizing and downsizing the link width, see "Link Establishment". 000001: x1 000011: x2 000111: x4 Note: This register field is sticky.
15:12	RO	0x0	reserved
11:8	RW	0x1	LINK_RATE LINK_RATE is an internally reserved field. Do not use. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
7	RW	0x0	FAST_LINK_MODE Fast Link Mode. Sets all internal LTSSM millisecond timers to Fast Mode for speeding up simulation. Forces the LTSSM training (link initialization) to use shorter time-outs and to link up faster. The default scaling factor can be changed using the DEFAULT_FAST_LINK_SCALING_FACTOR parameter or through the FAST_LINK_SCALING_FACTOR field in the TIMER_CTRL_MAX_FUNC_NUM_OFF register. Fast Link Mode can also be activated by setting the diag_ctrl_bus[2] pin to '1'. For more details, see the "Fast Link Simulation Mode" section in the "Integrating the Core with the PHY or Application RTL or Verification IP" chapter of the User Guide. For M-PCIe, this field also affects Remain Hibern8 Time, Minimum Activate Time, and RRAP timeout. If this bit is set to '1', tRRAPInitiatorResponse is set to 1.88 ms(60 ms/32). Note: This register field is sticky.
6	RW	0x0	LINK_DISABLE LINK_DISABLE is an internally reserved field. Do not use. Note: This register field is sticky.
5	RW	0x1	DLL_LINK_EN DLL Link Enable. Enables link initialization. When DLL Link Enable =0, the controller does not transmit InitFC DLLPs and does not establish a link. Note: This register field is sticky.
4	RO	0x0	reserved
3	RW	0x0	RESET_ASSERT Reset Assert. Triggers a recovery and forces the LTSSM to the hot reset state (downstream port only). Note: This register field is sticky.
2	RW	0x0	LOOPBACK_ENABLE Loopback Enable. Turns on loopback. For more details, see "Loopback". For M-PCIe, to force the master to enter Digital Loopback mode, you must set this field to "1" during Configuration.start state(initial discovery/configuration). M-PCIe doesn't support loopback mode from L0 state - only from Configuration.start. Note: This register field is sticky.
1	RW	0x0	SCRAMBLE_DISABLE Scramble Disable. Turns off data scrambling. Note: This register field is sticky.
0	RW	0x0	VENDOR_SPECIFIC_DLLP_REQ Vendor Specific DLLP Request. When software writes a '1' to this bit, the controller transmits the DLLP contained in the VENDOR_SPEC_DLLP field of VENDOR_SPEC_DLLP_OFF. Reading from this self-clearing register field always returns a '0'.

PL_LANE_SKEW_OFF

Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:27	RW	0x1	IMPLEMENT_NUM_LANES Implementation-specific Number of Lanes. Set the implementation-specific number of lanes. Allowed values are: 4'b0000: 1 lane 4'b0001: 2 lanes 4'b0011: 4 lanes 4'b0111: 8 lanes 4'b1111: 16 lanes The number of lanes to be used when in Loopback Master. The number of lanes programmed must be equal to or less than the valid number of lanes set in LINK_CAPABLE field. You must configure this field before initiating Loopback by writing in the LOOPBACK_ENABLE field. The controller will transition from Loopback.Entry to Loopback.Active after receiving two consecutive TS1 Ordered Sets with the Loopback bit asserted on the implementation specific number of lanes configured in this field. Note: This register field is sticky.
26	RW	0x0	ELASTIC_BUFFER_MODE Selects Elasticity Buffer operating mode: 0: Nominal Half Full Buffer mode 1: Nominal Empty Buffer Mode Note: This register field is sticky.
25	RW	0x0	ACK_NAK_DISABLE Ack/Nak Disable. Prevents the controller from sending ACK and NAK DLLPs. Note: This register field is sticky.
24	RW	0x0	FLOW_CTRL_DISABLE Flow Control Disable. Prevents the controller from sending FC DLLPs. Note: This register field is sticky.
23:0	RW	0x000000	INSERT_LANE_SKEW INSERT_LANE_SKEW is an internally reserved field. Do not use. Note: This register field is sticky.

PL_TIMER_CTRL_MAX_FUNC_NUM_OFF

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	FAST_LINK_SCALING_FACTOR Fast Link Timer Scaling Factor. Sets the scaling factor of LTSSM timer when FAST_LINK_MODE field in PORT_LINK_CTRL_OFF is set to '1'. 0: Scaling Factor is 1024 (1ms is 1us *a) 1: Scaling Factor is 256 (1ms is 4us) 2: Scaling Factor is 64 (1ms is 16us) 3: Scaling Factor is 16 (1ms is 64us) Note: This register field is sticky.
28:24	RW	0x00	UPDATE_FREQ_TIMER UPDATE_FREQ_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
23:19	RW	0x00	TIMER_MOD_ACK_NAK Ack Latency Timer Modifier. Increases the timer value for the Ack latency timer in increments of 64 clock cycles. A value of "0" represents no modification to the timer value. For more details, see the ROUND_TRIP_LATENCY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. Note: This register field is sticky.
18:14	RW	0x00	TIMER_MOD_REPLAY_TIMER Replay Timer Limit Modifier. Increases the time-out value for the replay timer in increments of 64 clock cycles at Gen1 or Gen2 speed, and in increments of 256 clock cycles at Gen3 speed. A value of "0" represents no modification to the timer limit. For more details, see the REPLAY_TIME_LIMIT field of the ACK_LATENCY_TIMER_OFF register. At Gen3 speed, the controller automatically changes the value of this field to DEFAULT_GEN3_REPLAY_ADJ. For M-PCIe, this field increases the time-out value for the replay timer in increments of 64 clock cycles at HS-Gear1, HS-Gear2, or HS-Gear3 speed. Note: This register field is sticky.
13:8	RO	0x00	reserved
7:0	RW	0x00	MAX_FUNC_NUM Maximum function number that can be used in a request. Configuration requests targeted at function numbers above this value are returned with UR (unsupported request). Note: This register field is sticky.

PL_SYMBOL_TIMER_FILTER_1_OFF

Address: Operational Base + offset (0x071C)

Bit	Attr	Reset Value	Description
31	RW	0x0	CX_FLT_MASK_RC_CFG_DISCARD 0: For RADM RC filter to not allow CFG transaction being received 1: For RADM RC filter to allow CFG transaction being received
30	RW	0x0	CX_FLT_MASK_RC_IO_DISCARD 0: For RADM RC filter to not allow IO transaction being received 1: For RADM RC filter to allow IO transaction being received
29	RW	0x0	CX_FLT_MASK_MSG_DROP 0: Drop MSG TLP (except for Vendor MSG). Send decoded message on the SII. 1: Do not Drop MSG (except for Vendor MSG). Send message TLPs to your application on TRGT1 and send decoded message on the SII. The default for this bit is the inverse of FLT_DROP_MSG. That is, if FLT_DROP_MSG =1, then the default of this bit is "0" (drop message TLPs). This bit only controls message TLPs other than Vendor MSGs. Vendor MSGs are controlled by Filter Mask Register 2, bits [1:0]. The controller never passes ATS Invalidate messages to the SII interface regardless of this filter rule setting. The controller passes all ATS Invalidate messages to TRGT1 (or AXI bridge master), as they are too big for the SII.

Bit	Attr	Reset Value	Description
28	RW	0x0	CX_FLT_MASK_CPL_ECRC_DISCARD Only used when completion queue is advertised with infinite credits and is in store-and-forward mode. 0: Discard completions with ECRC errors 1: Allow completions with ECRC errors to be passed up Reserved field for SW.
27	RW	0x0	CX_FLT_MASK_ECRC_DISCARD 0: Discard TLPs with ECRC errors 1: Allow TLPs with ECRC errors to be passed up
26	RW	0x0	CX_FLT_MASK_CPL_LEN_MATCH 0: Enforce length match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err 1: MASK length match for completions
25	RW	0x0	CX_FLT_MASK_CPL_ATTR_MATCH 0: Enforce attribute match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask attribute match for completions
24	RW	0x0	CX_FLT_MASK_CPL_TC_MATCH 0: Enforce Traffic Class match for completions; a violation results in a malformed TLP error, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Traffic Class match for completions
23	RW	0x0	CX_FLT_MASK_CPL_FUNC_MATCH 0: Enforce function match for completions; a violation results in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask function match for completions
22	RW	0x0	CX_FLT_MASK_CPL_REQID_MATCH 0: Enforce Req. Id match for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Req. Id match for completions
21	RW	0x0	CX_FLT_MASK_CPL_TAGERR_MATCH 0: Enforce Tag Error Rules for completions; a violation result in cpl_abort, and possibly AER of unexp_cpl_err, cpl_rcvd_ur, cpl_rcvd_ca 1: Mask Tag Error Rules for completions
20	RW	0x0	CX_FLT_MASK_LOCKED_RD_AS_UR 0: Treat locked Read TLPs as UR for EP; Supported for RC 1: Treat locked Read TLPs as Supported for EP; UR for RC
19	RW	0x0	CX_FLT_MASK_CFG_TYPE1_REQ_AS_UR 0: Treat CFG type1 TLPs as UR for EP; Supported for RC 1: Treat CFG type1 TLPs as Supported for EP; UR for RC When CX_SRIOV_ENABLE is set then this bit is set to allow the filter to process Type 1 Config requests if the EP consumes more than one bus number.
18	RW	0x0	CX_FLT_MASK_UR_OUTSIDE_BAR 0: Treat out-of-bar TLPs as UR 1: Do not treat out-of-bar TLPs as UR
17	RW	0x0	CX_FLT_MASK_UR_POIS 0: Treat poisoned request TLPs as UR 1: Do not treat poisoned request TLPs as UR The native controller always passes poisoned completions to your application except when you are using the DMA read channel.

Bit	Attr	Reset Value	Description
16	RW	0x0	CX_FLT_MASK_UR_FUNC_MISMATCH 0: Treat Function MisMatched TLPs as UR 1: Do not treat Function MisMatched TLPs as UR
15	RW	0x0	DISABLE_FC_WD_TIMER Disable FC Watchdog Timer. Note: This register field is sticky.
14:11	RW	0x0	EIDLE_TIMER EIDLE_TIMER is an internally reserved field. Do not use. Note: This register field is sticky.
10:0	RW	0x280	SKP_INT_VAL SKP Interval Value. The number of symbol times to wait between transmitting SKP ordered sets. Note that the controller actually waits the number of symbol times in this register plus 1 between transmitting SKP ordered sets. Your application must program this register accordingly. For example, if 1536 were programmed into this register (in a 250 MHz controller), then the controller actually transmits SKP ordered sets once every 1537 symbol times. The value programmed to this register is actually clock ticks and not symbol times. In a 125 MHz controller, programming the value programmed to this register should be scaled down by a factor of 2 (because one clock tick = two symbol times in this case). Note: This value is not used at Gen3 speed; the skip interval is hardcoded to 370 blocks. For M-PCIe configurations, if the 2K_PPM_DISABLED field in the M-PCIe Configuration Attribute is changed, then this field is changed automatically as follows. 2K_PPM_DISABLED=1: 1280 / CX_NB 2K_PPM_DISABLED=0: 228/CX_NB You need to set this field again if necessary when 2K_PPM_DISABLED is changed. Note: This register field is sticky.

PL_FILTER_MASK_2_OFF

Address: Operational Base + offset (0x0720)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	CX_FLT_MASK_POIS_ERROR_REPORTING 0: Disable masking of error reporting for Poisoned TLPs 1: Enable masking of error reporting for Poisoned TLPs
7	RW	0x0	CX_FLT_MASK_PRS_DROP 0: Allow PRS message to pass through 1: Drop PRS Messages silently This bit is ignored when the CX_FLT_MASK_MSG_DROP bit in the MASK_RADM_1 field of the SYMBOL_TIMER_FILTER_1_OFF register is set to '1'.
6	RW	0x0	CX_FLT_UNMASK_TD 0: Disable unmask TD bit if CX_STRIP_ECRC_ENABLE 1: Enable unmask TD bit if CX_STRIP_ECRC_ENABLE
5	RW	0x0	CX_FLT_UNMASK_UR_POIS_TRGT0 0: Disable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination 1: Enable unmask CX_FLT_MASK_UR_POIS with TRGT0 destination

Bit	Attr	Reset Value	Description
4	RW	0x0	CX_FLT_MASK_LN_VENMSG1_DROP 0: Allow LN message to pass through 1: Drop LN Messages silently
3	RW	0x0	CX_FLT_MASK_HANDLE_FLUSH 0: Disable controller Filter to handle flush request 1: Enable controller Filter to handle flush request
2	RW	0x0	CX_FLT_MASK_DABORT_4UCPL 0: Enable DLLP abort for unexpected completion 1: Do not enable DLLP abort for unexpected completion
1	RW	0x0	CX_FLT_MASK_VENMSG1_DROP 0: Vendor MSG Type 1 dropped silently 1: Vendor MSG Type 1 not dropped
0	RW	0x0	CX_FLT_MASK_VENMSG0_DROP 0: Vendor MSG Type 0 dropped with UR error reporting 1: Vendor MSG Type 0 not dropped

PL_AMBA_MUL_OB_DECOMP_NP_SUB_REQ_CTRL_OFF

Address: Operational Base + offset (0x0724)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	OB_RD_SPLIT_BURST_EN Enable AMBA Multiple Outbound Decomposed NP SubRequests. This bit when set to "0" disables the possibility of having multiple outstanding non-posted requests that were derived from decomposition of an outbound AMBA request. For more details, see "AXI Bridge Ordering" in the AXI chapter of the Databook. You should not clear this register unless your application master is requesting an amount of read data greater than Max_Read_Request_Size, and the remote device (or switch) is reordering completions that have different tags. Note: The access attributes of this field are as follows: Wire: R/W (sticky) Dbi: R/W (sticky) Note: This register field is sticky.

PL_PL_DEBUG0_OFF

Address: Operational Base + offset (0x0728)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DEB_REG_0 The value on cxpl_debug_info[31:0].

PL_PL_DEBUG1_OFF

Address: Operational Base + offset (0x072C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DEB_REG_1 The value on cxpl_debug_info[63:32].

PL_TX_P_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0730)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:12	RO	0x00	TX_P_HEADER_FC_CREDIT Transmit Posted Header FC Credits. The posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_P_DATA_FC_CREDIT Transmit Posted Data FC Credits. The posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_ph_cdts, xtlh_xadm_pd_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PL_TX_NP_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0734)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_NP_HEADER_FC_CREDIT Transmit Non-Posted Header FC Credits. The non-posted Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].
11:0	RO	0x000	TX_NP_DATA_FC_CREDIT Transmit Non-Posted Data FC Credits. The non-posted Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_nph_cdts, xtlh_xadm_npd_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PL_TX_CPL_FC_CREDIT_STATUS_OFF

Address: Operational Base + offset (0x0738)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RO	0x00	TX_CPL_HEADER_FC_CREDIT Transmit Completion Header FC Credits. The Completion Header credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

Bit	Attr	Reset Value	Description
11:0	RO	0x000	TX_CPL_DATA_FC_CREDIT Transmit Completion Data FC Credits. The Completion Data credits advertised by the receiver at the other end of the link, updated with each UpdateFC DLLP. Default value depends on the number of advertised credits for header and data [12'b0, xtlh_xadm_cplh_cdts, xtlh_xadm_cpld_cdts]; When the number of advertised completion credits (both header and data) are infinite, then the default would be [12'b0, 8'hFF, 12'hFFF].

PL_QUEUE_STATUS_OFF

Address: Operational Base + offset (0x073C)

Bit	Attr	Reset Value	Description
31	RW	0x0	TIMER_MOD_FLOW_CONTROL_EN FC Latency Timer Override Enable. When this bit is set, the value from the "FC Latency Timer Override Value" field in this register will override the FC latency timer value that the controller calculates according to the PCIe specification. Note: This register field is sticky.
30:29	RO	0x0	reserved
28:16	RW	0x0000	TIMER_MOD_FLOW_CONTROL FC Latency Timer Override Value. When you set the "FC Latency Timer Override Enable" in this register, the value in this field will override the FC latency timer value that the controller calculates according to the PCIe specification. For more details, see "Flow Control". Note: This register field is sticky.
15:14	RO	0x0	reserved
13	RO	0x0	RX_SERIALIZATION_Q_NON_EMPTY Receive Serialization Queue Not Empty. Indicates there is data in the serialization queue.
12:4	RO	0x000	reserved
3	RW	0x0	RX_QUEUE_OVERFLOW Receive Credit Queue Overflow. Indicates insufficient buffer space available to write to the P/NP/CPL credit queue.
2	RO	0x0	RX_QUEUE_NON_EMPTY Receive Credit Queue Not Empty. Indicates there is data in one or more of the receive buffers.
1	RO	0x0	TX_RETRY_BUFFER_NE Transmit Retry Buffer Not Empty. Indicates that there is data in the transmit retry buffer.
0	RO	0x0	RX_TLP_FC_CREDIT_NON_RETURN Received TLP FC Credits Not Returned. Indicates that the controller has received a TLP but has not yet sent an UpdateFC DLLP indicating that the credits for that TLP have been restored by the receiver at the other end of the link.

PL_VC_TX_ARBI_1_OFF

Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_3 WRR Weight for VC3.
23:16	RW	0x00	WRR_WEIGHT_VC_2 WRR Weight for VC2.
15:8	RW	0x00	WRR_WEIGHT_VC_1 WRR Weight for VC1.

Bit	Attr	Reset Value	Description
7:0	RW	0x0f	WRR_WEIGHT_VC_0 WRR Weight for VC0.

PL_VC_TX_ARBI_2_OFF

Address: Operational Base + offset (0x0744)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	WRR_WEIGHT_VC_7 WRR Weight for VC7.
23:16	RW	0x00	WRR_WEIGHT_VC_6 WRR Weight for VC6.
15:8	RW	0x00	WRR_WEIGHT_VC_5 WRR Weight for VC5.
7:0	RW	0x00	WRR_WEIGHT_VC_4 WRR Weight for VC4.

PL_VC0_P_RX_Q_CTRL_OFF

Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31	RW	0x0	VC_ORDERING_RX_Q VC Ordering for Receive Queues. Determines the VC ordering rule for the receive queues, used only in the segmented-buffer configuration: 1: Strict ordering, higher numbered VCs have higher priority 0: Round robin Note: This register field is sticky.
30	RW	0x1	TLP_TYPE_ORDERING_VC0 TLP Type Ordering for VC0. Determines the TLP type ordering rule for VC0 receive queues, used only in the segmented-buffer configuration: 1: PCIe ordering rules (recommended) 0: Strict ordering: posted, completion, then non-posted Note: This register field is sticky.
29:28	RO	0x0	reserved
27:26	RW	0x1	VC0_P_DATA_SCALE VC0 Scale Posted Data Credites. Note: This register field is sticky.
25:24	RW	0x1	VC0_P_HDR_SCALE VC0 Scale Posted Header Credites. Note: This register field is sticky.
23:20	RO	0x0	reserved
19:12	RO	0x27	VC0_P_HEADER_CREDIT VC0 Posted Header Credits. The number of initial posted header credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.
11:0	RO	0x048	VC0_P_DATA_CREDIT VC0 Posted Data Credits. The number of initial posted data credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.

PL_VC0_NP_RX_Q_CTRL_OFF

Address: Operational Base + offset (0x074C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:26	RW	0x1	VC0_NP_DATA_SCALE VC0 Scale Non-Posted Data Credites. Note: This register field is sticky.
25:24	RW	0x1	VC0_NP_HDR_SCALE VC0 Scale Non-Posted Header Credites. Note: This register field is sticky.
23:20	RO	0x0	reserved
19:12	RO	0x27	VC0_NP_HEADER_CREDIT VC0 Non-Posted Header Credits. The number of initial non-posted header credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.
11:0	RO	0x009	VC0_NP_DATA_CREDIT VC0 Non-Posted Data Credits. The number of initial non-posted data credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.

PL_VC0_CPL_RX_Q_CTRL_OFF

Address: Operational Base + offset (0x0750)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x1	VC0_CPL_DATA_SCALE VC0 Scale CPL Data Credites. Note: This register field is sticky.
25:24	RW	0x1	VC0_CPL_HDR_SCALE VC0 Scale CPL Header Credites. Note: This register field is sticky.
23:20	RO	0x0	reserved
19:12	RO	0x00	VC0_CPL_HEADER_CREDIT VC0 Completion Header Credits. The number of initial Completion header credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.
11:0	RO	0x000	VC0_CPL_DATA_CREDIT VC0 Completion Data Credits. The number of initial Completion data credits for VC0, used only in the segmented-buffer configuration. Note: This register field is sticky.

PL_GEN2_CTRL_OFF

Address: Operational Base + offset (0x080C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21	RW	0x0	Field0008 Electrical Idle Inference Mode at Gen1 Rate. Programmable mode to determine inferred electrical idle (EI) in Recovery.Speed or Loopback.Active (as slave) state at Gen1 speed by looking for a "1" value on RxElecIdle instead of looking for a "0" on RxValid. If the PHY fails to deassert the RxValid signal in Recovery.Speed or Loopback.Active (because of corrupted EIOS for example), then EI cannot be inferred successfully in the controller by just detecting the condition RxValid=0. 0: Use RxElecIdle signal to infer Electrical Idle 1: Use RxValid signal to infer Electrical Idle Note: This register field is sticky.
20	RW	0x0	SEL_DEEMPHASIS Used to set the de-emphasis level for upstream ports. This bit selects the level of de-emphasis the link operates at. 0: -6 dB 1: -3.5 dB Note: This register field is sticky.
19	RW	0x0	CONFIG_TX_COMP_RX Config Tx Compliance Receive Bit. When set to 1, signals LTSSM to transmit TS ordered sets with the compliance receive bit assert (equal to "1"). Note: This register field is sticky.
18	RW	0x0	CONFIG_PHY_TX_CHANGE Config PHY Tx Swing. Controls the PHY transmitter voltage swing level. The controller drives the mac_phy_txswing output from this register bit field. 0: Full Swing 1: Low Swing Note: This register field is sticky.
17	RW	0x0	DIRECT_SPEED_CHANGE Directed Speed Change. Writing "1" to this field instructs the LTSSM to initiate a speed change to Gen2 or Gen3 after the link is initialized at Gen1 speed. When the speed change occurs, the controller will clear the contents of this field; and a read to this field by your software will return a "0". To manually initiate the speed change: Write to LINK_CONTROL2_LINK_STATUS2_REG . PCIE_CAP_TARGET_LINK_SPEED in the local device Deassert this field Assert this field
16	RW	0x1	AUTO_LANE_FLIP_CTRL_EN Enable Auto flipping of the lanes. You must set the CX_AUTO_LANE_FLIP_CTRL_EN configuration parameter to include the hardware for this feature in the controller. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
15:13	RW	0x0	PRE_DET_LANE Predetermined Lane for Auto Flip. This field defines which physical lane is connected to logical Lane0 by the flip operation performed in Detect. Allowed values are: 3'b000: Connect logical Lane0 to physical lane 0 or CX_NL-1 or CX_NL/2-1 or CX_NL/4-1 or CX_NL/8-1, depending on which lane is detected 3'b001: Connect logical Lane0 to physical lane 1 3'b010: Connect logical Lane0 to physical lane 3 3'b011: Connect logical Lane0 to physical lane 7 3'b100: Connect logical Lane0 to physical lane 15 This field is used to restrict the receiver detect procedure to a particular lane when the default detect and polling procedure performed on all lanes cannot be successful. A notable example of when it is useful to program this field to a value different from the default, is when a lane is asymmetrically broken, that is, it is detected in Detect LTSSM state but it cannot exit Electrical Idle in Polling LTSSM state.
12:8	RW	0x02	NUM_OF_LANES Predetermined Number of Lanes. Defines the number of lanes which are connected and not bad. Used to limit the effective link width to ignore 'broken" or "unused" lanes that detect a receiver. Indicates the number of lanes to check for exit from Electrical Idle in Polling.Active and L2.Idle. It is possible that the LTSSM might detect a receiver on a bad or broken lane during the Detect Substate. However, it is also possible that such a lane might also fail to exit Electrical Idle and therefore prevent a valid link from being configured. This value is referred to as the "Predetermined Number of Lanes" in section 4.2.6.2.1 of the PCI Express Base 3.0 Specification, revision 1.0. Encoding is as follows: 0x01: 1 lane 0x02: 2 lanes 0x03: 3 lanes .. When you have unused lanes in your system, then you must change the value in this register to reflect the number of lanes. You must also change the value in the "Link Mode Enable" field of PORT_LINK_CTRL_OFF. The value in this register is normally the same as the encoded value in PORT_LINK_CTRL_OFF. If you find that one of your used lanes is bad then you must reduce the value in this register. For more information, see "How to Tie Off Unused Lanes." For information on upsizing and downsizing the link width, see "Link Establishment." Note: This register field is sticky.
7:0	RW	0xff	FAST_TRAINING_SEQ Sets the Number of Fast Training Sequences (N_FTS) that the controller advertises as its N_FTS during Gen2 or Gen3 link training. This value is used to inform the link partner about the PHY's ability to recover synchronization after a low power state. The number should be provided by the PHY vendor. Do not set N_FTS to zero; doing so can cause the LTSSM to go into the recovery state when exiting from L0s. This field is reserved (fixed to '0') for M-PCIe. Note: The access attributes of this field are as follows: Note: This register field is sticky.

PL_PHY_STATUS_OFF

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PHY_STATUS PHY Status. Data received directly from the phy_cfg_status bus. These is a GPIO register reflecting the values on the static phy_cfg_status input signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband status signalling requirements that you have for your PHY. Note: This register field is sticky.

PL_PHY_CONTROL_OFF

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PHY_CONTROL PHY Control. Data sent directly to the cfg_phy_control bus. These is a GPIO register driving the values on the static cfg_phy_control output signals. The usage is left completely to the user and does not in any way influence controller functionality. You can use it for any static sideband control signalling requirements that you have for your PHY.

PL_TRGT_MAP_CTRL_OFF

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	TARGET_MAP_INDEX The number of the PF Function on which the Target Values are set. This register does not respect the Byte Enable setting. any write will affect all register bits.
15:7	RO	0x000	reserved
6	RW	0x1	TARGET_MAP_ROM Target Value for the ROM page of the PF Function selected by the index number. This register does not respect the Byte Enable setting. any write will affect all register bits.
5:0	RW	0x07	TARGET_MAP_PF Target Values for each BAR on the PF Function selected by the index number. This register does not respect the Byte Enable setting. any write will affect all register bits.

PL_CLOCK_GATING_CTRL_OFF

Address: Operational Base + offset (0x088C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	RADM_CLK_GATING_EN Enable Radm clock gating feature. 0: Disable 1: Enable

PL_GEN3_RELATED_OFF

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	GEN3_EQ_INVREQ_EVAL_DIFF_DISABLE Eq InvalidRequest and RxEqEval Different Time Assertion Disable. Disable the assertion of Eq InvalidRequest and RxEqEval at different time.
22:19	RO	0x0	reserved
18	RW	0x0	GEN3_DC_BALANCE_DISABLE DC Balance Disable. Disable DC Balance feature.
17	RW	0x0	GEN3_DLLP_XMT_DELAY_DISABLE DLLP Transmission Delay Disable. Disable delay transmission of DLLPs before equalization.
16	RW	0x0	GEN3_EQUALIZATION_DISABLE Equalization Disable. Disable equalization feature. This bit cannot be changed once the LTSSM starts link training.
15:14	RO	0x0	reserved
13	RW	0x0	RXEQ_RGRDLESS_RXTS When set to '1', the controller as Gen3 EQ master asserts RxEqEval to instruct the PHY to do Rx adaptation and evaluation after a 500ns timeout from a new preset request. 0: mac_phy_rxeqeval asserts after 1us and 2 TS1 received from remote partner. 1: mac_phy_rxeqeval asserts after 500ns regardless of TS's received or not.
12	RW	0x0	RXEQ_PH01_EN Rx Equalization Phase 0/Phase 1 Hold Enable. When this bit is set the upstream port holds phase 0 (the downstream port holds phase 1) for 10ms. Holding phase 0 or phase 1 can be used to allow sufficient time for Rx Equalization to be performed by the PHY. This bit is used during Virtex-7 Gen3 equalization. The programmable bits [RXEQ_PH01_EN, EQ_PHASE_2_3] can be used to obtain the following variations of the equalization procedure: 00: Tx equalization only in phase 2/3 01: No Tx equalization, no Rx equalization 10: Tx equalization in phase 2/3, Rx equalization in phase 0/1 11: No Tx equalization, Rx equalization in phase 0/1
11	RW	0x0	EQ_REDO Equalization Redo Disable. Disable autonomous mechanism for requesting to redo the equalization process. Note: This register field is sticky.
10	RW	0x0	EQ_EIEOS_CNT Equalization EIEOS Count Reset Disable. Disable requesting reset of EIEOS count during equalization. Note: This register field is sticky.
9	RW	0x0	EQ_PHASE_2_3 Equalization Phase 2 and Phase 3 Disable. This applies to downstream ports only.
8	RW	0x0	DISABLE_SCRAMBLER_GEN_3 Disable Scrambler for Gen3 and Gen4 Data Rate.
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	GEN3_ZRXDC_NONCOMPL Gen3 Receiver Impedance ZRX-DC Not Compliant. Receivers that operate at 8.0 GT/s with an impedance other than the range defined by the ZRX-DC parameter for 2.5 GT/s (40-60 Ohms) must meet additional behavior requirements in the following LTSSM states: Polling, Rx_L0s, L1, L2, and Disabled. 0: The receiver complies with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. 1: The receiver does not comply with the ZRX-DC parameter for 2.5 GT/s when operating at 8 GT/s or higher. Note: This register field is sticky.

PL_GEN3_EQ_CONTROL_OFF

Address: Operational Base + offset (0x08A8)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x1	GEN3_REQ_SEND_CONSEC_EIEOS_FOR_PSET_MAP Request controller to send back-to-back EIEOS in Recovery.RcvrLock state until presets to coefficients mapping is complete. 0: Do not request 1: request
25	RW	0x0	GEN3_EQ_PSET_REQ_AS_COEF GEN3_EQ_PSET_REQ_AS_COEF is an internally reserved field. Do not use.
24	RW	0x0	GEN3_EQ_FOM_INC_INITIAL_EVAL Include Initial FOM. Include or not the FOM feedback from the initial preset evaluation performed in the EQ Master, when finding the highest FOM among all preset evaluations. 0: Do not include 1: Include

Bit	Attr	Reset Value	Description
23:8	RW	0x059f	GEN3_EQ_PSET_REQ_VEC Preset Request Vector. Requesting of Presets during the initial part of the EQ Master Phase. Encoding scheme is as follows: Bit [15:0] =0x0: No preset is requested and evaluated in EQ Master Phase. Bit [i] =1: "Preset=i" is requested and evaluated in EQ Master Phase. 0000000000000000: No preset be requested and evaluated in EQ Master Phase 000000xxxxxxxxx1: Preset 0 is requested and evaluated in EQ Master Phase 000000xxxxxxxx1x: Preset 1 is requested and evaluated in EQ Master Phase 000000xxxxxxx1xx: Preset 2 is requested and evaluated in EQ Master Phase 000000xxxxxx1xxx: Preset 3 is requested and evaluated in EQ Master Phase 000000xxxxx1xxxx: Preset 4 is requested and evaluated in EQ Master Phase 000000xxxx1xxxxx: Preset 5 is requested and evaluated in EQ Master Phase 000000xxx1xxxxxx: Preset 6 is requested and evaluated in EQ Master Phase 000000xx1xxxxxxx: Preset 7 is requested and evaluated in EQ Master Phase 000000x1xxxxxxxx: Preset 8 is requested and evaluated in EQ Master Phase 00000x1xxxxxxxxx: Preset 9 is requested and evaluated in EQ Master Phase 000001xxxxxxxxxx: Preset 10 is requested and evaluated in EQ Master Phase All other encodings: Reserved
7	RO	0x0	reserved
6	RW	0x1	GEN3_LOWER_RATE_EQ_REDO_ENABLE Support EQ redo and lower rate change: 0: not support 1: support
5	RW	0x1	GEN3_EQ_EVAL_2MS_DISABLE Phase2_3 2 ms Timeout Disable. Determine behavior in Phase2 for USP (Phase3 if DSP) when the PHY does not respond within 2ms to the assertion of RxEqEval: 0: abort the current evaluation, stop any attempt to modify the remote transmitter settings, Phase2 is terminated by the 24ms timeout 1: ignore the 2ms timeout and continue as normal. This is used to support PHYs that require more than 2ms to respond to the assertion of RxEqEval.

Bit	Attr	Reset Value	Description
4	RW	0x0	GEN3_EQ_PHASE23_EXIT_MODE Behavior After 24 ms Timeout (when optimal settings are not found). For a USP: Determine next LTSSM state from Phase2 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.Phase3 When optimal settings are not found then: Equalization Phase 2 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 2 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 2 Complete status bit is set in the "Link Status Register 2" For a DSP: Determine next LTSSM state from Phase3 after 24ms Timeout 0: Recovery.Speed 1: Recovery.Equalization.RcvrLock When optimal settings are not found then: Equalization Phase 3 Successful status bit is not set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 0 Equalization Phase 3 Successful status bit is set in the "Link Status Register 2" when GEN3_EQ_PHASE23_EXIT_MODE = 1 Equalization Phase 3 Complete status bit is set in the "Link Status Register 2"
3:0	RW	0x1	GEN3_EQ_FB_MODE Feedback Mode. 0000b: Direction Change 0001b: Figure Of Merit 0010b: Reserved .....: Reserved 1111b: Reserved

PL_GEN3_EQ_FB_MODE_DIR_CHANGE_OFF

Address: Operational Base + offset (0x08AC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	GEN3_EQ_FMDC_MAX_POST_CUSROR_DELTA Convergence Window Aperture for C+1. Post-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15.
13:10	RW	0x0	GEN3_EQ_FMDC_MAX_PRE_CUSROR_DELTA Convergence Window Aperture for C-1. Pre-cursor coefficients maximum delta within the convergence window depth. Allowed range: 0,1,2,..15.
9:5	RW	0x02	GEN3_EQ_FMDC_N_EVALS Convergence Window Depth. Number of consecutive evaluations considered in Phase 2/3 when determining if optimal coefficients have been found. Allowed range: 0,1,2,..16 up to a maximum of CX_GEN3_EQ_COEFQ_DEPTH. When set to 0, EQ Master is performed without sending any requests to the remote partner in Phase 2 for USP and Phase 3 for DSP. Therefore, the remote partner will not change its transmitter coefficients and will move to the next state.

Bit	Attr	Reset Value	Description
4:0	RW	0x00	GEN3_EQ_FMDC_T_MIN_PHASE23 Minimum Time (in ms) To Remain in EQ Master Phase. The LTSSM stays in EQ Master phase for at least this amount of time, before starting to check for convergence of the coefficients. Allowed values 0,1,...,24.

PL_ORDER_RULE_CTRL_OFF

Address: Operational Base + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	CPL_PASS_P Completion Passing Posted Ordering Rule Control. Determines if CPL can pass halted P queue. 0: CPL can not pass P (recommended) 1: CPL can pass P
7:0	RW	0x00	NP_PASS_P Non-Posted Passing Posted Ordering Rule Control. Determines if NP can pass halted P queue. 0 : NP can not pass P (recommended). 1 : NP can pass P

PL_PIPE_LOOPBACK_CONTROL_OFF

Address: Operational Base + offset (0x08B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	PIPE_LOOPBACK PIPE Loopback Enable. Indicates RMMI Loopback if M-PCIe. Note: This register field is sticky.
30:27	RO	0x0	reserved
26:24	RW	0x0	RXSTATUS_VALUE RXSTATUS_VALUE is an internally reserved field. Do not use.
23:22	RO	0x0	reserved
21:16	RW	0x00	RXSTATUS_LANE RXSTATUS_LANE is an internally reserved field. Do not use. Note: This register field is sticky.
15:0	RW	0x0003	LPBK_RXVALID LPBK_RXVALID is an internally reserved field. Do not use. Note: This register field is sticky.

PL_MISC_CONTROL_1_OFF

Address: Operational Base + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	ARI_DEVICE_NUMBER When ARI is enabled, this field enables use of the device ID. Note: This register field is sticky.
4	RW	0x0	DISABLE_AUTO_LTR_CLR_MSG Disable the autonomous generation of LTR clear message in upstream port. 0: Allow the autonomous generation of LTR clear message. 1: Disable the autonomous generation of LTR clear message. Default value is 0. For more details, see "Latency Tolerance Reporting (LTR) Message Generation [EP Mode]" in "Message Generation" section of the "Controller Operations" chapter of the Databook. Note: This register field is sticky.

Bit	Attr	Reset Value	Description
3	RW	0x0	SIMPLIFIED_REPLAY_TIMER Enables Simplified Replay Timer (Gen4). For more details, see "Transmit Replay" in the Controller Operations chapter of the Databook. Simplified Replay Timer Values are: A value from 24,000 to 31,000 Symbol Times when Extended Synch is 0b. A value from 80,000 to 100,000 Symbol Times when Extended Synch is 1b. Must not be changed while link is in use. Note: This register field is sticky.
2	RW	0x0	UR_CA_MASK_4_TRGT1 This field only applies to request TLPs (with UR filtering status) that you have chosen to forward to the application (when you set DEFAULT_TARGET in this register). When you set this field to '1', the core suppresses error logging, Error Message generation, and CPL generation (for non-posted requests). For more details, refer to the "Advanced Error Handling For Received TLPs" chapter of the Databook. You should set this if you have set the Default Target port logic register to '1'. Note: This register field is sticky.
1	RW	0x0	DEFAULT_TARGET Default target a received IO or MEM request with UR/CA/CRS is sent to by the controller. 0: The controller drops all incoming I/O or MEM requests (after corresponding error reporting). A completion with UR status will be generated for non-posted requests. 1: The controller forwards all incoming I/O or MEM requests with UR/CA/CRS status to your application For more details, see "ECRC Handling" and "Request TLP Routing Rules" in "Receive Routing" section of the "Controller Operations" chapter of the Databook. Default value is DEFAULT_TARGET configuration parameter. Note: This register field is sticky.
0	RW	0x0	DBI_RO_WR_EN Write to RO Registers Using DBI. When you set this field to "1", then some RO and HwInit bits are writable from the local application through the DBI. For more details, see "Writing to Read-Only Registers." Note: This register field is sticky.

PL_MULTI_LANE_CONTROL_OFF

Address: Operational Base + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	UPCONFIGURE_SUPPORT Upconfigure Support. The controller sends this value as the Link Upconfigure Capability in TS2 Ordered Sets in Configuration.Complete state.

Bit	Attr	Reset Value	Description
6	RW	0x0	DIRECT_LINK_WIDTH_CHANGE Directed Link Width Change. The controller always moves to Configuration state through Recovery state when this bit is set to '1'. If the upconfigure_capable variable is '1' and the PCIE_CAP_HW_AUTO_WIDTH_DISABLE bit in LINK_CONTROL_LINK_STATUS_REG is '0', the controller starts upconfigure or autonomous width downsizing (to the TARGET_LINK_WIDTH value) in the Configuration state. If TARGET_LINK_WIDTH value is 0x0, the controller does not start upconfigure or autonomous width downsizing in the Configuration state. The controller self-clears this field when the controller accepts this request.
5:0	RW	0x00	TARGET_LINK_WIDTH Target Link Width. Values correspond to: 6'b000000: Core does not start upconfigure or autonomous width downsizing in the Configuration state. 6'b000001: x1 6'b000010: x2 6'b000100: x4 6'b001000: x8 6'b010000: x16 6'b100000: x32

PL_PHY_INTEROP_CTRL_OFF

Address: Operational Base + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	L1_CLK_SEL L1 Clock control bit. 1: Controller does not request aux_clk switch and core_clk gating in L1. 0: Controller requests aux_clk switch and core_clk gating in L1. Note: This register field is sticky.
9	RW	0x0	L1_NOWAIT_P1 L1 entry control bit. 1: Core does not wait for PHY to acknowledge transition to P1 before entering L1. 0: Core waits for the PHY to acknowledge transition to P1 before entering L1. Note: This register field is sticky.
8	RW	0x0	L1SUB_EXIT_MODE L1 Exit Control Using phy_mac_pclkack_n. 1: Core exits L1 without waiting for the PHY to assert phy_mac_pclkack_n. 0: Core waits for the PHY to assert phy_mac_pclkack_n before exiting L1. Note: This register field is sticky.
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x3f	RXSTANDBY_CONTROL Rxstandby Control. Bits 0..5 determine if the controller asserts the RxStandby signal (mac_phy_rxstandby) in the indicated condition. Bit 6 enables the controller to perform the RxStandby/RxStandbyStatus handshake. [0]: Rx EIOS and subsequent T TX-IDLE-MIN [1]: Rate Change [2]: Inactive lane for upconfigure/downconfigure [3]: PowerDown=P1orP2 [4]: RxL0s.Idle [5]: EI Infer in L0 [6]: Execute RxStandby/RxStandbyStatus Handshake Note: This register field is sticky.

PL_TRGT_CPL_LUT_DELETE_ENTRY_OFF

Address: Operational Base + offset (0x08C8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	LOOK_UP_ID This number selects one entry to delete of the TRGT_CPL_LUT.

PL_LINK_FLUSH_CONTROL_OFF

Address: Operational Base + offset (0x08CC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	AUTO_FLUSH_EN Enables automatic flushing of pending requests before sending the reset request to the application logic to reset the PCIe controller and the AXI Bridge. The flushing process is initiated if any of the following events occur: Hot reset request. A downstream port (DSP) can "hot reset" an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Warm (Soft) reset request. Generated when exiting from D3 to D0 and cfg_pm_no_soft_rst=0. Link down reset request. A high to low transition on smlh_req_rst_not indicates the link has gone down and the controller is requesting a reset. If you disable automatic flushing, your application is responsible for resetting the PCIe controller and the AXI Bridge. Note: This register field is sticky.

PL_AMBA_ERROR_RESPONSE_DEFAULT_OFF

Address: Operational Base + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RW	0x27	AMBA_ERROR_RESPONSE_MAP AXI Slave Response Error Map. Allows you to selectively map the errors received from the PCIe completion (for non-posted requests) to the AXI slave responses, slv_rresp or slv_bresp. The recommended setting is SLVERR. CRS is always mapped to OKAY. bit 0: 0: UR (unsupported request) -> DECERR 1: UR (unsupported request) -> SLVERR bit 1: 0: CRS (configuration retry status) -> DECERR 1: CRS (configuration retry status) -> SLVERR bit 2 0: CA (completer abort) -> DECERR 1: CA (completer abort) -> SLVERR bit 3: Reserved bit 4: Reserved bit 5: 0: Completion Timeout -> DECERR 1: Completion Timeout -> SLVERR
9:5	RO	0x00	reserved
4:3	RW	0x0	AMBA_ERROR_RESPONSE_CRS CRS Slave Error Response Mapping. Determines the AXI slave response for CRS completions. 00: OKAY 01: OKAY with all FFFF_FFFF data for all CRS completions 10: OKAY with FFFF_0001 data for CRS completions to vendor ID read requests, OKAY with FFFF_FFFF data for all other CRS completions 11: SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Note: This register field is sticky.
2	RW	0x0	AMBA_ERROR_RESPONSE_VENDORID Vendor ID Non-existent Slave Error Response Mapping. Determines the AXI slave response for errors on reads to non-existent Vendor ID register. 0: OKAY (with FFFF data). 1: SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) Note: This register field is sticky.
1	RO	0x0	reserved
0	RW	0x0	AMBA_ERROR_RESPONSE_GLOBAL Global Slave Error Response Mapping. Determines the AXI slave response for all error scenarios on non-posted requests. 0: OKAY (with FFFF data for non-posted requests) 1: SLVERR/DECERR (the AXI_ERROR_RESPONSE_MAP field determines the PCIe-to-AXI Slave error response mapping) The error response mapping is not applicable to Non-existent Vendor ID register reads. Note: This register field is sticky.

PL_AMBA_LINK_TIMEOUT_OFF

Address: Operational Base + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	LINK_TIMEOUT_ENABLE_DEFAULT Disable Flush. You can disable the flush feature by setting this field to "1". Note: This register field is sticky.
7:0	RW	0x32	LINK_TIMEOUT_PERIOD_DEFAULT Timeout Value (ms). The timer will timeout and then flush the bridge TX request queues after this amount of time. The timer counts when there are pending outbound AXI slave interface requests and the PCIe TX link is not transmitting any of these requests. The timer is clocked by core_clk. For an M-PCIe configuration: Time unit of this field is 4 ms. Margin of error for RateA clock is < 1%. Margin of error for RateB clock is between 16% and 17%. Note: This register field is sticky.

PL_AMBA_ORDERING_CTRL_OFF

Address: Operational Base + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	AX_MSTR_ZEROLREAD_FW AXI Master Zero Length Read Forward to the application. The DW PCIe controller AXI bridge is able to terminate in order with the Posted transactions the zero length read, implementing the PCIe express flush semantics of the Posted transactions. 0x0: The zero length Read is terminated at the DW PCIe AXI bridge master 0x1: The zero length Read is forward to the application.
6:5	RO	0x0	reserved
4:3	RW	0x0	AX_MSTR_ORDR_P_EVENT_SEL AXI Master Posted Ordering Event Selector. This field selects how the master interface determines when a P write is completed when enforcing the PCIe ordering rule, "NP must not pass P" at the AXI Master Interface. The AXI protocol does not support ordering between channels. Therefore, NP reads can pass P on your AXI bus fabric. This can result in an ordering violation when the read overtakes a P that is going to the same address. Therefore, the bridge master does not issue any NP requests until all outstanding P writes reach their destination. It does this by waiting for the all of the write responses on the B channel. This can affect the performance of the master read channel. For scenarios where the interconnect serializes the AXI master "AW", "W" and "AR" channels,you can increase the performance by reducing the need to wait until the complete Posted transaction has effectively reached the application slave. 00: B'last event: wait for the all of the write responses on the B channel thereby ensuring that the complete Posted transaction has effectively reached the application slave (default). 01: AW'last event: wait until the complete Posted transaction has left the AXI address channel at the bridge master. 10: W'last event: wait until the complete Posted transaction has left the AXI data channel at the bridge master. 11: Reserved
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	AX_SNP_EN AXI Serialize Non-Posted Requests Enable. This field enables the AXI Bridge to serialize same ID Non-Posted Read/Write Requests on the wire. Serialization implies one outstanding same ID NP Read or Write on the wire and used to avoid AXI RAR and WAW hazards at the remote link partner.
0	RO	0x0	reserved

PL_COHERENCY_CONTROL_1_OFF

Address: Operational Base + offset (0x08E0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_LOW_ADDR Boundary Lower Address For Memory Type. Bits [31:0] of dword-aligned address of the boundary for Memory type. The two lower address LSBs are "00". Addresses up to but not including this value are in the lower address space region; addresses equal or greater than this value are in the upper address space region. Note: This register field is sticky.
1	RO	0x0	reserved
0	RW	0x0	CFG_MEMTYPE_VALUE Sets the memory type for the lower and upper parts of the address space: 0: lower = Peripheral; upper = Memory 1: lower = Memory type; upper = Peripheral Note: This register field is sticky.

PL_COHERENCY_CONTROL_2_OFF

Address: Operational Base + offset (0x08E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_MEMTYPE_BOUNDARY_HIGH_ADDR Boundary Upper Address For Memory Type. Bits [63:32] of the 64-bit dword-aligned address of the boundary for Memory type. Note: This register field is sticky.

PL_COHERENCY_CONTROL_3_OFF

Address: Operational Base + offset (0x08E8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RW	0x0	CFG_MSTR_AWCACHE_VALUE Master Write CACHE Signal Value. Value of the individual bits in mstr_awcache when CFG_MSTR_AWCACHE_MODE is '1'. Note: not applicable to message requests; for message requests the value of mstr_awcache is always "0000" Note: This register field is sticky.
26:23	RO	0x0	reserved
22:19	RW	0x0	CFG_MSTR_ARCACHE_VALUE Master Read CACHE Signal Value. Value of the individual bits in mstr_arcache when CFG_MSTR_ARCACHE_MODE is '1'. Note: This register field is sticky.
18:15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:11	RW	0x0	CFG_MSTR_AWCACHE_MODE Master Write CACHE Signal Behavior. Defines how the individual bits in mstr_awcache are controlled: 0: set automatically by the AXI master 1: set by the value of the corresponding bit of the CFG_MSTR_AWCACHE_VALUE field Note: for message requests the value of mstr_awcache is always "0000" regardless of the value of this bit Note: This register field is sticky.
10:7	RO	0x0	reserved
6:3	RW	0x0	CFG_MSTR_ARCACHE_MODE Master Read CACHE Signal Behavior. Defines how the individual bits in mstr_arcache are controlled: 0: set automatically by the AXI master 1: set by the value of the corresponding bit of the CFG_MSTR_ARCACHE_VALUE field Note: This register field is sticky.
2:0	RO	0x0	reserved

PL_AXI_MSTR_MSG_ADDR_LOW_OFF

Address: Operational Base + offset (0x08F0)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	CFG_AXIMSTR_MSG_ADDR_LOW Lower 20 bits of the programmable AXI address for Messages. Note: This register field is sticky.
11:0	RO	0x000	CFG_AXIMSTR_MSG_ADDR_LOW_RESERVED Reserved for future use. Note: This register field is sticky.

PL_AXI_MSTR_MSG_ADDR_HIGH_OFF

Address: Operational Base + offset (0x08F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	CFG_AXIMSTR_MSG_ADDR_HIGH Upper 32 bits of the programmable AXI address for Messages. Note: This register field is sticky.

PL_PCIE_VERSION_NUMBER_OFF

Address: Operational Base + offset (0x08F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3531302a	VERSION_NUMBER Version Number.

PL_PCIE_VERSION_TYPE_OFF

Address: Operational Base + offset (0x08FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x67612a2a	VERSION_TYPE Version Type.

PL_MSIX_ADDRESS_MATCH_LOW_OFF

Address: Operational Base + offset (0x0940)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	MSIX_ADDRESS_MATCH_LOW MSI-X Address Match Low Address. Note: This register field is sticky.
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	MSIX_ADDRESS_MATCH_EN MSI-X Match Enable. Enable the MSI-X Address Match feature when the AXI bridge is present. Note: This register field is sticky.

PL_MSIX_ADDRESS_MATCH_HIGH_OFF

Address: Operational Base + offset (0x0944)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSIX_ADDRESS_MATCH_HIGH MSI-X Address Match High Address. Note: This register field is sticky.

PL_MSIX_DOORBELL_OFF

Address: Operational Base + offset (0x0948)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	WO	0x00	MSIX_DOORBELL_PF MSIX Doorbell Physical Function. This register determines the Physical Function for the MSI-X transaction.
23:16	WO	0x00	MSIX_DOORBELL_VF MSIX Doorbell Virtual Function. This register determines the Virtual Function for the MSI-X transaction.
15	WO	0x0	MSIX_DOORBELL_VF_ACTIVE MSIX Doorbell Virtual Function Active. This register determines whether a Virtual Function is used to generate the MSI-X transaction.
14:12	WO	0x0	MSIX_DOORBELL_TC MSIX Doorbell Traffic Class. This register determines which traffic class to generate the MSI-X transaction with.
11	RO	0x0	reserved
10:0	WO	0x000	MSIX_DOORBELL_VECTOR MSI-X Doorbell Vector. This register determines which vector to generate the MSI-X transaction for.

PL_MSIX_RAM_CTRL_OFF

Address: Operational Base + offset (0x094C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	MSIX_RAM_CTRL_DBG_PBA MSIX PBA RAM Debug Mode. Use this bit to activate the debug mode and allow direct read/write access to the PBA. Use can also use the dbg_pba input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky.
24	RW	0x0	MSIX_RAM_CTRL_DBG_TABLE MSIX Table RAM Debug Mode. Use this bit to activate the debug mode and allow direct read/write access to the Table. Use can also use the dbg_table input to activate debug mode. Debug mode turns off the PF/VF/Offset-based addressing into the RAM and maps the entire table linearly from the base address of the BAR (indicated by the BIR) in function 0. Note: This register field is sticky.
23:17	RO	0x00	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	MSIX_RAM_CTRL_BYPASS MSIX RAM Control Bypass. The bypass field, when set, disables the internal generation of low power signals for both RAMs. It is up to the application to ensure the RAMs are in the proper power state before trying to access them. Moreover, the application needs to observe all timing requirements of the RAM low power signals before trying to use the MSIX functionality. Note: This register field is sticky.
15:10	RO	0x00	reserved
9	RW	0x0	MSIX_RAM_CTRL_PBA_SD MSIX PBA RAM Shut Down. Set this bit to drive the cfg_msix_pba_sd output to signal your external logic to place the MSIX PBA RAM in Shut Down low-power mode. Note: This register field is sticky.
8	RW	0x0	MSIX_RAM_CTRL_PBA_DS MSIX PBA RAM Deep Sleep. Set this bit to drive the cfg_msix_pba_ds output to signal your external logic to place the MSIX PBA RAM in Deep Sleep low-power mode. Note: This register field is sticky.
7:2	RO	0x00	reserved
1	RW	0x0	MSIX_RAM_CTRL_TABLE_SD MSIX Table RAM Shut Down. Set this bit to drive the cfg_msix_table_sd output to signal your external logic to place the MSIX Table RAM in Shut Down low-power mode. Note: This register field is sticky.
0	RW	0x0	MSIX_RAM_CTRL_TABLE_DS MSIX Table RAM Deep Sleep. Set this bit to drive the cfg_msix_table_ds output to signal your external logic to place the MSIX Table RAM in Deep Sleep low-power mode. Note: This register field is sticky.

PL_LTR_LATENCY_OFF

Address: Operational Base + offset (0x0B30)

Bit	Attr	Reset Value	Description
31	RW	0x0	NO_SNOOP_LATENCY_REQUIRE No Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W
30:29	RO	0x0	reserved
28:26	RW	0x0	NO_SNOOP_LATENCY_SCALE No Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W
25:16	RW	0x000	NO_SNOOP_LATENCY_VALUE No Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W
15	RW	0x0	SNOOP_LATENCY_REQUIRE Snoop Latency Requirement. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W

Bit	Attr	Reset Value	Description
14:13	RO	0x0	reserved
12:10	RW	0x0	SNOOP_LATENCY_SCALE Snoop Latency Scale. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W
9:0	RW	0x000	SNOOP_LATENCY_VALUE Snoop Latency Value. Note: The access attributes of this field are as follows: Wire: R Dbi: R/W

PL_AUX_CLK_FREQ_OFF

Address: Operational Base + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x018	AUX_CLK_FREQ The aux_clk frequency in MHz. This value is used to provide a 1 us reference for counting time during low-power states with aux_clk when the PHY has removed the pipe_clk. Frequencies lower than 1 MHz are possible but with a loss of accuracy in the time counted. If the actual frequency (f) of aux_clk does not exactly match the programmed frequency (f_prog), then there is an error in the time counted by the controller that can be expressed in percentage as: err% = (f_prog/f-1)*100. For example if f=2.5 MHz and f_prog=3 MHz, then err% =(3/2.5-1)*100 =20%, meaning that the time counted by the controller on aux_clk will be 20% greater than the time in us programmed in the corresponding time register (for example T_POWER_ON). Note: This register field is sticky.

PL_L1_SUBSTATES_OFF

Address: Operational Base + offset (0x0B44)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x3	L1SUB_T_PCLKACK Max delay (in 1us units) between a MAC request to remove the clock on mac_phy_pclkreq_n and a PHY response on phy_mac_pclkack_n. If the PHY does not respond within this time the request is aborted. Range is 0..3 Note: This register field is sticky.
5:2	RW	0x4	L1SUB_T_L1_2 Duration (in 1us units) of L1.2. Range is 0.15. Note: The timeout value can vary by 50%. Note: This register field is sticky.
1:0	RW	0x2	L1SUB_T_POWER_OFF Duration (in 1us units) of L1.2.Entry. Range is 0.3. Note: The timeout value can vary by 50%. Note: This register field is sticky.

PL_PIPE_RELATED_OFF

Address: Operational Base + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	PIPE_GARBAGE_DATA_MODE PIPE Garbage Data Mode. 0: PIPE Spec compliant mode: The MAC discards any symbols received after the electrical idle ordered-set until RxValid is deasserted. 1: Special PHY Support mode: The MAC discards any symbols received after the electrical idle ordered-set until when any of the following three conditions are true: RxValid is deasserted a valid RxStartBlock is received at 128b/130b encoding a valid COM symbol is received at 8b/10b encoding Note: This register field is sticky.
7:0	RO	0x00	reserved

18.5 Interface Description

Table 18-6 PCIe 2-lane DM G3 Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
pcie_button_rst_n	I	CLK32K_IN/CLK32K_OUT0/PCIE30X2_BUTTONRSTn/GPIO0_B0_u	PMU_GRF_GPIO0B_IOMUX_L[3:0]=4'h3
pcie_perst_n	I	PWM7_IR/SPI0_CS0_M0/PCIE30X2_PERSTn_M0/GPIO0_C6_d	PMU_GRF_GPIO0A_IOMUX_H[11:8]=4'h3
		LCDC_D6/VOP_BT656_D6_M0/SPI2_MOSI_M1/PCIE30X2_PERSTn_M1/I2S1_SDI3_M2/GPIO2_D6_d	GRF_GPIO2D_IOMUX_H[11:8] =4'h4
		EDP_DP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	GRF_GPIO4C_IOMUX_H[3:0] =4'h4
pcie_wake_in/out	I/O	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	PMU_GRF_GPIO0C_IOMUX_H[7:4] =4'h3
		LCDC_D5/VOP_BT656_D5_M0/SPI2_CS0_M1/PCIE30X2_WAKEn_M1/I2S1_SDI2_M2/GPIO2_D5_d	GRF_GPIO2D_IOMUX_H[7:4] =4'h4
		PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	GRF_GPIO4C_IOMUX_L[15:12] =4'h4
pcie_clkreq_in/out_n	I/O	GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	PMU_GRF_GPIO0A_IOMUX_H[11:8] =4'h3
		LCDC_D4/VOP_BT656_D4_M0/SPI2_CS1_M1/PCIE30X2_CLKREQn_M1/I2S1_SDI1_M2/GPIO2_D4_d	GRF_GPIO2D_IOMUX_H[3:0] =4'h4
		PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	GRF_GPIO4C_IOMUX_L[11:8] =4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

The M0/M1/M2 Group is controlled by GRF_IOFUNC_SEL5[7:6].

Table 18-7 PCIe 1-lane RC G3 Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
pcie_button_rst_n	I	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B3_u	PMU_GRF_GPIO0B_IOMUX_L[15:12]=4'h3
pcie_perst_n	I	PWM4/VOP_PWM_M0/PCIE30X1_PERSTn_M0/MCU_JTAG_TRSTn/GPIO0_C3_d	PMU_GRF_GPIO0C_IOMUX_L[15:12] =4'h3
		LCDC_D8/VOP_BT1120_D0/SPI1_CS0_M1/PCIE30X1_	GRF_GPIO3A_IOMUX_L[7:4] =4'h4

Module Pin	Dir.	Pin Name	IOMUX Setting
		PERSTn_M1/SDMMC2_D0_M1/GPIO3_A1_d	
		I2S1_MCLK_M0/UART3_RTSn_M0/SCR_CLK/PCIE30X1_PERSTn_M2/GPIO1_A2_d	GRF_GPIO1A_IOMUX_L[11:8] =4'h4
pcie_wake_in/out	I/O	PWM3_IR/EDP_DP_HPDIN_M1/PCIE30X1_WAKEn_M0/MCU_JTAG_TMS/GPIO0_C2_d	PMU_GRF_GPIO0C_IOMUX_L[11:8] =4'h3
		LCDC_D3/VOP_BT656_D3_M0/SPI0_CLK_M1/PCIE30X1_WAKEn_M1/I2S1_SDI0_M2/GPIO2_D3_d	GRF_GPIO2D_IOMUX_L[15:12] =4'h4
		I2S1_SCLK_TX_M0/UART3_CTSn_M0/SCR_IO/PCIE30X1_WAKEn_M2/ACODEC_DAC_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_L[15:12] =4'h4
pcie_clkreq_in/out_n	I/O	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	PMU_GRF_GPIO0A_IOMUX_H[3:0] =4'h3
		LCDC_D2/VOP_BT656_D2_M0/SPI0_CS0_M1/PCIE30X1_CLKREQn_M1/I2S1_LRCK_TX_M2/GPIO2_D2_d	GRF_GPIO2D_IOMUX_L[11:8] =4'h4
		I2S1_LRCK_TX_M0/UART4_RTSn_M0/SCR_RST/PCIE30X1_CLKREQn_M2/ACODEC_DAC_SYNC/GPIO1_A5_d	GRF_GPIO1A_IOMUX_H[7:4] =4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

The M0/M1/M2 Group is controlled by GRF_IOFUNC_SEL5[5:4].

Table 18-8 PCIe 1-lane RC G2 Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
pcie_button_rst_n	I	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	PMU_GRF_GPIO0B_IOMUX_H[3:0]=4'h3
pcie_perst_n	I	I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	PMU_GRF_GPIO0B_IOMUX_H[11:8] =4'h3
		LCDC_HSYNC/VOP_BT1120_D13/SPI1_MOSI_M1/PCIE20_PERSTn_M1/I2S1_SDO2_M2/GPIO3_C1_d	GRF_GPIO3C_IOMUX_L[7:4] =4'h4
		I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTn_M2/GPIO1_B2_d	GRF_GPIO1B_IOMUX_L[11:8] =4'h4
pcie_wake_in/out	I/O	I2C2_SCL_M0/SPI0_CLK_M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	PMU_GRF_GPIO0B_IOMUX_H[7:4] =4'h3
		LCDC_D1/VOP_BT656_D1_M0/SPI0_MOSI_M1/PCIE20_WAKEn_M1/I2S1_SCLK_TX_M2/GPIO2_D1_d	GRF_GPIO2D_IOMUX_L[7:4] =4'h4
		I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEn_M2/ACODEC_ADC_SYNC/GPIO1_B1_d	GRF_GPIO1B_IOMUX_L[7:4] =4'h4
pcie_clkreq_in/out_n	I/O	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	PMU_GRF_GPIO0A_IOMUX_H[7:4] =4'h3
		LCDC_D0/VOP_BT656_D0_M0/SPI0_MISO_M1/PCIE20_CLKREQn_M1/I2S1_MCLK_M2/GPIO2_D0_d	GRF_GPIO2D_IOMUX_L[3:0] =4'h4
		I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0/PCIE20_CLKREQn_M2/ACODEC_DAC_DATAR/GPIO1_B0_d	GRF_GPIO1B_IOMUX_L[3:0] =4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional

The M0/M1/M2 Group is controlled by GRF_IOFUNC_SEL5[3:2].

18.6 Application Notes

18.6.1 Clock and Reset

18.6.1.1 Clock Overview

The PCIe module uses multiple clock domains, it consists of system bus clocks (APB and AXI), Core function clock, PIPE interface clock, Power management clock, and PCIe PHY reference clock.

The system bus clock is generated from SOC main PLL internally, please refer to the relative chapter for details. System bus clock gating is handled automatically by PCIe controller, and the clock gating can be disable by software through PCIE_CLIENT_LOCAL_CRU_CTRL Register.

Core function clock is derived from the PIPE interface clock output from the PCIe PHY. In specific low power state, core function clock is gated and switch to Power management clock automatically.

The PHY TX PLL generates PIPE interface clock from the platform reference clock. The PCIe link Training and transaction is completely dependent upon availability of this clock. Application should not initiate transactions before ensuring that the PHY PLL is locked.

The Power management clock which should be fixed with 24MHz driven by crystal input clock. The PCIe controller uses this clock for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value of 24MHz to count real time.

Many PCIe connections, especially backplane connections, require a synchronous reference clock between the two link partners. To achieve this a common clock source, referred to as REFCLK in the PCI Express Card Electromechanical Specification, should be used by both ends of the PCIe link. the PCIe PHY provides 100MHz differential clock output (optional with SSC) in RC mode for system application. If Spread Spectrum Clocking (SSC) is used it is required that a common reference clock be used by the link partners. Most commercially available platforms with PCIe backplanes use Spread Spectrum Clocking to reduce EMI. If common clock architecture is used, the user driver should configure the PHY internal configuration bits to enable the feature of 100MHz differential clock output.

18.6.1.2 PCIe PHY Reference Clock

In RC mode, PCIe PHY can use internal single-ended clock which can be configured to 24Mhz, 25Mhz, 50Mhz or 100Mhz. Meanwhile, PCIe PHY can provide differential clock output for system application. The source of differential clock output can be select from internal single-ended clock or PHY TX PLL.

In EP mode, PCIe PHY can use internal single-ended clock or external differential clock input as its reference clock. The Reference clock structure and related configuration is shown below.

For more detail information, please refer to section PCIe2/USB3 PHY Detail Register Description for PHY register description.

18.6.1.3 Reset Overview

18.6.1.3.1 Power-On Reset

The power-on reset is used as cold reset of the PCIe. The entire module is reset when power-on reset is asserted. After de-assertion of the power-on reset, the PCIe PHY and PCIe Core function reset keep until the software release them. Application should finish PCIe PHY configuration and wait for TX PLL lock before release reset.

18.6.1.3.2 System reset

The PCIe Controller has the following distinct resets, all of these are configurable through software driver. This section describes the function of each of the reset inputs.

- button_rst_n: Button reset from board if related IO has been used. Please refer to Interface Description section for more information. This reset has an equal functionality with power-on reset.
- perst_n: This reset works as Warm Reset of PCIe if related IO has been used. Please refer to Interface Description section for more information.
- core_rst: This is the main reset for the PCIe Controller. It resets all the logic in the core

running in the CORE_CLK domain, except for the PMC module. It keeps reset with power-up reset by default. It also should be asserted when Hot Reset or link down reset occurs, but Application software can delay core_rst_n been asserted until system is ready to do core reset. This delayed reset operation will be discussed in next section.

- AXI Reset: All three AXI interface has its own reset input: mstr_aresetn, slv_aresetn, dbi_resetn. Each resets all logic in the specific AXI_CLK domain. Typically, these resets are be asserted whenever core_reset is asserted. Application software shall have the knowledge of choosing an appropriate time to drive this reset in order to avoid times when a transaction is in flight.
- non_sticky_rst_n: Resets all non-sticky bit registers in the configuration register space.
- sticky_rst_n : Resets all sticky bit registers in the configuration register space.
- pwr_rst_n: Resets the PMC module and resets all registers in the PM clock domain, including sticky bits.
- phy_rst_n: output reset signal to reset the PCIe PHY. This reset asserted along with Power-On Reset and Hot Reset.

PMC of PCIe Controller may request some system reset such as core_rst_n, sticky_rst_n, non_sticky_rst_n and pwr_rst_n. Application can use PCIE_CLIENT_LOCAL_CRU_CTRL register in client register group to disable these requests. Refer to PCIe Client Detail Register Description for more details.

18.6.1.3.3 Hot Reset and Link-Down Reset

A downstream port (DSP) can hot reset an upstream port (USP) by sending two consecutive TS1 ordered sets with the hot reset bit asserted. Eventually, the DSP and USP assert link_req_rst_not to request external logic to reset them. Alternatively, during normal operation, the link might fail and go down. After this link-down event, the controller requests the reset module to hot-reset the controller. There is no difference in the handling of a link-down reset or a hot reset; the controller core asserts the link_req_rst_not output requesting the reset module to reset the controller.

Hot Reset or Link-down reset cannot be activated before no transaction is appending on system bus. Application software must confirm that system bus is in IDLE state then let the reset operation go on.

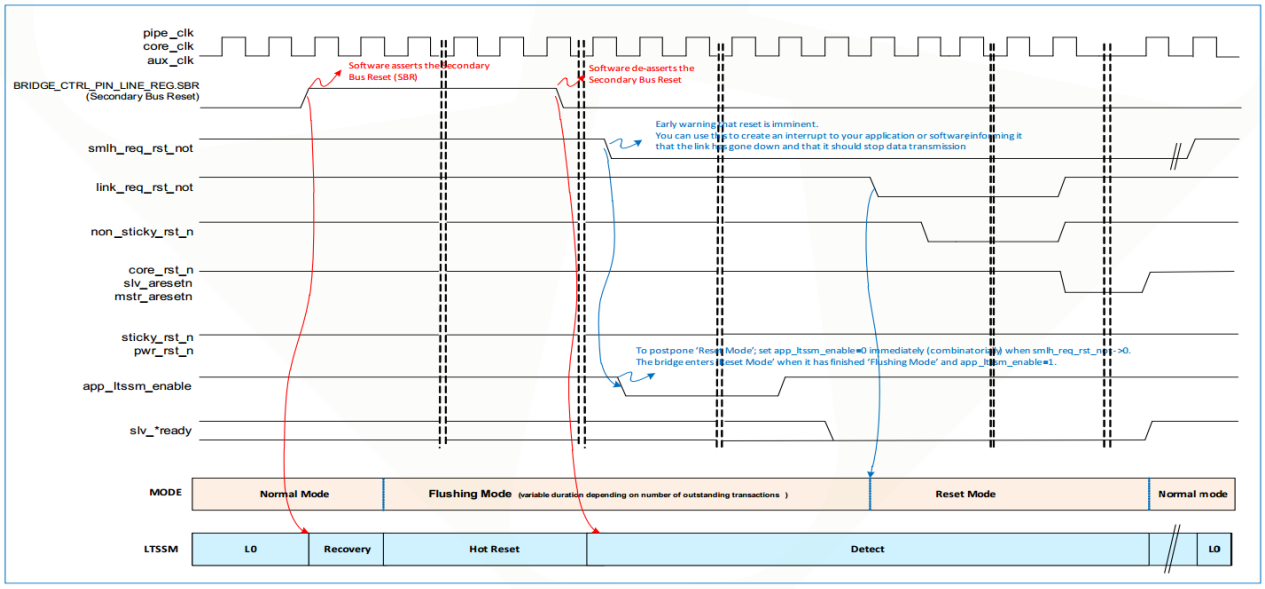


Fig. 18-4 Delaying the PCIe Hot Reset

Figure above illustrate the timing of handling Hot Reset. When Hot Reset or Link-down reset occurs, controller will assert smlh_req_rst_not as an early warning. This warning is an interrupt bit in Client Register group. app_ltssm_enable should be deasserted immediately to disable the LTSSM. Then the Hot Reset process is holding on. Software then should set the PCIe NIU in IDLE state by using PCIE GRF registers. After that, software can assert app_ltssm_enable to let the controller to finish the reset.

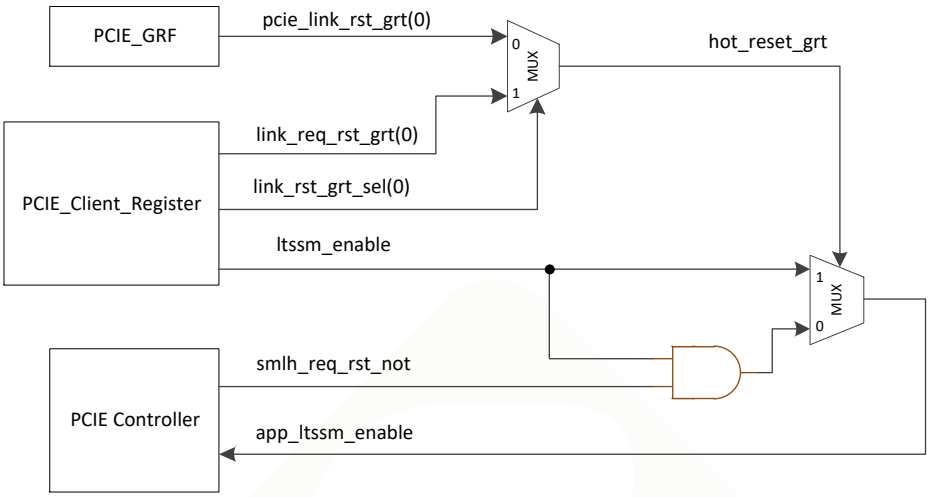


Fig. 18-5 PCIe Hot Reset Control Structure

Figure above illustrate the Hot Reset control structure, when application deassert link_rst_grt, the app_ltssm_enable will be gated if smlh_req_rst_not is asserted. Configure hot_reset_grt by PCIE_GRF register is recommend and the client register control path is reserved for future use.

The link down or hot reset flow is as follows:

1. When link is up, set pcie_link_rst_grt (bit 2 in PCIe_USB_GRF_PCIe_CON0 register) to 0. Then smlh_req_rst_not will gate ltssm_enable and delay the reset when link down.
2. When link down or hot reset occurs, interrupt bit in PCIE_CLIENT_INTR_STATUS_MISC will be set.
3. Set ltssm_enable to 0.
4. Set bit 1 in PCIe_USB_GRF_PCIe_CON0 register to 1 to IDLE PCIe NIU.
5. Wait bit 1 in PCIe_USB_GRF_PCIe_STATUS0 set to 1 which indicates PCIe NIU idle status.
6. Software stop all transactions or other operations to prepare for reset.
7. Let reset operation start and retrain the link: set pcie_link_rst_grt (bit 2 in PCIe_USB_GRF_PCIe_CON0 register) to 1 and set ltssm_enable to 1.
8. Wait for link up and then set pcie_link_rst_grt to 0 to prepare for the next link down reset.

18.6.2 Initialization

18.6.2.1 Initialization Sequence for RC Mode

The initialization sequence for RC mode is as follows:

1. Configure the IO for CLKREQ# and WAKE# signals. Configure the optional signals button_rst_n and perst_n if they are used. Please refer to section Interface Description for details.
2. Configure the CRU registers to provide reference clock to PCIe PHY. Please refer to CRU Chapter for more information.
3. Configure USB3PHY General Register File to set PIPE signals which are unused for PCIe to appropriate values.
4. Configure PHY registers to set PCIe PHY work in PCIe RC Mode. Configure Client Registers to set the PCIe Controller device_type to RC mode.
5. Configure PHY registers to set TX PLL parameters to appropriate values. For programming details, please refer to Programming setting for PCIe PHY TX PLL.
6. Wait for PCIe PHY TX PLL lock, then release software reset for PCIe Controller.
7. Assert pcie_link_rst_grt in PCIE_GRF (refer to section Hot Reset and Link-Down Reset) to free ltssm_enable to prepare for link training. This step must be down because smlh_req_rst_not is asserted after power-on reset until first link up.
8. You can program controller registers before Link training start if necessary. Link training can be initialed by setting ltssm_enable bit in register PCIE_CLIENT_GENERAL_CON to 1. Link training success will set phy_link_up_int interrupt status bit in register PCIE_CLIENT_INTR_STATUS_MISC to 1. And if data flow initialization success, dll_link_up_int interrupt status bit will be set to one in same register. To Initially, the controller tries to linkup at maximum Link width, when you have unused

lanes in your system, you must tie them off using the hardware and software procedures outlined in section Tie off Unused Lanes.
Link speed will change to Gen2 automatically if you set direct_speed_change bit to 1 in PL_GEN2_CTRL_OFF register and both device support Gen2 speed.

9. RC finish the device Enumeration. For example: read the configuration space of the downstream devices, program device capabilities, program the BARs of endpoints.
10. Writes to Bus Master Enable (BME), Memory Space Enable (MSE), then application can start application traffic generation.

18.6.2.2 Initialization Sequence for EP Mode

The initialization sequence for RC mode is as follows:

1. Configure the GPIO configure for CLKREQ# and WAKE# signals. Configure the optional signals button_rst_n and perst_n if they are used. Please refer to section Interface Description for details.
2. Configure the CRU registers to provide reference clock to PCIe PHY. Please refer to CRU Chapter for more information. Configure PCIe PHY register if external differential clock is use as reference clock.
3. Configure USB3PHY General Register File to set PIPE signals which are unused for PCIe to appropriate values.
4. Configure PHY registers to set PCIe PHY work in PCIe EP Mode. Configure Client Registers to set the PCIe Controller device_type to EP mode.
5. Configure PHY registers to set TX PLL parameters to appropriate values. For programming details, please refer to Programming setting for PCIe PHY TX PLL.
6. Wait for PCIe PHY TX PLL lock, then release software reset for PCIe Controller.
7. Assert pcie_link_rst_grt in PCIE_GRF (refer to section Hot Reset and Link-Down Reset) to free ltssm_enable to prepare for link training. This step must be down because smlh_req_rst_not is asserted after power-on reset until first link up.
8. You can program controller registers before Link training start if necessary. Link training can be initialed by setting ltssm_enable bit in register PCIE_CLIENT_GENERAL_CON to 1. Link training success will set phy_link_up_int interrupt status bit in register PCIE_CLIENT_INTR_STATUS_MISC to 1. And if data flow initialization success, dll_link_up_int interrupt status bit will be set to one in same register. To
Initially, the controller tries to linkup at maximum Link width, when you have unused lanes in your system, you must tie them off using the hardware and software procedures outlined in section Tie off Unused Lanes.
Link speed will change to Gen2 automatically if you set direct_speed_change bit to 1 in PL_GEN2_CTRL_OFF register and both device support Gen2 speed.
9. The PCIe then can accept configuration setup access, after emulation done, the transactions can be initiated.

18.6.2.3 Tie Off Unused Lanes

When the link width of the PHY is smaller than the link width of the controller, you must tie off the unused lanes of the controller's PIPE interface.
Following PHY input signal pins should be assigned proper values by configuring PCIe PHY GRF:
`pipe_pd_i_l0/1[1:0]'=2'b11
`pipe_txelecidle_i_l0/1'=1'b1
`pipe_txdetectrx_lb_i_l0/1'=1'b0
`pipe_txdata_i_l0/1[31:0]'=32'h0
`pipe_txdatak_i_l0/1[3:0]'=4'h0
`pipe_ebuffmode_i_l0/1'=1'b0
`pipe_rxterm_i_l0/1'=1'b0
`pipe_txcompliance_i_l0/1'=1'b0
`pipe_txoneszeros_i_l0/1'=1'b0
Following registers should be reprogram to proper values:

- LINK_CAPABLE field of the PORT_LINK_CTRL_OFF register to 6h1 from 6h7. This is used by the LTSSM in Detect.
- NUM_OF_LANES[8:0] field of the GEN2_CTRL_OFF register. This indicates to the LTSSM, the number of lanes to check for exiting from L2.Idle or Polling.Active.

- PCIE_CAP_MAX_LINK_WIDTH field of the LINK_CAPABILITIES_REG register

18.6.3 Address Translation

The controller uses the internal Address Translation Unit(iATU) to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

The iAUT has 16 inbound Address Translation regions and 16 outbound Address Translation regions. The minimum size of an Address Translation Region is 64k and the maximum size of an Address Translation Region is 4G.

18.6.3.1 Outbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The ATU also supports type translation. Without address translation, your application address is passed unmodified to the TLPs directly through the Tx application interface. You can program the iATU to implement your own outbound address translation scheme. The outbound features is as follows:

- Address Match mode operation for MEM and I/O, CFG, and MSG TLPs. No translation for completions.
- Supports type translation through TLP type header field replacement for MEM or I/O types to MSG/CFG types.
- Programmable TLP header field replacement. Including TYPE, TC, AT, ATTR, MSG-Code, TH, PH, ST.
- Multiple (up to 16) address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- Configuration Shift mode. Optimizes the memory footprint of CFG accesses destined for the Rx application interface in a multifunction device.
- Response code which defines the completion status to return for accesses matching a region.
- Supports regions from 64 KB to 4 GB in size.
- Payload Inhibit marks all TLPs as having no payload data.
- Header Substitution replaces bytes 8 to 11 (for 3 DWORD header) or bytes 12 to 15 (for 4 DWORD header), inclusive, of the outbound TLP header.
- Tag Substitution of the outbound TLP tag field.
- Function number bypass mode to allow function number information to be supplied from your application transmit interface while translating the address and other attributes of the TLP.
- DMA bypass mode to allow TLPs which are initiated by the embedded DMA engine, to pass through the iATU untranslated.

18.6.3.2 Outbound Basic Operation

The address field of each request MEM and I/O TLP is checked to see if it falls into any of the enabled address regions defined by the Start and End addresses as defined in Figure below. When an address match is found, then the TLP address field is modified as follows:

Translated Address = Original Address - Base Address + Target Address

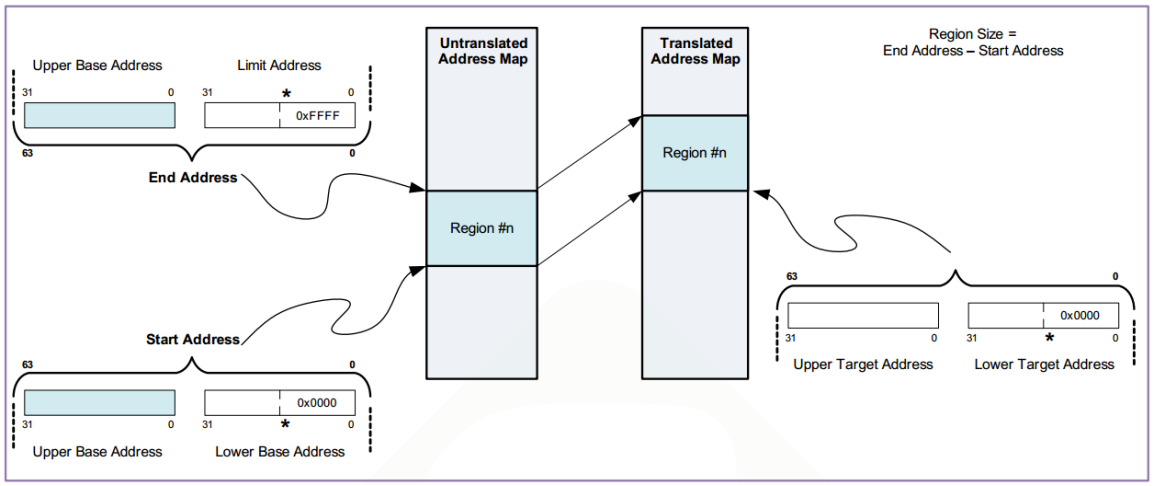


Fig. 18-6 PCIe Hot Reset Control Structure

The TYPE, TC, AT, TH, PH, ST, Function Number, and ATTR header fields are replaced with the corresponding fields in the IATU_REGION_CTRL_1_OFF_OUTBOUND_0 register. When your application address field matches more than one of the CX_ATU_NUM_OUTBOUND_REGIONS address regions, then the first (from lowest number 0) enabled region to be matched is used. For details on what happens when there is no address match, see "No Address Match Result". This operational mode (called Address Match Mode) is always used for outbound translation.

The minimum size of an address translation region is 64KB. So the lower 16 bits of the Base, Limit, and Target registers are zero and all address regions are aligned on 64 KB boundaries.

18.6.3.3 Outbound Detailed Operation

18.6.3.3.1 RID BDF Number Replacement

When there is a successful address match on an outbound TLP, then the function number used in generating the function part of the requester ID field of the TLP is taken from the 3-bit Function Number field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_iregister. The value in this field must be 0x0 unless multifunction operation in the controller is enabled. To override this behavior, use the "Function Number Translation Bypass Feature" described later.

18.6.3.3.2 iATU Outbound MSG Handling

The iATU supports TYPE translation/conversion of MEM and I/O TLPs to Msg/MsgD TLPs. This supports applications that are unable to directly generate Msg/MsgD TLPs. When there is a successful address match on an outbound MEM TLP, and the translated TLP type field is MSG (that is, the type field of the IATU_REGION_CTRL_1_OFF_OUTBOUND_i register is 10xxx), then the message code field of the TLP is set to the value in the Message Code field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.A Memory Write with an effective length of '0' is converted to Msg and all other MWr TLPs are converted to MsgD.

18.6.3.3.3 MEM-CFG Type Translation

The iATU supports translation of I/O and MEM TLPs to CFG TLPs. This is useful for applications that are unable to generate CFG TLPs. The 16-bit BDF is located at bits [31:16] of the translated address where:

Translated Address = Original Address - Base Address + Target Address

As an example:

Original Address[31:16] = {13h0,function_no[2:0]}

Base Address[31:16] = 16h0

Target Address[31:16] = {bus_no[7:0],device_no[4:0],3h0}

then:

Translated Address[31:16] = BDF ={bus_no[7:0], device_no[4:0], function_no[2:0]}

To handle eight functions (as the previous example indicates), you should use a 19-bit wide region size. For CFG transactions created directly by your application (asopposed to the iATU), you must ensure that the BDF field does not match any programmed iATU address region or else unintentional type translation could occur.

18.6.3.3.4 CFG Shift Feature

This feature is enabled by setting the CFG_SHIFT_MODE field the

IATU_REGION_CTRL_2_OFF_OUTBOUND_0 register. The iATU uses bits [27:12] of the original address to form bits [31:16] (BDF location) of the outgoing CFG TLP. This supports the Enhanced Configuration Address Mapping (ECAM) mechanism by allowing all outgoing I/O and MEM TLPs (that have been translated to CFG) to be mapped from memory space into any 256 MB region of the PCIe configuration space.

18.6.3.3.5 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeros in the upper 32 bits of the translated address. Otherwise, it sets it to four DWORDs when it detects a 64-bit address (that is, when there is a '1' in the upper 32 bits of the translated address). When the original address and the translated address are of different format, the iATU ensures that the TLP header size matches the translated address format.

18.6.3.3.6 Invert Feature

In normal operation an address match on an outbound TLP occurs when the untranslated address is in the region bounded by the base address and limit address. When the invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the base address and limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_iregister.

18.6.3.3.7 DMA Bypass Feature

When you do not want the iATU to translate outbound requests that are generated by the DMA, you must implement one of the following approaches:

■ Ensure that the combination of DMA channel address programming and iATU control register programming causes no translation of DMA traffic to be done in the iATU.

■ Activate the DMA bypass mode to allow request TLPs which are initiated by the embedded DMA controller to pass through the iATU untranslated. You can activate the DMA bypass mode by setting the DMA Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register to 1.

18.6.3.3.8 Function Number Translation Bypass Feature

In this mode the function number of the translated TLP is taken from your application transmit interface and not from the Function Number field of the REGION_CTRL_1_OFF_OUTBOUND_i register. You can activate the function number bypass mode by setting the Function Number Translation Bypass Enable field in the IATU_REGION_CTRL_2_OFF_OUTBOUND_i to '1'.

18.6.3.3.9 General Bypass

Application can program PCIE_CLIENT_AXI_SLV_ATU_BYPASS register to do general ATU bypassing. Note that you should make sure that there is no transfer pending before you program this register.

18.6.3.3.10 Header Substitution (Tx)

When enabled and region address is matched, the iATU fully substitutes bytes 8-11 (for 3 DWORD header) or bytes 12-15 (for 4 DWORD header) of the outbound TLP header with the contents of the LWR_TARGET_RW field in IATU_LWR_TARGET_ADDR_OFF_OUTBOUND_i. The expected usage scenario is for Vendor Defined Msg/MsgD and ATS transactions over the AXI bridge which is normally inefficient requiring a very large iATU region. Enabled using the HEADER_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

18.6.3.3.11 Tag Substitution (Tx)

When enabled and region address is matched, the iATU substitutes the TAGfield of the outbound TLP header with the contents of the TAG field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i. The expected usage scenario is translation from AXI MWr to Vendor Defined Msg/MsgD. Enabled using the TAG_SUBSTITUTE_EN field in IATU_REGION_CTRL_2_OFF_OUTBOUND_i.

Your application must not attempt to perform TAG substitution for outgoingnon-posted TLPs.

Note: If the iATU is programmed to allow a TLP to be matched to more than one iATU outbound regions, the Function Number Translation Bypass field of the IATU_REGION_CTRL_2_OFF_OUTBOUND_i register should be same for every region where that TLP can be matched.

18.6.3.3.12 No Address Match Result

When there is no address match then the address is untranslated but the TLP header information (for fields that are programmable) comes from the relevant fields on the

application transmit interface AXI slave.

18.6.3.4 Outbound Programming Example

Define Outbound Region 1 as:
64 KB I/O region from 0x80000000_d000000to 0x80000000_d000ffff, to be mapped to 0x00010000in the PCIe I/O space.

1. Setup the Region Base and Limit Address Registers.
   Write 0xd0000000to Address {0x208} to set the Lower Base Address.
   Write 0x80000000to Address {0x20C} to set the Upper Base Address.
   Write 0xd000ffff to Address {0x210} to set the Limit Address.
2. Setup the Target Address Registers.
   Write 0x00010000to Address {0x214} to set the Lower Target Address.
   Write 0x00000000to Address {0x218} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000002to Address {0x200} to define the type of the region to be I/O.
4. Enable the region.
   Write 0x80000000to Address {0x204} to enable the region.

18.6.3.5 Inbound Features

Address translation is used for mapping different address ranges to different memory spaces supported by your application. A typical example maps your application memory space to PCI memory space. The iATU supports type translation. Without address translation, your application address is passed from the TLPs directly through the AXI application interface. You can program the iATU to implement your own inbound address translation scheme without external logic.

- Programmable Match mode operation for MEM, I/O, CFG, and MSG TLPs. No translation for completions.
- Selectable BAR Match mode operation for I/O and MEM TLPs:

TLPs destined for the internal CDM (or ELBI) in an upstream port are not translated.
TLPs that are not error-free (ECRC, malformed and so on) are not translated.

- Programmable TLP header field matching:
  TYPE/TD/TC/AT/ATTR/MSG-Code/TH/PH/ST

❑ Function Number

- Multiple (up to 16) address regions programmable for location and size.
- Programmable enable/disable per region.
- Automatic FMT field translation between three DWORDs and four DWORDs for 64-bit addresses.
- Invert Address Matching mode to translate accesses outside of a successful address match.
- ECAM Configuration Shift mode to allow a 256 MB CFG1 space to be located anywhere in the 64-bit address space.
- Supports regions from 64 KB to 4 GB in size.
- Single Address Location to allow all TLPs to be translated to a single address location.
- Msg Type Match Mode to allow matching of any TLP of type Message.

18.6.3.6 Inbound Basic Operation

18.6.3.6.1 Overview

The following translation rules and limitations apply:

- When there is no match, then the address is untranslated. In addition
- TLPs destined for the internal registers in an upstream port are not translated.
- TLPs that are not error-free (ECRC, malformed and so on) are not translated.
- Address translation of all TLP types (MEM, I/O, CFG, and MSG) except completion is supported in Address Match mode. In BAR Match mode, only translation of I/O and MEM is supported.

The setting of the MATCH_MODE field in IATU_REGION_CTRL_2_OFF_INBOUND_0 determines how iATU inbound matching is done for each TLP type.

Table 18-9 Determination of Match Mode

TLP Type	MATCH_MODE =0	MATCH_MODE =1
MEM or I/O	Address Match Mode	BAR Match Mode
CFG0	Routing ID Match Mode	Accept Mode
MSG/MSGD	Address Match Mode	Vendor ID Match Mode

18.6.3.6.2 I/O and MEM Match Modes

Inbound address translation for I/O and MEM TLPs operates in one of two matching modes as determined by the "Inbound Match Mode" field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register.

Address Match Mode: The operation is similar to "Outbound Basic Operation (Address Match Mode)". The address field of each request TLP is checked to see if it falls into any of the enabled address regions. When an address match is found then the TLP address field is modified as follows:

Address = Address - Base Address + Target Address

BAR Match Mode:

Looking for an address match is a two-step process.

1. The standard internal PCI Express BAR Matching Mechanism checks if the address field of any MEM and I/O request TLP falls into any address region defined by the enabled BAR addresses and masks.
2. When a matched BAR is found, then the iATU compares the BAR ID to the BAR Number field in the IATU_REGION_CTRL_2_OFF_INBOUND_0 register for all enabled regions. Figure below provides more details on inbound translation in BAR Match Mode.

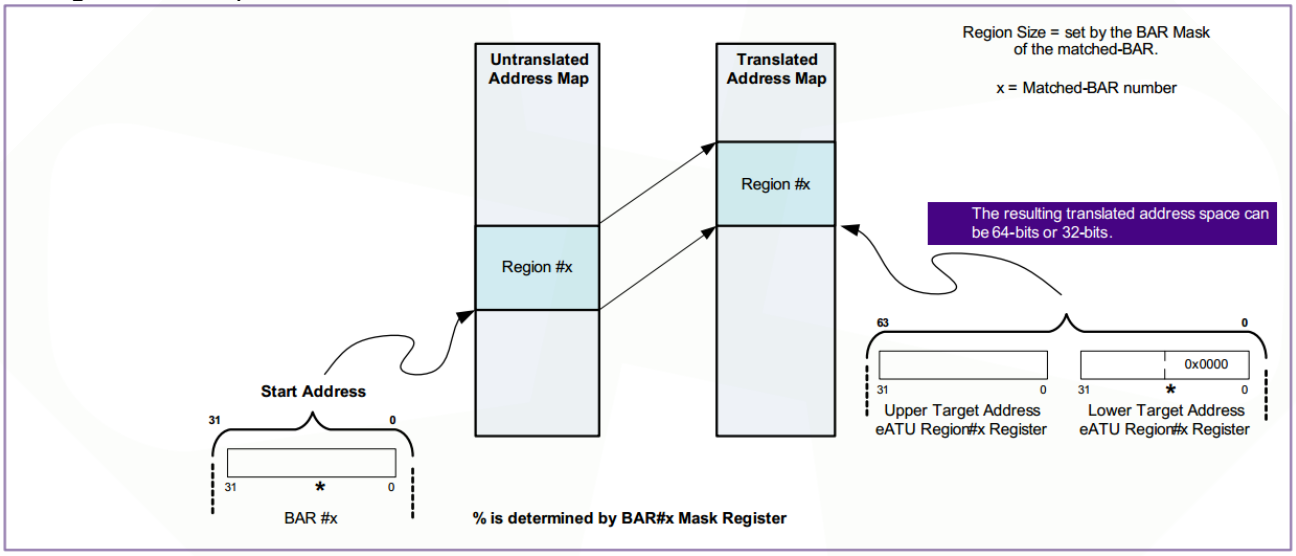


Fig. 18-7 Inbound BAR Match Mode

18.6.3.7 Inbound Detailed Operation

18.6.3.7.1 Single Address Location

When enabled and region address is matched, the TLPs can be translated to a single address location as determined by the target address register of the iATU region. This feature can be enabled using the SINGLE_ADDR_LOC_TRANS_EN field in IATU_REGION_CTRL_2_OFF_INBOUND_i. This feature is useful fortranslating messages on AXI bridge.

18.6.3.7.2 CFG Handling (Upstream Port)

The controller normally routes CFG TLPs (to the internal CDM or ELBI) without translation. The iATU only translates CFG0 TLPs that the controller has routed to the TRGT1. Inbound address translation for CFG0 TLPs operates in one of two matching modes as determined by the Inbound CFG0 Match Mode field in the IATU_REGION_CTRL_2_OFF_INBOUND_i register.

Accept Mode

The controller always accepts CFG0 TLPs even when the CFG bus number does not match the current bus number of the device. This mode follows that behavior. The routing ID of received CFG0 TLPs are ignored when determining a match.

Routing ID Match Mode

The operation is similar to "Outbound Basic Operation (Address Match Mode)". The routing

ID of the inbound CFG0 TLP must fall within the Base and Limit of the defined iATU region for matching to proceed. The iATU interprets the routing ID (Bytes1 8-11 of TLP header) as an address. This corresponds to the upper 16 bits of the address in MEM and I/O transactions.

CFG Shift Feature

Inbound CFG transactions routed to the Rx application interface can exist anywhere in address space, because the PCIe controller filter processes the routing ID (BDF) as bits [31:16] of an address. This BDF changes according on the PCIe bus topology. A compressor feature (CFG Shift Feature) can be enabled by setting the CFG Shift bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Bits [15:12] of the third DWORD1 of CFG TLPs are reserved. The compressor feature uses this fact to reduce the memory requirement. This shifts/maps the BDF (bits [31:16] of the third header DWORD, which would be matched against the Base and Limit addresses) of the incoming CfgRd0/CfgWr0 down to bits [27:12] of the translated address.

18.6.3.7.3 Optional Matching Fields

In address and BAR match modes, a successful address/BAR match can be optionally gated by successful matching of the following programmable TLP header fields (per region):

- TYPE/TD/TC/AT/ATTR/TH/PH/ST
- MSG Code (MSG TLPs only)
- Function number (MEM, I/O, or CFG TLPs only)
- Virtual function number (MEM or I/O TLPs only)

For each of the previous fields in the IATU_REGION_CTRL_1_OFF_INBOUND_i register, there is an associated Match Enable bit in the IATU_REGION_CTRL_2_OFF_INBOUND_i register. Address translation only proceeds when compares on all enabled field are successful.

18.6.3.7.4 Response Code Feature

When the Response Code field of the IATU_REGION_CTRL_REG_2_INBOUND_i register is set to a value other than 00, the controller uses it to determine the completion status field of completion TLPs sent in response to successfully matched non-posted TLPs. This can be set to unsupported request (UR) or completer abort (CA). When the error response field is set to 2b00, then the normal receive filter response for this TLP is used.

18.6.3.7.5 Inbound MSG Handling

Inbound message (Msg/MsgD) transactions can use one of two matching modes:

Address Match Mode

The third and fourth header DWORDs are treated as an address and are compared against the iATU Region Base and Limit Address registers. For vendor defined messages this allows specific messages to be filtered into memory at the target address. The Upper Base address should be set to BDF and Vendor ID. The Lower Base address can be used as a filter for specific messages.

Vendor ID Match Mode

This mode is relevant for ID-routed vendor defined messages. The iATU ignores the routing ID (BDF) in bits [31:16] of the third DWORD of the TLP header1, but compares it against the vendor ID in bits [15:0] of the third DWORD of the TLP header (bytes1 10 and 11). This allows vendor defined messages to be filtered against specific vendor IDs without needing to know the BDF number which might vary depending on the PCI topology. Bits [15:0] of the Region Upper Base register should be programmed with the required vendor ID as follows:

Region Upper Base [15:8] =byte 10

Region Upper Base [7:0] =byte 11

The lower base and limit register should be programmed to translate TLPs based on vendor-specific information in the fourth DWORD of the TLP header.

18.6.3.7.6 Msg Type Match Mode

Inbound message (Msg/MsgD) transactions can also use Msg Type Matching mode. When this mode is enabled and Single Address Location is enabled, the iATU matches Msg TLP Type field with TYPE field of IATU_REGION_CTRL_1_OFF_INBOUND_i register.

If Fuzzy Type Match Mode is also enabled, then any Msg received will be matched (that is, Msg Type's sub-field r[2:0], which specifies the Message routing mechanism, is ignored). The Message should be consumed by your application before the next message arrives as all messages go to the same address.

If SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is set for any region, then you must ensure that the same TLP cannot be matched in any other region where SINGLE_ADDRESS_LOCATION_TRANSLATE_EN is not set. If this happens radm_trgt1_hdr_uppr_bytes could have incorrect data.

18.6.3.7.7 Fuzzy Type Match Mode

When enabled, the iATU relaxes the matching of the TLP type field against the expected type field so that:

- CfgRd0 and CfgRd1 TLPs are seen as identical. Similar with CfgWr0 and CfgWr1.
- MWr, MRd and MRdLk TLPs are seen as identical.
- The routing field of MsgD TLPs is ignored.
- Atomic Ops TLPs-FetchAdd, Swap, and CAS are seen as identical.

For example, CFG0 in the type field in the IATU_REGION_CTRL_1_OFF_INBOUND_i register matches against an inbound CfgRd0, CfgRd1, CfgWr0, or CfgWr1 TLP. To enable this feature, set the Fuzzy Type Match Mode bit of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

18.6.3.7.8 FMT Translation

The iATU automatically sets the TLP format field for three DWORDs when it detects all zeroed in the upper 32 bits of the translated address. Otherwise it sets it to four DWORDs when it detects a 64-bit address (when there is a 1 in the upper 32 bits of the translated address). When the original address and the translated address are of a different format then the iATU ensures that the TLP header size matches the translated address format.

18.6.3.7.9 Invert Feature

Normally an address match on an inbound TLP occurs when the untranslated address is in the region bounded by the Base address and Limit address. When the Invert feature is activated, an address match occurs when the untranslated address is not in the region bounded by the Base address and Limit address. This feature is activated by setting the Invert field of the IATU_REGION_CTRL_OFF_2_INBOUND_i register.

18.6.3.8 Inbound Programming Example

You must not update the iATU registers while operations are in progress on the AXI bridge slave interface.

Example 1:

Define Inbound Region 2 as: MEM region matching BAR4 (BAR match mode) mapping to 0x8000_0000_2000_0000 in your application memory space

1. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x508} to set the Lower Target Address.
   Write 0x80000000 to Address {0x50C} to set the Upper Target Address.
2. Configure the region through the Region Control 1 Register.
   Write 0x00000000 to Address {0x500} to define the type of the region to be MEM.
3. Enable the region for BAR Match Mode.
   Write 0xC0000400 to Address {0x504} to enable the region for BAR match mode for BAR#4.

Example 2:

MEM region matching TLPs with addresses in the range 0x00010000 to 0x0005ffff mapped to 0x2000_0000 - 0x2004_ffff in your application memory space.

1. Setup the Region Base and Limit Address Registers.
   Write 0x00010000 to Address {0x108} to set the Lower Base Address.
   Write 0x00000000 to Address {0x10C} to set the Upper Base Address.
   Write 0x0005ffff to Address {0x110} to set the Limit Address
2. Setup the Target Address Registers.
   Write 0x20000000 to Address {0x114} to set the Lower Target Address.
   Write 0x10000000 to Address {0x118} to set the Upper Target Address.
3. Configure the region through the Region Control 1 Register.
   Write 0x00000000 to Address {0x100} to define the type of the region to be MEM.
4. Enable the region.
   Write 0x80000000 to Address {0x104} to enable the region in address match mode

18.6.4 PCIe Embedded DMA

18.6.4.1 PCIe DMA Overview

The RC system CPU, or the EP application CPU, can off load the transfer ring of large blocks

of data to the embedded DMA controller, leaving the CPU free to perform other tasks. You can configure the DMA to have one to eight read channels and one to eight write channels. It can simultaneously perform the following types of memory transactions:

DMA write

Transfer (copy) of a block of data from local memory to remote memory.

DMA read

Transfer (copy) of a block of data from remote memory to local memory.

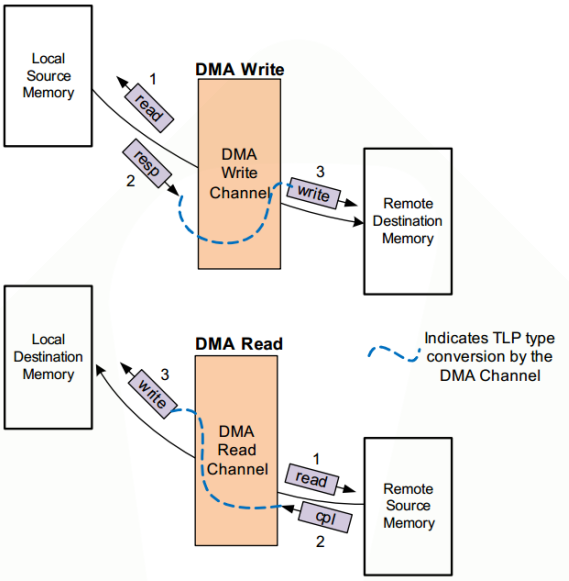


Fig. 18-8 System Level View of PCIe Embedded DMA

Therefore the DMA supports full duplex operation, processing read and write transfers at the same time, and in parallel with normal (non-DMA) traffic. Upon completion of a DMA transfer or an error, the DMA optionally interrupts the local CPU or sends an interrupt MWr (IMWr) to the remote CPU. The DMA is highly configurable and you can program it using the local DBI or over the PCIe wire.

In linked list mode, the DMA fetches the transfer control information (called channel context) for each transfer (block), from a list of DMA elements that have constructed in local memory.

18.6.4.2 Interrupts and Error Handling

The DMA generates two interrupts, read channel interrupt and write channel interrupt. Each of them can be caused by one of the two reasons:

Done: The DMA successfully completes the transfer.

Abort: The DMA fails to complete the transfer, or an error occurs during the transfer.

The interrupts are signaled to the software on your CPU, using one or both of the following mechanisms:

- Locally through the edma_rd_int or edma_wr_int field of PCIE_CLIENT_INTR_STATUS_MISC register.
- Remotely using a posted memory write (IMWr), which can be interpreted as an MSI or MSIX when directed toward the RC.

For remote interrupt, there are two programmable IMWr addresses per channel, one each for the done and abort interrupts. For MSI, you must program all IMWRr address registers with the same MSI address, as PCIe only supports a single MSI address per function.

A single IMWr data register is used for both types of interrupts, so you must read DMA_READ_INT_STATUS_OFF(or DMA_WRITE_INT_STATUS_OFF) to identify the interrupt type.

The interrupt handling mechanism is different for linked list (LL) mode (than non LL mode), and there are also some differences between the read and write channels.

18.6.4.2.1 Non Linked List Mode Interrupt Handling

You enable the local and remote interrupts through the local and remote interrupt enable (LIE and RIE) bits: DMA_CH_CONTROL1_OFF_WRCH_0.lie and DMA_CH_CONTROL1_OFF_WRCH_0.rie.

In the write channel, there is only one error condition that results in an abort interrupt. For

more details, see “Linked List Mode” on next section. You mask, clear, and read the status of each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below:

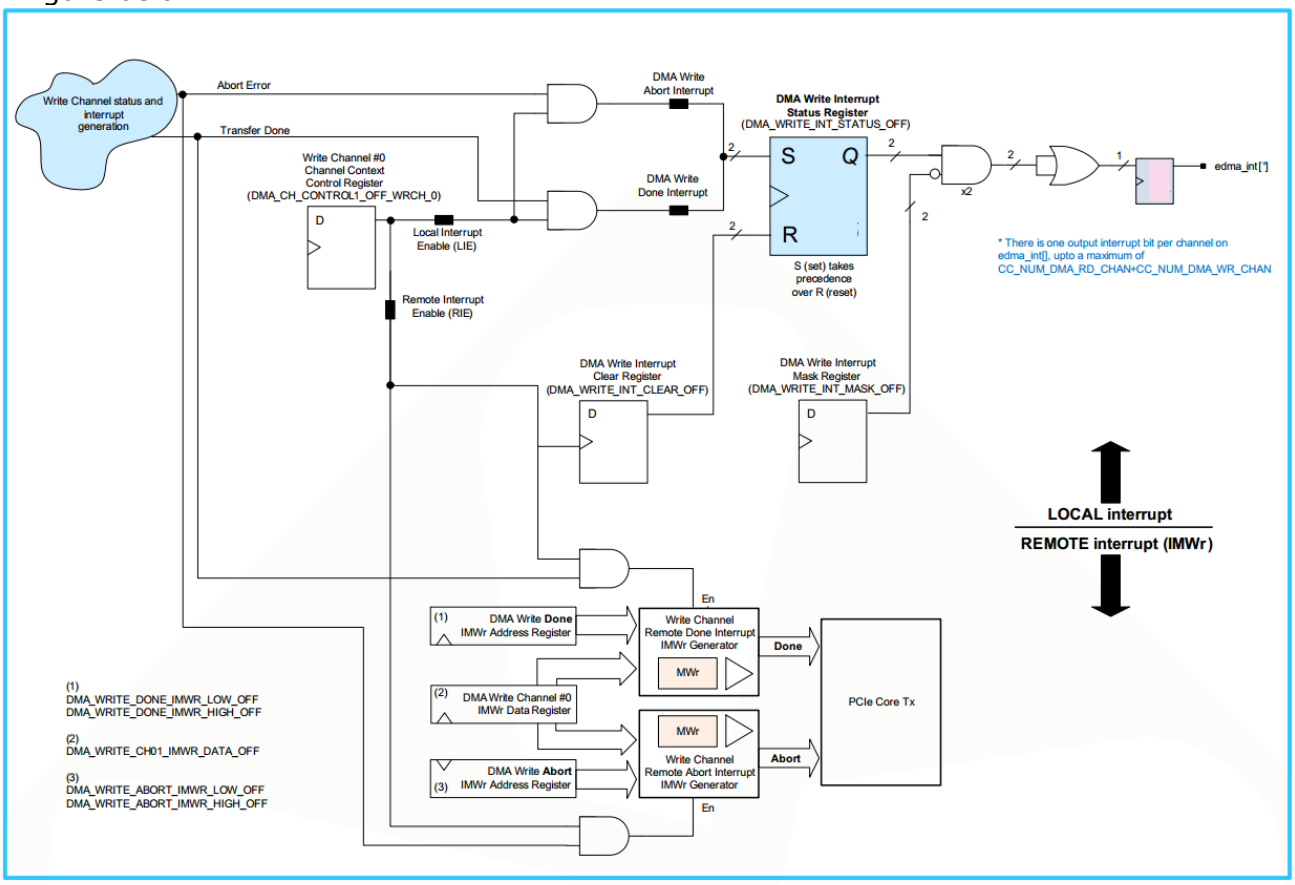


Fig. 18-9 Write Interrupt Generation - Non Linked List Mode

In the read channel, there are five error conditions that results in an abort interrupt. For more details, see “Linked List Mode” on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. However, you can read the status of each of the five abort errors (that contribute to the abort interrupt) through DMA_READ_ERR_STATUS_LOW_OFF and DMA_READ_ERR_STATUS_HIGH_OFF.

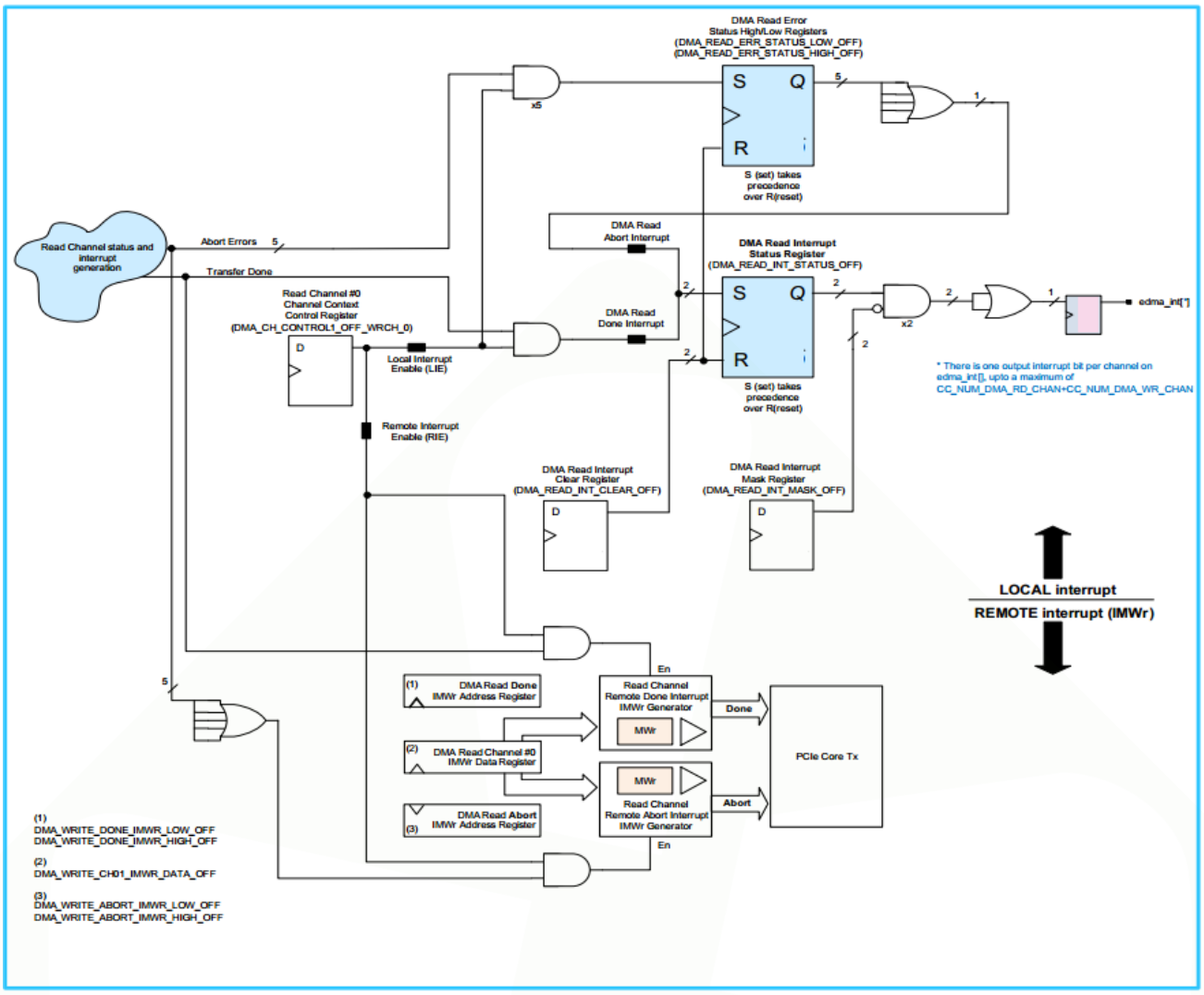


Fig. 18-10 Read Interrupt Generation - Non Linked List Mode

18.6.4.2.2 Linked List Mode Interrupt Handling

The LIE and RIE bits in the LL element enable the channel done interrupts (local and remote). The LLLAIE and LLRAIE bits of the DMA_WRITE_LINKED_LIST_ERR_EN_OFF and DMA_READ_LINKED_LIST_ERR_EN_OFF registers enable the channel abort interrupts (local and remote). In the write channel, there are two error conditions that results in an abort interrupt. For more details, see "Linked List Mode" on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. You can read the status of each of the two abort errors (that contribute to the abort interrupt) through the DMA_WRITE_ERR_STATUS_OFF register.

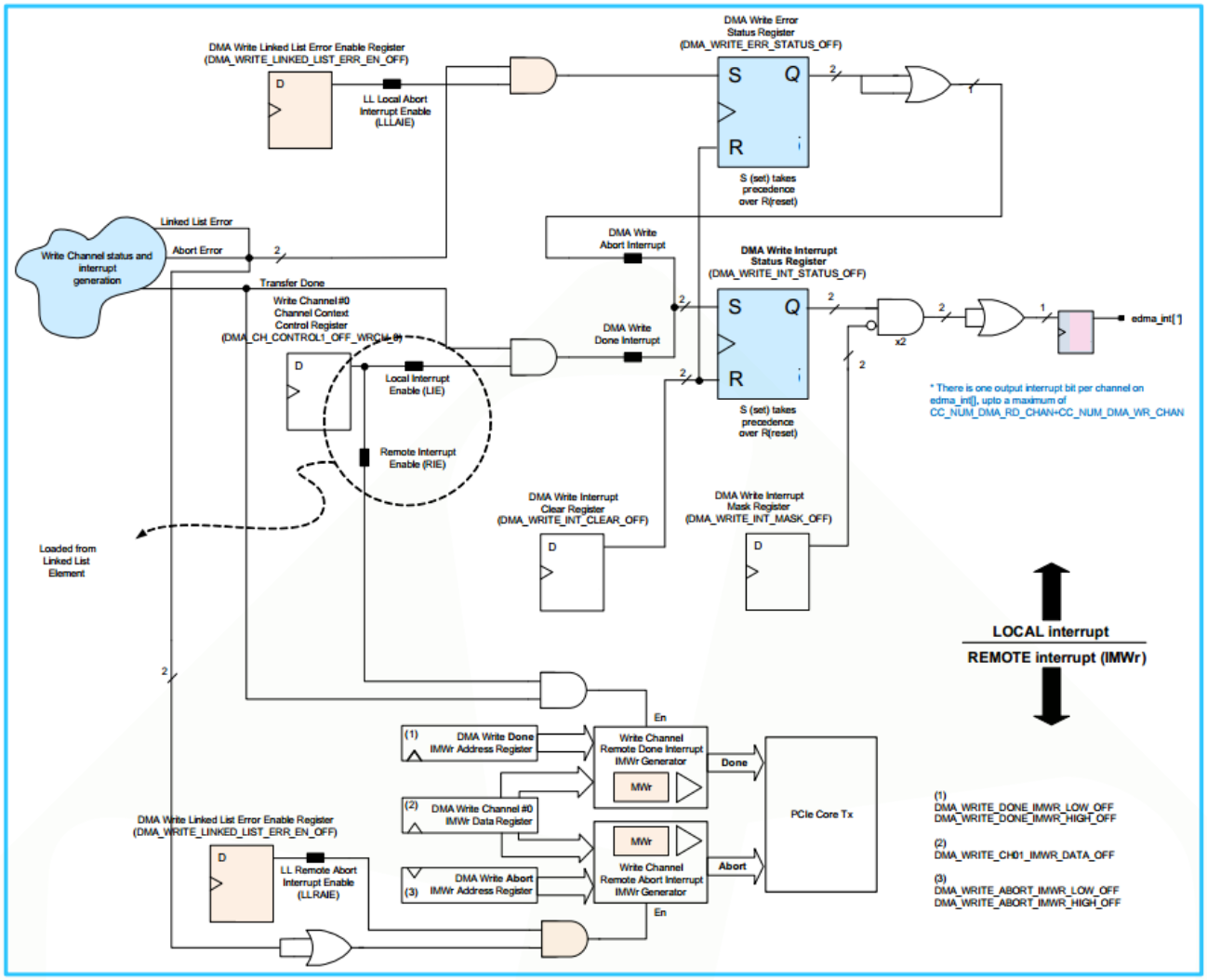


Fig. 18-11 Write Interrupt Generation - Linked List Mode

In the read channel, there are six error conditions that results in an abort interrupt. For more details, see “Linked List Mode” on next section. You mask and clear each of the two interrupts (done and abort) through the DMA interrupt registers as indicated in figure below. You can read the status of each of the six abort errors (that contribute to the abort interrupt) through the DMA_READ_ERR_STATUS_LOW_OFF and DMA_READ_ERR_STATUS_HIGH_OFF registers.

In non-linked list mode, LIE acts as a global switch. However when in linked list mode, LIE is just local to the current linked list element and the global switch is LLLAIE.

If the DMA driver is running on the host and the interrupt service routine is reading local interrupts to determine if the transfer is successful, then you must set LIE and RIE in the same element and you should mask or ignore the local interrupt pin. Setting RIE and LIE in element A followed by RIE (only) in element B is not a verified usage scenario.

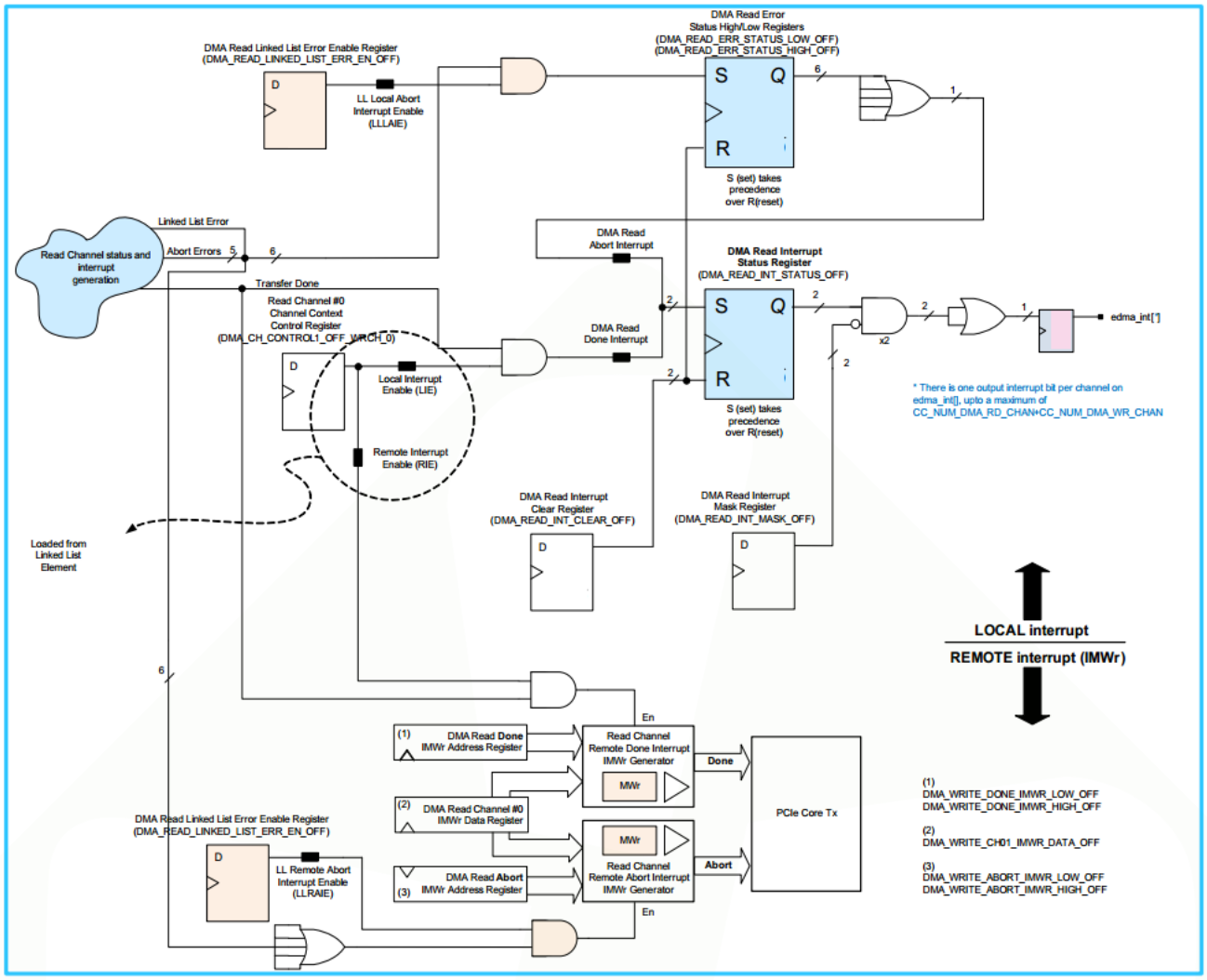


Fig. 18-12 Read Interrupt Generation - Linked List Mode

18.6.4.3 Linked List Mode

The DMA provides a linked list (LL) mode to efficiently move data from source to destination with minimal intervention from the local CPU. This mode provides an alternative to programming the DMA multiple times to transfer multiple blocks of data. The programming information (address, size, and so on) for each block of memory is pre-programmed by your software into a LL element (also known as a descriptor) in local memory. Each element (called a data element) in the LL structure (called a transfer list) can transfer up to 4 GB of data.

You enable LL operation for a channel, by setting the LLE field of the DMA_CH_CONTROL1_OFF_[WRCH|RDCH]_0 register to 1. Your application must produce the LL element structure in local memory as shown in figure below. Normally, all of the elements are contiguous (one after the other) in memory, and each element has six DWORDs containing the information about the block of data to be transferred. You program the channel context registers (DMA_LLP_LOW_OFF_WRCH_0 and DMA_LLP_HIGH_OFF_WRCH_0) with the location of where you have placed the LL element structure in local memory.

When you start the DMA transfer (by writing to the DMA Write Doorbell Register DMA_WRITE_DOORBELL_OFF or DMA Read Doorbell Register DMA_READ_DOORBELL_OFF), the DMA reads (consumes) each element from local memory, and loads the information (SAR, DAR, size, and so on) from that element into the channel context registers in the DMA. These channel context registers determine the operation of the channel that the DMA controller is currently servicing. The DMA then proceeds to transfer the block of data (as defined by the element), and when it is finished, reads the next element from local memory. Normally, all of the elements are contiguous (one after the other) in memory, with the starting address defined in the channel context DMA Linked List Pointer Low Register

DMA_LLP_LOW_OFF_WRCH_0.
When you want to jump in local memory to another element list (or recycle the consumed elements), then you set the LLP bit in the element (for example, link element #N-1 in figure below), specify the location of the next element structure using the LL Element Pointer DWORDs, and, set TCB to 1 (for recycling) or to 0 (to jump to another list).

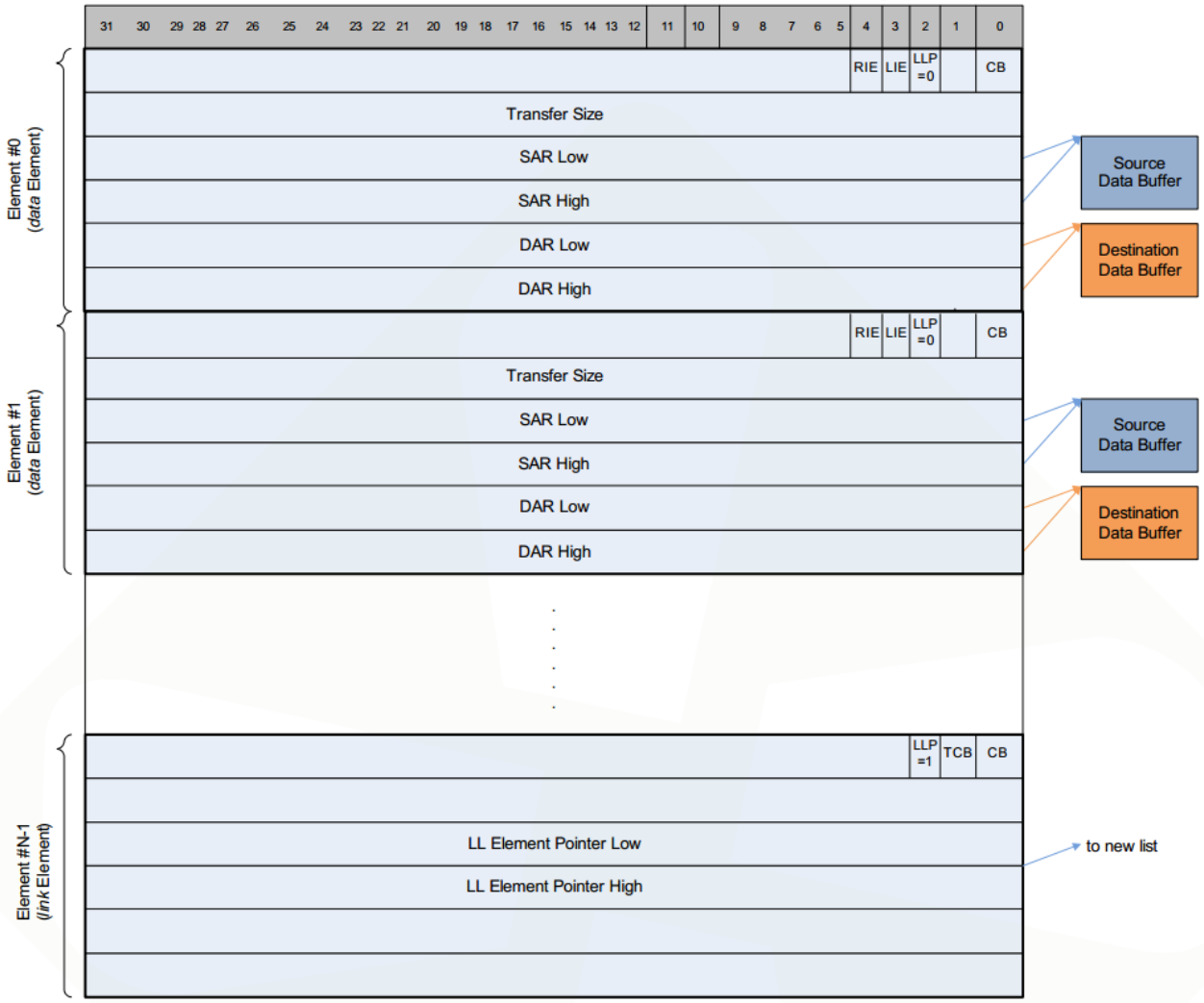


Fig. 18-13 Linked List Element/Descriptor Structure in Local Memory

18.6.4.3.1 LL Element and Channel Context Registers

Notice the similarity between a data element and the DMA Channel Context registers for each channel. Each element has six DWORDs as in Figure 9-6. There are eight channel context registers (DWORDs) for a channel. The DMA loads the six element DWORDs into the following channel context:

- CB, LLP, LIE, and RIE fields of the DMA Channel Control 1 register
- DMA Transfer Size
- DMA SAR Low and DMA SAR High
- DMA DAR Low and DMA DAR High

The definitions of the element DWORD bit fields are the same as the DMA Channel Context registers described in the "DMA Detail Register Description" section, with the exception of the LIE and RIE bits. The LIE and RIE bits in a LL element, only enable the done interrupt. In non-LL mode, the RIE and LIE bits (in the channel context registers) enable the done and abort interrupts.

18.6.4.4 Flow Control

18.6.4.4.1 Overview

This optional feature is available only for those channels which are configured to operate in linked list (LL) mode. It enables your application to flow control the DMA controller by using PCIE_CLIENT_DMA_HSHAKE_TOGG register, that is, your application determines when data block transfer starts.

In normal mode, as soon as the DMA is doorbelled, the DMA reads the LL descriptor, and starts the data block transfer. When this feature is enabled, the DMA reads the descriptor, but starts the data transfer only when your application logic toggles the [w|r]dxfer_go_togg field in PCIE_CLIENT_DMA_HSHAKE_TOGG register.
The DMA handshake mechanism can be turned on or off per channel using DMA_[WRITE/READ]_ENGINE_EN_OFF register. The handshake mechanism cannot be enabled/disabled when the channel status isactive, that is, when DMA_CH_CONTROL1_OFF_[WR|RD]CH_i.CS =01.

18.6.4.4.2 DMA Handshake Operation

The handshake between the DMA and your application is done using [w|r]dxfer_go_togg and [w|r]dxfer_done_togg. In case of a DMA Write, your application should toggle the wdxfer_go_togg signal to indicate data block availability. In case of a DMA Read, your application should toggle the rdxfer_go_togg signal to indicate that your application hardware is ready to receive a data block.
To keep a track of [w|r]dxfer_go_togg signal toggles, the DMA implements a 5-bit handshake counter for each write/read channel. When your application toggles [w|r]dxfer_go_togg signal, the handshake counter is incremented. The handshake counter value is taken into account by the DMA before performing the data transfer for each descriptor. The data transfer happens only when the handshake counter value is non-zero. When the data transfer is complete, the DMA decrements the handshake counter, and toggles [w|r]dxfer_done_togg signal to indicate completion of data transfer to your application.
The handshake counter is 5-bit wide, so only 32 outstanding [w|r]dxfer_go_toggrequests can be handled by the DMA for each channel. The DMA does not implement an overflow protection or overflow error indication mechanism for the handshake counter. It is the responsibility of your application to keep the number of [w|r]dxfer_go_togg toggles under check.
One example of the DMA operation when the handshake feature is enabled for a write channel is as follows:

1. The CPU doorbells channel 0.
2. The DMA resets the handshake counter for channel 0.
3. The DMA reads LL element 0 descriptor. After the DMA receives descriptor read completions, the DMA checks the value of the handshake counter.

If handshake counter =0, DMA waits until handshake counter >0 before transferring the data block.
If handshake counter >0, DMA transfers the data block immediately.

4. After the data transfer is complete, the DMA Decrements the handshake counter, and Toggles wdxfer_done_togg.
5. Steps 3-4 are repeated for all the remaining elements of the linked list.

18.6.4.5 Using the DMA

18.6.4.5.1 Source and Destination Address Registers

The DMA channel context SAR and DAR registers (DMA_SAR_LOW_OFF_WRCH_0, DMA_SAR_HIGH_OFF_WRCH_0 etc.) provide support for remote-to-local, and local-to-remote PCIe address mapping. You program the start of the local and remote data buffers using these registers, and the DMA increments the SAR and DAR as the DMA transfer progresses. For a write transfer, the SAR is the address of the local memory, and the DAR is the address of the remote memory, as shown in figure below.

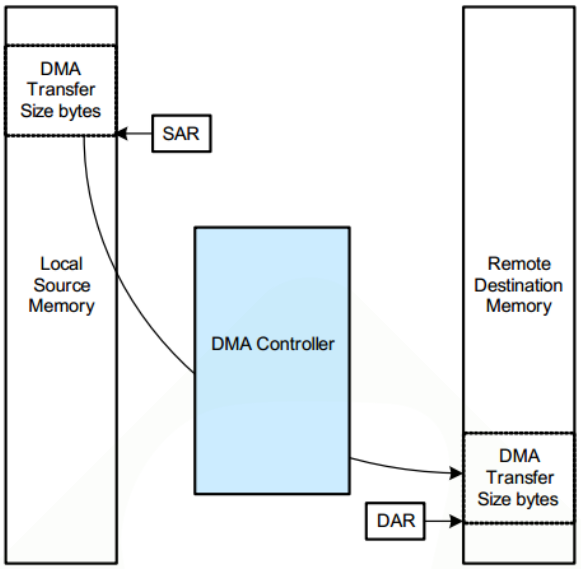


Fig. 18-14 Write Transfer: SAR and DAR for Write Channel

For a read transfer, the SAR is the address of the remote memory, and the DAR is the address of the local memory, as shown in Figure below.

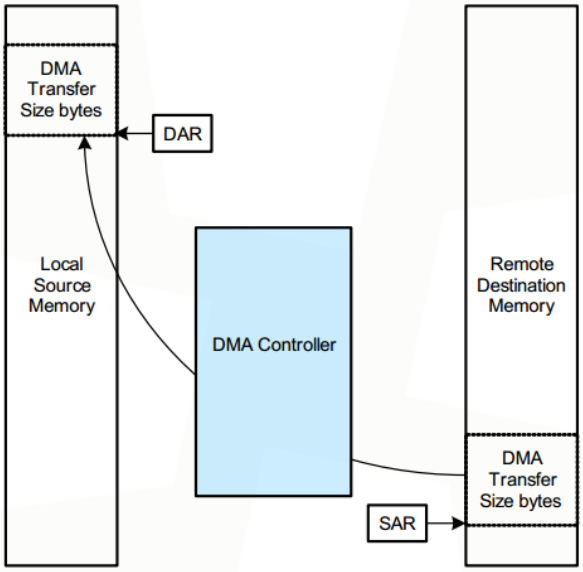


Fig. 18-15 Read Transfer: SAR and DAR for Write Channel

18.6.4.5.2 DMA Transfer Size Registers

You program the DMA transfer size using the DMA Transfer Size Register (DMA_TRANSFER_SIZE_OFF_WRCH_0 or DMA_TRANSFER_SIZE_OFF_RDCH_0). The maximum DMA transfer size is 4GB, and the minimum transfer size is one byte (0x1). The DMA decrements the value in this register as the DMA transfer progresses. When all bytes are successfully transferred, the value in this register is zero. In LL mode, the DMA overwrites this register with the corresponding dword of the LL element.

You can read this register to monitor the transfer progress. However, in some scenarios there is a delay before the controller updates this register. For example, when less than three channels are door belled, this register is only updated after a descriptor finishes (LL mode), or the transfer ends (non-LL mode).

18.6.4.5.3 Starting The DMA Transfer

After you program the DMA controller registers (including writing to the DMA Read Engine Enable or DMA Write Engine Enable register), you start a DMA transfer by writing zero to the Doorbell Number field of the DMA_WRITE_DOORBELL_OFF or DMA_READ_DOORBELL_OFF. You can program and start both a read and a write transfer at the same time. The DMA supports full duplex operation, processing read and write transfers at the same time and in parallel with normal (non-DMA) traffic.

18.6.4.5.4 Detecting the End of The DMA Transfer

Detecting End of Transfer without Errors

The normal end of a DMA transfer is detected by any of the following methods:
■ Local interrupt asserted.
■ Remote interrupt (IMWr) received.
■ Channel status field of the Channel Control 1 register is Stopped, and the DMA Transfer Size register is 0x0.
■ Polling of the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF) or DMA Read Interrupt Status Register (DMA_READ_INT_STATUS_OFF).

Detecting End of Transfer with Errors

The abnormal end of a DMA transfer is detected by any of the following methods:
■ Local interrupt (pin) asserted.
■ Remote interrupt (IMWr) received.
■ Polling of the DMA Write Interrupt Status Register (DMA_WRITE_INT_STATUS_OFF) or DMA Read Interrupt Status Register (DMA_READ_INT_STATUS_OFF).
■ Channel Status field of the Channel Control 1 register is Halted. When the DMA controller detects an error, it forces the DMA to stop issuing requests for the channel. It also sets the channel status field of the Channel Control 1 register to Halted, generates an abort interrupt (if enabled), and sends an abort IMWr (if enabled). The DMA Transfer Size register indicates the remaining number bytes to be transferred, except when there is an AXI write error during a DMA read transfer.
■ Channel Status field of the Channel Control 1 register is Stopped, and the DMA Transfer Size register is not 0x0. You have prematurely stopped this channel as described in "Stopping the DMA Transfer (Software Stop)"on next section

18.6.4.5.5 Stopping the DMA Transfer (Software Stop)

You can manually abort (stop) the DMA transfer by writing the channel number to the Doorbell Number field and writing 1 to the Stop field in DMA_[WRITE|READ]_DOORBELL_OFF. This causes the DMA to:

- Place the channel in a Stopped state. The channel Status field in DMA_CH_CONTROL1_OFF_WRCH_0 is Stopped and the value in DMA_TRANSFER_SIZE_OFF_WRCH_0 will not be 0x0.
- Wait for all outstanding pending transactions.
- Assert the abort interrupt (if it is enabled) in DMA_WRITE_INT_STATUS_OFF.

You might also do this as part of a function level reset (FLR). FLR does not directly affect the DMA transfer so you must manually stop the DMA transfer before initiating an FLR.

18.6.4.6 Programming Examples

This section provides two programming and operation example flows.

18.6.4.6.1 Non-LL Write Transfer

In this example, the IMWr generation is disabled, as the local CPU initiates the DMA transfer. The local CPU is interrupted using the pcie_sys_int interrupt. The SAR is the address of the local memory, and the DAR is the address of the remote memory. Write DMA Transfer is from 0xBEEF_BEE0 to 0xCAFE_CAF0. Table below provides the programming details for this example transfer. The transfer size is 1MB.

Table 18-10 Write DMA Transfer Example

Address 0x380000+	NAME	Value
0x00C	DMA Write Engine Enable You must not write 0 to this register. Even temporarily writing 0 to this register resets the DMA logic.	0x1
0x054	DMA Write Interrupt Mask	0x0
0x200	DMA Channel Control 1 register ■ Local Interrupt Enable (LIE) =1 ■ Remote Interrupt Enable (RIE) =0 ■ AT, RO, NS, TC, Function Number =0	0x04000008
0x208	DMA Transfer Size	0x00100000
0x20C	DMA SAR Low	0xBEEF_BEE0

Address 0x380000+	NAME	Value
0x210	DMA SAR High	0x0000_0000
0x214	DMA DAR Low	0xCAFE_CAF0
0x218	DMA DAR High	0x0000_0000
0x010	DMA Write Doorbell	0x0

18.6.4.6.2 Non-LL Read Transfer

In this example, the local interrupt generation is disabled, as the remote CPU initiates the DMA transfer. The remote CPU is interrupted using an IMWr. The SAR is the address of the remote memory, and the DAR is the address of the local memory. Read DMA Transfer from 0xBEEF_BEE0 to 0xCAFE_CAF0. Table below provides the programming details for this example transfer. The transfer size is 1MB.

Table 18-11 Read DMA Transfer Example

Address 0x380000+	NAME	Value
0x02C	DMA Read Engine Enable You must not write 0 to this register. Even temporarily writing 0 to this register resets the DMA logic.	0x1
0x0CC/0x0D0	DMA Read Done IMWr Address Low and high	IMWr Address #1
0x0D4/0x0D8	DMA Read Abort IMWr Address Low and High	IMWr Address #2
0x0DC	DMA Read Channel 0 IMWr Data	IMWr Data
0x200	DMA Channel Control 1 register ■ Local Interrupt Enable (LIE) =0 ■ Remote Interrupt Enable (RIE) =1 ■ AT, RO, NS, TC, Function Number =0	0x04000010
0x208	DMA Transfer Size	0x00100000
0x20C	DMA SAR Low	0xBEEF_BEE0
0x210	DMA SAR High	0x0000_0000
0x214	DMA DAR Low	0xCAFE_CAF0
0x218	DMA DAR High	0x0000_0000
0x030	DMA Read Doorbell	0x0

18.6.5 PCIe Message Handling

This section describes the processing of messages through the controller. For a proper understanding of messages you should be familiar with Section 2.2.8, "Message Request Rules" of the PCI Express Base Specification, Revision 3.0.

18.6.5.1 Message Generation

These are three methods to generate PCIe Messages:

- Specific MSG interface

  You can use PCIE_CLIENT_MSG_GEN_CON register to generate messages such as:
  Vendor-Defined Message
  Legacy PCI Interrupt Message
  PME_Turn_Off message
  Unlock message
  LTR Message
  OBFF Message
  Refer to register description for more details.

- AXI bridge

  In this method, you should program the PCIE_CLIENT_AXI_SLV_AWMISC_HDR PCIE_CLIENT_AXI_SLV_AWMISC_HDR3 and PCIE_CLIENT_AXI_SLV_AWMISC_HDR4 registers to set these parameters:
  slv_awmisc_info [4:0] =MSG

slv_awmisc_info [20:13] = message code
slv_awmisc_tag [5:0] = tag
slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
Then you can send zero length memory write (slv_awstrb=0) to generate the message. You must not program registers mentioned above when there are normal transfers pending on AXI slave interface. And should set these registers in normal value when you want to send MWr TLP. This method is not recommend because of these limitations.

- AXI bridge and iATU

Program related client register fields as follows:
slv_awmisc_info[4:0] =MEM
slv_awmisc_info_hdr_[3|4]dw = 3rd and 4th TLP header DWORD
Then iATU needs to be configured to to translate MWr to Msg TLPs. Refer to "Address Translation" for more details. This method is not recommend because that it needs additional iATU resources.

18.6.5.2 Message Reception

PCIe controller use pcie_msg_int interrupt to indicate the reception of PCIe Message. Application can poll to PCIE_CLIENT_INTR_STATUS_MSG_RX register to check the status of Message reception. Refer to register information for details.

18.6.6 PCIe Power Management

18.6.6.1 Overview

The controller supports two categories of PM operations to control the device state (D-state) and link state. For a proper understanding of PCIe Power management you should be familiar with Section 5, "Power Management" of the PCI Express Base Specification, Revision 3.0.

Software PCI Compatible PM (PCI-PM)

- D-state PM of Function. The host software can direct the function to enter any of the D1, D2, or D3 low-power states. It does this by writing to the Power Management Control and Status Register (PMCSR) in the PCI-PM capability structure.
- D-state PM of Link. Link states are not visible to PCI-PM legacy compatible software, and are derived from the power management D-states of the components connected to that link. The action of changing the D-state in the PMCSR indirectly causes a change in the link power state. The L1 state is entered whenever all functions of a USP on a link are programmed to a non-D0 state. The entry into L2 and L3 states is initiated by the DSP.

PCIe PM Mechanisms

- Active State PM (ASPM).When the USP is in L0 and detects idleness on the link for a specific amount of time, it automatically transitions the link to the L0s or L1 (optional) power state.
- L1 Substates. This is an optional PCIe feature that enables components on a link to further reduce idle power consumption while the link is in L1, including almost complete removal of power for the high speed PHY circuits.

18.6.6.2 L0s Operation

L0s is a low-power state enabled by ASPM. ASPM controls entry into L0s for the transmitter. The remote device controls entry into L0s for the receiver.

18.6.6.2.1 L0s Entry

All of these condition must be met:

■ ASPM L0s is enabled through the ASPM Control field in the Link Control register.

■ L0s entry conditions as defined in Section 5.4.1.1.1, "Entry into the L0s State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L0S_ENTRANCE_LATENCY field in ACK_F_ASPM_CTRL_OFF).

■ No higher stage of power-down requested.

18.6.6.2.2 L0s Exit

Any of these condition can be met:

■ A DLLP or TLP is pending to be sent.

■ L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, are satisfied.

■ PCIe link partner requests to enter into link recovery.

18.6.6.3 L1 Operation (Non-substates)

The following topic will be discussed in this section: L1 (ASPM/PM) Entry and Exit Conditions

and L1 Clock PM (L1 with REFCLK removal/PLL Off) Entry and Exit Conditions.
18.6.6.3.1 L1 (ASPM/PM) Entry

L1 is a low-power state enabled either by ASPM (L1-ASPM) or by the software changing the D-state (L1-PM). The L1 state is a bi-directional link low-power state and both link partners must negotiate to go to this state.
The L1-ASPM entry negotiation handshake uses PM_Active_State_Request_L1 DLLPs, PM_Request_Ack DLLPs, and PM_Active_State_Nak MSG TLPs. Refer to PCIe Basic Specification for more information.
There are three scenarios that cause the controller to enter L1 under ASPM conditions.
Scenario 1: L1 Idle Timeout In L0s
All of these condition must be met in the USP:
■ ASPM L1 and L0s are enabled through the ASPM Control field in the Link Control register.
■ The ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to '0' and the link state is L0s for both link partners, or the ENTER_ASPMfield of ACK_F_ASPM_CTRL_OFFis set to '1'.
■ L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
■ No higher stage of power-down requested.
■ Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
■ There are no in-progress transactions in the controller
■ There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
■ There are no pending DMA transfers.
Scenario 2: L1 Idle Timeout In L0
All of these condition must be met in the USP:
■ ASPM L1 is enabled and L0s is not enabled through the ASPM Control field in the Link Control register.
■ Link state is L0.
■ L1 entry conditions as defined in Section 5.4.1.2.1, "Entry into the L1 State" of the PCI Express Base Specification, Revision 3.0, exist for a duration of time (determined by the L1_ENTRANCE_LATENCYfield in ACK_F_ASPM_CTRL_OFF).
■ No higher stage of power down-requested.
■ Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
■ There are no in-progress transactions in the controller.
■ There are no pending requests at the AXI slave interface, that is, slv_a*valid must be 0.
■ There are no pending DMA transfers.
Scenario 3: Application Controlled (USP only)
All of these condition must be met in the USP:
■ ASPM L1 is enabled through the ASPM Control field in the Link Control register.
■ Your application write 1 to the app_req_entr_l1 field in PCIE_CLIENT_POWER_CON register.
■ Your USP application is not asserting the app_xfer_pending field in PCIE_CLIENT_POWER_CON register.
■ There are no in-progress transactions in the controller.
■ There are no pending requests at the AXI slave interface, that is, slv_a*validmust be 0.
■ There are no pending DMA transfers.
L1-PM Entry
The power management state of a link is determined bythe D-state of theUSP.When you change the device state of the USP to D1, D2, or D3hot by writing to the PMCSR, the controller must initiate a link state transition to L1.
An USP application asserting the app_xfer_pending field does not prevent L1-PM entry, but will cause immediate exit from L1-PM.
18.6.6.3.2 L1-PM/L1-ASPM Exit
Any of these condition are met:

■ A DLLP or TLP is pending to be sent.
■ Your application asserts the app_req_exit_l1 field.
■ Link partner is requesting exit from L1.
■ Your application asserts the app_xfer_pending field.
■ Your application asserts the app_pm_xmt_pme field.
When the USP is programmed with capability to support PME; it sends a PME message to the RC which calls the PM software to transition the USP to the D0 state. Therefore, you should only use app_pm_xmt_pme for L1-PM exit.
■ PM software (RC) requests a higher stage of power-down by writing to the PMCSR in the USP.
■ Your application (USP) requests transmission of VDM, MSI/MSIX, or LTR message. Legacy interrupt is not included.
■ Your application (DSP) requests transmission of Unlock message.
■ Your application is requesting to send traffic by asserting or slv_a*valid.
■ Your application doorbells a DMA read or write channel, or DMA controller is requesting data.
■ Your application (DSP) initiates link disable, or link retrain (by setting PCIE_CAP_LINK_DISABLE or PCIE_CAP_RETRAIN_LINK field in LINK_CONTROL_LINK_STATUS_REG to 1).
■ Your application (DSP) initiates hot reset by either:

- ❑ setting RESET_ASSERT field in PORT_LINK_CTRL_OFF to 1, or
- ❑ setting SBR field in BRIDGE_CTRL_INT_PIN_INT_LINE_REG to 1, or
- ❑ toggling app_init_rst field in PCIE_CLIENT_GENERAL_CON.

■ Your application requests a speed change (by setting DIRECT_SPEED_CHANGE field in GEN2_CTRL_OFF to 1).
■ Your application requests link width change (by setting DIRECT_LINK_WIDTH_CHANGE field in MULTI_LANE_CONTROL_OFF is set to 1).

18.6.6.3.3 L1 Clock PM

For an USP, host software uses the Enable Clock Power Management bit in the Link Control register to enable this feature. For a DSP, this register bit is hard coded to '0' and cannot be used to control this behavior. Your application can use the app_clk_pm_en input to dynamically control whether to execute L1 with or without Clock PM.
■ The Support Clock Power Management bit in the Link Capabilities register must be set. For downstream ports it is hardcoded to 0, for upstream ports it can be accessed through the DBI.
■ The Enable Clock Power Management bit in the Link Control register must be set.
■ You must set the app_clk_pm_en field to 1. The controller only samples app_clk_pm_en when L1 is entered.
L1 with Clock PM and L1 substates work orthogonal to each other. L1 with Clock PM uses the mac_phy_pclkreq_n[0]signaling, and L1 substates uses the mac_phy_pclkreq_n[1]signaling. However, L1 substates takes precedence over Clock PM within the cores PM state machine.

18.6.6.4 L1 Substate

The L1 substates are applicable in both the ASPM and PCI-PM L1 link states. L1 substates management utilizes a per-link sideband signal called CLKREQ#.
■ During L1 substates it is assumed that core_clk is turned off and that aux_clk is active. It is required that your application switches aux_clk to a low frequency free running clock on entry into L1.
■ The controller uses aux_clk for counting time during L1 substates. You must program the frequency of this clock into the L1_SUBSTATES_OFF register with a value in the range 1...1000MHz to count real time. Frequencies lower than 1 MHz are possible, but with a loss of accuracy in the time counted.
■ When the electrical idle detection circuitry is disabled it is assumed that the PHY holds the signal phy_mac_rxelecidle to 1.
After the link has entered L1 through the normal L1 negotiation, the USP can initiate the

sequence for entering the target L1 substate (L1.1 or L1.2) by tri-stating its CLKREQ# output buffer. The entry sequence can only proceed if the DSP is also tri-stating its CLKREQ# output buffer, resulting in the bidirectional CLKREQ# signal being pulled up to 1. Otherwise CLKREQ# will remain asserted at 0 and the link state will stay in L1. The exit sequence can be initiated by either ports by asserting CLKREQ# to 0. For each port there are two cases to consider, the first where the exit is initiated locally, the second where the exit is initiated remotely. L1 substates management utilizes a per-link sideband signal called CLKREQ#.

18.6.6.4.1 L1 Substates Software Control

When the controller enters L1, the target L1 substate depends on several programming bits:

- PM Control/Status Register
  - USP: The current D-state
  - DSP: The DLLP type that was used by USP to request L1
- L1 Substates Control 1 Register
  - ASPM PM L1.1 Enabled
  - ASPM PM L1.2 Enabled
  - PCI PM L1.1 Enabled
  - PCI PM L1.2 Enabled

After the USP controller enters L1, it uses the D-state of the device to determine if L1 was entered in ASPM mode or PCI-PM mode.

After the DSP controller enters L1, it uses the USPs DLLPL1 request type to determine if L1 was entered in ASPM mode or PCI-PM mode. The next tables shows the target L1 substate as a function of the relevant programming bits.

Table 18-12 Target L1 Substate as a Function of Software Controls (USP)

D-State	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
!D0	-	-	-	0	0	L1
!D0	-	-	-	1	0	L1.1
!D0	-	-	-	-	1	L1.2
D0	0	0	-	-	-	L1
D0	1	0	-	-	-	L1.1
D0	0	1	0	-	-	L1
D0	1	1	0	-	-	L1.1
D0	-	1	1	-	-	L1.2

Table 18-13 Target L1 Substate as a Function of Software Controls (DSP)

DLLP Receive	ASPM L1.1 Enabled	ASPM L1.2 Enabled	LTR >= Threshold	PCI PM L1.1 Enabled	PCI PM L1.2 Enabled	Target L1 Substate
PM_Enter_L1	-	-	-	0	0	L1
	-	-	-	1	0	L1.1
	-	-	-	-	1	L1.2
PM_Active_State_Request_L1	0	0	-	-	-	L1
	1	0	-	-	-	L1.1
	0	1	0	-	-	L1
	1	1	0	-	-	L1.1
	-	1	1	-	-	L1.2

The Reported LTR is the maximum of the snoop/no snoop latency values embedded in LTR messages transmitted by the upstream ports or received by the downstream port. The controller stores these values in the port logic LTR Latency Register (LTR_LATENCY_OFF). When the requirement bit in the message is 0, the latency value is considered infinite (that

is, the check with the threshold always pass).

18.6.6.4.2 L1 Substates Entry and Exit

PCIe link entered L1 substate automatically if related enable bit is set and LTSSM already in L1 state, refer to section L1 Substates Software Control for details.

L1 substates Exit can be triggered locally or Remotely. For locally initiated exit, refer to section L1-PM/L1-ASPM Exit. Remotely initiated exit begin when CLKREQ# is asserted by remote PCIe partner.

18.6.6.5 L2 and L3 Power Down Entry and Exit

L2/L3 entry is initiated after the RC calls power management software to initiate the removal of power and clocks. USPs of devices in D0, D1, D2, and D3hot must respond to the receipt of a PME_Turn_Off MSG TLP by transmitting a PME_TO_Ack MSG TLP. The device must then request a link transition to L2/L3_Ready. L2/L3_Ready is a bi-directional link power down state. If your application is not ready to be shut-down, it must keep the app_ready_entr_l23 field de-asserted.

L2/L3 Entry

All of these condition must be met:

■ PME_Turn_Off/PME_TO_Ack handshake has been completed.

■ Your USP application is ready to be turned off; app_ready_entr_l23=1.

■ After sending the PME_TO_Ack, the USP initiates the L2/L3 Ready transition protocol by sending the PM_Enter_L23 DLLP. The RC responds with the PM_Request_Ack.

L2/L3 Exit

Any of these condition can be met:

■ When the USP is programmed with capability to support PME, your application can assert the apps_pm_xmt_pme field to request the controller to wake up. The USP then sends a PM_PME MSG TLP to the RC which calls the PM software to transition the USP out of the D3 state.

■ Device is programmed with capability to support PME and your application requests the controller to wake up by triggering a native hot-plug event.

■ Link partner is requesting exit from L2/L3.

18.6.6.6 Dynamic Power Allocation (DPA)

The DPA capability enables software to actively manage and optimize function power usage when in the D0 state. DPA is not applicable to power states D1-D3.

For details on how your application interacts with the controller, see the description of the dpa_sub_upd_int field in PCIE_CLIENT_INTR_STATUS_MISC register.

18.6.7 PCIe Interrupt

The PCIe provides six types of interrupt to system interrupt controller. They can be divided into MSI/MSI-X, PCIe Error interrupt, PCIe Message Receive interrupt, PCIe Legacy interrupt, PCIe System interrupt and PCIe Power Management Interrupt. When operating as RC, the PCIe is capable of handling both MSI/MSI-X and legacy interrupts. This is because when operating as RC it should be able to service both PCIe end points as well as legacy endpoints. It is capable of generating MSI or Legacy interrupt if the PCIe is configured as EP. Notes that PCIe EP component can't generate both Legacy and MSI/MSI-X interrupt. It is either one or the other. The interrupt type an EP generates is configured during configuration time.

Interrupt status and mask bits are located in client register group, some interrupts are handle by client register directly, but some interrupts are generated by events deep into controller and software should clear the root cause to serve the interrupt events. For more information, refer to the register description.

Table 18-14 PCIe Interrupt Table

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
118	PCIe System Interrupt	PHY link up interrupt	RC & EP
		DLL link up interrupt	RC & EP
		Link down reset request interrupt	RC & EP
		Slot status change interrupt	RC

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
		Hot plug interrupt	RC
		Link autonomous bandwidth interrupt	RC
		Bandwidth Management Interrupt	RC
		EDMA write channel interrupt	RC & EP
		EDMA read channel interrupt	RC & EP
		DPA update interrupt	EP
		Resizable BAR update interrupt	EP
119	PCIe Legacy interrupt	INTA received interrupt	RC
		INTB received interrupt	RC
		INTC received interrupt	RC
		INTD received interrupt	RC
		INTA sent interrupt	EP
		INTB sent interrupt	EP
		INTC sent interrupt	EP
		INTD sent interrupt	EP
120	PCIe message received interrupt	Vendor message received interrupt	RC & EP
		Unlock message received interrupt	EP
		LTR message received interrupt	RC
		PME status Interrupt	RC
		PM_PME message received interrupt	RC
		PME_TO_Ack message received interrupt	RC
		PME Turnoff message received interrupt	EP
		'IDLE' OBFF message received interrupt	RC
		'OBFF' OBFF message received interrupt	RC
		'CPU Active' OBFF message received interrupt	RC
121	PCIe Error interrupt	Root Error Status interrupt	RC
		Completion TLP Rx timeout interrupt	RC & EP
		Completion TLP Tx timeout interrupt	RC & EP
		ERR_COR message sent interrupt	EP
		ERR_NONFATAL message sent interrupt	EP
		ERR_FATAL message sent interrupt	EP
		ERR_COR message received	RC
		ERR_NONFATAL message received	RC
		ERR_FATAL message received	RC
		Receive FIFO overflowed interrupt	RC & EP
136	PCIe Power Management interrupt	L1 substate entry interrupt	RC & EP
		L1 entry interrupt	RC & EP
		L2 entry interrupt	RC & EP
		L0s entry interrupt	RC & EP
		L1 substate exit interrupt	RC & EP
		L1 exit interrupt	RC & EP
		L2 exit interrupt	RC & EP
		L0s exit interrupt	RC & EP

System Interrupt Event ID	Interrupt description (level 1)	Interrupt subset (level 2)	Support mode
		D-state changed interrupt	EP
XXX	MSI/MSI-X	message signaled interrupt	RC service and EP initiate

18.7 PCIe Appendix

18.7.1 LTSSM Code

S_DETECT_QUIET	6'h00
S_DETECT_ACT	6'h01
S_POLL_ACTIVE	6'h02
S_POLL_COMPLIANCE	6'h03
S_POLL_CONFIG	6'h04
S_PRE_DETECT_QUIET	6'h05
S_DETECT_WAIT	6'h06
S_CFG_LINKWD_START	6'h07
S_CFG_LINKWD_ACEPT	6'h08
S_CFG_LANENUM_WAIT	6'h09
S_CFG_LANENUM_ACEPT	6'h0A
S_CFG_COMPLETE	6'h0B
S_CFG_IDLE	6'h0C
S_RCVRY_LOCK	6'h0D
S_RCVRY_SPEED	6'h0E
S_RCVRY_RCVRCFG	6'h0F
S_RCVRY_IDLE	6'h10
S_RCVRY_EQ0	6'h20
S_RCVRY_EQ1	6'h21
S_RCVRY_EQ2	6'h22
S_RCVRY_EQ3	6'h23
S_L0	6'h11
S_L0S	6'h12
S_L123_SEND_EIDLE	6'h13
S_L1_IDLE	6'h14
S_L2_IDLE	6'h15
S_L2_WAKE	6'h16
S_DISABLED_ENTRY	6'h17
S_DISABLED_IDLE	6'h18
S_DISABLED	6'h19
S_LPBK_ENTRY	6'h1A
S_LPBK_ACTIVE	6'h1B
S_LPBK_EXIT	6'h1C
S_LPBK_EXIT_TIMEOUT	6'h1D
S_HOT_RESET_ENTRY	6'h1E
S_HOT_RESET	6'h1F

Chapter 19 SATA Host

19.1 Overview

Sata Host implements the Serial Advanced Technology Attachment(SATA)storage interface for physical storage devices.

Sata Host supports the following features:

- Include 3 ports, and each port can connect up to 5 devices using PM switching
- SATA 1.5Gb/s,SATA 3.0Gb/s,SATA 6.0Gb/s speeds
- eSATA
- Compliant with Serial ATA 3.3 specifications
- Compliant with AHCI Revision 1.3.1
- OOB signaling detection and generation
- Digital support of Mechanical presence switch and cold presence detect
- Activity LED support
- Digital support of device hot-plugging
- Output port to indicate speed that is negotiated after COMRESET for power optimization
- Memory Data Protection(ECC) and Error Correction(ECC)
- Memory Data Protection Diagnostic Error Injection
- SATA 1.5Gb/s,SATA 3.0Gb/s,and SATA 6.0Gb/s speed negotiation
- Asynchronous signal recovery, including retry polling
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Hardware-assisted Native Command Queuing for up to 32 entries
- Port Multiplier with FIS-based switching
- Disabling RX and TX Data clocks during power down modes
- Any sector size
- AXI interface used for configuration only support single
- AXI interface used to fetch data from memory

19.2 Block Diagram

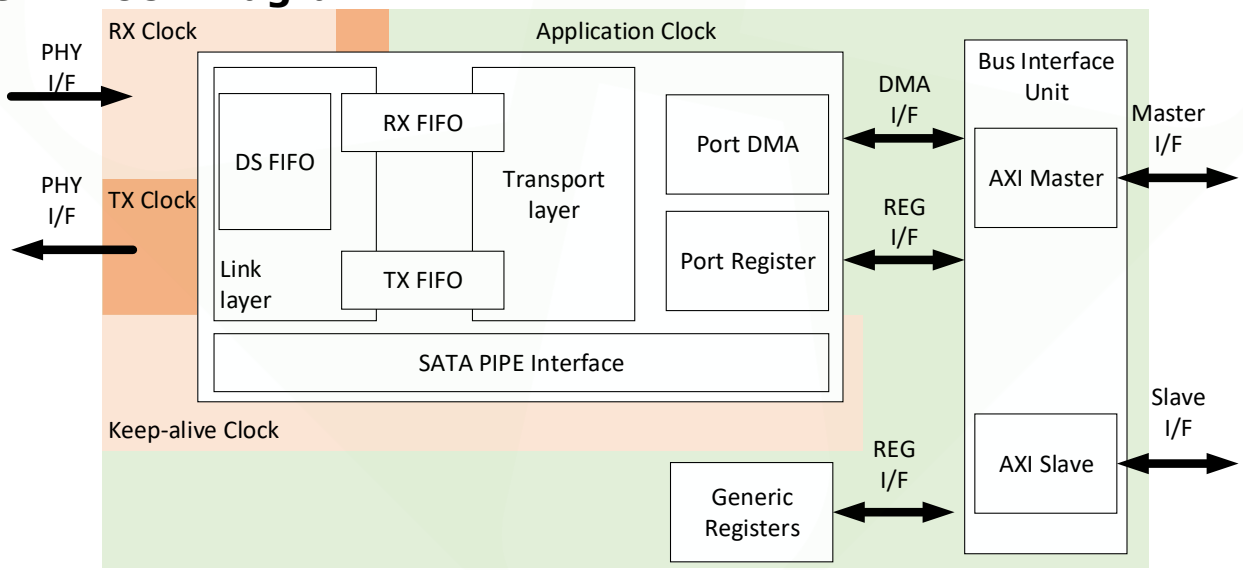


Fig. 19-1 SATA host Architecture

19.3 Function Description

19.3.1 Bus Interface Unit(BIU)

The Bus Interface Unit provides two interfaces:

AXI Master - This interface enables the SATA AHCI DMA engine to read and write to an AXI slave connected to AXI BIU.

AXI Slave - This interface enables an AXI master to read an write through the AXI BIU to the SATA AHCI registers.

19.3.2 Generic Registers(GCSR)

This module implements all global registers and provides the following functions:

- Generic configuration and control
- Global interrupt support
- BIST operation

19.3.3 Port Registers(PCSR)

The port registers module implements all Port-specific registers:

- Command list and FIS Based address
- Interrupt status/ enable
- Port command / status
- Task file data/signature /serial ATA
- DMA status/control

19.3.4 Port DMA(PDMA)

This module performs the following functions:

- Monitors commands posted by system software using the CI register
- Control data transfer between the Transport layer FIFOs and system memory using Physical Region Descriptor Table(PRDT)
- Transfers non-Data FISes received from the device to system memory using Received FIS Structure

Most of the communication between the PDMA and software is done using two system memory descriptors that are constructed by software prior to initiating the transfer: FIS descriptor, which contains FISes received from that device; and the command list, which contains a list of 1 to 32 commands available for Port to execute and the pointers for data transfers. Some additional communication is done by registers located in the GCSR and PCSR modules.

System memory structures are described in the SATA AHCI specification and are not repeated in this document.

The PDMA module operates in the application clock(aclk) domain.

19.3.5 Port Transport layer

The transport layer block provides FIS reception and transmission functions of the SATA transport layer. It operates in two clock domains: transmit and application. During reception, the transport layer receives a new FIS from the link layer through the RX FIFO, decodes the FIS type, and instructs the PDMA to route the FIS payload data to the appropriate location in system memory. During transmission, the transport layer instructs the PDMA to construct the appropriate FIS, and then passes it to the link layer through the TX FIFO. The transport layer block receives all the PHY/Link errors from the link layer, detects transport errors and passes them to the PCSR for setting the corresponding error bits.

The transport layer processes one FIS at time on the transmit side, meaning only one FIS is allowed in the TX FIFO at a time. On the receive side, RX FIFO can potentially contain more than one FIS at a time. For example, when the device transmits several DMA data FISes back-to-back with minimal delay, the RX FIFO still has the previous Data FIS while the next FIS is being received. The transport layer also contains a small internal eight-DWORD RX FIFO1 that is used for non-data FISes and FIS "End Status."

19.3.6 Port Link layer

This module optional OOB signaling, system initialization, speed negotiation, frame negotiation and arbitration, envelope framing/de-framing, CRC calculating, insertion and checking, flow control, frame acknowledgement and status reporting, data scrambling/de-scrambling for EMI reduction, repeat primitive data transmission and reception handling, ALIGN primitive detection, dropping and data alignment and power management.

19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as

follows.

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SATA_CAP	0x0000	W	0x6737FF85	HBA Capabilities Register
SATA_GHC	0x0004	W	0x80000000	Global HBA Control Register
SATA_GIS	0x0008	W	0x00000000	Interrupt Status Register
SATA_PI	0x000C	W	0x00000000	Ports Implemented Register
SATA_VS	0x0010	W	0x00010300	AHCI Version Register
SATA_CCC_CTL	0x0014	W	0x00010108	Command Completion Coalescing Control
SATA_CCC_PORTS	0x0018	W	0x00000000	Command Completion Coalescing Ports
SATA_CAP2	0x0024	W	0x00000004	HBA Capabilities Extended Register
SATA_BISTAFR	0x00A0	W	0x00000000	BIST Activate FIS Register
SATA_MEMEDRXFERRCNT	0x00A0	W	0x00000000	RX FIFO RAM Address Parity Error Count Register
SATA_BISTCR	0x00A4	W	0x00004700	BIST Control Register
SATA_MEMEDRXFERRDATA	0x00A4	W	0x00000000	RX FIFO RAM Data ECC Error Location and Syndrome Register
SATA_BISTFCTR	0x00A8	W	0x00000000	BIST FIS Count Register
SATA_MEMEDTXFERRCNT	0x00A8	W	0x00000000	ECC TX FIFO RAM Error Count Register
SATA_BISTSR	0x00AC	W	0x00000000	BIST Status Register
SATA_MEMEDTXFERRDATA	0x00AC	W	0x00000000	TX FIFO RAM Data ECC Error Location and Syndrome Register
SATA_BISTDECR	0x00B0	W	0x00000000	BIST DWORD Error Count Register
SATA_MEMEDFBSERRCNT	0x00B0	W	0x00000000	ECC TX FIFO RAM Error Count Register
SATA_MEMEDFBSERRDATA	0x00B4	W	0x00000000	FBS RAM Data ECC Error Location and Syndrome Register
SATA_MEMEDERRINJ	0x00B8	W	0x00000000	ECC Error Detection Status and Error Injection Register
SATA_OOBR	0x00BC	W	0x04070C15	OOB Register
SATA_MEMEDRXFERRDATAU	0x00BC	W	0x00000000	Rx FIFO RAM Data Parity Error Syndrome Upper Bits Register
SATA_MEMEDTXFERRDATAU	0x00C0	W	0x00000000	Tx FIFO RAM Data Parity Error Syndrome Upper Bits Register
SATA_DIAGNR3	0x00C4	W	0x00000000	DIAGNR3
SATA_MEMEDFBSERRDATAU	0x00C4	W	0x00000000	FBS RAM Data Parity Error Syndrome Upper Bits Register
SATA_GPARAM3	0x00DC	W	0x0000004D	Global Parameter 3 Register
SATA_TIMER1MS	0x00E0	W	0x000493E0	Timer 1-ms Register
SATA_MEMDPCR	0x00E4	W	0x00000000	ECC/Parity Global Control Register
SATA_GPARAM1R	0x00E8	W	0x98000C00	Global Parameter 1 Register
SATA_GPARAM2R	0x00EC	W	0x00000832	Global Parameter 2 Register
SATA_TESTR	0x00F4	W	0x00000000	Test Register
SATA_IDR	0x00FC	W	0x00000000	ID Register
SATA_CLB	0x0100	W	0x00000000	Port Command List Base Address Register
SATA_FB	0x0108	W	0x00000000	Port FIS Base Address Register
SATA_PIS	0x0110	W	0x00000000	Port Interrupt Status Register
SATA_PIE	0x0114	W	0x00000000	Port Interrupt Enable Register
SATA_CMD	0x0118	W	0x00000000	Port Command Register

Name	Offset	Size	Reset Value	Description
SATA_TFD	0x0120	W	0x00000000	Port Task File Data Register
SATA_SIG	0x0124	W	0x00000000	Port Signature Register
SATA_SSTS	0x0128	W	0x00000000	Port Serial ATA Status (SStatus) Register
SATA_SCTL	0x012C	W	0x00000000	Port Serial ATA Control Register
SATA_SERR	0x0130	W	0x00000000	Port Serial ATA Error Register
SATA_SACT	0x0134	W	0x00000000	Port Serial ATA Active Register
SATA_CI	0x0138	W	0x00000000	Port Command Issue Register
SATA_SNTF	0x013C	W	0x00000000	Port Serial ATA Notification Register
SATA_FBS	0x0140	W	0x00000000	Port FIS-Based Switching Control Register
SATA_DMACR	0x0170	W	0x00000000	Port DMA Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

19.4.3 Detail Registers Description

SATA_CAP

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	s64a Tie 0, do not supports 64-bit addressable data structures.
30	RO	0x1	sncq Supports SATA native command queuing by handing DMA Setup FIS natively.
29	RO	0x1	ssntf Supports PnSNTF(SNotification)register and its associated functionality.
28	RW	0x0	smps This bit is set by the system firmware/BIOS when platform supports mechanical presence for hot plug operation.
27	RW	0x0	sss Support for staggered devices' spin-up.
26	RO	0x1	salp Tie 1, supports auto-generating Link Layer requests to the PARTIAL or SLUMBER power management states when there are no commands to process.
25	RO	0x1	sal Tie 1, supports activity indication using signal Pn_act_led.
24	RO	0x1	sclo Tie1 , supports the PnCMA.CLO bit functionality for Port Multiplier devices' enumeration.
23:20	RO	0x3	iss Supports SATA 1.5Gb/s,SATA 3Gb/s,SATA 6Gb/s interface speeds.
19	RO	0x0	reserved
18	RO	0x1	sam Tie 1, support AHCI mode only and does not supports legacy, task-file based register interface.
17	RO	0x1	spm Tie 1, supports command-based switching Port Multiplier on any of its ports.
16	RO	0x1	fbss FIS-Based Switching supported.

Bit	Attr	Reset Value	Description
15	RO	0x1	pmd Supports multiple DRQ block data transfer for the PIO command protocol.
14	RO	0x1	ssc Supports transitions to the interface SLUMBER power management state.
13	RO	0x1	psc Supports transitions to the interface PARTIAL power management state.
12:8	RO	0x1f	ncs Supports 32 command slots per Port.
7	RO	0x1	cccs Command Completion Coalescing Supported.
6	RO	0x0	ems Does not support enclosure management.
5	RO	0x0	sxs Supports External SATA.
4:0	RO	0x05	np Supports 5 ports.

SATA_GHC

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x1	ae This bit is always set.
30:2	RO	0x00000000	reserved
1	RW	0x0	ie This global bit enables interrupts. When cleared, all interrupt sources from all the ports are disabled. When set, interrupts are enabled and interrupt event caused intrq assertion.
0	WO	0x0	hr When set by the software, this bit causes an internal Global reset. All state machines that relate to data transfers and queuing return to and idle state, and all the ports are re-initialized by sending COMRESET when staggered spin-up is not supported. When staggered spin-up is supported, then the software must spin-up each port after this reset has complete.

SATA_GIS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ips When set, this bit indicates that the corresponding Ports or Command Completion Coalescing logic has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the PnIS bits and enabled by the PnIE or CCC interrupt is generated. Set bits are cleared by the software writing 1 to all bits to clear.

SATA_PI

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	pi This register is bit significant. 1: The corresponding Port is available for the software to use. 0: The Port is not available for the software to use.

SATA_VS

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	mjr Indicates that the major AHCI version is 1.
15:0	RO	0x0300	mnr Indicates that the monor AHCI version is 30 or 31.

SATA_CCC_CTL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	tv This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC.
15:8	RW	0x01	cc This field specifies the number of command completions that are necessary to cause a CCC interrupt.
7:3	RO	0x01	intr_int This field specifies the interrupt used by the ccc feature, using the number of ports configured for the core.
2:1	RO	0x0	reserved
0	RW	0x0	en The options for this field are: 0: CCC feature is disabled and no CCC interrupts are generated. 1: CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions.

SATA_CCC_PORTS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	prt This field is bit significant. Each bit corresponds to a particular Port, where bit 0 corresponds to Port0.The options for this field are: 1: the corresponding Port is part of the CCC feature. 0: the corresponding Port is not part of the CCC feature. Bits set in this register must also have the corresponding bit set in the PI (Ports Implemented Register). This field is reset on Global reset (GHC.HR=1).

SATA_CAP2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x1	apst Supports automatic Partial to Slumber transaction.
1	RO	0x0	nvmp Does not support NVMHCI.

Bit	Attr	Reset Value	Description
0	RO	0x0	bph Tie0, does not support BOH.

SATA_BISTAFR

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	ncp Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit only mode (BISTAFR.PD=0xC0 or 0xE0): 0xF1: Low transition density pattern (LTDP) 0xB5: High transition density pattern (HTDP) 0xAB: Low frequency spectral component pattern (LFSCP) 0x7F: Simultaneous switching outputs pattern (SSOP) 0x78: Mid frequency test pattern (MFTP) 0x4A: High frequency test pattern (HFTP) 0x7E: Low frequency test pattern (LFTP) When none of these values is decoded, the Lone bit pattern (LBP) is transmitted by default.
7:0	RO	0x00	pd Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the DWC_ahsata in one of the following BIST modes: 0x10: Far-end retimed 0x08: Far-end analog (when PHY supports this mode) 0xC0: Far-end transmit only 0xE0: Far-end transmit only with scrambler bypassed All other values should not be used by the device, otherwise, the FIS is negatively acknowledged with R_ERRp. For far-end transmit only modes BISTAFR.NCP field contains the required data pattern.

SATA_MEMEDRXFERRCNT

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	mem_rxf_corr_err_cnt RX FIFO Corrected RAM Data Error Count.
7:0	RO	0x00	mem_rxf_uncorr_err_cnt RX FIFO Uncorrected RAM Data Error Count.

SATA_BISTCR

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	old_phy_ready Old phy_ready.

Bit	Attr	Reset Value	Description
24	RO	0x0	late_phy_ready When set, this bit changes monitoring of phy_ready to be the "OR" of phy_ready or phy_rx_data_vld so that a "late arriving", or even "never asserting" phy_ready. This requires that phy_rx_data_vld does not become valid until after the PHY has locked onto post OOB incoming ALIGNs, and the ALIGNs are valid from the PHY. This will not work if phy_rx_data_vld is asserted during OOB data bursts. This behavior is intended for PHYs that assert phy_ready late, but will also work if phy_ready never asserts or is not present.
23:21	RO	0x0	reserved
20	WO	0x0	ferlb When set, this bit is used to put the hardware Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.
19	RO	0x0	reserved
18	WO	0x0	txo This bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value when the device is disconnected.
17	WO	0x0	cntclr This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1: Clear BISTFCTR, BISTSR, and BISTDECR registers.
16	WO	0x0	nearlb This bit places the Port PHY into near-end analog loopback mode. This field is one-shot type and reads returns 0. 1: Near-end analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.
15	RW	0x0	llb When set, masks out phy_sig_det from the OOB Detector in BIST Loopback Mode, and the only way to exit BIST Loopback mode is to clear the register bit (requires access to the Device AMBA register interface), then issue COMRESET or receive COMINIT as normal. Alternately, a power on reset will automatically clear the BIST Loopback Mode register bit.
14	RO	0x1	qphyinit When set, this bit enables quick PHY initialization feature. The Link does not require any ALIGNs to transition from OOB to normal operation.
13:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x7	llc This field controls the Port Link Layer functions: scrambler, de-scrambler, and repeat primitive drop. Note the different meanings for normal and BIST modes of operation: Bit 8 - SCRAM The options for this field are: 0: Scrambler disabled in normal mode, enabled in BIST mode 1: Scrambler enabled in normal mode, disabled in BIST mode Bit 9 - DESCRAM The options for this field are: 0: Descrambler disabled in normal mode, enabled in BIST mode 1: Descrambler enabled in normal mode, disabled in BIST mode Bit 10 - RPD The options for this field are: 0: Repeat primitive drop function disabled in normal mode, NA in BIST mode. 1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The SCRAM bit is cleared (enabled) by the Port when the Port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=0xC0). In normal mode, the functions scrambler, descrambler, or RPD can be changed only during Port reset (PnSCTL.DET=0x1).
7	RO	0x0	reserved
6	RW	0x0	erren This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding PnSERR bits. The options for this field are: 0: Filter errors outside the FIS, allow errors inside the FIS; 1: Allow errors outside or inside the FIS.
5	RW	0x0	flip This bit is used to change disparity of the current test pattern to the opposite every time its state is changed by the software.
4	RW	0x0	pv This bit is used to select either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP patterns. The options for this field are: 0: Short pattern version, 1: Long pattern version.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	pattern This field defines one of the following SATA-compliant patterns for far-end retimed/far-end analog/near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit. The options for this field are: 0x0: Simultaneous switching outputs pattern (SSOP) 0x1: High transition density pattern (HTDP) 0x2: Low transition density pattern (LTDP) 0x3: Low frequency spectral component pattern (LFSCP) 0x4: Composite pattern (COMP) 0x5: Lone bit pattern (LBP) 0x6: Mid frequency test pattern (MFTP) 0x7: High frequency test pattern (HFTP) 0x8: Low frequency test pattern (LFTP) All other values are reserved and should not be used. If the value is none of the listed previously, Composite pattern (COMP) is transmitted by default.

SATA_MEMEDRXFERRDATA

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_rxf_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome width excess the range of the filed MEMEDRXFERRDATA.mem_rxf_err_synd, extra bits is logged in another register MEMEDRXFERRDATAU.mem_rxf_err_synd_u.
11:0	RO	0x000	mem_rxf_err_addr RX FIFO RAM Data Ecc/Parity Error Location This filed logs the error location (the address of which the RAM data Ecc/Parity error detected).

SATA_BISTFCTR

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	count Received BIST FIS Count.

SATA_MEMEDTXFERRCNT

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	mem_txf_corr_err_cnt TX FIFO Corrected RAM Data Error Count.
7:0	RO	0x00	mem_txf_uncorr_err_cnt TX FIFO Uncorrected RAM Data Error Coun.

SATA_BISTSR

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

Bit	Attr	Reset Value	Description
23:16	RO	0x00	brsterr This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected. The BRSTERR value does not roll over and freezes at FFh.
15:0	RO	0x0000	framerr This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received. The FRAMERR value does not roll over and freezes at FFFFh.

SATA_MEMEDTXFERRDATA

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_txf_err_synd This field logs the error syndrome of the RAM Data Ecc error, if the syndrome width excess the range of the filed MEMEDTXFERRDATA.mem_txf_err_synd, extra bits is logged in another register MEMEDTXFERRDATAU.mem_txf_err_synd_u.
11:0	RO	0x000	mem_txf_err_addr This filed logs the error location (the address of which the RAM data Ecc error detected).

SATA_BISTDECR

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dwerr This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received. The DWERR value does not roll over and freezes when it exceeds 0xFFFF_F000.

SATA_MEMEDFBSERRCNT

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	mem_fbs_corr_err_cnt FBS Corrected RAM Data Error Count.
7:0	RW	0x00	mem_fbs_uncorr_err_cnt FBS Uncorrected RAM Data Error Count.

SATA_MEMEDFBSERRDATA

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	mem_fbs_err_synd This field logs the error syndrome of the RAM Data Ecc/Parity error, if the syndrome width excess the range of the filed MEMEDFBSERRDATA.mem_fbs_err_synd, extra bits is logged in another register MEMEDFBSERRDATAU.mem_fbs_err_synd_u.
11:0	RO	0x000	mem_fbs_err_addr This filed logs the error location (the address of which the RAM data Ecc/Parity error detected).

SATA_MEMEDERRINJ

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	ued Indicates a single bit uncorrected, or multiple bit error was detected. Cleared by writing '1' to this field.
16	RW	0x0	ced Indicates a single bit error was corrected. Cleared by writing '1' to this field.
15:5	RO	0x000	reserved
4	RW	0x0	oneB_2B Select 'single-bit' or 'two-bit' errors.
3	RW	0x0	cont Selects 'one-shot' (0) or 'continuous' (1) errors.
2:1	RW	0x0	mem_sel 2'b00: All three memory interfaces 2'b01: RX FIFO Memory, 2'b10: TX FIFO Memory, 2'b11: FBS RAM.
0	RW	0x0	err_inj_valid The values in the rest of the fields of this register are valid only when this bit is set to 1.

SATA_OOBR

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31	RW	0x0	we The options for this field are: 1: OOBR bits [30:0] can be written 0: OOBR bits [30:0] are read-only This bit is cleared when COMRESET is detected.
30:24	RW	0x04	cwMin This field is RW when WE=1 and RO when WE=0.
23:16	RW	0x07	cwMax This field is RW when WE=1 and RO when WE=0.
15:8	RW	0x0c	ciMin This field is RW when WE=1 and RO when WE=0.
7:0	RW	0x15	ciMax This field is RW when WE=1 and RO when WE=0.

SATA_MEMEDRXFERRDATAU

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_rxf_err_synd_u When the Rx FIFO RAM Data parity error syndrome width excess the range of the register MEMEDRXFERRDATA.mem_rx_err_synd, extra bits is logged in this field.

SATA_MEMEDTXFERRDATAU

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_txf_err_synd_u When the Tx FIFO RAM Data parity error syndrome width excess the range of the register MEMEDTXFERRDATA.mem_tx_err_synd, extra bits is logged in this field.

SATA_DIAGNR3

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fbcsw_cnt FIS-based context switching counter.

SATA_MEMEDFBSERRDATAU

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mem_fbs_err_synd_u When the FBS RAM Data parity error syndrome width excess the range of the register MEMEDFBSERRDATA.mem_fbs_err_synd, extra bits is logged in this field.

SATA_GPARAM3

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	mem_ap_support The options for this field are as follows: 0: No Address Protection Support, 1: Address Protection Support enabled.
7:3	RO	0x09	phy_type PHY Interface Type.
2	RO	0x1	mem_ecc_cor_en The options for this field are as follows: 0: Single-bit error correction not performed, 1: Single-bit correction performed.
1	RO	0x0	mem_dp_type The options for this field are as follows: 0: ECC, 1: Parity.
0	RO	0x1	mem_dp_support The options for this field are as follows: 0: No Data Protection Support, 1: Data Protection Support enabled.

SATA_TIMER1MS

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x493e0	timv This field contains the following value for the internal timer to generate 1-ms tick: Famba*1000, where Famba = AMBA clock frequency in MHz.

SATA_MEMDPCR

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
9	RO	0x0	mem_par_even This value is derived from the MEM_PAR_EVEN parameter. The options for this field are as follows: 0: Generate odd type of parity for data (if parity type protection selected) and address; 1: Generate even type of parity for data (if parity type protection selected) and address.
8	RW	0x0	mem_err_inj_loc The options for this field are as follows: 0: Inject error on data bits; 1: Inject error on data checkbits.
7	RW	0x0	mem_ed_log_clr_en 0: All error detection and correction logging registers are cleared by Global or COMRESET. 1: All error detection and correction logging registers are cleared only when MEMDPCR.EM_ED_LOG_CLR is set.
6	WO	0x0	mem_ed_log_clr This field clears all error detection and correction logging registers when written. This bit clears itself one cycle after written.
5	RW	0x0	mem_ed_log_dis This field disables error detection and correction logging when set.
4	RW	0x0	mem_ed_ce_en This field enables correctable error detection interrupt(INFS). (For diagnostic purposes only).
3	RW	0x0	mem_ed_pdmaf_dis This field disables PDMA from entering a fatal error state when an uncorrectable error is detected. (For diagnostic purposes only).
2	RW	0x0	mem_ed_ifs_dis This field disables setting the IFS interrupt register bit (interface fatal error status interrupt) when an uncorrectable error is detected.
1	RW	0x0	mem_ec_dis When set, disables the single error correcting features everywhere, and all errors are reported as uncorrectable.
0	RW	0x0	mem_ed_dis All ECC/Parity error detection, correction, interrupt generation and Fatal error state transitions are disabled when this bit is set to 1.

SATA_GPARAM1R

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31	RO	0x1	align_m The options for this field are: 0: Misaligned, 1: Aligned.
30	RO	0x0	rx_buffer 0: Exclude, 1: Include.

Bit	Attr	Reset Value	Description
29:28	RO	0x1	phy_data The options for this field are: 0x0: 8bit, 0x1: 16bit, 0x2: 32bit.
27	RO	0x1	phy_rst The options for this field are: 0: Low enable, 1: High enable.
26:21	RO	0x00	phy_ctrl PHY Control Width.
20:15	RO	0x00	phy_stat PHY Status Width.
14	RO	0x0	latch_m Do not support latch mode.
13:11	RO	0x1	phy_type Support pipe phy.
10	RO	0x1	return_err Support amba error response.
9:0	RO	0x000	reserved

SATA_GPARAM2R

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	bist_m The options for this field are: 0: FIS, 1: DWORD.
18:16	RO	0x0	reserved
15	RO	0x0	fbs_support The options for this field are: 0: Exclude, 1: Include.
14	RO	0x0	reserved
13	RO	0x0	dev_mp The options for this field are: 0: Exclude, 1: Include.
12	RO	0x0	encode_m The options for this field are: 0: Exclude, 1: Include.
11	RO	0x1	rxoob_clk_m The options for this field are: 0: RxClock, 1: Separate.
10	RO	0x0	rx_oob_m The options for this field are: 0: Exclude, 1: Include.
9	RO	0x0	tx_oob_m The options for this field are: 0: Exclude, 1: Include.

Bit	Attr	Reset Value	Description
8:0	RO	0x032	rxoob_clk_lower Rx OOB Clock Frequency (Lower).

SATA_TESTR

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	bsel This field is used to select a bank for BIST or Data Protection operation or Address Protection operation. The options for this field are: 0x0: BIST registers selected 0x1: Data Protection registers selected 0x2: Address Protection registers selected 0x3: Reserved.
23:19	RO	0x00	reserved
18:16	RW	0x0	psel This field is used to select a Port for BIST operation. The options for this field are: 0x0: Port0 is selected 0x1: Port1 is selected 0x2: Port2 is selected 0x3: Port3 is selected 0x4: Port4 is selected 0x5: Port5 is selected 0x6: Port6 is selected 0x7: Port7 is selected.
15:1	RO	0x0000	reserved
0	RW	0x0	test_if This bit is used to put the slave interface into the test mode. The options for this field are: 0: Normal mode: the read back value of some registers is a function of the state and does not match the value written. 1: Test mode: the read back value of the registers matches the value written. Normal operation is disabled.

SATA_IDR

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	id Hard-coded hexadecimal identification value.

SATA_CLB

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	clb Indicates the 32-bit base physical address for the command list for this Port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB-aligned as indicated by bits [9:0] being read only.
9:0	RO	0x000	reserved

SATA_FB

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	fb Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256byte-aligned as indicated by bits [7:0] being read only.
7:0	RO	0x00	reserved

SATA_PIS

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpds This bit is set when the P_cp_det input changes its state due to the insertion or removal of the device.
30	RW	0x0	tfes This bit is set whenever the PTFD.STS register is updated by the device and the error bit [0] is set.
29	RW	0x0	hbfs This bit is set when AXI Master detects an ERROR response from the slave. Port DMA transitions to a fatal state until the software clears PCMD.ST bit or resets the interface by way of Port or Global reset.
28	RW	0x0	hbds This bit is always cleared to 0.
27	RW	0x0	ifs This bit is set when any of the following conditions are detected: SYNC escape is received from the device during non-Data or Data FIS transmission or reception (PSERR.DIAG_S and ERR_P are set); One or more of the following errors are detected during Data FIS transfer: Protocol (PSERR.ERR_P) CRC (PSERR.DIAG_C) Handshake (PSERR.DIAG_H) PHY Not Ready (PSERR.ERR_C) Unknown FIS is received with good CRC, but the length exceeds 64 bytes; PRD table byte count is zero; DMA Setup FIS is received with a TAG corresponding to inactive (PSACT bit is cleared) command slot; RAM address protection error detected (when hardware configuration parameter MEM_AP_SUPPORT is set to Include, and the MEM_AP_ERRFB_EN is set to Include, and the MEMDPCR.MEM_ADDR_ED_IFS_DIS register bit is set to 0); and/or Uncorrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, and the MEMDPCR.MEM_ED_IFS_DIS register bit is set to 0). Port DMA transitions to a fatal state until the software clears PCMD.ST bit or resets the interface by way of Port or Global reset.

Bit	Attr	Reset Value	Description
26	RW	0x0	infs This bit is set when any of the following conditions are detected: One or more of the following errors are detected during non-data FIS transfer: Protocol (PnSERR.ERR_P) CRC (PnSERR.DIAG_C) Handshake (PnSERR.DIAG_H) PHY Not Ready (PnSERR.ERR_C) Command list underflow during read operation (such as, DMA read) when the software builds command table that has more total bytes than the transaction given to the device Corrected error detected (when hardware configuration parameter MEM_DP_SUPPORT is set to Include, MEM_DP_TYPE is set to ECC, and the MEMDPCR.MEM_ED_CE_EN register bit is set to 1) In both cases Port operation continues normally. When error is detected during non-data FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface.
25	RO	0x0	reserved
24	RW	0x0	ofs This bit is set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears PnCMD.ST bit or resets the interface by way of Port or Global reset.
23	RW	0x0	ipms Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22	RW	0x0	prcs This bit reflects the state of the PnSERR.DIAG_N bit. When set to 1, indicates the internal Pn_phy_ready signal changed state. To clear this bit, the software must clear the PnSERR.DIAG_N bit to 0.
21:8	RO	0x0000	reserved
7	RW	0x0	dmps This bit is set when the Pn_mp_switch input changes its state as a result of a mechanical switch attached to this Port opening or closing. This bit is valid only when both CAP.SMPS and PnCMD.MPSP are set.
6	RO	0x0	pcs This bit reflects the state of the PnSERR.DIAG_X bit: 1: Change in Current Connect Status; 0: No change in Current Connect Status. This bit is cleared only when PnSERR.DIAG_X is cleared.
5	RW	0x0	dps A PRD with the I bit set has transferred all of its data.

Bit	Attr	Reset Value	Description
4	RO	0x0	ufs When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the PnSERR.DIAG_F bit to 0.
3	RW	0x0	sdbs A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
2	RW	0x0	dss A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
1	RW	0x0	pss A PIO Setup FIS has been received with the 'I' bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	RW	0x0	dhrs A Device-to-Host Register FIS has been received with the 'I' bit set, and has been copied into system memory.

SATA_PIE

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RW	0x0	cpde Enable Cold Port Detect.
30	RW	0x0	tfee Enable Task File Error.
29	RW	0x0	hbfe Host Bus Fatal Error Enable.
28	RW	0x0	hbde Host Bus Data Error Enable.
27	RW	0x0	ife Interface Fatal Error Enable.
26	RW	0x0	infe Interface Non-Fatal Error Enable.
25	RO	0x0	reserved
24	RW	0x0	ofe Overflow Enable.
23	RW	0x0	ipme Incorrect Port Multiplier Enable.
22	RW	0x0	prce PHY Ready Change Enable.
21:8	RO	0x0000	reserved
7	RW	0x0	dmpe Device Mechanical Presence Status Enable.
6	RO	0x0	pce Port Connect Change Status Enable.
5	RW	0x0	dpe Descriptor Processed Enable.
4	RO	0x0	ufe Unknown FIS Interrupt Enable.
3	RW	0x0	sdbe Set Device Bits Interrupt Enable.
2	RW	0x0	dse DMA Setup FIS Interrupt Enable.

Bit	Attr	Reset Value	Description
1	RW	0x0	pse PIO Setup FIS Interrupt Enable.
0	RW	0x0	dhre Device-to-Host Register FIS Interrupt Enable.

SATA_CMD

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	icc This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state or L_NoCommPower state, writes to this field cause the Port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state or L_NoCommPower, writes to this field have no effect. Else: Reserved 0x6: Slumber. This causes the Port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. 0x2: Partial. This causes the Port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. 0x1: Active. This causes the Port to request a transition of the interface into the active state.
27	RW	0x0	asp The options for this field are: When set to 1, and PnCMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: The Port clears the PnCI and the PnSACT register is cleared. The Port clears the PnSACT register and PnCI is cleared. When cleared to 0, and PnCMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: The Port clears the PnCI register and the PnSACT register is cleared. The Port clears the PnSACT register and PnCI is cleared.
26	RW	0x0	alpe When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the PnCMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled.
25	RW	0x0	dlae When set to 1, PnCMD.ATAPI=1, and commands are active, the Port asserts Pn_act_led output .
24	RW	0x0	atapi This bit is used by the Port to control whether to assert Pn_act_led output when commands are active. The options for this field are: 0: non-ATAPI device 1: ATAPI device

Bit	Attr	Reset Value	Description
23	RW	0x0	apste When this bit is set and the DWC_ahsata Link layer negotiates Partial power management state with the device, it transitions into the Slumber state directly, regardless whether it was host software-, Port (aggressive)-, or device-initiated.
22	RW	0x0	fbscp When set to 1, indicates that this Port supports Port Multiplier FIS-based switching. When cleared to 0, indicates that this Port does not support FIS-based switching. This bit may only be set to 1.
21	RW	0x0	esp When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Port's signal only connector is not externally accessible.
20	RW	0x0	cpd To enable the cold presence detection feature, DEV_CP_DET must be set to Include. Otherwise this bit is read-only '0' on reset. The options for this field are: 1: Platform supports cold presence detection on this Port. When this bit is set to 1, PnCMD.HPCP must also be set to 1. 0: Platform does not support cold presence detection on this Port.
19	RW	0x0	mpsp To enable the mechanical presence detection feature. The options for this field are: 1: Indicates the platform supports a mechanical presence switch attached to this Port. 0: Indicates the platform does not support a mechanical presence switch attached to this Port. When this bit is set to 1, PnCMD.HPCP should also be set to 1.
18	RW	0x0	hpcp The options for this field are: 1: Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blindmate device hot plug. 0: Indicates that this Port's signal and power connectors are not externally accessible.
17	RO	0x0	pma The software is responsible for detecting whether a Port Multiplier is present; the Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 1: A Port Multiplier is attached to this Port. 0: A Port Multiplier is not attached to this Port.
16	RO	0x0	cps This bit reports whether a device is currently detected on this Port as indicated by the Pn_cp_det input state (assuming PnCMD.CPD=1). The options for this field are: 1: device is attached to this Port 0: no device attached to this Port
15	RO	0x0	cr When this bit is set to '1', the command list DMA engine for this Port is running.

Bit	Attr	Reset Value	Description
14	RO	0x0	fr When set to '1', the FIS Receive DMA engine for the Port is running.
13	RO	0x0	mpss The software must use this bit only when both CAP.SMPS and PnCMD.MPSP are set. This bit reports the state of a mechanical presence switch attached to this Port as indicated by the Pn_mp_switch input state (assuming CAP.SMPS=1 and PnCMD.MPSP=1). The options for this field are: 0: Switch is closed 1: Switch is open When CAP.SMPS=0 then this bit is cleared to 0.
12:8	RW	0x00	ccs This field is set to the command slot value of the command that is currently being issued by the Port. When PnCMD.ST transitions from 1 to 0, this field is cleared again to 0x00. After PnCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PnCMD.CCS+1. For example, after the Port has issued its first command, when CCS=0x00 and PnCI is set to 0x3, the next command issued is from command slot 1. This field is valid only when PnCMD.ST is set to 1.
7:5	RO	0x0	reserved
4	RW	0x0	fre When set to 1, the Port may post received FISes into the FIS receive area pointed to by PnFB (and PnFBU when M_HADDR_WIDTH=64). When cleared, received FISes are not accepted by the Port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until PnFB (PnFBU) has been programmed with a valid pointer to the FIS receive area. When the software wishes to move the base, this bit must first be cleared, and the software must wait for the PnCMD.FR bit to be cleared.
3	RW	0x0	clo Setting this bit to 1 causes PnTFD.STS.BSY and PnTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PnTFD.STS register. This bit is cleared to 0 when PnTFD.STS.BSY and PnTFD.STS.DRQ have been cleared to 0. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting PnCMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behavior.

Bit	Attr	Reset Value	Description
2	RW	0x0	pod This bit is read/write when cold presence detection is supported on this Port as indicated by PnCMD.CPD=1. This bit is read-only 1 when cold presence detection is not supported and PnCMD.CPD=0. When set, the Port asserts the Pn_cp_pod output pin so that it may be used to provide power to a cold-presence detectable Port.
1	RW	0x0	sud This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the Port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface.
0	RW	0x0	st When set to 1, the Port processes the command list. When cleared, the Port does not process the command list. Whenever this bit is changed from a 0 to a 1, the Port starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PnCI register is cleared by the Port upon transition into an idle state.

SATA_TFD

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	err This field contains the latest copy of the task file error register.
7:0	RO	0x00	sts This field contains the latest copy of the task file status register. The bits that affect DWC_ahsata operation are: Bit [7] BSY: Indicates the interface is busy Bits [6:4] cs: Command specific Bit [3] DRQ: Indicates a data transfer is requested Bits [2:1] cs: Command specific Bit [0] ERR: Indicates an error during the transfer

SATA_SIG

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sig This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: Bits [31:24]: LBA High (Cylinder High) Register Bits [23:16]: LBA Mid (Cylinder Low) Register Bits [15:8]: LBA Low (Sector Number) Register Bits [7:0]: Sector Count Register This field is updated once after a reset sequence (cause by asynchronous, port, or soft reset). Reset on Global or Port reset.

SATA_SSTS

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
11:8	RO	0x0	ipm Indicates the current interface state. The options for this field are: 0x0: Device not present or communication not established 0x1: Interface in Active state 0x2: Interface in Partial power management state 0x6: Interface in Slumber power management state 0x8: Interface in DevSleep power management state
7:4	RO	0x0	spd Indicates the negotiated interface communication speed. The options for this field are: 0x0: Device not present or communication not established 0x1: 1.5 Gb/s communication rate negotiated 0x2: 3.0 Gb/s communication rate negotiated 0x3: 6.0 Gb/s communication rate negotiated
3:0	RO	0x0	det Indicates the interface device detection and PHY state. The options for this field are: 0x0: No device detected and PHY communication not established 0x1: Device presence detected but PHY communication not established (COMINIT is detected) 0x3: Device presence detected and PHY communication established ('PHY Ready' is detected) 0x4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

SATA_SCTL

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	ipm This field indicates which power states the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the Port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 0x0: No interface power management state restrictions 0x1: Transitions to the Partial state disabled 0x2: Transitions to the Slumber state disabled 0x3: Transitions to both Partial and Slumber states disabled.
7:6	RO	0x0	reserved
5:4	RW	0x0	spd This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 0x0: No speed negotiation restrictions 0x1: Limit speed negotiation to SATA 1.5 Gb/s communication rate 0x2: Limit speed negotiation to SATA 3.0 Gb/s communication rate 0x3: Limit speed negotiation to a rate not greater than SATA 6.0 Gb/s communication rate.
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	det Controls the Port's device detection and interface initialization. The options for this field are: 0x0: No device detection or initialization action requested 0x1: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re initialized. Assert the corresponding Pn_phy_reset(_n) output when DET=0x1. It negates Pn_phy_reset(_n) and sends COMRESET OOB sequence when DET=0x0. 0x4: Disable the Serial ATA interface and put the Port PHY in offline mode.

SATA_SERR

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	diag_x This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the PnIS.PCS bit.
25	RW	0x0	diag_f This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64 bytes.
24	RW	0x0	diag_t This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared.
23	RW	0x0	diag_s This bit indicates that one or more Link state machine error conditions was encountered. One of the conditions that cause this bit to be set is device doing SYNC escape during FIS transmission.
22	RW	0x0	diag_h This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	RW	0x0	diag_c This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception.
20	RO	0x0	diag_d This bit is always cleared to 0 since it is not used by the AHCI specification.
19	RW	0x0	diag_b This bit indicates errors were detected by 10b/8b decoder.
18	RW	0x0	diag_w This bit is set when PHY COMWAKE signal is detected.
17	RW	0x0	diag_i This bit is set when the PHY detects some internal error as indicated by the assertion of the Pn_phy_rx_err input.
16	RW	0x0	diag_n This bit indicates that the PHY Ready signal changed state. This bit is reflected in the PnIS.PRCS bit.

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11	RW	0x0	err_e This bit is set to 1 when one or more AXI bus ERROR responses are detected on the master interface.
10	RW	0x0	err_p This bit is set to 1 when any of the following conditions are detected. Transport state transition error (DIAG_T) Link sequence error (DIAG_S) RX FIFO overflow Link bad end error (WTRM instead of EOF is received).
9	RW	0x0	err_c This bit is set to 1 when PHY Ready signal is negated due to the loss of communication with the device or problems with interface, but not after transition from active to Partial or Slumber power management state.
8	RW	0x0	err_t This bit is set when any of the following PnSERR register bits are set during Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake) ERR_C ('PHY Ready' negation) .
7:2	RO	0x00	reserved
1	RW	0x0	err_m This bit is set to 1 when the PHY Ready condition is asserted under the following conditions: At any time except when there is a transition from power-down mode to Active state After interface initialization (after power on or COMRESET) .
0	RW	0x0	err_i This bit is set when any of the following PnSERR register bits is set during non-Data FIS transfer: ERR_P (Protocol) DIAG_C (CRC) DIAG_H (Handshake)

SATA_SACT

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ds This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing PnCI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: The software writes PnCMD.ST from a 1 to a 0. The device sends a Set Device Bits FIS to the Port. The Port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The Port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: Port reset (COMRESET). Software reset.

SATA_CI

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ci This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the Port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when PnCMD.ST is set to 1.

SATA_SNTF

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	pmn This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the DWC_ahsata Port with the Notification bit set: PM Port 0x0 sets bit 0. PM Port 0x1 sets bit 1. ... PM Port 0xF sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

SATA_FBS

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:16	RO	0x0	dwe This field is set by the sata controller to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when PFBS.SDE=1.
15:12	RW	0x0	ado This field is hard-wired to the FBS_PMPN_MAX value.
11:8	RW	0x0	dev Software sets this field to the Port Multiplier port value of the next command to issue. This field enables the sata controller to know the port the command to be issues to without fetching the command header. Software should not issue commands to multiple Port Multiplier ports on the same write of the PCI register. This bit is reset on Global reset.
7:3	RO	0x00	reserved
2	RW	0x0	sde When this field is set to 1 and a fatal error condition has occurred, the sata controller believes the error is localized to one device such that software's first error recovery step should be to utilize the PFBS.DEC functionality. When cleared to 0 and a fatal error condition has occurred, the error applies to the entire Port. To clear the error, software should clear PCMD.ST to 0. This bit is cleared on PFBS.DEC being set to 1 or on PCMD.ST being cleared to 0. This bit is reset on Global reset.
1	RW	0x0	dec When set to 1 by software, the sata controller clears the device-specific error condition. It flushes any commands outstanding for the device that experienced the error, including clearing PCI and PSACT bits for that device to 0. The sata controller clears this bit to 0 when it completes error recovery actions. When software writes a 0 to this bit, there is no effect. Software should only set this bit to 1 if PFBS.EN=1 and PFBS.SDE=1. This bit is reset on Global reset.
0	RW	0x0	en 1: A Port Multiplier is attached and the DWC_ahsata uses FIS-based switching to communicate with it. 0: FIS-based switching is not being used (command-based switching is used instead). Software should only change the value of this bit when PCMD.ST=0. This bit is reset on Global reset.

SATA_DMACR

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	rxts This field defines the Port DMA transaction size in FIFO words for receive (system bus write, device read) operation. The options for this field are: 0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 All other values are reserved and should not be used. This field is read-write when PnCMD.ST=0 and read-only when PnCMD.ST=1.
3:0	RW	0x0	txts This field defines the DMA transaction size in FIFO words for transmit (system bus read, device write) operation. The options for this field are: 0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 All other values are reserved and should not be used. This field is read-write when PnCMD.ST=0 and read-only when PnCMD.ST=1.

19.5 Interface Description

Table 19-1 SATA host interface description

Module Pin	Dir.	Pad Name	IOMUX Setting
SATA0_CPDET	I	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	GRF_IOFUNC_SEL5[13]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[2:0]=3'h2
SATA1_CPDET	I	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	GRF_IOFUNC_SEL5[14]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[2:0]=3'h2
SATA2_CPDET	I	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	GRF_IOFUNC_SEL5[15]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[2:0]=3'h2
SATA0_MPSWITCH	I	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	GRF_IOFUNC_SEL5[10]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[6:4]=3'h2

Module Pin	Dir.	Pad Name	IOMUX Setting
SATA1_MPSWITCH	I	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	GRF_IOFUNC_SEL5[11]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[6:4]=3'h2
SATA2_MPSWITCH	I	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	GRF_IOFUNC_SEL5[12]=1'h1 & PMU_GRF_GPIO0A_IOMUX_H[6:4]=3'h2
SATA0_CPPOD	O	GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	GRF_IOFUNC_SEL5[9:8]=2'h0 & PMU_GRF_GPIO0A_IOMUX_H[10:8]=3'h1
SATA1_CPPOD		GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	GRF_IOFUNC_SEL5[9:8]=2'h1 & PMU_GRF_GPIO0A_IOMUX_H[10:8]=3'h1
SATA2_CPPOD		GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	GRF_IOFUNC_SEL5[9:8]=2'h2 & PMU_GRF_GPIO0A_IOMUX_H[10:8]=3'h1
SATA0_ACTLED	O	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	GRF_GPIO4C_IOMUX_H[10:8]=3'h3
SATA1_ACTLED	O	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	GRF_GPIO4C_IOMUX_H[6:4]=3'h3
SATA2_ACTLED	O	EDP_DP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	GRF_GPIO4C_IOMUX_H[2:0]=3'h3

19.6 Application Notes

19.6.1 Data transfer

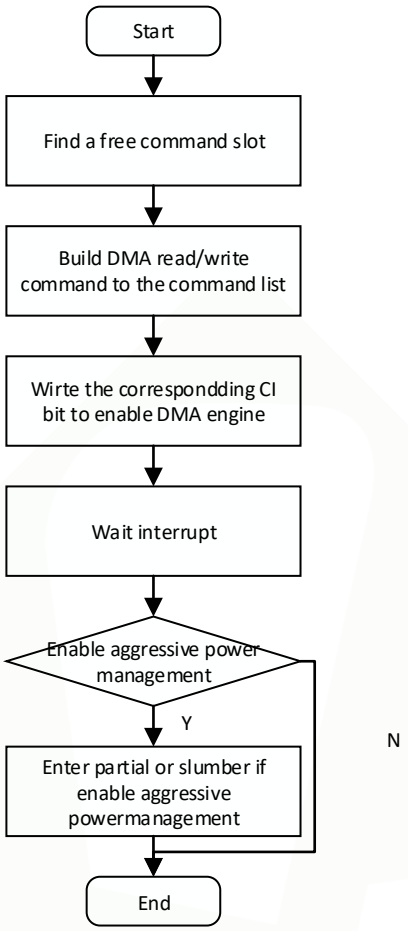


Fig. 19-2 Data transfer flow

19.6.2 Port multiple support

When a port is connected to a Port Multiplier, software must first enumerate it by issuing software reset to Port 0xF(control Port) on the Port Multiplier. When the signature returned corresponds to a Port Multiplier, then a Port Multiplier is attached. When the signature returned corresponds to another device type, then a Port Multiplier is not attached.

The SATA host provides command list override feature via CMD.CLO to help software reliably enumerate the Port Multiplier:

- software ensures that CMD.ST bit is 0;
- software constructs the two register FISes required for a software reset in the command list, where the PM port field value in the register FIS is set to 0xF;
- software set CMD.CLO to 1 to force the BSY and DRQ bits in the TFD register to be cleared;
- software sets CMD.ST bit to 1 and set appropriate CI bits in order to begin execution of the software reset command.

19.6.3 Interrupt

The SATA host uses two-tiered interrupt structure.

First tier(GIS register)

The first tier is identified by the GIS and GHC registers. GHC.IE bit enables interrupts for the entire host: when it is cleared, intrq output is not asserted regardless of any bits set in the GIS register. GHC.IE bit acts as a mask and does not affect the setting of any interrupt status bits.

Second tier(PIS registers)

The second tier is identified in each port through the PIS(status) and PIE(interrupt enable) register. The PIS register has various interrupt bits that can be individually enabled or disabled by setting the corresponding bit in the PIE. The status bit in the PIS is always set regardless of the setting of the corresponding PIE bit.

19.6.4 reset condition

System reset

System bus resets SATA host by asserting aresetn=0. It is usually initiated on power-up or during system bus failure. All components of the host are initialized, including ports, Generic registers, BIU.

Global reset

Software may globally reset host by setting GHC.HR to 1. When software sets the GHC.HR bit to 1, the host performs an internal reset action, then clears this bit to 0 when the reset is complete. A software write of 0 to GHC.HR has no affect.
Port reset (COMRESET)
Software causes a Port reset by writing 1h to the SCTL.DET field to invoke COMRESET on the interface and start a re-establishment of the PHY Layer communication. Software should wait at least 1ms before clearing SCTL.DET to 0h. After clearing SCTL.DET to 0h, software should wait for communication to be re-established as indicated by 0 of SSTS.DET being set to 1. Then software should write all ones to SERR register to clear any bits that were set as part of the Port reset.
Software reset
Software builds two H2D register FISes in the command list. The first register FIS has the SRST bit set to 1 in the control field of the register FIS, the “C” bit is cleared to “0” in the register FIS, and the command table has the CH[R] (reset) and CH[C] (clear BSY ON R_OK) bits set to “1”. The CH[R] bit causes the Port to perform a SYNC escape when necessary to put the device into an idle condition before sending the software reset. The CH[C] bit needs to be set for the first register FIS to clear the BSY bit and proceed to issue the next register FIS since the device does not send a response to the first register FIS in a software reset sequence. The second register FIS has SRST=”0” in the control field of the register FIS, the “C” bit is cleared to “0” in the register FIS, and the command tables has the CH[R] and CH[C] bits cleared to “0”. When issuing a software reset sequence, there should not be other commands in the command list. Before issuing the software reset, software must clear CMD.ST, wait for the Port to be idle, and then re-set CMD.ST. TFD.STS.BSY and TFD.STS.DRQ must be cleared prior to issuing the reset. When TFD.STS.BSY or TFD.STS.DRQ is still set based on the failed command, then a Port reset should be attempted or command list override should be used.

19.6.5 Staggered spin-up

The CMD.SUD bit is used to manipulate the PHY behavior. SCTL.DET and CMD.SUD must be set correctly in order to avoid illegal combinations of the two values. Table 1-1 describes interaction between the CMD.SUD and SCTL.DET bits.

Table 19-2 CMD.SUD and SCTL.DET interaction

SCTL.DET	CMD.SUD	Mode	Behavior
0	0		Interface is in a reduced power state. When COMINIT is received then SERR.DIAG_X is set and no response is sent to the device COMWAVE is ignored. The application must place the Port into this state only when no device is detected as connected to this Port. In this mode, the Port forces the PHY into a low power state without requesting a SLUMBER transition on the link.
0	0->1		Port sends COMRESET, begins initialization sequence.
0	1		Normal operating state when the Port is performing data transfer.
1	0	Illegal	This combination is prohibited in hardware, i.e. CMD.SUD can not be cleared when SCTL/DET=1h, and SCTL.DET can not be set to 1h when CMD.SUD=0.
1	1	Reset	Port continuously transmits COMRESET and does not listen for COMINIT. When COMINIT is received in this state, the SERR.DIAG_X bit is set.
1->0	1	Initialize	Port stops sending COMRESET, being initialization sequence
4	N/A	Off	Port PHY is off.

Software must only clear CMD.SUD when it believe that no device is attached. In listen mode, the Port PHY enters a reduced power state, equivalent to the SLUMBER power management state. The Port PHY enters this state without negotiating a transition to SLUMBER on the link, as asking for a transition to SLUMBER when no device is attached fails, and therefore the PHY remains in a high power state. To avoid this software should ensure that SSTS.DET=0x0 indicating that no device is present before clearing CMD.SUD.

19.6.6 Activity LED

The CAP.SAL=1 indicates that the activity LED feature is enabled to software. Act_led outputs is used to drive an external LED based upon activity of the Port:

- 1 - LED On
- 0 - LED Off

The port drives the LED active if:

- (CI!=0 or SACT!=0) and CMD.ATAPI = 0
- (CI!=0 or SACT!=0) and CMD.ATAPI = 1 and CMD.DLAE = 1

The Port drives the LED off when CI and SACT are both cleared to 0.

19.6.7 Asynchronous notification

The SATA host supports asynchronous notification feature as indicated by the CAP.SSNT=1. This feature allows an ATAPI device to send a signal to the host when media is inserted or removed and avoid polling the device for media changes. The signal sent to the host is Set Device Bits FIS with the "I" and "N" bits set to "1".

To use asynchronous notification, software should set the IS.SDBS bit to enable interrupt notification on a Set Device Bits FIS. When accesses to the ATAPI device are idle, software should place the device in a low power state. When the device has media change, it signals this to the host with a Set Device Bits FIS. In response to receiving a IS.SDBS interrupt on an idle Port, the software should interrogate the device to determine the cause of the interrupt.

The first DWORD of any FIS received by the host contains a 4-bit Port Multiplier field. The PM port field indicates which Port behind the Port Multiplier issued the FIS to the host. When a set device bits FIS is received by the host and "N" bit is set, the bit position in the SNTF register corresponding to the PM Port field is set. The host sets the IS.SDBS to "1" when the "I" bit is set in the set device bits FIS. This causes an interrupt to be generated when that interrupt is enabled.

19.6.8 BIST operation

18.6.8.1 Loopback responder

Software must ensure that the CMD.ST bit is set, the Port is in idle state, and there are no outstanding commands by checking CI and SACT registers are both cleared, TFD.STS register BSY, DRQ and ERR bits are all cleared.

The host enters one of the BIST loopback responder modes when a corresponding BIST Activate FIS is successfully received from the device and is supported by the host. SSTS.DET field return 4h when read. Since BIST registers' locations are shared between all the active ports, software must first select the Port for BIST operation by writing the Port number to the TESTR.PSEL field before accessing BISTAFR.

The following loopback responder modes are supported by the host:

- Far-end retimed
  - The Port receives BIST activate FIS with pattern definition field=0x10 from the RX FIFO and stores it in the BIST AFR.PD field
  - All the data received from the device in the form of a SATA-compliant pattern is retimed in the Link Layer and transmitted back to the device.
  - Alternately, this mode can be initiated with device disconnected from the Port PHY when software writes BISTCR.FERLB=1. After the device is connected to the host, the device must transmit the number of ALIGNs required for the PHY to sync.
- Far-end analog
  - The Port receives BIST active FIS with pattern definition field =0x08 from the RX FIFO and stores it in the BISTAFR.PD field
  - The Port asserts phy_farafelb signal to the PHY to put it to the Far-end analog loopback mode. The PHY receives and retransmits the raw data without retiming
- Far-end transmit only
  - The Port receives BIST activate FIS with pattern definition field = 0xC0(scrambling is enabled) or 0xE0 (scrambling is bypassed) from the RX FIFO and stores it in the BISTAFR.PD field. The second DWORD of the BIST activate FIS least significant byte is stored in the BISTAFR.NCP field.
  - The Port transmits corresponding a SATA non-compliant test pattern to the device based on the BISTAFR.NCP value:
    - 0xF1: Low transition density pattern(LTDP)
    - 0xB5: High transition density pattern(HTDP)
    - 0xAB:Low frequency spectral component pattern(LFSCP)
    - 0x7F:Simultaneous switching outputs pattern(SSOP)
    - 0x78:Mid frequency test pattern(MFTP)
    - 0x4A:High frequency test pattern(HFTP)
    - 0x7E:Low frequency test pattern(LFTP)

If none of the previous pattern is decoded, the Lone bit pattern(LBP) is transmitted by default.

- Alternately, this mode can be initiated with the device disconnected from the Port PHY when software writes a one to BISTCR.TXO bit. Host transmits non-compliant BIST pattern defined by the value in the BISTCR.PATTERN field.

Loopback responder BIST modes can be exited either when the device signals COMINIT OOB condition, or when the software initiates Port reset.

18.6.8.2 Loopback initiator

The software first selects the Port for BIST operation by writing the Port number to the TESTR.PSEL field, then the required pattern by writing to the BISTCR.PATTERN field.
The software builds a BIST FIS with the required mode in the commands list and sets CTBAz[B]. Once a BIST command is placed into the list, software is not allowed to build any more commands until it clears CMD.ST. After the Port successfully transmits this FIS, it enters this mode and generates/receives the compliant test pattern selected by the BISTCR.PATTERN field.
SSTS.DET return 4h when read. BISTCR and BISTFCTR registers are updated with error/FIS count information for each received BIST FIS.
The following BIST initiator modes can be requested by the software:

- Far-end retimed
  - The host software writes the BISTCR.PATTERN field to select one of the SATA-defined compliant patterns:
    - 0x0:Simultaneous switching outputs pattern(SSOP)
    - 0x1:High transition density pattern (HTDP)
    - 0x2:Low transition density pattern(LTDP)
    - 0x3:Low frequency spectral component pattern(LFSCP)
    - 0x4:Composite pattern(COMP)
    - 0x5:Lone bit pattern(LBP)
    - 0x6:Mid frequency test pattern(MFTP)
    - 0x7:High frequency test pattern(HFTP)
    - 0x8:Low frequency test pattern(LFTP)
  - The software prepares BIST Activate FIS with bits[23:16]=0x10 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - After successful transmission of the BIST Activate FIS the Port generates the requested compliant pattern in the form of BIST frames continuously and checks for errors on the receive side.
  - BISTCTR register is updated with received BIST frame count and BISTSR - with frame /burst error count. SERR register is updated with CRC, disparity and 10B8B errors for each frame. BISTFCTR, BISTSR, and BISTDECR registers can be cleared by writing 1 to the BISTCR.CNTCLR bit.
  - To change the pattern, the software issues a Port Reset, write to the BISTCR.PATTERN field to select a new pattern and re-issues the command by setting the CI bit.

- Far-end analog
  - The software prepares BIST Activate FIS with bits[23:16]=0x8 of the first DWORD in the command list. The Port sends this BIST Activate FIS to the device.
  - The operation proceeds as described in the Far-end retimed test above.

- Near-end analog
  - This mode can be initiated either in the PARTIAL power management mode or with the device disconnected from the Port PHY. The software issues a PARTIAL power state request to the device via CMD.ICC field and sets the BISTCR.NEALB bit. The BISTCR.PATTERN field selects the required BIST pattern.
  - The Port asserts phy_nearfelb to the PHY. The PHY loops the data from its transmitter to its receiver and ignores any data coming from the device.

- Far-end transmit only
  - The software prepares BIST Activate FIS in the command list with the second and third DWORDs containing the required pattern, and the first DWORD - with the Pattern definition value corresponding to the required mode - Bit 23 is set, bits

20,19,17 cleared and bits 22,21 and 18 are used to enable the following options:
  - Bit 22 is set - Bypass ALIGN
  - Bit 21 is set - Bypass scrambling
  - Bit 18 is set - primitive bit
- The Port sends this BIST Activate FIS to the device.
- After the device acknowledges the reception of this FIS with R_OKp, the Port disables the PHY receiver and transmitter.

Loopback initiator BIST modes can be terminated either by the device when it signals COMINIT OOB condition(except the near-end analog mode), or when the software initiates Port reset.

19.6.9 command completion coalescing

A command completion coalescing(CCC) feature is used to reduce the interrupt and command completion overhead in a heavily-loaded system. The host generates an interrupt to allow software to process completed commands when either of there conditions is true:

- A software-specified number of commands have completed
- A software-specified time-out has expired

This feature applies to all ports selected to be in the CCC set by software via the CCC_PORTS register.
CCC logic used specific register TIMERIMS to generate 1ms interval based on the application clock frequency. Software must load this register with the required value before enabling the CCC feature: Fappclk*1000, where Fappclk = aclk frequency, in MHz.
Additional Command completion coalescing details and examples can be found in the AHCI specification.

Chapter 20 Gigabit Media Access Controller (GMAC)

20.1 Overview

The Ethernet Quality-of-Service controller(EQOS is commonly referred to as GMAC in this document) provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY. The GMAC includes a DMA controller. The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.

20.1.1 MAC Features

20.1.1.1 MAC Tx and Rx Common Features

- Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit Media Independent Interface (RGMII) PHYs
- 64-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction
- Media clock generation and recovery
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

20.1.1.2 MAC Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to 16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Frame Preemption for MAC Tx

20.1.1.3 MAC Rx Features

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status
- Programmable watchdog timeout limit
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Optional module to detect remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in full-duplex mode)
- Frame Preemption for MAC Rx

20.1.2 MTL Features

20.1.2.1 MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Optimization for packet-oriented transfers with packets delimiters
- Option to have dual-port RAM based asynchronous FIFO controllers or Single-port RAM based synchronous FIFO controllers

- RAM memory instantiation outside the top-level module to facilitate memory testing or instantiation
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)
- Optional Debug and slave mode operation on Queue 0 (default queue)

20.1.2.2 MTL Tx Features

- TX FIFO sizes on transmission is 16 KB
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption
- Optional module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Programmable interrupt options for different operational conditions
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO

20.1.2.3 MTL Rx Features

- Rx queue sizes in the Receive path is 32 KB
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level
- Option to replicate received multicast packets for transfer by multiple Rx DMA channels
- Option to have a programmable lookup table based flexible Parser for filtering and steering the Rx packets

20.1.3 DMA Block Features

- 64-bit data transfers
- Separate DMA channel in the Transmit path for each queue in MTL
- Single or multiple DMA channels for any number of queues in MTL Receive path
- Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- Selectable number of Tx DMA channels with TSO/USO feature enabled
- Time-sensitive conditional packet fetching from system memory by comparing the Slot

Time or IEEE 1588 time information provided in the descriptor (useful for AV applications)

- Programmable control for Transmit Descriptor posted writes to improve the throughput
- Sideband signals to control starting and stopping of DMA channels

20.2 Block Diagram

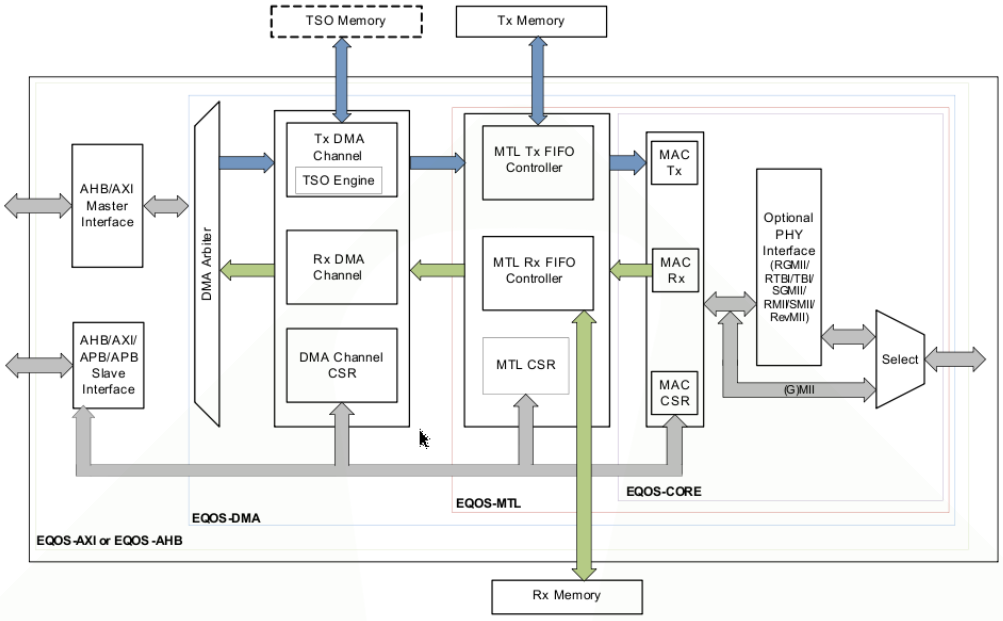


Fig. 20-1 GMAC Block Diagram

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.

The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).

The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).

The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

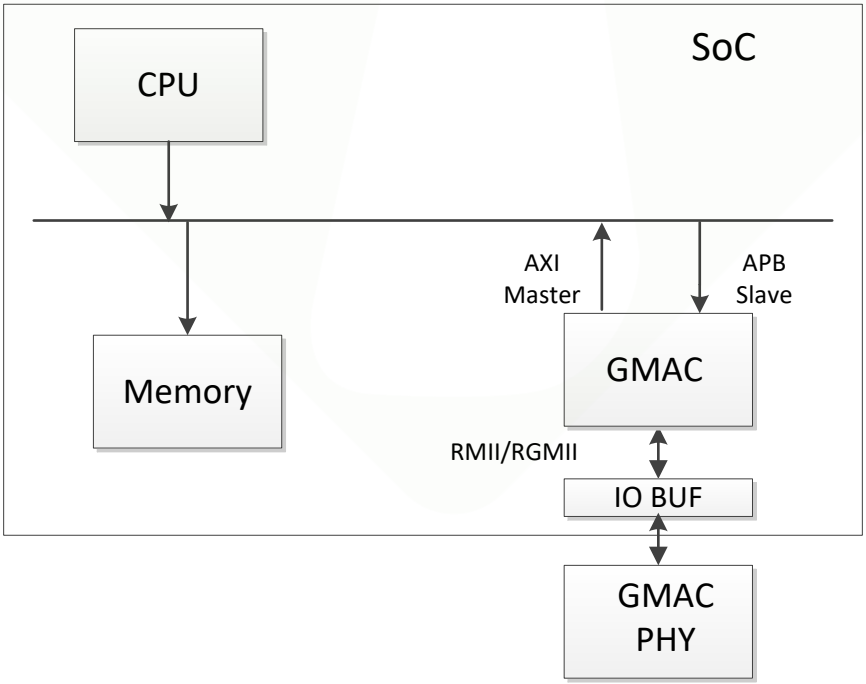


Fig. 20-2 GMAC in SOC

GMAC Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces and Supports 10/100-Mbps data transfer rates with the RMII interfaces.

20.3 Function Description

20.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in Fig.1-3.

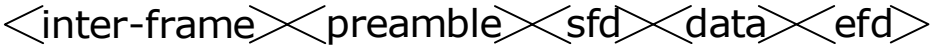


Fig. 20-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

20.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation.
Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

20.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in Fig.1-4. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

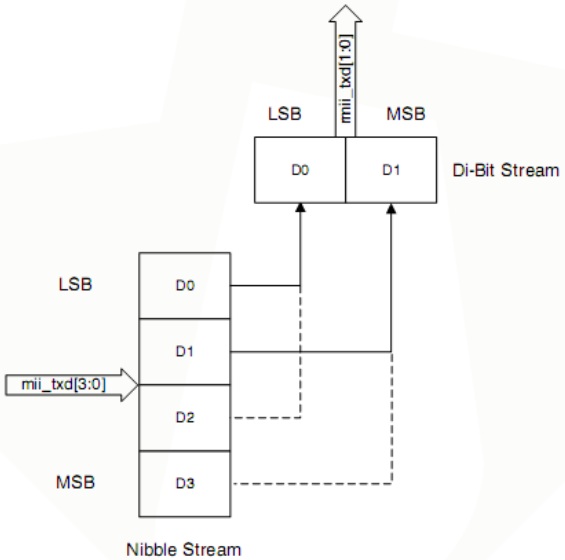


Fig. 20-4 RMII Transmission Bit Ordering

20.3.1.3 RMII Transmit Timing Diagrams

Fig.1-5 through 1-8 show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

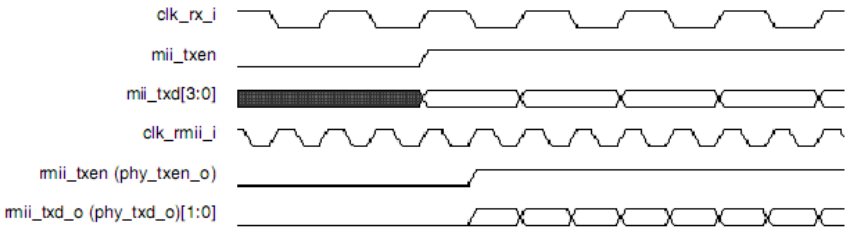


Fig. 20-5 Start of MII and RMII Transmission in 100-Mbps Mode

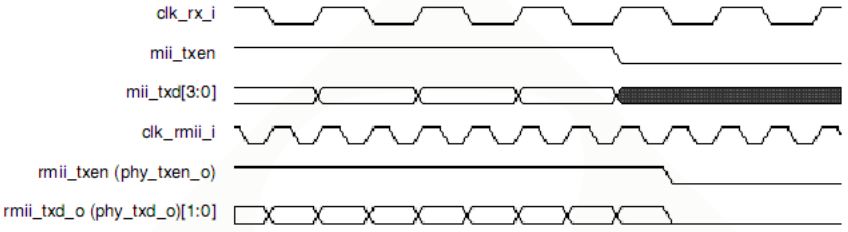


Fig. 20-6 End of MII and RMII Transmission in 100-Mbps Mode

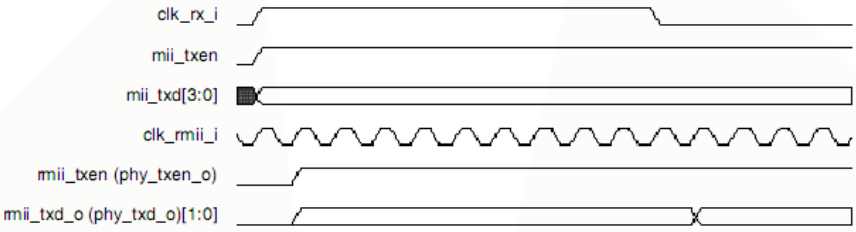


Fig. 20-7 Start of MII and RMII Transmission in 10-Mbps Mode

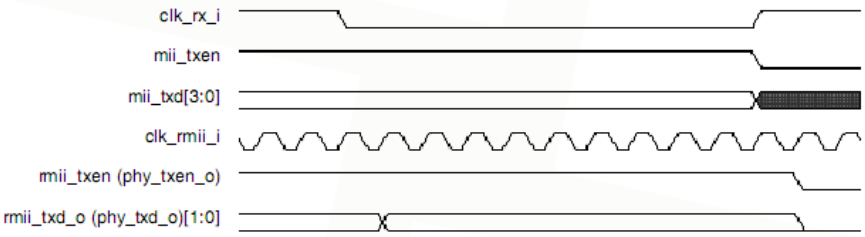


Fig. 20-8 End of MII and RMII Transmission in 10-Mbps Mode

20.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in Fig.1-9. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

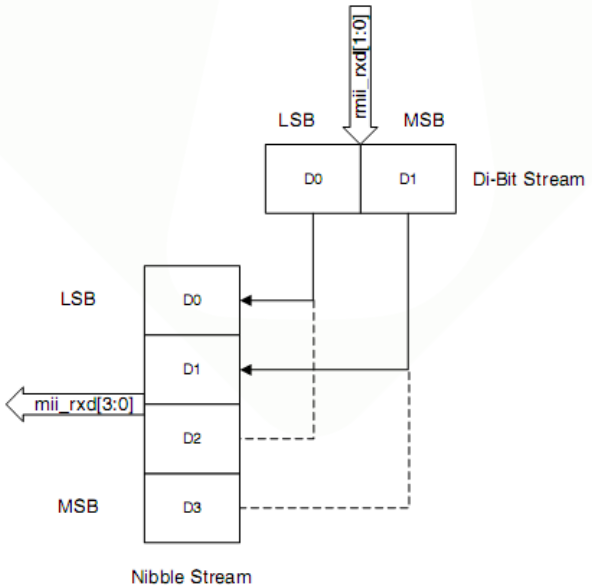


Fig. 20-9 RMII Receive Bit Ordering

20.3.1.5 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection

20.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the GMAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.

The MDIO frame structure is as follows:

Table 20-1 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b00
OPCODE	■ 2'b00 ■ 2'b01 ■ 2'b10 ■ 2'b11
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the GMAC drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16

Field	Description
	bits.

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 20-2 MDIO Clause 22 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01 : Write ■ 2'b10 : Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the GMAC drives MDIO ■ In read operation, the PHY drives MDIO

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

20.3.3 Power Management and Energy Efficient Ethernet

The GMAC supports the following techniques to save power.

- Magic Packet
- Remote Wakeup
- Energy Efficient Ethernet

The Magic Packet and Remove Wakeup techniques are used to save power in the host system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the GMAC (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.

The Energy Efficient Ethernet (EEE) mode is compliant with the IEEE 802.3az-2010 standard. It is primarily targeted to save power in the Ethernet port when there is no traffic on the line. In this mode, the host indicates to the far-end that it does not have any packets to transmit for near future and puts the transmitter port (MAC Controller, PCS and PHY layers) into low-power mode. Similarly, the Receiver port can also be put into low-power mode when the far-end host indicates that it does not have any traffic to transfer. This allows significant saving of power in the Ethernet port (mainly in the PHY) with intermittent and bursty traffic profile. The triggering of entry and exit out of the EEE mode is controlled by the MAC and is supported within the GMAC.

Simultaneous operation of the EEE mode along with any or both the other power saving modes is also supported in GMAC.

20.3.4 IEEE 1588 Timestamp Support

The IEEE 1588 defines a Precision Time Protocol (PTP) which enables precise synchronization of time in measurement and control systems. This protocol enables heterogeneous systems that include clocks of varying inherent precision, resolution, and stability to synchronize. The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources.

The GMAC supports the IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2). The IEEE 1588-2002 supports PTP transported over UDP/IP and IEEE 1588-2008 supports PTP transported over Ethernet. The GMAC provides programmable support for both standards. The controller supports the following features:

- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary, boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a master or slave for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format

20.3.5 TCP/IP Segmentation Offload (TSO) Engine

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.

It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

20.3.6 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.

The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the “MAC_Packet_Filter” register.

The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

20.4 Register Description

20.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_Configuration	0x0000	W	0x00000000	The MAC Configuration Register establishes the operating mode of the MAC
GMAC_MAC_Ext_Configuration	0x0004	W	0x00000000	The MAC Extended Configuration Register establishes the operating mode of the MAC

Name	Offset	Size	Reset Value	Description
GMAC_MAC_Packet_Filter	0x0008	W	0x00000000	The MAC Packet Filter register contains the filter controls for receiving packets
GMAC_MAC_Watchdog_Timeout	0x000C	W	0x00000000	The Watchdog Timeout register controls the watchdog timeout for received packets
GMAC_MAC_Hash_Table_Reg0	0x0010	W	0x00000000	The Hash Table Register 0 contains the first 32 bits of the hash table
GMAC_MAC_Hash_Table_Reg1	0x0014	W	0x00000000	The Hash Table Register 1 contains the second 32 bits of the hash table
GMAC_MAC_VLAN_Tag	0x0050	W	0x00000000	The VLAN Tag register identifies the IEEE 802.1Q VLAN type packets
GMAC_MAC_Q0_Tx_Flow_Ctrl	0x0070	W	0x00000000	The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC
GMAC_MAC_Rx_Flow_Ctrl	0x0090	W	0x00000000	The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet
GMAC_MAC_Interrupt_Status	0x00B0	W	0x00000000	The Interrupt Status register contains the status of interrupts
GMAC_MAC_Interrupt_Enable	0x00B4	W	0x00000000	The Interrupt Enable register contains the masks for generating the interrupts
GMAC_MAC_Rx_Tx_Status	0x00B8	W	0x00000000	The Receive Transmit Status register contains the Receive and Transmit Error status
GMAC_MAC_PMT_Control_Status	0x00C0	W	0x00000000	The PMT Control and Status Register
GMAC_MAC_RWK_Packet_Filter	0x00C4	W	0x00000000	The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register
GMAC_RWK_Filter0_Byte_Mask	0x10C0	W	0x00000000	RWK Filter0 Byte Mask
GMAC_RWK_Filter1_Byte_Mask	0x10C4	W	0x00000000	RWK Filter1 Byte Mask
GMAC_RWK_Filter2_Byte_Mask	0x10C8	W	0x00000000	RWK Filter2 Byte Mask
GMAC_RWK_Filter3_Byte_Mask	0x10CC	W	0x00000000	RWK Filter3 Byte Mask
GMAC_RWK_Filter01_CRC	0x10D0	W	0x00000000	RWK Filter 0/1 CRC-16
GMAC_RWK_Filter23_CRC	0x10D4	W	0x00000000	RWK Filter 2/3 CRC-16
GMAC_RWK_Filter_Offset	0x10D8	W	0x00000000	RWK Filter Offset

Name	Offset	Size	Reset Value	Description
GMAC_RWK_Filter_Command	0x10DC	W	0x00000000	RWK Filter Command
GMAC_MAC_LPI_Control_Status	0x00D0	W	0x00000000	The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read
GMAC_MAC_LPI_Timers_Control	0x00D4	W	0x03E80000	The LPI Timers Control register controls the timeout values in the LPI states.
GMAC_MAC_LPI_Entry_Timer	0x00D8	W	0x00000000	This register controls the Tx LPI entry timer
GMAC_MAC_1US_Tic_Counter	0x00DC	W	0x0000003F	This register controls the generation of the Reference time (1 microsecond tic)
GMAC_MAC_PHYIF_Control_Status	0x00F8	W	0x00000000	PHY Interface Control and Status Register
GMAC_MAC_Version	0x0110	W	0x00003051	The version register identifies the version of the DWC_ether_qos
GMAC_MAC_Debug	0x0114	W	0x00000000	The Debug register provides the debug status of various MAC blocks
GMAC_MAC_HW_Feature0	0x011C	W	0x160171E3	This register indicates the presence of first set of the optional features or functions
GMAC_MAC_HW_Feature1	0x0120	W	0x010C01C8	This register indicates the presence of second set of the optional features or functions
GMAC_MAC_HW_Feature2	0x0124	W	0x10000000	This register indicates the presence of third set of the optional features or functions
GMAC_MAC_HW_Feature3	0x0128	W	0x00000000	This register indicates the presence of fourth set the optional features or functions
GMAC_MAC_MDIO_Address	0x0200	W	0x00000000	The MDIO Address register controls the management cycles to external PHY through a management interface
GMAC_MAC_MDIO_Data	0x0204	W	0x00000000	The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address
GMAC_MAC_CSR_SW_Ctrl	0x0230	W	0x00000000	This register contains SW programmable controls for changing the CSR access response and status bits clearing
GMAC_MAC_Address0_High	0x0300	W	0x0000FFFF	The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station
GMAC_MAC_Address0_Low	0x0304	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station

Name	Offset	Size	Reset Value	Description
GMAC_MMC_Control	0x0700	W	0x00000000	This register establishes the operating mode of MMC
GMAC_MMC_Rx_Interrupt	0x0704	W	0x00000000	Maintains the interrupts generated from all Receive statistics counters
GMAC_MMC_Tx_Interrupt	0x0708	W	0x00000000	Maintains the interrupts generated from all Transmit statistics counters
GMAC_MMC_Rx_Interrupt_Mask	0x070C	W	0x00000000	This register maintains the masks for interrupts generated from all Receive statistics counters
GMAC_MMC_Tx_Interrupt_Mask	0x0710	W	0x00000000	This register maintains the masks for interrupts generated from all Transmit statistics counters
GMAC_Tx_Octet_Count_Good_Bad	0x0714	W	0x00000000	This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets
GMAC_Tx_Packet_Count_Good_Bad	0x0718	W	0x00000000	This register provides the number of good and bad packets, exclusive of retried packets
GMAC_Tx_Underflow_Error_Packets	0x0748	W	0x00000000	This register provides the number of packets aborted because of packets underflow error
GMAC_Tx_Carrier_Error_Packets	0x0760	W	0x00000000	This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier)
GMAC_Tx_Octet_Count_Good	0x0764	W	0x00000000	This register provides the number of bytes exclusive of preamble, only in good packets
GMAC_Tx_Packet_Count_Good	0x0768	W	0x00000000	This register provides the number of good packets transmitted by DWC_ether_qos
GMAC_Rx_Packets_Count_Good_Bad	0x0780	W	0x00000000	This register provides the number of good and bad packets received by DWC_ether_qos
GMAC_Rx_Octet_Count_Good_Bad	0x0784	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, in good and bad packets
GMAC_Rx_Octet_Count_Good	0x0788	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets
GMAC_Rx_Multicast_Packets_Good	0x0790	W	0x00000000	This register provides the number of good multicast packets received by
GMAC_Rx_CRC_Error_Packets	0x0794	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with CRC error

Name	Offset	Size	Reset Value	Description
GMAC_Rx_Length_Error_Packets	0x07C8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field
GMAC_Rx_FIFO_Overflow_Packets	0x07D4	W	0x00000000	This register provides the number of missed received packets because of FIFO overflow
GMAC_MMC_IPC_Rx_Interrupt_Mask	0x0800	W	0x00000000	This register maintains the mask for the interrupt generated from the receive IPC statistic counters
GMAC_MMC_IPC_Rx_Interrupt	0x0808	W	0x00000000	This register maintains the interrupt that the receive IPC statistic counters generate
GMAC_RxIPv4_Good_Packets	0x0810	W	0x00000000	This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload
GMAC_RxIPv4_Header_Error_Packets	0x0814	W	0x00000000	This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors
GMAC_RxIPv6_Good_Packets	0x0824	W	0x00000000	This register provides the number of good IPv6 datagrams received by DWC_ether_qos
GMAC_RxIPv6_Header_Error_Packets	0x0828	W	0x00000000	This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors
GMAC_RxUDP_Error_Packets	0x0834	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error
GMAC_RxTCP_Error_Packets	0x083C	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error
GMAC_RxICMP_Error_Packets	0x0844	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error
GMAC_RxIPv4_Header_Error_Octets	0x0854	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv4 data_grams with header errors (checksum, length, version mismatch)

Name	Offset	Size	Reset Value	Description
GMAC_RxIPv6_Header_Error_Octets	0x0868	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv6 data_grams with header errors (length, version mismatch)
GMAC_RxUDP_Error_Octets	0x0874	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors
GMAC_RxTCP_Error_Octets	0x087C	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors
GMAC_RxICMP_Error_Octets	0x0884	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment
GMAC_MAC_Timestamp_Control	0x0B00	W	0x00000000	This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver
GMAC_MAC_Sub_Second_Increment	0x0B04	W	0x00000000	Specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock
GMAC_MAC_System_Time_Secs	0x0B08	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_System_Time_NS	0x0B0C	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_Sys_Time_Secs_Update	0x0B10	W	0x00000000	The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC
GMAC_MAC_Sys_Time_NS_Update	0x0B14	W	0x00000000	MAC System Time Nanoseconds Update register
GMAC_MAC_Timestamp_Addend	0x0B18	W	0x00000000	Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register)
GMAC_MAC_Timestamp_Status	0x0B20	W	0x00000000	Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register

Name	Offset	Size	Reset Value	Description
GMAC_MAC_Tx_TS_Status_NS	0x0B30	W	0x00000000	This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled
GMAC_MAC_Tx_TS_Status_Secs	0x0B34	W	0x00000000	The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted
GMAC_MAC_Auxiliary_Control	0x0B40	W	0x00000000	The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot
GMAC_MAC_Auxiliary_TS_NS	0x0B48	W	0x00000000	The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot
GMAC_MAC_Auxiliary_TS_Secs	0x0B4C	W	0x00000000	The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register
GMAC_MAC_TS_Ingress_Corr_NS	0x0B58	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path
GMAC_MAC_TS_Egress_Corr_NS	0x0B5C	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path
GMAC_MAC_TS_Ingress_Latency	0x0B68	W	0x00000000	This register holds the Ingress MAC latency
GMAC_MAC_TS_Egress_Latency	0x0B6C	W	0x00000000	This register holds the Egress MAC latency
GMAC_MAC_PPS_Control	0x0B70	W	0x00000000	PPS Control register
GMAC_MTL_DBG_CTL	0x0C08	W	0x00000000	The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access
GMAC_MTL_DBG_STS	0x0C0C	W	0x01900000	The FIFO Debug Status register contains the status of FIFO debug access
GMAC_MTL_FIFO_Debug_Data	0x0C10	W	0x00000000	The FIFO Debug Data register contains the data to be written to or read from the FIFOs
GMAC_MTL_Interrupt_Status	0x0C20	W	0x00000000	The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC

Name	Offset	Size	Reset Value	Description
GMAC_MTL_TxQ0_Operation_Mode	0x0D00	W	0x00000000	The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands
GMAC_MTL_TxQ0_Underflow	0x0D04	W	0x00000000	The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush
GMAC_MTL_TxQ0_Debug	0x0D08	W	0x00000000	The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_Q0_Interrupt_Ctrl_Status	0x0D2C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 0 interrupts
GMAC_MTL_RxQ0_Operation_Mode	0x0D30	W	0x00000000	The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command
GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt	0x0D34	W	0x00000000	The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RxQ0_Debug	0x0D38	W	0x00000000	The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue
GMAC_DMA_Mode	0x1000	W	0x00000000	The Bus Mode register establishes the bus operating modes for the DMA
GMAC_DMA_SysBus_Mode	0x1004	W	0x00010000	The System Bus mode register controls the behavior of the AHB or AXI master
GMAC_DMA_Interrupt_Status	0x1008	W	0x00000000	The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC
GMAC_DMA_Debug_Status0	0x100C	W	0x00000000	The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose
GMAC_AXI_LPI_Entry_Interval	0x1040	W	0x00000000	This register is used to control the AXI LPI entry interval

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.4.2 Detail Registers Description

GMAC_MAC_Configuration

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	ARPEN ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. Values: 1'b0: ARP Offload is disabled 1'b1: ARP Offload is enabled
30:28	RO	0x0	reserved
27	RW	0x0	IPC Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled.The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. Values: 1'b0: IP header/payload checksum checking is disabled 1'b1: IP header/payload checksum checking is enabled
26:24	RW	0x0	IPG Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode.In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG.The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. Values: 3'b000: 96 bit times IPG 3'b001: 88 bit times IPG 3'b010: 80 bit times IPG 3'b011: 72 bit times IPG 3'b100: 64 bit times IPG 3'b101: 56 bit times IPG 3'b110: 48 bit times IPG 3'b111: 40 bit times IPG

Bit	Attr	Reset Value	Description
23	RW	0x0	GPSLCE Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. Values: 1'b0: Giant Packet Size Limit Control is disabled 1'b1: Giant Packet Size Limit Control is enabled
22	RW	0x0	S2KP IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets.When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. Values: 1'b0: Support upto 2K packet is disabled 1'b1: Support upto 2K packet is Enabled
21	RW	0x0	CST CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits. Values: 1'b0: CRC stripping for Type packets is disabled 1'b1: CRC stripping for Type packets is enabled

Bit	Attr	Reset Value	Description
20	RW	0x0	ACS Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit . Values: 1'b0: Automatic Pad or CRC Stripping is disabled 1'b1: Automatic Pad or CRC Stripping is enabled
19	RW	0x0	WD Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes.When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. Values: 1'b0: Watchdog is enabled 1'b1: Watchdog is disabled
18	RW	0x0	BE Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. Values: 1'b0: Packet Burst is disabled 1'b1: Packet Burst is enabled
17	RW	0x0	JD Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet. Values: 1'b0: Jabber is enabled 1'b1: Jabber is disabled
16	RW	0x0	JE Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. Values: 1'b0: Jumbo packet is disabled 1'b1: Jumbo packet is enabled

Bit	Attr	Reset Value	Description
15	RW	0x0	PS Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit. Values: 1'b0: For 1000 or 2500 Mbps operations 1'b1: For 10 or 100 Mbps operations
14	RW	0x0	FES Speed This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit. Values: 1'b0: 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 1'b1: 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0
13	RW	0x0	DM Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
12	RW	0x0	LM Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. Values: 1'b0: Loopback is disabled 1'b1: Loopback is enabled
11	RW	0x0	ECRSFD Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low.When this bit is reset, the MAC transmitter ignores the status of the CRS signal. Values: 1'b0: ECRSFD is disabled 1'b1: ECRSFD is enabled
10	RW	0x0	DO Disable Receive Own When this bit is set, the MAC disables the reception of packets when the gmii_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY.This bit is not applicable in the full-duplex mode. Values: 1'b0: Enable Receive Own 1'b1: Disable Receive Own

Bit	Attr	Reset Value	Description
9	RW	0x0	DCRS Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. Values: 1'b0: Enable Carrier Sense During Transmission 1'b1: Disable Carrier Sense During Transmission
8	RW	0x0	DR Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status.When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. Values: 1'b0: Enable Retry 1'b1: Disable Retry
7	RO	0x0	reserved
6:5	RW	0x0	BL Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. Values: 2'b00: k = min(n,10) 2'b01: k = min(n,8) 2'b10: k = min(n,4) 2'b11: k = min(n,1)

Bit	Attr	Reset Value	Description
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. Values: 1'b0: Deferral check function is disabled 1'b1: Deferral check function is enabled
3:2	RW	0x0	PRELEN Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. Values: 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved
1	RW	0x0	TE Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets. Values: 1'b0: Transmitter is disabled 1'b1: Transmitter is enabled
0	RW	0x0	RE Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. Values: 1'b0: Receiver is disabled 1'b1: Receiver is enabled

GMAC_MAC_Ext_Configuration

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	EIPG Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: EIPG, IPG 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	RW	0x0	EIPGEN Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Values: 1'b0: Extended Inter-Packet Gap is disabled 1'b1: Extended Inter-Packet Gap is enabled
23:19	RO	0x00	reserved
18	RW	0x0	USP Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. Values: 1'b0: Unicast Slow Protocol Packet Detection is disabled 1'b1: Unicast Slow Protocol Packet Detection is enabled
17	RW	0x0	SPEN Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Values: 1'b0: Slow Protocol Detection is disabled 1'b1: Slow Protocol Detection is enabled

Bit	Attr	Reset Value	Description
16	RW	0x0	DCRCC Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Values: 1'b0: CRC Checking is enabled 1'b1: CRC Checking is disabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	GPSL Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

GMAC_MAC_Packet_Filter

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	VTFE VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. Values: 1'b0: VLAN Tag Filter is disabled 1'b1: VLAN Tag Filter is enabled
15:11	RO	0x00	reserved
10	RW	0x0	HPF Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. Values: 1'b0: Hash or Perfect Filter is disabled 2'b1: Hash or Perfect Filter is enabled
9:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PCF Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). Values: 2'b00: MAC filters all control packets from reaching the application 2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2'b10: MAC forwards all control packets to the application even if they fail the Address filter 2'b11: MAC forwards the control packets that pass the Address filter
5	RW	0x0	DBF Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. Values: 1'b0: Enable Broadcast Packets 1'b1: Disable Broadcast Packets
4	RW	0x0	PM Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. Values: 1'b0: Pass All Multicast is disabled 1'b1: Pass All Multicast is enabled
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. Values: 1'b0: DA Inverse Filtering is disabled 1'b1: DA Inverse Filtering is enabled
2	RW	0x0	HMC Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Multicast is disabled 1'b1: Hash Multicast is enabled

Bit	Attr	Reset Value	Description
1	RW	0x0	HUC Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Unicast is disabled 1'b1: Hash Unicast is enabled
0	RW	0x0	PR Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. Values: 1'b0: Promiscuous Mode is disabled 1'b1: Promiscuous Mode is enabled

GMAC_MAC_Watchdog_Timeout

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PWE Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. Values: 1'b0: Programmable Watchdog is disabled 1'b1: Programmable Watchdog is enabled
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	WTO Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. Values: 4'b0000: 2 KB 4'b0001: 3 KB 4'b0010: 4 KB 4'b0011: 5 KB 4'b0100: 6 KB 4'b0101: 7 KB 4'b0110: 8 KB 4'b0111: 9 KB 4'b1000: 10 KB 4'b1001: 11 KB 4'b1010: 12 KB 4'b1011: 13 KB 4'b1100: 14 KB 4'b1101: 15 KB 4'b1110: 16383 Bytes 4'b1111: Reserved

GMAC_MAC_Hash_Table_Reg0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT31T0 MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). 2. Perform bitwise reversal for the value obtained in Step 1. 3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_Hash_Table_Reg1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT63T32 MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

GMAC_MAC_VLAN_Tag

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	EVLRXS Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. Values: 1'b0: VLAN Tag in Rx status is disabled 1'b1: VLAN Tag in Rx status is enabled
23	RO	0x0	reserved

Bit	Attr	Reset Value	Description
22:21	RW	0x0	EVLS Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. Values: 2'b00: Do not strip 2'b01: Strip if VLAN filter passes 2'b10: Strip if VLAN filter fails 2'b11: Always strip
20	RW	0x0	DOVLTC Disable VLAN Type Check When this bit is set, the MAC does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. Values: 1'b0: VLAN Type Check is enabled 1'b1: VLAN Type Check is disabled
19	RW	0x0	ERSVLM Enable Receive S-VLAN Match When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for filtering or matching. Values: 1'b0: Receive S-VLAN Match is disabled 1'b1: Receive S-VLAN Match is enabled
18	RW	0x0	ESVL Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. Values: 1'b0: S-VLAN is disabled 1'b1: S-VLAN is enabled
17	RW	0x0	VTIM VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. Values: 1'b0: VLAN Tag Inverse Match is disabled 1'b1: VLAN Tag Inverse Match is enabled

Bit	Attr	Reset Value	Description
16	RW	0x0	ETV Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. Similarly, when enabled, only 12 bits of the VLAN tag in the received packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for comparison and VLAN hash filtering. Values: 1'b0: 12-Bit VLAN Tag Comparison is disabled 1'b1: 12-Bit VLAN Tag Comparison is enabled
15:0	RW	0x0000	VL VLAN Tag Identifier for Receive Packets This field contains the 802.1Q VLAN tag to identify the VLAN packets. This VLAN tag identifier is compared to the 15th and 16th bytes of the packets being received for VLAN packets. The following list describes the bits of this field: 1. Bits[15:13]: User Priority 2. Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3. Bits[11:0]: VLAN Identifier (VID) field of VLAN tag When the ETV bit is set, only the VID is used for comparison. If this field ([11:0] if ETV is set) is all zeros, the MAC does not check the 15th and 16th bytes for VLAN tag comparison and declares all packets with Type field value of 0x8100 or 0x88a8 as VLAN packets.

GMAC_MAC_Q0_Tx_Flow_Ctrl

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. Values: 1'b0: Zero-Quanta Pause packet generation is enabled 1'b1: Zero-Quanta Pause packet generation is disabled

Bit	Attr	Reset Value	Description
6:4	RW	0x0	PLT Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. Values: 3'b000: Pause Time minus 4 Slot Times (PT -4 slot times) 3'b001: Pause Time minus 28 Slot Times (PT -28 slot times) 3'b010: Pause Time minus 36 Slot Times (PT -36 slot times) 3'b011: Pause Time minus 144 Slot Times (PT -144 slot times) 3'b100: Pause Time minus 256 Slot Times (PT -256 slot times) 3'b101: Pause Time minus 512 Slot Times (PT -512 slot times) 3'b110: Reserved
3:2	RO	0x0	reserved
1	RW	0x0	TFE Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Values: 1'b0: Transmit Flow Control is disabled 1'b1: Transmit Flow Control is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	FCB_BPA Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flow Control Busy or Backpressure Acti_vate is disabled 1'b1: Flow Control Busy or Backpressure Acti_vate is enabled

GMAC_MAC_Rx_Flow_Ctrl

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	UP Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. Values: 1'b0: Unicast Pause Packet Detect disabled 1'b1: Unicast Pause Packet Detect enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	RFE Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. Values: 1'b0: Receive Flow Control is disabled 1'b1: Receive Flow Control is enabled

GMAC_MAC_Interrupt_Status

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	MDIOIS MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: MDIO Interrupt status not active 1'b1: MDIO Interrupt status active
17:15	RO	0x0	reserved
14	RO	0x0	RXSTSIS Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Receive Interrupt status not active 1'b1: Receive Interrupt status active

Bit	Attr	Reset Value	Description
13	RO	0x0	TXSTSIS Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: 1. Excessive Collision (EXCOL) 2. Late Collision (LCOL) 3. Excessive Deferral (EXDEF) 4. Loss of Carrier (LCARR) 5. No Carrier (NCARR) 6. Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Transmit Interrupt status not active 1'b1: Transmit Interrupt status active
12	RO	0x0	TSIS Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: 1. The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. 2. There is an overflow in the Seconds register. 3. The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. Values: 1'b0: Timestamp Interrupt status not active 1'b1: Timestamp Interrupt status active
11	RO	0x0	MMCRXIPIS MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. Values: 1'b0: MMC Receive Checksum Offload Inter_rupt status not active 1'b1: MMC Receive Checksum Offload Interrupt status active

Bit	Attr	Reset Value	Description
10	RO	0x0	MMCTXIS MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Transmit Interrupt status not active 1'b1: MMC Transmit Interrupt status active
9	RO	0x0	MMCRXIS MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Receive Interrupt status not active 1'b1: MMC Receive Interrupt status active
8	RO	0x0	MMCIS MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Interrupt status not active 1'b1: MMC Interrupt status active
7:6	RO	0x0	reserved
5	RO	0x0	LPIIS LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: LPI Interrupt status not active 1'b1: LPI Interrupt status active
4	RO	0x0	PMTIS PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. Values: 1'b0: PMT Interrupt status not active 1'b1: PMT Interrupt status active

Bit	Attr	Reset Value	Description
3	RO	0x0	PHYIS PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: PHY Interrupt not detected 1'b1: PHY Interrupt detected
2:1	RO	0x0	reserved
0	RO	0x0	RGSMIIIS RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. Values: 1'b0: RGMII or SMII Interrupt Status is not active 1'b1: RGMII or SMII Interrupt Status is active

GMAC_MAC_Interrupt_Enable

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	MDIOIE MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. Values: 1'b0: MDIO Interrupt is disabled 1'b1: MDIO Interrupt is enabled
17:15	RO	0x0	reserved
14	RW	0x0	RXSTSIE Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Receive Status Interrupt is disabled 1'b1: Receive Status Interrupt is enabled
13	RW	0x0	TXSTSIE Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Timestamp Status Interrupt is disabled 1'b1: Timestamp Status Interrupt is enabled

Bit	Attr	Reset Value	Description
12	RW	0x0	TSIE Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. Values: 1'b0: Timestamp Interrupt is disabled 1'b1: Timestamp Interrupt is enabled
11:6	RO	0x00	reserved
5	RW	0x0	LPIIE LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. Values: 1'b0: LPI Interrupt is disabled 1'b1: LPI Interrupt is enabled
4	RW	0x0	PMTIE PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. Values: 1'b0: PMT Interrupt is disabled 1'b1: PMT Interrupt is enabled
3	RW	0x0	PHYIE PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. Values: 1'b0: PHY Interrupt is disabled 1'b1: PHY Interrupt is enabled
2:1	RO	0x0	reserved
0	RW	0x0	RGSMIIIE RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. Values: 1'b0: RGMII or SMII Interrupt is disabled 1'b1: RGMII or SMII Interrupt is enabled

GMAC_MAC_Rx_Tx_Status

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RO	0x0	RWT Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No receive watchdog timeout 1'b1: Receive watchdog timed out
7:6	RO	0x0	reserved
5	RO	0x0	EXCOL Excessive Collisions When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Excessive collision is sensed
4	RO	0x0	LCOL Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Late collision is sensed
3	RO	0x0	EXDEF Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Excessive deferral 1'b1: Excessive deferral

Bit	Attr	Reset Value	Description
2	RO	0x0	LCARR Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: Loss of carrier
1	RO	0x0	NCARR No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: No carrier
0	RO	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Transmit Jabber Timeout 1'b1: Transmit Jabber Timeout occurr

GMAC_MAC_PMT_Control_Status

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	RWKFILTRST Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset 1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset
30:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RO	0x00	RWKPTR Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	RO	0x0000	reserved
10	RW	0x0	RWKPFE Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-up Packet Forwarding is disabled 1'b1: Remote Wake-up Packet Forwarding is enabled
9	RW	0x0	GLBLUCAST Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. Values: 1'b0: Global unicast is disabled 1'b1: Global unicast is enabled
8:7	RO	0x0	reserved
6	RO	0x0	RWKPRCVD Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Remote wake-up packet is received 1'b1: Remote wake-up packet is received

Bit	Attr	Reset Value	Description
5	RO	0x0	MGKPRCVD Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Magic packet is received 1'b1: Magic packet is received
4:3	RO	0x0	reserved
2	RW	0x0	RWKPKTEN Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. Values: 1'b0: Remote wake-up packet is disabled 1'b1: Remote wake-up packet is enabled
1	RW	0x0	MGKPKTEN Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. Values: 1'b0: Magic Packet is disabled 1'b1: Magic Packet is enabled
0	RW	0x0	PWRDWN Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Power down is disabled 1'b1: Power down is enabled

GMAC_MAC_RWK_Packet_Filter

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR RWK Packet Filter This field contains the various controls of RWK Packet filter. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfil_ter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_P_MT_Control_Status register. The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31. The fields of Remote Wakeup Filter are described as follows: Filter i Command: The 4-bit filter i command controls the filter i operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 3. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are provided below: (1) The And_Previous bit setting is applicable within a set of 4 filters. (2) Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Pre_vious bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect. (3) If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered.

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR(cont.) (4) If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type. 4. Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled. Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet. 1. The MSB (31st bit) must be zero. 2. Bit j[30:0] is the byte mask. 3. If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored. Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets. 1. This 8-bit pattern-offset is the offset for the filter i first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet. Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register. 1. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1 2. Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following: (1)32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation. (2) 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations.

GMAC_RWK_Filter0_Byte_Mask

Address: Operational Base + offset (0x10C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter0_Byte_Mask Filter0 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_Filter1_Byte_Mask

Address: Operational Base + offset (0x10C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter1_Byte_Mask Filter1 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_Filter2_Byte_Mask

Address: Operational Base + offset (0x10C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter2_Byte_Mask Filter2 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_Filter3_Byte_Mask

Address: Operational Base + offset (0x10CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Filter3_Byte_Mask Filter3 32-bit Mask Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation.

GMAC_RWK_Filter01_CRC

Address: Operational Base + offset (0x10D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter1_CRC Filter1 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter0_CRC Filter0 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1

GMAC_RWK_Filter23_CRC

Address: Operational Base + offset (0x10D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Filter3_CRC Filter3 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1
15:0	RW	0x0000	Filter2_CRC Filter2 CRC-16 This filter CRC-16 contains the CRC_16 value of the pattern. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15+ x^2 + 1

GMAC_RWK_Filter_Offset

Address: Operational Base + offset (0x10D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Filter3_Offset Filter3 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
23:16	RW	0x00	Filter2_Offset Filter2 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
15:8	RW	0x00	Filter1_Offset Filter1 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.
7:0	RW	0x00	Filter0_Offset Filter0 Offset This filter offset defines the offset (within the packet) from which the filter examines the packets. 1. This 8-bit pattern-offset is the offset for the filter first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet.

GMAC_RWK_Filter_Command

Address: Operational Base + offset (0x10DC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	Filter3_Command Filter3 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
23:20	RO	0x0	reserved
19:16	RW	0x0	Filter2_Command Filter2 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	Filter1_Command Filter1 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.
7:4	RO	0x0	reserved
3:0	RW	0x0	Filter0_Command Filter0 Command The 4-bit filter command controls the filter operation. 1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. 2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value. 3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". 4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. 5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled.

GMAC_MAC_LPI_Control_Status

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21	RW	0x0	LPITCSE LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. Values: 1'b0: LPI Tx Clock Stop is disabled 1'b1: LPI Tx Clock Stop is enabled
20	RW	0x0	LPIATE LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. Values: 1'b0: LPI Timer is disabled 1'b1: LPI Timer is enabled
19	RW	0x0	LPITXA LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. Values: 1'b0: LPI Tx Automate is disabled 1'b1: LPI Tx Automate is enabled

Bit	Attr	Reset Value	Description
18	RW	0x0	PLSEN PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. Values: 1'b0: PHY Link Status is disabled 1'b1: PHY Link Status is enabled
17	RW	0x0	PLS PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. Values: 1'b0: link is down 1'b1: link is okay (UP)
16	RW	0x0	LPIEN LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. Values: 1'b0: LPI state is disabled 1'b1: LPI state is enabled
15:10	RO	0x00	reserved
9	RO	0x0	RLPIST Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. Values: 1'b0: Receive LPI state not detected 1'b1: Receive LPI state detected
8	RO	0x0	TLPIST Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. Values: 1'b0: Transmit LPI state not detected 1'b1: Transmit LPI state detected
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	RLPIEX Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 1'b0: Receive LPI exit not detected 1'b1: Receive LPI exit detected
2	RO	0x0	RLPIEN Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 1'b0: Receive LPI entry not detected 1'b1: Receive LPI entry detected
1	RO	0x0	TLPIEX Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Transmit LPI exit not detected 1'b1: Transmit LPI exit detected
0	RO	0x0	TLPIEN Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Transmit LPI entry not detected 1'b1: Transmit LPI entry detected

GMAC_MAC_LPI_Timers_Control

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x3e8	LST LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	RW	0x0000	TWT LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

GMAC_MAC_LPI_Entry_Timer

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:3	RW	0x00000	LPIET LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	RO	0x0	reserved

GMAC_MAC_1US_Tic_Counter

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x03f	TIC_1US_CNTR 1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

GMAC_MAC_PHYIF_Control_Status

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RO	0x0	LNKSTS Link Status This bit indicates whether the link is up (1'b1) or down (1'b0). Values: 1'b0: Link down 1'b1: Link up

Bit	Attr	Reset Value	Description
18:17	RO	0x0	LNKSPEED Link Speed This bit indicates the current speed of the link. Bit 2 is reserved when the MAC is configured for the SMII PHY interface. Values: 2'b00: 2.5 MHz 2'b01: 25 MHz 2'b10: 125 MHz 2'b11: Reserved
16	RO	0x0	LNKMOD Link Mode This bit indicates the current mode of operation of the link. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
15:2	RO	0x0000	reserved
1	RW	0x0	LUD Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface. Values: 1'b0: Link down 1'b1: Link up
0	RW	0x0	TC Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: 1. "Reduced Gigabit Media Independent Interface" 2. "Serial Media Independent Interface" 3. "Serial Gigabit Media Independent Interface" Values: 1'b0: Disable Transmit Configuration in RGMII, SGMII, or SMII 1'b1: Enable Transmit Configuration in RGMII, SGMII, or SMII

GMAC_MAC_Version

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x30	USERVER User-defined Version (configured with coreConsultant)
7:0	RW	0x51	SNPSVER Synopsys-defined Version

GMAC_MAC_Debug

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
18:17	RO	0x0	TFCSTS MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module. Values: 2'b00: Idle state 2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 2'b10: Generating and transmitting a Pause control packet (in full-duplex mode) 2'b11: Transferring input packet for transmission
16	RO	0x0	TPESTS MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected 1'b1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	RO	0x0000	reserved
2:1	RO	0x0	RFCFCSTS MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RO	0x0	RPESTS MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Receive Protocol Engine Status not detected 1'b1: MAC GMII or MII Receive Protocol Engine Status detected

GMAC_MAC_HW_Feature0

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x1	ACTPHYSEL Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. Values: 4'b0000: GMII or MII 4'b0001: RGMII 4'b0010: SGMII 4'b0011: TBI 4'b0100: RMII 4'b0101: RTBI 4'b0110: SMII 4'b0111: RevMII

Bit	Attr	Reset Value	Description
27	RO	0x0	SAVLANINS Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected. Values: 1'b0: Source Address or VLAN Insertion Enable option is not selected 1'b1: Source Address or VLAN Insertion Enable option is selected
26:25	RO	0x3	TSSTSSEL Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 2'b00: Internal 2'b01: External 2'b10: Both 2'b11: Reserved
24	RO	0x0	MACADR64SEL MAC Addresses 64-127 Selected This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected. Values: 1'b0: MAC Addresses 64-127 Select option is not selected 1'b1: MAC Addresses 64-127 Select option is selected
23	RO	0x0	MACADR32SEL MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected. Values: 1'b0: MAC Addresses 32-63 Select option is not selected 1'b1: MAC Addresses 32-63 Select option is selected
22:18	RO	0x00	ADDMACADRSEL MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option.
17	RO	0x0	reserved
16	RO	0x1	RXCOESEL Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected. Values: 1'b0: Receive Checksum Offload Enable option is not selected 1'b1: Receive Checksum Offload Enable option is selected
15	RO	0x0	reserved
14	RO	0x1	TXCOESEL Transmit Checksum Offload Enabled This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected. Values: 1'b0: Transmit Checksum Offload Enable option is not selected 1'b1: Transmit Checksum Offload Enable option is selected

Bit	Attr	Reset Value	Description
13	RO	0x1	EEESEL Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected. Values: 1'b0: Energy Efficient Ethernet Enable option is not selected 1'b1: Energy Efficient Ethernet Enable option is selected
12	RO	0x1	TSSEL IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 1'b0: IEEE 1588-2008 Timestamp Enable option is not selected. 1'b1: IEEE 1588-2008 Timestamp Enable option is selected.
11:10	RO	0x0	reserved
9	RO	0x0	ARPOFFSEL ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected. Values: 1'b0: ARP Offload Enable option is not selected 1'b1: ARP Offload Enable option is selected
8	RO	0x1	MMCSEL RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected. Values: 1'b0: RMON Module Enable option is not selected 1'b1: RMON Module Enable option is selected
7	RO	0x1	MGKSEL PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected. Values: 1'b0: PMT Magic Packet Enable option is not selected 1'b1: PMT Magic Packet Enable option is selected
6	RO	0x1	RWKSEL PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected. Values: 1'b0: PMT Remote Wake-up Packet Enable option is not selected 1'b1: PMT Remote Wake-up Packet Enable option is selected
5	RO	0x1	SMASEL SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected. Values: 1'b0: SMA (MDIO) Interface not selected 1'b1: SMA (MDIO) Interface selected

Bit	Attr	Reset Value	Description
4	RO	0x0	VLHASH VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected. Values: 1'b0: VLAN Hash Filter not selected 1'b1: VLAN Hash Filter selected
3	RO	0x0	PCSSEL PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected. Values: 1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface) 1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface)
2	RO	0x0	HDSEL Half-duplex Support This bit is set to 1 when the half-duplex mode is selected. Values: 1'b0: No Half-duplex support 1'b1: Half-duplex support
1	RO	0x1	GMIISEL 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation. Values: 1'b0: No 1000 Mbps support 1'b1: 1000 Mbps support
0	RO	0x1	MIISEL 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation. Values: 1'b0: No 10 or 100 Mbps support 1'b1: 10 or 100 Mbps support

GMAC_MAC_HW_Feature1

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RO	0x0	L3L4FNUM Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: Values: 4'b0000: No L3 or L4 Filter 4'b0001: 1 L3 or L4 Filter 4'b0010: 2 L3 or L4 Filters 4'b0011: 3 L3 or L4 Filters 4'b0100: 4 L3 or L4 Filters 4'b0101: 5 L3 or L4 Filters 4'b0110: 6 L3 or L4 Filters 4'b0111: 7 L3 or L4 Filters 4'b1000: 8 L3 or L4 Filters
26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RO	0x1	HASHTBLSZ Hash Table Size This field indicates the size of the hash table: Values: 2'b00: No hash table 2'b01: 64 2'b10: 128 2'b11: 256
23	RO	0x0	POUOST One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. Values: 1'b0: One Step for PTP over UDP/IP Feature is not selected 1'b1: One Step for PTP over UDP/IP Feature is selected
22	RO	0x0	reserved
21	RO	0x0	RAVSEL Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. Values: 1'b0: Rx Side Only AV Feature is not selected 1'b1: Rx Side Only AV Feature is selected
20	RO	0x0	AVSEL AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected. Values: 1'b0: AV Feature is not selected 1'b1: AV Feature is selected
19	RO	0x1	DBGMEMA DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected. Values: 1'b0: DMA Debug Registers option is not selected 1'b1: DMA Debug Registers option is selected
18	RO	0x1	TSOEN TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected. Values: 1'b0: TCP Segmentation Offload Feature is not selected 1'b1: TCP Segmentation Offload Feature is selected
17	RO	0x0	SPHEN Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected. Values: 1'b0: Split Header Feature is not selected 1'b1: Split Header Feature is selected

Bit	Attr	Reset Value	Description
16	RO	0x0	DCBEN DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected. Values: 1'b0: DCB Feature is not selected 1'b1: DCB Feature is selected
15:14	RO	0x0	ADDR64 Address Width This field indicates the configured address width: Values: 2'b00: 32 2'b01: 40 2'b10: 48 2'b11: Reserved
13	RO	0x0	ADVTHWORD IEEE 1588 High Word Register Enable This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected. Values: 1'b0: IEEE 1588 High Word Register option is not selected 1'b1: IEEE 1588 High Word Register option is selected
12	RO	0x0	PTOEN PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. Values: 1'b0: PTP Offload feature is not selected 1'b1: PTP Offload feature is selected
11	RO	0x0	OSTEN One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. Values: 1'b0: One-Step Timestamping feature is not selected 1'b1: One-Step Timestamping feature is selected
10:6	RO	0x07	TXFIFOSIZE MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: Reserved

Bit	Attr	Reset Value	Description
5	RO	0x0	SPRAM Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected. Values: 1'b0: Single Port RAM feature is not selected 1'b1: Single Port RAM feature is selected
4:0	RO	0x08	RXFIFOSIZE MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: 256 KB 5'b01100: Reserved

GMAC_MAC_HW_Feature2

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x1	AUXSNAPNUM Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: Values: 3'b000: No auxiliary input 3'b001: 1 auxiliary input 3'b010: 2 auxiliary input 3'b011: 3 auxiliary input 3'b100: 4 auxiliary input 3'b101: Reserved
27	RO	0x0	reserved
26:24	RO	0x0	PPSOUTNUM Number of PPS Outputs This field indicates the number of PPS outputs: Values: 3'b000: No PPS output 3'b001: 1 PPS output 3'b010: 2 PPS output 3'b011: 3 PPS output 3'b100: 4 PPS output 3'b101: Reserved
23:22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21:18	RO	0x0	TXCHCNT Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels: Values: 4'b0000: 1 MTL Tx Channel 4'b0001: 2 MTL Tx Channels 4'b0010: 3 MTL Tx Channels 4'b0011: 4 MTL Tx Channels 4'b0100: 5 MTL Tx Channels 4'b0101: 6 MTL Tx Channels 4'b0110: 7 MTL Tx Channels 4'b0111: 8 MTL Tx Channels
17:16	RO	0x0	reserved
15:12	RO	0x0	RXCHCNT Number of DMA Receive Channels This field indicates the number of DMA Receive channels: Values: 4'b0000: 1 MTL Rx Channel 4'b0001: 2 MTL Rx Channels 4'b0010: 3 MTL Rx Channels 4'b0011: 4 MTL Rx Channels 4'b0100: 5 MTL Rx Channels 4'b0101: 6 MTL Rx Channels 4'b0110: 7 MTL Rx Channels 4'b0111: 8 MTL Rx Channels
11:10	RO	0x0	reserved
9:6	RO	0x0	TXQCNT Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues: Values: 4'b0000: 1 MTL Tx Queue 4'b0001: 2 MTL Tx Queues 4'b0010: 3 MTL Tx Queues 4'b0011: 4 MTL Tx Queues 4'b0100: 5 MTL Tx Queues 4'b0101: 6 MTL Tx Queues 4'b0110: 7 MTL Tx Queues 4'b0111: 8 MTL Tx Queues
5:4	RO	0x0	reserved
3:0	RO	0x0	RXQCNT Number of MTL Receive Queues This field indicates the number of MTL Receive queues: Values: 4'b0000: 1 MTL Rx Queue 4'b0001: 2 MTL Rx Queues 4'b0010: 3 MTL Rx Queues 4'b0011: 4 MTL Rx Queues 4'b0100: 5 MTL Rx Queues 4'b0101: 6 MTL Rx Queues 4'b0110: 7 MTL Rx Queues 4'b0111: 8 MTL Rx Queues

GMAC_MAC_HW_Feature3

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RO	0x0	ASP Automotive Safety Package Following are the encoding for the different Safety features. Values: 2'b00: No Safety features selected 2'b01: Only "ECC protection for external memory" feature is selected 2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external inter_face" feature 2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
27	RO	0x0	TBSSEL Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected. Values: 1'b0: Time Based Scheduling Enable feature is not selected 1'b1: Time Based Scheduling Enable feature is selected
26	RO	0x0	FPESEL Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected. Values: 1'b0: Frame Preemption Enable feature is not selected 1'b1: Frame Preemption Enable feature is selected
25:22	RO	0x0	reserved
21:20	RO	0x0	ESTWID Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. Values: 2'b00: Width not configured 2'b01: 16 2'b10: 20 2'b11: 24
19:17	RW	0x0	ESTDEP Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5. Values: 3'b000: No Depth configured 3'b001: 64 3'b010: 128 3'b011: 256 3'b100: 512 3'b101: 1024 3'b110: Reserved

Bit	Attr	Reset Value	Description
16	RO	0x0	ESTSEL Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. Values: 1'b0: Enable Enhancements to Scheduling Traffic feature is not selected 1'b1: Enable Enhancements to Scheduling Traffic feature is selected
15	RO	0x0	reserved
14:13	RO	0x0	FRPES Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. Values: 2'b00: 64 Entries 2'b01: 128 Entries 2'b10: 256 Entries 2'b11: Reserved
12:11	RO	0x0	FRPBS Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. Values: 2'b00: 64 Bytes 2'b01: 128 Bytes 2'b10: 256 Bytes 2'b11: Reserved
10	RO	0x0	FRPSEL Flexible Receive Parser Selected This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected. Values: 1'b0: Flexible Receive Parser feature is not selected 1'b1: Flexible Receive Parser feature is selected
9	RO	0x0	PDUPSEL Broadcast/Multicast Packet Duplication This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected. Values: 1'b0: Broadcast/Multicast Packet Duplication feature is not selected 1'b1: Broadcast/Multicast Packet Duplication feature is selected
8:6	RO	0x0	reserved
5	RO	0x0	DVLAN Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. Values: 1'b0: Double VLAN option is not selected 1'b1: Double VLAN option is selected

Bit	Attr	Reset Value	Description
4	RO	0x0	CBTISEL Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. Values: 1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
3	RO	0x0	reserved
2:0	RO	0x0	NRVF Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected: Values: 3'b000: No Extended Rx VLAN Filters 3'b001: 4 Extended Rx VLAN Filters 3'b010: 8 Extended Rx VLAN Filters 3'b011: 16 Extended Rx VLAN Filters 3'b100: 24 Extended Rx VLAN Filters 3'b101: 32 Extended Rx VLAN Filters 3'b110: Reserved

GMAC_MAC_MDIO_Address

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	PSE Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. Values: 1'b0: Preamble Suppression disabled 1'b1: Preamble Suppression enabled
26	RW	0x0	BTB Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. Values: 1'b0: Back to Back transactions disabled 1'b1: Back to Back transactions enabled

Bit	Attr	Reset Value	Description
25:21	RW	0x00	PA Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	RW	0x00	RDA Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	RO	0x0	reserved
14:12	RW	0x0	NTC Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	RW	0x0	CR CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 4'b1000: CSR clock/4 4'b1001: CSR clock/6 4'b1010: CSR clock/8 4'b1011: CSR clock/10 4'b1100: CSR clock/12 4'b1101: CSR clock/14 4'b1110: CSR clock/16 4'b1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	SKAP Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. Values: 1'b0: Skip Address Packet is disabled 1'b1: Skip Address Packet is enabled
3	RW	0x0	GOC_1 GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 2'b00: Reserved 2'b01: Write 2'b10: Post Read Increment Address for Clause 45 PHY 2'b11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid. Values: 1'b0: GMII Operation Command 1 is disabled 1'b1: GMII Operation Command 1 is enabled
2	RW	0x0	GOC_0 GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1. Values: 1'b0: GMII Operation Command 0 is disabled 1'b1: GMII Operation Command 0 is enabled
1	RW	0x0	C45E Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. Values: 1'b0: Clause 45 PHY is disabled 1'b1: Clause 45 PHY is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	GB GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: GMII Busy is disabled 1'b1: GMII Busy is enabled

GMAC_MAC_MDIO_Data

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RA Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	RW	0x0000	GD GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

GMAC_MAC_CSR_SW_Ctrl

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	RCWE Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. Values: 1'b0: Register Clear on Write 1 is disabled 1'b1: Register Clear on Write 1 is enabled

GMAC_MAC_Address0_High

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30:16	RO	0x0000	reserved
15:0	RW	0xffff	ADDRHI MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_Address0_Low

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MMC_Control

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	UCDBC Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. Values: 1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled 1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	CNTPRSTLVL Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. Values: 1'b0: Full-Half Preset is disabled 1'b1: Full-Half Preset is enabled
4	RW	0x0	CNTPRST Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters Preset is disabled 1'b1: Counters Preset is enabled
3	RW	0x0	CNTFREEZ MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. Values: 1'b0: MMC Counter Freeze is disabled 1'b1: MMC Counter Freeze is enabled
2	RW	0x0	RSTONRD Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. Values: 1'b0: Reset on Read is disabled 1'b1: Reset on Read is enabled
1	RW	0x0	CNTSTOPRO Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. Values: 1'b0: Counter Stop Rollover is disabled 1'b1: Counter Stop Rollover is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	CNTRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters are not reset 1'b1: All counters are reset

GMAC_MMC_Rx_Interrupt

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	RXFOVPIS MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected
20:19	RO	0x0	reserved
18	RO	0x0	RXLENERPIS MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected
17:6	RO	0x000	reserved
5	RO	0x0	RXCRCERPIS MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detecte 1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected

Bit	Attr	Reset Value	Description
4	RO	0x0	RXMCGPIS MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected
3	RO	0x0	reserved
2	RO	0x0	RXGOCTIS MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Octet Counter Interrupt Status detected
1	RO	0x0	RXGBOCTIS MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected
0	RO	0x0	RXGBPKTIS MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected

GMAC_MMC_Tx_Interrupt

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21	RO	0x0	TXGPKTIS MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Packet Counter Interrupt Status detected
20	RO	0x0	TXGOCTIS MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Octet Counter Interrupt Status detected
19	RO	0x0	TXCARERPIS MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected
18:14	RO	0x00	reserved
13	RO	0x0	TXUFLOWERPIS MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected
12:2	RO	0x000	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	TXGBPKTIS MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected
0	RO	0x0	TXGBOCTIS MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected

GMAC_MMC_Rx_Interrupt_Mask

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	RXFOVPIM MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled
20:19	RO	0x0	reserved
18	RW	0x0	RXLENERPIM MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled
17:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	RXCRCERPIM MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled
4	RW	0x0	RXMCGPIM MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled
3	RO	0x0	reserved
2	RW	0x0	RXGOCTIM MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled
1	RW	0x0	RXGBOCTIM MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled
0	RW	0x0	RXGBPKTIM MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled

GMAC_MMC_Tx_Interrupt_Mask

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

Bit	Attr	Reset Value	Description
21	RW	0x0	TXGPKTIM MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled
20	RW	0x0	TXGOCTIM MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled
19	RW	0x0	TXCARERPIM MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled
18:14	RO	0x00	reserved
13	RW	0x0	TXUFLOWERPIM MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled
12:2	RO	0x000	reserved
1	RW	0x0	TXGBPKTIM MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	TXGBOCTIM MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled

GMAC_Tx_Octet_Count_Good_Bad

Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTGB Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

GMAC_Tx_Packet_Count_Good_Bad

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTGB Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

GMAC_Tx_Underflow_Error_Packets

Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXUNDRFLW Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

GMAC_Tx_Carrier_Error_Packets

Address: Operational Base + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXCARR Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

GMAC_Tx_Octet_Count_Good

Address: Operational Base + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTG Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

GMAC_Tx_Packet_Count_Good

Address: Operational Base + offset (0x0768)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTG Tx Packet Count Good This field indicates the number of good packets transmitted.

GMAC_Rx_Packets_Count_Good_Bad

Address: Operational Base + offset (0x0780)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPKTGB Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

GMAC_Rx_Octet_Count_Good_Bad

Address: Operational Base + offset (0x0784)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTGB Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

GMAC_Rx_Octet_Count_Good

Address: Operational Base + offset (0x0788)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTG Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

GMAC_Rx_Multicast_Packets_Good

Address: Operational Base + offset (0x0790)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXMCASTG Rx Multicast Packets Good This field indicates the number of good multicast packets received.

GMAC_Rx_CRC_Error_Packets

Address: Operational Base + offset (0x0794)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXCRCERR Rx CRC Error Packets This field indicates the number of packets received with CRC error.

GMAC_Rx_Length_Error_Packets

Address: Operational Base + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXLENERR Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

GMAC_Rx_FIFO_Overflow_Packets

Address: Operational Base + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXFIFOOVFL Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

GMAC_MMC_IPC_Rx_Interrupt_Mask

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RXICMPEROIM MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled
28	RO	0x0	reserved
27	RW	0x0	RXTCPEROIM MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled
26	RO	0x0	reserved
25	RW	0x0	RXUDPEROIM MMC Receive UDP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled
24:23	RO	0x0	reserved
22	RW	0x0	RXIPV6HEROIM MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Value: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled
21:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	RXIPV4HEROIM MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled
16:14	RO	0x0	reserved
13	RW	0x0	RXICMPERPIM MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RO	0x0	reserved
11	RW	0x0	RXTCPERPIM MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RO	0x0	reserved
9	RW	0x0	RXUDPERPIM MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8:7	RO	0x0	reserved
6	RW	0x0	RXIPV6HERPIM MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled

Bit	Attr	Reset Value	Description
5	RW	0x0	RXIPV6GPIM MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:2	RO	0x0	reserved
1	RW	0x0	RXIPV4HERPIM MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled
0	RW	0x0	RXIPV4GPIM MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

GMAC_MMC_IPC_Rx_Interrupt

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	RXICMPEROIS MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected
28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RO	0x0	RXTCPEROIS MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected
26	RO	0x0	reserved
25	RO	0x0	RXUDPEROIS MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected
24:23	RO	0x0	reserved
22	RO	0x0	RXIPV6HEROIS MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected
21:18	RO	0x0	reserved
17	RO	0x0	RXIPV4HEROIS MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected
16:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RO	0x0	RXICMPERPIS MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RO	0x0	reserved
11	RO	0x0	RXTCPERPIS MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RO	0x0	reserved
9	RO	0x0	RXUDPERPIS MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected
8:7	RO	0x0	reserved
6	RO	0x0	RXIPV6HERPIS MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected

Bit	Attr	Reset Value	Description
5	RO	0x0	RXIPV6GPIS MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:2	RO	0x0	reserved
1	RO	0x0	RXIPV4HERPIS MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected
0	RO	0x0	RXIPV4GPIS MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

GMAC_RxIPv4_Good_Packets

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4GDPKT RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RxIPv4_Header_Error_Packets

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERRPKT RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

GMAC_RxIPv6_Good_Packets

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6GDPKT RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RxIPv6_Header_Error_Packets

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERRPKT RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

GMAC_RxUDP_Error_Packets

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERRPKT RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

GMAC_RxTCP_Error_Packets

Address: Operational Base + offset (0x083C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERRPKT RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

GMAC_RxICMP_Error_Packets

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERRPKT RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

GMAC_RxIPv4_Header_Error_Octets

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERROCT RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RxIPv6_Header_Error_Octets

Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERROCT RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RxUDP_Error_Octets

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERROCT RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RxTCP_Error_Octets

Address: Operational Base + offset (0x087C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERROCT RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RxICMP_Error_Octets

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERROCT RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_MAC_Timestamp_Control

Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	AV8021ASMEN AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. Values: 1'b0: AV 802.1AS Mode is disabled 1'b1: AV 802.1AS Mode is enabled
27:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	TXTSSTSM Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. Values: 1'b0: Transmit Timestamp Status Mode is disabled 1'b1: Transmit Timestamp Status Mode is enabled
23:21	RO	0x0	reserved
20	RW	0x0	ESTI External System Time Input When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: 1. To take the timestamp provided as status 2. To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time. Values: 1'b0: External System Time Input is disabled 1'b1: External System Time Input is enabled
19	RO	0x0	reserved
18	RW	0x0	TSENMACADDR Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. Values: 1'b0: MAC Address for PTP Packet Filtering is disabled 1'b1: MAC Address for PTP Packet Filtering is enabled
17:16	RW	0x0	SNAPTYPSEL Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.

Bit	Attr	Reset Value	Description
15	RW	0x0	TSMSTRENA Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. Values: 1'b0: Snapshot for Messages Relevant to Master is disabled 1'b1: Snapshot for Messages Relevant to Master is enabled
14	RW	0x0	TSEVNTENA Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. Values: 1'b0: Timestamp Snapshot for Event Messages is disabled 1'b1: Timestamp Snapshot for Event Messages is enabled
13	RW	0x0	TSIPV4ENA Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. Values: 1'b0: Processing of PTP Packets Sent over IPv4-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv4-UDP is enabled
12	RW	0x0	TSIPV6ENA Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. Values: 1'b0: Processing of PTP Packets Sent over IPv6-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv6-UDP is enabled
11	RW	0x0	TSIPENA Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. Values: 1'b0: Processing of PTP over Ethernet Packets is disabled 1'b1: Processing of PTP over Ethernet Packets is enabled
10	RW	0x0	TSVER2ENA Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. Values: 1'b0: PTP Packet Processing for Version 2 Format is disabled 1'b1: PTP Packet Processing for Version 2 Format is enabled

Bit	Attr	Reset Value	Description
9	RW	0x0	TSCTRLSSR Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. Values: 1'b0: Timestamp Digital or Binary Rollover Control is disabled 1'b1: Timestamp Digital or Binary Rollover Control is enabled
8	RW	0x0	TSENALL Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. Values: 1'b0: Timestamp for All Packets disabled 1'b1: Timestamp for All Packets enabled
7:6	RO	0x0	reserved
5	RW	0x0	TSADDREG Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Addend Register is not updated 1'b1: Addend Register is updated
4	RW	0x0	TSTRIG Enable Timestamp Interrupt Trigger When this bit is set, the timestamp interrupt is generated when the System Time becomes greater than the value written in the Target Time register. This bit is reset after the Timestamp Trigger Interrupt is generated. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp Interrupt Trigger is not enabled 1'b1: Timestamp Interrupt Trigger is enabled

Bit	Attr	Reset Value	Description
3	RW	0x0	TSUPDT Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not updated 1'b1: Timestamp is updated
2	RW	0x0	TSINIT Initalize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not initialized 1'b1: Timestamp is initialized
1	RW	0x0	TSCFUPDT Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. Values: 1'b0: Coarse method is used to update system timestamp 1'b1: Fine method is used to update system timestamp
0	RW	0x0	TSENA Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode.On the Receive side, the MAC processes the 1588 packets only if this bit is set. Values: 1'b0: Timestamp is disabled 1'b1: Timestamp is enabled

GMAC_MAC_Sub_Second_Increment

Address: Operational Base + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	SSINC Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:0	RO	0x0000	reserved

GMAC_MAC_System_Time_Secs

Address: Operational Base + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

GMAC_MAC_System_Time_NS

Address: Operational Base + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

GMAC_MAC_Sys_Time_Secs_Update

Address: Operational Base + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

GMAC_MAC_Sys_Time_NS_Update

Address: Operational Base + offset (0x0B14)

Bit	Attr	Reset Value	Description
31	RW	0x0	ADDSUB Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. Values: 1'b0: Add time 1'b1: Subtract time
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register.When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

GMAC_MAC_Timestamp_Addend

Address: Operational Base + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSAR Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

GMAC_MAC_Timestamp_Status

Address: Operational Base + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	ATSNS Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.

Bit	Attr	Reset Value	Description
24	RO	0x0	ATSSTM Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Values: 1'b0: Auxiliary Timestamp Snapshot Trigger Missed status not detected 1'b1: Auxiliary Timestamp Snapshot Trigger Missed status detected
23:16	RO	0x00	reserved
15	RO	0x0	TXTSSIS Tx Timestamp Status Interrupt Status In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Tx Timestamp Status Interrupt status not detected 1'b1: Tx Timestamp Status Interrupt status detected
14:4	RO	0x000	reserved
3	RO	0x0	TSTRGTERR0 Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Error status not detected 1'b1: Timestamp Target Time Error status detected
2	RO	0x0	AUXTSTRIG Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Auxiliary Timestamp Trigger Snapshot status not detected 1'b1: Auxiliary Timestamp Trigger Snapshot status detected

Bit	Attr	Reset Value	Description
1	RO	0x0	TSTARGT0 Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Reached status not detected 1'b1: Timestamp Target Time Reached status detected
0	RO	0x0	TSSOVF Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Seconds Overflow status not detected 1'b1: Timestamp Seconds Overflow status detected

GMAC_MAC_Tx_TS_Status_NS

Address: Operational Base + offset (0x0B30)

Bit	Attr	Reset Value	Description
31	RO	0x0	TXTSSMIS Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: 1. The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset. 2. The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Transmit Timestamp Status Missed status not detected 1'b1: Transmit Timestamp Status Missed status detected
30:0	RO	0x00000000	TXTSSLO Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

GMAC_MAC_Tx_TS_Status_Secs

Address: Operational Base + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXTSSHI Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

GMAC_MAC_Auxiliary_Control

Address: Operational Base + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ATSFC Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Auxiliary Snapshot FIFO Clear is disabled 1'b1: Auxiliary Snapshot FIFO Clear is enabled

GMAC_MAC_Auxiliary_TS_NS

Address: Operational Base + offset (0x0B48)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	AUXTSLO Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

GMAC_MAC_Auxiliary_TS_Secs

Address: Operational Base + offset (0x0B4C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AUXTSHI Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

GMAC_MAC_TS_Ingress_Corr_NS

Address: Operational Base + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSIC Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

GMAC_MAC_TS_Egress_Corr_NS

Address: Operational Base + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSEC Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

GMAC_MAC_TS_Ingress_Latency

Address: Operational Base + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ITLNS Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.

Bit	Attr	Reset Value	Description
15:8	RO	0x00	ITLSNS Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	RO	0x00	reserved

GMAC_MAC_TS_Egress_Latency

Address: Operational Base + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ETLNS Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	RO	0x00	ETLSNS Egress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	RO	0x00	reserved

GMAC_MAC_PPS_Control

Address: Operational Base + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	PPSCTRL_PPSCMD PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 4'b0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. 4'b0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 4'b0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 4'b0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. ... 4'b1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: 1. When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms. 2. When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high). 3. When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high). This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	PPSCTRL_PPSCMD(cont.) Flexible PPS Output (ptp_pps_o[0]) Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: 4'b0000: No Command 4'b0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. 4'b0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. 4'b0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. 4'b0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. 4'b0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). 4'b0110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. 4'b0111-4'b1111: Reserved

GMAC_MTL_DBG_CTL

Address: Operational Base + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	STSIE Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode. Values: 1'b0: Transmit Packet Available Interrupt Status is disabled 1'b1: Transmit Packet Available Interrupt Status is enabled

Bit	Attr	Reset Value	Description
14	RW	0x0	PKTIE Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. Values: 1'b0: Receive Packet Available Interrupt Status is disabled 1'b1: Receive Packet Available Interrupt Status is enabled
13:12	RW	0x0	FIFOSEL FIFO Selected for Access This field indicates the FIFO selected for debug access: Values: 2'b00: Tx FIFO 2'b01: Tx Status FIFO (only read access when SLVMOD is set) 2'b10: TSO FIFO (cannot be accessed when SLVMOD is set) 2'b11: Rx FIFO
11	RW	0x0	FIFOWREN FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Write is disabled 1'b1: FIFO Write is enabled
10	RW	0x0	FIFORDEN FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Read is disabled 1'b1: FIFO Read is enabled
9	RW	0x0	RSTSEL Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset Pointers of Selected FIFO is disabled 1'b1: Reset Pointers of Selected FIFO is enabled

Bit	Attr	Reset Value	Description
8	RW	0x0	RSTALL Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset All Pointers is disabled 1'b1: Reset All Pointers is enabled
7	RO	0x0	reserved
6:5	RW	0x0	PKTSTATE Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
4	RO	0x0	reserved
3:2	RW	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
1	RW	0x0	DBGMOD Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: 1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO 2. Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: 1. Write access to the Tx FIFO 2. Read access to the Rx FIFO and Tx Status FIFO Values: 1'b0: Debug Mode Access to FIFO is disabled 1'b1: Debug Mode Access to FIFO is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	FDBGEN FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. Values: 1'b0: FIFO Debug Access is disabled 1'b1: FIFO Debug Access is enabled

GMAC_MTL_DBG_STS

Address: Operational Base + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x320	LOCR Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/(DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H.
14:10	RO	0x00	reserved
9	RW	0x0	STSI Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Transmit Status Available Interrupt Status not detected 1'b1: Transmit Status Available Interrupt Status detected
8	RW	0x0	PKTI Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Receive Packet Available Interrupt Status not detected 1'b1: Receive Packet Available Interrupt Status detected
7:5	RO	0x0	reserved
4:3	RO	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid

Bit	Attr	Reset Value	Description
2:1	RO	0x0	PKTSTATE Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
0	RO	0x0	FIFOBUSY FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: 1. All other fields of this register 2. All fields of the MTL_FIFO_Debug_Data register Values: 1'b0: FIFO Busy not detected 1'b1: FIFO Busy detected

GMAC_MTL_FIFO_Debug_Data

Address: Operational Base + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FDBGDATA FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

GMAC_MTL_Interrupt_Status

Address: Operational Base + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	DBGIS Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Debug Interrupt status not detected 1'b1: Debug Interrupt status detected

Bit	Attr	Reset Value	Description
16:1	RO	0x0000	reserved
0	RO	0x0	Q0IS Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Queue 0 Interrupt status not detected 1'b1: Queue 0 Interrupt status detected

GMAC_MTL_TxQ0_Operation_Mode

Address: Operational Base + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes
3:2	RO	0x0	reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled

Bit	Attr	Reset Value	Description
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TxQ0_Underflow

Address: Operational Base + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TxQ0_Debug

Address: Operational Base + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.

Bit	Attr	Reset Value	Description
19	RO	0x0	reserved
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_Q0_Interrupt_Ctrl_Status

Address: Operational Base + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:9	RO	0x00	reserved
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:1	RO	0x00	reserved
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RxQ0_Operation_Mode

Address: Operational Base + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:14	RW	0x00	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	RW	0x00	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD.
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled

Bit	Attr	Reset Value	Description
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled 1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt

Address: Operational Base + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_RxQ0_Debug

Address: Operational Base + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

GMAC_DMA_Mode

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
17:16	RW	0x0	INTM Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: 1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) 2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) 3. sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corre_sponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b11: Reserved Values: 2'b00: See above description 2'b01: See above description 2'b10: See above description 2'b11: Reserved
15:9	RO	0x00	reserved
8	RW	0x0	DSPW Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. Values: 1'b0: Descriptor Posted Write is disabled 1'b1: Descriptor Posted Write is enabled
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	SWR Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Software Reset is disabled 1'b1: Software Reset is enabled

GMAC_DMA_SysBus_Mode

Address: Operational Base + offset (0x1004)

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Values: 1'b0: Low Power Interface (LPI) is disabled 1'b1: Low Power Interface (LPI) is enabled
30	RW	0x0	LPI_XIT_PKT Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. Values: 1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled 1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled
29:26	RO	0x0	reserved
25:24	RW	0x0	WR_OSR_LMT AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: 1. Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ = 4 2. Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ!= 16

Bit	Attr	Reset Value	Description
23:19	RO	0x00	reserved
18:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: 1. Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ = 4 2. Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ!= 16
15:13	RO	0x0	reserved
12	RW	0x0	AAL Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. Values: 1'b0: Address-Aligned Beats is disabled 1'b1: Address-Aligned Beats is enabled
11	RO	0x0	reserved
10	RW	0x0	AALE Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. Values: 1'b0: Automatic AXI LPI is disabled 1'b1: Automatic AXI LPI is enabled
9:4	RO	0x00	reserved
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 16
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 8
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 4

Bit	Attr	Reset Value	Description
0	RW	0x0	FB Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. 1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field 2. Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. Values: 1'b0: Fixed Burst Length is disabled 1'b1: Fixed Burst Length is enabled

GMAC_DMA_Interrupt_Status

Address: Operational Base + offset (0x1008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	MACIS MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. Values: 1'b0: MAC Interrupt Status not detected 1'b1: MAC Interrupt Status detected
16	RO	0x0	MTLIS MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. Values: 1'b0: MTL Interrupt Status not detected 1'b1: MTL Interrupt Status detected
15:1	RO	0x0000	reserved
0	RO	0x0	DC0IS DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. Values: 1'b0: DMA Channel 0 Interrupt Status not detected 1'b1: DMA Channel 0 Interrupt Status detected

GMAC_DMA_Debug_Status0

Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:12	RO	0x0	TPS0 DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Transmit Command issued) 4'b0001: Running (Fetching Tx Transfer Descriptor) 4'b0010: Running (Waiting for status) 4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 4'b0100: Timestamp write state 4'b0101: Reserved for future use 4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 4'b0111: Running (Closing Tx Descriptor)
11:8	RO	0x0	RPS0 DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Receive Command issued) 4'b0001: Running (Fetching Rx Transfer Descriptor) 4'b0010: Reserved for future use 4'b0011: Running (Waiting for Rx packet) 4'b0100: Suspended (Rx Descriptor Unavailable) 4'b0101: Running (Closing the Rx Descriptor) 4'b0110: Timestamp write state 4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory)
7:2	RO	0x00	reserved
1	RO	0x0	AXRHSTS AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. Values: 1'b0: AXI Master Read Channel Status not detected 1'b1: AXI Master Read Channel Status detected
0	RO	0x0	AXWHSTS AXI Master Write Channel or AHB Master Status EQOS-AXI Configuration: When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. EQOS-AHB Configuration: When high, this bit indicates that the AHB master FSMs are in the non-idle state. Values: 1'b0: AXI Master Write Channel or AHB Master Status not detected 1'b1: AXI Master Write Channel or AHB Master Status detected

GMAC_AXI_LPI_Entry_Interval

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	LPIEI LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state. 0 indicates 64 clock cycles.

20.5 Interface Description

Table 20-3 EQOS0 Interface

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac0_rxd2	I	SDMMC1_D0/GMAC0_RXD2/UART6_RX_M0/GPIO2_A3_u	GRF_GPIO2A_IOMUX_SEL_L[14:12]=3'b010
gmac0_rxd3	I	SDMMC1_D1/GMAC0_RXD3/UART6_TX_M0/GPIO2_A4_u	GRF_GPIO2A_IOMUX_SEL_H[2:0]=3'b010
gmac0_rxclk	I	SDMMC1_D2/GMAC0_RXCLK/UART7_RX_M0/GPIO2_A5_u	GRF_GPIO2A_IOMUX_SEL_H[6:4]=3'b010
gmac0_txd2	O	SDMMC1_D3/GMAC0_TXD2/UART7_TX_M0/GPIO2_A6_u	GRF_GPIO2A_IOMUX_SEL_H[10:8]=3'b010
gmac0_txd3	O	SDMMC1_CMD/GMAC0_TXD3/UART9_RX_M0/GPIO2_A7_u	GRF_GPIO2A_IOMUX_SEL_H[14:12]=3'b010
gmac0_txclk	O	SDMMC1_CLK/GMAC0_TXCLK/UART9_TX_M0/GPIO2_B0_d	GRF_GPIO2B_IOMUX_SEL_L[2:0]=3'b010
gmac0_txd0	O	GMAC0_TXD0/UART1_RX_M0/GPIO2_B3_u	GRF_GPIO2B_IOMUX_SEL_L[14:12]=3'b001
gmac0_txd1	O	GMAC0_TXD1/UART1_TX_M0/GPIO2_B4_u	GRF_GPIO2B_IOMUX_SEL_H[2:0]=3'b001
gmac0_txen	O	GMAC0_TXEN/UART1_RTSn_M0/SPI1_CLK_M0/GPIO2_B5_u	GRF_GPIO2B_IOMUX_SEL_H[6:4]=3'b001
gmac0_rxd0	I	GMAC0_RXD0/UART1_CTSn_M0/SPI1_MISO_M0/GPIO2_B6_u	GRF_GPIO2B_IOMUX_SEL_H[10:8]=3'b001
gmac0_rxd1	I	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	GRF_GPIO2B_IOMUX_SEL_H[14:12]=3'b0010
gmac0_rxdvcrs	I	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	GRF_GPIO2C_IOMUX_SEL_H[2:0]=3'b010
gmac0_mclkinout	I/O	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	GRF_GPIO2C_IOMUX_SEL_L[10:8]=3'b010
gmac0_rxer	I	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	GRF_GPIO2C_IOMUX_SEL_H[6:4]=3'b010
gmac0_mdc	O	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	GRF_GPIO2C_IOMUX_SEL_L[14:12]=3'b010
gmac0_mdio	I/O	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	GRF_GPIO2C_IOMUX_SEL_H[2:0]=3'b010

Table 20-4 EQOS1 Interface M0

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac1_txd2m0	O	LCDC_D9/VOP_BT1120_D1/GMAC1_TXD2_M0/I2S3_MCLK_M0/SDMMC2_D1_M1/GPIO3_A2_d	GRF_GPIO3A_IOMUX_SEL_L[10:8]=3'b011
gmac1_txd3m0	O	LCDC_D10/VOP_BT1120_D2/GMAC1_TXD3_M0/I2S3_SCLK_M0/SDMMC2_D2_M1/GPIO3_A3_d	GRF_GPIO3A_IOMUX_SEL_H[14:12]=3'b011
gmac1_rxd2m0	I	LCDC_D11/VOP_BT1120_D3/GMAC1_RXD2_M0/I2S3_LRCK_M0/SDMMC2_D3_M1/GPIO3_A4_d	GRF_GPIO3A_IOMUX_SEL_H[2:0]=3'b011
gmac1_rxd3m0	I	LCDC_D12/VOP_BT1120_D4/GMAC1_RXD3_M0/I2S3_SDO_M0/SDMMC2_CMD_M1/GPIO3_A5_d	GRF_GPIO3A_IOMUX_SEL_H[6:4]=3'b011
gmac1_txclkm0	O	LCDC_D13/VOP_BT1120_CLK/GMAC1_TXCLK_M0/I2S3_SDI_M0/SDMMC2_CLK_M1/GPIO3_A6_d	GRF_GPIO3A_IOMUX_SEL_H[10:8]=3'b011
gmac1_rxclkm0	I	LCDC_D14/VOP_BT1120_D5/GMAC1_RXCLK_M0/SDMMC2_DET_M1/GPIO3_A7_d	GRF_GPIO3A_IOMUX_SEL_H[14:12]=3'b011
gmac1_rxd0m0	I	LCDC_D16/VOP_BT1120_D7/GMAC1_RXD0_M0/UART4_RX_M1/PWM8_M0/GPIO3_B1_d	GRF_GPIO3B_IOMUX_SEL_L[6:4]=3'b011
gmac1_rxd1m0	I	LCDC_D17/VOP_BT1120_D8/GMAC1_RXD1_M0/UART4_TX_M1/PWM9_M0/GPIO3_B2_d	GRF_GPIO3B_IOMUX_SEL_L[10:8]=3'b011
gmac1_rxdvcrsm0	I	LCDC_D18/VOP_BT1120_D9/GMAC1_RXDV_CRS_M0/I2C5_SCL_M0/PDM_SDI0_M2/GPIO3_B3_d	GRF_GPIO3B_IOMUX_SEL_L[14:12]=3'b011
gmac1_rxerm0	I	LCDC_D19/VOP_BT1120_D10/GMAC1_RXER_M0/I2C5_SDA_M0/PDM_SDI1_M2/GPIO3_B4_d	GRF_GPIO3B_IOMUX_SEL_H[2:0]=3'b011
gmac1_txd0m0	O	LCDC_D20/VOP_BT1120_D11/GMAC1_TXD0_M0/I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d	GRF_GPIO3B_IOMUX_SEL_H[6:4]=3'b011
gmac1_txd1m0	O	LCDC_D21/VOP_BT1120_D12/GMAC1_TXD1_M0/I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d	GRF_GPIO3B_IOMUX_SEL_H[10:8]=3'b011

gmac1_txenm0	O	LCDC_D22/PWM12_M0/GMAC1_TXEN_M0/UART3_TX_M1/PDM_SDI2_M2/GPIO3_B7_d	GRF_GPIO3B_IOMUX_SEL_H[14:12]=3'b011
gmac1_mclkinoutm0	I/O	LCDC_D23/PWM13_M0/GMAC1_MCLKINOUT_M0/UART3_RX_M1/PDM_SDI3_M2/GPIO3_C0_d	GRF_GPIO3C_IOMUX_SEL_L[2:0]=3'b011
Management interface			
mac_mdio_m0	I/O	PWM14_M0/VOP_PWM_M1/GMAC1_MDC_M0/UART7_TX_M1/PDM_CLK1_M2/GPIO3_C4_d	GRF_GPIO3C_IOMUX_SEL_H[2:0]=3'b011
gmac1_mdcm0	O	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	GRF_GPIO3C_IOMUX_SEL_H[6:4]=3'b011

Table 20-5 EQOS1 Interface M1

Module Pin	Dir.	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac1_txd2m1	O	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1/UART1_TX_M1/PDM_CLK0_M1/GPIO3_D6_d	GRF_GPIO3D_IOMUX_SEL_H[10:8]=3'b011
gmac1_txd3m1	O	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M1/UART1_RX_M1/PDM_SDI0_M1/GPIO3_D7_d	GRF_GPIO3D_IOMUX_SEL_H[14:12]=3'b011
gmac1_txclkm1	O	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1/PDM_CLK1_M1/GPIO4_A0_d	GRF_GPIO4A_IOMUX_SEL_L[2:0]=3'b011
gmac1_rxd2m1	I	CIF_D11/EBC_SDDO11/GMAC1_RXD2_M1/PDM_SDI1_M1/GPIO4_A1_d	GRF_GPIO4A_IOMUX_SEL_L[6:4]=3'b011
gmac1_rxd3m1	I	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1/UART7_TX_M2/PDM_SDI2_M1/GPIO4_A2_d	GRF_GPIO4A_IOMUX_SEL_L[10:8]=3'b011
gmac1_rxclkm1	I	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1/UART7_RX_M2/PDM_SDI3_M1/GPIO4_A3_d	GRF_GPIO4A_IOMUX_SEL_L[14:12]=3'b011
gmac1_txd0m1	O	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	GRF_GPIO4A_IOMUX_SEL_H[2:0]=3'b011
gmac1_txd1m1	O	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	GRF_GPIO4A_IOMUX_SEL_H[6:4]=3'b011
gmac1_txenm1	O	ISP_FLASHTRIGOUT/EBC_SDCE0/GMAC1_TXEN_M1/SPI3_CS0_M0/I2S1_SCLK_RX_M1/GPIO4_A6_d	GRF_GPIO4A_IOMUX_SEL_H[10:8]=3'b011
gmac1_rxd0m1	I	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1/SPI3_CS1_M0/I2S1_LRCK_RX_M1/GPIO4_A7_d	GRF_GPIO4A_IOMUX_SEL_H[14:12]=3'b011
gmac1_rxd1m1	I	CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1/SPI3_MISO_M0/I2S1_SDO1_M1/GPIO4_B0_d	GRF_GPIO4B_IOMUX_SEL_L[2:0]=3'b011
gmac1_rxdvcrsm1	I	ISP_PRELIGHT_TRIG/EBC_SDCE3/GMAC1_RXDV_CRS_M1/I2S1_SDO2_M1/GPIO4_B1_d	GRF_GPIO4B_IOMUX_SEL_L[6:4]=3'b011
gmac1_rxerm1	I	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1/SPI3_MOSI_M0/I2S2_SDI_M1/GPIO4_B2_d	GRF_GPIO4B_IOMUX_SEL_L[10:8]=3'b011
Management interface			
gmac1_mdcm1	O	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTSn_M1/I2S2_MCLK_M1/GPIO4_B6_d	GRF_GPIO4B_IOMUX_SEL_H[10:8]=3'b011
gmac1_mdiom1	I/O	CIF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1/I2S2_SCLK_TX_M1/GPIO4_B7_d	GRF_GPIO4B_IOMUX_SEL_H[14:12]=3'b011

20.6 Application Note

20.6.1 Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.
The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The GMAC supports the ring structure for the DMA descriptor.

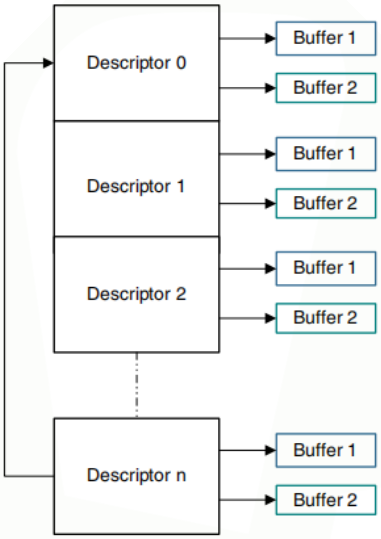


Fig. 20-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.
The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached.
For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

20.6.2 Transmit Descriptors

The DMA in GMAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis.
The Transmit Normal descriptor has two formats: Read format and Write-Back format.

20.6.3 Transmit Normal Descriptor (Read Format)

Table 20-6 TDES0 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 20-7 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16-bits of the Buffer 1 Address Pointer.

Table 20-8 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/T MWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option

Bit	Name	Description
		should be used only with the VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core
13:0	HL or B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 20-9 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit

Bit	Name	Description
		(TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. ■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address

Bit	Name	Description
		■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. ■ 2'b11: Reserved These bits are valid in the EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNUM or THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled. ■ 2'b10: IP header checksum and payload checksum calculation and

Bit	Name	Description
		insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0.

20.6.4 Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet.
this format is only applicable to the last descriptor of a packet.

Table 20-10 TDES0 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set

Table 20-11 TDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 20-12 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Rsvd	Reserved

Table 20-13 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:24	Rsvd	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be:

Bit	Name	Description
		■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet ■ All 1s ■ CTXT, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:18	Rsvd	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC.
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier ■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This

Bit	Name	Description
		bit is set only when the JD bit of the MAC_Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.

Bit	Name	Description
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

20.6.5 Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step

timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit

Table 20-14 TDES0 Context Descriptor

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 20-15 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 20-16 TDES2 Context Descriptor

Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Rsvd	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 20-17 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.

Bit	Name	Description
30	CTXT	Context Type This bit should be set to 1'b1 for Context descriptor.
29:28	Rsvd	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	Rsvd	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet ■ All 1s ■ CD, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status Register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:20	Rsvd	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits:

Bit	Name	Description
		■ 2'b00: Do not add the inner VLAN tag. ■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames. These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

20.6.6 Receive Descriptors

The DMA in GMAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.
The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

20.6.7 Receive Normal Descriptors(Read Format)

Table 20-18 TDES0 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	BUF1AP	Header or Buffer 1 Address Pointer

Bit	Name	Description
		When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet. The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer. If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width.

Table 20-19 TDES1 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 20-20 TDES2 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 20-21 TDES3 Normal Descriptor(Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Rsvd	Reserved

Bit	Name	Description
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Rsvd	Reserved

20.6.8 Receive Normal Descriptors(Write-Back Format)

Table 20-22 TDES0 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 20-23 TDES1 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid

Bit	Name	Description
		only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types) ■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP.

Bit	Name	Description
		Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following: ■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP/AV payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ 3'b110: AV Tagged Data Packet ■ 3'b111: AV Tagged Control Packet ■ 3'b101: AV Untagged Control Packet ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 20-24 TDES2 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched

Bit	Name	Description
		These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: ■ 000: Filter 0 ■ 001: Filter 1 ■ 010: Filter 2 ■ 011: Filter 3 ■ 100: Filter 4 ■ 101: Filter 5 ■ 110: Filter 6 ■ 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. Note: This status is not available when Flexible RX Parser is enabled.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by

Bit	Name	Description
		the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. Note: This status is not available when Flexible RX Parser is enabled.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value. Note: This status is not available when Flexible RX Parser is enabled.
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. Note: When this bit is set, ES bit of RDES3 is also set.
16	SAF/RXPD	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. Note: When this bit is set, ES bit of RDES3 is also set.
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when DWC_EQOS_ERVFE is not enabled. If DWC_EQOS_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames.
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when DWC_EQOS_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled. For more information, see the Filter Status topic.
13:11	Rsvd	Reserved
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP

Bit	Name	Description
		Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time). This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header. boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.

Table 20-25 TDES3 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} ■ 2'b00: Intermediate Descriptor ■ 2'b01: First Descriptor ■ 2'b10: Reserved ■ 2'b11: Descriptor Error (due to all 1s) Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not

Bit	Name	Description
		marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). Note: Giant packet indicates only the packet length. It does not cause any packet truncation.
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error

Bit	Name	Description
		When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO.
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error when this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: ■ 3'b000: The packet is a length packet ■ 3'b001: The packet is a type packet. ■ 3'b011: The packet is a ARP Request packet type ■ 3'b100: The packet is a type packet with VLAN Tag ■ 3'b101: The packet is a type packet with Double VLAN Tag ■ 3'b110: The packet is a MAC Control packet type ■ 3'b111: The packet is a OAM packet type ■ 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set.

Bit	Name	Description
14	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

20.6.9 Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 20-26 TDES0 Context Descriptor

Bit	Name	Description
31:0	RSTL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 20-27 TDES1 Context Descriptor

Bit	Name	Description
31:0	RSTH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.

Table 20-28 TDES2 Context Descriptor

Bit	Name	Description
31:0	Rsvd	Reserved

Table 20-29 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception

Bit	Name	Description
		■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate a descriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2'b00: Reserved ■ 2'b01: Reserved ■ 2'b10: Context Descriptor ■ 2'b11: Descriptor Error Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.
28:0	Rsvd	Reserved

20.6.10 Programming Guide

20.6.10.1 Initializing DMA

Complete the following steps to initialize the DMA:
1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:
a. AAL
b. Fixed burst or undefined burst
c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.
d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])
4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section "Descriptors".
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= DWC_EQOS_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <= DWC_EQOS_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1) and

DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= DWC_EQOS_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:
- DMA_CH(#i)_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of the DMA_CH(#i)_RX_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1) register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

20.6.10.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 and MTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

20.6.10.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter
d. Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrl register:
a. Pause time and other Pause frame control bits
b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.

5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

20.6.10.4 Performing Normal Receive and Transmit Operation

During normal operation of the GMAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:
1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc and DMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

20.6.10.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_EQOS_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

20.6.10.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during GMAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.
6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register and MAC_System_Time_Nanoseconds_Update Register with the appropriate time value.
8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.

b. Program registers MAC_Timestamp_Ingress_Asym_Corr and MAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

20.6.10.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Update registers (MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

20.6.10.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet. Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

20.6.11 Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure. The mux selecting rmii_speed is CRU_CLKSEL_CON31[2]/ CRU_CLKSEL_CON31[2].

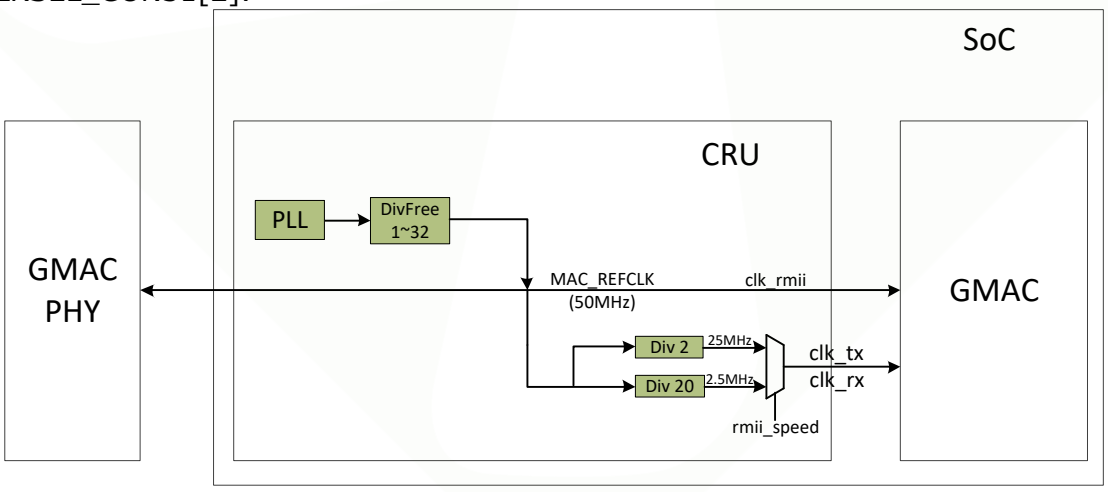


Fig. 20-11 RMII Clock Architecture When Clock Source From CRU

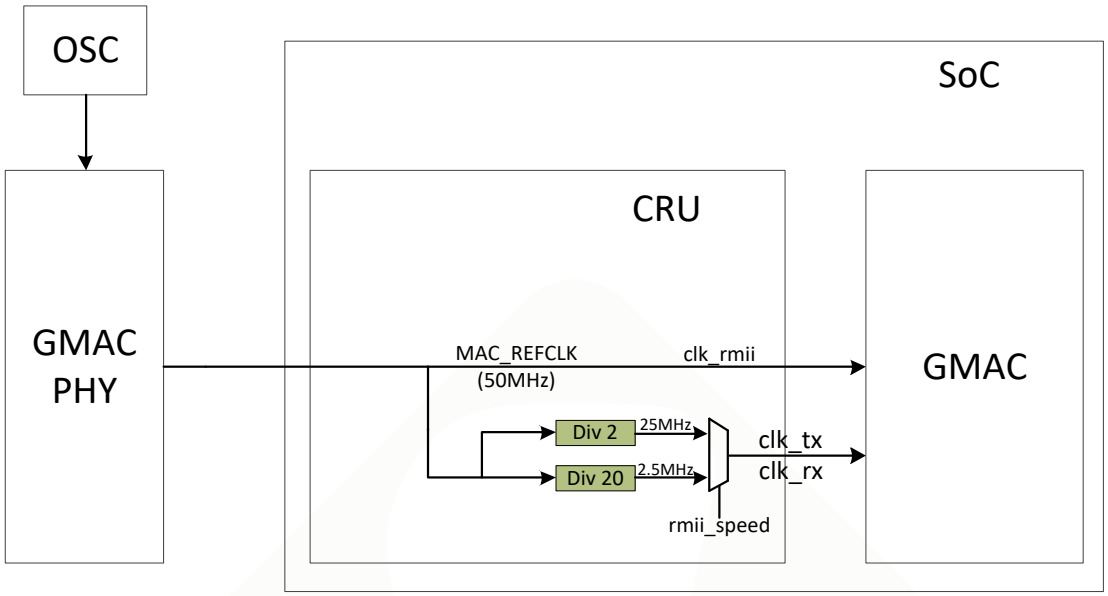


Fig. 20-12 RMII Clock Architecture When Clock Source From External OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure.In order to dynamically adjust the timing between TX/RX clocks with data, delayline is integrated in TX and RX clock path. Register GRF_MAC0_CON1[1:0]/GRF_MAC1_CON1[1:0] can enable the delayline and GRF_MAC0_CON0[15:0]/GRF_MAC1_CON0[15:0] is used to determine the delay length. There are 200 delay elements in each delayline.

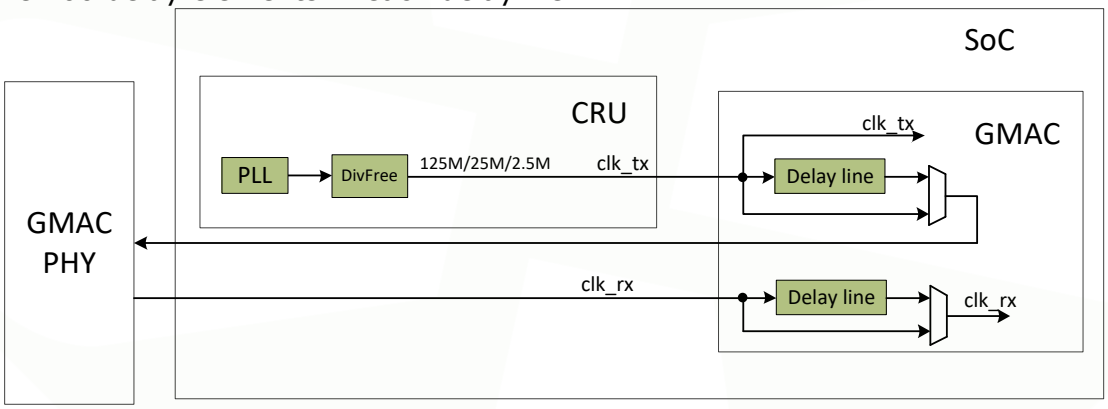


Fig. 20-13 RGMII Clock Architecture When Clock Source From CRU

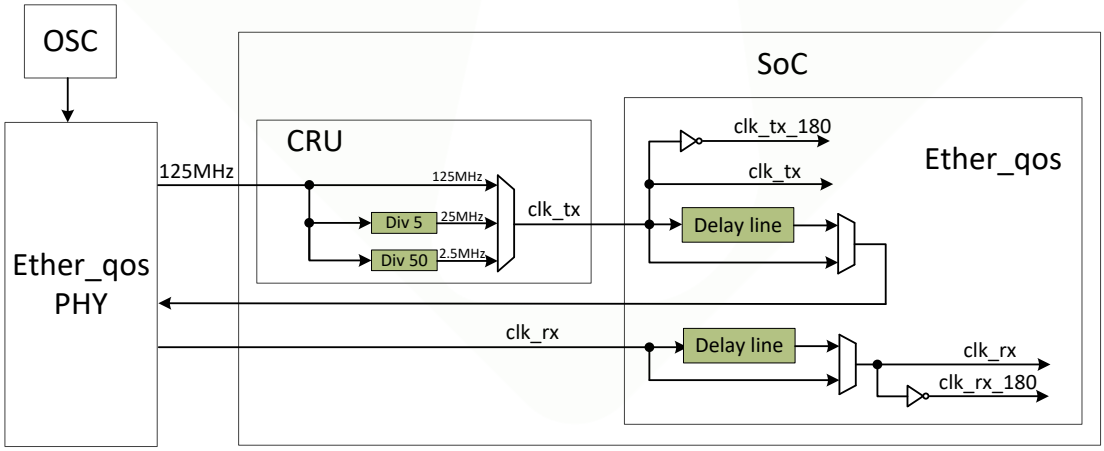


Fig. 20-14 RGMII Clock Architecture When Clock Source From External OSC

Chapter 21 QSGMII/SGMII_PCS

21.1 Overview

The Physical Coding Sublayer (PCS) layer provides an interface between the Media Access Control (MAC) and Physical Medium Attachment Sublayer (PMA) through a Media independent interface.

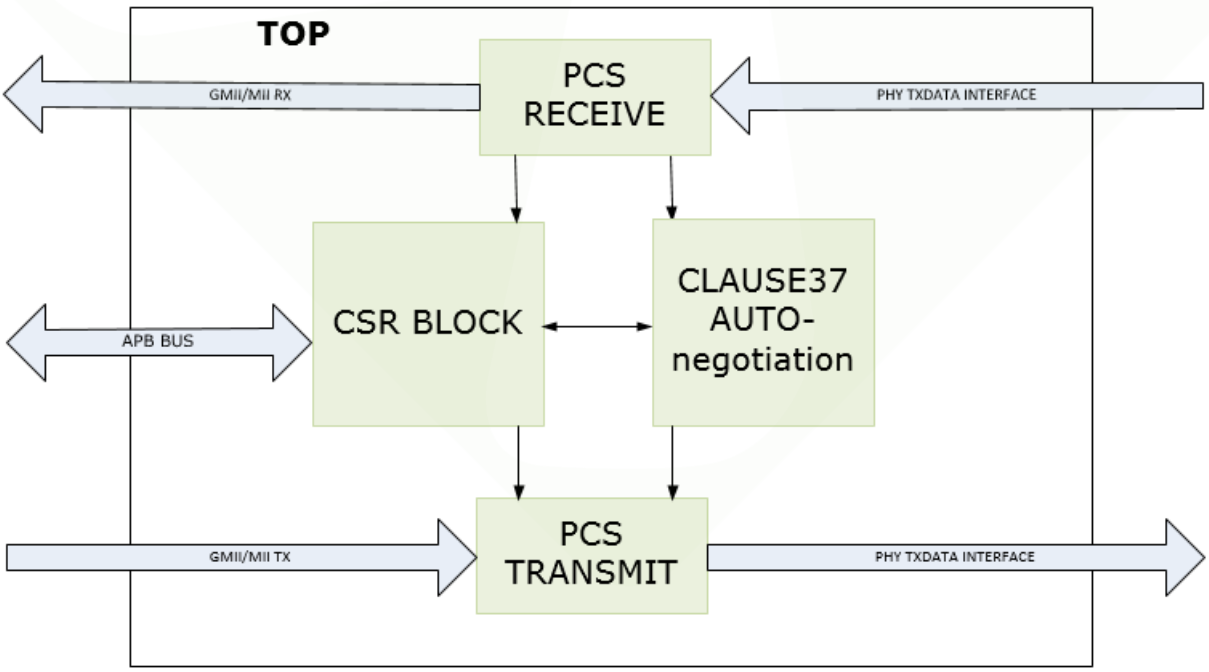
The following features are implemented in the QSGMII/SGMII_PCS:

- 1000BASE-X support
- Clause 37 auto-negotiation support in 1G mode
- SGMII/QSGMII interface support
- AMBA APB-3 (32-bit register) configuration management interface
- GMII interface Mac interface
- Configurable Device and Package Identifier (OUI numbers)
- Vendor-specific Register sets (VR) to control the PCS functions
- HFTP, LFTP and MFTP test pattern generation in 1000BASEX_Only PCS mode
- Clock Rate compensation of 200ppm (+/- 100 ppm) on the Receive MAC interface
- Energy Efficient Ethernet Support
- Supports loopback control from the PHY Transmit to the PHY Receive lane
- Supports various error status signals and statistics for monitoring and debugging.
- Provides programmable control to reduce the simulation time by reducing the timer values defined in the IEEE standard.
- Provides programmable Device or Package identifiers (OUI numbers as defined in IEEE Std 802.3).
- Provides programmable features to dynamically enable or disable MMD devices present in some configurations.
- Supports various error status signals and statistics for monitoring and debugging.

21.2 Function Description

21.2.1 QSGMII/SGMII_PCS Block Diagram

Fig. 21-1 illustrates the functional blocks of QSGMII/SGMII_PCS.



21.2.2 PCS Transmit Block

The PCS Transmit block implements the following functions:

- Support GMII interface in 1000BASE-X
- Performs 8B/10B data encoding
- Generates Idle pattern (as defined in Clause 36 for 1000BASE-X)
- Generates the following test patterns defined in IEEE Std 802.3
- Provides lane disable control for Lane 3, Lane 2, and Lane 1

21.2.3 PCS Receive Block

The PCS Transmit block implements the following functions:

- Support GMII interface in 1000BASE-X
- Performs code group alignment on each lane
- Performs 8B/10B data decoding on each lane
- Generates Idle pattern (as defined in Clause 36 for 1000BASE-X)
- Generates the following test patterns defined in IEEE Std 802.3
- Provides lane disable control for Lane 3, Lane 2, and Lane 1

21.2.4 Clause 37 Auto-Negotiation

The QSGMII/SGMII_PCS supports auto-negotiation in the 1000BASE-X and SGMII/QSGMII modes. Auto-negotiation enables the QSGMII/SGMII_PCS to do the following:

- Advertise its speed, duplex mode (full-duplex or half-duplex), and flow control capabilities.
- Acquire capabilities of its remote partner and link status to converge on a common operating mode and flow-control mechanism.

This block performs the following functions:

- Recognizes or generates the |C| order set
- Supports the SGMII and 1000BASE-X Clause 37 auto-negotiation protocol

1.2.4.1 Description of Clause 37 Auto-Negotiation

The Clause 37 auto-negotiation is enabled by default when Mode of Operation (MAIN_MODE) is 1000BASEX-Only PCS. The QSGMII/SGMII_PCS supports the IEEE-defined MII and auto-negotiation registers as defined in Clause 22 and Clause 37. The Clause 37 auto-negotiation is based on the PCS /C/ order set shown in Table 1-1

/C/	Configurtation	Number of Code Groups	Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg

Table 21-1 Configuration Order Sets

The /C/ order set is sent or received during auto-negotiation. The link partners exchange information in a 16-bit word known as configuration register (Config_Reg) which is a part of the /C/ order set. The link partners first exchange the Config_Reg Base Page, and then may exchange the Config_Reg Next Page.

21.2.5 Serial Gigabit Media Independent Interface (SGMII)

The Serial Gigabit Media Independent Interface (SGMII) converts the GMII or MII interface, between the Gigabit MAC and the Gigabit PHY, to a serial interface. Using the SGMII interface lowers the pin count required for the GMII interface. However, the reduced pin count may increase the power consumption because the SGMII interface maintains a constant 1250 Mbps data rate, irrespective of the operating speed of the MAC.

The SGMII block has the following features:

- Supports 10 Mbps, 100 Mbps, and 1000 Mbps speed modes.
  The QSGMII/SGMII_PCS uses the RAL blocks to convert the data (with different speed and data width) from the MAC to the internal speed of 125 MHz, 8-bit required for the SGMII link speed (1.25 Gbps).
- Provides status signals (link speed, duplex mode, and link status) from the PHY to the MAC.

The SGMII interface uses the Clause 37 auto-negotiation to know the speed, duplex mode, and link status negotiated by the PHY. To enable the Clause 37 auto-negotiation in the SGMII mode, you need to program Bits[2:1] of the VR_MII_AN_CTRL to 2'b10.

1.2.5.1 SGMII Auto-Reconfiguration

QSGMII/SGMII_PCS supports automatic reconfiguration of SGMII speed/duplex mode based on the outcome of auto-negotiation. This feature can be enabled by programming bit[9] (MAC_AUTO_SW) of VR_MII_DIG_CTRL1 when operating in SGMII MAC mode. QSGMII/SGMII_PCS is initially configured in the speed/duplex mode as programmed in the SR_MII_CTRL. If MAC_AUTO_SW bit is enabled, QSGMII/SGMII_PCS automatically switches to the negotiated speed mode after the completion of CL37 Auto-negotiation. This eliminates the software over-head of reading CL37 AN SGMII Status from VR_MII_AN_INTR_STS and then programming SS13 and SS6 speed-selection bits of SR_MII_CTRL appropriately.
When QSGMII/SGMII_PCS is configured in PHY Mode and if bit[0] (PHY_MODE_CTRL) of VR_MII_DIG_CTRL1 is set to 1, QSGMII/SGMII_PCS configures itself to the speed/duplex mode as indicated by PCS_sgmii_link_speed_i[1:0] and PCS_sgmii_full_duplex_i inputs (which are provided by the underlying copper PHY). In addition, when there is a change in any of these inputs QSGMII/SGMII_PCS intiates/restarts SGMII auto-negotiation.
The SGMII Link speed, duplex mode, and link status are indicated on the PCS_link_speed_o, PCS_sgmii_full_duplex_o, and PCS_sgmii_link_sts_o output ports respectively. These ports reflect the values as shown in Table 1-2 based on the selected configuration/register settings.

21.2.6 Quad SGMII (QSGMII)

Quad Serial Gigabit Media Independent Interface is an extension of SGMII. QSGMII interface transfers data between a 4-port Gigabit MAC (or 4 separate MACs) and a 4-port Gigabit PHY (or 4 separate PHYs) over a serial line operating at 5Gbps. QSGMII eliminates the need to have 4 separate GMII or MII interfaces between the MAC and PHY and reduces the pin count considerably. Each port can operate at a data rate of 10/100/100Mbps. QSGMII Mode can be enabled in QSGMII/SGMII_PCS by programming bits[2:1] of VR MII MMD AN Control Register to 2'b11.
Figure 20-2 the components of QSGMII Transmitter.

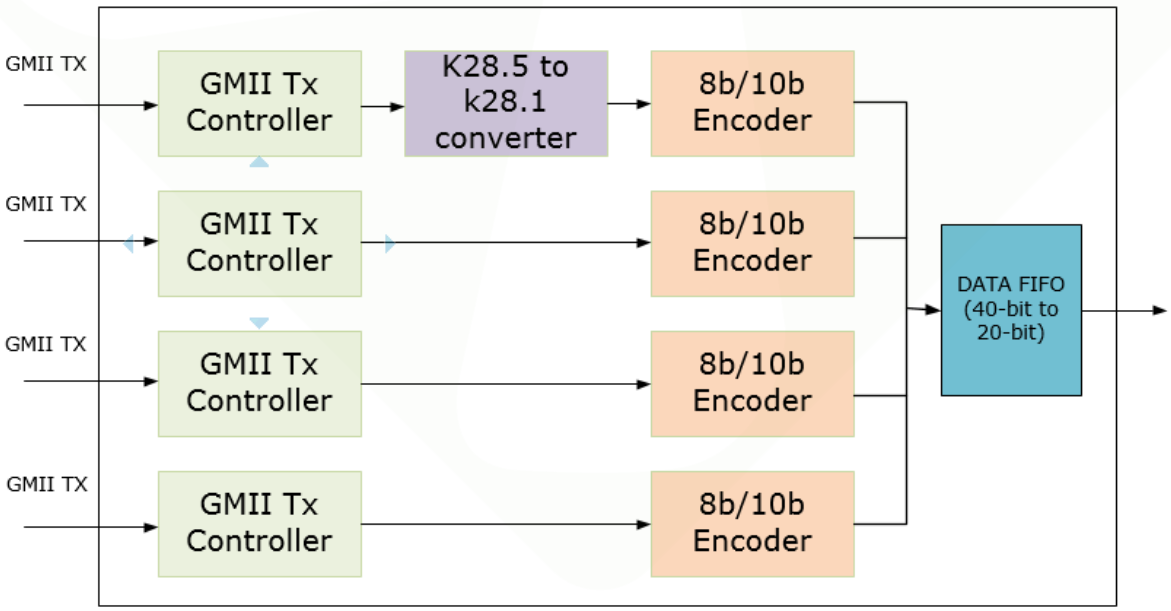


Fig. 21-2 QSGMII Transmitter Architecture

Fig. 20-3 the components of QSGMII Receiver.

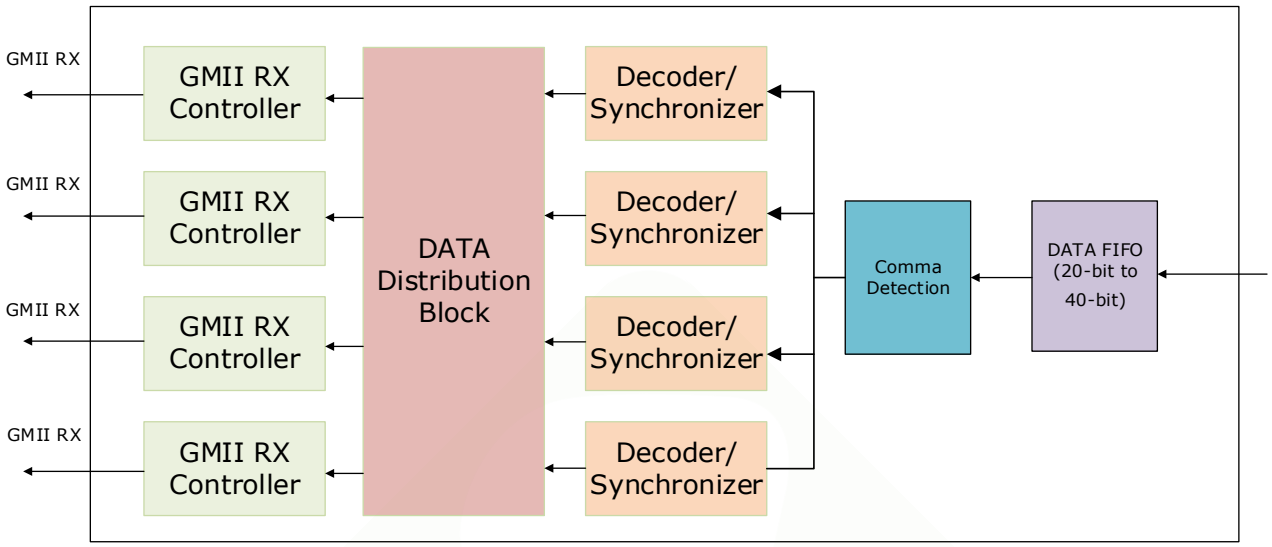


Fig. 21-3 QSGMII Receiver Architecture

QSGMII/SGMII_PCS supports the following features in QSGMII mode:

- Supports 10 Mbps, 100 Mbps and 1000 Mbps along each port

  QSGMII/SGMII_PCS uses the RAL blocks at each of the 4 GMII/MII interface to convert the data (with different speed and data width) from the MACs to 8-bit data operating at 125MHz. In the transmit path, the data from the four MAC ports are time-division multiplexed, processed suitably (as defined by the specification) and finally converted to 20-bit data at 250MHz to interface with the SERDES. As per QSGMII specification, K28.5 pattern is replaced with K28.1 pattern in the data sent from port 0 MAC. In the receive path, QSGMII/SGMII_PCS receives 20-bit data at 250MHz from the SERDES. The received data is processed suitably, de-multiplexed and separated-out into 4 separate data traffics. The K28.1 character plays a key role in ensuring that the received data traffic is routed correctly to the intended GMII/MII port.

- Supports Clause 37 auto-negotiation for each port

  Each of the 4 ports can make use of QSGMII auto-negotiation (based on IEEE802.3-Clause 37) to exchange the speed, duplex mode and the link status with the link partner. Auto-negotiation operation along one port is independent of the other ports. QSGMII/SGMII_PCS can be used either at MAC end of QSGMII link (TX_CONFIG=0) or at the PHY end. The auto-negotiation operation is similar to that of SGMII and involves the exchange of /C/ order sets.

21.2.7 EEE Controller

Energy Efficient Ethernet, specified in IEEE Std 802.3az-2010, helps to save energy or reduce power consumption in the PHY when no data transmission or reception is required for a very long duration. The basic principle of this feature is that when the MAC transmitter indicates that it does not have any data to transmit, the local transmitter (which includes the PCS and the PHY) and the remote-end PHY receiver can be put in the power-save or sleep mode to save energy.

1.2.7.1 EEE Transmit Controller

The QSGMII/SGMII_PCS Transmit path implements the following functions when the EEE support is selected:

- Monitor the XGMII or GMII interface for Low Power Idle (LPI) pattern
- Maintain the following EEE states in the Transmit path:
  - Sleep (LPI request monitoring state)
  - Quiet (Power-save state)
  - Alert (Pre-wakeup state) in the PCS-R mode
  - Wakeup (Refresh state)

The Transmit LPI flow is triggered when the MAC drives the LPI signals on the XGMII or GMII interface. The QSGMII/SGMII_PCS maintains various states in which it periodically includes refresh signaling and freezing the transmitter in the quiet state. By maintaining this predefined sequence, the protocol ensures that the link is alive and at the same time power is saved. When the MAC stops sending the LPI pattern (and starts sending the IDLE pattern), the EEE Transmit controller also comes out of this sequence and reverts to the IDLE (or normal transmit) state.
The timers used in the EEE Transmit Controller have the default values given in the IEEE standard. You can change these default values (within a range) according to your requirement.

Figure 1-4 describes the Transmit LPI flow on the GMII Interface. The MAC triggers the LPI mode in the QSGMII/SGMII_PCS by driving the following:

- gmii_txd_i[7:0] = 8'h01, gmii_en_i = 0, and gmii_tx_er_i = 1 when GMII port is present in your configuration
- xgmii_txd_i[7:0] = 8'h01, xgmii_txc_i[0] = 0, and xgmii_txc_i[1] = 1 when the GMII interface is shared with the XGMII pins in your configuration

If the clk_xgmii_tx_i or clk_mii_tx_i clock (SGMII mode) is used in the QSGMII/SGMII_PCS to sample GMII, theMAC can gate the clk_xgmii_tx_i or clk_mii_tx_i clock after 9 clocks of asserting the LPI Idle. If the clk_xgxs_i or clk_rpcs_tx_i clock is used to sample GMII, clock gating based on the MAC is not applicable.

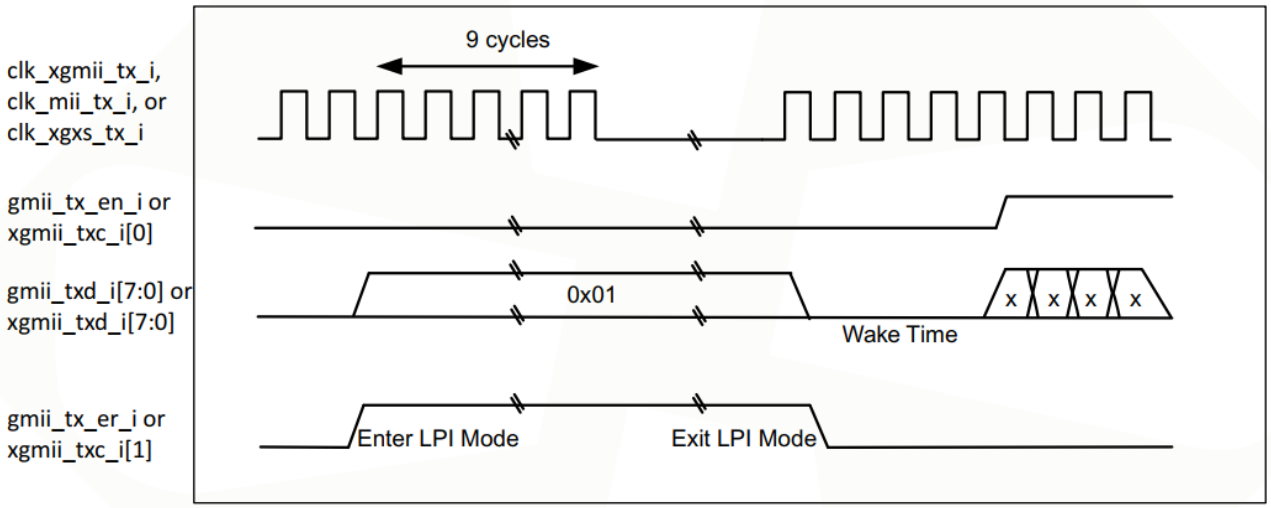


Fig. 21-4 1G MAC Transmit LPI

1.2.7.2 Transparent LPI Mode

In addition to the standard EEE Mode, QSGMII/SGMII_PCS supports the transparent LPI Mode in its transmit path. In this mode, EEE operation involves mere encoding of LPI patterns (received on on XGMII/GMII Tx interface) and sending it to the SERDES. On detecting Lower-Power Idle on XGMII/GMII Tx interface, QSGMII/SGMII_PCS goes to the TX_SLEEP state and remains in this state till MAC stops sending LPI. It does not transition to TX_QUIET state. This mode does not involve gating-off of any clocks to QSGMII/SGMII_PCS. In addition, the serdes transmitter is not disabled (PCS_tx_data_en_o signal remains high). MAC should ensure that it does not gate-off XGMII/GMII Tx clock to QSGMII/SGMII_PCS during this mode of operation.
This mode can be enabled by programming 'TRN_LPI' bit of VR XS or PCS MMD EEE Mode Control 1 Register (or VR MII MMD PCS MMD EEE Mode Control 1 Register for 1000BaseX-Only PCS configurations) in addition to 'LTX_EN' bit of VR XS or PCS MMD EEE Mode Control 0 Register.

1.2.7.3 EEE Receive Controller

The PCS Receive path implements the following functions when the EEE support is selected:

- Decode the received LPI code group from the link partner.
- Maintain the following EEE states in the Receive path:
  - Sleep (LPI request monitoring state)

- Quiet (Power-Save state)
- Wake (Refresh state)
- Wake-up Fault (Error Monitoring)

The sequence in the state machine helps in saving the power in the PHY or PCS because some of the functional blocks can be switched off in the Quiet state. In addition, during Refresh state, the Rx path is re-synchronized so that it can monitor the link status. The timers used in the EEE Rx Controller have the default values as given in the IEEE standard. You can change these default values (within a range) according to your requirement.
The Rx low power mode is triggered when the QSGMII/SGMII_PCS receives the LPI Idle code group on the link. It exits the LPI mode when the link partner stops transmitting the LPI Idle code groups.
The Rx LPI mode is triggered when the QSGMII/SGMII_PCS receives the LPI from the link partner. After successful decoding, the controller enters the Sleep state and drives the LPI patterns on the Rx XGMII signals as shown in the Figure 1-5. the following LPI pattern is driven to the MAC on GMII:

- gmii_rxd_o[7:0] or xgmii_rxd_o[7:0] = 8'h06
- gmii_rx_dv_o or xgmii_rxd_o[0] = 0
- gmii_rx_er_o or xgmii_rxd_o[1] = 1

In this mode, the PCS_lrx_clk_gat_o signal is asserted after the 9 clocks of driving the LPI pattern on the GMII interface. It can be used to gate off the clocks on the GMII Rx interface on the MAC and the QSGMII/SGMII_PCS. The 9 clock duration can be increased by programming Bits[15:12] of VR_XS_PCS_EEE_MCTRL0 RegisterVR PCS MMD EEE Mode Control Register.

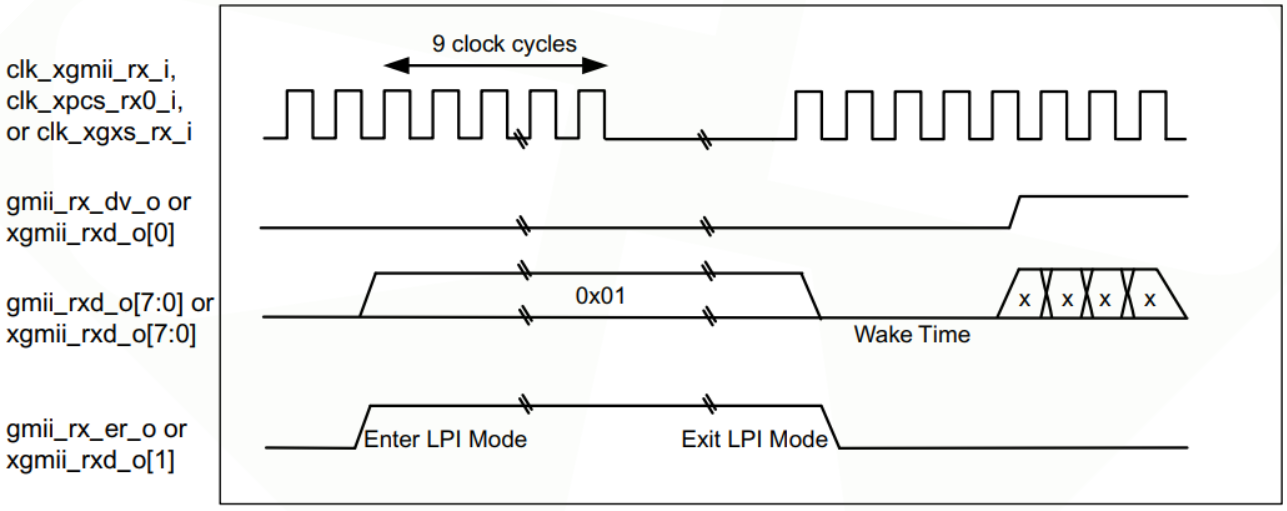


Fig. 21-5 1G MAC Receive LPI

21.2.8 Reset Generation

The reset generation block generates the reset for other blocks of the QSGMII/SGMII_PCS. The QSGMII/SGMII_PCS supports the following types of reset:

- Hardware Reset
  You can issue the hardware reset by asserting the pwr_on_rst_n signal. When this reset is asserted, all internal blocks of the QSGMII/SGMII_PCS are reset. In addition, the PCS_reset_n_o signal is asserted to reset
- Standard Soft Reset
  You can issue the standard soft reset by setting Bit 15 of the following registers:
  - SR_PMA_CTRL1 Register
  - SR_XS_PCS_CTRL1 Register or SR PCS MMD Control1 Register
  - SR_AN_CTRL Register

- SR_MII_CTRL Register

The QSGMII/SGMII_PCS clears this bit after 32 clocks cycles of the clk_csr_i clock. When this reset bit is set, all internal blocks of the QSGMII/SGMII_PCS, except the Management Interface block, get reset. In addition, the PCS_reset_n_o signal is asserted to reset the PHY.

- Power-Down Mode

You can issue the power-down mode by setting Bit 11 of the following registers:

- VR_MII_AN_CTRL
- VR_XS_PCS_DIG_CTRL1 Register or VR PCS MMD Digital Control1 Register
- VR_AN_DIG_CTRL1 Register or VR AN MMD Digital Control1 Register
- VR_MII_DIG_CTRL1 Register or VR MII MMD Digital Control1 Register

When this bit is set, the host needs to clear this bit when it wants to power up the QSGMII/SGMII_PCS. When this bit is set, all internal blocks of the QSGMII/SGMII_PCS are reset, except the Management Interface block and the CSR block. The PCS_reset_n_o output is not asserted during the power-down mode.

21.3 Register Description

21.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

21.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
QSGMII/SGMII_PCS_SR_MII_1_CTRL	0x080000	W	0x00000140	SR MII_1 MMD Control Register
QSGMII/SGMII_PCS_SR_MII_1_STS	0x080004	W	0x00000109	SR MII_1 MMD Status Register
QSGMII/SGMII_PCS_SR_MII_1_DEV_ID1	0x080008	W	0x00007996	SR MII_1 MMD Device Identifier Register 1
QSGMII/SGMII_PCS_SR_MII_1_DEV_ID2	0x08000C	W	0x0000CC00	SR MII_1 MMD Device Identifier Register 2
QSGMII/SGMII_PCS_SR_MII_1_AN_ADV	0x080010	W	0x00000020	SR MII_1 MMD AN Advertisement Register
QSGMII/SGMII_PCS_SR_MII_1_LP_BABL	0x080014	W	0x00000000	SR MII_1 MMD AN Link Partner Base Ability Register
QSGMII/SGMII_PCS_SR_MII_1_AN_EXPN	0x080018	W	0x00000000	SR MII_1 MMD AN Expansion Register
QSGMII/SGMII_PCS_SR_MII_1_EXT_STS	0x08003C	W	0x0000C000	SR MII_1 MMD Extended Status Register
QSGMII/SGMII_PCS_VR_MII_1_DIG_CTRL1	0x0A0000	W	0x00002400	VR MII_1 MMD Digital Control1 Register
QSGMII/SGMII_PCS_VR_MII_1_AN_CTRL	0x0A0004	W	0x00000000	VR MII_1 MMD AN Control Register
QSGMII/SGMII_PCS_VR_MII_1_AN_INTR_STS	0x0A0008	W	0x00000000	VR MII_1 MMD AN Interrupt and Status Register
QSGMII/SGMII_PCS_VR_MII_1_TC	0x0A000C	W	0x00000000	VR MII_1 MMD Test Control Register.
QSGMII/SGMII_PCS_VR_MII_1_DBG_CTRL	0x0A0014	W	0x00000000	VR MII_1 MMD Debug Control Register
QSGMII/SGMII_PCS_VR_MII_1_EEE_MCTRL0	0x0A0018	W	0x0000899C	VR MII_1 MMD EEE Mode Control Register

Name	Offset	Size	Reset Value	Description
QSGMII/SGMII_PCS_VR_MII_1_EEE_TXTIMER	0x0A0020	W	0x00000000	VR MII_1 MMD EEE Tx Timer Register
QSGMII/SGMII_PCS_VR_MII_1_EEE_RXTIMER	0x0A0024	W	0x00000000	VR MII_1 MMD EEE Rx Timer Register
QSGMII/SGMII_PCS_VR_MII_1_LINK_TIMER_CTRL	0x0A0028	W	0x00000000	VR MII_1 MMD Link Timer Control Register
QSGMII/SGMII_PCS_VR_MII_1_EEE_MCTRL1	0x0A002C	W	0x00000000	VR MII_1 MMD EEE Mode Control 1 Register
QSGMII/SGMII_PCS_VR_MII_1_DIG_STS	0x0A0040	W	0x00000010	VR MII_1 MMD Digital Status Register.
QSGMII/SGMII_PCS_VR_MII_1_ICG_ERRCNT1	0x0A0044	W	0x00000000	VR MII_1 MMD Invalid Code Group Error Count1 Register
QSGMII/SGMII_PCS_VR_MII_1_DIG_CTRL2	0x0A0384	W	0x00000000	VR MII_1 MMD Digital Control2 Register
QSGMII/SGMII_PCS_VR_MII_1_DIG_ERRCNT_SEL	0x0A0388	W	0x00000000	VR MII_1 MMD Digital Error Count Select Register
QSGMII/SGMII_PCS_SR_MII_2_CTRL	0x0C0000	W	0x00000140	SR MII_2 MMD Control Register
QSGMII/SGMII_PCS_SR_MII_2_STS	0x0C0004	W	0x00000109	SR MII_2 MMD Status Register
QSGMII/SGMII_PCS_SR_MII_2_DEV_ID1	0x0C0008	W	0x00007996	SR MII_2 MMD Device Identifier Register 1
QSGMII/SGMII_PCS_SR_MII_2_DEV_ID2	0x0C000C	W	0x0000CC00	SR MII_2 MMD Device Identifier Register 2
QSGMII/SGMII_PCS_SR_MII_2_AN_ADV	0x0C0010	W	0x00000020	SR MII_2 MMD AN Advertisement Register
QSGMII/SGMII_PCS_SR_MII_2_LP_BABL	0x0C0014	W	0x00000000	SR MII_2 MMD AN Link Partner Base Ability Register
QSGMII/SGMII_PCS_SR_MII_2_AN_EXPN	0x0C0018	W	0x00000000	SR MII_2 MMD AN Expansion Register
QSGMII/SGMII_PCS_SR_MII_2_EXT_STS	0x0C003C	W	0x0000C000	SR MII_2 MMD Extended Status Register
QSGMII/SGMII_PCS_VR_MII_2_DIG_CTRL1	0x0E0000	W	0x00002400	VR MII_2 MMD Digital Control1 Register
QSGMII/SGMII_PCS_VR_MII_2_AN_CTRL	0x0E0004	W	0x00000000	VR MII_2 MMD AN Control Register
QSGMII/SGMII_PCS_VR_MII_2_AN_INTR_STS	0x0E0008	W	0x00000000	VR MII_2 MMD AN Interrupt and Status Register
QSGMII/SGMII_PCS_VR_MII_2_TC	0x0E000C	W	0x00000000	VR MII_2 MMD Test Control Register.
QSGMII/SGMII_PCS_VR_MII_2_DBG_CTRL	0x0E0014	W	0x00000000	VR MII_2 MMD Debug Control Register
QSGMII/SGMII_PCS_VR_MII_2_EEE_MCTRL0	0x0E0018	W	0x0000899C	VR MII_2 MMD EEE Mode Control Register
QSGMII/SGMII_PCS_VR_MII_2_EEE_TXTIMER	0x0E0020	W	0x00000000	VR MII_2 MMD EEE Tx Timer Register
QSGMII/SGMII_PCS_VR_MII_2_EEE_RXTIMER	0x0E0024	W	0x00000000	VR MII_2 MMD EEE Rx Timer Register
QSGMII/SGMII_PCS_VR_MII_2_LINK_TIMER_CTRL	0x0E0028	W	0x00000000	VR MII_2 MMD Link Timer Control Register
QSGMII/SGMII_PCS_VR_MII_2_EEE_MCTRL1	0x0E002C	W	0x00000000	VR MII_2 MMD EEE Mode Control 1 Register

Name	Offset	Size	Reset Value	Description
QSGMII/SGMII_PCS_VR_MII_2_DIG_STS	0x0E0040	W	0x00000010	VR MII_2 MMD Digital Status Register.
QSGMII/SGMII_PCS_VR_MII_2_ICG_ERRCNT1	0x0E0044	W	0x00000000	VR MII_2 MMD Invalid Code Group Error Count1 Register
QSGMII/SGMII_PCS_VR_MII_2_DIG_CTRL2	0x0E0384	W	0x00000000	VR MII_2 MMD Digital Control2 Register
QSGMII/SGMII_PCS_VR_MII_2_DIG_ERRCNT_SEL	0x0E0388	W	0x00000000	VR MII_2 MMD Digital Error Count Select Register
QSGMII/SGMII_PCS_SR_MII_3_CTRL	0x100000	W	0x00000140	SR MII_3 MMD Control Register
QSGMII/SGMII_PCS_SR_MII_3_STS	0x100004	W	0x00000109	SR MII_3 MMD Status Register
QSGMII/SGMII_PCS_SR_MII_3_DEV_ID1	0x100008	W	0x00007996	SR MII_3 MMD Device Identifier Register 1
QSGMII/SGMII_PCS_SR_MII_3_DEV_ID2	0x10000C	W	0x0000CC00	SR MII_3 MMD Device Identifier Register 2
QSGMII/SGMII_PCS_SR_MII_3_AN_ADV	0x100010	W	0x00000020	SR MII_3 MMD AN Advertisement Register
QSGMII/SGMII_PCS_SR_MII_3_LP_BABL	0x100014	W	0x00000000	SR MII_3 MMD AN Link Partner Base Ability Register
QSGMII/SGMII_PCS_SR_MII_3_AN_EXPN	0x100018	W	0x00000000	SR MII_3 MMD AN Expansion Register
QSGMII/SGMII_PCS_SR_MII_3_EXT_STS	0x10003C	W	0x0000C000	SR MII_3 MMD Extended Status Register
QSGMII/SGMII_PCS_VR_MII_3_DIG_CTRL1	0x120000	W	0x00002400	VR MII_3 MMD Digital Control1 Register
QSGMII/SGMII_PCS_VR_MII_3_AN_CTRL	0x120004	W	0x00000000	VR MII_3 MMD AN Control Register
QSGMII/SGMII_PCS_VR_MII_3_AN_INTR_STS	0x120008	W	0x00000000	VR MII_3 MMD AN Interrupt and Status Register
QSGMII/SGMII_PCS_VR_MII_3_TC	0x12000C	W	0x00000000	VR MII_3 MMD Test Control Register.
QSGMII/SGMII_PCS_VR_MII_3_DBG_CTRL	0x120014	W	0x00000000	VR MII_3 MMD Debug Control Register
QSGMII/SGMII_PCS_VR_MII_3_EEE_MCTRL0	0x120018	W	0x0000899C	VR MII_3 MMD EEE Mode Control Register
QSGMII/SGMII_PCS_VR_MII_3_EEE_TXTIMER	0x120020	W	0x00000000	VR MII_3 MMD EEE Tx Timer Register
QSGMII/SGMII_PCS_VR_MII_3_EEE_RXTIMER	0x120024	W	0x00000000	VR MII_3 MMD EEE Rx Timer Register
QSGMII/SGMII_PCS_VR_MII_3_LINK_TIMER_CTRL	0x120028	W	0x00000000	VR MII_3 MMD Link Timer Control Register
QSGMII/SGMII_PCS_VR_MII_3_EEE_MCTRL1	0x12002C	W	0x00000000	VR MII_3 MMD EEE Mode Control 1 Register
QSGMII/SGMII_PCS_VR_MII_3_DIG_STS	0x120040	W	0x00000010	VR MII_3 MMD Digital Status Register.
QSGMII/SGMII_PCS_VR_MII_3_ICG_ERRCNT1	0x120044	W	0x00000000	VR MII_3 MMD Invalid Code Group Error Count1 Register
QSGMII/SGMII_PCS_VR_MII_3_DIG_CTRL2	0x120384	W	0x00000000	VR MII_3 MMD Digital Control2 Register
QSGMII/SGMII_PCS_VR_MII_3_DIG_ERRCNT_SEL	0x120388	W	0x00000000	VR MII_3 MMD Digital Error Count Select Register

Name	Offset	Size	Reset Value	Description
QSGMII/SGMII_PCS_SR_VSMMD_PMA_ID1	0x180000	W	0x00000000	SR Control MMD PMA Device Identifier Register 1
QSGMII/SGMII_PCS_SR_VSMMD_PMA_ID2	0x180004	W	0x00000000	SR Control MMD PMA Device Identifier Register 2
QSGMII/SGMII_PCS_SR_VSMMD_DEV_ID1	0x180008	W	0x00000000	SR Control MMD Device Identifier Register 1
QSGMII/SGMII_PCS_SR_VSMMD_DEV_ID2	0x18000C	W	0x00000000	SR Control MMD Device Identifier Register 2
QSGMII/SGMII_PCS_SR_VSMMD_PCS_ID1	0x180010	W	0x00007996	SR Control MMD PCS Device Identifier Register 1
QSGMII/SGMII_PCS_SR_VSMMD_PCS_ID2	0x180014	W	0x0000CED0	SR Control MMD PCS Device Identifier Register 2
QSGMII/SGMII_PCS_SR_VSMMD_AN_ID1	0x180018	W	0x00000000	SR Control MMD AN Device Identifier Register 1
QSGMII/SGMII_PCS_SR_VSMMD_AN_ID2	0x18001C	W	0x00000000	SR Control MMD AN Device Identifier Register 2
QSGMII/SGMII_PCS_SR_VSMMD_STS	0x180020	W	0x00000000	SR Control MMD Status Register
QSGMII/SGMII_PCS_SR_VSMMD_CTRL	0x180024	W	0x00000004	SR Control MMD Control Register
QSGMII/SGMII_PCS_SR_VSMMD_PKGID1	0x18038	W	0x00000000	SR Control MMD Package Identifier Register 1
QSGMII/SGMII_PCS_SR_VSMMD_PKGID2	0x18003C	W	0x00000000	SR Control MMD Package Identifier Register 2
QSGMII/SGMII_PCS_SR_MII_CTRL	0x1C0000	W	0x00000140	SR MII MMD Control Register
QSGMII/SGMII_PCS_SR_MII_STS	0x1C0004	W	0x00000109	SR MII_1 MMD Status Register
QSGMII/SGMII_PCS_SR_MII_DEV_ID1	0x1C0008	W	0x00007996	SR MII MMD Device Identifier Register 1
QSGMII/SGMII_PCS_SR_MII_DEV_ID2	0x1C000C	W	0x0000CED0	SR MII MMD Device Identifier Register 2
QSGMII/SGMII_PCS_SR_MII_AN_ADV	0x1C0010	W	0x00000020	SR MII MMD AN Advertisement Register
QSGMII/SGMII_PCS_SR_MII_LP_BABL	0x1C0014	W	0x00000000	SR MII MMD AN Link Partner Base Ability Register
QSGMII/SGMII_PCS_SR_MII_AN_EXPN	0x1C0018	W	0x00000000	SR MII MMD AN Expansion Register
QSGMII/SGMII_PCS_SR_MII_EXT_STS	0x1C003C	W	0x0000C000	SR MII MMD Extended Status Register
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_ABL	0x1C1C20	W	0x00000003	SR MII MMD Time Sync Capability Register.
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MAX_DLY_LWR	0x1C1C24	W	0x00000038	SR MII MMD Time Sync Tx Max Delay Lower Register.
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MAX_DLY_UPR	0x1C1C28	W	0x00000000	SR MII MMD Time Sync Tx Max Delay Upper Register
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MIN_DLY_LWR	0x1C1C2C	W	0x00000038	SR MII MMD Time Sync Tx Min Delay Lower Register.

Name	Offset	Size	Reset Value	Description
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MIN_DLY_UPR	0x1C1C30	W	0x00000000	SR MII MMD Time Sync Tx Min Delay Upper Register.
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MAX_DLY_LWR	0x1C1C34	W	0x00000058	
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MAX_DLY_UPR	0x1C1C38	W	0x00000000	SR MII MMD Time Sync Rx Max Delay Upper Register.
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MIN_DLY_LWR	0x1C1C3C	W	0x00000050	SR MII MMD Time Sync Rx Min Delay Lower Register.
QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MIN_DLY_UPR	0x1C1C40	W	0x00000000	SR MII MMD Time Sync Rx Min Delay Upper Register
QSGMII/SGMII_PCS_VR_MII_DIG_CTRL1	0x1E0000	W	0x00002400	VR MII MMD Digital Control1 Register
QSGMII/SGMII_PCS_VR_MII_AN_CTRL	0x1E0004	W	0x00000000	VR MII MMD AN Control Register
QSGMII/SGMII_PCS_VR_MII_AN_INTR_STS	0x1E0008	W	0x0000000A	VR MII MMD AN Interrupt and Status Register
QSGMII/SGMII_PCS_VR_MII_TC	0x1E000C	W	0x00000000	VR MII MMD Test Control Register.
QSGMII/SGMII_PCS_VR_MII_DBG_CTRL	0x1E0014	W	0x00000000	VR MII MMD Debug Control Register
QSGMII/SGMII_PCS_VR_MII_EEE_MCTRL0	0x1E0018	W	0x0000899C	VR MII MMD EEE Mode Control Register
QSGMII/SGMII_PCS_VR_MII_EEE_TXTIMER	0x1E0020	W	0x00000000	VR MII MMD EEE Tx Timer Register
QSGMII/SGMII_PCS_VR_MII_EEE_RXTIMER	0x1E0024	W	0x00000000	VR MII MMD EEE Rx Timer Register
QSGMII/SGMII_PCS_VR_MII_LINK_TIMER_CTRL	0x1E0028	W	0x00000000	VR MII MMD Link Timer Control Register
QSGMII/SGMII_PCS_VR_MII_EEE_MCTRL1	0x1E002C	W	0x00000000	VR MII MMD EEE Mode Control 1 Register
QSGMII/SGMII_PCS_VR_MII_DIG_STS	0x1E0040	W	0x00000010	VR MII MMD Digital Status Register.
QSGMII/SGMII_PCS_VR_MII_ICG_ERRCNT1	0x1E0044	W	0x00000000	VR MII MMD Invalid Code Group Error Count1 Register
QSGMII/SGMII_PCS_VR_MII_MISC_STS	0x1E0060	W	0x00000000	VR MII MMD Miscellaneous Status Register
QSGMII/SGMII_PCS_VR_MII_RX_LSTS	0x1E0080	W	0x00000000	VR MII PHY Rx Lane Status Register
QSGMII/SGMII_PCS_VR_MII_DIG_CTRL2	0x1E0384	W	0x00000000	VR MII MMD Digital Control2 Register
QSGMII/SGMII_PCS_VR_MII_DIG_ERRCNT_SEL	0x1E0388	W	0x00000000	VR MII MMD Digital Error Count Select Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.3.3 Detail Registers Description

QSGMII/SGMII_PCS_SR_MII_1_CTRL

Address: Operational Base + offset (0x080000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RST Soft Reset (RW,SC Type) For Non-Synopsys PHY configurations: When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface
14	RO	0x0	LBE Loopback Enable This bit reflects the value of LBE bit of SR_MII_CTRL Register.
13	RW	0x0	SS13 Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed of GMII/XGMII port 1. Speed encoding as follows: For QSGMII: When SS6=1 and SS13=0, speed is 1000 Mbps When SS6=0 and SS13=1, speed is 100 Mbps When SS6=0 and SS13=0, speed is 10 Mbps
12	RW	0x0	AN_ENABLE Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 auto-negotiation process for port 1.
11	RW	0x0	LPM Power-Down Mode This bit controls the power-down mode of the QSGMII/SGMII_PCS. 0: Normal operation 1: The QSGMII/SGMII_PCS goes to the power-down mode along with the PHY. For non-Synopsys PHY, the PCS_pdown_o port is asserted. When the host clears this bit, the QSGMII/SGMII_PCS resumes the normal operation. In a Synopsys PHY configuration, after clearing this bit, the host must wait until Bits[4:2] of VR_XS_PCS_DIG_STS/VR_MII_DIG_STS Register indicate that the QSGMII/SGMII_PCS is in the normal state
10	RO	0x0	Reserved_10 Reserved
9	RW	0x0	RESTART_AN Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the QSGMII/SGMII_PCS initiates the auto-negotiation process for port 1. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The QSGMII/SGMII_PCS clears this bit after restarting the auto-negotiation.

Bit	Attr	Reset Value	Description
8	RW	0x1	DUPLEX_MODE Duplex Mode This bit specifies the duplex mode of the QSGMII/SGMII_PCS along port 1. 0: Half duplex 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process.
7	RO	0x0	Reserved_7 Reserved
6	RW	0x1	SS6 Speed Selection This bit, along with the SS5 and SS13 bits of this register indicates the speed of operation of GMII/XGMII Port 1. For more information, see description of the SS13 bit.
5	RO	0x0	SS5 Speed Selection This bit, along with SS6 and SS13 bits, control the speed of operation of XGMII/GMII Port 1. For more information, see description of the SS13 bit.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_1_STS

Address: Operational Base + offset (0x080004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ABL100T4 100BASE-T4 Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
14	RO	0x0	FD100ABL 100BASE-X Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
13	RO	0x0	HD100ABL 100BASE-X Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
12	RO	0x0	FD10ABL 10 Mbps Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
11	RO	0x0	HD10ABL 10 Mbps Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality

Bit	Attr	Reset Value	Description
10	RO	0x0	FD100T 100BASE-T2 Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
9	RO	0x0	HD100T 100BASE-T2 Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
8	RO	0x1	EXT_STS_ABL Extended Status Information 0: No Extended Status information is present at register address 16'h000F of this MMD device. 1: Extended Status information is present at register address 16'h000F of this MMD device. QSGMII/SGMII_PCS returns this bit as 1.
7	RO	0x0	UN_DIR_ABL Unidirectional Ability 1: The QSGMII/SGMII_PCS is able to transmit GMII irrespective of whether device has determined the valid link or not. 0: The QSGMII/SGMII_PCS is able to transmit GMII only when the device has determined the valid link. The QSGMII/SGMII_PCS always returns this bit as 0.
6	RO	0x0	MF_PRE_SUP MF Preamble Suppression 1: The QSGMII/SGMII_PCS accepts the MDIO frames with preamble suppressed. 0: The QSGMII/SGMII_PCS does not accept the MDIO frames with preamble suppressed. This bit is always set to 0
5	RO	0x0	AN_CMPL Auto-negotiation Complete for Port 1 1: The AN process is complete 0: The AN process is not complete This bit returns 0 if AN_ENABLE of SR_MII_1_CTRL Register is set to 0.
4	RO	0x0	RF Remote Fault This register bit is shared with RF bit of SR_MII_STS register. The value returned by this field should be ignored by the software as it is not valid in QSGMII/SGMII/USXGMII Modes
3	RO	0x1	AN_ABL Auto-negotiation Ability The QSGMII/SGMII_PCS always returns this bit as 1. 1: The QSGMII/SGMII_PCS is able to perform auto-negotiation. 0: The QSGMII/SGMII_PCS is not able to perform auto-negotiation
2	RO	0x0	LINK_STS Link Status This register bit is shared with RLU bit of SR_MII_STS register.
1	RO	0x0	Reserved_1 Reserved

Bit	Attr	Reset Value	Description
0	RO	0x1	EXT_REG_CAP Extended Register Capability 1: Extended Register capability exists. This bit is always set to 1. 0: Extended Register capability does not exist.

QSGMII/SGMII_PCS_SR_MII_1_DEV_ID1

Address: Operational Base + offset (0x080008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x7996	VS_MII_DEV_OUI_3_18 Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer. This register reflects the same value as that of SR_MII_DEV_ID1 register.

QSGMII/SGMII_PCS_SR_MII_1_DEV_ID2

Address: Operational Base + offset (0x08000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x33	VS_MMD_DEV_OUI_19_24 Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer.
9:4	RO	0x00	VS_MMD_DEV_MMN_5_0 Model Number This field contains the 5-bit Model Number of the device.
3:0	RO	0x0	VS_MMD_DEV_RN_3_0 Revision Number This field contains the 4-bit Revision Number of the device

QSGMII/SGMII_PCS_SR_MII_1_AN_ADV

Address: Operational Base + offset (0x080010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP Next Page This bit reflects the value of NP bit of SR_MII_AN_ADV Register.
14	RO	0x0	Reserved_14 Reserved
13:12	RO	0x0	RF Remote Fault This bit reflects the value of RF bit of SR_MII_AN_ADV Register.
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	PAUSE Pause Ability. This bit reflects the value of PAUSE bit of SR_MII_AN_ADV Register
6	RO	0x0	HD Half Duplex This bit reflects the value of HD bit of SR_MII_AN_ADV Register.

Bit	Attr	Reset Value	Description
5	RW	0x1	FD Full Duplex When this bit is set, it indicates the device (port 1) can operate in full-duplex mode. This bit is used in Clause 37 auto-negotiation (Tx_Config_Reg) done by port 1, when QSGMII/SGMII_PCS is configured as PHY-side QSGMII.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_1_LP_BABL

Address: Operational Base + offset (0x080014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	LP_NP Next Page
14	RO	0x0	LP_ACK ACK bit from the Link Partner
13:12	RO	0x0	LP_RF Remote Fault
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	LP_PAUSE Pause Ability
6	RO	0x0	LP_HD Half Duplex
5	RO	0x0	LP_FD Full Duplex
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_1_AN_EXPN

Address: Operational Base + offset (0x080018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	LD_NP_ABL Local Device NP Able 1: The local device has the next page ability 0: The local device does not have the next page ability The QSGMII/SGMII_PCS always returns this bit as 0 because it does not support Next Page.
1	RO	0x0	PG_RCVD Page Received (RO, LH Type) This bit indicates that the local device received a page from the link partner (during port 1 auto-negotiation). 1: The local device received a new page 0: The local device did not receive a new page
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_SR_MII_1_EXT_STS

Address: Operational Base + offset (0x08003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x1	CAP_1G_X_FD 1000BASE-X Full-Duplex Capable
14	RO	0x1	CAP_1G_X_HD 1000BASE-X Half-Duplex Capable
13	RO	0x0	CAP_1G_T_FD 1000BASE-T Full-Duplex Capable
12	RO	0x0	CAP_1G_T_HD 1000BASE-T Half-Duplex Capable
11:0	RO	0x000	Reserved_11_0 Reserved

QSGMII/SGMII_PCS_VR_MII_1_DIG_CTRL1

Address: Operational Base + offset (0x0A0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	VR_RST Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: For Synopsys PHY: This bit is self cleared when Bits[4:2] in VR_MII_DIG_STS Register are equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. For Non-Synopsys PHY:This bit is self cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface Note: For information about the read or write access for any register during the reset process, see "Special Case Register Access" section.
14	RW	0x0	R2TLBE Rx to Tx Loopback Enable This bit controls the loopback path from the GMII/XGMII Rx to the GMII/XGMII Tx at the GMII/XGMII interface (port 1). 0: Loopback path is disabled 1: Loopback path is enabled
13	RO	0x1	EN_VSMMD1 Enable Vendor-Specific MMD1 This is a read-only bit which reflects the value of EN_VSMMD1 bit of VR_MII_DIG_CTRL1 Register.
12	RO	0x0	CL37_BP Enable Clause 37 AN in Backplane Configuration This is a read-only bit which reflects the value of CL37_BP bit of VR_MII_DIG_CTRL1 Register.
11	RO	0x0	PWRSV Reserved
10	RW	0x1	CS_EN Clock Stop Enable 1: The PHY may stop the clock during LPI mode 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC (connected to GMII Port 1) during Rx LPI mode. Note: This field is valid only in QSGMII mode

Bit	Attr	Reset Value	Description
9	RW	0x0	MAC_AUTO_SW Automatic Speed Mode Change after CL37 AN (for port 1) If this field is set to 1, QSGMII/SGMII_PCS automatically switches to the negotiated USXGMII/QSGMII(port1) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when QSGMII/SGMII_PCS is configured as MAC-side USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, QSGMII/SGMII_PCS operates at the speed/duplex mode as per the values programmed to SR_MII_1_CTRL Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR_MII_1_AN_INTR_STS Register and then program SR_MII_1_CTRL Register appropriately. If this bit is set to 1 in QSGMII mode, PCS_qsgmii_link_sts_p1_o, PCS_link_speed_p1_o and PCS_qsgmii_full_duplex_p1_o outputs reflect the auto-negotiated values, that is, values from CL37_ANSGM_STS field of VR_MII_1_AN_INTR_STS Register. For USXGMII mode, if clk_xgmii_tx_p1_i and clk_xgmii_rx_p1_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USRA_RST' bit prior to starting packet transfer in the new speed mode.
8	RO	0x0	INIT INIT This bit reflects the value of INIT bit of VR_MII_DIG_CTRL1 Register.
7	RO	0x0	MSK_RD_ERR Mask Running Disparity Error This bit reflects the value of MSK_RD_ERR bit of VR_MII_DIG_CTRL1 Register.
6	RW	0x0	PRE_EMP Pre-emption Packet Enable. This bit should be set to 1 to allow the QSGMII/SGMII_PCS to properly receive/transmit pre-emption packets along GMII port 1, when operating in 10M/100M Modes.

Bit	Attr	Reset Value	Description
5	RO	0x0	USRA_RST USXGMII Rate Adaptor Reset (Port 1) This bit can be set to 1 to reset/initialize the USXGMII Rate Adaptor Logic (for port 1) inside QSGMII/SGMII_PCS. The Rate Adaptor Logic maps GMII data to XGMII (and vice-versa in Rx path) data and perform data replication for lower USXGMII speeds. This is a self-clear bit (RW,SC) and clears itself after the reset of Tx and Rx Rate Adaptor Logic is complete. After setting this bit to 1, application should poll this bit till it self-clears. Note: If CLKCOMP=Enabled, this bit also initializes the clock compensation FIFO (corresponding to port 1). When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of VR_MII_1_DIG_STS Register might get set incorrectly. Therefore, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits are reliable.
4	RO	0x0	DTXLANED_0 Tx Lane 0 Disable This bit reflects the value of DTXLANED_0 bit of VR_MII_DIG_CTRL1 Register.
3	RO	0x0	CL37_TMR_OVR_RIDE Over-Ride Control for CL37 Link Timer. This bit reflects the value of CL37_TMR_OVR_RIDE bit of VR_MII_DIG_CTRL1 Register.
2	RO	0x0	EN_2_5G_MODE Enable 2.5G GMII Mode (GMII interface over-clocked 2.5 This bit reflects the value of EN_2_5G_MODE bit of VR_MII_DIG_CTRL1 Register.
1	RO	0x0	BYP_PWRUP Reserved
0	RO	0x0	PHY_MODE_CTRL QSGMII/USXGMII PHY mode control on Port 1 This bit controls the Clause 37 auto-negotiation when operating in QSGMII/USXGMII (Port 1) PHY mode. QSGMI: When this bit is set to 1, QSGMII/SGMII_PCS advertises the values of input ports PCS_qsgmii_link_sts_p1_i, PCS_qsgmii_link_speed_p1_i and PCS_qsgmii_full_duplex_p1_i during QSGMII(Port 1) auto-negotiation. When this bit is set to 0, QSGMII(Port 1) auto-negotiation advertises the values programmed to: bit 4 (SGMII_LINK_STS) of VR_MII_1_AN_CTRL Register bit 13 (ss13) and 6 (ss6) of SR_MII_1_CTRL Register and bit 5 (FD) of SR_MII_1_AN_ADV Register

QSGMII/SGMII_PCS_VR_MII_1_AN_CTRL

Address: Operational Base + offset (0x0A0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	Reserved_15_10 Reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	IND_TX_EN Independent Transmit Enable If this bit is set to 1, QSGMII/SGMII_PCS is able to transmit the port 1 GMII Tx data, irrespective of its receive link status during QSGMII mode (provided auto-negotiation is not enabled). If this bit is set to 0, QSGMII/SGMII_PCS sends IDLE (for port 1) till its receiver has attained synchronization.
8	RW	0x0	MII_CTRL MII Control This bit controls the width of the MAC interface (connected to GMII port 1) when operating at 10 Mbps or 100 Mbps 0: 4-bit MII 1: 8-bit MII This bit also controls the PCS_mii_ctrl_p1_o signal which is used for external clock multiplexing of the clk_mii_tx_p1_i/clk_xgmii_tx_p1_i and clk_mii_rx_p1_i/clk_xgmii_rx_p1_i signals
7:5	RO	0x0	Reserved_7_5 Reserved
4	RW	0x0	SGMII_LINK_STS QSGMII/USXGMII Link Status (port 1) This bit is used in Bit 15 of the Tx_Config_Reg during Clause 37 auto-negotiation (along port 1) when QSGMII/SGMII_PCS is programmed as QSGMII-PHY (or as USXGMII-PHY) and when PHY_MODE_CTRL bit of VR_MII_1_DIG_CTRL1 Register is 0 . 0: Link Down 1: Link Up
3	RO	0x0	TX_CONFIG Transmit Configuration This field reflects the value of TX_CONFIG of VR_MII_AN_CTRL Register.
2:1	RO	0x0	PCS_MODE PCS Mode This field reflects the value of PCS_MODE of VR_MII_AN_CTRL Register for configurations with QSGMII support. For other configurations, this field returns 2'b00.
0	RW	0x0	MII_AN_INTR_EN Clause 37 AN Complete Interrupt Enable (port 1) When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete (on port 1) interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

QSGMII/SGMII_PCS_VR_MII_1_AN_INTR_STS

Address: Operational Base + offset (0x0A0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	Reserved_15 Reserved

Bit	Attr	Reset Value	Description
14:8	RO	0x00	USXG_AN_STS USXGMII Clause 37 AN Status (along Port 1) This field is valid only when clause 37 auto-negotiation is complete in USXGMII Mode along Port 1. It indicates the status received from remote link after the USXGMII auto-negotiation is complete. USXG_AN_STS[6] 0: Link is Down 1: Link is Up USXG_AN_STS[5] 0: Half Duplex 1: Full Duplex USXG_AN_STS[4:2] 000: 10 Mbps speed link 001: 100 Mbps speed link 010: 1000 Mbps speed link 011: 10 Gbps speed link 100: 2.5 Gbps speed link 101: 5 Gbps speed link USXG_AN_STS[1] 1: EEE supported 0: EEE not supported USXG_AN_STS[0] 1: EEE clock-stop supported 0: EEE clock-stop not supported Note:This field is present only in configurations with Multi-port USXGMII support.
7	RO	0x0	Reserved_7 Reserved
6	RO	0x0	LP_CK_STP Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or enable in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. Note:This field is present only in configurations with QSGMII
5	RO	0x0	LP_EEE_CAP Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 1 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. Note:This field is present only in configurations with QSGMII.

Bit	Attr	Reset Value	Description
4:1	RO	0x0	CL37_ANSGM_STS Clause 37 AN QSGMII Status (port 1) This field is valid only when the PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. It indicates the status received from remote link partner. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link CL37_ANSGM_STS[3] 0: Link is Down 1: Link is Up Note:This field is present only in configurations with QSGMII.
0	RW	0x0	CL37_ANCMPLT_INTR Clause 37 AN Complete Interrupt (SS,WC Type) The QSGMII/SGMII_PCS sets this bit when Clause 37 auto-negotiation is complete for port 1. The host must clear this bit by writing 0 to it.

QSGMII/SGMII_PCS_VR_MII_1_TC

Address: Operational Base + offset (0x0A000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	TPE Test Pattern Enable Lanes
1:0	RO	0x0	TP Test Pattern Select

QSGMII/SGMII_PCS_VR_MII_1_DBG_CTRL

Address: Operational Base + offset (0x0A0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	TX_PMBL_CTL Transmit Preamble Control This bit merely reflects the value of TX_PMBL_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
7	RO	0x0	RX_SYNC_CTL Receive Synchronization Control . This bit merely reflects the value of RX_SYNC_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
6	RO	0x0	RX_DT_EN_CTL Rx Data Enable Control. This bit merely reflects the value of RX_DT_EN_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).

Bit	Attr	Reset Value	Description
5	RO	0x0	SUPRESS_EEE_LOS_DET Suppress EEE Loss of Signal Detection. This bit merely reflects the value of SUPRESS_EEE_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
4	RO	0x0	SUPRESS_LOS_DET Suppress Loss of Signal Detection This bit merely reflects the value of SUPRESS_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations)
3:1	RO	0x0	reserved
0	RW	0x0	RESTAR_SYNC Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on port 1. The host must clear this bit to 0 before setting it to 1 next time.

QSGMII/SGMII_PCS_VR_MII_1_EEE_MCTRL0

Address: Operational Base + offset (0x0A0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x8	CLKSTOP Clock Stop
11:8	RO	0x9	MULT_FACT_100NS 100 ns Clock Tic Multiplying Factor
7	RO	0x1	RX_EN_CTRL Rx Control Enable
6	RO	0x0	SIGN_BIT Effective 100 ns Tic Value
5	RO	0x0	Reserved_5 Reserved
4	RO	0x1	TX_EN_CTRL Tx Control Enable
3	RO	0x1	RX_QUIET_EN Rx Quiet Enable
2	RO	0x1	TX_QUIET_EN Tx Quiet Enable
1	RO	0x0	LRX_EN LPI Rx Enable
0	RO	0x0	LTX_EN LPI Tx Enable

QSGMII/SGMII_PCS_VR_MII_1_EEE_TXTIMER

Address: Operational Base + offset (0x0A0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	TSL_RES TSL Resolution

QSGMII/SGMII_PCS_VR_MII_1_EEE_RXTIMER

Address: Operational Base + offset (0x0A0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:8	RO	0x00	TWR_RES TWR Resolution
7:0	RO	0x00	RES_100U 100 us Resolution

QSGMII/SGMII_PCS_VR_MII_1_LINK_TIMER_CTRL

Address: Operational Base + offset (0x0A0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	VR_MII_1_LINK_TIMER_CTRL Programmable Link Timer Value for Clause 37 auto-negotiation.

QSGMII/SGMII_PCS_VR_MII_1_EEE_MCTRL1

Address: Operational Base + offset (0x0A002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	TRN_LPI Transparent Tx LPI Mode Enable

QSGMII/SGMII_PCS_VR_MII_1_DIG_STS

Address: Operational Base + offset (0x0A0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	LTX_STATE LPI Transmit State. This field reflects the value of LTX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).
12:10	RO	0x0	LRX_STATE LPI Receive State This field reflects the value of LRX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).

Bit	Attr	Reset Value	Description
9	RO	0x0	INV_XGM_CHAR Invalid XGMII Character (RO,LH Type) -Port 1 This bit indicates an invalid XGMII character on the Transmit path (port 1). 0: No Invalid XGMII character 1: Invalid character This bit is set when one of the following conditions is true on the XGMII interface: |Q| is detected on a lane other than Lane 0. |Q| is detected on Lane 0 and also any of the following conditions is true: No 8'h00 data in Lane 1. No 8'h00 data in Lane 2. No 8'h01 or 8'h02 data on Lane 3. |E| or |T| is encountered in non-data phase and |Q| is encountered in data phase. |D| is detected during the Idle phase (after Terminate and before valid SOF). |I| is detected during the data phase (after SOF and before Terminate). Note: This field is present only for Multi-port USXGMII configurations.
8	RO	0x0	INV_XGM_T Invalid XGMII T Character (RO,LH Type) -Port 1 This bit indicates that the transmit data (port 1) received on XGMII has an invalid Terminate character. 0: Normal operation 1: Invalid Terminate character The following can cause an invalid Terminate character: In Terminate column, before lane corresponds to the |T| character, there is a |I| or |Q| character. In Terminate column, after lane corresponds to the |T| character, there is a non-|I| character Note:This field is present only for Multi-port USXGMII configurations.
7	RO	0x0	INV_XGM_SOP Invalid XGMII Start Character (RO,LH Type) -Port 1 This bit indicates that the XGMII transmit (Port 1) frame contains invalid SOP character. 0: Normal operation 1: Invalid SOP character An invalid SOP event occurs when a |S| character is detected in a lane other than Lane 0. Note:This field is present only for Multi-port USXGMII configurations.
6	RO	0x0	RXFIFO_OVF Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow for port 1. 0: Normal operation 1: FIFO overflow

Bit	Attr	Reset Value	Description
5	RO	0x0	RXFIFO_UNDF Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow for port 1. 0: Normal operation 1: FIFO underflow
4:2	RO	0x4	PSEQ_STATE Reserved
1	RO	0x0	LB_ACTIVE Reserved
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_VR_MII_1_ICG_ERRCNT1

Address: Operational Base + offset (0x0A0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	EC0 Invalid Code Group Count -Port 1 (RO,LH Type) This field gives the invalid code group count in port 1 (of QSGMII) when Bit 4 of VR MII_1 MMD Digital Error Count Select Register is set to 1.

QSGMII/SGMII_PCS_VR_MII_1_DIG_CTRL2

Address: Operational Base + offset (0x0A0384)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	TX_POL_INV_0 Tx Polarity Invert on Lane 0
3:1	RO	0x0	Reserved_3_1 Reserved
0	RO	0x0	RX_POL_INV_0 Rx Polarity Invert on Lane 0

QSGMII/SGMII_PCS_VR_MII_1_DIG_ERRCNT_SEL

Address: Operational Base + offset (0x0A0388)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	INV_EC_EN Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors (on port 1) is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR_MII_1_ICG_ERRCNT1 Register.
3:1	RO	0x0	Reserved_3_1 Reserved
0	RW	0x0	COR Clear on Read When this bit is set and the host reads port 1 error counter (VR_MII_1_ICG_ERRCNT1 Register), that counter is cleared after the read cycle. 0: Normal operation 1: Clear error counter that is read

QSGMII/SGMII_PCS_SR_MII_2_CTRL

Address: Operational Base + offset (0x0C0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RST Soft Reset (RW,SC Type) For Non-Synopsys PHY configurations: When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface
14	RO	0x0	LBE Loopback Enable This bit reflects the value of LBE bit of SR_MII_CTRL Register.
13	RW	0x0	SS13 Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed of GMII/XGMII port 2. Speed encoding as follows: For QSGMII: When SS6=1 and SS13=0, speed is 1000 Mbps When SS6=0 and SS13=1, speed is 100 Mbps When SS6=0 and SS13=0, speed is 10 Mbps
12	RW	0x0	AN_ENABLE Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 auto-negotiation process for port 2.
11	RW	0x0	LPM Power-Down Mode This bit controls the power-down mode of the QSGMII/SGMII_PCS. 0: Normal operation 1: The QSGMII/SGMII_PCS goes to the power-down mode along with the PHY. For non-Synopsys PHY, the PCS_pdown_o port is asserted. When the host clears this bit, the QSGMII/SGMII_PCS resumes the normal operation. In a Synopsys PHY configuration, after clearing this bit, the host must wait until Bits[4:2] of VR_XS_PCS_DIG_STS/VR_MII_DIG_STS Register indicate that the QSGMII/SGMII_PCS is in the normal state
10	RO	0x0	Reserved_10 Reserved
9	RW	0x0	RESTART_AN Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the QSGMII/SGMII_PCS initiates the auto-negotiation process for port 2. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The QSGMII/SGMII_PCS clears this bit after restarting the auto-negotiation.

Bit	Attr	Reset Value	Description
8	RW	0x1	DUPLEX_MODE Duplex Mode This bit specifies the duplex mode of the QSGMII/SGMII_PCS along port 2. 0: Half duplex 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process.
7	RO	0x0	Reserved_7 Reserved
6	RW	0x1	SS6 Speed Selection This bit, along with the SS5 and SS13 bits of this register indicates the speed of operation of GMII/XGMII Port 2. For more information, see description of the SS13 bit.
5	RO	0x0	SS5 Speed Selection This bit, along with SS6 and SS13 bits, control the speed of operation of XGMII/GMII Port 2. For more information, see description of the SS13 bit.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_2_STS

Address: Operational Base + offset (0x0C0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ABL100T4 100BASE-T4 Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
14	RO	0x0	FD100ABL 100BASE-X Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
13	RO	0x0	HD100ABL 100BASE-X Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
12	RO	0x0	FD10ABL 10 Mbps Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
11	RO	0x0	HD10ABL 10 Mbps Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality

Bit	Attr	Reset Value	Description
10	RO	0x0	FD100T 100BASE-T2 Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
9	RO	0x0	HD100T 100BASE-T2 Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
8	RO	0x1	EXT_STS_ABL Extended Status Information 0: No Extended Status information is present at register address 16'h000F of this MMD device. 1: Extended Status information is present at register address 16'h000F of this MMD device. QSGMII/SGMII_PCS returns this bit as 1.
7	RO	0x0	UN_DIR_ABL Unidirectional Ability 1: The QSGMII/SGMII_PCS is able to transmit GMII irrespective of whether device has determined the valid link or not. 0: The QSGMII/SGMII_PCS is able to transmit GMII only when the device has determined the valid link. The QSGMII/SGMII_PCS always returns this bit as 0.
6	RO	0x0	MF_PRE_SUP MF Preamble Suppression 1: The QSGMII/SGMII_PCS accepts the MDIO frames with preamble suppressed. 0: The QSGMII/SGMII_PCS does not accept the MDIO frames with preamble suppressed. This bit is always set to 0
5	RO	0x0	AN_CMPL Auto-negotiation Complete for Port 2 1: The AN process is complete 0: The AN process is not complete This bit returns 0 if AN_ENABLE of SR_MII_1_CTRL Register is set to 0.
4	RO	0x0	RF Remote Fault This register bit is shared with RF bit of SR_MII_STS register. The value returned by this field should be ignored by the software as it is not valid in QSGMII/SGMII/USXGMII Modes
3	RO	0x1	AN_ABL Auto-negotiation Ability The QSGMII/SGMII_PCS always returns this bit as 1. 1: The QSGMII/SGMII_PCS is able to perform auto-negotiation. 0: The QSGMII/SGMII_PCS is not able to perform auto-negotiation
2	RO	0x0	LINK_STS Link Status This register bit is shared with RLU bit of SR_MII_STS register.
1	RO	0x0	Reserved_1 Reserved

Bit	Attr	Reset Value	Description
0	RO	0x1	EXT_REG_CAP Extended Register Capability 1: Extended Register capability exists. This bit is always set to 1. 0: Extended Register capability does not exist.

QSGMII/SGMII_PCS_SR_MII_2_DEV_ID1

Address: Operational Base + offset (0x0C0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x7996	VS_MII_DEV_OUI_3_18 Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer. This register reflects the same value as that of SR_MII_DEV_ID1 register.

QSGMII/SGMII_PCS_SR_MII_2_DEV_ID2

Address: Operational Base + offset (0x0C000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x33	VS_MMD_DEV_OUI_19_24 Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer.
9:4	RO	0x00	VS_MMD_DEV_MMN_5_0 Model Number This field contains the 5-bit Model Number of the device.
3:0	RO	0x0	VS_MMD_DEV_RN_3_0 Revision Number This field contains the 4-bit Revision Number of the device

QSGMII/SGMII_PCS_SR_MII_2_AN_ADV

Address: Operational Base + offset (0x0C0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP Next Page This bit reflects the value of NP bit of SR_MII_AN_ADV Register.
14	RO	0x0	Reserved_14 Reserved
13:12	RO	0x0	RF Remote Fault This bit reflects the value of RF bit of SR_MII_AN_ADV Register.
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	PAUSE Pause Ability. This bit reflects the value of PAUSE bit of SR_MII_AN_ADV Register
6	RO	0x0	HD Half Duplex This bit reflects the value of HD bit of SR_MII_AN_ADV Register.

Bit	Attr	Reset Value	Description
5	RW	0x1	FD Full Duplex When this bit is set, it indicates the device (port 1) can operate in full-duplex mode. This bit is used in Clause 37 auto-negotiation (Tx_Config_Reg) done by port 1, when QSGMII/SGMII_PCS is configured as PHY-side QSGMII.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_2_LP_BABL

Address: Operational Base + offset (0x0C0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	LP_NP Next Page
14	RO	0x0	LP_ACK ACK bit from the Link Partner
13:12	RO	0x0	LP_RF Remote Fault
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	LP_PAUSE Pause Ability
6	RO	0x0	LP_HD Half Duplex
5	RO	0x0	LP_FD Full Duplex
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_2_AN_EXPN

Address: Operational Base + offset (0x0C0018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	LD_NP_ABL Local Device NP Able 1: The local device has the next page ability 0: The local device does not have the next page ability The QSGMII/SGMII_PCS always returns this bit as 0 because it does not support Next Page.
1	RO	0x0	PG_RCVD Page Received (RO, LH Type) This bit indicates that the local device received a page from the link partner (during port 1 auto-negotiation). 1: The local device received a new page 0: The local device did not receive a new page
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_SR_MII_2_EXT_STS

Address: Operational Base + offset (0x0C003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x1	CAP_1G_X_FD 1000BASE-X Full-Duplex Capable
14	RO	0x1	CAP_1G_X_HD 1000BASE-X Half-Duplex Capable
13	RO	0x0	CAP_1G_T_FD 1000BASE-T Full-Duplex Capable
12	RO	0x0	CAP_1G_T_HD 1000BASE-T Half-Duplex Capable
11:0	RO	0x000	Reserved_11_0 Reserved

QSGMII/SGMII_PCS_VR_MII_2_DIG_CTRL1

Address: Operational Base + offset (0x0E0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	VR_RST Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: For Synopsys PHY: This bit is self cleared when Bits[4:2] in VR_MII_DIG_STS Register are equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. For Non-Synopsys PHY:This bit is self cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface Note: For information about the read or write access for any register during the reset process, see "Special Case Register Access" section.
14	RW	0x0	R2TLBE Rx to Tx Loopback Enable This bit controls the loopback path from the GMII/XGMII Rx to the GMII/XGMII Tx at the GMII/XGMII interface (port 1). 0: Loopback path is disabled 1: Loopback path is enabled
13	RO	0x1	EN_VSMMD1 Enable Vendor-Specific MMD1 This is a read-only bit which reflects the value of EN_VSMMD1 bit of VR_MII_DIG_CTRL1 Register.
12	RO	0x0	CL37_BP Enable Clause 37 AN in Backplane Configuration This is a read-only bit which reflects the value of CL37_BP bit of VR_MII_DIG_CTRL1 Register.
11	RO	0x0	PWRSV Reserved
10	RW	0x1	CS_EN Clock Stop Enable 1: The PHY may stop the clock during LPI mode 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC (connected to GMII Port 1) during Rx LPI mode. Note: This field is valid only in QSGMII mode

Bit	Attr	Reset Value	Description
9	RW	0x0	MAC_AUTO_SW Automatic Speed Mode Change after CL37 AN (for port 1) If this field is set to 1, QSGMII/SGMII_PCS automatically switches to the negotiated USXGMII/QSGMII(port1) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when QSGMII/SGMII_PCS is configured as MAC-side USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, QSGMII/SGMII_PCS operates at the speed/duplex mode as per the values programmed to SR_MII_1_CTRL Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR_MII_1_AN_INTR_STS Register and then program SR_MII_1_CTRL Register appropriately. If this bit is set to 1 in QSGMII mode, PCS_qsgmii_link_sts_p1_o, PCS_link_speed_p1_o and PCS_qsgmii_full_duplex_p1_o outputs reflect the auto-negotiated values, that is, values from CL37_ANSGM_STS field of VR_MII_1_AN_INTR_STS Register. For USXGMII mode, if clk_xgmii_tx_p1_i and clk_xgmii_rx_p1_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USRA_RST' bit prior to starting packet transfer in the new speed mode.
8	RO	0x0	INIT INIT This bit reflects the value of INIT bit of VR_MII_DIG_CTRL1 Register.
7	RO	0x0	MSK_RD_ERR Mask Running Disparity Error This bit reflects the value of MSK_RD_ERR bit of VR_MII_DIG_CTRL1 Register.
6	RW	0x0	PRE_EMP Pre-emption Packet Enable. This bit should be set to 1 to allow the QSGMII/SGMII_PCS to properly receive/transmit pre-emption packets along GMII port 1, when operating in 10M/100M Modes.

Bit	Attr	Reset Value	Description
5	RO	0x0	USRA_RST USXGMII Rate Adaptor Reset (Port 1) This bit can be set to 1 to reset/initialize the USXGMII Rate Adaptor Logic (for port 1) inside QSGMII/SGMII_PCS. The Rate Adaptor Logic maps GMII data to XGMII (and vice-versa in Rx path) data and perform data replication for lower USXGMII speeds. This is a self-clear bit (RW,SC) and clears itself after the reset of Tx and Rx Rate Adaptor Logic is complete. After setting this bit to 1, application should poll this bit till it self-clears. Note: If CLKCOMP=Enabled, this bit also initializes the clock compensation FIFO (corresponding to port 1). When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of VR_MII_1_DIG_STS Register might get set incorrectly. Therefore, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits are reliable.
4	RO	0x0	DTXLANED_0 Tx Lane 0 Disable This bit reflects the value of DTXLANED_0 bit of VR_MII_DIG_CTRL1 Register.
3	RO	0x0	CL37_TMR_OVR_RIDE Over-Ride Control for CL37 Link Timer. This bit reflects the value of CL37_TMR_OVR_RIDE bit of VR_MII_DIG_CTRL1 Register.
2	RO	0x0	EN_2_5G_MODE Enable 2.5G GMII Mode (GMII interface over-clocked 2.5 This bit reflects the value of EN_2_5G_MODE bit of VR_MII_DIG_CTRL1 Register.
1	RO	0x0	BYP_PWRUP Reserved
0	RO	0x0	PHY_MODE_CTRL QSGMII/USXGMII PHY mode control on Port 1 This bit controls the Clause 37 auto-negotiation when operating in QSGMII/USXGMII (Port 1) PHY mode. QSGMI: When this bit is set to 1, QSGMII/SGMII_PCS advertises the values of input ports PCS_qsgmii_link_sts_p1_i, PCS_qsgmii_link_speed_p1_i and PCS_qsgmii_full_duplex_p1_i during QSGMII(Port 1) auto-negotiation. When this bit is set to 0, QSGMII(Port 1) auto-negotiation advertises the values programmed to: bit 4 (SGMII_LINK_STS) of VR_MII_1_AN_CTRL Register bit 13 (ss13) and 6 (ss6) of SR_MII_1_CTRL Register and bit 5 (FD) of SR_MII_1_AN_ADV Register

QSGMII/SGMII_PCS_VR_MII_2_AN_CTRL

Address: Operational Base + offset (0x0E0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RU	0x00	Reserved_15_10 Reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	IND_TX_EN Independent Transmit Enable If this bit is set to 1, QSGMII/SGMII_PCS is able to transmit the port 1 GMII Tx data, irrespective of its receive link status during QSGMII mode (provided auto-negotiation is not enabled). If this bit is set to 0, QSGMII/SGMII_PCS sends IDLE (for port 1) till its receiver has attained synchronization.
8	RW	0x0	MII_CTRL MII Control This bit controls the width of the MAC interface (connected to GMII port 1) when operating at 10 Mbps or 100 Mbps 0: 4-bit MII 1: 8-bit MII This bit also controls the PCS_mii_ctrl_p1_o signal which is used for external clock multiplexing of the clk_mii_tx_p1_i/clk_xgmii_tx_p1_i and clk_mii_rx_p1_i/clk_xgmii_rx_p1_i signals
7:5	RO	0x0	Reserved_7_5 Reserved
4	RW	0x0	SGMII_LINK_STS QSGMII/USXGMII Link Status (port 1) This bit is used in Bit 15 of the Tx_Config_Reg during Clause 37 auto-negotiation (along port 1) when QSGMII/SGMII_PCS is programmed as QSGMII-PHY (or as USXGMII-PHY) and when PHY_MODE_CTRL bit of VR_MII_1_DIG_CTRL1 Register is 0 . 0: Link Down 1: Link Up
3	RO	0x0	TX_CONFIG Transmit Configuration This field reflects the value of TX_CONFIG of VR_MII_AN_CTRL Register.
2:1	RO	0x0	PCS_MODE PCS Mode This field reflects the value of PCS_MODE of VR_MII_AN_CTRL Register for configurations with QSGMII support. For other configurations, this field returns 2'b00.
0	RW	0x0	MII_AN_INTR_EN Clause 37 AN Complete Interrupt Enable (port 2) When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete (on port 2) interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

QSGMII/SGMII_PCS_VR_MII_2_AN_INTR_STS

Address: Operational Base + offset (0x0E0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	Reserved_15 Reserved

Bit	Attr	Reset Value	Description
14:8	RO	0x00	USXG_AN_STS USXGMII Clause 37 AN Status (along Port 2) This field is valid only when clause 37 auto-negotiation is complete in USXGMII Mode along Port 2. It indicates the status received from remote link after the USXGMII auto-negotiation is complete. USXG_AN_STS[6] 0: Link is Down 1: Link is Up USXG_AN_STS[5] 0: Half Duplex 1: Full Duplex USXG_AN_STS[4:2] 000: 10 Mbps speed link 001: 100 Mbps speed link 010: 1000 Mbps speed link 011: 10 Gbps speed link 100: 2.5 Gbps speed link 101: 5 Gbps speed link USXG_AN_STS[1] 1: EEE supported 0: EEE not supported USXG_AN_STS[0] 1: EEE clock-stop supported 0: EEE clock-stop not supported Note:This field is present only in configurations with Multi-port USXGMII support.
7	RO	0x0	Reserved_7 Reserved
6	RO	0x0	LP_CK_STP Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or enable in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. Note:This field is present only in configurations with QSGMII
5	RO	0x0	LP_EEE_CAP Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 1 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. Note:This field is present only in configurations with QSGMII.

Bit	Attr	Reset Value	Description
4:1	RO	0x0	CL37_ANSGM_STS Clause 37 AN QSGMII Status (port 2) This field is valid only when the PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. It indicates the status received from remote link partner. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link CL37_ANSGM_STS[3] 0: Link is Down 1: Link is Up Note:This field is present only in configurations with QSGMII.
0	RW	0x0	CL37_ANCMPLT_INTR Clause 37 AN Complete Interrupt (SS,WC Type) The QSGMII/SGMII_PCS sets this bit when Clause 37 auto-negotiation is complete for port 1. The host must clear this bit by writing 0 to it.

QSGMII/SGMII_PCS_VR_MII_2_TC

Address: Operational Base + offset (0x0E000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	TPE Test Pattern Enable Lanes
1:0	RO	0x0	TP Test Pattern Select

QSGMII/SGMII_PCS_VR_MII_2_DBG_CTRL

Address: Operational Base + offset (0x0E0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	TX_PMBL_CTL Transmit Preamble Control This bit merely reflects the value of TX_PMBL_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
7	RO	0x0	RX_SYNC_CTL Receive Synchronization Control . This bit merely reflects the value of RX_SYNC_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
6	RO	0x0	RX_DT_EN_CTL Rx Data Enable Control. This bit merely reflects the value of RX_DT_EN_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).

Bit	Attr	Reset Value	Description
5	RO	0x0	SUPRESS_EEE_LOS_DET Suppress EEE Loss of Signal Detection. This bit merely reflects the value of SUPRESS_EEE_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
4	RO	0x0	SUPRESS_LOS_DET Suppress Loss of Signal Detection This bit merely reflects the value of SUPRESS_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations)
3:1	RO	0x0	reserved
0	RW	0x0	RESTAR_SYNC Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on port 1. The host must clear this bit to 0 before setting it to 1 next time.

QSGMII/SGMII_PCS_VR_MII_2_EEE_MCTRL0

Address: Operational Base + offset (0x0E0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x8	CLKSTOP Clock Stop
11:8	RO	0x9	MULT_FACT_100NS 100 ns Clock Tic Multiplying Factor
7	RO	0x1	RX_EN_CTRL Rx Control Enable
6	RO	0x0	SIGN_BIT Effective 100 ns Tic Value
5	RO	0x0	Reserved_5 Reserved
4	RO	0x1	TX_EN_CTRL Tx Control Enable
3	RO	0x1	RX_QUIET_EN Rx Quiet Enable
2	RO	0x1	TX_QUIET_EN Tx Quiet Enable
1	RO	0x0	LRX_EN LPI Rx Enable
0	RO	0x0	LTX_EN LPI Tx Enable

QSGMII/SGMII_PCS_VR_MII_2_EEE_TXTIMER

Address: Operational Base + offset (0x0E0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	TSL_RES TSL Resolution

QSGMII/SGMII_PCS_VR_MII_2_EEE_RXTIMER

Address: Operational Base + offset (0x0E0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:8	RO	0x00	TWR_RES TWR Resolution
7:0	RO	0x00	RES_100U 100 us Resolution

QSGMII/SGMII_PCS_VR_MII_2_LINK_TIMER_CTRL

Address: Operational Base + offset (0x0E0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	VR_MII_1_LINK_TIMER_CTRL Programmable Link Timer Value for Clause 37 auto-negotiation.

QSGMII/SGMII_PCS_VR_MII_2_EEE_MCTRL1

Address: Operational Base + offset (0x0E002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	TRN_LPI Transparent Tx LPI Mode Enable

QSGMII/SGMII_PCS_VR_MII_2_DIG_STS

Address: Operational Base + offset (0x0E0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	LTX_STATE LPI Transmit State. This field reflects the value of LTX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).
12:10	RO	0x0	LRX_STATE LPI Receive State This field reflects the value of LRX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).

Bit	Attr	Reset Value	Description
9	RO	0x0	INV_XGM_CHAR Invalid XGMII Character (RO,LH Type) -Port 2 This bit indicates an invalid XGMII character on the Transmit path (port 2). 0: No Invalid XGMII character 1: Invalid character This bit is set when one of the following conditions is true on the XGMII interface: |Q| is detected on a lane other than Lane 0. |Q| is detected on Lane 0 and also any of the following conditions is true: No 8'h00 data in Lane 1. No 8'h00 data in Lane 2. No 8'h01 or 8'h02 data on Lane 3. |E| or |T| is encountered in non-data phase and |Q| is encountered in data phase. |D| is detected during the Idle phase (after Terminate and before valid SOF). |I| is detected during the data phase (after SOF and before Terminate). Note: This field is present only for Multi-port USXGMII configurations.
8	RO	0x0	INV_XGM_T Invalid XGMII T Character (RO,LH Type) -Port 2 This bit indicates that the transmit data (port 2) received on XGMII has an invalid Terminate character. 0: Normal operation 1: Invalid Terminate character The following can cause an invalid Terminate character: In Terminate column, before lane corresponds to the |T| character, there is a |I| or |Q| character. In Terminate column, after lane corresponds to the |T| character, there is a non-|I| character Note:This field is present only for Multi-port USXGMII configurations.
7	RO	0x0	INV_XGM_SOP Invalid XGMII Start Character (RO,LH Type) -Port 2 This bit indicates that the XGMII transmit (Port 1) frame contains invalid SOP character. 0: Normal operation 1: Invalid SOP character An invalid SOP event occurs when a |S| character is detected in a lane other than Lane 0. Note:This field is present only for Multi-port USXGMII configurations.
6	RO	0x0	RXFIFO_OVF Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow for port 2. 0: Normal operation 1: FIFO overflow

Bit	Attr	Reset Value	Description
5	RO	0x0	RXFIFO_UNDF Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow for port 2. 0: Normal operation 1: FIFO underflow
4:2	RO	0x4	PSEQ_STATE Reserved
1	RO	0x0	LB_ACTIVE Reserved
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_VR_MII_2_ICG_ERRCNT1

Address: Operational Base + offset (0x0E0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	EC0 Invalid Code Group Count -Port 2 (RO,LH Type) This field gives the invalid code group count in port 2 (of QSGMII) when Bit 4 of VR MII_1 MMD Digital Error Count Select Register is set to 1.

QSGMII/SGMII_PCS_VR_MII_2_DIG_CTRL2

Address: Operational Base + offset (0x0E0384)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	TX_POL_INV_0 Tx Polarity Invert on Lane 0
3:1	RO	0x0	Reserved_3_1 Reserved
0	RO	0x0	RX_POL_INV_0 Rx Polarity Invert on Lane 0

QSGMII/SGMII_PCS_VR_MII_2_DIG_ERRCNT_SEL

Address: Operational Base + offset (0x0E0388)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	INV_EC_EN Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors (on port 1) is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR_MII_1_ICG_ERRCNT1 Register.
3:1	RO	0x0	Reserved_3_1 Reserved
0	RW	0x0	COR Clear on Read When this bit is set and the host reads port 2 error counter (VR_MII_1_ICG_ERRCNT1 Register), that counter is cleared after the read cycle. 0: Normal operation 1: Clear error counter that is read

QSGMII/SGMII_PCS_SR_MII_3_CTRL

Address: Operational Base + offset (0x100000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RST Soft Reset (RW,SC Type) For Non-Synopsys PHY configurations: When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface
14	RO	0x0	LBE Loopback Enable This bit reflects the value of LBE bit of SR_MII_CTRL Register.
13	RW	0x0	SS13 Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed of GMII/XGMII port 3. Speed encoding as follows: For QSGMII: When SS6=1 and SS13=0, speed is 1000 Mbps When SS6=0 and SS13=1, speed is 100 Mbps When SS6=0 and SS13=0, speed is 10 Mbps
12	RW	0x0	AN_ENABLE Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 auto-negotiation process for port 3.
11	RW	0x0	LPM Power-Down Mode This bit controls the power-down mode of the QSGMII/SGMII_PCS. 0: Normal operation 1: The QSGMII/SGMII_PCS goes to the power-down mode along with the PHY. For non-Synopsys PHY, the PCS_pdown_o port is asserted. When the host clears this bit, the QSGMII/SGMII_PCS resumes the normal operation. In a Synopsys PHY configuration, after clearing this bit, the host must wait until Bits[4:2] of VR_XS_PCS_DIG_STS/VR_MII_DIG_STS Register indicate that the QSGMII/SGMII_PCS is in the normal state
10	RO	0x0	Reserved_10 Reserved
9	RW	0x0	RESTART_AN Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the QSGMII/SGMII_PCS initiates the auto-negotiation process for port 3. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The QSGMII/SGMII_PCS clears this bit after restarting the auto-negotiation.

Bit	Attr	Reset Value	Description
8	RW	0x1	DUPLEX_MODE Duplex Mode This bit specifies the duplex mode of the QSGMII/SGMII_PCS along port 3. 0: Half duplex 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process.
7	RO	0x0	Reserved_7 Reserved
6	RW	0x1	SS6 Speed Selection This bit, along with the SS5 and SS13 bits of this register indicates the speed of operation of GMII/XGMII Port 3. For more information, see description of the SS13 bit.
5	RO	0x0	SS5 Speed Selection This bit, along with SS6 and SS13 bits, control the speed of operation of XGMII/GMII Port 3. For more information, see description of the SS13 bit.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_3_STS

Address: Operational Base + offset (0x100004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ABL100T4 100BASE-T4 Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
14	RO	0x0	FD100ABL 100BASE-X Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
13	RO	0x0	HD100ABL 100BASE-X Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
12	RO	0x0	FD10ABL 10 Mbps Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
11	RO	0x0	HD10ABL 10 Mbps Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality

Bit	Attr	Reset Value	Description
10	RO	0x0	FD100T 100BASE-T2 Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
9	RO	0x0	HD100T 100BASE-T2 Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
8	RO	0x1	EXT_STS_ABL Extended Status Information 0: No Extended Status information is present at register address 16'h000F of this MMD device. 1: Extended Status information is present at register address 16'h000F of this MMD device. QSGMII/SGMII_PCS returns this bit as 1.
7	RO	0x0	UN_DIR_ABL Unidirectional Ability 1: The QSGMII/SGMII_PCS is able to transmit GMII irrespective of whether device has determined the valid link or not. 0: The QSGMII/SGMII_PCS is able to transmit GMII only when the device has determined the valid link. The QSGMII/SGMII_PCS always returns this bit as 0.
6	RO	0x0	MF_PRE_SUP MF Preamble Suppression 1: The QSGMII/SGMII_PCS accepts the MDIO frames with preamble suppressed. 0: The QSGMII/SGMII_PCS does not accept the MDIO frames with preamble suppressed. This bit is always set to 0
5	RO	0x0	AN_CMPL Auto-negotiation Complete for Port 3 1: The AN process is complete 0: The AN process is not complete This bit returns 0 if AN_ENABLE of SR_MII_1_CTRL Register is set to 0.
4	RO	0x0	RF Remote Fault This register bit is shared with RF bit of SR_MII_STS register. The value returned by this field should be ignored by the software as it is not valid in QSGMII/SGMII/USXGMII Modes
3	RO	0x1	AN_ABL Auto-negotiation Ability The QSGMII/SGMII_PCS always returns this bit as 1. 1: The QSGMII/SGMII_PCS is able to perform auto-negotiation. 0: The QSGMII/SGMII_PCS is not able to perform auto-negotiation
2	RO	0x0	LINK_STS Link Status This register bit is shared with RLU bit of SR_MII_STS register.
1	RO	0x0	Reserved_1 Reserved

Bit	Attr	Reset Value	Description
0	RO	0x1	EXT_REG_CAP Extended Register Capability 1: Extended Register capability exists. This bit is always set to 1. 0: Extended Register capability does not exist.

QSGMII/SGMII_PCS_SR_MII_3_DEV_ID1

Address: Operational Base + offset (0x100008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x7996	VS_MII_DEV_OUI_3_18 Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer. This register reflects the same value as that of SR_MII_DEV_ID1 register.

QSGMII/SGMII_PCS_SR_MII_3_DEV_ID2

Address: Operational Base + offset (0x10000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x33	VS_MMD_DEV_OUI_19_24 Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer.
9:4	RO	0x00	VS_MMD_DEV_MMN_5_0 Model Number This field contains the 5-bit Model Number of the device.
3:0	RO	0x0	VS_MMD_DEV_RN_3_0 Revision Number This field contains the 4-bit Revision Number of the device

QSGMII/SGMII_PCS_SR_MII_3_AN_ADV

Address: Operational Base + offset (0x100010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP Next Page This bit reflects the value of NP bit of SR_MII_AN_ADV Register.
14	RO	0x0	Reserved_14 Reserved
13:12	RO	0x0	RF Remote Fault This bit reflects the value of RF bit of SR_MII_AN_ADV Register.
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	PAUSE Pause Ability. This bit reflects the value of PAUSE bit of SR_MII_AN_ADV Register
6	RO	0x0	HD Half Duplex This bit reflects the value of HD bit of SR_MII_AN_ADV Register.

Bit	Attr	Reset Value	Description
5	RW	0x1	FD Full Duplex When this bit is set, it indicates the device (port 1) can operate in full-duplex mode. This bit is used in Clause 37 auto-negotiation (Tx_Config_Reg) done by port 1, when QSGMII/SGMII_PCS is configured as PHY-side QSGMII.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_3_LP_BABL

Address: Operational Base + offset (0x100014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	LP_NP Next Page
14	RO	0x0	LP_ACK ACK bit from the Link Partner
13:12	RO	0x0	LP_RF Remote Fault
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	LP_PAUSE Pause Ability
6	RO	0x0	LP_HD Half Duplex
5	RO	0x0	LP_FD Full Duplex
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_3_AN_EXPN

Address: Operational Base + offset (0x100018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	LD_NP_ABL Local Device NP Able 1: The local device has the next page ability 0: The local device does not have the next page ability The QSGMII/SGMII_PCS always returns this bit as 0 because it does not support Next Page.
1	RO	0x0	PG_RCVD Page Received (RO, LH Type) This bit indicates that the local device received a page from the link partner (during port 1 auto-negotiation). 1: The local device received a new page 0: The local device did not receive a new page
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_SR_MII_3_EXT_STS

Address: Operational Base + offset (0x10003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15	RO	0x1	CAP_1G_X_FD 1000BASE-X Full-Duplex Capable
14	RO	0x1	CAP_1G_X_HD 1000BASE-X Half-Duplex Capable
13	RO	0x0	CAP_1G_T_FD 1000BASE-T Full-Duplex Capable
12	RO	0x0	CAP_1G_T_HD 1000BASE-T Half-Duplex Capable
11:0	RO	0x000	Reserved_11_0 Reserved

QSGMII/SGMII_PCS_VR_MII_3_DIG_CTRL1

Address: Operational Base + offset (0x120000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	VR_RST Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: For Synopsys PHY: This bit is self cleared when Bits[4:2] in VR_MII_DIG_STS Register are equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. For Non-Synopsys PHY:This bit is self cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface Note: For information about the read or write access for any register during the reset process, see "Special Case Register Access" section.
14	RW	0x0	R2TLBE Rx to Tx Loopback Enable This bit controls the loopback path from the GMII/XGMII Rx to the GMII/XGMII Tx at the GMII/XGMII interface (port 3). 0: Loopback path is disabled 1: Loopback path is enabled
13	RO	0x1	EN_VSMMD1 Enable Vendor-Specific MMD1 This is a read-only bit which reflects the value of EN_VSMMD1 bit of VR_MII_DIG_CTRL1 Register.
12	RO	0x0	CL37_BP Enable Clause 37 AN in Backplane Configuration This is a read-only bit which reflects the value of CL37_BP bit of VR_MII_DIG_CTRL1 Register.
11	RO	0x0	PWRSV Reserved
10	RW	0x1	CS_EN Clock Stop Enable 1: The PHY may stop the clock during LPI mode 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC (connected to GMII Port 1) during Rx LPI mode. Note: This field is valid only in QSGMII mode

Bit	Attr	Reset Value	Description
9	RW	0x0	MAC_AUTO_SW Automatic Speed Mode Change after CL37 AN (for port 3) If this field is set to 1, QSGMII/SGMII_PCS automatically switches to the negotiated USXGMII/QSGMII(port3) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when QSGMII/SGMII_PCS is configured as MAC-side USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, QSGMII/SGMII_PCS operates at the speed/duplex mode as per the values programmed to SR_MII_1_CTRL Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR_MII_1_AN_INTR_STS Register and then program SR_MII_1_CTRL Register appropriately. If this bit is set to 1 in QSGMII mode, PCS_qsgmii_link_sts_p1_o, PCS_link_speed_p1_o and PCS_qsgmii_full_duplex_p1_o outputs reflect the auto-negotiated values, that is, values from CL37_ANSGM_STS field of VR_MII_1_AN_INTR_STS Register. For USXGMII mode, if clk_xgmii_tx_p1_i and clk_xgmii_rx_p1_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USRA_RST' bit prior to starting packet transfer in the new speed mode.
8	RO	0x0	INIT INIT This bit reflects the value of INIT bit of VR_MII_DIG_CTRL1 Register.
7	RO	0x0	MSK_RD_ERR Mask Running Disparity Error This bit reflects the value of MSK_RD_ERR bit of VR_MII_DIG_CTRL1 Register.
6	RW	0x0	PRE_EMP Pre-emption Packet Enable. This bit should be set to 1 to allow the QSGMII/SGMII_PCS to properly receive/transmit pre-emption packets along GMII port 1, when operating in 10M/100M Modes.

Bit	Attr	Reset Value	Description
5	RO	0x0	USRA_RST USXGMII Rate Adaptor Reset (Port 1) This bit can be set to 1 to reset/initialize the USXGMII Rate Adaptor Logic (for port 1) inside QSGMII/SGMII_PCS. The Rate Adaptor Logic maps GMII data to XGMII (and vice-versa in Rx path) data and perform data replication for lower USXGMII speeds. This is a self-clear bit (RW,SC) and clears itself after the reset of Tx and Rx Rate Adaptor Logic is complete. After setting this bit to 1, application should poll this bit till it self-clears. Note: If CLKCOMP=Enabled, this bit also initializes the clock compensation FIFO (corresponding to port 1). When this bit is programmed to 1, RXFIFO_OVF/RXFIFO_UNF bits of VR_MII_1_DIG_STS Register might get set incorrectly. Therefore, read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits are reliable.
4	RO	0x0	DTXLANED_0 Tx Lane 0 Disable This bit reflects the value of DTXLANED_0 bit of VR_MII_DIG_CTRL1 Register.
3	RO	0x0	CL37_TMR_OVR_RIDE Over-Ride Control for CL37 Link Timer. This bit reflects the value of CL37_TMR_OVR_RIDE bit of VR_MII_DIG_CTRL1 Register.
2	RO	0x0	EN_2_5G_MODE Enable 2.5G GMII Mode (GMII interface over-clocked 2.5 This bit reflects the value of EN_2_5G_MODE bit of VR_MII_DIG_CTRL1 Register.
1	RO	0x0	BYP_PWRUP Reserved
0	RO	0x0	PHY_MODE_CTRL QSGMII/USXGMII PHY mode control on Port 3 This bit controls the Clause 37 auto-negotiation when operating in QSGMII/USXGMII (Port 1) PHY mode. QSGMI: When this bit is set to 1, QSGMII/SGMII_PCS advertises the values of input ports PCS_qsgmii_link_sts_p1_i, PCS_qsgmii_link_speed_p1_i and PCS_qsgmii_full_duplex_p1_i during QSGMII(Port 3) auto-negotiation. When this bit is set to 0, QSGMII(Port 3) auto-negotiation advertises the values programmed to: bit 4 (SGMII_LINK_STS) of VR_MII_1_AN_CTRL Register bit 13 (ss13) and 6 (ss6) of SR_MII_1_CTRL Register and bit 5 (FD) of SR_MII_1_AN_ADV Register

QSGMII/SGMII_PCS_VR_MII_3_AN_CTRL

Address: Operational Base + offset (0x120004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	Reserved_15_10 Reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	IND_TX_EN Independent Transmit Enable If this bit is set to 1, QSGMII/SGMII_PCS is able to transmit the port 1 GMII Tx data, irrespective of its receive link status during QSGMII mode (provided auto-negotiation is not enabled). If this bit is set to 0, QSGMII/SGMII_PCS sends IDLE (for port 1) till its receiver has attained synchronization.
8	RW	0x0	MII_CTRL MII Control This bit controls the width of the MAC interface (connected to GMII port 1) when operating at 10 Mbps or 100 Mbps 0: 4-bit MII 1: 8-bit MII This bit also controls the PCS_mii_ctrl_p1_o signal which is used for external clock multiplexing of the clk_mii_tx_p1_i/clk_xgmii_tx_p1_i and clk_mii_rx_p1_i/clk_xgmii_rx_p1_i signals
7:5	RO	0x0	Reserved_7_5 Reserved
4	RW	0x0	SGMII_LINK_STS QSGMII/USXGMII Link Status (port 1) This bit is used in Bit 15 of the Tx_Config_Reg during Clause 37 auto-negotiation (along port 1) when QSGMII/SGMII_PCS is programmed as QSGMII-PHY (or as USXGMII-PHY) and when PHY_MODE_CTRL bit of VR_MII_1_DIG_CTRL1 Register is 0 . 0: Link Down 1: Link Up
3	RO	0x0	TX_CONFIG Transmit Configuration This field reflects the value of TX_CONFIG of VR_MII_AN_CTRL Register.
2:1	RO	0x0	PCS_MODE PCS Mode This field reflects the value of PCS_MODE of VR_MII_AN_CTRL Register for configurations with QSGMII support. For other configurations, this field returns 2'b00.
0	RW	0x0	MII_AN_INTR_EN Clause 37 AN Complete Interrupt Enable (port 2) When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete (on port 2) interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

QSGMII/SGMII_PCS_VR_MII_3_AN_INTR_STS

Address: Operational Base + offset (0x120008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	Reserved_15 Reserved

Bit	Attr	Reset Value	Description
14:8	RO	0x00	USXG_AN_STS USXGMII Clause 37 AN Status (along Port 2) This field is valid only when clause 37 auto-negotiation is complete in USXGMII Mode along Port 2. It indicates the status received from remote link after the USXGMII auto-negotiation is complete. USXG_AN_STS[6] 0: Link is Down 1: Link is Up USXG_AN_STS[5] 0: Half Duplex 1: Full Duplex USXG_AN_STS[4:2] 000: 10 Mbps speed link 001: 100 Mbps speed link 010: 1000 Mbps speed link 011: 10 Gbps speed link 100: 2.5 Gbps speed link 101: 5 Gbps speed link USXG_AN_STS[1] 1: EEE supported 0: EEE not supported USXG_AN_STS[0] 1: EEE clock-stop supported 0: EEE clock-stop not supported Note:This field is present only in configurations with Multi-port USXGMII support.
7	RO	0x0	Reserved_7 Reserved
6	RO	0x0	LP_CK_STP Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or enable in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. Note:This field is present only in configurations with QSGMII
5	RO	0x0	LP_EEE_CAP Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 1 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. Note:This field is present only in configurations with QSGMII.

Bit	Attr	Reset Value	Description
4:1	RO	0x0	CL37_ANSGM_STS Clause 37 AN QSGMII Status (port 2) This field is valid only when the PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 2. It indicates the status received from remote link partner. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link CL37_ANSGM_STS[3] 0: Link is Down 1: Link is Up Note:This field is present only in configurations with QSGMII.
0	RW	0x0	CL37_ANCMPLT_INTR Clause 37 AN Complete Interrupt (SS,WC Type) The QSGMII/SGMII_PCS sets this bit when Clause 37 auto-negotiation is complete for port 1. The host must clear this bit by writing 0 to it.

QSGMII/SGMII_PCS_VR_MII_3_TC

Address: Operational Base + offset (0x12000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	TPE Test Pattern Enable Lanes
1:0	RO	0x0	TP Test Pattern Select

QSGMII/SGMII_PCS_VR_MII_3_DBG_CTRL

Address: Operational Base + offset (0x120014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	TX_PMBL_CTL Transmit Preamble Control This bit merely reflects the value of TX_PMBL_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
7	RO	0x0	RX_SYNC_CTL Receive Synchronization Control . This bit merely reflects the value of RX_SYNC_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
6	RO	0x0	RX_DT_EN_CTL Rx Data Enable Control. This bit merely reflects the value of RX_DT_EN_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).

Bit	Attr	Reset Value	Description
5	RO	0x0	SUPRESS_EEE_LOS_DET Suppress EEE Loss of Signal Detection. This bit merely reflects the value of SUPRESS_EEE_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
4	RO	0x0	SUPRESS_LOS_DET Suppress Loss of Signal Detection This bit merely reflects the value of SUPRESS_LOS_DET field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations)
3:1	RO	0x0	reserved
0	RW	0x0	RESTAR_SYNC Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on port 1. The host must clear this bit to 0 before setting it to 1 next time.

QSGMII/SGMII_PCS_VR_MII_3_EEE_MCTRL0

Address: Operational Base + offset (0x120018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x8	CLKSTOP Clock Stop
11:8	RO	0x9	MULT_FACT_100NS 100 ns Clock Tic Multiplying Factor
7	RO	0x1	RX_EN_CTRL Rx Control Enable
6	RO	0x0	SIGN_BIT Effective 100 ns Tic Value
5	RO	0x0	Reserved_5 Reserved
4	RO	0x1	TX_EN_CTRL Tx Control Enable
3	RO	0x1	RX_QUIET_EN Rx Quiet Enable
2	RO	0x1	TX_QUIET_EN Tx Quiet Enable
1	RO	0x0	LRX_EN LPI Rx Enable
0	RO	0x0	LTX_EN LPI Tx Enable

QSGMII/SGMII_PCS_VR_MII_3_EEE_TXTIMER

Address: Operational Base + offset (0x120020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	TSL_RES TSL Resolution

QSGMII/SGMII_PCS_VR_MII_3_EEE_RXTIMER

Address: Operational Base + offset (0x120024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:8	RO	0x00	TWR_RES TWR Resolution
7:0	RO	0x00	RES_100U 100 us Resolution

QSGMII/SGMII_PCS_VR_MII_3_LINK_TIMER_CTRL

Address: Operational Base + offset (0x120028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	VR_MII_1_LINK_TIMER_CTRL Programmable Link Timer Value for Clause 37 auto-negotiation.

QSGMII/SGMII_PCS_VR_MII_3_EEE_MCTRL1

Address: Operational Base + offset (0x12002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	TRN_LPI Transparent Tx LPI Mode Enable

QSGMII/SGMII_PCS_VR_MII_3_DIG_STS

Address: Operational Base + offset (0x120040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	LTX_STATE LPI Transmit State. This field reflects the value of LTX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).
12:10	RO	0x0	LRX_STATE LPI Receive State This field reflects the value of LRX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).

Bit	Attr	Reset Value	Description
9	RO	0x0	INV_XGM_CHAR Invalid XGMII Character (RO,LH Type) -Port 2 This bit indicates an invalid XGMII character on the Transmit path (port 2). 0: No Invalid XGMII character 1: Invalid character This bit is set when one of the following conditions is true on the XGMII interface: |Q| is detected on a lane other than Lane 0. |Q| is detected on Lane 0 and also any of the following conditions is true: No 8'h00 data in Lane 1. No 8'h00 data in Lane 2. No 8'h01 or 8'h02 data on Lane 3. |E| or |T| is encountered in non-data phase and |Q| is encountered in data phase. |D| is detected during the Idle phase (after Terminate and before valid SOF). |I| is detected during the data phase (after SOF and before Terminate). Note: This field is present only for Multi-port USXGMII configurations.
8	RO	0x0	INV_XGM_T Invalid XGMII T Character (RO,LH Type) -Port 2 This bit indicates that the transmit data (port 2) received on XGMII has an invalid Terminate character. 0: Normal operation 1: Invalid Terminate character The following can cause an invalid Terminate character: In Terminate column, before lane corresponds to the |T| character, there is a |I| or |Q| character. In Terminate column, after lane corresponds to the |T| character, there is a non-|I| character Note:This field is present only for Multi-port USXGMII configurations.
7	RO	0x0	INV_XGM_SOP Invalid XGMII Start Character (RO,LH Type) -Port 2 This bit indicates that the XGMII transmit (Port 1) frame contains invalid SOP character. 0: Normal operation 1: Invalid SOP character An invalid SOP event occurs when a |S| character is detected in a lane other than Lane 0. Note:This field is present only for Multi-port USXGMII configurations.
6	RO	0x0	RXFIFO_OVF Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow for port 2. 0: Normal operation 1: FIFO overflow

Bit	Attr	Reset Value	Description
5	RO	0x0	RXFIFO_UNDF Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow for port 2. 0: Normal operation 1: FIFO underflow
4:2	RO	0x4	PSEQ_STATE Reserved
1	RO	0x0	LB_ACTIVE Reserved
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_VR_MII_3_ICG_ERRCNT1

Address: Operational Base + offset (0x120044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	EC0 Invalid Code Group Count -Port 2 (RO,LH Type) This field gives the invalid code group count in port 2 (of QSGMII) when Bit 4 of VR MII_1 MMD Digital Error Count Select Register is set to 1.

QSGMII/SGMII_PCS_VR_MII_3_DIG_CTRL2

Address: Operational Base + offset (0x120384)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	TX_POL_INV_0 Tx Polarity Invert on Lane 0
3:1	RO	0x0	Reserved_3_1 Reserved
0	RO	0x0	RX_POL_INV_0 Rx Polarity Invert on Lane 0

QSGMII/SGMII_PCS_VR_MII_3_DIG_ERRCNT_SEL

Address: Operational Base + offset (0x120388)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	INV_EC_EN Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors (on port 1) is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR_MII_1_ICG_ERRCNT1 Register.
3:1	RO	0x0	Reserved_3_1 Reserved
0	RW	0x0	COR Clear on Read When this bit is set and the host reads port 2 error counter (VR_MII_1_ICG_ERRCNT1 Register), that counter is cleared after the read cycle. 0: Normal operation 1: Clear error counter that is read

QSGMII/SGMII_PCS_SR_VSMMD_PMA_ID1

Address: Operational Base + offset (0x180000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	PMADOUI_3_18 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_PMA_ID2

Address: Operational Base + offset (0x180004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RO	0x0	PMADOUI_19_24 Reserved
9:4	RO	0x00	PMADMMN_5_0 Reserved
3:0	RO	0x0	PMADRN_3_0 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_DEV_ID1

Address: Operational Base + offset (0x180008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	VSDOUI_3_18 Organizationally Unique Identifier[3:18] for Vendor-Specific MMD1 This field contains Bits[18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. You can configure the value of each MMD using coreConsultant. Access Type: RW: For configurations with IEEE_REG_WR_SUPPORT=Enabled. RO: For all other configurations.

QSGMII/SGMII_PCS_SR_VSMMD_DEV_ID2

Address: Operational Base + offset (0x18000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	VSDOUI_19_24 Organizationally Unique Identifier[19:24] for Vendor-Specific MMD1 This field contains Bits[24:19] of the device manufacturer's 24 bit OUI. The QSGMII/SGMII_PCS offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer.
9:4	RO	0x00	VSDMMN_5_0 Model Number for Vendor-Specific MMD1 This field contains the 6-bit Model number of the vendor-specific MMD1.You can configure the default value through coreConsultant. Access Type: RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. RO: For all other configurations.

Bit	Attr	Reset Value	Description
3:0	RO	0x0	VSDRN_3_0 Revision Number for Vendor-Specific MMD1 This field contains the 4-bit Revision number of the vendor-specific MMD1. You can configure the default value through coreConsultant. Access Type: RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. RO: For all other configurations.

QSGMII/SGMII_PCS_SR_VSMMD_PCS_ID1

Address: Operational Base + offset (0x180010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x7996	PCSDOUI_3_18 Organizationally Unique Identifier[3:18] for PCS MMD This field contains Bits[18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. The default value of this register is similar to the default value of SR XS or PCS MMD Device Identifier Register 1. The value written in this register is reflected in SR XS or PCS MMD Device Identifier Register 1.

QSGMII/SGMII_PCS_SR_VSMMD_PCS_ID2

Address: Operational Base + offset (0x180014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x33	PCSDOUI_19_24 Organizationally Unique Identifier[19:24] for PCS MMD This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2.
9:4	RO	0x2d	PCSDMMN_5_0 Model Number for XS or PCS MMD This field contains the 6-bit Model number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2.
3:0	RO	0x0	PCSDRN_3_0 Revision Number for XS or PCS MMD This field contains the 4-bit Revision number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2.

QSGMII/SGMII_PCS_SR_VSMMD_AN_ID1

Address: Operational Base + offset (0x180018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ANDOUI_3_18 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_AN_ID2

Address: Operational Base + offset (0x18001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	ANDOUI_19_24 Reserved
9:4	RO	0x00	ANDMMN_5_0 Reserved
3:0	RO	0x0	ANDRN_3_0 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_STS

Address: Operational Base + offset (0x180020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	VSDP Control MMD Device Present This field indicates if the control MMD device is present and responding to this address: 10: Device responding at this address 11, 01, or 00: No device responding at this address
13:0	RO	0x0000	Reserved_13_0 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_CTRL

Address: Operational Base + offset (0x180024)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	PD_CTRL Power Down Control This bit is used to control the output port 'PCS_pdown_o'. If this bit is set, PCS_pdown_o port is NOT asserted when LPM (Low Power Enable) bit is programmed to 1. If this bit is low, PCS_down_o port is asserted when LPM (Low Power Enable) bit is programmed to 1.
4	RW	0x0	FASTSIM Fast Simulation Enable When set, this bit indicates that the Fast simulation is enabled. When this bit is set to 1, all IEEE Std 802.3 defined long timers, implemented in the QSGMII/SGMII_PCS are reduced to shorter time period to reduce the simulation time. The long timers are implemented in Clause 73 and Clause 37 auto-negotiation modules and also EEE Tx and Rx modules. Testable: untestable
3	RW	0x0	PMA_MMD_EN Reserved

Bit	Attr	Reset Value	Description
2	RW	0x1	MII_MMD_EN VS MMD Enable When set, this bit indicates that the vendor-specific MMD1 device is accessible. When reset, this bit indicates that the vendor-specific MMD2 (MII MMD) device is not accessible.
1	RO	0x0	PCS_XS_MMD_EN Reserved
0	RO	0x0	AN_MMD_EN Reserved

QSGMII/SGMII_PCS_SR_VSMMD_PKGID1

Address: Operational Base + offset (0x18038)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	MMDPOUI_3_18 Reserved

QSGMII/SGMII_PCS_SR_VSMMD_PKGID2

Address: Operational Base + offset (0x18003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	MMDPOUI_19_24 Reserved
9:4	RO	0x00	MMDPMMN_5_0 Reserved
3:0	RO	0x0	MMDPRN_3_0 Reserved

QSGMII/SGMII_PCS_SR_MII_CTRL

Address: Operational Base + offset (0x1C0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	RST Soft Reset (RW,SC Type) For Non-Synopsys PHY configurations: When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface
14	RW	0x0	LBE Loopback Enable This bit reflects the value of LBE bit of SR_MII_CTRL Register.
13	RW	0x0	SS13 Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed of GMII/XGMII port 1. Speed encoding as follows: For QSGMII: When SS6=1 and SS13=0, speed is 1000 Mbps When SS6=0 and SS13=1, speed is 100 Mbps When SS6=0 and SS13=0, speed is 10 Mbps

Bit	Attr	Reset Value	Description
12	RW	0x0	AN_ENABLE Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 auto-negotiation process for port 1.
11	RW	0x0	LPM Power-Down Mode This bit controls the power-down mode of the QSGMII/SGMII_PCS. 0: Normal operation 1: The QSGMII/SGMII_PCS goes to the power-down mode along with the PHY. For non-Synopsys PHY, the PCS_pdown_o port is asserted. When the host clears this bit, the QSGMII/SGMII_PCS resumes the normal operation. In a Synopsys PHY configuration, after clearing this bit, the host must wait until Bits[4:2] of VR_XS_PCS_DIG_STS/VR_MII_DIG_STS Register indicate that the QSGMII/SGMII_PCS is in the normal state
10	RO	0x0	Reserved_10 Reserved
9	RW	0x0	RESTART_AN Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the QSGMII/SGMII_PCS initiates the auto-negotiation process for port 1. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The QSGMII/SGMII_PCS clears this bit after restarting the auto-negotiation.
8	RW	0x1	DUPLEX_MODE Duplex Mode This bit specifies the duplex mode of the QSGMII/SGMII_PCS along port 1. 0: Half duplex 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process.
7	RO	0x0	Reserved_7 Reserved
6	RW	0x1	SS6 Speed Selection This bit, along with the SS5 and SS13 bits of this register indicates the speed of operation of GMII/XGMII Port 1. For more information, see description of the SS13 bit.
5	RO	0x0	SS5 Speed Selection This bit, along with SS6 and SS13 bits, control the speed of operation of XGMII/GMII Port 1. For more information, see description of the SS13 bit.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_STS

Address: Operational Base + offset (0x1C0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	ABL100T4 100BASE-T4 Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
14	RO	0x0	FD100ABL 100BASE-X Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
13	RO	0x0	HD100ABL 100BASE-X Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
12	RO	0x0	FD10ABL 10 Mbps Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
11	RO	0x0	HD10ABL 10 Mbps Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
10	RO	0x0	FD100T 100BASE-T2 Full-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality
9	RO	0x0	HD100T 100BASE-T2 Half-Duplex Ability The QSGMII/SGMII_PCS always returns 0 because it does not support this functionality.
8	RO	0x1	EXT_STS_ABL Extended Status Information 0: No Extended Status information is present at register address 16'h000F of this MMD device. 1: Extended Status information is present at register address 16'h000F of this MMD device. QSGMII/SGMII_PCS returns this bit as 1.
7	RO	0x0	UN_DIR_ABL Unidirectional Ability 1: The QSGMII/SGMII_PCS is able to transmit GMII irrespective of whether device has determined the valid link or not. 0: The QSGMII/SGMII_PCS is able to transmit GMII only when the device has determined the valid link. The QSGMII/SGMII_PCS always returns this bit as 0.

Bit	Attr	Reset Value	Description
6	RO	0x0	MF_PRE_SUP MF Preamble Suppression 1: The QSGMII/SGMII_PCS accepts the MDIO frames with preamble suppressed. 0: The QSGMII/SGMII_PCS does not accept the MDIO frames with preamble suppressed. This bit is always set to 0
5	RO	0x0	AN_CMPL Auto-negotiation Complete for Port 1 1: The AN process is complete 0: The AN process is not complete This bit returns 0 if AN_ENABLE of SR_MII_1_CTRL Register is set to 0.
4	RO	0x0	RF Remote Fault This register bit is shared with RF bit of SR_MII_STS register. The value returned by this field should be ignored by the software as it is not valid in QSGMII/SGMII/USXGMII Modes
3	RO	0x1	AN_ABL Auto-negotiation Ability The QSGMII/SGMII_PCS always returns this bit as 1. 1: The QSGMII/SGMII_PCS is able to perform auto-negotiation. 0: The QSGMII/SGMII_PCS is not able to perform auto-negotiation
2	RO	0x0	LINK_STS Link Status This register bit is shared with RLU bit of SR_MII_STS register.
1	RO	0x0	Reserved_1 Reserved
0	RO	0x1	EXT_REG_CAP Extended Register Capability 1: Extended Register capability exists. This bit is always set to 1. 0: Extended Register capability does not exist.

QSGMII/SGMII_PCS_SR_MII_DEV_ID1

Address: Operational Base + offset (0x1C0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x7996	VS_MII_DEV_OUI_3_18 Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer. This register reflects the same value as that of SR_MII_DEV_ID1 register.

QSGMII/SGMII_PCS_SR_MII_DEV_ID2

Address: Operational Base + offset (0x1C000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:10	RO	0x33	VS_MMD_DEV_OUI_19_24 Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The QSGMII/SGMII_PCS offers 24 configurable Bits[24:1] for identifying the device manufacturer.
9:4	RO	0x2d	VS_MMD_DEV_MMN_5_0 Model Number This field contains the 5-bit Model Number of the device.
3:0	RO	0x0	VS_MMD_DEV_RN_3_0 Revision Number This field contains the 4-bit Revision Number of the device

QSGMII/SGMII_PCS_SR_MII_AN_ADV

Address: Operational Base + offset (0x1C0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	NP Next Page This bit reflects the value of NP bit of SR_MII_AN_ADV Register.
14	RO	0x0	Reserved_14 Reserved
13:12	RW	0x0	RF Remote Fault This bit reflects the value of RF bit of SR_MII_AN_ADV Register.
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RW	0x0	PAUSE Pause Ability. This bit reflects the value of PAUSE bit of SR_MII_AN_ADV Register
6	RW	0x0	HD Half Duplex This bit reflects the value of HD bit of SR_MII_AN_ADV Register.
5	RW	0x1	FD Full Duplex When this bit is set, it indicates the device (port 1) can operate in full-duplex mode. This bit is used in Clause 37 auto-negotiation (Tx_Config_Reg) done by port 1, when QSGMII/SGMII_PCS is configured as PHY-side QSGMII.
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_LP_BABL

Address: Operational Base + offset (0x1C0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	LP_NP Next Page
14	RO	0x0	LP_ACK ACK bit from the Link Partner
13:12	RO	0x0	LP_RF Remote Fault

Bit	Attr	Reset Value	Description
11:9	RO	0x0	Reserved_11_9 Reserved
8:7	RO	0x0	LP_PAUSE Pause Ability
6	RO	0x0	LP_HD Half Duplex
5	RO	0x0	LP_FD Full Duplex
4:0	RO	0x00	Reserved_4_0 Reserved

QSGMII/SGMII_PCS_SR_MII_AN_EXPN

Address: Operational Base + offset (0x1C0018)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	LD_NP_ABL Local Device NP Able 1: The local device has the next page ability 0: The local device does not have the next page ability The QSGMII/SGMII_PCS always returns this bit as 0 because it does not support Next Page.
1	RO	0x0	PG_RCVD Page Received (RO, LH Type) This bit indicates that the local device received a page from the link partner (during port 1 auto-negotiation). 1: The local device received a new page 0: The local device did not receive a new page
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_SR_MII_EXT_STS

Address: Operational Base + offset (0x1C003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x1	CAP_1G_X_FD 1000BASE-X Full-Duplex Capable
14	RO	0x1	CAP_1G_X_HD 1000BASE-X Half-Duplex Capable
13	RO	0x0	CAP_1G_T_FD 1000BASE-T Full-Duplex Capable
12	RO	0x0	CAP_1G_T_HD 1000BASE-T Half-Duplex Capable
11:0	RO	0x000	Reserved_11_0 Reserved

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_ABL

Address: Operational Base + offset (0x1C1C20)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	RO	0x1	MII_TX_DLY_ABL QSGMII/SGMII_PCS Transmit Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum transmit data delay of QSGMII/SGMII_PCS is available in MII MMD Tx Time Delay Registers
0	RO	0x1	MII_RX_DLY_ABL QSGMII/SGMII_PCS Receive Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum receive data delay of QSGMII/SGMII_PCS is available in MII MMD Rx Time Delay Registers

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MAX_DLY_LWR

Address: Operational Base + offset (0x1C1C24)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x038	MII_TX_MAX_DLY_LWR This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nanoseconds) of QSGMII/SGMII_PCS.

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MAX_DLY_UPR

Address: Operational Base + offset (0x1C1C28)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	MII_TX_MAX_DLY_UPR This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nanoseconds) of QSGMII/SGMII_PCS.

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MIN_DLY_LWR

Address: Operational Base + offset (0x1C1C2C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x038	MII_TX_MIN_DLY_LWR This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nanoseconds) of QSGMII/SGMII_PCS

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_TX_MIN_DLY_UPR

Address: Operational Base + offset (0x1C1C30)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	MII_TX_MIN_DLY_UPR This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nanoseconds) of QSGMII/SGMII_PCS.

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MAX_DLY_LWR

Address: Operational Base + offset (0x1C1C34)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RO	0x0058	MII_RX_MAX_DLY_LWR This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nanoseconds) of QSGMII/SGMII_PCS.

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MAX_DLY_UPR

Address: Operational Base + offset (0x1C1C38)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	MII_RX_MAX_DLY_UPR This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nanoseconds) of QSGMII/SGMII_PCS

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MIN_DLY_LWR

Address: Operational Base + offset (0x1C1C3C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0050	MII_RX_MIN_DLY_LWR This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nanoseconds) of PCS.

QSGMII/SGMII_PCS_SR_MII_TIME_SYNC_RX_MIN_DLY_UPR

Address: Operational Base + offset (0x1C1C40)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	MII_RX_MIN_DLY_UPR This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nanoseconds) of PCS

QSGMII/SGMII_PCS_VR_MII_DIG_CTRL1

Address: Operational Base + offset (0x1E0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	VR_RST Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: For Synopsys PHY: This bit is self cleared when Bits[4:2] in VR_MII_DIG_STS Register are equal to 3'b100, that is, Tx/Rx clocks are stable and in Power_Good state. For Non-Synopsys PHY:This bit is self cleared after the following: 32 clk_csr_i clocks for the MCI interface 1 MDC clock period for the MDIO interface Note: For information about the read or write access for any register during the reset process, see "Special Case Register Access" section.

Bit	Attr	Reset Value	Description
14	RW	0x0	R2TLBE Rx to Tx Loopback Enable This bit controls the loopback path from the GMII/XGMII Rx to the GMII/XGMII Tx at the GMII/XGMII interface (port 1). 0: Loopback path is disabled 1: Loopback path is enabled
13	RW	0x1	EN_VSMMD1 Enable Vendor-Specific MMD1 This is a read-only bit which reflects the value of EN_VSMMD1 bit of VR_MII_DIG_CTRL1 Register.
12	RO	0x0	CL37_BP Enable Clause 37 AN in Backplane Configuration This is a read-only bit which reflects the value of CL37_BP bit of VR_MII_DIG_CTRL1 Register.
11	RO	0x0	PWRSV Reserved
10	RW	0x1	CS_EN Clock Stop Enable 1: The PHY may stop the clock during LPI mode 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC (connected to GMII Port 1) during Rx LPI mode. Note: This field is valid only in QSGMII mode
9	RW	0x0	MAC_AUTO_SW Automatic Speed Mode Change after CL37 AN (for port 1) If this field is set to 1, QSGMII/SGMII_PCS automatically switches to the negotiated USXGMII/QSGMII(port1) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when QSGMII/SGMII_PCS is configured as MAC-side USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, QSGMII/SGMII_PCS operates at the speed/duplex mode as per the values programmed to SR_MII_1_CTRL Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR_MII_1_AN_INTR_STS Register and then program SR_MII_1_CTRL Register appropriately. If this bit is set to 1 in QSGMII mode, PCS_qsgmii_link_sts_p1_o, PCS_link_speed_p1_o and PCS_qsgmii_full_duplex_p1_o outputs reflect the auto-negotiated values, that is, values from CL37_ANSGM_STS field of VR_MII_1_AN_INTR_STS Register. For USXGMII mode, if clk_xgmii_tx_p1_i and clk_xgmii_rx_p1_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USRA_RST' bit prior to starting packet transfer in the new speed mode.
8	RW	0x0	INIT INIT This bit reflects the value of INIT bit of VR_MII_DIG_CTRL1 Register.

Bit	Attr	Reset Value	Description
7	RW	0x0	MSK_RD_ERR Mask Running Disparity Error This bit reflects the value of MSK_RD_ERR bit of VR_MII_DIG_CTRL1 Register.
6	RW	0x0	PRE_EMP Pre-emption Packet Enable. This bit should be set to 1 to allow the QSGMII/SGMII_PCS to properly receive/transmit pre-emption packets along GMII port 1, when operating in 10M/100M Modes.
5	RO	0x0	EN_100M Enable 100Mbps PCS Mode. This bit should be set to 1 to enable 100Mbps PCS Mode of operation.This bit drives the output port 'PCS_100m_o'.
4	RW	0x0	DTXLANED_0 Tx Lane 0 Disable This bit reflects the value of DTXLANED_0 bit of VR_MII_DIG_CTRL1 Register.
3	RW	0x0	CL37_TMR_OVR_RIDE Over-Ride Control for CL37 Link Timer. This bit reflects the value of CL37_TMR_OVR_RIDE bit of VR_MII_DIG_CTRL1 Register.
2	RW	0x0	EN_2_5G_MODE Enable 2.5G GMII Mode (GMII interface over-clocked 2.5 This bit reflects the value of EN_2_5G_MODE bit of VR_MII_DIG_CTRL1 Register.
1	RO	0x0	BYP_PWRUP Reserved
0	RO	0x0	PHY_MODE_CTRL QSGMII/USXGMII PHY mode control on Port 1 This bit controls the Clause 37 auto-negotiation when operating in QSGMII/USXGMII (Port 1) PHY mode. QSGMI: When this bit is set to 1, QSGMII/SGMII_PCS advertises the values of input ports PCS_qsgmii_link_sts_p1_i, PCS_qsgmii_link_speed_p1_i and PCS_qsgmii_full_duplex_p1_i during QSGMII(Port 1) auto-negotiation. When this bit is set to 0, QSGMII(Port 1) auto-negotiation advertises the values programmed to: bit 4 (SGMII_LINK_STS) of VR_MII_1_AN_CTRL Register bit 13 (ss13) and 6 (ss6) of SR_MII_1_CTRL Register and bit 5 (FD) of SR_MII_1_AN_ADV Register

QSGMII/SGMII_PCS_VR_MII_AN_CTRL

Address: Operational Base + offset (0x1E0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:10	RO	0x00	Reserved_15_10 Reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	IND_TX_EN Independent Transmit Enable If this bit is set to 1, QSGMII/SGMII_PCS is able to transmit the port 1 GMII Tx data, irrespective of its receive link status during QSGMII mode (provided auto-negotiation is not enabled). If this bit is set to 0, QSGMII/SGMII_PCS sends IDLE (for port 1) till its receiver has attained synchronization.
8	RW	0x0	MII_CTRL MII Control This bit controls the width of the MAC interface (connected to GMII port 1) when operating at 10 Mbps or 100 Mbps 0: 4-bit MII 1: 8-bit MII This bit also controls the PCS_mii_ctrl_p1_o signal which is used for external clock multiplexing of the clk_mii_tx_p1_i/clk_xgmii_tx_p1_i and clk_mii_rx_p1_i/clk_xgmii_rx_p1_i signals
7:5	RO	0x0	Reserved_7_5 Reserved
4	RW	0x0	SGMII_LINK_STS QSGMII/USXGMII Link Status (port 1) This bit is used in Bit 15 of the Tx_Config_Reg during Clause 37 auto-negotiation (along port 1) when QSGMII/SGMII_PCS is programmed as QSGMII-PHY (or as USXGMII-PHY) and when PHY_MODE_CTRL bit of VR_MII_1_DIG_CTRL1 Register is 0 . 0: Link Down 1: Link Up
3	RW	0x0	TX_CONFIG When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXMII_EN=Enabled:Transmit Configuration This bit controls the Config_Reg value to be used during the Clause 37 auto-negotiation in the SGMII/QSGMII/USXGMII mode. 1: Configures the QSGMII/SGMII_PCS as the PHY side SGMII/QSGMII/USXGMII. 0: Configures the QSGMII/SGMII_PCS as the MAC side SGMII/QSGMII/USXGMII.
2:1	RW	0x0	PCS_MODE When SGMII_EN=Enabled or QSGMII_EN=Enabled:PCS Mode This field controls the auto-negotiation (and operating) mode. 00: 1000BASE-X mode (clause 37 auto-negotiation is as per 1000BaseX). 10: SGMII mode (clause 37 auto-negotiation is as per SGMII). 11: QSGMII mode (clause 37 auto-negotiation conforms to QSGMII) If this field is set as 2'b11, then QSGMII/SGMII_PCS asserts the 'xgxs_qsgmii_mode_o' port.
0	RW	0x0	MII_AN_INTR_EN Clause 37 AN Complete Interrupt Enable (port 1) When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete (on port 1) interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

QSGMII/SGMII_PCS_VR_MII_AN_INTR_STS

Address: Operational Base + offset (0x1E0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	Reserved_15 Reserved
14:8	RO	0x00	USXG_AN_STS USXGMII Clause 37 AN Status (along Port 1) This field is valid only when clause 37 auto-negotiation is complete in USXGMII Mode along Port 1. It indicates the status received from remote link after the USXGMII auto-negotiation is complete. USXG_AN_STS[6] 0: Link is Down 1: Link is Up USXG_AN_STS[5] 0: Half Duplex 1: Full Duplex USXG_AN_STS[4:2] 000: 10 Mbps speed link 001: 100 Mbps speed link 010: 1000 Mbps speed link 011: 10 Gbps speed link 100: 2.5 Gbps speed link 101: 5 Gbps speed link USXG_AN_STS[1] 1: EEE supported 0: EEE not supported USXG_AN_STS[0] 1: EEE clock-stop supported 0: EEE clock-stop not supported Note:This field is present only in configurations with Multi-port USXGMII support.
7	RO	0x0	Reserved_7 Reserved
6	RO	0x0	LP_CK_STP Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or enable in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. Note:This field is present only in configurations with QSGMII
5	RO	0x0	LP_EEE_CAP Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 1 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. Note:This field is present only in configurations with QSGMII.

Bit	Attr	Reset Value	Description
4:1	RO	0x5	CL37_ANSGM_STS Clause 37 AN QSGMII Status (port 1) This field is valid only when the PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 1. It indicates the status received from remote link partner. CL37_ANSGM_STS[0] 0: Half Duplex 1: Full Duplex CL37_ANSGM_STS[2:1] 00: 10 Mbps speed link 01: 100 Mbps speed link 10: 1000 Mbps speed link CL37_ANSGM_STS[3] 0: Link is Down 1: Link is Up Note:This field is present only in configurations with QSGMII.
0	RW	0x0	CL37_ANCMPLT_INTR Clause 37 AN Complete Interrupt (SS,WC Type) The QSGMII/SGMII_PCS sets this bit when Clause 37 auto-negotiation is complete for port 1. The host must clear this bit by writing 0 to it.

QSGMII/SGMII_PCS_VR_MII_TC

Address: Operational Base + offset (0x1E000C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	TPE Test Pattern Enable Lanes This bit indicates that a test pattern can be enabled in the Tx path after the current normal frame transmission is complete. 0: Test pattern disabled 1: Test pattern enabled Dependencies: The specific test pattern that is generated is based on Bits[1:0] of this register
1:0	RW	0x0	TP Test Pattern Select This field indicates the pattern type that is enabled with Bit 2 of this register. The following are the supported test patterns: 2'b00: High Frequency Test Pattern 2'b01: Low Frequency Test Pattern 2'b10: Mixed Frequency Test Pattern 2'b11: Reserved The definition of these test patterns is specified in IEEE Std 802.3ae, Annex 48A.

QSGMII/SGMII_PCS_VR_MII_DBG_CTRL

Address: Operational Base + offset (0x1E0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	TX_PMBL_CTL Transmit Preamble Control This bit can be set to 1 to prevent possible preamble truncation in the QSGMII/SGMII_PCS transmitter when operating in 1000BASE-X (or 2.5G Mode over GMII) Mode. As per IEEE spec, it is permissible for a compliant 1000BASE-X PCS transmit process to truncate the first byte of preamble in order to align the start of the packet on the EVEN boundary. If this bit is set to 1, QSGMII/SGMII_PCS does not delete any preamble bytes (received from GMII Tx interface) and passes on the same number of preamble bytes to its output. QSGMII/SGMII_PCS carries out this operation by adjusting the IPG. This mode is a deviation from Clause 36 of IEEE802.3 specification. But it can prove useful when operating at 2.5G Mode (over clocked 1000BASE-X Mode) and the far-end device is compliant to IEEE802.3bz/cb specification.
7	RO	0x0	RX_SYNC_CTL Receive Synchronization Control . This bit merely reflects the value of RX_SYNC_CTL field of VR_MII_DBG_CTRL Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DEBUG_CTRL Register (for other configurations).
6	RO	0x0	RX_DT_EN_CTL Reserved
5	RW	0x0	SUPRESS_EEE_LOS_DET Suppress EEE Loss of Signal Detection. When this field is set to 1, Loss of Signal indicated by the PHY (based on input port PCS_los_i) is ignored by QSGMII/SGMII_PCS while evaluating the Receive link when operating in EEE mode. Receive link is evaluated based the on data received by QSGMII/SGMII_PCS from PHY. When this field is set to 0, Loss of signal indicated by the PHY is considered by the QSGMII/SGMII_PCS while evaluating the Receive link status in EEE mode.
4	RW	0x0	SUPRESS_LOS_DET Suppress Loss of Signal Detection When this field is set to 1, Loss of Signal indicated by the PHY (based on input port PCS_los_i) is ignored by QSGMII/SGMII_PCS while evaluating the Receive link. Receive link is evaluated based the Rx data received on the 'xgxs_rx_datalane_i' port of QSGMII/SGMII_PCS. When this field is set to 0, Loss of signal indicated by the PHY is considered by the QSGMII/SGMII_PCS while evaluating the Receive link status.
3:1	RO	0x0	reserved
0	RW	0x0	RESTAR_SYNC Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on port 1. The host must clear this bit to 0 before setting it to 1 next time.

QSGMII/SGMII_PCS_VR_MII_EEE_MCTRL0

Address: Operational Base + offset (0x1E0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x8	CLKSTOP Clock Stop This field holds the count value after which the Rx clock to the MAC can be stopped. The default value is 8. The host should program this value depending on the capability of the MAC. This field is used to control the assertion of the PCS_lrx_clk_gat_o signal (to gate the Rx clock of the MAC) By default, the PCS_lrx_clk_gat_o signal is asserted after the PCS Rx module detects the LPI pattern followed by the following: Number of clk_xgxs_rx0_i or clk_rpcs_rx_i clocks (specified in this field) + clk_eee_i synchronization delay + FIFO initialization delay
11:8	RW	0x9	MULT_FACT_100NS 100 ns Clock Tic Multiplying Factor This bit is the multiplying factor to the clk_eee_i clock time period to make it closer to 100 ns. For example, if the clk_eee_i clock time period (clk_eee_i_time_period) is 10 ns, the value of this field is 9, that is, 1 less than 10. This value should be programmed such that the clk_eee_i_time_period * (MULT_FACT_100NS + 1) should be within 80 ns to 120 ns. The default value of this register is 9, assuming that the default clk_eee_i time period to be 10 ns.
7	RO	0x1	RX_EN_CTRL Rx Control Enable This bit controls the generation of the PCS_rx_en_olane signal. When this bit is set to 1, the PCS_rx_en_olane signal is de-asserted when the EEE receive controller reaches the Quiet state. When this bit set to 0, the PCS_rx_en_olane signal is not de-asserted when the EEE transmit controller reaches the Quiet state.
6	RO	0x0	SIGN_BIT Effective 100 ns Tic Value The host should use this bit to fine tune the EEE timing requirement. The host should set this bit to 0 when the clk_eee_i_time_period * (MULT_FACT_100NS + 1) value is more than 100 ns. The host should set this bit to 1 when the clk_eee_i clock period * (MULT_FACT_100NS + 1) value is less than or equal to 100 ns.
5	RO	0x0	Reserved_5 Reserved
4	RW	0x1	TX_EN_CTRL Tx Control Enable This bit controls the generation of the following signals: xgxs_txlane_en_o (for Synopsys PHY) PCS_tx_en_olane (for non-Synopsys PHY) When this bit is set to 1, the xgxs_txlane_en_o or PCS_tx_en_olane signal is de-asserted when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xgxs_txlane_en_o or PCS_tx_en_olane signal is not de-asserted when the EEE transmit controller reaches the Quiet state.

Bit	Attr	Reset Value	Description
3	RW	0x1	RX_QUIET_EN Rx Quiet Enable This bit controls the generation of the PCS_lpitx_quiet_o output. When this bit is set to 1, the PCS_lpitx_quiet_o output is set to 1 when the EEE receive controller reaches the Quiet state. When this bit set to 0, the PCS_lpitx_quiet_o output is not set to 1.
2	RW	0x1	TX_QUIET_EN Tx Quiet Enable This bit controls the generation of the PCS_lpitx_quiet_o output. When this bit is set to 1, the PCS_lpitx_quiet_o output is set to 1 when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the PCS_lpitx_quiet_o output is not set to 1.
1	RW	0x0	LRX_EN LPI Rx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the QSGMII/SGMII_PCS receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the QSGMII/SGMII_PCS receive path.
0	RW	0x0	LTX_EN LPI Rx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the QSGMII/SGMII_PCS receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the QSGMII/SGMII_PCS receive path.

QSGMII/SGMII_PCS_VR_MII_EEE_TXTIMER

Address: Operational Base + offset (0x1E0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	TSL_RES TSL Resolution This field stores the resolution value for the TSL timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TSL timer. The QSGMII/SGMII_PCS maintains the default value of the TSL timer as 199, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns to produce 19900 ns (19.9 us) as per the TSL requirement in the IEEE standard. If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 90, the default TSL timer produces 17910 ns (17.91 us) which is lesser than the standard 19.9 us. To make it 19.9 us, you should program this register such that (199 +/- TSL_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) is greater than 19.9 us and less than 20.1 us (max limit), that is, (199 + TSL_RES)*90 = 19.9 us. TWL_RES = 23 meets the requirement which produces 19.98 us. The SIGN_BIT should be programmed as 1.

QSGMII/SGMII_PCS_VR_MII_EEE_RXTIMER

Address: Operational Base + offset (0x1E0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	TWR_RES TWR Resolution This field stores the resolution value for the TWR timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TWR timer. The default value is 11 us for 1000BASEX-Only PCS mode. This value is as per the requirements specified in the standard assuming that clk_eee_i_time_period * (MULT_FACT_100NS + 1) produces 100 ns tick. Example: For KX mode, the time requirement is 11 us. The QSGMII/SGMII_PCS maintains the default value of the TWR timer as 110, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns to produce 11000 ns (11 us). If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 110, the default TWR timer produces 12100 ns (12.1 us) which is more than 11 us. To make it 11 us, you must program this register such that (110 +/- TWR_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 11 us. Therefore, use the following equation: (110 - TWR_RES) * 110 = 11000 ns TWL_RES = 10 meets the requirement which produces 11 us. The SIGN_BIT should be programmed as 0.
7:0	RW	0x00	RES_100U 100 us Resolution This field stores the resolution value for the 100 us timer. If the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the 100 us timer. This field is used to control the generation of 100 us time tick using the clk_eee_i clock and MULT_FACT_100NS field. By default, the 100 us timer is generated assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns. Therefore, the QSGMII/SGMII_PCS maintains the default value of the 100 us timer as 1000 to achieve 100000 ns (100 us). You should use this field if clk_eee_i_time_period * (MULT_FACT_100NS + 1) is not equal to 100 ns. To program this field, use the following equation: (1000 +/- RES_100US)* ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 100 us The SIGN_BIT should be programmed as 1 for (+) and 0 for (-).

QSGMII/SGMII_PCS_VR_MII_LINK_TIMER_CTRL

Address: Operational Base + offset (0x1E0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	VR_MII_1_LINK_TIMER_CTRL Programmable Link Timer Value for Clause 37 auto-negotiation. This field can be programmed to any desired value if application wishes to override the standard specified values for Link Timer used during Clause 37 Auto negotiation. Link timer is implemented in QSGMII/SGMII_PCS using a 24-bit timer.When operating in USXGMII mode, link timer runs at 156.25 MHz. When operating in 1000BaseX/SGMII mode, this timer operates at 125 MHz. For USXGMII configurations:This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer.The lower 8-bits are hard-coded as zero. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h100, which corresponds to a duration of 1638 ns (256*6.4ns) in USXGMII mode or 2048 ns (256*8ns) in 1000BaseX/SGMII mode. For configurations without USXGMII:This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer.The lower 8-bits are hardcoded as 8'h7D. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h17D, which corresponds to a duration of 3048 ns (381*8ns). After programming this register, application should perform either of the following steps, so that the new values takes effect: Set CL37_TMR_OVR_RIDE bit (bit[3]) of VR_MII_DIG_CTRL1 Register to 1 FAST_SIM bit of SR Control MMD Control Register should be cleared (if already set) and then set back to 1.

QSGMII/SGMII_PCS_VR_MII_EEE_MCTRL1

Address: Operational Base + offset (0x1E002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRN_LPI Transparent Tx LPI Mode Enable. When set to 1 (along with LTX_EN=1), transparent LPI mode gets activated in the QSGMII/SGMII_PCS Transmit path. In this mode, the transmit LPI state-machine does not move to TX_QUIET state. On detecting Lower-Power Idle on GMII Tx interface, QSGMII/SGMII_PCS goes to the TX_SLEEP state and remains in this state till MAC stops sending LPI. In this mode,QSGMII/SGMII_PCS merely sends the encoded LPI pattern to the serdes. This mode does not involve gating-off of any clocks to QSGMII/SGMII_PCS. In addition, the serdes transmitter is not disabled (PCS_tx_data_en_o signal remains high). MAC should ensure that it does not gate-off XGMII/GMII Tx clock to QSGMII/SGMII_PCS during this mode of operation.

QSGMII/SGMII_PCS_VR_MII_DIG_STS

Address: Operational Base + offset (0x1E0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RO	0x0	LTX_STATE LPI Transmit State. This field reflects the value of LTX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).
12:10	RO	0x0	LRX_STATE LPI Receive State This field reflects the value of LRX_STATE field of VR_MII_DIG_STS Register (for 1000BaseX-Only PCS configurations) or VR_XS_PCS_DIG_STS Register (for other configurations).
9	RO	0x0	INV_XGM_CHAR Invalid XGMII Character (RO,LH Type) -Port 1 This bit indicates an invalid XGMII character on the Transmit path (port 1). 0: No Invalid XGMII character 1: Invalid character This bit is set when one of the following conditions is true on the XGMII interface: |Q| is detected on a lane other than Lane 0. |Q| is detected on Lane 0 and also any of the following conditions is true: No 8'h00 data in Lane 1. No 8'h00 data in Lane 2. No 8'h01 or 8'h02 data on Lane 3. |E| or |T| is encountered in non-data phase and |Q| is encountered in data phase. |D| is detected during the Idle phase (after Terminate and before valid SOF). |I| is detected during the data phase (after SOF and before Terminate). Note: This field is present only for Multi-port USXGMII configurations.
8	RO	0x0	INV_XGM_T Invalid XGMII T Character (RO,LH Type) -Port 1 This bit indicates that the transmit data (port 1) received on XGMII has an invalid Terminate character. 0: Normal operation 1: Invalid Terminate character The following can cause an invalid Terminate character: In Terminate column, before lane corresponds to the |T| character, there is a |I| or |Q| character. In Terminate column, after lane corresponds to the |T| character, there is a non-|I| character Note:This field is present only for Multi-port USXGMII configurations.

Bit	Attr	Reset Value	Description
7	RW	0x0	INV_XGM_SOP Invalid XGMII Start Character (RO,LH Type) -Port 1 This bit indicates that the XGMII transmit (Port 1) frame contains invalid SOP character. 0: Normal operation 1: Invalid SOP character An invalid SOP event occurs when a |S| character is detected in a lane other than Lane 0. Note:This field is present only for Multi-port USXGMII configurations.
6	RO	0x0	RXFIFO_OVF Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow for port 1. 0: Normal operation 1: FIFO overflow
5	RO	0x0	RXFIFO_UNDF Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow for port 1. 0: Normal operation 1: FIFO underflow
4:2	RO	0x4	PSEQ_STATE Reserved
1	RO	0x0	LB_ACTIVE Reserved
0	RO	0x0	Reserved_0 Reserved

QSGMII/SGMII_PCS_VR_MII_ICG_ERRCNT1

Address: Operational Base + offset (0x1E0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	EC0 Invalid Code Group Count -Port 1 (RO,LH Type) This field gives the invalid code group count in port 1 (of QSGMII) when Bit 4 of VR MII_1 MMD Digital Error Count Select Register is set to 1.

QSGMII/SGMII_PCS_VR_MII_MISC_STS

Address: Operational Base + offset (0x1E0060)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	BIT_SFT Bit Shift This field indicates the number of bit-shifts carried-out by comma-detect logic so as to align the incoming 10-bit XGXS Rx data

QSGMII/SGMII_PCS_VR_MII_RX_LSTS

Address: Operational Base + offset (0x1E0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:13	RO	0x0	RX_VALID_3_1 DPLL Lock Status for Lanes[3:1] This field indicates that the DPLL in the PHY is locked on the serial data in the corresponding lane. 3'b**1: Lane 1 DPLL bit locked 3'b*1*: Lane 2 DPLL bit locked 3'b1**: Lane 3 DPLL bit locked Dependency: This field is present only the following configurations: Synopsys PHY configurations Backplane Ethernet PCS configurations with non-Synopsys PHY
12	RO	0x0	RX_VALID_0 DPLL Lock Status for Lane 0 This field indicates that the DPLL in the PHY is locked on the serial data in Lane 0. The value 1'b1 indicates that Lane 0 DPLL bit is locked. Dependency: This field is present only the following configurations: Synopsys PHY configurations Backplane Ethernet PCS configurations with non-Synopsys PHY
11:9	RO	0x0	RX_PLL_STATE_3_1 Reserved
8	RO	0x0	RX_PLL_STATE_0 Reserved
7:5	RO	0x0	SIG_DET_3_1 Reserved
4	RO	0x0	SIG_DET_0 Rx Signal Detect for Lane 0 This bit indicates that the Rx detected the signal on Lane 0. This bit is the complement value of the signals input from PHY (PCS_los_i[0]) on Lane 0. The value 1'b1 indicates that Lane 0 signal is detected.
3:0	RO	0x0	Reserved_3_0 Reserved

QSGMII/SGMII_PCS_VR_MII_DIG_CTRL2

Address: Operational Base + offset (0x1E0384)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	TX_POL_INV_0 Tx Polarity Invert on Lane 0 When set to 1, this bit reverses the data polarity on the Tx differential lines of Lane 0.
3:1	RO	0x0	Reserved_3_1 Reserved
0	RW	0x0	RX_POL_INV_0 Rx Polarity Invert on Lane 0 When set, the bits within this field indicate that the data received on Rx serial line is inverted on Lane 0. This reverses the polarity on the data received from the PHY core. The value 1 indicates that Rx data on Lane 0 is inverted

QSGMII/SGMII_PCS_VR_MII_DIG_ERRCNT_SEL

Address: Operational Base + offset (0x1E0388)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	INV_EC_EN Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors (on port 1) is enabled. 0: The counting of errors is disabled 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR_MII_1_ICG_ERRCNT1 Register.
3:1	RO	0x0	Reserved_3_1 Reserved
0	RW	0x0	COR Clear on Read When this bit is set and the host reads port 1 error counter (VR_MII_1_ICG_ERRCNT1 Register), that counter is cleared after the read cycle. 0: Normal operation 1: Clear error counter that is read

21.4 Application Notes

21.4.1 Initializing the QSGMII/SGMII_PCS Controller

Complete the following steps to initialize the QSGMII/SGMII_PCS controller:
1. Switch on the power supply. Reset is asserted (pwr_on_rst_n=0).
2. Wait for the required amount of time depending on the PHY requirements.
3. De-assert reset (pwr_on_rst_n=1)
4. Wait till the 15th bit of SR_MII_CTRL Register is read as 0
5. (Optional). If you have "Enable Clause 37 Auto-Negotiation" parameter enabled, then follow the programming flow outlined in "Programming Guidelines for Clause 37 Auto-Negotiation"
6. If clauses 37, 72, or 73 are not enabled, wait for LINK_STS of SR_MII_STS Register to be set to 1 The QSGMII/SGMII_PCS core is now ready to transmit or receive data.

21.4.2 Switching to 1G and 10 or 100 Mbps SGMII Speed

In 1G mode, the QSGMII/SGMII_PCS-PHY interface works at 10-bit parallel data with the clock rate of 125 MHz. Only Lane 0 is functional. The serial lane works at the baud rate of 1.25 Gbps. The effective data transfer rate, considering the overhead of 8B/10B encoding or decoding, is 1 Gbps.
To switch between the 1G and 10G modes, program Bit 13 (SS13) of SR_PMA_CTRL1and SR_XS_PCS_CTRL1 Registers. When this bit is cleared to 1, QSGMII/SGMII_PCS operates in the 1000BASE-X (1G) mode. The output signal PCS_kx_kx4n_o is asserted when the QSGMII/SGMII_PCS works in this mode.
To switch from SGMII and 1000BASE-X mode and vice-versa, program PCS_MODE field of VR_MII_AN_CTRL register to 2'b10 or 2'b00 respectively.

Programming Sequence for Non-Synopsys PHY
To switch to 1G or KX mode when using non-Synopsys PHY, complete the following steps:
1. Write 4'b0001 to Bits[3:0] of SR_XS_PCS_CTRL2
2. Clear Bit 0 of VR_XS_PCS_XAUI_CTRL to 0. This bit controls the PCS_rxaui_mode_o output.
3. Set Bit 13 of SR_PMA_CTRL1 (only for Backplane Ethernet PCS configurations) or SR_XS_PCS_CTRL1 to 0. This bit controls the PCS_kx_kx4n_o output. This bit is inverted to drive the PCS_kx_kx4n_o output.
4. (Optional) If the SGMII mode is enabled, you can program Bit 13 and Bit 6 of the SR_MII_CTRL to set the SGMII speed as shown in following table.

Speed mode	SS6	SS13
1000 Mbps SGMII	1	0
100 Mbps SGMII	0	1
10 Mbps SGMII	0	0

5. Set Bit 11 of SR_XS_PCS_CTRL1 to 1 to power down QSGMII/SGMII_PCS.
6. Wait till Bits[4:2] of VR_XS_PCS_DIG_STS are set to any value other than 3'b100.
7. Clear Bit 11 of the SR_XS_PCS_CTRL1 to 0 to power up QSGMII/SGMII_PCS.

21.4.3 Programming Guidelines for QSGMII Mode

To switch to QSGMII mode, perform the following steps:
1. Clear Bit [13] of SR_XS_PCS_CTRL1 Register to 0.
2. Program bits [2:1] of VR_MII_AN_CTRL Register to 2'b11. This asserts 'xgxs_qsgmii_mode_o' port of QSGMII/SGMII_PCS.
3. Set Bit [11] of SR_MII_CTRL Register to 1 to power down QSGMII/SGMII_PCS.
4. Wait till Bits[4:2] of VR_MII_DIG_STS Register are set to any value other than 3'b100.
5. Clear Bit [11] of SR_MII_CTRL Register to 0 to power up QSGMII/SGMII_PCS.

21.4.4 Programming Guidelines for Clause 37 Auto-Negotiation

The Clause 37 auto-negotiation is enabled only when Bit 12 of the SR_MII_CTRL Register is set. The default value of this bit is 1. When this bit is enabled, the Clause 37 auto-negotiation is initiated on the following events:

- Power on Reset
- Soft Reset

The QSGMII/SGMII_PCS initiates the auto-negotiation on the following events:

- When the link partner requests auto-negotiation by transmitting configuration code groups.
- When the receive data path loses code group synchronization for more than 10 ms (in 1000BASE-X mode) or 1.6 ms (in SGMII mode).
- When an error condition is detected while receiving the /C/ or /I/ order sets.
- When the host or software requests auto-negotiation by setting Bit 9 in the SR_MII_CTRL Register.

The following list explains the auto-negotiation process:
1. The QSGMII/SGMII_PCS starts auto-negotiation by first transmitting the configuration words with all zeroes for 10 ms (1.6 ms for the SGMII interface).
2. The SR_MII_AN_ADV Register content is transmitted in the configuration words in the 1000BASE-X mode. In the SGMII mode, the values given in the following Table are transmitted in the configuration word. The auto-negotiation is complete when both link partners have exchanged their base pages.

Config_Reg Bit	1000BASE-X Mode	SGMII ModeValue When TX _CONFIG = 0 Value	SGMII ModeValue When TX _CONFIG = 1 Value
15	Next page support (NP)	0	Link UP or Link Down. If bit[0] of VR_MII_DIG_CTRL1 is 0, this bit is derived from Bit 4 (SGMII_LINK_STS) of the VR_MII_AN_CTRL. If bit[0] of VR_MII_DIG_CTRL1 is 1, this bit is derived from the input port 'PCS_sgmii_link_sts_i'
14	ACK	1	1
13	RF[1]	0	0

Config_Reg Bit	1000BASE-X Mode	SGMII ModeValue When TX _CONFIG = 0 Value	SGMII ModeValue When TX _CONFIG = 1 Value
12	RF[0]	0	FULL_DUPLEX If bit[0] of VR_MII_DIG_CTRL1 is 0, this bit is derived from Bit 5 (FD) of the SR_MII_AN_ADV. If bit[0] of VR_MII_DIG_CTRL1 is 1, this bit is derived from the input port 'PCS_sgmii_full_duplex_i'
11:10	Reserved	0	If bit[0] of VR_MII_DIG_CTRL1 is 0,the value of these bits is derived from Bit 13 (SS13) and Bit 6 (SS6) of the SR_MII_CTRL. If bit[0] of VR_MII_DIG_CTRL1 is 1, this bit is derived from the input port 'PCS_sgmii_link_speed_i[1:0]' ■ 10: 1000 Mbps ■ 01: 100 Mbps ■ 00: 10 Mbps
9	0 (Reserved)	0	0
8	PAUSE[1]	0	0
7	PAUSE[0]	0	0
6	HALF_DUPLEX	0	0
5	FULL_DUPLEX	0	0
4	0 (Reserved)	0	0
3	0 (Reserved)	0	0
2	0 (Reserved)	0	0
1	0 (Reserved)	0	0
0	0 (Reserved)	1	1

3. QSGMII/SGMII_PCS generates an interrupt on completion (sbd_intr_o) of auto-negotiation when Bit 0 of VR_MII_AN_CTRL Register is set to 1.
4. The auto-negotiation completion is indicated in the VR_MII_AN_INTR_STS Register.
5. In the MAC attached to the QSGMII/SGMII_PCS, the Transmit and Receive Flow Control mode is determined based on the capabilities of the partner (given in SR_MII_LP_BABL) and the half-duplex or full-duplex operating mode.
In SGMII auto-negotiation, the received link status such as speed, duplex mode is also given in the VR_MII_AN_INTR_STS Register.
When Clause 37 auto-negotiation is complete, QSGMII/SGMII_PCS automatically resolves the duplex mode by selecting the duplex mode of its link partner. If auto-negotiation is disabled, the QSGMII/SGMII_PCS selects the duplex mode defined in Bit 8 of SR_MII_CTRL Register.

21.4.4.1 SGMII Auto-Negotiation

Clause 37 auto-negotiation can be performed in the SGMII mode by programming various registers as follows:
1. In configurations with both 10G and 1G mode speed mode, switch QSGMII/SGMII_PCS to 1G speed mode by following the steps described in "Switching to 1G or KX Mode and 10 or 100 Mbps SGMII Speed"
2. Disable Clause 37 auto-negotiation by programming bit [12] (AN_ENABLE) of SR_MII_CTRL Register to 0 (in case it is already enabled).
4. Program various fields of VR_MII_AN_CTRL Register appropriately as follows:

- Program PCS_MODE to 2'b10
- Program TX_CONFIG to 1 (PHY side SGMII) or 0 (MAC side SGMII) based on your

requirement

- Program MII_AN_INTR_EN to 1, to enable auto-negotiation complete interrupt
- If TX_CONFIG is set to 1 and bit[0] of VR_MII_DIG_CTRL1 Register is set to 0, program SGMII_LINK_STS to indicate the link status to the MAC side SGMII.
- Program MII_CTRL to 0 or 1, as per your requirement.

5. If QSGMII/SGMII_PCS is configured as PHY-side SGMII in the previous step, you can program bit [0] of VR_MII_DIG_CTRL1 Register to 1, if you wish to use the values of the PCS_sgmii_link_sts_i input ports. PCS_sgmii_full_duplex_i and PCS_sgmii_link_speed_i as the transmitted configuration word.
6. If QSGMII/SGMII_PCS is configured as PHY-side SGMII and if bit[0] of VR_MII_DIG_CTRL1 Register is set to 0,

- Program SS13 and SS6 bits of SR_MII_CTRL Register to the required SGMII Speed
- Program bit [5] (FD) of SR_MII_AN_ADV to the desired mode. This step is mandatory even if you wish to leave the FD register bit to its default value.

7. If QSGMII/SGMII_PCS is configured as MAC-side SGMII in step 4, program bit[9] of VR_MII_DIG_CTRL1 Register to 1, for QSGMII/SGMII_PCS to automatically switch to the negotiated link-speed, after the completion of auto-negotiation.
8. Enable CL37 Auto-negotiation by programming bit[12] of the SR_MII_CTRL Register to 1.

21.4.4.2 QSGMII Auto-Negotiation

Clause 37 auto-negotiation can be independently performed for each of the 4 ports, when operating in QSGMII mode. QSGMII/SGMII_PCS has 4 separate MMDs (MII, MII_1, MII_2 and MII_3) to control (and to reflect the status) the auto-negotiation operation.

- MII MMD -> Port 0
- MII_1 MMD -> Port 1
- MII_2 MMD -> Port 2
- MII_3 MMD -> Port 3

After switching to QSGMII mode (as described in "Programming Guidelines for QSGMII Mode" follow these steps to enable auto-negotiation on a particular port (say port 2).
1. In Backplane Ethernet PCS configurations, program bit [12] (AN_EN) of SR AN MMD Control Register to 0 and bit [12] (CL37_BP) of VR XS or PCS MMD Digital Control1 Register to 1.
2. Disable Clause 37 auto-negotiation by programming bit [12] (AN_ENABLE) of SR MII_2 MMD Control Register to 0 (required only in case it is already enabled).
3. Program various fields of VR MII_2 MMD AN Control Register appropriately as follows:

- Program TX_CONFIG to 1 (PHY side QSGMII) or 0 (MAC side QSGMII) based on your requirement
- Program MII_AN_INTR_EN to 1, to enable auto-negotiation complete interrupt (optional step)
- Program QSGMII_LINK_STS suitably to indicate the link status to the MAC side QSGMII, if TX_CONFIG is set to 1 (QSGMII-PHY) and bit [0] of VR MII_2 MMD Digital Control 1 Register is set to 0.
- Program MII_CTRL to 0 or 1, as per your requirement.

4. If QSGMII/SGMII_PCS is configured as PHY-side QSGMII in the previous step, you can program bit [0] of VR MII_2 MMD Digital Control 1 Register to 1, if you wish to use the values of the PCS_qsgmii_link_sts_p2_i,PCS_qsgmii_full_duplex_p2_i andPCS_qsgmii_link_speed_p2_i input ports as the transmitted configuration word.
5. If QSGMII/SGMII_PCS is configured as PHY-side QSGMII and if bit [0] of VR MII_2 MMD Digital Control 1 Register is set to 0,

- Program SS13 and SS6 bits of SR MII_2 MMD Control Register to the required Speed Mode.
- Program bit [5] (FD) of SR MII_2 MMD AN Advertisement Register to the desired mode

These values get advertised in the configuration word transmitted to the link partner.
6. If QSGMII/SGMII_PCS is configured as MAC-side QSGMII in step 3, program bit [9] of VR MII_2 MMD Digital Control 1 Register to 1, so that QSGMII/SGMII_PCS automatically switches to the negotiated link-speed, after the completion of auto-negotiation. (optional step)
7. Enable CL37 Auto-negotiation, by programming bit [12] of the SR MII_2 MMD Control Register to 1. Completion of auto-negotiation is indicated by bit [0] of VR MII_2 MMD AN Interrupt Status Register. If step 6 has not been performed, program SS13 and SS6 bits of SR MII_2 MMD Control Register suitably, based on the outcome of auto-negotiation (CL37_ANSGM_STS field of VR MII_2 MMD AN Interrupt Status Register).

21.4.5 Programming Guidelines for Energy Efficient Ethernet

To enable the Energy Efficient Ethernet (EEE) feature, the host should complete the following:
1. Check if QSGMII/SGMII_PCS supports the EEE feature by reading the SR_XS_PCS_EEE_ABL register. If Bit 4 of this register is set, it indicates that QSGMII/SGMII_PCS supports EEE in1000BASE-X mode.
2. Program various timers used in the EEE mode depending on the clk_eee_i clock frequency:
For 1000BASEX-Only PCS configurations, program the following registers:

- VR_MII_EEE_MCTRL0
- VR_MII_EEE_TXTIMER
- VR_MII_EEE_RXTIMER

3. Enable the EEE feature on the Tx path by setting Bit 0 of VR_XS_PCS_EEE_MCTRL0 Register. Similarly, enable the EEE feature on the Rx path by setting Bit 1 of VR_XS_PCS_EEE_MCTRL0 Register. When these bits are set, QSGMII/SGMII_PCS enables the encoding or decoding of the LPI code groups and also enables the EEE Tx and Rx controllers.

Chapter 22 MULTI-PHY

22.1 Overview

MULTI-PHY IP support physical layer of multiple application including USB3.0 Super Speed (5GT/s), PCIE Gen1/Gen2(2.5GT/s and 5GT/s), SATA Gen1/Gen2/Gen3 (1.5GT/3GT/6GT) and QSGMII(1.25GT/5GT).

The key features of the MULTI-PHY core include:

- Compatible with PCIE/USB3/SATA/QSGMII base Specification
- Fully compatible with PIPE3.1 interface specification
- Data rate configurable to 1.25G/1.5G/2.5G/3G/5G/6G for different application
- Support 16-bit or 32-bit parallel interface when encode/decode enabled
- Support 20-bit parallel interface when encode/decode bypassed
- Support flexible reference clock frequency
- Support 100MHz differential reference clock input or output (optional with SSC) in PCIE Mode
- Support Spread-Spectrum clock (SSC) generation and receiving from -5000ppm to 0ppm
- Support programmable transmit amplitude and De-emphasis
- Support TX detect RX function in PCIE and USB3.0 Mode
- Support Beacon signal generation and detection in PCIE Mode
- Support Low Frequency Periodic Signaling (LFPS) generation and detection in USB3.0 Mode
- Support COMWAKE, COMINIT and COMRESET (OOB) generation and detection in SATA Mode
- Support L1 sub-state power management
- Support RX low latency mode in SATA operation mode
- Support Loopback BERT and Multiple Pattern BIST Mode

22.2 Function Description

22.2.1 Block Diagram and Description

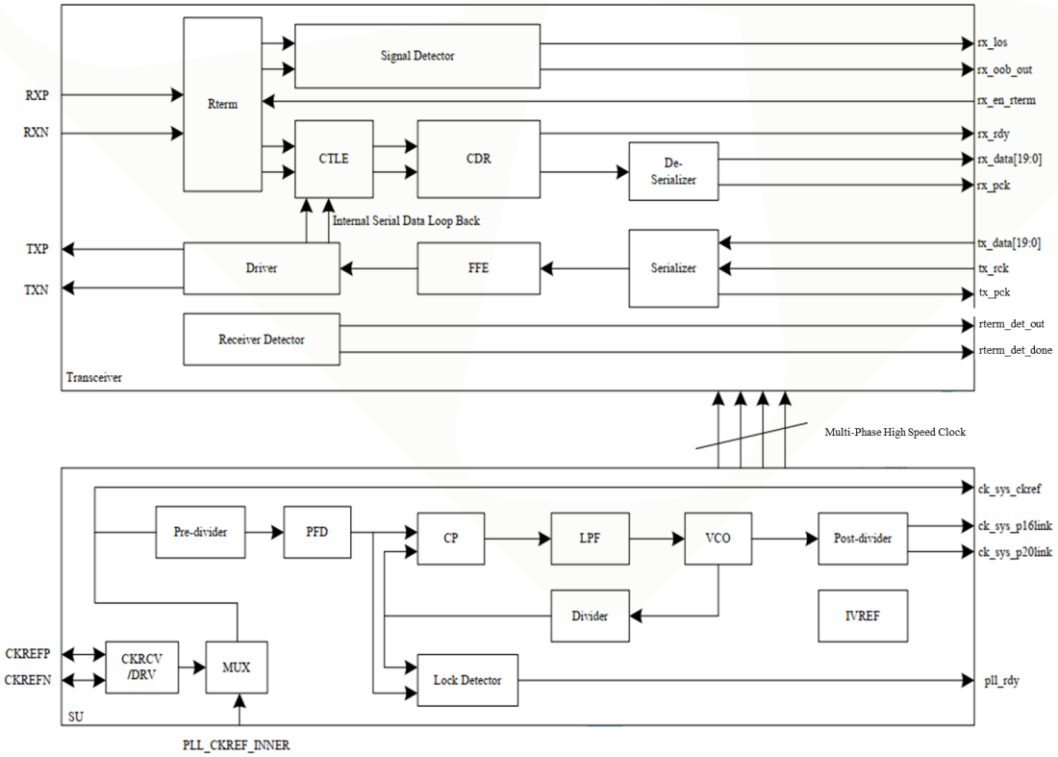


Fig. 22-1 PMA Block Diagram of Multi-PHY

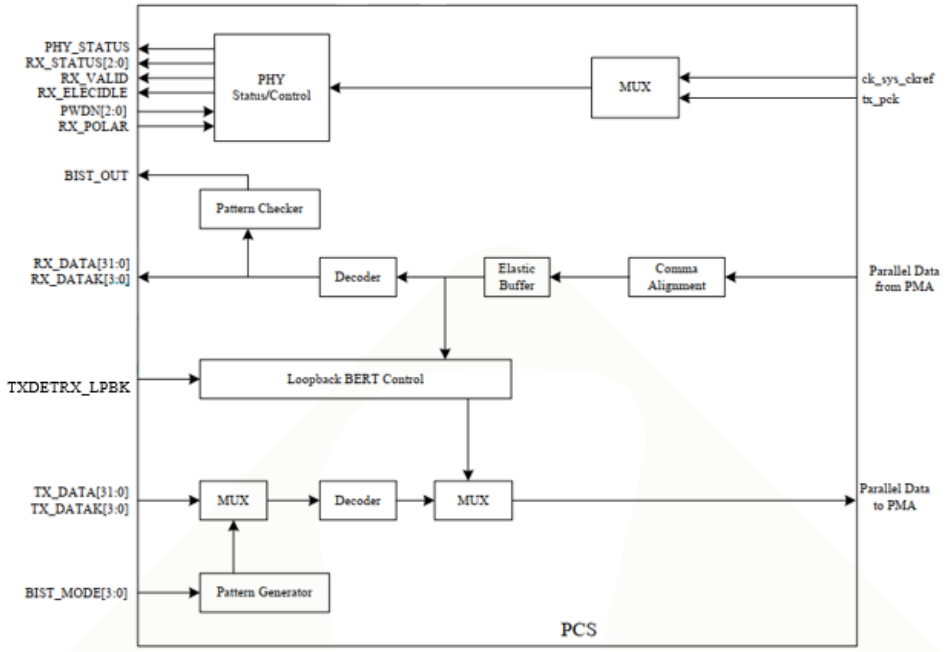


Fig. 22-2 PCS Block Diagram of Multi-PHY

Multi-PHY includes two major blocks, PMA and PCS. PMA is an analog macro to perform serialto parallel and parallel to serial conversion. PMA includes three blocks, Transmitter, Receiver and SU(includes PLL, IVREF, etc.). PCS is a digital synthesis macro to perform PHY coding sub-layer function like 8bit/10bit code and decode, elastic buffer, comma alignment and BERT loopback, it also includes a register interface to access internal control registers with APB interface.

22.2.2 SHARED UNIT (SU)

PLL takes reference clock input from CKREFP/N and PLL_CKREF_INNER, to generate a high speed clock for data transmission and clock data recovery. The high speed clock generated by PLL could be SSC (spectrum spread clock) modulated if SSC mode is turned on. When SSC is enabled, the PHY is transmitting spread-spectrum serial data with frequency offset in 31.5KHz periodically.

IVREF includes a voltage and current reference generator, which comprises a Bandgap Reference and a Voltage Regulator. Reference voltage and current are generated for internal circuit usage. IVREF block is always on as long as IP power up, it will consume ~170uA static current all the time.

CKDRV is an input/output differential clock buffer, when it is used as input, it can receive a wide range differential reference clock. When used as output, CKDRV can drive a 100MHz differential clock for PCIE host application.

22.2.3 TRANSMITTER (TX)

The Serializer block converts parallel data from PHY PCS to high speed serial data by using high speed clock generated by PLL. A feed forward equalizer (FFE) is implemented to compensate channel ISI.

Driver will convert the serial data to differential signal on TXP/TXM, also the driver will transmit Beacon Signal (PCIE2.0), OOB(SATA) or LFPS(USB3.0) signaling. The differential output amplitude and Deemphasis level can be programmed via setting PIPE3 control pins TX_SWING, TX_DEEMPH[2:0] and TX_MARGIN[2:0].

The receiver detector will be used to detect the far-end receiver present or not.

22.2.4 RECEIVER (RX)

The CTLE (Continuous Time Linear Equalizer) is used to compensate channel loss and cancel ISI of the input signals by boosting high frequency gain. The CTLE can be set to adaptive

mode or manual setting mode.
The CDR (Clock and Data Recover) tracks input data stream and generate recovered clock for data deserializer. De-Serializer converts incoming serial bit stream recovered by CDR into a synchronized parallel data bus and forward it to PHY PCS block.
The Signal Detector detects OOB/LFPS on the RX input pair.

22.2.5 PCS

PCS module is a pure digital synthesis module, it works as an interface between PMA and MAC, it accomplishes functions including comma alignment, 8bit/10bit code/decode, elastic buffer, power control and IP testing. This module also includes a APB interface for accessing PHY control registers. PCS is fully compatible with the PIPE3 interface of "PHY interface for PCI express and USB3.0 architecture by intel".

22.3 Register Description

22.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

22.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
Multi-PHY_Register001	0x0000	W	0x00000000	Register001
Multi-PHY_Register002	0x0004	W	0x00000080	Register002
Multi-PHY_Register003	0x0008	W	0x000000FF	Register003
Multi-PHY_Register004	0x000C	W	0x00000000	Register004
Multi-PHY_Register005	0x0010	W	0x00000000	Register005
Multi-PHY_Register006	0x0014	W	0x00000000	Register006
Multi-PHY_Register007	0x0018	W	0x00000088	Register007
Multi-PHY_Register008	0x001C	W	0x00000008	Register008
Multi-PHY_Register009	0x0020	W	0x000000E0	Register009
Multi-PHY_Register011	0x0028	W	0x0000005D	Register011
Multi-PHY_Register012	0x002C	W	0x00000002	Register012
Multi-PHY_Register013	0x0030	W	0x00000004	Register013
Multi-PHY_Register014	0x0034	W	0x0000003B	Register014
Multi-PHY_Register015	0x0038	W	0x00000040	Register015
Multi-PHY_Register016	0x003C	W	0x00000063	Register016
Multi-PHY_Register017	0x0040	W	0x00000000	Register017
Multi-PHY_Register018	0x0044	W	0x00000032	Register018
Multi-PHY_Register019	0x0048	W	0x00000003	Register019
Multi-PHY_Register020	0x004C	W	0x00000007	Register020
Multi-PHY_Register021	0x0050	W	0x00000011	Register021
Multi-PHY_Register022	0x0054	W	0x00000041	Register022
Multi-PHY_Register023	0x0058	W	0x0000002C	Register023
Multi-PHY_Register024	0x005C	W	0x00000030	Register024
Multi-PHY_Register025	0x0060	W	0x00000000	Register025
Multi-PHY_Register026	0x0064	W	0x00000000	Register026
Multi-PHY_Register027	0x0068	W	0x00000010	Register027
Multi-PHY_Register028	0x006C	W	0x00000000	Register028
Multi-PHY_Register029	0x0070	W	0x00000005	Register029
Multi-PHY_Register030	0x0074	W	0x00000000	Register030
Multi-PHY_Register031	0x0078	W	0x00000000	Register031
Multi-PHY_Register032	0x007C	W	0x00000000	Register032
Multi-PHY_Register033	0x0080	W	0x00000000	Register033

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

22.3.3 Detail Registers Description

Multi-PHY_Register001

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	CLK_OUT_SEL Select which internal clock connect to output test_clk 1'b0: TXPLL clock/4 1'b1: RXCDR clock/4
6	RW	0x0	INV_TXPLL_CLK If 1, invert the PLL clock from PHY to PCS in PCS
5	RW	0x0	INV_RXCDR_CLK If 1, invert the CDR clock from PHY to PCS in PCS
4:0	RO	0x00	reserved

Multi-PHY_Register002

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x2	PWDN_CTRL[1:0] [0]: If 1, PHY block power controlled by pwon** signals instead of PIPE signals [1]: Enable IVREF in PMA when pwdn_ctrl[0]=1
5:1	RO	0x00	reserved
0	RW	0x0	CUSTOM_SPECIFIC Bypass elastic_buffer in sata mode

Multi-PHY_Register003

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	PWDN_CTRL[9:2] [2]: Enable PWON_TX_BUF to power on TX driver in PMA pwdn_ctrl[0]=1 [3]: Enable PWON_TXPLL to power on PLL in PMA pwdn_ctrl[0]=1 [4]: Enable PWON_IDLE_DET to power on PCIE EIDLE detect driver in PMA pwdn_ctrl[0]=1 [5]: Enable PWON_LFPS_DET to power on USB LFPS detect in PMA pwdn_ctrl[0]=1 [6]: Enable PWON_RX_BUF to power on RX CTLE in PMA pwdn_ctrl[0]=1 [7]: Enable PWON_CDR to power on RX CDR in PMA pwdn_ctrl[0]=1 [8]: Enable PWON_OOB_DET to power on SATA OOB detect in PMA pwdn_ctrl[0]=1 [9]: Enable PWON_HS_DET to power on SATA high speed data detect in PMA pwdn_ctrl[0]=1

Multi-PHY_Register004

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	RX_RTERM_VCOM RX vcom voltage select signal 2'b00: GND 2'b01/10: floating 2'b11: 320mV
5:0	RO	0x00	reserved

Multi-PHY_Register005

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

Multi-PHY_Register006

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	PLL_CLKREF_DIV Pll input clock divider, valid when su_trim[14]=1 2'b00: 1 2'b01: 1/2 2'b10: 1/3 2'b11: 1/4
5:0	RO	0x00	reserved

Multi-PHY_Register007

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x8	TX_RTERM TX output resister adjust signal by step about 1ohm 4'b0000: 60 4'b1000: 50 4'b1111: 44 default: not supported
3:0	RW	0x8	RX_RTERM RX input resister adjust signal by step about 1ohm 4'b0000: 60 4'b1000: 50 4'b1111: 43.5 default: not supported

Multi-PHY_Register008

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	BYPS_CDR_EN 1'b0: CDR recovered clock will be operation while PLL is locked and CDR is operation, and rx_cdr_trim[7] only can be set to 1'b0 using reference clock for rx_rdy generation. 1'b1: CDR recovered clock will be operation while PLL is locked, and rx_cdr_trim[7] can be set to 1'b1 using recovered clock for rx_rdy generation.
6	RW	0x0	TX_SWING Reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	NEAR_END_LPK_ENABLE PHY Near end loop back enable in BIST mode
4	RW	0x0	SSC_EN In U3 and SATA mode, this bit= 1, set SSC on In PCIE mode, this bit=0 set SSC off
3:0	RW	0x8	TX_SWING_COM TX boost level adjust signal 3'b000: minimum 3'b111: maximum default: not supported

Multi-PHY_Register009

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	BYPS_CDR_FL_EN 1'b0: rx_rdy is pulse singal to indicate CDR start to clock and data recoved from input serial data. 1'b1: rx_rdy is not controlled by PMA/PCS interface signal "cdr_fl_en".
6	RW	0x1	BYPS_CPATH_LIMIT 1'b0: CDR CPATH will be reset while CDR CPATH is overflow. 1'b1: CDR CPATH will be locked to MAX frequency offset while CDR CPATH is overflow.
5	RW	0x1	BYPS_CPATH_OVERFLOW 1'b0: CDR CPATH is controlled by CDR CPATH overflow. 1'b1: CDR CPATH is not controlled by CDR CPATH overflow
4	RW	0x0	BYPS_FGAIN_ADPT 1'b0: CDR CPATH gain is X2 while CDR recover frequency while rx_cdr_trim[6]=0. 1'b1: CDR CPATH gain is X1 while CDR recover frequency while rx_cdr_trim[6]=0.
3	RW	0x0	BYPS_PWON_RX_BUF 1'b0: CTLE and LOS detector is controlled by PWDN[1:0]. 1'b1: CTLE and LOS detector is operation while reference clock and RX termination are present.
2	RW	0x0	BYPS_PWON_RX_CDR 1'b0: CDR is controlled by PWDN[1:0]. 1'b1: CDR is operation after PLL is locked while reference clock and RX termination are present.
1	RW	0x0	BYPS_PWON_TX_BUF 1'b0: TX Driver is controlled by PWDN[1:0]. 1'b1: TX Driver is operation after PLL is locked while reference clock is present and TX detect RX is finished.
0	RW	0x0	BYPS_RESETN 1'b0: PMA is reset by RSTN. 1'b1: PMA is not controlled by RSTN.

Multi-PHY_Register011

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x5d	SU_TRIM[7:0] Refer as SU adjust signal[7:0] [2:0]: PLL KVCO adjust, 000: min, 111:max [3]: PLL force lock [6:4]: PLL charge pump current adjust, 000: min, 111:max [7]: PLL LPF R1 adjust[0] 0: max, 1:min [11]: bypass pll power down control [12]: bypass ref clock detect function [13]: bypass vcntl detect [14]: bypass PLL loop divider code [15]: bypass ivref power down control [16]: bypass PLL lock detect mode of always detect [17]: bypass POR function [18]: bypass ivref power down control [19]: CKRCV common voltage adjust 0: floating 1: GND [21:20]: CKRCV termination resister adjust 00: 100ohm 01: 200ohm 10: 1000ohm 11: Hi-Z [22]: CKRCV mode select 0: difference receiver mode 1: signal receiver mode (CKREFP is valid,CKREFN is disable) [24:23]: CKRCV amp input common voltage adjust 00: 480 mV 01: 510 mV 10: 600 mV (default) 11: 660 mV [28:25]: CKDRV output swing adjust, 0000:100 mV, 1111:860 mV, step:50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

Multi-PHY_Register012

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	SU_TRIM[15:8] Refer as SU adjust signal [15:8] [2:0] PLL LPF R1 adjust, 00: max, 11:min [3]: bypass pll power down control [4]: bypass ref clock detect function [5]: bypass vcntl detect [6]: bypass PLL loop divider code [7]: bypass ivref power down control

Multi-PHY_Register013

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	SU_TRIM[23:16] Refer as SU adjust signal [23:16] [0]: bypass PLL lock detect mode of always detect [1]: bypass POR function [2]: bypass ivref power down control [3]: CKRCV common voltage adjust 1'b0: floating 1'b1: GND [5:4]: CKRCV termination resister adjust 2'b00: 100ohm 2'b01: 200ohm 2'b10: 1000ohm 2'b11: Hi-Z [6]: CKRCV mode select 1'b0: difference receiver mode 1'b1: signal receiver mode (CKREFP is valid,CKREFN is disable) [7]: CKRCV amp input common voltage adjust[0] 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [28:25]: CKDRV output swing adjust, 0000:100 mV, 1111:860 mV, step:50 mV [29]: CKDRV input clock select signal, 0: ck100m_pcie from PLL 1: ckref from CKRCV [31:30]: CKDRV output slew rate adjust, 00: fast, 11: slow

Multi-PHY_Register014

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x3b	SU_TRIM[31:24] Refer as SU adjust signal[31:0] [0]: CKRCV amp input common voltage adjust[1] 2'b00: 480 mV 2'b01: 510 mV 2'b10: 600 mV (default) 2'b11: 660 mV [4:1]: CKDRV output swing adjust 4'b0000:100 mV 4'b1111:860 mV step:50 mV [5]: CKDRV input clock select signal 1'b0: ck100m_pcie from PLL 1'b1: ckref from CKRCV [7:6]: CKDRV output slew rate adjust 2'b00: fast 2'b11: slow default: not supported

Multi-PHY_Register015

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x1	SSC_CNT[1:0] PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signals should be set to its default value unless the user want change the 31.5KHz SSC modulation frequency When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want change the 32.8KHz SSC modulation frequency
5:2	RW	0x0	TEST_SEL Reserved
1	RW	0x0	RX_TSEQ USB Mode When asserted, it is used to instruct USB3.0 PHY to bypass normal operation and do a receiver equalization training. Please refer to PIPE3 interface and USB3.0 base spec for more detail information
0	RW	0x0	EN_ADPT Adaptive Continuous Time Linear Equalizer (CTLE) enable signal 1'b1: enable adaptive CTLE 1'b0: disable adaptive CTLE

Multi-PHY_Register016

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x63	SSC_CNT[9:2] PLL control SSC module period When the pll_ckref_inner is 100MHz/25MHz, This signals should be set to its default value unless the user want change the 31.5KHz SSC modulation frequency When the pll_ckref_inner is 24MHz, this signal should be set to its default value unless the user want change the 32.8KHz SSC modulation frequency

Multi-PHY_Register017

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	PLL_DIV[7:0] Pll loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction

Multi-PHY_Register018

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	FREZ_APT_EQ 1'b1: the adaptive equalizer will freeze at its final result when equalizer training pattern transmission is done. This signal is used in USB3.1 mode, when equalizer training pattern transmission is done, IP user can stop adaptive equalization and freeze the result. 1'b0: the adaptive equalizer will be always working when the adaptive equalizer function is enable

Bit	Attr	Reset Value	Description
6:0	RW	0x32	PLL_DIV[14:8] Pll loop divider, valid when su_trim[14]=1, [14:10] is the integer number of divider factor, and [9:0] are the decimal fraction

Multi-PHY_Register019

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RW	0x0	RX_AFE_TRIM Receiver 2st stage equalizer res control, used to adjust pole-zero of RX eq.
2:0	RW	0x3	RX_AFE_CTRIM Receiver 1st stage equalizer cap control, used to adjust pole-zero of RX EQ

Multi-PHY_Register020

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	BEACOM_TIMEOUT_SEL PCIE beacon timeout select
4	RW	0x0	RX_POLAR RX output polarity set 1'b0 : no invert RX output data polarity 1'b1 : invert RX output data polarity
3:0	RW	0x7	RX_AFE_RTRIM Receiver 1st stage equalizer res control, used to adjust pole-zero of RX eq

Multi-PHY_Register021

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x11	RX_SQDET_TRIM[7:0] RX squelch adjust[7:0] [2:0]: squelch input filler bandwidth adjust; 3'b000: max bandwidth 3'b111: min bandwidth default: not supported [4:3]: squelch delay adjust; 2'b00: max delay 2'b11: min delay default: not supported [6:5]: amp bias adjust, 2'b00: max ibias 2'b11: min ibias default: not supported [7]: squelch detect vth adjust[0] 2'b00: min vth 2'b11: max vth default: not supported

Multi-PHY_Register022

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x4	RX_ADPT_EQ_TRIM[3:0] RX_ADPT_EQ_TRIM[3:0] [6:4]: adaptive equalizer detection threshold control [7]: adaptive equalizer gain control
3:0	RW	0x1	RX_SQDER_TRIM[11:8] RX squelch adjust[11:8] [0]: squelch detect vth adjust[1] 2'b00: min vth 2'b11: max vth default: not supported [1]: bypass rx_superspeed, 1: rx_superspeed=1 [2]: rx_superspeed function select 1'b0: ~los output, 1'b1: ~los output | squelch output [3]: rx_pcie_idle function select 1'b0: ~ squelch output 1'b1: los output

Multi-PHY_Register023

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2c	RX_ADPT_EQ_TRIM[11:4] RX_ADPT_EQ_TRIM[11:4] [2:0]: adaptive equalizer bandwidth control [4:3]: adaptive output refresh bandwidth control [5]: bypass the adaptive Cj function [6]: test mode select [7]: Reserved

Multi-PHY_Register024

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x3	RX_CDR_TRIM[3:0] [3]: CDR gain adjust, 1: 1/8. 0: 1/4([4]=1), 1/8([4]=0) [2:0]: The slew rate control for PI, 000: fast slew rate, 111: slow slew rate
3:0	RW	0x0	RX_LOS_TRIM RX los detect adjust [1:0]: low vth adjust; [3:2]: Reserved

Multi-PHY_Register025

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RX_CDR_TRIM[11:4] [0]: CDR gain adjust 1'b0: 1/8. 1'b1: 1/4 when rx_cdr_trim[3]=1 [1]: CDR phase path gain adjust 1'b0: x1 1'b1: x2 [2]: CDR cpath bandwidth gain adjust 1'b0: low bandwidth 1'b1: high bandwidth [3]: rx_rdy counter clock select 1'b0: ref clock 1'b1: CDR recovery clock [5:4]: rx_rdy delay time select 2'b00: 1.28us 2'b01: 0.64us 2'b10: 2.56us 2'b11: 5.12us [7:6]: Reserved

Multi-PHY_Register026

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TX_TRIM[7:0] TX adjust [3:0]: TX FFE adjust valid when tx_trim[4]=1; [4]: manual mode enable [5]: force rterm detect ready, 1: force rtern_det_out=1 [6]: force eidle, 1: txp/txm is eidle [7]: hi-z idle enable

Multi-PHY_Register027

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	TX_TRIM[15:8] TX adjust [0]: tx_pck invert enable [1]: MSB enable [2]: bypass low resister eidle mode 1'b0: eidle has not hi-z mode 1'b1: eidle has hi-z mode [3]: bypass 0.6kohm charge resister 1'b0: 0.6kohm resister 1'b1: 1kohm resister [5:4]: rterm detect vth adjust; 2'b00: max vth 2'b11: min vth [6]: bypass signal of gate_tx_pck,

Multi-PHY_Register028

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RX_TRIM [0]: rx_pck invert enable [1]: RX MSB enable [7:2]: Reserved

Multi-PHY_Register029

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	TX_MARGIN Reserved
4:0	RW	0x05	RTERM_DET_TRIM [1:0]: rterm detect pre-charge time adjust 2'b00: 512us 2'b11: 4096us [3:2]: rterm detect post-charge time adjust 2'b00: 8us 2'b11: 64us [4]: Reserved

Multi-PHY_Register030

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	UNUSED Reserved
3	RO	0x0	reserved
2:0	RW	0x0	TX_DEEMPH[2:0] Reserved

Multi-PHY_Register031

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TESTO_SEL pcs internal signal to testo io select

Multi-PHY_Register032

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	RES[7:0] [0]: bypass the mode of pd_ck100m controlling CKDRV 1'b0: CKDRV is on only in PCIE mode 1'b1: CKDRV is controlled by ckref_src[1:0]; [1]: select signal of pll_lock to TX/RX 1'b0: pll_lock is controlled by rate[1:0] 1'b1: pll_lock is not controlled by rate[1:0] [2]: bypass the mode of rate[1:0] controlling pll_lock_pcs 1'b0: pll_lock_pcs is controlled by rate[1:0] 1'b1: pll_lock_pcs is not controlled by rate[1:0] [7:3]: Reserved

Multi-PHY_Register033

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	RES[15:8] [0]: pll_rdy delay control when rate change 1'b0: delay 3*TX_PCK relative to the falling edge of gate_tx_pck, 1'b1: delay about 20us relative to the falling edge of gate_tx_pck [1]: select pll_lock to TX/RX 1'b0: pll_lock_txrx is same to pll_lock_pcs 1'b1: pll_lock_txrx is not controled by gate_tx_pck [4:2]: PLL KVCO fine tuning signals [7:5]: Reserved

22.4 Interface Description
22.5 Application Notes
22.5.1 Operation Mode Support
The following mode are supported for IP operation, IP configuration other than this list are not supported

Table 22-1 PHY operation mode

QSGMII MODE	PHY_MODE	RATE	BUS_WIDTH	PHY Operation Mode
0	00	00	00	PCIE Gen1, 32bit, PCLK=62.5M
			01	PCIE Gen1, 16bit, PCLK=125M
		01	00	PCIE Gen2, 32bit, PCLK=125M
			01	PCIE Gen2, 16bit, PCLK=250M
	01	00	00	USB3.0, 32bit, PCLK=125M
	01	00	01	USB3.0, 16bit, PCLK=250M
	10	00	00	SATA Gen1, 32bit, PCLK=37.5M
			01	SATA Gen1, 16bit, PCLK=75M
		01	00	SATA Gen2, 32bit, PCLK=75M
			01	SATA Gen2, 16bit, PCLK=150M
		10	00	SATA Gen3, 32bit, PCLK=150M
			01	SATA Gen3, 16bit, PCLK=300M
1	00	00	01	SGMII, 20bit, PCLK=62.5M
		10	01	QSGMII, 20bit, PCLK=125M

- QSGMII MODE is configured by GRF_PIPE_CON3[15]
- PHY MODE is configured by GRF_PIPE_CON2[1] first to enable the selection, then configured by GRF_PIPE_CON0[3:2]
- RATE is configured by GRF_PIPE_CON0[5:4]
- BUS_WIDTH is configured by GRF_PIPE_CON0[1:0]

22.5.2 POWER DOWN MODE
Power down control signals to individual analog modules are generated based on PWDN[1:0]

setting from PIPE inputs as shown in table2/3/4. An override function is provided for debug purpose, see register list. (√ – active; ×– power down)

Table 22-2 PCIE power down mode

PWDN[1:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
00	--	√	√	√	√
01	0(illegal)	√	√	√	√
	1	×	√	√	√
10	0(illegal)	√	×	×	√
	1	×	×	×	√
11	0	√	×	×	×
	1	×	×	×	×

In PCIE mode, power for IVREF and PCIE idle detector are always on, while power for LFPS, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

Note: If TX_ELECIDLE and TX_COMPLIANCE are both asserted, all powers are off.

Table 22-3 USB3 power down mode

PWDN[1:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
00	--	√	√	√	√
01	0	√	√	×	√
	1	√	√	×	√
10	0	√	√	×	√
	1	√	√	×	√
11	0	√	√	×	×
	1	×	√	×	×

In USB3.0 mode, power for IVREF and LFPS detector are always on, while power for PCIE idle, 1.5G SATA idle and 3G/6G SATA idle detectors are always off, and power of LFPS detector and power of Rx buffer are turned off if termination is not on.

Table 22-4 SATA power down mode

PWDN[1:0]	TX_ELECIDLE	TX_Buffer	RX_Buffer	CDR	TX_PLL
00	--	√	√	√	√
01	0(illegal)	√	×	√	√
	1	×	×	√	√
11	0	√	×	×	√
	1	×	×	×	√

In SATA mode, power for IVREF and 1.5G SATA idle detector are always on, while power for LFPS and PCIE idle detectors are always off, and power of Rx buffer is off when RX_STANDBY is high.

Chapter 23 AXI_SPLIT

23.1 AXI_SPLIT

AXI_SPLIT is a bridge between main bus interconnect and DDR controller to covert standard AXI protocol to specific format that conforms to the AXI interface of the DDR controller. It is designed to support the applications that two different capacity of memory particles are used in 32-bit memory interface or 16-bit memory interface.

AXI_SPLIT supports the following features:

- Support bypass mode
- Support one internal 12-bit wide and 32-location deep FIFO for storing AXI read command
- Support split address configurable by DDRGRF
- Support memory system made up of different capacity of memory particles
- Support the high or low 16 bits of 32-bit memory interface, high or low 8 bits of 16-bit memory interface configurable if the input address is above the split address

23.2 Block Diagram

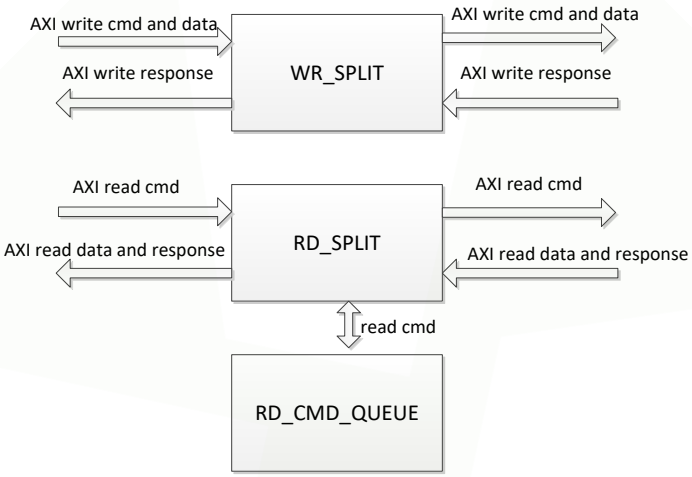


Fig.23-1 AXI_SPLIT Block Diagram

AXI_SPLIT comprises with:

- WR_SPLIT: AXI write split
- RD_SPLIT: AXI read split
- RD_CMD_QUEUE: AXI read command queue

The WR_SPLIT and RD_SPLIT are used to covert standard AXI protocol to specific format. In order to support read outstanding transactions, the read commands extracted from standard AXI are pushed into RD_CMD_QUEUE and pop from the queue if read response return.

23.3 Register Description

This section describes the control/status registers of the design. There is no configuration port in AXI_SPLIT, it is configured by DDR_GRF. Please refer to DDR_GRF or the following register summary.

23.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
AXI_SPLIT_SPLIT_CTRL	0x0000	W	0x00000110	Split Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.3.2 Detail Register Description

AXI_SPLIT_SPLIT_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:9	RW	0x0	SPMODE 2'b00: DDR controller and PHY are configured as 32 bits mode. Low 16 bits are valid if access address is above split address. 2'b01: DDR controller and PHY are configured as 32 bits mode. High 16 bits are valid if access address is above split address. 2'b10: DDR controller and PHY are configured as 16 bits mode. Low 8 bits are valid if access address is above split address. 2'b11: DDR controller and PHY are configured as 16 bits mode. High 8 bits are valid if access address is above split address.
8	RW	0x0	BYPASS 1'b0: Not bypass 1'b1: Bypass
7:0	RW	0x00	SPADDR Split address high 8 bits. For example, if SPADDR=0x10, then the split address is 0x10000000. The AXI_SPLIT will be bypassed if read or write DDR below split address, otherwise a standard AXI burst will be split.

23.4 Application Notes

The AXI_SPLIT begins to work if BYPASS=0 and write or read DDR address are above SPADDR, otherwise it will be bypassed. Following figures are four modes that it supports. In order to illustrate how the AXI_SPLIT works, it assumes that total range of DDR is from 0x00000000 to 0x2fffffff and split address is 0x20000000.

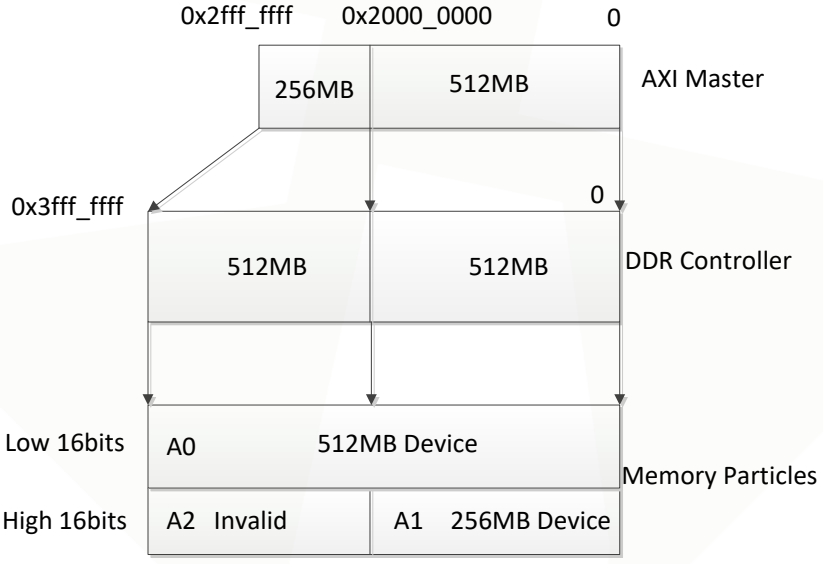


Fig.23-2 Mode 0

Mode 0 shows that an AXI Master can access DDR from address 0x00000000 to 0x2fff_ffff. The AXI_SPLIT will convert input write or read DDR address above split address if BYPASS is 0, and then output converted address to the DDR controller. As a result, area A2 is invalid and will not be accessed. This mode is only valid if the DDR controller and PHY are configured as 32-bit mode.

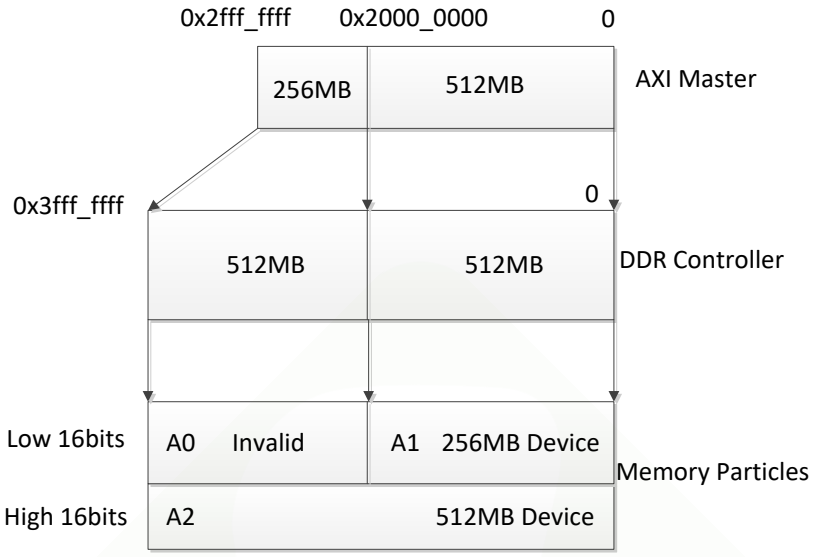


Fig.23-3 Mode 1

Mode 1 is similar as mode 0 except that high 16 bits are valid if access address is above split address. As a result, area A0 is invalid and will not be accessed.

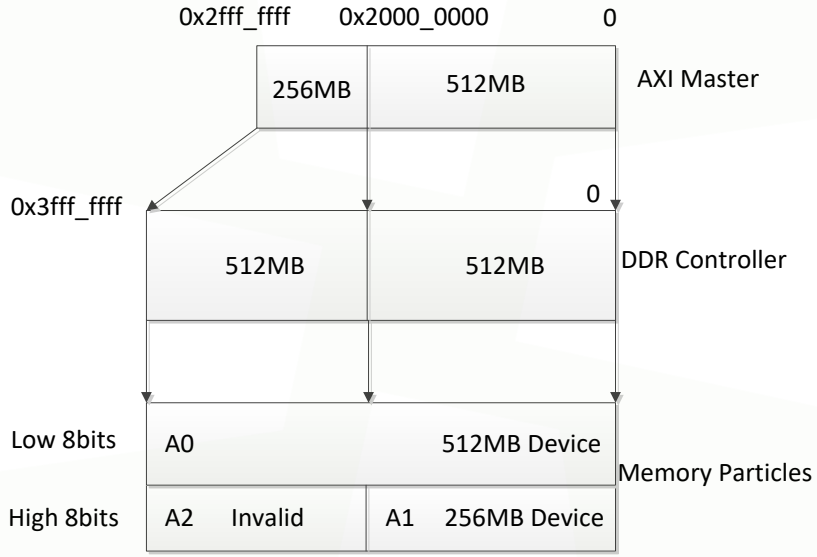


Fig.23-4 Mode 2

Mode 2 is only valid if the DDR controller and PHY are configured as 16-bit mode. As a result, area A2 is invalid and will not be accessed.

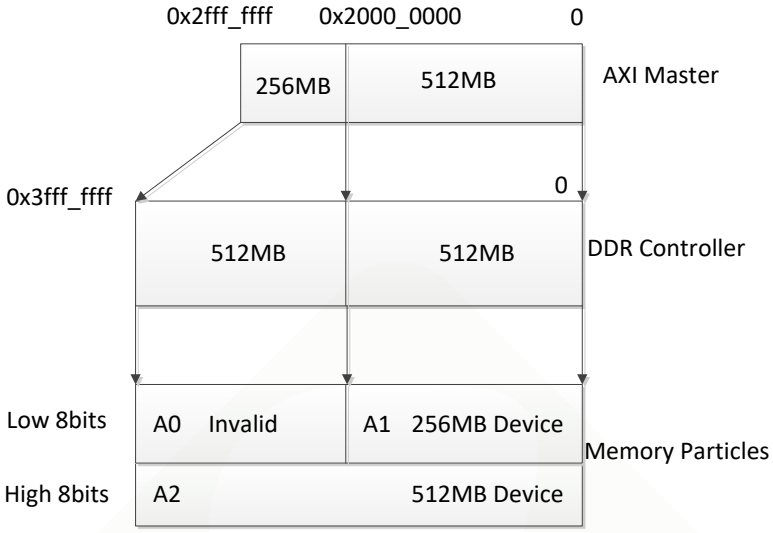


Fig.23-5 Mode 3

Mode 3 is similar as mode 2 except that high 8 bits are valid if access address is above split address. As a result, area A0 is invalid and will not be accessed.

Chapter 24 CAN

24.1 Overview

CAN (Controller Area Network) bus is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer. It is a message-based protocol, designed originally for multiplex electrical wiring within automobiles to save on copper, but is also used in many other contexts.

CAN controller supports the following features:

- Support CAN 2.0B protocol
- Support 32-bit APB bus
- Support classical and can-fd transmit or receive standard frame
- Support classical and can-fd transmit or receive extended frame
- Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval
- Support transmit or receive error count
- Support acceptance filtering
- Support bit error, bit stuffing error, form error, ack error and crc error
- Support 7 types of interrupt and all interrupt can be masked
- Support CAN controller status query
- Support capture the bit position of arbitration section where the arbitration was lost
- Support error code check
- Support self test mode
- Support single sample and three sample configurable
- Support SJW(reSynchronization Jump Width) configurable
- Support BRP(system prescaler coefficient) configurable
- Support bit timing configurable
- Support loop-back mode for self-test operation
- Support silent mode for debug
- Support receive self-transmit data mode(rxstx_mode)
- Support TX data and RX data order select
- Support RX data cover mode
- Support auto retransmission mode
- Support auto bus on after bus-off state
- Support space_rx_mode
- Support transmitter delay compensation and SSP position configurable
- Support sleep mode
- Support timestamp
- Support transmit event FIFO
- Support 2 transmit buffers
- Support receive buffer/FIFO mode
- Support protocol exception event
- Support DMA

24.2 Function Description

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

24.2.1 Block Diagram

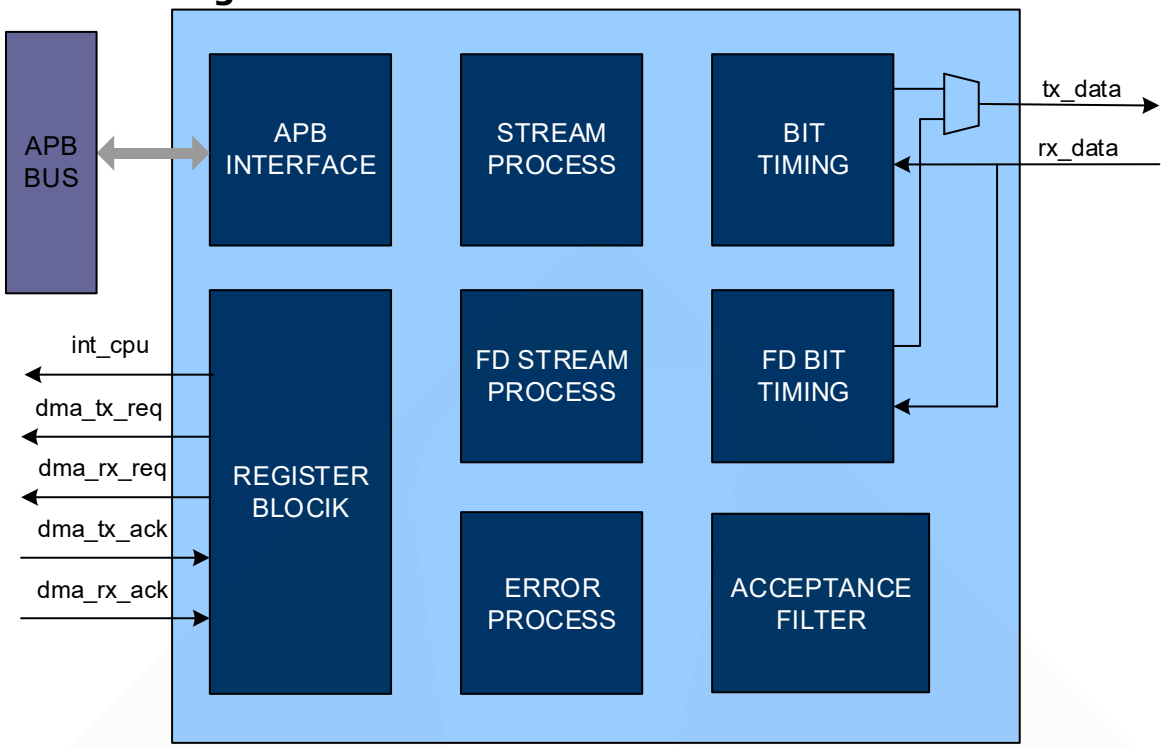


Fig.24-1 CAN Controller Block Diagram

This version of CAN controller includes the previous version of CAN logic in compliance with old software application and also includes new CANFD logic which support transmitting and receiving both CAN and CANFD frame.

24.2.2 ACCEPTANCE FILTER

The acceptance filter performs filtering using the acceptance ID register and the ID mask register. The acceptance filter uses multiple-time filtering. It includes the old version receiving filter and five addition ID filters. Each ID filter pair has a Filter Mask register and a Filter ID register. Each filter pair is controlled by corresponding FILTER CTRL bit in AFR register. For each pair using ID register and ID mask register(controlled by acceptance filter register)sampling all the bits of the ID, it is compared with the ID register. It is not a comparison every time a bit is sampled. And don't check the bit in the ID mask register that is 1. Once all the ID bits have passed the filtering, the controller considers the frame data as the desired ID, thereby performing the next operation.

24.2.3 BIT TIMING

24.2.3.1 Bit Timing Logic

The CAN FD protocol defines two bit rates, the first for the ARBITRATION-PHASE with a longer bit time and the second for the data phase with the same or with a shorter bit time. The definition for the first bit rate is the same as for the NOMINAL BIT RATE and the NOMINAL BIT TIME in the CAN protocol specification. The definition for the second bit rate, the DATA BIT RATE WITH the DATA BIT TIME, requires a separate configuration register set.

The bit timing logic controls the sampling point position through the buffer bits in the timing register to ensure the accuracy of the data sampling. The bit timing logic receives the clock frequency division signal for identification, sets the bus timing parameters, establishes synchronization parameters, and adjusts the bus transmission rate. At the same time, the bus is monitored and the message to be sent is transmitted to the bus at the set timing.

According to the provisions of the CAN protocol: the CAN bus is always at a high level when no message is sent, and the continuous recessive bit is monitored on the bus. At this time, the bus is in an idle state, and the arbitration priority is low, ready to receive data at any time. When the bus detects a transition from a recessive bit to a dominant bit, it is proved that the frame start bit starts transmitting, and the bus performs a hard synchronization in the bit start sync segment. Then, in the process of receiving the message, once the edge of the transition close to the sampling point is detected and the

edge of the edge and the synchronization segment have a phase error lower than the synchronization width (SJW is taken when the value exceeds SJW), the controller executes once resynchronization, resynchronization can be performed multiple times during one data transmission.

24.2.3.2 Bit Timing Definition

The transmission time of each bit is divided into 4 parts:

$$t_{nbt} = t_{sync\_seg} + t_{prop\_seg} + t_{phase\_seg1} + t_{phase\_seg2}$$

t_{sync_seg}, t_{prop_seg}, t_{phase_seg1} and t_{phase_seg2} are integer multiples of the unit time(t_{sclk}), and this unit time is a specific multiple of the system clock, which is determined by the division factor BRP in the bus timing register: 1. The counter is obtained by the BRP operation; 2. The system clock clk is counted by the counter; 3. When the limit is reached, a clock with a period of t_{sclk} is generated.

In the system design, considering the cyclical occurrence of each time period, a state machine with three states is used in the bit timing design. The three states correspond to the sync segment(sync_seg) and the phase buffer segment 1 (phase_seg1=phase_seg1+prog_seg) and the phase buffer segment 2 (phase_seg2), respectively. Where PHASE_SEG1 range: 1~16; PHASE_SEG2 range: 1~8; BRP range: 1~64.

$$t_{sync\_seg} = 1 \times t_{sclk}$$

$$t_{prop\_seg} + t_{phase\_seg1} = t_{sclk} \times (8 \times TSEG1.3 + 4 \times TSEG1.2 + 2 \times TSEG1.1 + TSEG1.0 + 1)$$

$$t_{phase\_seg2} = t_{sclk} \times (4 \times TSEG2.2 + 2 \times TSEG2.1 + TSEG1.0 + 1)$$

Define a counter to count t_{sclk}. When the count reaches the TSEG1, TSEG2 defined in the bus timing register and the length of the synchronization segment defined in the design, the system will generate the corresponding transition conditions: go_seg1, go_seg2, go_sync. By judging these transition conditions, the control state machine cycles through the above three states.

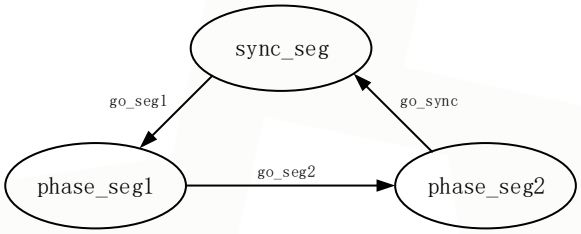


Fig.24-2 Bit timing FSM

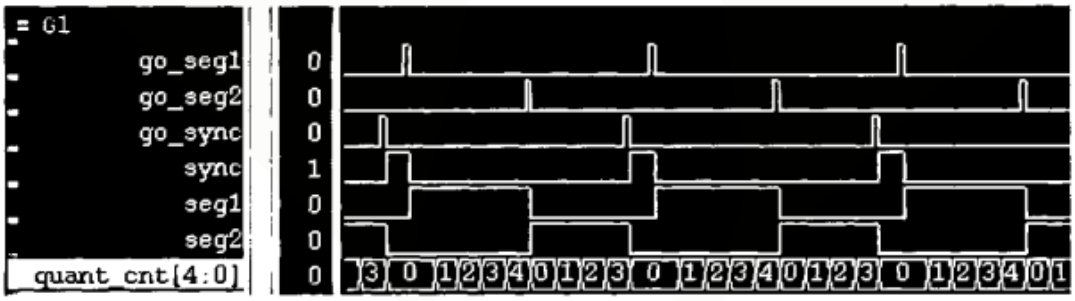


Fig.24-3 Bit timing waveform diagram

24.2.3.3 Bit time transition

The first part of a CAN FD frame, until the BRS bit, is transmitted with the NOMINAL BIT RATE. The bit rate is switched if the BRS bit is recessive, until the CRC DELIMITER is reached or until the CAN FD controller sees an error condition that results in the starting of an ERROR FRAME. CAN FD ERROR FRAMES, as well as ACK FIELD, END OF FRAME, OVERLOAD FRAMES, and all frames in CAN format are transmitted with the NOMINAL BIT RATE.

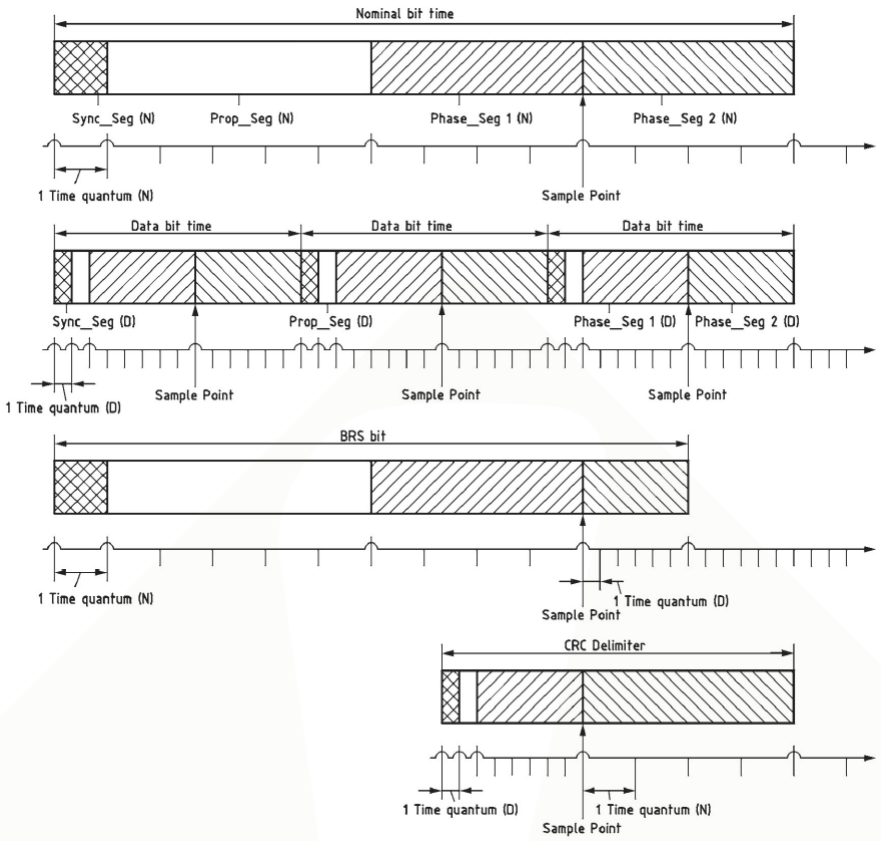
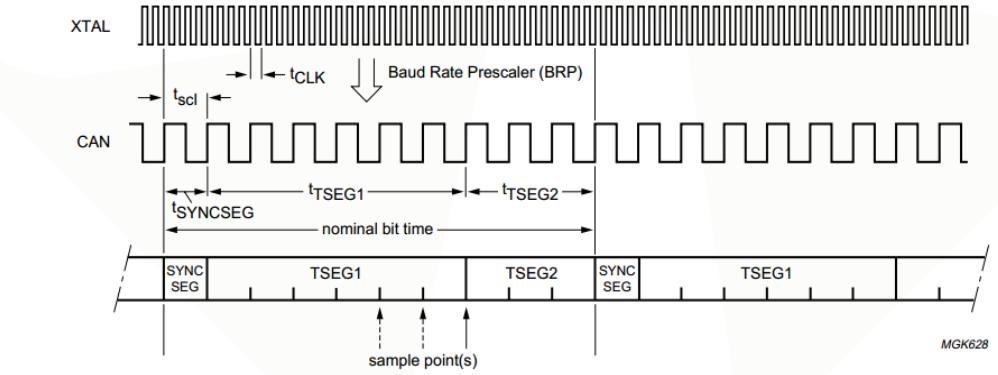


Fig.24-4 CANFD Frame Bit Time

24.2.3.4 Sampling Point and Sending Point

Sampling Point: According to the agreement, the sample point sample_point should be between phase_seg1 and phase_seg2. It is designed to be in the position of phase_seg2 synchronization. The sampling pulse width is defined as one system clock cycle. Considering the accuracy of sampling, you can use the method of taking three samples to take the mean. The interval between each sample point is one t_{sclk}.



Possible values are BRP = 000001, TSEG1 = 0101 and TSEG2 = 010.

Fig.24-5 Three sampling diagram

Sending Point: The location of the transmission point(tx_point) should be at the beginning of each bit time according to the protocol, and it is designed to synchronize it with the go_sync signal. In addition, if it is in sync or resynchronize, tx_point will be valid immediately.

24.2.3.5 Bit Synchronization

With the synchronization method, one or more nodes that satisfy the synchronization condition align their synchronization segments with the transmission data on the bus at a

specific time. Synchronization occurs on the 1-to-0 transition edge in order to control the distance from the transition edge to the sample point. Two synchronization methods are defined in the CAN bus communication protocol: hard synchronization and resynchronization.

Hard_sync: All nodes must be synchronized to the leading edge of the starting frame of the node that first started transmitting the message. At the beginning of each frame of data, a synchronization action is taken between the nodes.

Hard synchronization implementation method: determine whether the bus state meets the frame start condition specified in the protocol, and the node is not in the state of the data to be transmitted. At this time, a hard synchronization flag signal hard_sync is generated, and the pulse width is a system clock; The hard_sync entry is added to the control condition of the go_seg1 signal, and go_seg1 is valid immediately when the hard_sync signal is '1'. Therefore, once the hard synchronization condition is met, the system enters the phase_seg1 segment, thereby achieving synchronization.

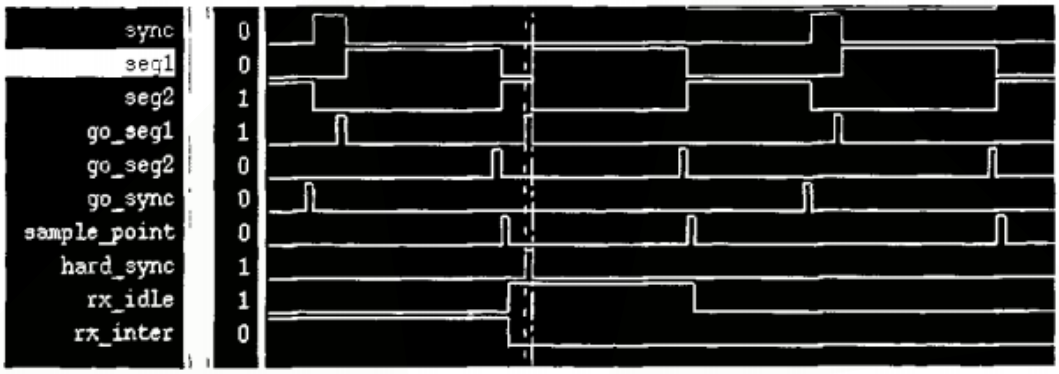


Fig.24-6 Hard_sync waveform diagram

Resynchronization: In addition to generating hard synchronization at the beginning of each frame of data, the CAN bus communication protocol also specifies the transmission of data for each frame. When the timing coordination between the nodes is not ideal, it will be resynchronized, so that the cooperation between the nodes is in a good state.

For the receiver, the bus changes it received should occur in the sync segment. Once the receiver's status violates this rule, the receiver will perform a resynchronization.

Two situations that require resynchronization:

1. The jump of the bus value '1' to '0' occurs between the sync segment and the sample point, which is a delay jump;

2. The jump of the bus value '1' to '0' occurs between the sample point and the sync segment, which is an early jump.

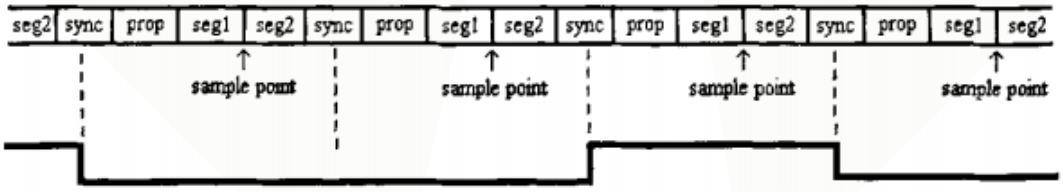


Fig.24-7 Resynchronization

Resynchronization method:

1. Condition for resynchronization: the receiver is in a mode of receiving data (not inter-frame space or bus idle), and a resynchronization flag signal ‘resync’ is generated when a jump of the bus value '1' to '0' occurs;

2. According to the position of the resynchronization flag signal, it is determined that the abnormal jump is a delay jump or an early jump;

3. Counting the delay or the length of the advance by the counter;

4. In this bit, phase_seg1 is added with a delay time or phase_seg2 is subtracted from the advance time to obtain a new phase buffer time for the bit, thereby achieving synchronization.

24.2.3.6 Transmitter Delay Compensation

During the data phase of a CAN FD transmission, only one node is transmitting; all others are receiving. Therefore, the propagation delay does not limit the maximum data

rate.
When transmitting via pin, TXCAN, the CAN FD Controller module receives the transmitted data from its local CAN transceiver via pin, RXCAN. The received data are delayed by the CAN
transceiver's loop delay. In case this delay is greater than 1 + DTSEG1, a bit error will be detected.

In order to enable a data phase bit time that is shorter than the transceiver loop delay, the
Transmitter Delay Compensation (TDC) is implemented. Instead of sampling after DTSEG1, a
Secondary Sample Point (SSP) is calculated and used for sampling during the data phase of a
CAN FD message.

Fig. 1-8 illustrates how the transceiver loop delay is measured and Equation SSP = TDCV + TDCO shows how the SSP is calculated.

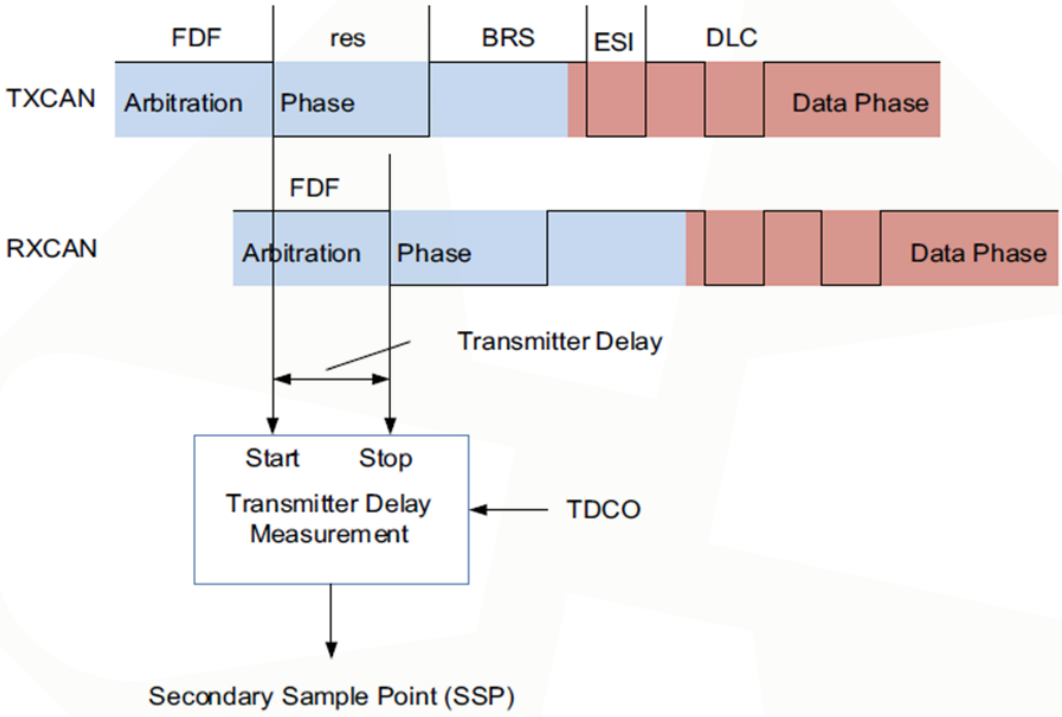


Fig.24-8 Measurement of Secondary Sample Point

24.2.4 STREAM PROCESS

24.2.4.1 Data Buffering

The data cache includes two parts: a transmit buffer and a receive buffer. The data to be sent on the CAN bus is loaded into the buffer area. This buffer area is called the "transmission buffer"; The data received from the CAN bus is also stored in the buffer area, which is called the "receiver buffer". The size of the buffer is 13 bytes, including 1 byte frame information, 2 to 4 byte identifiers (standard or extended frame), and 8 bytes of data.

The CPU configures the transmission of the data information (frame information, identification code, data), and then enable the transmit bit. The transmit data information is spliced into a parallel complete data to be transmitted (including the CRC check code) according to the current frame information and stored in transmission buffer. Stream process unit wait for the appropriate time to send data to the bit timing unit.

The received message is placed in the receiving buffer. After receiving, the receiving completion interrupt will be generated. After receiving the interrupt, the CPU will read the data in the receiving buffer and clear the receiving buffer, and STATE[0] will be 0. If the CPU does not read in time, STATE[1] will remain at 1. If a new message is received at this time,

overflow will occur and not respond with ack by default.

In new CANFD design, there is another independent transmit buffer which has another corresponding transmit request bit. Besides, there is a receive FIFO can be configured to use. Rx data has a RDATA address to be read by host. The size of data is 18 word (1 word frame information, 1 word Id, 16 word data) for transmit and 19 word (1 word timestamp additional) for receive. Rx FIFO has 32bits×128 memory space which allow to contain 6 receive message.

Two transmit request bit in CAN_CMD corresponds to two transmit buffers. Transmit message must written to registers before setting transmit request bit. After setting transmit request bit, transmit messages in registers stores in corresponding transmit buffer. When the RKCAN buffer1 transmission frame complete, 'tx_req_1' is automatically cleared to 0.

CANFD support RX FIFO. When FIFO enabled, receive data stored in FIFO as Receive FIFO message format shown below. Rdata should read from the RXFIFO entrance. IF FIFO is disabled, Rdata stored in Rdata registers and should read from those registers every time.

Table 24-1 Receive FIFO message format

NAME	Offset	Access	Description
RX FIFO RB0-INFO	0x0000	RO	Same as CAN_RXFRAMEINFO
RX FIFO RB0-ID	0x0004	RO	Same as CAN_RXID
RX FIFO TB0-TIMESTAMP	0x0008	RO	RX TIMESTAMP VALUE
RX FIFO RB0-DATA0	0x000c	RO	Same as CAN_RXDATA
RX FIFO RB0-DATA1	0x0010	RO	Same as CAN_RXDATA
RX FIFO RB0-DATA2	0x0014	RO	Same as CAN_RXDATA
...	...	...	...
RX FIFO RB0-DATA15	0x0048	RO	Same as CAN_RXDATA

24.2.4.2 Receive Data

According to the bus protocol, taking the data frame of the extended frame format as an example, the receiving data state machine is as follows:

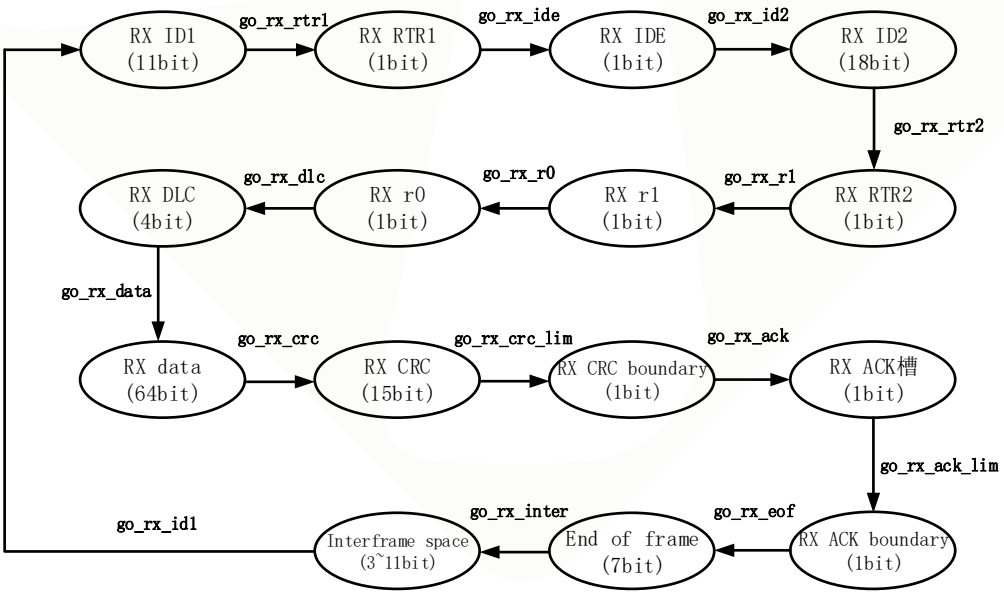


Fig.24-9 Receive data state diagram

Each state of the state machine corresponds to which "field" of the frame data the receiver is in when receiving data, and only one of all state flags is valid at the same time. The method of implementation is as follows:

Define a bit counter(bit_cnt), add one to each sample point (provided by the bit timing

module). At the same time, according to the current state of the state machine, it is determined in this state that the bit counter needs to count to what value (determined by the length of each field defined in the protocol) to generate a jump signal to the next state transition. Whenever a hopping signal is generated, the counter is cleared and ready to begin counting for the next state.

The receiving state machine ensures that the bus controller can automatically recognize the current receiving state when receiving data. After that, the data of each data field needs to be stored in the corresponding register according to different states, and then the next operation is performed.

24.2.4.3 Transmit Data

The CAN FD accesses message element space of a buffer in TX block only if the respective request bit is set. The Host must respect access rules to avoid memory collisions, that is, after the Host sets a buffer ready request through the CMD register, it should not read or write the respective message element space until the respective request bit is in a clear/unset state.

Parallel data is serially transmitted to the bus according to a specific timing. The sending point is the tx_point. The transmit counter is self-added in the valid data portion of the data frame, and is cleared when one frame of data is transmitted or the bus is in an error state.

The implementation is as follows:

1. Combine all the data to be sent into a completely parallel data chain according to the currently set frame type;

2, using tx_pointer as a data link pointer, obtaining a serial data signal (tx_bit) to be transmitted;

3. Determine what type of data to send according to the current state, and determine the data tx_next to be sent at the next transmission time;

4. Synchronize the data transmission signal tx with the tx_next through the transmission point tx_point to obtain a true transmission signal tx.

24.2.4.4 Bit Stuffing

Bit stuffing is a function set to prevent burst errors. Add a bit of inversion data when the same level lasts 5 bits.

In CAN FD format frames, the CAN bit stuffing method is changed for the CRC SEQUENCE. Here, the STUFF-BITS shall be inserted at fixed positions. There shall be a fixed STUFF-BIT before the first bit of the CRC SEQUENCE, even if the last bits of the preceding field do not fulfill the CAN stuff condition. A further STUFF-BIT shall be inserted after each fourth bit of the CRC SEQUENCE. The value of such a fixed STUFF-BIT shall be the inverse value of the bit preceding the fixed STUFF-BIT.

Sending unit: The data between the SOF and CRC segments when transmitting data frames and remote frames. If the same level lasts for 5 bits, the next bit (bit 6) is inserted with the level of the 1st bit and the first 5 bits.

Receiving unit: Data between SOF and CRC segments when receiving data frames and remote frames. If the same level lasts for 5 digits, the next bit (bit 6) needs to be deleted and received. If the 6th bit is the same level as the first 5 bits, it will be treated as an error and an error frame will be sent.

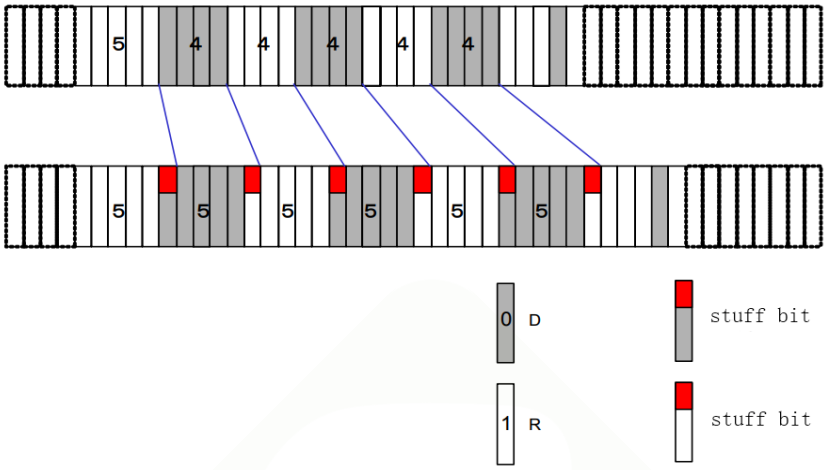


Fig.24-10 Bit Stuffing

24.2.4.5 Transmit Event FIFO

The Transmit Event FIFO (TEF) allows the application to keep track of the order and time the messages were transmitted. The TEF works similar to a Receive FIFO, which is a 32bits× 16 FIFO. Instead of storing received messages, it stores transmitted messages. Messages are only saved if TEF.enable is set. The Sequence Number (SEQ) of the transmitted message is copied into the TEF Object. The payload data are not stored. Transmitted messages are timestamped if TEFTSEN is set. Transmit message format store in TXE FIFO as follow:

Table 24-2 TXE FIFO message format

NAME	Offset	Access	Description
TXE FIFO TB0-INFO	0x0000	RO	Same as CAN_TXFRAMEINFO
TXE FIFO TB0-ID	0x0004	RO	Same as CAN_TXID
TXE FIFO TB0-TIMESTAMP	0x0008	RO	TX TIMESTAMP VALUE
TXE FIFO TB1-INFO	0x000c	RO	Same as CAN_TXFRAMEINFO
TXE FIFO TB1-ID	0x0010	RO	Same as CAN_TXID
TXE FIFO TB1-TIMESTAMP	0x0014	RO	TX TIMESTAMP VALUE
…	…	…	…

24.2.4.6 TIMESTAMP

The CAN FD Controller module contains a Time Base Counter (TBC). The TBC is a 32-bit free-running counter that increments on multiples of CANCLK and rolls over to zero. TBC can be cleared by writing any value to TBC.

- TIMESTAMP_CTRL is used to configure the prescaler for the TBC.
- Setting TIMESTAMP_CTRL.TBCEN enables the TBC.
- Clearing TBCEN disables, stops and resets the TBC.
- The TBC has to be disabled before writing to TBC by clearing TBCEN.
- The application can read TBC at any time. Like with any multibyte counter, the application has to consider that the counter increments and might rollover between reading the different bytes of the counter. A rollover of the TBC will generate an interrupt.

Capturing of time stamps at the SAMPLE POINTS of the START OF FRAME bits of received and transmitted frames.

24.2.5 ERROR PROCESS

There are five types of errors. Multiple errors can occur at the same time.

- **BIT ERROR**:
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at that bit time, when the bit value that is monitored is different form the bit value that is sent. An exception is the sending of a 'recessive' bit

during the stuffed bit stream of the ARBITRATION FIELD of during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interpret this as a BIT ERROR.

- **BIT STUFF ERROR**:
  A STUFF ERROR has to be detected at the bit time of the 6th consecutive equal bit level in a message field that should be coded by the method of bit stuffing.
- **FORM ERROR**:
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits. (Exception is the detection of a dominant bit during the last bit of END OF FRAME by a RECEIVER, or the detection of a dominant bit during the last bit of ERROR DELIMITER or OVERLOAD DELIMITER by any node). When the value of a fixed STUFF-BIT in the CAN FD format CRC SEQUENCE is equal to its preceding bit, this shall also be detected as a FORM-ERROR.
- **ACK ERROR**:
  An ACK ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during the ACK SLOT.
- **CRC ERROR**:
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

24.3 Register Description

24.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

24.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CAN_MODE	0x0000	W	0x00000000	CAN controller working mode configure register
CAN_CMD	0x0004	W	0x00000000	CAN command register
CAN_STATE	0x0008	W	0x00000000	CAN state register
CAN_INT	0x000c	W	0x00000000	Interrupt state register
CAN_INT_MASK	0x0010	W	0x00000000	Interrupt enable registers
CAN_DMA_CTRL	0x0014	W	0x00000000	dma mode control
CAN_BITTIMING	0x0018	W	0x00000000	Bit timing configure register
CAN_ARBITFAIL	0x0028	W	0x00000000	Arbit fail code register
CAN_ERROR_CODE	0x002c	W	0x00000000	Error code register
CAN_RXERRORCNT	0x0034	W	0x00000000	Receive error counter
CAN_TXERRORCNT	0x0038	W	0x00000000	Transmit error counter
CAN_IDCODE	0x003c	W	0x00000000	CAN controller's identifier
CAN_IDMASK	0x0040	W	0x00000000	Identification code bit mask register
CAN_TXFRAMEINFO	0x0050	W	0x00000000	TX frame information configuration register
CAN_TXID	0x0054	W	0x00000000	CAN controller transmit ID
CAN_TXDATA0	0x0058	W	0x00000000	CAN controller transmit DATA1
CAN_TXDATA1	0x005c	W	0x00000000	CAN controller transmit DATA1

Name	Offset	Size	Reset Value	Description
CAN_RXFRAMEINFO	0x0060	W	0x00000000	RX frame information register.This register needs to be read(clear) before receiving the next frame.
CAN_RXID	0x0064	W	0x00000000	CAN controller receive ID.This register needs to be read(clear) before receiving the next frame.
CAN_RXDATA0	0x0068	W	0x00000000	Receive Data Reg0This register needs to be read(clear) before receiving the next frame.
CAN_RXDATA1	0x006c	W	0x00000000	Receive Data Reg1This register needs to be read(clear) before receiving the next frame.
CAN_RTL_VERSION	0x0070	W	0x00000021	CAN RTL version
CAN_FD_NOMINAL_BITTIMING	0x0100	W	0x00000000	CANFD nominal bit timing configure
CAN_FD_DATA_BITTIMING	0x0104	W	0x00000000	CANFD data bit timing configure
CAN_TRANSMIT_DELAY_COMPENSATION	0x0108	W	0x00000000	transmitter delay compensation configure
CAN_TIMESTAMP_CTRL	0x010c	W	0x00000000	timestamp counter configure
CAN_TIMESTAMP	0x0110	W	0x00000000	timestamp counter
CAN_TXEVENT_FIFO_CTRL	0x0114	W	0x00000000	tx event fifo configure
CAN_RX_FIFO_CTRL	0x0118	W	0x00000000	rx fifo configure
CAN_AFR_CTRL	0x011c	W	0x00000000	Acceptance filter register control
CAN_IDCODE0	0x0120	W	0x00000000	CAN controller's identifier
CAN_IDMASK0	0x0124	W	0x00000000	Identification code bit mask register
CAN_IDCODE1	0x0128	W	0x00000000	CAN controller's identifier
CAN_IDMASK1	0x012c	W	0x00000000	Identification code bit mask register
CAN_IDCODE2	0x0130	W	0x00000000	CAN controller's identifier
CAN_IDMASK2	0x0134	W	0x00000000	Identification code bit mask register
CAN_IDCODE3	0x0138	W	0x00000000	CAN controller's identifier
CAN_IDMASK3	0x013c	W	0x00000000	Identification code bit mask register
CAN_IDCODE4	0x0140	W	0x00000000	CAN controller's identifier
CAN_IDMASK4	0x0144	W	0x00000000	Identification code bit mask register
CAN_FD_TXFRAMEINFO	0x0200	W	0x00000000	CANFD TX frame information configuration register
CAN_FD_TXID	0x0204	W	0x00000000	CAN controller transmit ID

Name	Offset	Size	Reset Value	Description
CAN_FD_TXDATA0	0x0208	W	0x00000000	CANFD controller transmit DATA0
CAN_FD_TXDATA1	0x020c	W	0x00000000	CAN controller transmit DATA1
CAN_FD_TXDATA2	0x0210	W	0x00000000	CAN controller transmit DATA2
CAN_FD_TXDATA3	0x0214	W	0x00000000	CAN controller transmit DATA3
CAN_FD_TXDATA4	0x0218	W	0x00000000	CAN controller transmit DATA4
CAN_FD_TXDATA5	0x021c	W	0x00000000	CAN controller transmit DATA5
CAN_FD_TXDATA6	0x0220	W	0x00000000	CAN controller transmit DATA6
CAN_FD_TXDATA7	0x0224	W	0x00000000	CAN controller transmit DATA7
CAN_FD_TXDATA8	0x0228	W	0x00000000	CAN controller transmit DATA8
CAN_FD_TXDATA9	0x022c	W	0x00000000	CAN controller transmit DATA9
CAN_FD_TXDATA10	0x0230	W	0x00000000	CAN controller transmit DATA10
CAN_FD_TXDATA11	0x0234	W	0x00000000	CAN controller transmit DATA11
CAN_FD_TXDATA12	0x0238	W	0x00000000	CAN controller transmit DATA12
CAN_FD_TXDATA13	0x023c	W	0x00000000	CAN controller transmit DATA13
CAN_FD_TXDATA14	0x0240	W	0x00000000	CAN controller transmit DATA14
CAN_FD_TXDATA15	0x0244	W	0x00000000	CAN controller transmit DATA15
CAN_FD_RXFRAMEINFO	0x0300	W	0x00000000	CANFD RX frame information configuration register
CAN_FD_RXID	0x0304	W	0x00000000	CAN controller receive ID
CAN_FD_RXTIMESTAMP	0x0308	W	0x00000000	CAN controller receive timestamp
CAN_FD_RXDATA0	0x030c	W	0x00000000	Receive Data Reg0.This register refresh after receiving the next frame.
CAN_FD_RXDATA1	0x0310	W	0x00000000	Receive Data Reg1.This register refresh after receiving the next frame.
CAN_FD_RXDATA2	0x0314	W	0x00000000	Receive Data Reg2This register refresh after receiving the next frame.
CAN_FD_RXDATA3	0x0318	W	0x00000000	Receive Data Reg3This register refresh after receiving the next frame.
CAN_FD_RXDATA4	0x031c	W	0x00000000	Receive Data Reg4This register refresh after receiving the next frame.
CAN_FD_RXDATA5	0x0320	W	0x00000000	Receive Data Reg5This register refresh after receiving the next frame.
CAN_FD_RXDATA6	0x0324	W	0x00000000	Receive Data Reg6This register refresh after receiving the next frame.

Name	Offset	Size	Reset Value	Description
CAN_FD_RXDATA7	0x0328	W	0x00000000	Receive Data Reg7This register refresh after receiving the next frame.
CAN_FD_RXDATA8	0x032c	W	0x00000000	Receive Data Reg8This register refresh after receiving the next frame.
CAN_FD_RXDATA9	0x0330	W	0x00000000	Receive Data Reg9This register refresh after receiving the next frame.
CAN_FD_RXDATA10	0x0334	W	0x00000000	Receive Data Reg10This register refresh after receiving the next frame.
CAN_FD_RXDATA11	0x0338	W	0x00000000	Receive Data Reg11This register refresh after receiving the next frame.
CAN_FD_RXDATA12	0x033c	W	0x00000000	Receive Data Reg12This register refresh after receiving the next frame.
CAN_FD_RXDATA13	0x0340	W	0x00000000	Receive Data Reg13This register refresh after receiving the next frame.
CAN_FD_RXDATA14	0x0344	W	0x00000000	Receive Data Reg14This register refresh after receiving the next frame.
CAN_FD_RXDATA15	0x0348	W	0x00000000	Receive Data Reg15This register refresh after receiving the next frame.
CAN_RX_FIFO_RDATA	0x0400	W	0x00000000	This register gives the value read from rx fifo
CAN_TXE_FIFO_RDATA	0x0500	W	0x00000000	This register gives the value read from tx event fifo

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

24.3.3 Detail Register Description

CAN_MODE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	CAN_FD_mode_enable CAN FD Mode ENABLE. 1'b0 : Disable. 1'b1 : Enable.

Bit	Attr	Reset Value	Description
14	RW	0x0	DPEE Disable Protocol Exception Event Detection/Generation. 1'b0: PEE detection/generation is enabled. If the CAN FD receiver detects the res bit as 1, it goes to Bus Integration state (PEE_config) and waits for Bus Idle condition (11 consecutive nominal recessive bits). The error counter remains unchanged. 1'b1: Disable Protocol Exception Event detection/generation by CAN FD receiver if "res" bit in CAN FD frame is detected as 1. In this case, CAN FD receiver generates Form error.
13	RW	0x0	BRSD CAN FD Bit Rate Switch Disable Override. 1'b0: Makes the core transmit CAN FD frames as per BRS bit in the TX Message element. 1'b1: Makes the core transmit CAN FD frames only in nominal bit rate (by overriding the TX Message element BRS bit setting).
12	RW	0x0	space_rx_mode Interframe Spaceing RX Mode. 1'b0 : Enable. 1'b1 : Disable.
11	RW	0x0	auto_bus_on Auto Bus On Enable. 1'b0 : After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0. 1'b1 : Automatic reset TEC/REC to bus_on after 128 occurrence of 11 consecutive recessive bits have been monitored on the bus.
10	RW	0x0	auto_retx_mode Auto Retransmission Mode. 1'b0 : Disable. RKCAN return to idle state after transmit DATA/RTR frame failed, and set tx_req to 0. 1'b1 : Enable. The RKCAN automatically retransmit frames which have lost arbitration or have been disturbed by errors during transmission.
9	RW	0x0	ovld_mode Overload Mode. 1'b0: overload lite mode. 1'b1: overload extended mode. RKCAN
8	RW	0x0	cover_mode Rx Data Cover Mode. 1'b0 : RKCAN can't receive new frame before receive registers cleared. 1'b1 : RKCAN can receive new frame before receive registers cleared, and new rxdata will cover old rxdata.

Bit	Attr	Reset Value	Description
7	RW	0x0	rxsort_mode RX Data Sort Mode. 1'b0: The data received first is placed in the lower address. 1'b1: The data received first moves to the upper address, and the data received later is placed at the lower addrsss.
6	RW	0x0	txorder_mode TX Data Order Mode. 1'b0: tx_data1[7:0] --> tx_data1[15:8] --> tx_data1[23:16] --> tx_data1[31:24] -->tx_data2[7:0] --> tx_data2[15:8] --> tx_data2[23:16] --> tx_data2[31:24]. 1'b1: tx_data2[31:0] --> tx_data1[31:0].
5	RW	0x0	rxstx_mode Receive Self Transmit data mode. 1'b0: Disable; 1'b1: Enable. When the RKCAN sends data, it can also receive the data sent by itself.
4	RW	0x0	lback_mode Loopback Mode. 1'b0: Disable. 1'b1: Enable.
3	RW	0x0	silent_mode Silent Mode. 1'b0: Disable. 1'b1: Enable.
2	RW	0x0	self_test Self check ACK slot when TX frame. 1'b0: Normal 1'b1: Self test mode. When in self test mode, the receiver does not need to return an ACK signal when receiving data. Therefore, no ack_error will occur in self test mode. When in 'lback_mode' or 'silent_mode', it need to enable 'self_test' mode when sending frame.
1	RW	0x0	sleep_mode Sleep Mode This is the Sleep mode request bit. 1'b0: No such request. 1'b1: Request core to be in Sleep mode. This bit is cleared when the core wakes up from Sleep mode.
0	RW	0x0	work_mode Work Mode. 1'b0: Reset mode, CAN stop transmit and registers can be configured. 1'b1: Work mode, CAN enter the working mode, RX/TX data.

CAN_CMD

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	R/W SC	0x0	tx1_req Transmit request enable 1'b0: Disable; 1'b1: Enable. When 'tx_req' is enable, the RKCAN buffer1 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer1 transmission frame complete, 'tx_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.
0	R/W SC	0x0	tx0_req Transmit request enable 1'b0: Disable; 1'b1: Enable. When 'tx_req' is enable, the RKCAN buffer0 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer0 transmission frame complete, 'tx_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.

CAN_STATE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RO	0x0	sleep_state sleep_state 1'b0: None 1'b1: CAN controller is in the sleep state
5	RO	0x0	bus_off_state 1'b0: None 1'b1: Bus off state: When the error counter is incremented to 255, the CAN controller will enter the bus off state, generate an error warning interrupt and enter reset mode, waiting for the CPU to restart. (rx/tx_err_cnt >=32'd255)
4	RO	0x0	error_warning_state 1'b0: None 1'b1: Error state: At least one error counter has reached the error warning threshold (rx/tx_err_cnt >=32'd96)
3	RO	0x0	tx_period 1'b0: Not in transmiting state 1'b1: CAN controller is in the transmiting state
2	RO	0x0	rx_period 1'b0: Not in receiving state 1'b1: CAN controller is in the receiving state

Bit	Attr	Reset Value	Description
1	RO	0x0	tx_buffer_full Transmit buffer full flag bit 1'b0: Not full 1'b1: TX buffer is full. There is data in buffer waiting to be sent or being sent.
0	RO	0x0	rx_buffer_full Receive buffer full flag bit 1'b0: Not full 1'b1: RX buffer is full. A complete message is stored in the buffer.

CAN_INT

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	wakeup_int 1'b0: None 1'b1: Indicates that the core entered Normal mode from Sleep mode. Write 1 then clear.
13	W1C	0x0	tx_event_fifo_full_int 0 = None 1 = Indicates that TX Event FIFO is full based on watermark programming. The interrupt continues to assert as long as the TX Event FIFO Fill Level is above TX Event FIFO Full watermark.
12	W1C	0x0	tx_event_fifo_overflow_int 0 = None 1 = Indicates that a message has been lost. This condition occurs when the core has successfully transmitted a message for which an event store is requested but the TX Event FIFO is full.
11	W1C	0x0	timestamp_counter_overflow_int 1'b0: None 1'b1: 1 = Indicates that Timestamp counter rolled over (from 0xffff to 0x0). Write 1 then clear.
10	W1C	0x0	bus_off_recovery_int 1'b0: None 1'b1: Indicates that the core recoveryed from Bus-off mode. Write 1 then clear.
9	W1C	0x0	bus_off_int 1'b0: None 1'b1: Indicates that the CAN core entered Bus-off mode. Write 1 then clear.

Bit	Attr	Reset Value	Description
8	W1C	0x0	rx_fifo_overflow_int RX FIFO Overflow Interrupt (RX FIFO ENABLE). 0 = None 1 = Indicates that a message has been lost. This condition occurs when a new message with ID matching to Receive FIFO is received and the Receive FIFO is full.
7	W1C	0x0	rx_fifo_full_int RX FIFO full Interrupt (FIFO Mode enable). 1'b0: None 1'b1: Indicates that RX FIFO is full based on watermark setting.
6	W1C	0x0	error_int 1'b0: None 1'b1: CAN bus error interrupt. This interrupt is generated when a bus error is detected. Error details can refer to the ERROR_CODE register. Write 1 then clear.
5	W1C	0x0	tx_arbit_fail_int 1'b0: None 1'b1: Arbitration loss interrupt. This interrupt is generated when the loss of arbitration is turned into a receiver. Write 1 then clear.
4	W1C	0x0	passive_error_int 1'b0: None 1'b1: Passive error interrput. This interrupt is generated when the controller enters an error passive state (at least one error counter reaches 127) or returns from the error passive state to the error active state. Write 1 then clear.
3	W1C	0x0	overload_int 1'b0: None 1'b1: CAN bus overload interrupt. This interrupt is generated when a overload frame is generated.
2	W1C	0x0	error_warning_int Error warning interrupt 1'b0: None 1'b1: error_warning_int. This interrupt is generated when the error_warning_state bits change. Write 1 then clear.
1	W1C	0x0	tx_finish_int Transmit finish interrupt 1'b0: None 1'b1: tx_finish_int. CAN controller sends the message and the buffer is empty. Write 1 then clear.
0	W1C	0x0	rx_finish_int Receive finish interrupt 1'b0: None 1'b1: RX finish int. CAN controller has received the message and the rx_buffer is full. Write 1 then clear.

CAN_INT_MASK

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	wakeup_int_mask 1'b0: Unmasked 1'b1: Masked
13	RW	0x0	tx_event_fifo_full_int_mask 1'b0: Unmasked 1'b1: Masked
12	RW	0x0	tx_event_fifo_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
11	RW	0x0	timestamp_counter_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
10	RW	0x0	bus_off_recovery_int_mask 1'b0: Unmasked 1'b1: Masked
9	RW	0x0	bus_off_int_mask 1'b0: Unmasked 1'b1: Masked
8	RW	0x0	rx_fifo_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
7	RW	0x0	rx_fifo_full_int_mask 1'b0: Unmasked 1'b1: Masked
6	RW	0x0	error_int_mask 1'b0: Unmasked 1'b1: Masked
5	RW	0x0	tx_arbit_fail_int_mask 1'b0: Unmasked 1'b1: Masked
4	RW	0x0	passive_error_int_mask 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	rx_buffer_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	error_warning_int_mask 1'b0: Unmasked 1'b1: Masked

Bit	Attr	Reset Value	Description
1	RW	0x0	tx_finish_int_mask 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	rx_finish_int_mask 1'b0: Unmasked 1'b1: Masked

CAN_DMA_CTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	dma_rx_mode DMA receive request enable 1'b0: Disable; 1'b1: Enable. When 'DMA_rx_req' is enable, the RKCAN is in the DMA receive mode. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is clear.
0	RW	0x0	dma_tx_mode DMA Transmit request enable 1'b0: Disable; 1'b1: Enable. When 'DMA_tx_req' is enable, the RKCAN is in the DMA transmit mode. When RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.

CAN_BITTIMING

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	sample_mode CAN controller sampling mode configuration register. 1'b0: Single sample mode 11'b1: Three sample mode 推荐使用single sample mode.
15:14	RW	0x0	sjw SJW: reSynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
13:8	RW	0x00	brp brp: system prescaler coefficient Tsclk = 2 x Tclk x (brp + 1).
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
3:0	RW	0x0	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

CAN_ARBITFAIL

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RO	0x00	arbit_fail_code This register indicates the bit position of arbitration section where the arbitration was lost.

CAN_ERROR_CODE

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	error_phase 0: Arbitration Phase 1: Data Phase
28:26	RO	0x0	error_type Error type: 3'b000: BIT ERROR 3'b001: BIT STUFF ERROR 3'b010: FORM ERROR 3'b011: ACK ERROR 3'b100: CRC ERROR
25	RO	0x0	error_direction 1'b0: TX error 1'b1: RX error
24:16	RW	0x000	tx_error_position Indicate transmit error position. 9'b000000001 : TRANSMIT_IDLE. 9'b000000010 : TRANSMIT_SOF_DLC. 9'b000000100 : TRANSMIT_DATA. 9'b000001000 : TRANSMIT_STUFF_COUNT. 9'b000010000 : TRANSMIT_CRC. 9'b000100000 : TRANSMIT_ACK_EOF. 9'b001000000 : TRANSMIT_ACK. 9'b010000000 : TRANSMIT_ERROR. 9'b100000000 : TRANSMIT_OVERLOAD.

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	rx_error_position Indicate receive error position 16'b0000000000000001: RECEIVE_IDLE 16'b0000000000000010: RECEIVE_SOF_IDE 16'b0000000000000100: RECEIVE_ID2_RTR 16'b0000000000001000: RECEIVE_FDF 16'b0000000000010000: RECEIVE_RES 16'b0000000000100000: RECEIVE_BRS_ESI 16'b0000000001000000: RECEIVE_DLC 16'b0000000010000000: RECEIVE_DATA 16'b0000000100000000: RECEIVE_STUFF_COUNT 16'b0000001000000000: RECEIVE_CRC 16'b0000010000000000: RECEIVE_CRC_LIM 16'b0000100000000000: RECEIVE_ACK 16'b0001000000000000: RECEIVE_ACK_LIM 16'b0010000000000000: RECEIVE_EOF 16'b0100000000000000: RECEIVE_SPACE 16'b1000000000000000: RECEIVE_BUF_INT

CAN_RXERRORCNT

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	rx_err_cnt Receive Error Counter(REC). Actual state of the Receive Error Counter. Value between 0 and 127.

CAN_TXERRORCNT

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RO	0x000	tx_err_cnt Transmit Error Counter(TEC). Actual state of the Transmit Error Counter. Value between 0 and 255.

CAN_IDCODE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_TXFRAMEINFO

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5:4	RO	0x0	reserved
3:0	RW	0x0	txdata_length Transmit data length configure register.(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte others: reserved

CAN_TXID

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

CAN_TXDATA0

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0

CAN_TXDATA1

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1

CAN_RXFRAMEINFO

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RC	0x0	rxframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RC	0x0	rx_rtr 1'b0: Data frame 1'b1: Remote frame
5:4	RO	0x0	reserved
3:0	RC	0x0	rxdata_length Receive data length register.(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte others: reserved

CAN_RXID

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RC	0x00000000	rx_id rx_id[28:0]

CAN_RXDATA0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RC	0x00000000	rx_data0 rx_data0[31:0]

CAN_RXDATA1

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RC	0x00000000	rx_data1 rx_data1[31:0]

CAN_RTL_VERSION

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000021	version CAN rtl version = 32'h22

CAN_FD_NOMINAL_BITTIMING

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	sample_mode CAN controller sampling mode configuration register. 1'b0: Single sample mode 1'b1: Three sample mode
30:24	RW	0x00	sjw SJW: reSynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
23:16	RW	0x00	brq brp: system prescaler coefficient Tsclk = 2 x Tclk x (brp + 1).
15	RO	0x0	reserved
14:8	RW	0x00	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
7:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

CAN_FD_DATA_BITTIMING

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	sample_mode CAN controller sampling mode configuration register. 1'b0: Single sample mode 1'b1: Three sample mode
20:17	RW	0x0	sjw SJW: reSynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
16:9	RW	0x00	brq brp: system prescaler coefficient Tsclk = 2 x Tclk x (brp + 1).
8:5	RW	0x0	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)
4:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

CAN_TRANSMIT_DELAY_COMPENSATION

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:1	RW	0x00	tdc_offset Transmitter Delay Compensation Offset This offset is specified in CAN clock cycles and is added to the measured transmitter delay to place the Secondary Sample Point (SSP) at appropriate position (for example, set this to half data bit time in terms of CAN clock cycles to place SSP in the middle of the data bit).
0	RW	0x0	tdc_enable Transmitter Delay Compensation (TDC) Enable 1 = Enables TDC function as specified in the CAN FD standard. 0 = TDC is disabled.

CAN_TIMESTAMP_CTRL

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:1	RW	0x00	time_base_counter_prescale Time Base Counter Prescaler bit 0 = TBC increments every 1 clock 1 = TBC increments every 2 clock ... 31 = TBC increments every 32 clock
0	RW	0x0	time_base_counter_enable Time Base Counter (TBC) Enable 1 = Enables TBC 0 = Disable and reset TBC

CAN_TIMESTAMP

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	time_base_counter This Status field gives running value of the timestamp counter.

CAN_TXEVENT_FIFO_CTRL

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:5	RW	0x0	TXE_FIFO_CNT TXE_FIFO_FRAME_CNT This field represents number of frame in TXE FIFO
4:1	RW	0x0	TXE_FIFO_WATERMARK TX Event FIFO generates FULL interrupt based on the value programmed in this field. Set it within (1-15) range. The TX FIFO Full Watermark interrupt in the ISR register continues to assert as long as the TX Event FIFO Fill Level is above TX Event FIFO Full watermark.
0	RW	0x0	TXE_FIFO_ENABLE transmit event fifo enable 0: disable 1: enable

CAN_RX_FIFO_CTRL

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:4	RO	0x0	rx_fifo_cnt RX_FIFO_FRAME_CNT This field represents number of frame in Rx FIFO

Bit	Attr	Reset Value	Description
3:1	RW	0x0	rx_fifo_full_watermark RX FIFO Full Watermark. RX FIFO generates FULL interrupt based on the value programmed in this field. Set it within (1-5) range. The RX FIFO Full Watermark interrupt in the ISR register continues to assert as long as the RX FIFO-0 Fill Level is above RX FIFO Full watermark. This field can be written to only when CEN bit in SRR is 0.
0	RW	0x0	rx_fifo_enable receive fifo enable bit 0: disable 1: enable

CAN_AFR_CTRL

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	UAF5 enable the use of acceptance filter pair 5 0: disable 1: enable
3	RW	0x0	UAF4 enable the use of acceptance filter pair 4 0: disable 1: enable
2	RW	0x0	UAF3 enable the use of acceptance filter pair 3 0: disable 1: enable
1	RW	0x0	UAF2 enable the use of acceptance filter pair 2 0: disable 1: enable
0	RW	0x0	UAF1 enable the use of acceptance filter pair 1 0: disable 1: enable

CAN_IDCODE0

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK0

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_IDCODE1

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK1

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_IDCODE2

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK2

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_IDCODE3

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK3

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_IDCODE4

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_code CAN controller ID code: Standard frame ID: id_code[10:0]; Extended frame ID: id_code[28:0].

CAN_IDMASK4

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	id_mask [0]: Unmasked [1]: Masked

CAN_FD_TXFRAMEINFO

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RW	0x0	tx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CAN FD format frames. 1 = CAN FD format frame. 0 = CAN format frame.
4	RW	0x0	tx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1 = Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. 0 = Bit rate is not switched inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set to 0.
3:0	RW	0x0	txdata_length Transmit data length configure register.(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

CAN_FD_TXID

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

CAN_FD_TXDATA0

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0

CAN_FD_TXDATA1

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1

CAN_FD_TXDATA2

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data2 tx_data2

CAN_FD_TXDATA3

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data3 tx_data3

CAN_FD_TXDATA4

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data4 tx_data4

CAN_FD_TXDATA5

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data5 tx_data5

CAN_FD_TXDATA6

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data6 tx_data6

CAN_FD_TXDATA7

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data7 tx_data7

CAN_FD_TXDATA8

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data8 tx_data8

CAN_FD_TXDATA9

Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data9 tx_data9

CAN_FD_TXDATA10

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data10 tx_data10

CAN_FD_TXDATA11

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data11 tx_data11

CAN_FD_TXDATA12

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data12 tx_data12

CAN_FD_TXDATA13

Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data13 tx_data13

CAN_FD_TXDATA14

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data14 tx_data14

CAN_FD_TXDATA15

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data15 tx_data15

CAN_FD_RXFRAMEINFO

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	rxframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	rx_rtr 1'b0: Data frame 1'b1: Remote frame
5	RW	0x0	rx_fdf Extended Data Length/FD Frame Format This bit distinguishes between CAN format and CAN FD format frames. 1 = CAN FD format frame. 0 = CAN format frame. to 0.
4	RW	0x0	rx_brs Bit Rate Switch The BRS bit decides whether the bit rate is switched inside a CAN FD format frame or not (provided BRSD bit is not set in MSR register). 1 = Bit rate is switched from the standard bit rate of the Arbitration phase to the preconfigured alternate bit rate of the Data phase inside a CAN FD frame. 0 = Bit rate is not switched inside a CAN FD frame. Note: BRS does not exist in CAN format frames and should be set

Bit	Attr	Reset Value	Description
3:0	RW	0x0	rxdata_length Transmit data length configure register.(unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

CAN_FD_RXID

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	rx_id can_rx_id[28:0]

CAN_FD_RXTIMESTAMP

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timestamp rx_timestamp

CAN_FD_RXDATA0

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data0 rx_data0[31:0]

CAN_FD_RXDATA1

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data1 rx_data1[31:0]

CAN_FD_RXDATA2

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data2 rx_data2[31:0]

CAN_FD_RXDATA3

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data3 rx_data3[31:0]

CAN_FD_RXDATA4

Address: Operational Base + offset (0x031c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data4 rx_data4[31:0]

CAN_FD_RXDATA5

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data5 rx_data5[31:0]

CAN_FD_RXDATA6

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data6 rx_data6[31:0]

CAN_FD_RXDATA7

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data7 rx_data7[31:0]

CAN_FD_RXDATA8

Address: Operational Base + offset (0x032c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data8 rx_data8[31:0]

CAN_FD_RXDATA9

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data9 rx_data9[31:0]

CAN_FD_RXDATA10

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data10 rx_data10[31:0]

CAN_FD_RXDATA11

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data11 rx_data11[31:0]

CAN_FD_RXDATA12

Address: Operational Base + offset (0x033c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data12 rx_data12[31:0]

CAN_FD_RXDATA13

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data13 rx_data13[31:0]

CAN_FD_RXDATA14

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data14 rx_data14[31:0]

CAN_FD_RXDATA15

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data15 rx_data15[31:0]

CAN_RX_FIFO_RDATA

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_fifo_rdata rx fifo read data value

CAN_TXE_FIFO_RDATA

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	txe_fifo_rdata tx event fifo read data value

24.4 Interface Description

Table 24-3 CAN Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
CAN0mux0 Interface			
can0_rx	I	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	PMUGRF_GPIO0B_IOMUX_SEL_H[3:0]=4'h2
can0_tx	O	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B3_u	PMUGRF_GPIO0B_IOMUX_SEL_L[15:12]=4'h2
CAN0mux1 Interface			
can0_rx	I	SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1/GPIO2_A2_d	GRF_GPIO2A_IOMUX_SEL_L[11:8]=4'h4
can0_tx	O	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	GRF_GPIO2A_IOMUX_SEL_L[7:4]=4'h4
CAN1mux0 Interface			
can1_rx	I	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	GRF_GPIO1A_IOMUX_SEL_L[3:0]=4'h2
can1_tx	O	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	PMUGRF_GPIO1A_IOMUX_SEL_L[7:4]=4'h2
CAN1mux1 Interface			
can1_rx	I	PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	GRF_GPIO4C_IOMUX_SEL_L[11:8]=4'h4
can1_tx	O	PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	GRF_GPIO4C_IOMUX_SEL_L[15:12]=4'h4
CAN2mux0 Interface			
can2_rx	I	I2C2_SDA_M1/EBC_GDSP/CAN2_RX_M0/ISP_FLASH_TRIGIN/VOP_BT656_CLK_M1/GPIO4_B4_d	PMUGRF_GPIO4B_IOMUX_SEL_H[3:0]=4'h3
can2_tx	O	I2C2_SCL_M1/EBC_SDSHR/CAN2_TX_M0/I2S1_SDO3_M1/GPIO4_B5_d	PMUGRF_GPIO4B_IOMUX_SEL_H[7:4]=4'h3
CAN2mux1 Interface			
can2_rx	I	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	GRF_GPIO2B_IOMUX_SEL_L[7:4]=4'h4
can2_tx	O	SDMMC1_DET/I2C4_SCL_M1/UART8_CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	GRF_GPIO2B_IOMUX_SEL_L[11:8]=4'h4

24.5 Application Notes

24.5.1 Controller initialization flow

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

After the initialization is completed, the controller enters the working mode, sends the frame to be sent to the buffer, and then sets the "send request" flag of the command register to start transmitting.

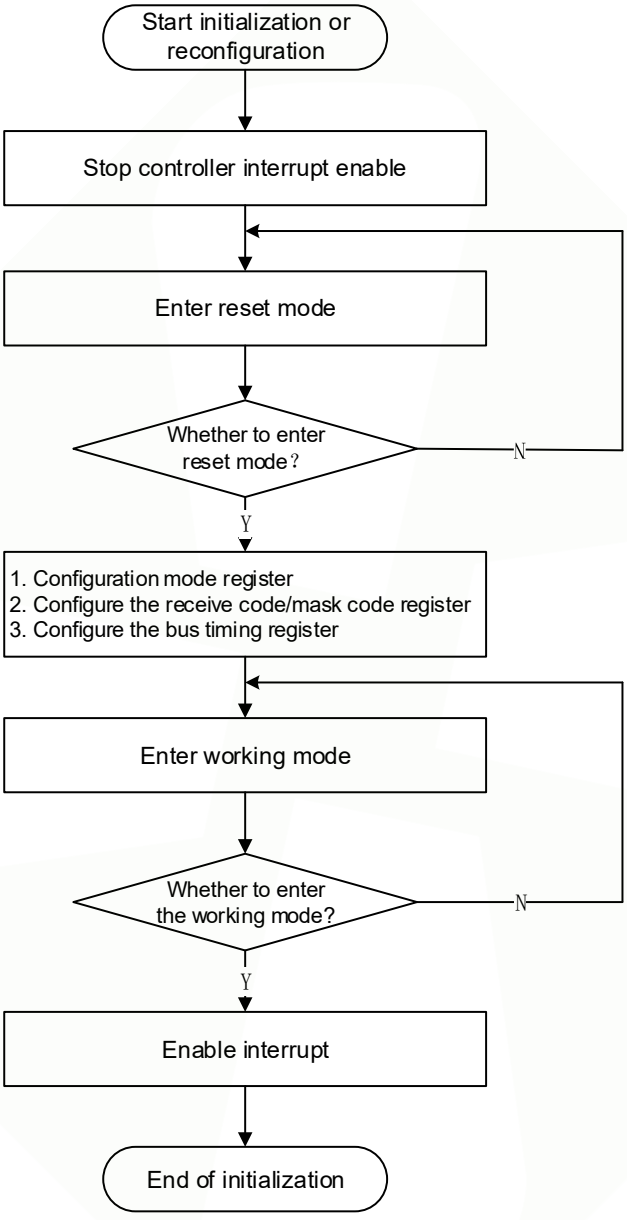


Fig.24-11 CANFD Initialization Flow

24.5.2 Loop-back Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

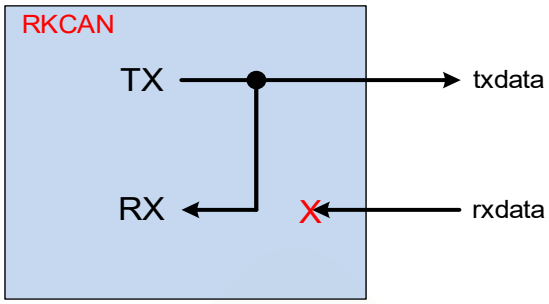


Fig.24-12 Loopback Mode

24.5.3 Silent Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

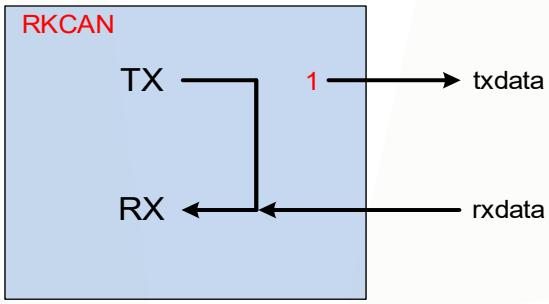


Fig.24-13 Silent Mode

24.5.4 RXSTX Mode

(1)rxstx_mode=0, RKCAN cannot receive the data sent by itself;
(2)rxstx_mode=1, RKCAN can receive the data sent by itself, and when the ID of the frame is the same as the ID_CODE of RKCAN itself, RKCAN will store the frame information into CAN_RXDATA1/2.

24.5.5 TXORDER Mode

The TXORDER Mode is used to determine the order in which data is sent.
(1)txorder_mode=0, Data transmission order is "tx_data1[7:0] --> tx_data1[15:8] --> tx_data1[23:16] --> tx_data1[31:24] -->tx_data2[7:0] --> tx_data2[15:8] --> tx_data2[23:16] --> tx_data2[31:24]";
(2)txorder_mode=1, Data transmission order is "tx_data2[31:0] --> tx_data1[31:0]".

24.5.6 RXSORT Mode

The TXSORT Mode is used to determine how the received data is stoted.
(1)rxsort_mode=0: The data received first is placed in the lower address;
(2)rxsort_mode=1: The data received first moves to the upper address, and the data received later is placed at the lower addrsss.

24.5.7 COVER Mode

(1)cover_mode=1'b0 : RKCAN can't receive new frame before receive registers cleared.
(2)cover_mode=1'b1 : RKCAN can receive new frame before receive registers cleared, and new rxdata will cover old rxdata.

24.5.8 Overload Mode

According to the CAN protocol, a CAN transceiver will generate an OVERLOAD frame in three cases:

CASE1: When the CAN is used as a receiver, if it is necessary to delay the next frame.

CASE2:Detection of a dominant bit at the first and second bit of Intermission.

CASE3:If an CAN node samples a dominant bit at the eight bit(the last bit) of an ERROR DELIMITER or OVERLOAD DELIMITER.

1’b0:Overload Lite Mode: RKCAN only generates overload frames in the CASE2.

1’b1:Overload Extended Mode: RKCAN can generates overload frames in all three cases.

24.5.9 Auto Retx Mode

Auto Retransmission Mode.

1'b0 : Disable. RKCAN return to idle state after transmit DATA/RTR frame failed, and set tx_req to 0.

1'b1 : Enable. The RKCAN automatically retransmit frames which have lost arbitration or have been disturbed by errors during transmission.

24.5.10 Auto Bus On

Auto Bus On Enable.

1'b0 : After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0.

1'b1 : Automatic reset TEC/REC to bus_on after 128 occurrence of 11 consecutive recessive bits have been monitored on the bus.

24.5.11 Sleep Mode

The core enters Sleep mode from Configuration or Normal mode when the SLEEP bit is 1 in the CAN_MODE register, the CAN bus is idle, and there are no pending transmission requests.

The core enters Configuration mode when any configuration condition is satisfied. The core enters Normal mode (clearing the SLEEP request bit in thesleep register and also clearing the corresponding status bit) under the following (wake-up) conditions:

- Whenever the SLEEP bit is set to 0.
- Whenever the SLEEP bit is 1, and bus activity is detected.
- Whenever there is a new message for transmission.

Interrupts are generated when the core enters Sleep mode or wakes up from Sleep mode.

24.5.12 DMA Support

The CANFD supports DMA signalling with the use of two output signals (dma_tx_req and dma_rx_req) to indicate when transmit buffer is empty or when the receive FIFO is full. The controller uses two DMA channels, one for the transmit data and one for the receive data. DMA transmit and receive support enabled by setting corresponding bit in CAN_DMA_CTRL register. Once enabled whenever both transmit buffer is empty dma_tx_req is set, DMA should write transmit message. At last CPU set transmit request bit to initiate CANFD.

If RX FIFO is disabled, dma_rx_req is set when message received successfully, DMA should read Rdata from receive registers.

If RX FIFO is enabled, dma_rx_req is set when message received and FIFO reached watermark，DMA should read Rdata from Rx FIFO entrance.

24.5.13 CANFD MODE

The CANFD MODE from CAN_MODE register decide the controller internal setting. When it is disabled, it uses the previous can design, which only transmit and receive CAN frame. If CANFD mode enabled, it allows added feature and can transmit/receive both CAN and CANFD frame.

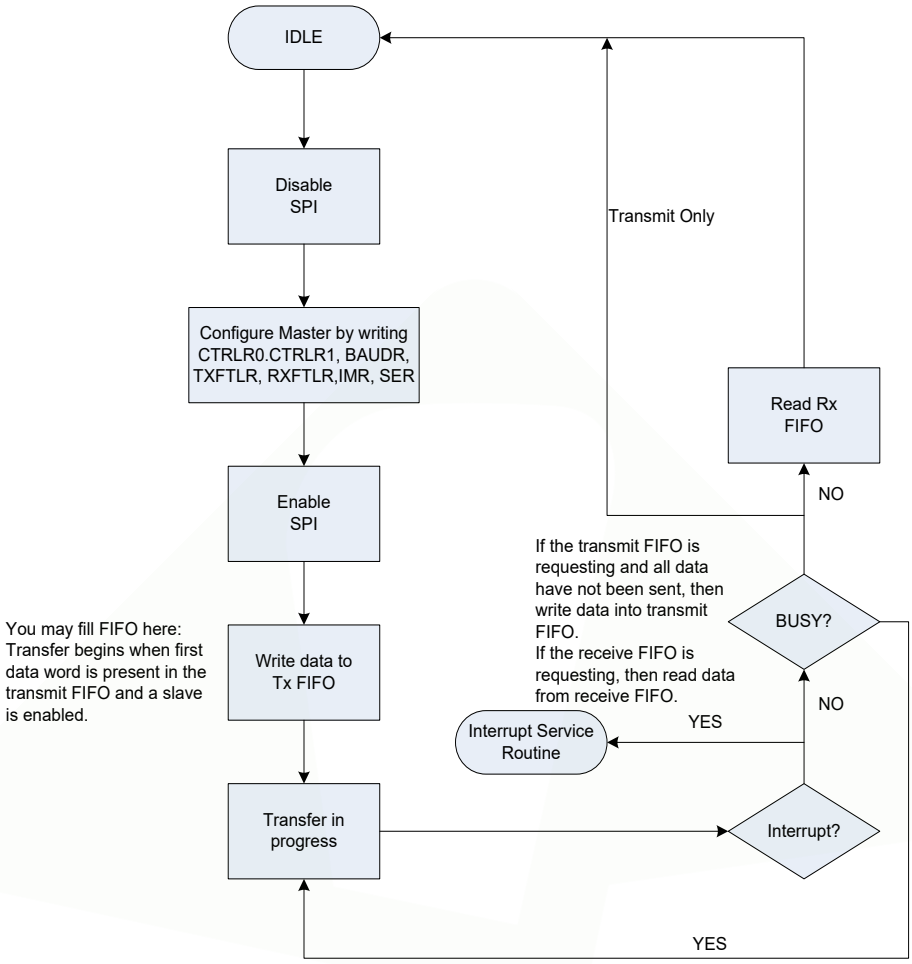


Fig.24-14 SPI Master transfer flow diagram

```
wire        clk_spi0_en          = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con30[11]
wire        pclk_spi1_en         = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con30[12]
wire        clk_spi1_en          = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con30[13]
wire        pclk_spi2_en         = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con30[14]
wire        clk_spi2_en          = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con30[15]
wire        pclk_spi3_en         = soc_test_mode ? 'd0
                                   ) & (~pd_bus_gatemask);      : (cru_gate_con31[0]
wire        clk_spi3_en          = soc_test_mode ? 'd0         : (cru_gate_con31[1]
```

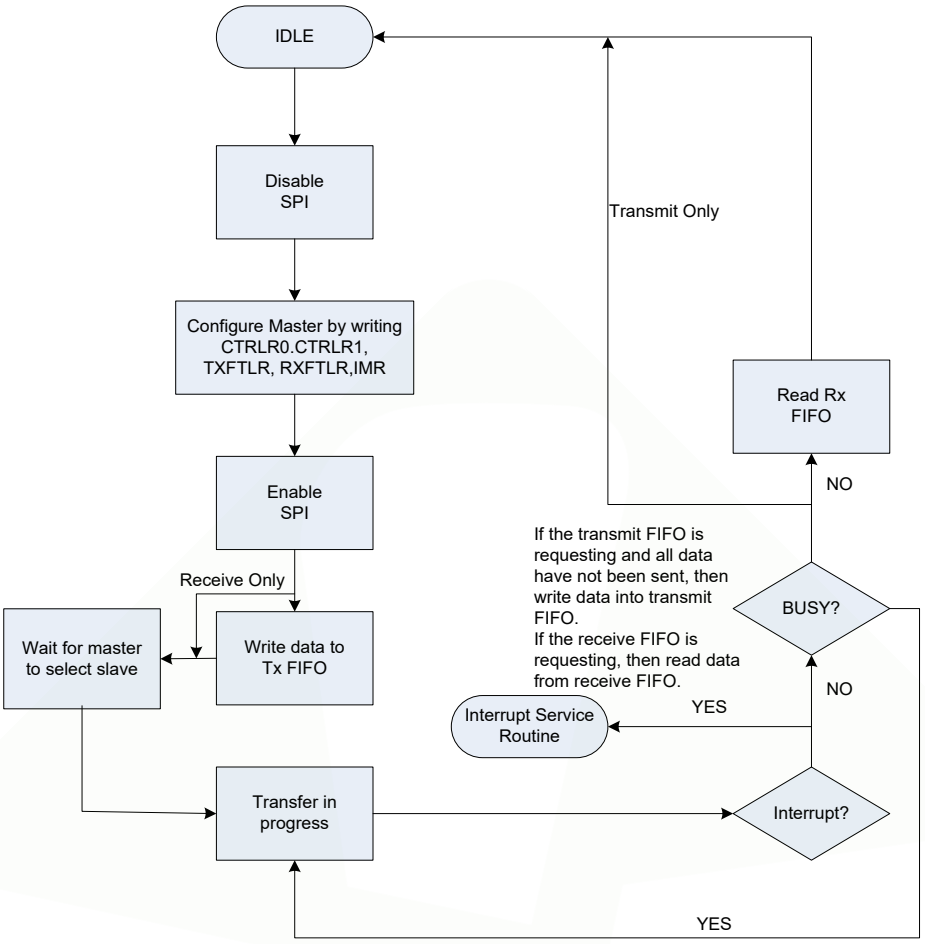


Fig.24-15 SPI Slave transfer flow diagram

Chapter 25 Smart Card Reader (SCR)

25.1 Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the superior system and the Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

SCR supports the following features:

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) specifications
- Performs functions needed for complete smart card sessions, including:
- Card activation and deactivation
- Cold/warm reset
- Answer to Reset (ATR) response reception
- Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
- T=0 for asynchronous half-duplex character transmission
- T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Configurable timing functions:
- Smart card activation time
- Smart card reset time
- Guard time
- Timeout timers
- Automatic operating voltage class selection
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Advanced Peripheral Bus (APB) slave interface for easy integration with AMBA-based host systems Block Diagram

25.2 Block Diagram

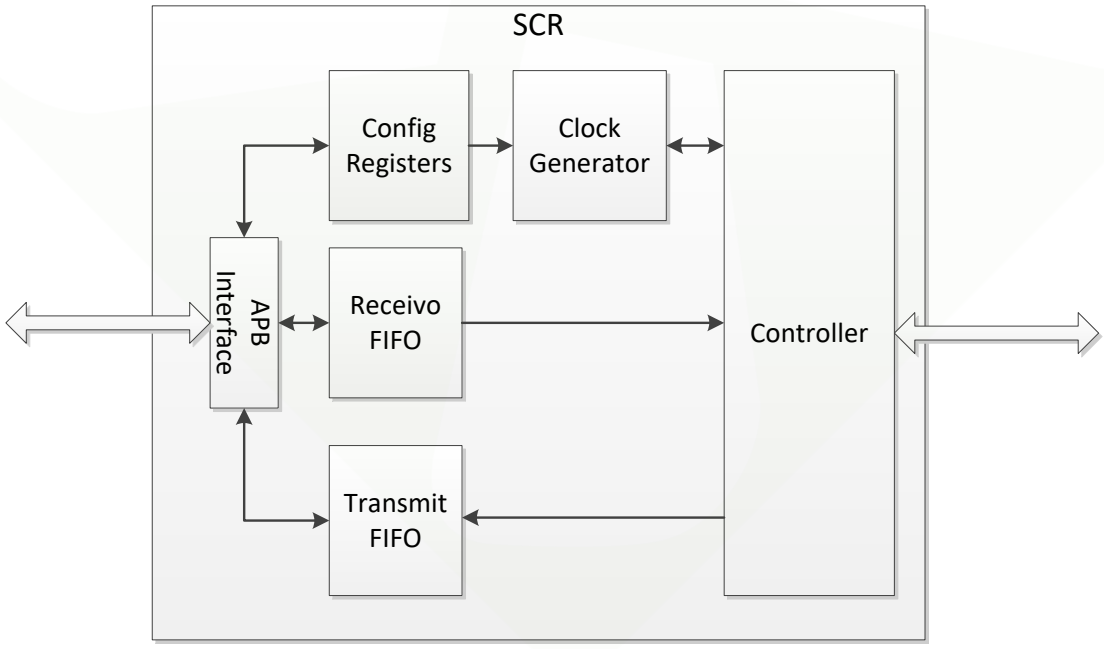


Fig.25-1 SCR Block Diagram

The host processor gets access to PWM Register Block through the APB slave interface.

25.2.1 APB Interface

The host processor gets access to PWM Register Block through the APB slave interface.

25.2.2 Configuration Registers
The Configuration Registers block provides control over all functions of the Smart Card Reader

25.2.3 Controller
The Controller is the main block in the SCR core. This block controls receiving characters transmitted by the Smart Card, storing them in the RX FIFO, and transmitting them to the Smart Card. This block also performs card activation, deactivation, and cold and warm reset. After the card is reset, the Answer To Reset (ATR) sequence is received by the controller and stored in RX FIFO.
The parallel to serial conversion needed to transmit data from a Smart Card Reader to a Smart Card and the serial to parallel conversion needed to transmit data in the opposite direction is performed by the UART. The UART also performs the guard time, parity checking and character repeating functions.

25.2.4 Receive FIFO
The Receive FIFO is used to store the data received from the Smart Card until the data is read out by the superior system.

25.2.5 Transmit FIFO
The Transmit FIFO is used to store the data to be transmitted to the Smart Card.

25.2.6 Clock Generator
The Clock Generator generates the Smart Card Clock signal and the Baud Clock Impulse signal, used in timing the Smart Card Reader.)

25.3 Function Description
A Smart Card session consists of following stages:
- Smart Card insertion
- Activation of contacts and cold reset sequence
- Answer To Reset sequence (ATR)
- Execution of transaction
- Deactivation of contacts
- Smart Card removal

25.3.1 Smart Card Insertion
A Smart Card session starts with the insertion of the Smart Card. This event is signaled to the SCR using the SCDETECT input. The SCPRESENT bit is set and also the SCINS interrupt is asserted (if enabled).
When the external card detect switch is not used, the input pin SCDETECT must be tied to inactive state.

25.3.2 Automatic operating voltage class selection
There are three operating classes (1.8V - class C, 3V - class B and 5V - class A) defined in ISO/IEC 7816-3(2006) specification. Only 1.8V and 3.3V are supported by the SCR.
Before the activation of contacts, operating classes have to be enabled via bits VCC18, VCC33 in CTRL2 register. In case that no operating class is enabled, the controller performs activation for all two voltage classes (1.8V, 3V) in sequence.
When Smart Card Reader performs activation of contacts the lowest enabled voltage class is automatically applied first. When the first character start bit of ATR sequence is received, the selected voltage class is correct (even if the ATR is then received with errors). When the ATR sequence reception does not start, ATRFAIL interrupt is not activated, deactivation is performed and next higher enabled voltage class is applied. If the ATR sequence reception does not start and no other higher class is enabled was already applied the ATRFAIL interrupt is activated and the last applied voltage class remains active.
After the automatic voltage class selection is finished the selected class can be read from bits VCC18, VCC33 in CTRL2 register. If the automatic voltage class selection fails, these bits remain untouched.
There is a delay applied between deactivation of contacts with lower voltage class and activation of contacts with higher voltage class. This delay should be at least 10 ms according to the ISO/IEC 7816-3 specification.

25.3.3 Activation of Contacts and Cold Reset Sequence
When the Smart Card is properly inserted and the ACT bit in CTRL2 register is asserted, the

activation of contacts can be started. The duration of each part of the activation is the time Ta, which is equal to the ADEATIME register value. If no Vpp is necessary, the activation and deactivation part of Vpp can be omitted by clearing the AUTOADEAVPP bit in SCPADS register.
The Cold Reset sequence follows immediately after the activation. Time (Tc) is the duration of the Reset. The EMV specification recommends that this value should be between 40000 and 45000. The activation of contacts and cold reset sequence is shown in Fig.24-2.

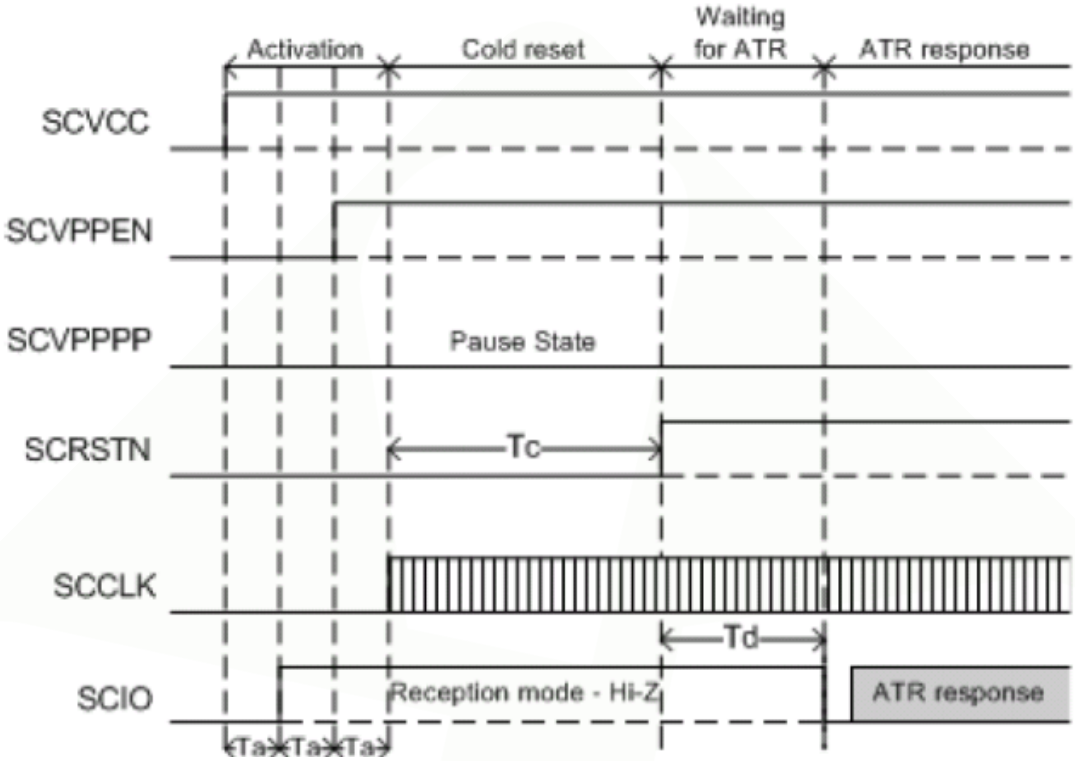


Fig.25-2 Activation, Cold Reset and ATR

25.3.4 Execution of Transaction

All transfers between the Smart Card Reader and a Smart Card are under the control of the superior system. It controls the number of characters sent to the Smart Card and it knows the number of characters expected to be returned from the Smart Card.

25.3.5 Warm Reset

The Warm Reset sequence is initialized by setting the WRST bit in the CTRL2 register to '1'.Smart Card Reader drives the SCRSTN signal to '0' to perform the Warm Reset as shown in Fig. 24-3. After the SCRSTN assertion, the Warm Reset sequence then continues the same way as the Cold Reset sequence.

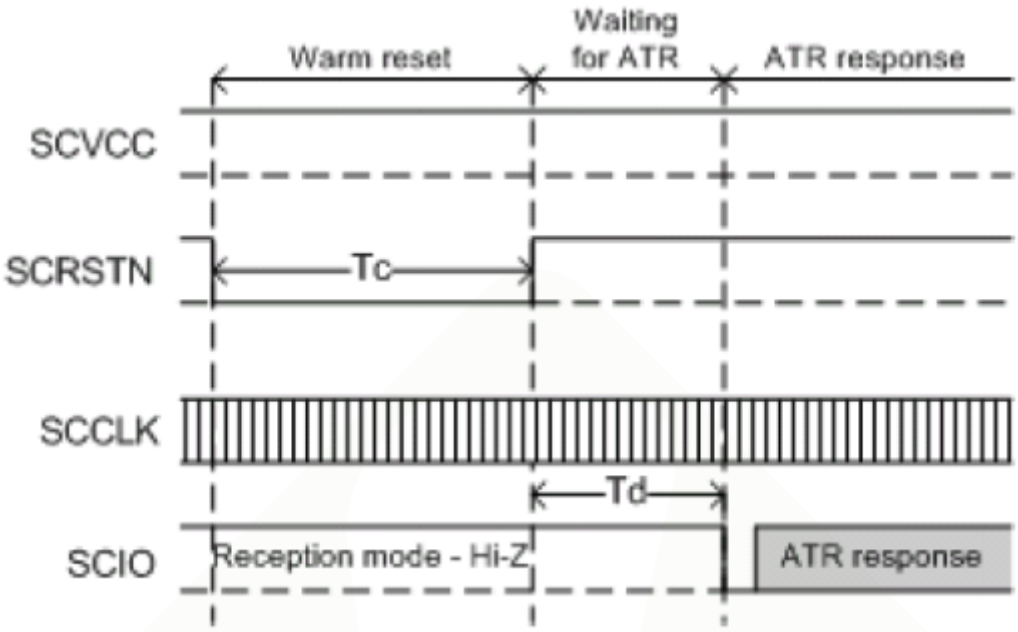


Fig.25-3 Warm Reset and ATR

25.3.6 Deactivation of Contacts

After the smart card reader detects the removal of the smart card (SCREM interrupt) or the superior system initiates deactivation by setting the DEACT bit in the CTRL2 register to '1', the deactivation is performed immediately as shown in . The duration time (Ta), of each part of the deactivation sequence time is defined in the ADEATIME register.

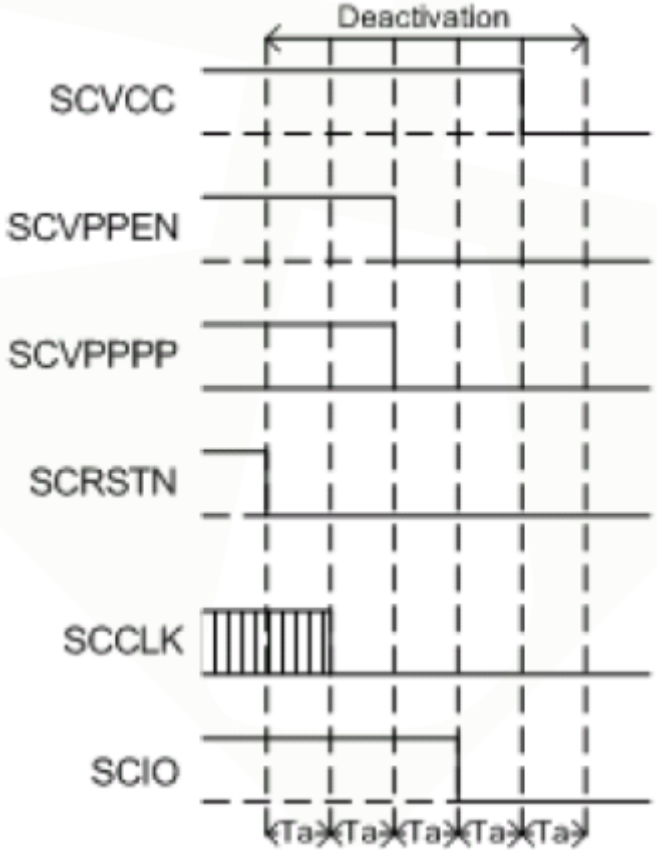


Fig.25-4 Deactivation Sequence

25.4 Register Description

25.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SCR_CTRL1	0x0000	HW	0x00000000	Control Register 1
SCR_CTRL2	0x0004	HW	0x00000000	Control Register 2
SCR_SCPADS	0x0008	HW	0x00000000	Smart Card Pads Register
SCR_INTEN1	0x000C	HW	0x00000000	Interrupt Enable Register 1
SCR_INTSTAT1	0x0010	HW	0x00000000	Interrupt Status Register 1
SCR_FIFOCTRL	0x0014	HW	0x00000000	FIFO Control Register
SCR_LEGTXFICNT	0x0018	B	0x00000000	Legacy TX FIFO Counter
SCR_LEGRXFICNT	0x0019	B	0x00000000	Legacy RX FIFO Counter
SCR_RXFITH	0x001C	HW	0x00000000	RX FIFO Threshold
SCR_REP	0x0020	B	0x00000000	Repeat
SCR_SCCDDIV	0x0024	HW	0x00000000	Smart Card Clock Divisor
SCR_BAUDDIV	0x0028	HW	0x00000000	Baud Clock Divisor
SCR_SCGUTIME	0x002C	B	0x00000000	Smart Card Guard-time
SCR_ADEATIME	0x0030	HW	0x00000000	Activation / Deactivation Time
SCR_LOWRSTTIME	0x0034	HW	0x00000000	Reset Duration
SCR_ATRSTARTLIMIT	0x0038	HW	0x00000000	ATR Start Limit
SCR_C2CLIM	0x003C	HW	0x00000000	Two Characters Delay Limit
SCR_INTEN2	0x0040	HW	0x00000000	Interrupt Enable Register 2
SCR_INTSTAT2	0x0044	HW	0x00000000	Interrupt Status Register 2
SCR_TXFITH	0x0048	HW	0x00000000	TX FIFO Threshold
SCR_TXFIFOCNT	0x004C	HW	0x00000000	TX FIFO Counter
SCR_RXFIFOCNT	0x0050	HW	0x00000000	RX FIFO Counter
SCR_BAUDTUNE	0x0054	B	0x00000000	Baud Tune Register
SCR_FIFO	0x0200	B	0x00000000	FIFO

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.2 Detail Registers Description

SCR_CTRL1

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	GINTEN When high, INTERRUPT output assertion is enabled.
14	RO	0x0	reserved
13	RW	0x0	TCKEN When enabled all ATR bytes beginning from T0 are being XOR-ed. The result must be equal to TCK byte (when present). If the TCK byte does not match the computed value the ATR is considered to be malformed.
12	RW	0x0	ATRSTFLUSH When enabled, both FIFOs are flushed before the ATR is started.
11	RW	0x0	T0T1 Controls the using of T=0 or T=1 protocol. No character repeating is used when T=1 protocol is selected. The Character Guard-time (minimum delay between the leading edges of two consecutive characters) is reduced to 11 ETU when T=1 protocol is used and Guard-time value N = 255. The delay between the leading edge of the last received character and the leading edge of the first character transmitted is 16 ETU when T=0 protocol is used and 22 ETU when T=1 protocol is used.

Bit	Attr	Reset Value	Description
10	RW	0x0	TS2FIFO Enables to store the first ATR character TS in RX FIFO. During ideal card session there is no necessity to store TS character, so it can be disabled
9	RW	0x0	RXEN When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
8	RW	0x0	TXEN When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card
7	RW	0x0	CLKSTOPVAL The value of the scclk output during the clock stop state.
6	RW	0x0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in 'Z' state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is de-asserted. New character transmission can be started by superior system after the CLKSTARTDELAY time expires. The expiration of both times is signaled by the CLKSTOPRUN bit in the Interrupt registers. Reading '1' from this bit signals that the clock is stopped or CLKSTARTDELAY time not expired yet. Reading '0' from this bit signals that the clock is not stopped.
5:3	RO	0x0	reserved
2	RW	0x0	PECH2FIFO Enables storage of the characters received with wrong parity in RX FIFO.
1	RW	0x0	INVORD When High, inverse bit ordering convention(MSB-LSB) is used.
0	RW	0x0	INVLEV When high, inverse level convention is used(A= '1', Z='0');

SCR_CTRL2

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	Reserved Reserved bits are hard-wired to zero
7	RW	0x0	VCC50 Control 5V Smart Card Vcc. Setting of this bit allows selection of 5V Vcc for Smart Card session (Class A). After the selection of operating class is completed, this bit is in '1' if this class was selected. Default value after reset is '0'.
6	RW	0x0	VCC33 Setting of this bit allows selection of 3V Vcc for Smart Card session (Class B). After the selection of operating class is completed, this bit is in '1' if this class was selected. Default value after reset is '0'.
5	RW	0x0	VCC18 Control 1.8V Smart Card Vcc. Setting of this bit allows selection of 1.8V Vcc for Smart Card session (Class C). After the selection of operating class is completed, this bit is in '1' if this class was selected. Default value after reset is '0'.

Bit	Attr	Reset Value	Description
4	RW	0x0	DEACT Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
3	RW	0x0	ACT Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.
2	WO	0x0	WARMRST Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
1:0	RO	0x0	reserved

SCR_SCPADS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	SCPRESENT This bit is set to '1' when the SCDETECT input is active at least for SCDETECTTIME
8	RW	0x0	DSCFCB It provides direct access to SCFCB output
7	RW	0x0	DSCVPPPP It provides direct access to SCVPPPP output
6	RW	0x0	DSCVPPEN It provides direct access to SCVPPEN output
5	RW	0x0	AUTOADEAVPP When high, it enables automatic handling of DSCVPPEN and DSCVPPPP signals during activation and deactivation sequence.
4	RW	0x0	DSCVCC Direct Smart Card Vcc. When DIRACCPADS = '1', the DSCVCC bit provides direct access to SCVCCx outputs. The appropriate SCVCC18, SCVCC33 and SCVCC50 outputs are driven according to state of bits VCC18, VCC33 and VCC50 in CTRL2 register.
3	RW	0x0	DSCRST When DIRACCPADS = '1', the DSCRST bit provides direct access to SCRST output
2	RW	0x0	DSCCLK When DIRACCPADS = '1', the DSCCLK bit provides direct access to SCCLK output
1	RW	0x0	DSCIO When DIRACCPADS = '1', the DSCIO bit provides direct access to SCIO pad.
0	RW	0x0	DIRACCPADS When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

SCR_INTEN1

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCDEACT When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
14	RW	0x0	SCACT When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.

Bit	Attr	Reset Value	Description
13	RW	0x0	SCINS When enabled, this interrupt is asserted after the smart card insertion
12	RW	0x0	SCREM When enabled, this interrupt is asserted after the smart card removal.
11	RW	0x0	ATRDONE When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
10	RW	0x0	ATRFAIL When enabled, this interrupt is asserted if the ATR sequence fails.
9	RW	0x0	RXTHRESHOLD When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
8	RW	0x0	C2CFULL When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
7	RW	0x0	RXPERR When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used
6	RW	0x0	TXPERR When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard-time after the character transmission was repeated TXREPEAT-times
5	RW	0x0	RXDONE When enabled, this interrupt is asserted after a character was received from the Smart Card.
4	RW	0x0	TXDONE When enabled, this interrupt is asserted after one character was transmitted to the Smart Card.
3	RW	0x0	CLKSTOPRUN When enabled, this interrupt is asserted in two cases: 1. When the smart card clock is stopped (after CLOCKSTOP assertion). 2. When the new character transfer can be started (the smart card clock is fully running after CLOCKSTOP de-assertion).
2	RW	0x0	RXFIFULL When enabled, this interrupt is asserted if the RX FIFO is filled up.
1	RW	0x0	TXFIEMPTY When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	RW	0x0	TXFIDONE When enabled, this interrupt is asserted after all bytes from TX FIFO were transferred to the Smart Card

SCR_INTSTAT1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCDEACT When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
14	RW	0x0	SCACT When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.
13	RW	0x0	SCINS When enabled, this interrupt is asserted after the smart card insertion
12	RW	0x0	SCREM When enabled, this interrupt is asserted after the smart card removal.
11	RW	0x0	ATRDONE When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
10	RW	0x0	ATRFAIL When enabled, this interrupt is asserted if the ATR sequence fails.
9	RW	0x0	RXTHRESHOLD When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
8	RW	0x0	C2CFULL When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
7	RW	0x0	RXPERR When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used
6	RW	0x0	TXPERR When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard-time after the character transmission was repeated TXREPEAT-times
5	RW	0x0	RXDONE When enabled, this interrupt is asserted after a character was received from the Smart Card.
4	RW	0x0	TXDONE When enabled, this interrupt is asserted after one character was transmitted to the Smart Card.
3	RW	0x0	CLKSTOPRUN When enabled, this interrupt is asserted in two cases: 1. When the smart card clock is stopped (after CLOCKSTOP assertion). 2. When the new character transfer can be started (the smart card clock is fully running after CLOCKSTOP de-assertion).
2	RW	0x0	RXFIFULL When enabled, this interrupt is asserted if the RX FIFO is filled up.
1	RW	0x0	TXFIEMPTY When enabled, this interrupt is asserted if the TX FIFO is emptied out.

Bit	Attr	Reset Value	Description
0	RW	0x0	TXFIDONE When enabled, this interrupt is asserted after all bytes from TX FIFO were transferred to the Smart Card

SCR_FIFOCTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	WO	0x0	RXFIFLUSH RX FIFO is flushed, when '1' is written to this bit.
9	RO	0x0	RXFIFULL RX FIFO Full
8	RO	0x0	RXFIEMPTY RX FIFO Empty
7:3	RO	0x00	reserved
2	WO	0x0	TXFIFLUSH TX FIFO is flushed, when '1' is written to this bit.
1	RO	0x0	TXFIFULL TX FIFO Full
0	RO	0x0	TXFIEMPTY TX FIFO Empty.

SCR_LEGTXFICNT

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	LEGTXFICNT It is equal to TX FIFO Counter up to value 255. All values above 255 are read as 255. It is recommended to use the 16-bit TX FIFO Counter instead of this register.

SCR_LEGRXFICNT

Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	LEGRXFICNT It is equal to RX FIFO Counter up to value 255. All values above 255 are read as 255. It is recommended to use the 16-bit RX FIFO Counter instead of this register.

SCR_RXFITH

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	RXFITH The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold

SCR_REP

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RXREP This is a 4-bit, read/write register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the 1 ETU long error signal during the guard-time
3:0	RW	0x0	TXREP This is a 4-bit, read/write register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guardtime.

SCR_SCCDDIV

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	SCCDDIV This is a 16-bit, read/write register that defines the divisor value used to generate the Smart Card Clock from the system clock.

SCR_BAUDDIV

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	BAUDDIV This is a 16-bit, read/write register that defines a divisor value used to generate the Baud Clock impulses from the system clock

SCR_SCGUTIME

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	SCGUTI This is an 8-bit, read/write register that sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in Elementary Time Units (ETU). The parity error is besides signaled during the guardtime

SCR_ADEATIME

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	ADEATIME Sets the duration of each part of the activation and deactivation sequence. The value is in Smart Card Clock Cycles.
7:0	RW	0x00	Reserved Reserved bits are hard-wired to zero.

SCR_LOWRSTTIME

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	LOWRSTTIME Sets the duration of the smart card reset sequence. This value is same for the cold and warm reset. The value is in terms of smart card clock cycles.

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Reserved Bits (7:0) of this register are hard-wired to zero.

SCR_ATRSTARTLIMIT

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	ATRSTARTLIMIT Defines the maximum time between the rising edge of the SCRSTN signal and the start of ATR response. The value is in terms of smart card clock cycles
7:0	RW	0x00	Reserved Bits (7:0) of this register are hard-wired to zero

SCR_C2CLIM

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	C2CLIM This is a 16-bit, read/write register that sets the maximum time between the leading edges of two, consecutive characters. The value is in ETUs.

SCR_INTEN2

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	TCKERR When enabled, this interrupt is asserted if the TCK byte does not match computed value.
0	RW	0x0	TXTHRESHOLD When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.

SCR_INTSTAT2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	TCKERR When enabled, this interrupt is asserted if the TCK byte does not match computed value.
0	RW	0x0	TXTHRESHOLD When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.

SCR_TXFITH

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	TXFITH The interrupt is asserted when the number of bytes in TX FIFO is equal or less than the threshold

SCR_TXFIFOCNT

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	TXFIFOCNT This is a 16-bit, read-only register that provides the number of bytes stored in the RX FIFO

SCR_RXFIFOCNT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	RXFIFOCNT This is a 16-bit, read-only register that provides the number of bytes stored in the RX FIFO.

SCR_BAUDTUNE

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	BAUDTUNE This is a 3-bit, read/write register that defines an additional value used to increase the accuracy of the Baud Clock impulses

SCR_FIFO

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	FIFO This is an 8-bit, read/write register that provides access to the receive and transmit FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer. All read/write accesses at address range 200h-3ffh are redirected to the FIFO.

25.5 Interface Description

Table 25-1 SCR Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
sc_clk	O	I2S1_MCLK_M0/UART3_RTSn_M0/SCR_CLK/PCIE30X1_PERSTn_M2/GPIO1_A2_d	GRF_GPIO1A_IOMUX_L[11:8]=4'h3
sc_rst	O	I2S1_LRCK_TX_M0/UART4_RTSn_M0/SCR_RST/PCIE30X1_CLKREQn_M2/ACODEC_DAC_SYNC/GPIO1_A5_d	GRF_GPIO1A_IOMUX_H[7:4]=4'h3
sc_detect	I	I2S1_SDO0_M0/UART4_CTSn_M0/SCR_DET/AUDIOPWM_ROUT_N/ACODEC_DAC_DATAL/GPIO1_A7_d	GRF_GPIO1A_IOMUX_H[15:12]=4'h3
sc_io	I	I2S1_SCLK_TX_M0/UART3_CTSn_M0/SCR_IO/PCIE30X1_WAKEn_M2/ACODEC_DAC_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_L[15:12]=4'h3

Notes: I=input, O=output, I/O=input/output, bidirectional

25.6 Application Notes

25.6.1 BCHST/BCHLOC/BCHDE/SPARE Application

The Smart Card Clock signal is used as the main clock for the smart card. Its frequency can be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock.

The SCCLK frequency is given by the following equation:

$$\mathrm{SCCLK_{freq}} = \frac{\mathrm{CLK\_freq}}{2 * (\mathrm{SCCDIV} + 1)}, \qquad \mathrm{SCCDIV} \cong \frac{\mathrm{CLK_{freq}}}{2 * \mathrm{SCCLK_{freq}}} - 1$$

SCCLK_freq– Smart Card Clock Frequency

CLK_freq- System Clock Frequency

The Baud Clock Impulse signal is used to transmit and receive serial data between the Smart Card Reader and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV)which is used to divide the system clock. The BAUDDIV value must be >= 4. The BAUD rate is given by the following equation:

$$\mathrm{BAUD_{rate}} = \frac{\mathrm{CLK\_freq}}{2 * (\mathrm{BAUDDIV} + 1)}$$

The duration of one bit, Elementary Time Unit (ETU) and parameters F and D are defined in the ISO/IEC7816-3 specification.

$$\frac{1}{\mathrm{BAUD\_rate}} \cong \mathrm{ETU} = \frac{\mathrm{F}}{\mathrm{D}} * \frac{1}{\mathrm{SCCLK_{freq}}}, \frac{\mathrm{F}}{\mathrm{D}} \cong \frac{\mathrm{BAUDDIV} + 1}{\mathrm{SCCDIV} + 1}$$

BAUDDIV equation based on SCCDIV value and Smart Card parameters F and D is following:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{\mathrm{F}}{\mathrm{D}} - 1$$

During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 Smart Card Clock Cycles (given by parameters F=372 and D=1). In this case, the BAUDDIV should be:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{372}{1} - 1$$

After the ATR is completed, the BAUDDIV register value can be changed according to Smart Card parameters F and D.

Baud Tune Register (BAUDTUNE) 3-bit value that can be used to increase the accuracy of the Baud Clock impulses timing by using the BAUDTUNE Increment from Table listed below in combination with BAUDDIV register value.

Table 25-2 BAUDTUNE register

BAUDTUNE	000	001	010	011	100	101	110	111
BAUDTUNEINCR	+0	+0.125	0.25	+0.375	+0.5	+0.625	+0.75	+0.875

$$\mathrm{BAUDDIV} + \mathrm{BAUDTUNE_{INCR}} \cong (\mathrm{SCCDIV} + 1) * \frac{\mathrm{F}}{\mathrm{D}} - 1$$

The BAUDDIV register value (nearest integer) can be computed using following equation:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{\mathrm{F}}{\mathrm{D}} - 1 - \mathrm{BAUDTUNE_{INCR}}$$

25.6.2 Smart Card Detect Application

It is configurable for SCR's detect pin when Smart Card is inserted.

When config GRF_SOC_CON2[5]=0, SCDETECT`s active state is 1.

When config GRF_SOC_CON2[5]=1, SCDETECT`s active state is 0.

Chapter 26 EBC

26.1 Overview

EBC is the TCON module for E-ink Electronic Paper Display (EPD).

26.1.1 Features

- **System interface**
  - AHB slave for register configuration
  - AHB master for frame data transfer (DMA)
  - Interrupt output
- **EPD interface**
  - E-ink EPD compatible
  - Up to 2200x1650 resolution
  - Up to 16 level gray scale
  - Up to 256 frames every scanning
  - LUT updateable (16KB)
  - Direct mode and LUT mode, THREE_WIN_MODE, EINK_mode
  - All-update mode and Diff-update mode
  - Single-phase and multi-phase mode
  - Support window display
  - Source driver interface
  - Gate driver interface

26.2 Block Diagram

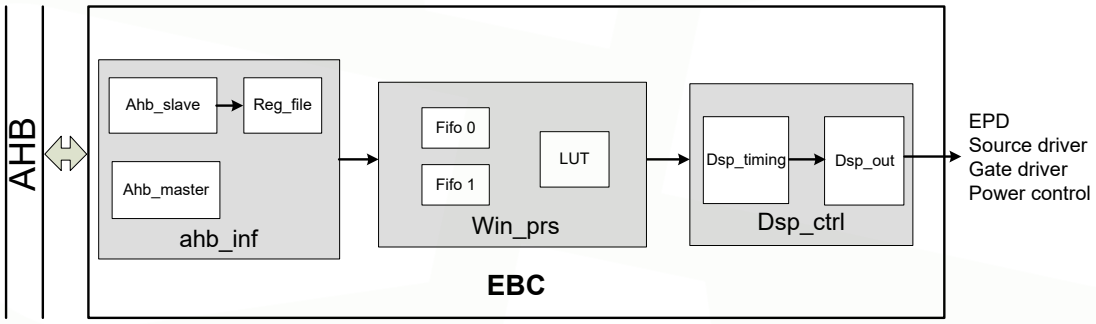


Fig.26-1 EBC Block Diagram

26.3 Function Description

26.3.1 Data Format

Table 26-1 EBC Input Data Format

DSP_LUT MODE	WIN_FMT [1:0]	Data format	Bit Map
0	xx	S-data(2bpp)	{S3[7:0], S2[7:0], S1[7:0], S0[7:0]}
1	00	Y-data(4bpp)	{Y7[3:0], Y6[3:0], Y5[3:0], Y4[3:0], Y3[3:0], Y2[3:0], Y1[3:0], Y0[3:0]}
1	01	Y-data(8bpp)	{Y3[7:0], Y2[7:0], Y1[7:0], Y0[7:0]}
1	10	RGB888	{8'bx, R[7:0], G[7:0], B[7:0]}
1	11	RGB565	{ R1[4:0], G1[5:0], B1[4:0], R0[4:0], G0[5:0], B0[4:0]}

26.3.2 Waveform generation mode

1. Direct mode

In direct scanning mode, the source data is just read by internal DMA and sent to the display output directly.

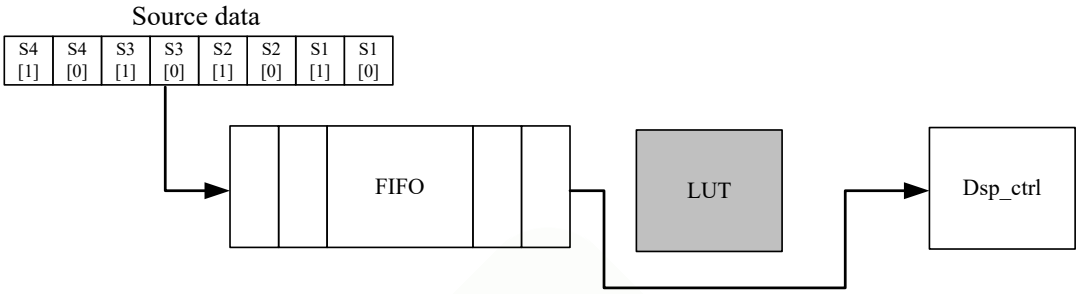


Fig.26-2 EBC Block Diagram

2. LUT mode

In LUT scanning mode, internal DMA read the original pixel data into the FIFO, then the pixel data is sent to the look-up table to be translated the EPD source data.

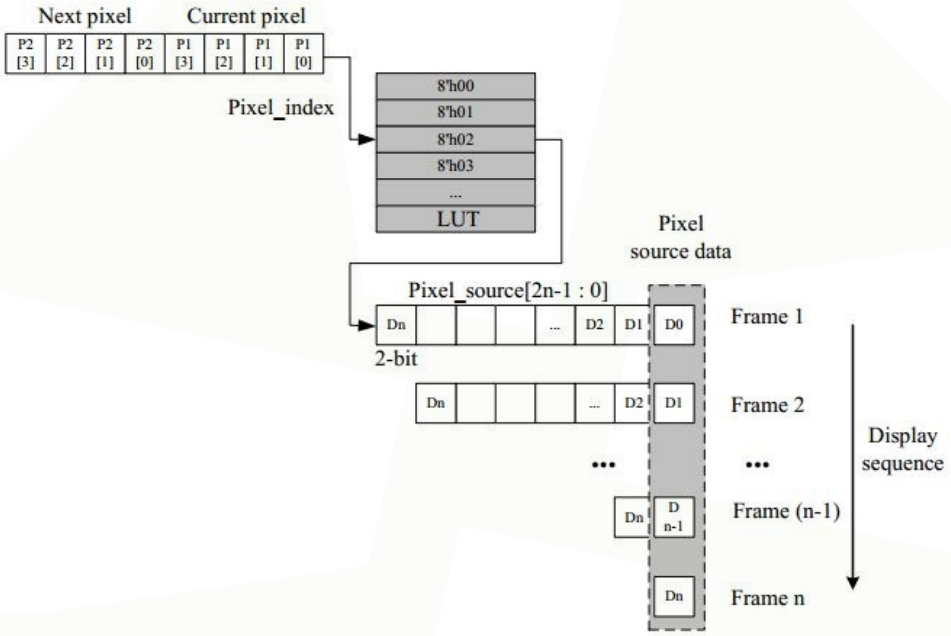


Fig.26-3 LUT mode Diagram

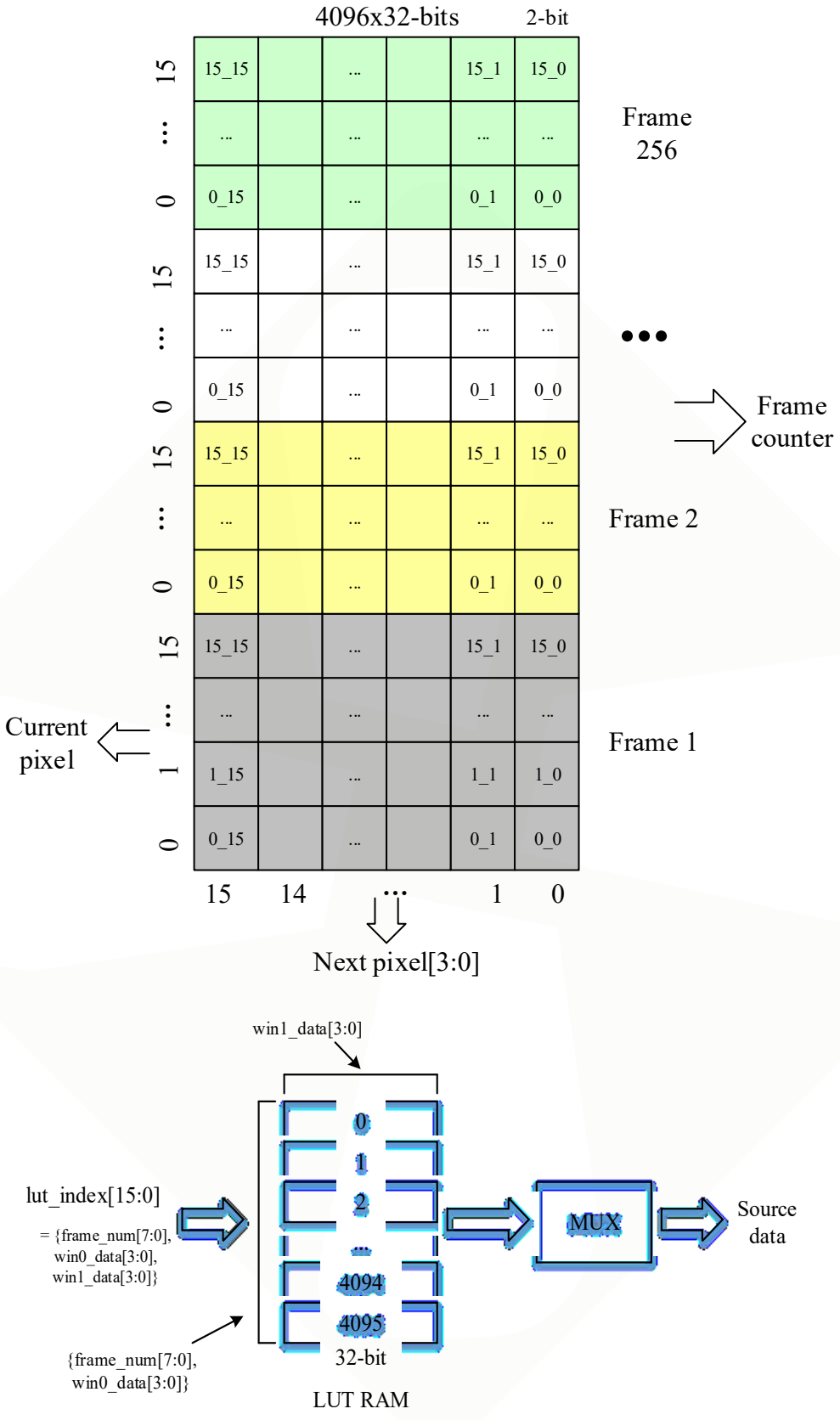


Fig.26-4 EBC LUT structure

3. 3win LUT mode

Compared with the LUT mode, in addition to the current image and the target image, the memory also contains frame number information. The frame number information in the

original LUT mode is counted by a counter, while the frame number information in 3win_mode is read from memory.

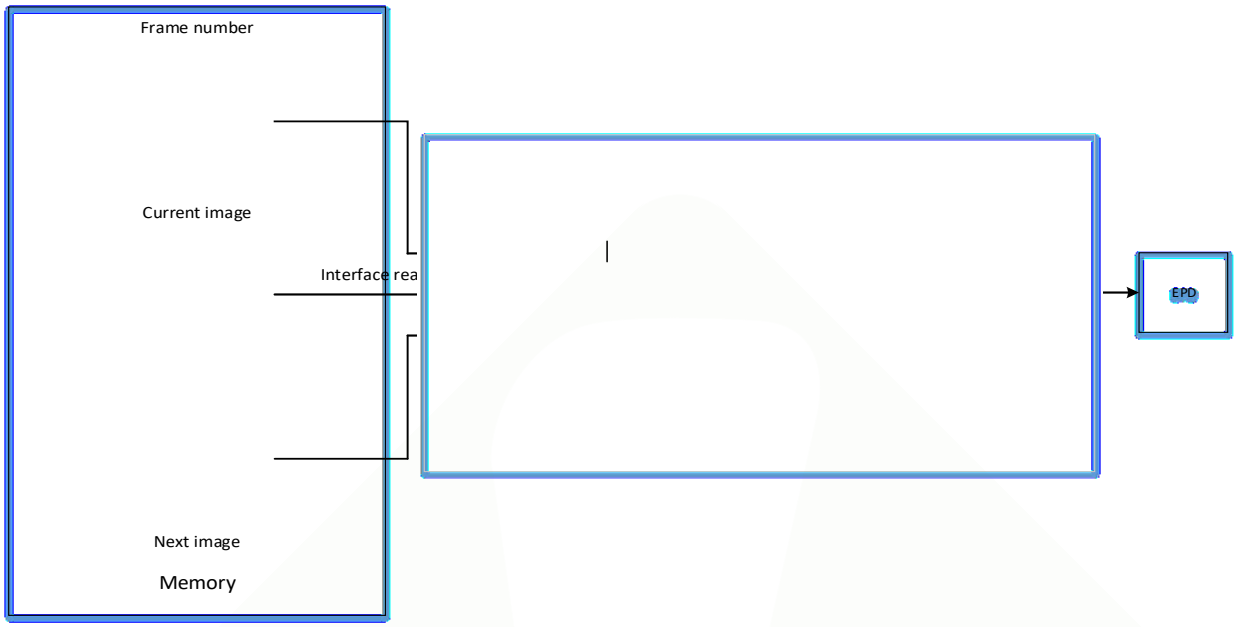


Fig.26-5 EBC 3win mode

4. EINK mode

Different from the other two look-up table modes, the data of the current image and the next image of eink_mode are stored in the same memory.

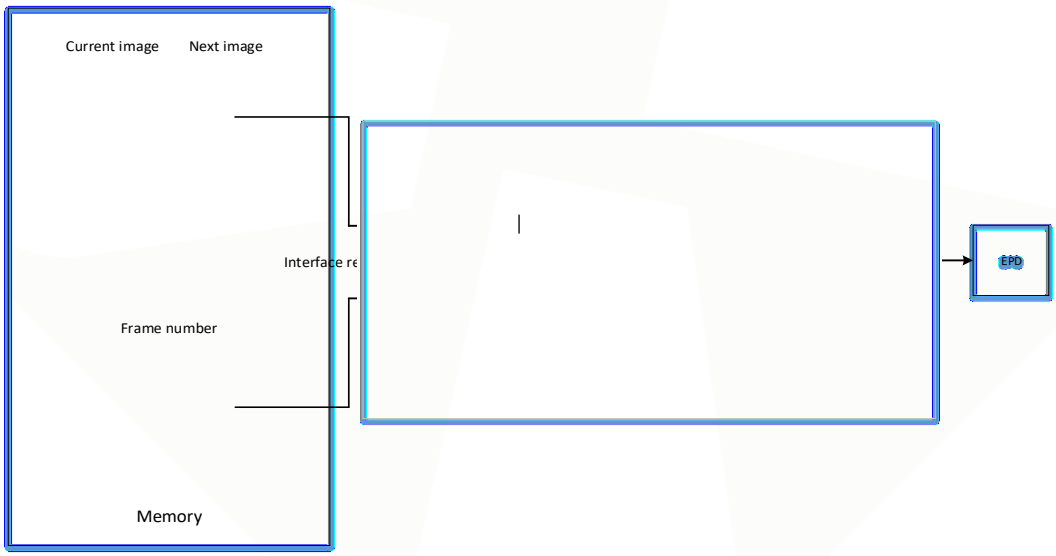


Fig.26-6 EINK mode

26.3.3 Window display mode

Window display is supported in EBC, dsp_win_width/dsp_win_height and dsp_win_st should be set to define the display window. The source value of other area is background value, which is configurable.

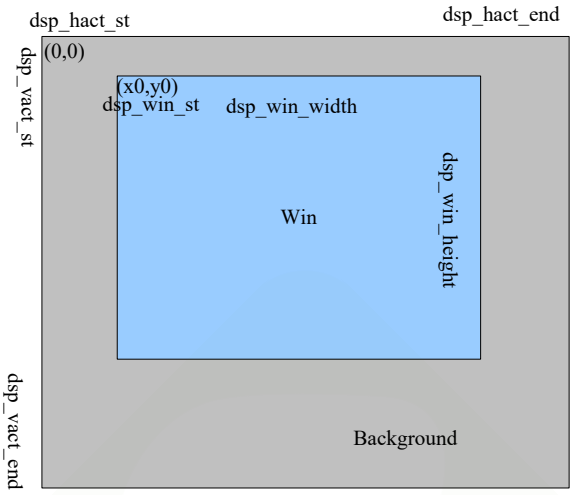


Fig.26-7 EBC window display

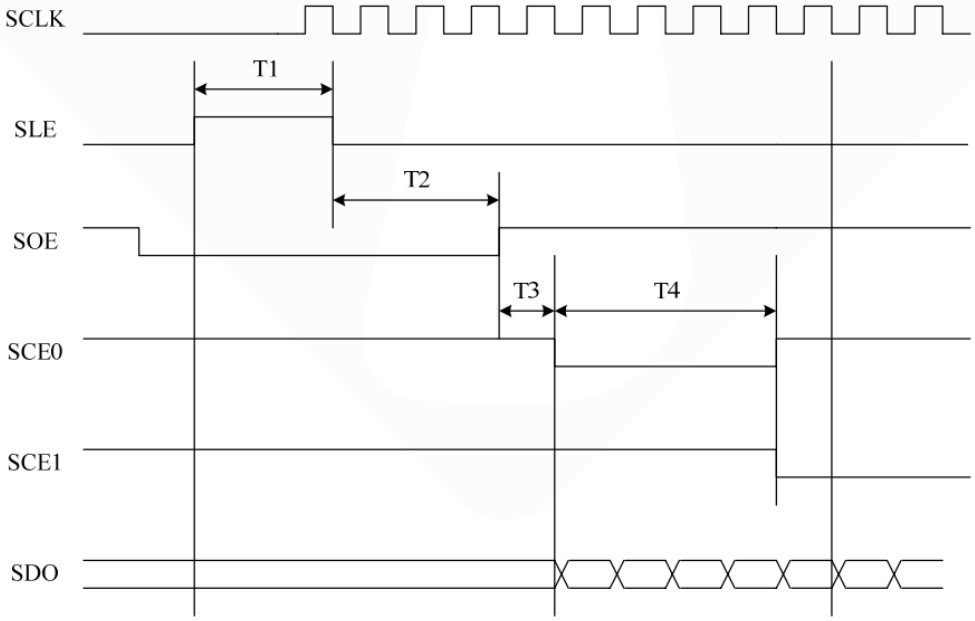
26.3.4 IO description

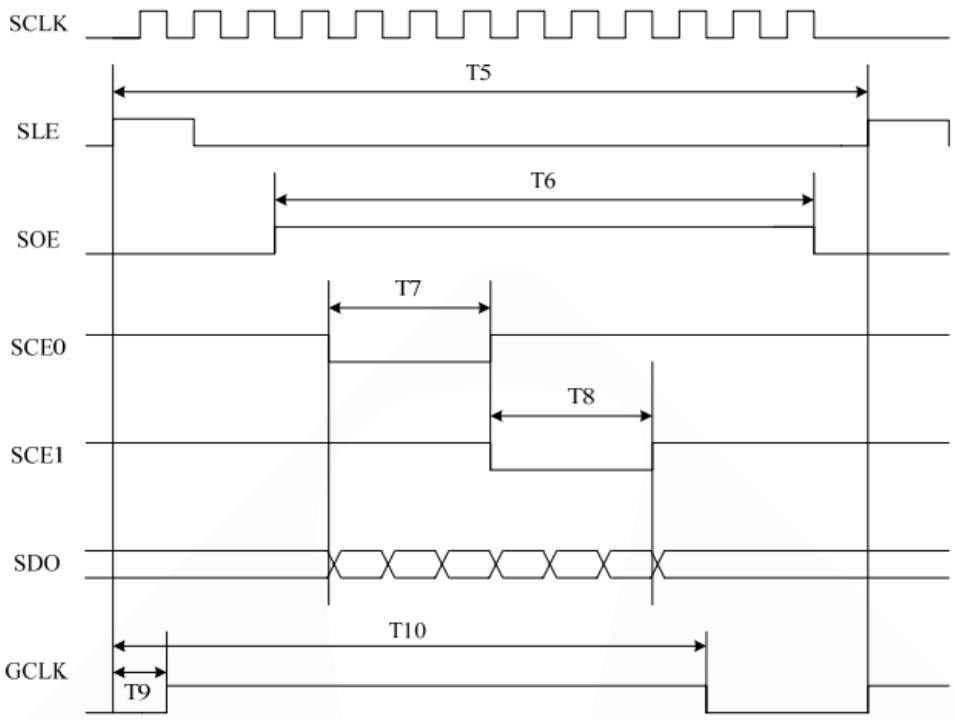
Table 26-2 EBC output pins

EINK	Description
SCLK	Source clock
SLE	Source latch data enable
SOE	Source data enable/start pulse
SCE[5:0]	
SDO[7:0]	Source data
SDIR	X scanning direction
GCLK	Gate clock
GSP	Gate start pulse
GOE	Gate output enable
GDIR	Y scanning direction
BORDER[1:0]	COM voltage
VCOM_CTRL	VCOM enable
PWR[2:0]	POWER control

26.3.5 Eink EPD driver interface

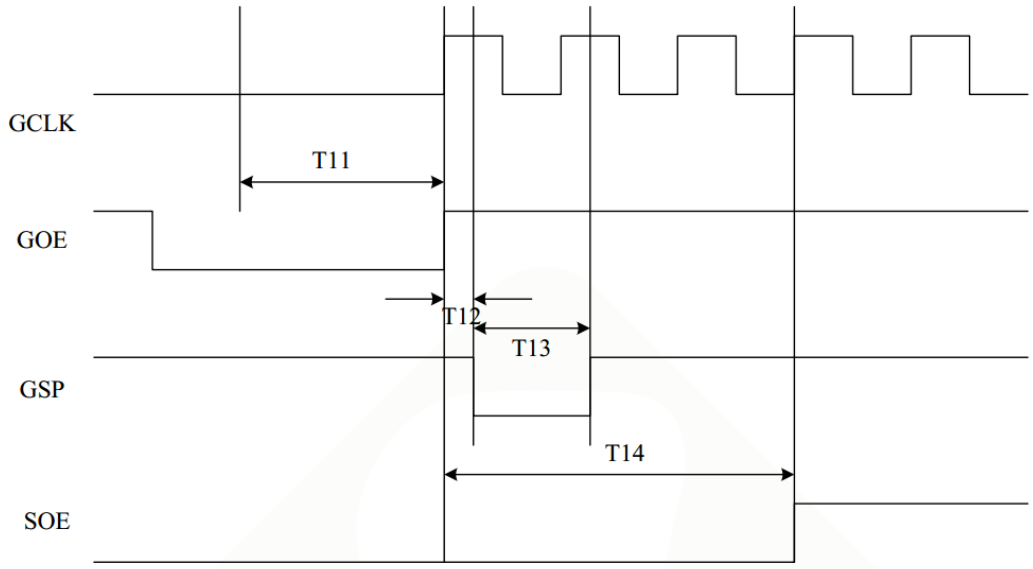
1. Source driver interface

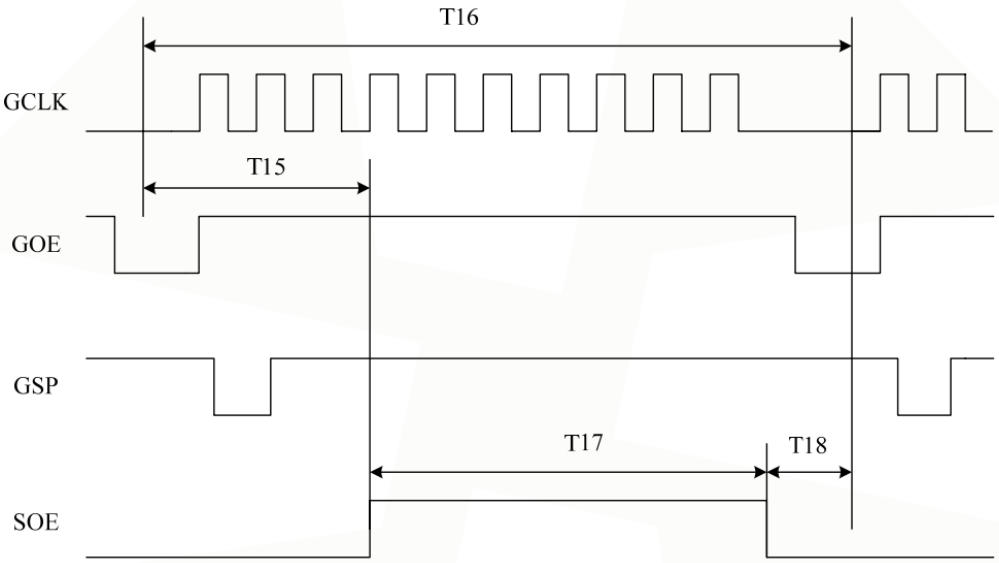




Timing	Value (6-inch 800x600)	Register setting
DCLK	33.25MHz	
SCLK	4 DCLK(8.3125 MHz)	(DSP_CLK_DIV+1)
T1	10 SCLK	DSP_HS_END
T2	3 SCLK	(DSP_HACT_ST – DSP_HS_END)
T3	1 SCLK	Fixed
T1+T2+T3	14 SCLK	DSP_WIN_XST
T4	100 SCLK	DSP_SCE_WIDTH
T5	315 SCLK	DSP_HTOTAL
T6	300 SCLK	(DSP_HACT_END – DSP_HACT_ST)
T7	100 SCLK	DSP_SCE_WIDTH
T8	100 SCLK	DSP_SCE_WIDTH
T9	0 SCLK	DSP_GCLK_ST
T10	215 SCLK	DSP_GCLK_END

2. Gate driver interface





Timing	Value (6-inch 800x600)	Register setting
GCLK	315 SCLK	DSP_HTOTAL
T11	4 GCLK	DSP_VS_END
T12	107 SCLK	(DSP_GD_END/2)
T13	1 GCLK	Fixed
T14	4 GCLK	(DSP_VACT_ST - DSP_VS_END)
T15	8 GCLK	DSP_VACT_ST
T16	619 GCLK	DSP_VTOTAL
T17	601 GCLK	(DSP_VACT_END - DSP_VACT_ST)
T18	11 GCLK	(DSP_VTOTAL - DSP_VACT_END)

26.4 Register Description

26.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EBC_DSP_START	0x0000	W	0x00000000	Frame start register
EBC_EPD_CTRL	0x0004	W	0x00000000	EPD control register
EBC_DSP_CTRL	0x0008	W	0x00000000	display control register
EBC_DSP_HTIMING0	0x000C	W	0x00000000	panel scanning timing register(horizontal period, hsync pulse width)
EBC_DSP_HTIMING1	0x0010	W	0x00000000	panel scanning timing register(horizontal active start/end point)
EBC_DSP_VTIMING0	0x0014	W	0x00000000	panel scanning timing register(vertical period, vsync pulse width)
EBC_DSP_VTIMING1	0x0018	W	0x00000000	panel scanning timing register(vertical active start/end point)
EBC_DSP_ACT_INFO	0x001C	W	0x00000000	display width/height register
EBC_WIN_CTRL	0x0020	W	0x00000000	win data start address in memory
EBC_WIN_MST0	0x0024	W	0x00000000	current image data start address in memory
EBC_WIN_MST1	0x0028	W	0x00000000	next image data start address in memory
EBC_WIN_VIR	0x002C	W	0x00000000	win virtual width/height register
EBC_WIN_ACT	0x0030	W	0x00000000	Win active width/height register
EBC_WIN_DSP	0x0034	W	0x00000000	win display width/height register
EBC_WIN_DSP_ST	0x0038	W	0x00000000	win display start point
EBC_INT_STATUS	0x003C	W	0x00000000	Interrupt status register
EBC_VCOM0	0x0040	W	0x00000000	VCOM setting register
EBC_VCOM1	0x0044	W	0x00000000	VCOM setting register
EBC_VCOM2	0x0048	W	0x00000000	VCOM setting register
EBC_VCOM3	0x004C	W	0x00000000	VCOM setting register
EBC_CONFIG_DONE	0x0050	W	0x00000000	register config done flag
EBC_VNUM	0x0054	W	0x00000000	EBC line flag num
EBC_WIN_MST2	0x0058	W	0x00000000	Frame win memory start
EBC_LUT_ADDRESS_MAP_0	0x1000	W	0x00000000	LUT ADDRESS_0
EBC_LUT_ADDRESS_MAP_4095	0x4FFC	W	0x00000000	LUT ADDRESS_4095

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.2 Detail Register Description

EBC_DSP_START

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	dsp_out_low 1'b0: normal 1'b1: outputs are low
30:26	RO	0x00	reserved
25:16	RW	0x000	dsp_sdce_width source driver length
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	dsp_eink_mode eink mode enable 1'b0: lut mode or direct mode or 3win mode 1'b1: eink mode
12	RW	0x0	sw_burst_ctrl 1'b0: original burst 1'b1: modified burst
11:10	RO	0x0	reserved
9:2	RW	0x00	dsp_frm_total frame total number(n) frame_num = n+1.
1	RW	0x0	dsp_rst soft reset bit
0	RW	0x0	dsp_frm_st frame start bit writing '1' to trigger frame display. read this bit for hold status.

EBC_EPD_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	eink_mode_swap 1'b0: no swap 1'b1: swap
30	RW	0x0	eink_mode_frm_sel 1'b0: frame cnt 1'b1: win2 data
29:27	RO	0x0	reserved
26:16	RW	0x000	dsp_gd_end GCLK falling edge point(SCLK), which count from the falling edge of hsync
15:8	RW	0x00	dsp_gd_st GCLK rising edge point(SCLK), which count from the falling edge of hsync
7	RW	0x0	dsp_three_win_mode three win mode enable 1'b0: lut mode or direct mode 1'b1: three win mode
6	RW	0x0	dsp_sddw_mode source data output width 1'b0: 8-bit output 1'b1: 16-bit output
5	RW	0x0	epd_auo EPD panel 1'b0: Eink 1'b1: AUO
4:2	RW	0x0	epd_pwr power enable
1	RW	0x0	epd_gdrl gate scanning direction 1'b0: top to button 1'b1: button to top

Bit	Attr	Reset Value	Description
0	RW	0x0	epd_sdshr source scanning direction 1'b0: left to right 1'b1: right to left

EBC_DSP_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	dsp_swap_mode display swap for 8bit output 2'b00: SDO[7:0] = P3,P2,P1,P0 2'b01: SDO[7:0] = P1,P0,P3,P2 2'b10: SDO[7:0] = P2,P3,P0,P1 2'b11: SDO[7:0] = P0,P1,P2,P3 for 16bit output 2'b00: SDO[15:0] = P7,P6,P5,P4,P3,P2,P1,P0 2'b01: SDO[15:0] = P4,P5,P6,P7,P0,P1,P2,P3 2'b10: SDO[15:0] = P0,P1,P2,P3,P4,P5,P6,P7 2'b11: SDO[15:0] = P3,P2,P1,P0,P7,P6,P5,P4
29	RW	0x0	dsp_diff_mode diff update mode enable 1'b0: normal update mode 1'b1: diff update mode
28	RW	0x0	dsp_lut_mode display mode 1'b0: direct mode 1'b1: LUT mode
27	RW	0x0	dsp_vcom_mode VCOM Mode 1'b0: one phase scanning mode 1'b1: multi phase scanning mode
26	RW	0x0	dsp_gdoe_pol DSP OUTPUT GOE polarity invert 1'b0: default 1'b1: invert
25	RW	0x0	dsp_gdsp_pol DSP OUTPUT GSP polarity invert 1'b0: default 1'b1: invert
24	RW	0x0	dsp_gdclk_pol DSP OUTPUT GCLK polarity invert 1'b0: default 1'b1: invert
23	RW	0x0	dsp_sdce_pol DSP OUTPUT SCE polarity invert 1'b0: default 1'b1: invert
22	RW	0x0	dsp_sdoe_pol DSP OUTPUT SOE polarity invert 1'b0: default 1'b1: invert

Bit	Attr	Reset Value	Description
21	RW	0x0	dsp_sdle_pol DSP OUTPUT SLE polarity invert 1'b0: default 1'b1: invert
20	RW	0x0	dsp_sdclk_pol DSP_OUTPUT SCLK polarity invert 1'b0: default 1'b1: invert
19:16	RW	0x0	dsp_sdclk_div SCLK divide rate SCLK = (DSP_CLK_DIV + 1) * DCLK
15:0	RW	0x0000	dsp_background SDO default value

EBC_DSP_HTIMING0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_htotal panel display scanning horizontal period.
15:8	RO	0x00	reserved
7:0	RW	0x00	dsp_hs_end panel display scanning hsync(SLE) pulse width.

EBC_DSP_HTIMING1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dsp_hact_end panel display scanning horizontal active end point
15:8	RO	0x00	reserved
7:0	RW	0x00	dsp_hact_st panel display scanning horizontal active start point

EBC_DSP_VTIMING0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dsp_vtotal panel display scanning vertical period.
15:8	RO	0x00	reserved
7:0	RW	0x00	dsp_vs_end panel display scanning vsync(GOE) pulse width.

EBC_DSP_VTIMING1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dsp_vact_end panel display scanning vertical active end point
15:8	RO	0x00	reserved
7:0	RW	0x00	dsp_vact_st panel display scanning vertical active start point

EBC_DSP_ACT_INFO

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	dsp_height display height
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_width display width

EBC_WIN_CTRL

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:19	RW	0x000	win2_fifo_almost_full_level win2(frame_num) fifo almost full level
18	RW	0x0	win_en win enable
17:13	RW	0x00	ahb_incr_num_reg ahb master incr num
12:10	RW	0x0	ahb_burst_reg ahb master burst type
9:2	RW	0x00	win_fifo_almost_full_level win fifo almost full level
1:0	RW	0x0	win_fmt win source data format: 2'b00: Y-data(4bpp) 2'b01: Y-data(8bpp) 2'b10: RGB888(24bpp) 2'b11: RGB565(16bpp)

EBC_WIN_MST0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	win_mst0 start address of current image data in memory

EBC_WIN_MST1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	win_mst1 start address of next image data in memory

EBC_WIN_VIR

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	win_vir_height win virtual height
15:0	RW	0x0000	win_vir_width win virtual width

EBC_WIN_ACT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	win_act_height win active height
15:12	RO	0x0	reserved
11:0	RW	0x000	win_act_width win active width

EBC_WIN_DSP

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	win_dsp_height win display height
15:12	RO	0x0	reserved
11:0	RW	0x000	win_dsp_width win display width

EBC_WIN_DSP_ST

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	win_dsp_yst win display y start point
15:12	RO	0x0	reserved
11:0	RW	0x000	win_dsp_xst win display x start point

EBC_INT_STATUS

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:12	RW	0x00	dsp_frm_int_num frame number of the scanning flag interrupt the display frame number when the flag interrupt occur, the range is (0~DSP_FRM_NUM-1).
11	RW	0x0	line_flag_int_clr line flag interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
10	RW	0x0	dsp_frm_int_clr display frame interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
9	RW	0x0	dsp_end_int_clr display end interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
8	RW	0x0	frm_end_int_clr frame end interrupt clear: after be set to 1, this bit will clear by itself 1 cycle later.
7	RW	0x0	line_flag_int_msk line flag interrupt mask 1'b0: unmask 1'b1: mask

Bit	Attr	Reset Value	Description
6	RW	0x0	dsp_frm_int_msk frame flag interrupt mask: 1'b0: unmask 1'b1: mask
5	RW	0x0	dsp_end_int_msk display end interrupt mask: 1'b0: unmask 1'b1: mask
4	RW	0x0	frm_end_int_msk frame end interrupt mask: 1'b0: unmask 1'b1: mask
3	RO	0x0	line_flag_int_st line flag interrupt status
2	RO	0x0	dsp_frm_int_st frame flag interrupt status
1	RO	0x0	dsp_end_int_st display end interrupt status
0	RO	0x0	frm_end_int_st frame end interrupt status

EBC_VCOM0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_0 VCOM[1:0] values in 0-15 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_1 VCOM[1:0] values in 16-31 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_2 VCOM[1:0] values in 32-47 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_VCOM3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_border_3 VCOM[1:0] values in 48-64 frame. The VCOM [1:0] indicate the COM voltage in one frame. The VCOM can be different in different frame. So we can set the VCOM [1:0] sequence using display frames before start the display.

EBC_CONFIG_DONE

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	reg_config_done in the first setting of the register, the new value was saved into the mirror register. when all the register config finish, writing this register to enable the copyright of the mirror register to real register. then register would be updated at the start of every frame.

EBC_VNUM

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	dsp_vcnt readable register for Internal line number
15:12	RO	0x0	reserved
11:0	RW	0x000	line_flag_num line number of the scanning flag interrupt the display line number when the flag interrupt occur,the range is (0~DSP_VTOTAL-1).

EBC_WIN_MST2

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win_mst2 start address of frame data in memory

EBC_LUT_ADDRESS_MAP_0

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_data0 LUT_data0

EBC_LUT_ADDRESS_MAP_4095

Address: Operational Base + offset (0x4FFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_data4095 LUT_data4095

26.5 Interface Description

Table 26-3 EBC Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
ebc_sddo[0]	I/O	GPIO3_C6/EBC_SDDO0	GRF_GPIO3C_IOMUX_H[11:8] = 4'h2
ebc_sddo[1]	I/O	GPIO3_C7/EBC_SDDO1	GRF_GPIO3C_IOMUX_H[15:12] = 4'h2
ebc_sddo[2]	I/O	GPIO3_D0/EBC_SDDO2	GRF_GPIO3D_IOMUX_L[3:0] = 4'h2
ebc_sddo[3]	I/O	GPIO3_D1/EBC_SDDO3	GRF_GPIO3D_IOMUX_L[7:4] = 4'h2
ebc_sddo[4]	I/O	GPIO3_D2/EBC_SDDO4	GRF_GPIO3D_IOMUX_L[11:8] = 4'h2
ebc_sddo[5]	I/O	GPIO3_D3/EBC_SDDO5	GRF_GPIO3D_IOMUX_L[15:12] = 4'h2
ebc_sddo[6]	I/O	GPIO3_D4/EBC_SDDO6	GRF_GPIO3D_IOMUX_H[3:0] = 4'h2
ebc_sddo[7]	I/O	GPIO3_D5/EBC_SDDO7	GRF_GPIO3D_IOMUX_H[7:4] = 4'h2

Module Pin	Dir.	Pad Name	IOMUX Setting
ebc_sddo[8]	I/O	GPIO3_D6/EBC_SDDO8	GRF_GPIO3D_IOMUX_H[11:8] = 4'h2
ebc_sddo[9]	I/O	GPIO3_D7/EBC_SDDO9	GRF_GPIO3D_IOMUX_H[15:12] = 4'h2
ebc_sddo[10]	I/O	GPIO4_A0/EBC_SDDO10	GRF_GPIO4A_IOMUX_L[3:0] = 4'h2
ebc_sddo[11]	I/O	GPIO4_A1/EBC_SDDO11	GRF_GPIO4A_IOMUX_L[7:4] = 4'h2
ebc_sddo[12]	I/O	GPIO4_A2/EBC_SDDO12	GRF_GPIO4A_IOMUX_L[11:8] = 4'h2
ebc_sddo[13]	I/O	GPIO4_A3/EBC_SDDO13	GRF_GPIO4A_IOMUX_L[15:12] = 4'h2
ebc_sddo[14]	I/O	GPIO4_A4/EBC_SDDO14	GRF_GPIO4A_IOMUX_H[3:0] = 4'h2
ebc_sddo[15]	I/O	GPIO4_A5/EBC_SDDO15	GRF_GPIO4A_IOMUX_H[7:4] = 4'h2
ebc_sdce[0]	I/O	GPIO4_A6/EBC_SDCE0	GRF_GPIO4A_IOMUX_H[11:8] = 4'h2
ebc_sdce[1]	I/O	GPIO4_A7/EBC_SDCE1	GRF_GPIO4A_IOMUX_H[15:12] = 4'h2
ebc_sdce[2]	I/O	GPIO4_B0/EBC_SDCE2	GRF_GPIO4B_IOMUX_L[3:0] = 4'h2
ebc_sdce[3]	I/O	GPIO4_B1/EBC_SDCE3	GRF_GPIO4B_IOMUX_L[7:4] = 4'h2
ebc_vcom	I/O	GPIO4_B2/EBC_VCOM	GRF_GPIO4B_IOMUX_L[11:8] = 4'h2
ebc_gdoe	I/O	GPIO4_B3/EBC_GDOE	GRF_GPIO4B_IOMUX_L[15:12] = 4'h2
ebc_gdsp	I/O	GPIO4_B4/EBC_GDSP	GRF_GPIO4B_IOMUX_H[3:0] = 4'h2
ebc_sdshr	I/O	GPIO4_B5/EBC_SDSHR	GRF_GPIO4B_IOMUX_H[7:4] = 4'h2
ebc_sdle	I/O	GPIO4_B6/EBC_SDLE	GRF_GPIO4B_IOMUX_H[11:8] = 4'h2
ebc_sdoe	I/O	GPIO4_B7/EBC_SDOE	GRF_GPIO4B_IOMUX_H[15:12] = 4'h2
ebc_gdclk	I/O	GPIO4_C0/EBC_GDCLK	GRF_GPIO4C_IOMUX_L[3:0] = 4'h2
ebc_sdclk	I/O	GPIO4_C1/EBC_SDCLK	GRF_GPIO4C_IOMUX_L[7:4] = 4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

26.6 Application Notes

We use AHB bus to configure EBC. There are four modes in EBC and the specific configuration is as follow.

26.6.1 Direct mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=0, dsp_lut_mode=0;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

26.6.2 LUT mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=0, dsp_lut_mode=1;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

26.6.3 3win LUT mode

Step1: set dsp_eink_mode=0, dsp_three_win_mode=1, dsp_lut_mode=0;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen;

26.6.4 Eink_mode

Step1: set dsp_eink_mode=1, dsp_three_win_mode=0, dsp_lut_mode=0, eink_mode_swap=1;
Step2: set dsp_sdclk_div=4'd3 for 8-bit screen or set dsp_sdclk_div=4'd7 for 16-bit screen.

Chapter 27 MIPI CSI HOST

27.1 Overview

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY following PHY Protocol Interface, as defined in "MIPI Alliance Specification for D-PHY, Version 1.1-7 November 2011"
- Up to four D-PHY RX data lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
  - RGB, YUV, and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types
- Error detection and correction
  - PHY level
  - Packet level
  - Line level
  - Frame level
- Support DSI video mode/command mode

27.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

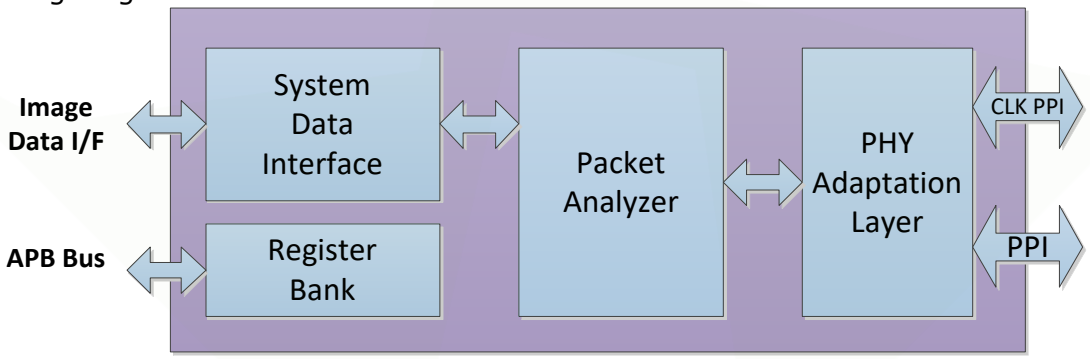


Fig. 27-1 MIPI CSI-2 Host Controller Architecture

- **PHY Adaptation Layer**: Manages the D-PHY PPI interface
- **Packet Analyzer**: Merges the data from the different lanes
- **Image Data Interface**: Reorders pixels into 32-bit data for memory storage and generates timing accurate video synchronization signals
- **AMBA-APB Register Bank**: Provides access to configuration and control registers

27.3 Function Description

27.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.

Following table presents some predefined and supported camera settings, assuming the

following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of following table presents the minimum number of lanes required for each configuration.

Table 27-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

27.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY errors such as synchronization pattern mismatch

Following table shows all the errors that CSI-2 Host Controller can identify.

Table 27-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.
phy_errsoths_*	Start of transmission error on data lane* but	PHY	Informative only since PHY can recover from this

Error	Description	Level	Action
	synchronization can still be achieved		error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packet	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packet	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packet	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packet	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_match_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CSI2HOST_VERSION	0x0000	W	0x00000000	Controller version identification
CSI2HOST_N_LANES	0x0004	W	0x00000000	Number of active data lanes
CSI2HOST_CSI2_RESETN	0x0010	W	0x00000000	CSI2 controller reset
CSI2HOST_PHY_STATE	0x0014	W	0x00000000	General settings for all blocks
CSI2HOST_DATA_IDS_1	0x0018	W	0x00000000	Data IDS for which IDI reports line boundary matching errors
CSI2HOST_DATA_IDS_2	0x001C	W	0x00000000	Data IDS for which IDI reports line boundary matching errors
CSI2HOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSI2HOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSI2HOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSI2HOST_MSK2	0x002C	W	0x00000000	Masks for errors 2
CSI2HOST_CONTROL	0x0040	W	0x0C204000	Control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

27.4.3 Detail Registers Description

CSI2HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	version Version of the csi2host.

CSI2HOST_N_LANES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	n_lanes Number of active data lanes. 2'b00: 1 data lane(lane 0) 2'b01: 2 data lanes(lane0 and 1) 2'b10: 3 data lanes(lane0,1,and 2) 2'b11: 4 data lanes(ALL) Can only be updated when the D-PHY lane is in the Stop state.

CSI2HOST_CSI2_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	csi2_resetn CSI2 controller reset output. Active low.

CSI2HOST_PHY_STATE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	bypass_2ecc_tst Payload Bypass test mode for double ECC errors.
10	RO	0x0	phy_stopstateclk Clock lane in Stop state.
9	RO	0x0	phy_rxulpsclknot This signal indicates that the clock lane module has entered the Ultra Low Power state. Active low.
8	RO	0x0	phy_rxclkactivehs Indicates that the clock lane is actively receiving a DDR clock.
7	RO	0x0	phy_stopstatedata_3 Data lane 3 in Stop state.
6	RO	0x0	phy_stopstatedata_2 Data lane 2 in Stop state.
5	RO	0x0	phy_stopstatedata_1 Data lane 1 in Stop state.
4	RO	0x0	phy_stopstatedata_0 Data lane 0 in Stop state.
3	RO	0x0	phy_rxulpsesc_3 Lane module0 has entered the Ultra Low Power mode.
2	RO	0x0	phy_rxulpsesc_2 Lane module2 has entered the Ultra Low Power mode.

Bit	Attr	Reset Value	Description
1	RO	0x0	phy_rxulpsesc_1 Lane module1 has entered the Ultra Low Power mode.
0	RO	0x0	phy_rxulpsesc_0 Lane module0 has entered the Ultra Low Power mode.

CSI2HOST_DATA_IDS_1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	di3_vc Data ID 3 virtual channel.
29:24	RW	0x00	di3_dt Data ID 3 data type.
23:22	RW	0x0	di2_vc Data ID 2 virtual channel.
21:16	RW	0x00	di2_dt Data ID 2 data type.
15:14	RW	0x0	di1_vc Data ID 1 virtual channel.
13:8	RW	0x00	di1_dt Data ID 1 data type.
7:6	RW	0x0	di0_vc Data ID 0 virtual channel.
5:0	RW	0x00	di0_dt Data ID 0 data type.

CSI2HOST_DATA_IDS_2

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	di7_vc Data ID 7 virtual channel.
29:24	RW	0x00	di7_dt Data ID 7 data type.
23:22	RW	0x0	di6_vc Data ID 6 virtual channel.
21:16	RW	0x00	di6_dt Data ID 6 data type.
15:14	RW	0x0	di5_vc Data ID 5 virtual channel.
13:8	RW	0x00	di5_dt Data ID 5 data type.
7:6	RW	0x0	di4_vc Data ID 4 virtual channel.
5:0	RW	0x00	di4_dt Data ID 4 data type.

CSI2HOST_ERR1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	err_ph_crc_lane2 Packet crc error of lane2 when sw_cphy_en=1.
30	RW	0x0	err_ph_crc_lane1 Packet crc error of lane1 when sw_cphy_en=1.
29	RW	0x0	err_ph_crc_lane0 Packet crc error of lane0 when sw_cphy_en=1.

Bit	Attr	Reset Value	Description
28	RO	0x0	err_ecc_double Header ECC contains 2 errors,unrecoverable.
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3.
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2.
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1.
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0.
23:16	RO	0x00	reserved
15	RO	0x0	err_frame_data_vc3 Last received frame,in virtual channel 3,had at least one CRC error.
14	RO	0x0	err_frame_data_vc2 Last received frame,in virtual channel 2,had at least one CRC error.
13	RO	0x0	err_frame_data_vc1 Last received frame,in virtual channel 1,had at least one CRC error.
12	RO	0x0	err_frame_data_vc0 Last received frame,in virtual channel 0,had at least one CRC error.
11	RO	0x0	err_f_seq_vc3 Incorrect frame sequence detected in virtual channel 3.
10	RO	0x0	err_f_seq_vc2 Incorrect frame sequence detected in virtual channel 2.
9	RO	0x0	err_f_seq_vc1 Incorrect frame sequence detected in virtual channel 1.
8	RO	0x0	err_f_seq_vc0 Incorrect frame sequence detected in virtual channel 0.
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3.
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2.
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1.
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0.
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3.
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2.
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1.
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0(no synchronization achieved).

CSI2HOST_ERR2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RW	0x0	phy_errcodehs_3 Lane 3 receiv error code.
26	RW	0x0	phy_errcodehs_2 Lane 2 receiv error code.
25	RW	0x0	phy_errcodehs_1 Lane 1 receiv error code.
24	RW	0x0	phy_errcodehs_0 Lane 0 receiv error code.
23:16	RO	0x00	reserved
15	RW	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3.
14	RW	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2.
13	RW	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1.
12	RW	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0.
11	RW	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3.
10	RW	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2.
9	RW	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1.
8	RW	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0.
7	RW	0x0	phy_errsoths_3 Start of transmission error on data lane 3(synchronization can still be achieved).
6	RW	0x0	phy_errsoths_2 Start of transmission error on data lane 2(synchronization can still be achieved).
5	RW	0x0	phy_errsoths_1 Start of transmission error on data lane 1(synchronization can still be achieved).
4	RW	0x0	phy_errsoths_0 Start of transmission error on data lane 0(synchronization can still be achieved).
3	RW	0x0	phy_erresc_3 Escape entry error(ULPM) on data lane 3.
2	RW	0x0	phy_erresc_2 Escape entry error(ULPM) on data lane 2.
1	RW	0x0	phy_erresc_1 Escape entry error(ULPM) on data lane 1.
0	RW	0x0	phy_erresc_0 Escape entry error(ULPM) on data lane 0.

CSI2HOST_MSK1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31	RW	0x0	mask_err_ph_crc_lane2 Mask for err_ph_crc_lane2.
30	RW	0x0	mask_err_ph_crc_lane1 Mask for err_ph_crc_lane1.
29	RW	0x0	mask_err_ph_crc_lane0 Mask for err_ph_crc_lane0.
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double.
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc.
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc.
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc.
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3.
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2.
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1.
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0.
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3.
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2.
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1.
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0.
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc3.
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc2.
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1.
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0.
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3.
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2.
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1.
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0.

CSI2HOST_MSK2

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27	RW	0x0	mask_phy_errcodehs_3 Mask for phy_errcodehs_3.
26	RW	0x0	mask_phy_errcodehs_2 Mask for phy_errcodehs_2.
25	RW	0x0	mask_phy_errcodehs_1 Mask for phy_errcodehs_1.
24	RW	0x0	mask_phy_errcodehs_0 Mask for phy_errcodehs_0.
23:16	RO	0x00	reserved
15	RW	0x0	mask_err_id_vc3 Mask for err_id_vc3.
14	RW	0x0	mask_err_id_vc2 Mask for err_id_vc2.
13	RW	0x0	mask_err_id_vc1 Mask for err_id_vc1.
12	RW	0x0	mask_err_id_vc0 Mask for err_id_vc0.
11	RW	0x0	mask_vc3_err_ecc_corrected Mask for vc3_err_ecc_corrected.
10	RW	0x0	mask_vc2_err_ecc_corrected Mask for vc2_err_ecc_corrected.
9	RW	0x0	mask_vc1_err_ecc_corrected Mask for vc1_err_ecc_corrected.
8	RW	0x0	mask_vc0_err_ecc_corrected Mask for vc0_err_ecc_corrected.
7	RW	0x0	mask_phy_errsoths_3 Mask for phy_errsoths_3.
6	RW	0x0	mask_phy_errsoths_2 Mask for phy_errsoths_2.
5	RW	0x0	mask_phy_errsoths_1 Mask for phy_errsoths_1
4	RW	0x0	mask_phy_errsoths_0 Mask for phy_errsoths_0.
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3.
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2.
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1.
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0.

CSI2HOST_CONTROL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RW	0x03	sw_datatype_le The datatype of line end.
25:20	RW	0x02	sw_datatype_ls The datatype of line start.
19:14	RW	0x01	sw_datatype_fe The datatype of frame end.
13:8	RW	0x00	sw_datatype_fs The datatype of frame start.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	sw_dsi_en 1'b0: For csi2 1'b1: For dsi
3:1	RO	0x0	reserved
0	RW	0x0	sw_cphy_en 1'b0: For dphy 1'b1: For cphy

27.5 Application Notes

The most important step is configuring the right CSI2HOST_N_LANES before pulling up csi_resetn. If the host is used to receive DSI data, the sw_dsi_en must be enabled, and the sw_datatype_fs, sw_datatype_fe, sw_datatype_ls, sw_datatype_le must be configured correctly. When the sw_dsi_en is enabled, those debug or error detection registers are useless.

Chapter 28 MIPI CSI DPHY

28.1 Overview

The features of MIPI CSI DPHY are as follow:

- Analog mixed-signal hard-macro LP/HS Receiver solution
- Designed to MIPI v1.2 Specifications
- Integrated PHY Protocol Interface(PPI) interfaces to DSI/CSI and UniPro MIPI protocols
- 2.5 Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 10 Gbps transfer rate
- HS-RX, LP-RX, LP-TX and Calibration supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- LOW-Power dissipation: less than 1.5mA/Lane in D-PHY HS RX mode
- Buffers with tunable On-Die-Termination
- Includes embedded ESD, boundary scan and BIST
- Dual clock lanes mode supported

28.2 Block Diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the 'Control and Interface Logic'(CIL) function depend on the Lane type and Lane side.

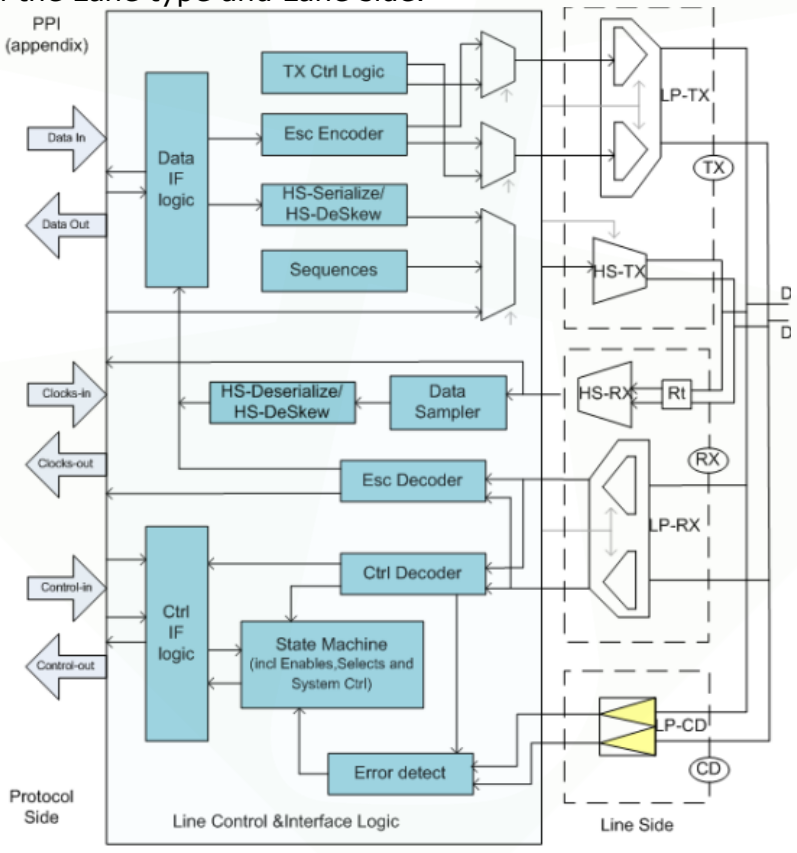


Fig. 28-1 MIPI CSI DPHY Block Diagram

28.3 Register Description

28.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

28.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DPHYRX_LANE_EN	0x0000	W	0x00000000	Clk/data lane enable
DPHYRX_DIGITAL_CLK_PHASE	0x0034	W	0x00000000	Digital clock phase
DPHYRX_LANE_CLK_3_PHASE	0x0038	W	0x00000000	Lane clock/3 phase
DPHYRX_LANE_2_1_0_PHASE	0x003C	W	0x00000000	Data lane 2/1/0 phase
DPHYRX_DIGITAL_CLK_REVERSE	0x0048	W	0x00000000	Digital clock reverse
DPHYRX_DUAL_CLK_ENABLE	0x0080	W	0x00000001	MIPI/LVDS enable
DPHYRX_LANE_CK_MODE	0x0128	W	0x00000000	Clock lane mode
DPHYRX_LANE_CK_MSB	0x0138	W	0x00000000	MSB enable
DPHYRX_LANE_CK_TTAGO	0x0140	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_CK_TTASURE	0x0144	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_CK_TTAWAIT	0x0148	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_CK_THSSETTLE	0x0160	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_CK_CAL_EN	0x0168	W	0x00000000	Calibration reception enable
DPHYRX_LANE_0_MSB	0x01B8	W	0x00000000	MSB enable
DPHYRX_LANE_0_TTAGO	0x01C0	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_0_TTASURE	0x01C4	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_0_TTAWAIT	0x01C8	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_0_THSSETTLE	0x01E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_0_CAL_EN	0x01E8	W	0x00000000	Calibration reception enable
DPHYRX_LANE_1_MSB	0x0238	W	0x00000000	MSB enable
DPHYRX_LANE_1_TTAGO	0x0240	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_1_TTASURE	0x0244	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_1_TTAWAIT	0x0248	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_1_THSSETTLE	0x0260	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_1_CAL_EN	0x0268	W	0x00000000	Calibration reception enable
DPHYRX_LANE_2_MSB	0x02B8	W	0x00000000	MSB enable
DPHYRX_LANE_2_TTAGO	0x02C0	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_2_TTASURE	0x02C4	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_2_TTAWAIT	0x02C8	W	0x00000032	The value of counter for Tta-wait of turnaround

Name	Offset	Size	Reset Value	Description
DPHYRX_LANE_2_THSSETTLE	0x02E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_2_CAL_EN	0x02E8	W	0x00000000	Calibration reception enable
DPHYRX_LANE_3_MSB	0x0338	W	0x00000000	MSB enable
DPHYRX_LANE_3_TTAGO	0x0340	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_3_TTASURE	0x0344	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_3_TTAWAIT	0x0348	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_3_THSSETTLE	0x0360	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_3_CAL_EN	0x0368	W	0x00000000	Calibration reception enable
DPHYRX_LANE_CK1_MODE	0x03A8	W	0x00000000	Clock lane1 mode
DPHYRX_LANE_CK1_MSB	0x03B8	W	0x00000000	MSB enable
DPHYRX_LANE_CK1_TTAGO	0x03C0	W	0x00000004	The value of counter for Tta-go of turnaround
DPHYRX_LANE_CK1_TTASURE	0x03C4	W	0x00000001	The value of counter for Tta-sure of turnaround
DPHYRX_LANE_CK1_TTAWAIT	0x03C8	W	0x00000032	The value of counter for Tta-wait of turnaround
DPHYRX_LANE_CK1_THSSETTLE	0x03E0	W	0x0000001B	The count time of the THS-SETTLE by protocol
DPHYRX_LANE_CK1_CAL_EN	0x03E8	W	0x00000000	Calibration reception enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

28.3.3 Detail Registers Description

DPHYRX_LANE_EN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_en_ck Enable D-PHY clock lane:active high.
5	RW	0x0	lane_en_3 Enable D-PHY lane3:active high.
4	RW	0x0	lane_en_2 Enable D-PHY lane2:active high.
3	RW	0x0	lane_en_1 Enable D-PHY lane1:active high.
2	RW	0x0	lane_en_0 Enable D-PHY lane0:active high.
1:0	RO	0x0	reserved

DPHYRX_DIGITAL_CLK_PHASE

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	digital_clk_phase 3'b000: Phase 0(default value) 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

DPHYRX_LANE_CLK_3_PHASE

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	lane_clk_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
3:1	RW	0x0	lane_3_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
0	RW	0x0	lane_2_phase_msb See lane_2_phase for the details of the register.

DPHYRX_LANE_2_1_0_PHASE

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	lane_2_phase {lane_2_phase_msb,lane_2_phase} 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
5:3	RW	0x0	lane_1_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.
2:0	RW	0x0	lane_0_phase 3'b000: Phase 0 3'b001: Phase 1 3'b010: Phase 2 3'b011: Phase 3(default value) 3'b100: Phase 4 3'b101: Phase 5 3'b110: Phase 6 3'b111: Phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.

DPHYRX_DIGITAL_CLK_REVERSE

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	digital_clk_reverse 1'b0: Make the digital sample clock positive(default value) 1'b1: Reverse the digital sample clock
6:0	RO	0x00	reserved

DPHYRX_DUAL_CLK_ENABLE

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dual_clk_mode_en 1'b0: Enable single clock lane mode 1'b1: Enable dual clock lanes mode
5:1	RO	0x00	reserved
0	RW	0x1	reg_dig_rstn 1'b0: Reset 1'b1: Normal

DPHYRX_LANE_CK_MODE

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

DPHYRX_LANE_CK_MSB

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_ck_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_CK_TTAGO

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_CK_TTASURE

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_CK_TTAWAIT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_CK_THSSETTLE

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_ck_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_CK_CAL_EN

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

DPHYRX_LANE_0_MSB

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_0_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_0_TTAGO

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_0_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_0_TTASURE

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_0_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_0_TTAWAIT

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_0_THSSETTLE

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_0_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_0_CAL_EN

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_0_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

DPHYRX_LANE_1_MSB

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_1_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_1_TTAGO

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_1_TTASURE

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_1_TTAWAIT

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_1_THSSETTLE

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_1_CAL_EN

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

DPHYRX_LANE_2_MSB

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_2_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_2_TTAGO

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_2_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_2_TTASURE

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_2_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_2_TTAWAIT

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_2_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_2_THSSETTLE

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_2_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_2_CAL_EN

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_2_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

DPHYRX_LANE_3_MSB

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_3_msb MSB enable for pin_rxdatahs_*. 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_3_TTAGO

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_3_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_3_TTASURE

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_3_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_3_TTAWAIT

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_0_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_3_THSSETTLE

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x1b	lane_3_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_3_CAL_EN

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_3_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

DPHYRX_LANE_CK1_MODE

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	lane_ck1_mode 2'b00: Disable continuous clock mode 2'b11: Enable continuous clock mode
3:0	RO	0x0	reserved

DPHYRX_LANE_CK1_MSB

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	lane_ck1_msb MSB enable for pin_rxdatahs_* 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

DPHYRX_LANE_CK1_TTAGO

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x04	lane_ck1_ttago The value of counter for Tta-go of turnaround. Tta-go = Ttxclkesc*value.

DPHYRX_LANE_CK1_TTASURE

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x01	lane_ck1_ttasure The value of counter for Tta-sure of turnaround. Tta-sure = Ttxclkesc*value.

DPHYRX_LANE_CK1_TTAWAIT

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x32	lane_ck1_ttawait The value of counter for Tta-wait of turnaround. Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value.

DPHYRX_LANE_CK1_THSSETTLE

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1b	lane_ck1_thssettle The count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. Frequency(1/UI) Value(HEX) 80-110MHz 02 110-150MHz 03 150-200MHz 06 200-250MHz 06 250-300MHz 06 300-400MHz 08 400-500MHz 0b 500-600MHz 0e 600-700MHz 10 700-800MHz 12 800-1000MHz 16 1000-1200MHz 1e 1200-1400MHz 23 1400-1600MHz 2d 1600-1800MHz 32 1800-2000MHz 37 2000-2200MHz 3c 2200-2400MHz 41 2400-2500MHz 46

DPHYRX_LANE_CK1_CAL_EN

Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lane_ck1_cal_en Calibration reception enable. 1'b0: Disable calibration reception 1'b1: Enable calibration reception
6:0	RO	0x00	reserved

28.4 Application Notes

28.4.1 MIPI SINGLE CLOCK LANE Mode Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x01f001f0 to register GRF_VI_CON0.Enable the clock lane and 4 data lanes.
step3: According to data rate, write corresponding value to Ths-settle registers for lanes.

28.4.2 MIPI DUAL CLOCK LANES MODE Application

step1: send 0x7d to register LANE_EN. Enable the D-PHY.
step2: send 0x5f to register DUAL_CLK_ENABLE.Enable dual clock lanes mode.
step3: send 0x05f005f0 to register GRF_VI_CON0.Enable 2 clock lanes and 4 data lanes.
step4: According to data rate, write corresponding value to Ths-settle registers for lanes.

In dual clock lanes mode,GRF_VI_CON1 must be configured according to the following table.

	LANE0/1	LANE2/3	GRF_VI_CON1 VALUE
Connected IP	ISP	CSI2HOST	0x08800880
	CSI2HOST	ISP	0x10801080
	ISP、CSI2HOST		0x00800080
		ISP、CSI2HOST	0x18801880

Chapter 29 MIPI DSI HOST Controller

29.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI DSI HOST Controller supports the following features:

- The MIPI DSI HOST Controller conforms to the following standards
  - MIPI Alliance Specification for DSI v1.1
  - MIPI Alliance Specification for DCS v1.1
  - MIPI Alliance Standard for DPI-2
  - MIPI Alliance Specification for SDF v1.0
  - MIPI Alliance Specification for DPHY v1.2
  - AMBA 2.0 Specification(APB) from ARM
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Maximum resolution is 1920x1080@60Hz
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands

- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

29.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

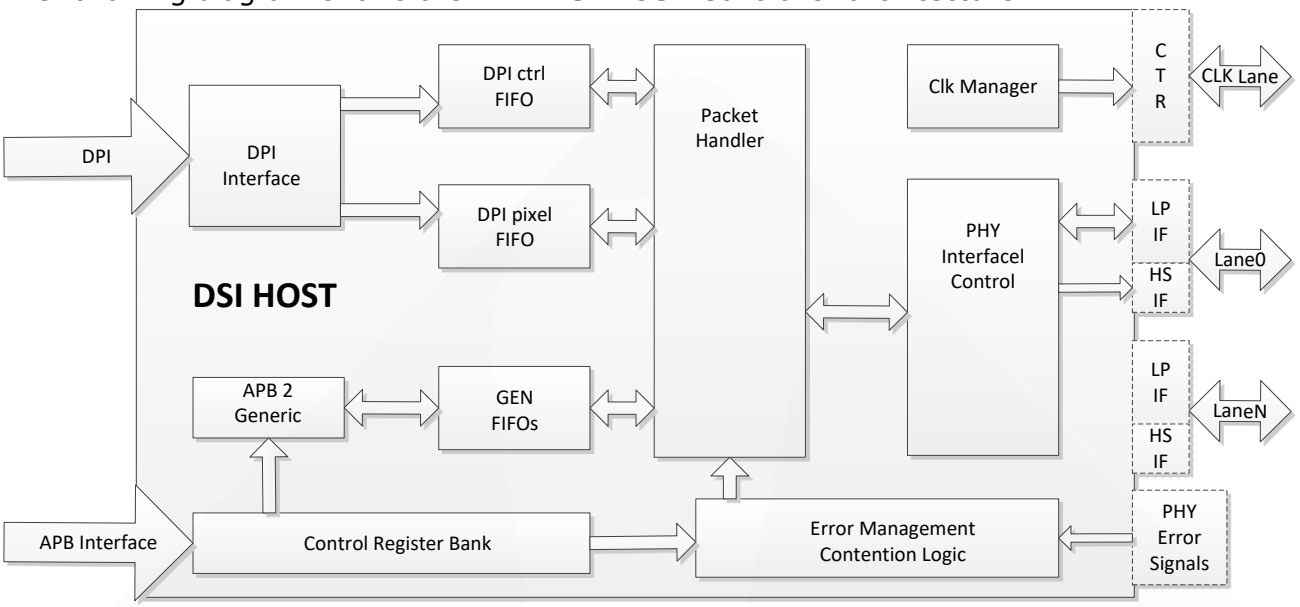


Fig. 29-1 MIPI DSI HOST Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.
The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFO: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

29.3 Function Description

29.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of VO_CON[9:8] in the GRF Module. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 29-1 Color table

Signal Line	**16-bit**			**18-bit**		**24bit**
Config	**Config1**	**Config2**	**Config3**	**Config1**	**Config2**	**Config1**
Dpidata23	Not used	Not used	Not used	Not used	Not used	R7
Dpidata22	Not used	Not used	Not used	Not used	Not used	R6
Dpidata21	Not used	Not used	R4	Not used	R5	R5
Dpidata20	Not used	R4	R3	Not used	R4	R4
Dpidata19	Not used	R3	R2	Not used	R3	R3
Dpidata18	Not used	R2	R1	Not used	R2	R2
Dpidata17	Not used	R1	R0	R5	R1	R1
Dpidata16	Not used	R0	Not used	R4	R0	R0
Dpidata15	R4	Not used	Not used	R3	Not used	G7
Dpidata14	G3	Not used	Not used	G2	Not used	G6
Dpidata13	G2	G5	G5	G1	G5	G5
Dpidata12	G1	G4	G4	G0	G4	G4
Dpidata11	G0	G3	G3	G5	G3	G3
Dpidata10	G5	G2	G2	G4	G2	G2
Dpidata9	G4	G1	G1	G3	G1	G1
Dpidata8	G3	G0	G0	G2	G0	G0
Dpidata7	G2	Not used	Not used	G1	Not used	B7
Dpidata6	G1	Not used	Not used	G0	Not used	B6
Dpidata5	G0	Not used	B4	B5	B5	B5
Dpidata4	B4	B4	B3	B4	B4	B4
Dpidata3	B3	B3	B2	B3	B3	B3
Dpidata2	B2	B2	B1	B2	B2	B2
Dpidata1	B1	B1	B0	B1	B1	B1
Dpidata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

29.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation.

Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.

The valid packets available to be transmitted through the Generic interface are as follows:
- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.
The transfer of packets through the APB bus is based on the following conditions:
The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB interface.
The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps.
The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.

To drive the APB interface to achieve high bandwidth Command mode traffic transported by

the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.

The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus.

After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figure show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams.In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

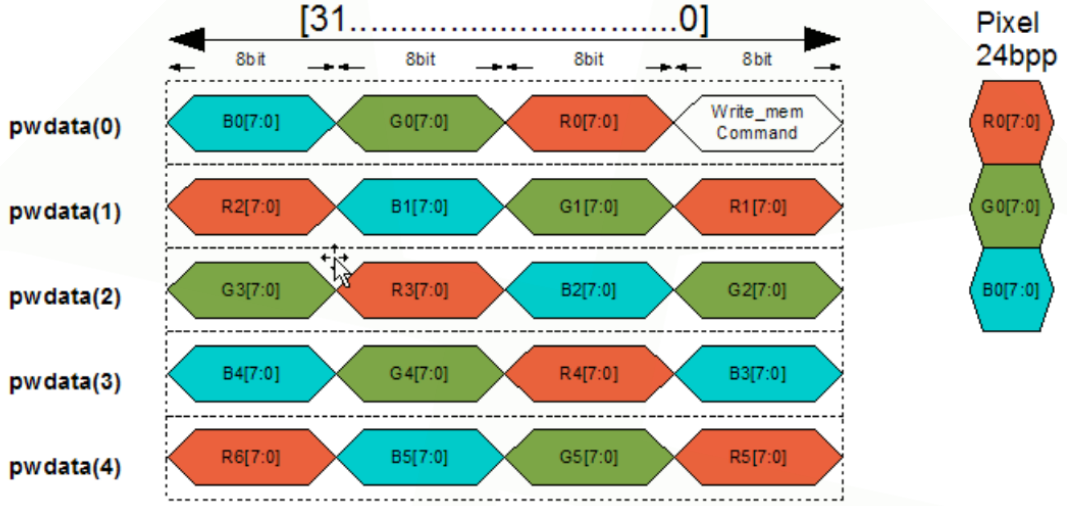


Fig 1-2 24 bpp APB Pixel to Byte Organization

29.3.3 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

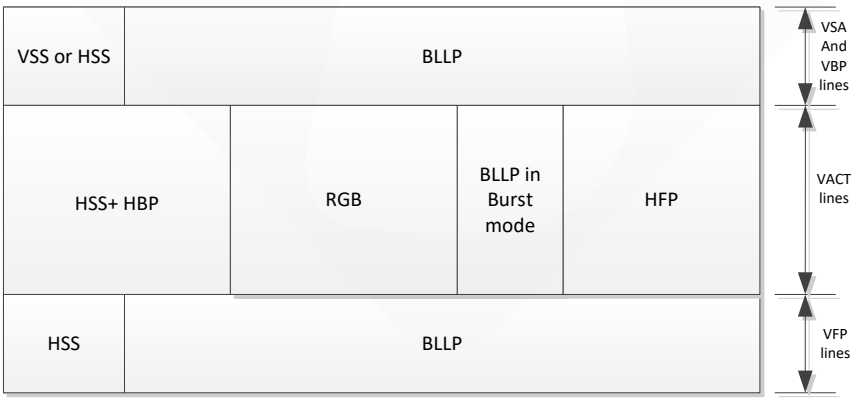


Fig. 29-3 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled

- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) * (number of lines -1) shorter than tL.

The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.

If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.

The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP
Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2
Where, tL=Line time, and tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses).

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.

The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.

Consider an example with 12.6 μs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:

- Sync pulses are not being transmitted
- Two lane byte clock ticks are required to transmit a short packet

$$phy\_lp2hs\_time = 16$$
$$phy\_lp2p\_time = 20$$

In this example, a 11-byte command can be transmitted as follows:

$$outvact\_lpcmd\_time = 11bytes$$

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:
Invact_lpcmd_time=((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape clock period) / 8. Where,

$$tHFP = line\_time - tHSA - tHBP - tHACT$$

tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes
The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.

Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6µs. With a lane byte clock of 100 MHz, 1260 clock ticks are available to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6µs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3µs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.

A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode:

$$phy\_lp2hs\_time = 16$$

In this example invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3µs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.
Following figure illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

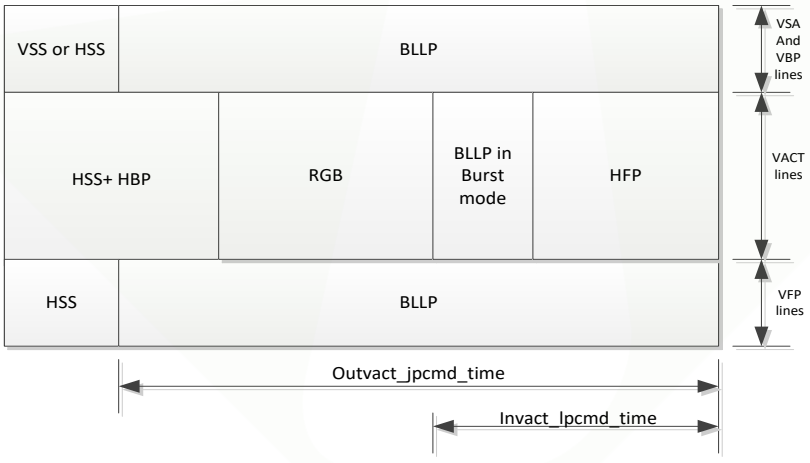


Fig. 29-4 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is required.

On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.

The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.
The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time
In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time
Where,
LPDT command time = (8*Host escape clock period) / Lane byte clock period
Read command time in LP mode = (32 * host escape clock period) / lane byte clock period
It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.

Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (＞16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

29.4 Register Description

29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

29.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VERSION	0x0000	W	0x3133302a	Version
MIPI_DSI_HOST_PWR_UP	0x0004	W	0x00000000	Power up
MIPI_DSI_HOST_CLKMGR_CFG	0x0008	W	0x00000000	Configure the factor of the internal dividers to divide lanebyteclk
MIPI_DSI_HOST_DPI_VCID	0x000c	W	0x00000000	DPI virtual channel id
MIPI_DSI_HOST_DPI_COLOR_CODING	0x0010	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_CFG_POL	0x0014	W	0x00000000	Polarity of the DPI signals
MIPI_DSI_HOST_DPI_LP_CMD_TIM	0x0018	W	0x00000000	The timing for the low-power command while in video mode

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_PCKHDL_CFG	0x002c	W	0x00000000	Configures how EoTp,BTA,CRC and ECC are to be used , to meet the peripheral's characteristics
MIPI_DSI_HOST_GEN_VCID	0x0030	W	0x00000000	The virtual channel id of the read responses to store and return to the Generic interface
MIPI_DSI_HOST_MODE_CFG	0x0034	W	0x00000001	This register configures the mode of operation - Video mode or Command mode(Commands can be sent even in video mode too)
MIPI_DSI_HOST_VID_MODE_CFG	0x0038	W	0x00000000	Configure several aspects of the Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE	0x003c	W	0x00000000	The video packet size
MIPI_DSI_HOST_VID_NUM_CHUNKS	0x0040	W	0x00000000	The number of chunks to use
MIPI_DSI_HOST_VID_NULL_SIZE	0x0044	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME	0x0048	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME	0x004c	W	0x00000000	HBP time
MIPI_DSI_HOST_VID_HLINE_TIME	0x0050	W	0x00000000	The overall time for video line
MIPI_DSI_HOST_VID_VSA_LINES	0x0054	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES	0x0058	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES	0x005c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES	0x0060	W	0x00000000	The vertical resolution of the video
MIPI_DSI_HOST_EDPI_CMD_SIZE	0x0064	W	0x00000000	The size of eDPI packet
MIPI_DSI_HOST_CMD_MODE_CFG	0x0068	W	0x00000000	Configure several aspects of the command mode operation
MIPI_DSI_HOST_GEN_HDR	0x006c	W	0x00000000	Set the header for new packets sent using the Generic interface
MIPI_DSI_HOST_GEN_PLD_DATA	0x0070	W	0x00000000	The payload for the packet sent using the Generic interface
MIPI_DSI_HOST_CMD_PKT_STATUS	0x0074	W	0x00000000	The status of FIFOs related to the Generic interface
MIPI_DSI_HOST_TO_CNT_CFG	0x0078	W	0x00000000	The counters that trigger the timeout error

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_HS_RD_TO_CNT	0x007c	W	0x00000000	The Peripheral Response timeout after high-speed read operation
MIPI_DSI_HOST_LP_RD_TO_CNT	0x0080	W	0x00000000	The Peripheral Response timeout after low-power read operation
MIPI_DSI_HOST_HS_WR_TO_CNT	0x0084	W	0x00000000	The Peripheral Response timeout after high-speed write operation
MIPI_DSI_HOST_LP_WR_TO_CNT	0x0088	W	0x00000000	The Peripheral Response timeout after low-power write operation
MIPI_DSI_HOST_BTA_TO_CNT	0x008c	W	0x00000000	The Peripheral Response timeout after the Bus Turnaround completion
MIPI_DSI_HOST_SDF_3D	0x0090	W	0x00000000	The 3D control information for VSS Packets in video mode
MIPI_DSI_HOST_LPCLK_CTRL	0x0094	W	0x00000000	Using non-continuous clock in the clock lane
MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG	0x0098	W	0x00000000	Set the time that the HOST assumes in calculations for the clock lane to switch between high-speed and low-power
MIPI_DSI_HOST_PHY_TMR_CFG	0x009c	W	0x00000000	Set the time that the HOST assumes in calculations for the data lanes to switch between high-speed and low-power
MIPI_DSI_HOST_PHY_RSTZ	0x00a0	W	0x00000000	The reset of the PLL and DPHY
MIPI_DSI_HOST_PHY_IF_CFG	0x00a4	W	0x00000003	The minimum time to remain in Stop state
MIPI_DSI_HOST_PHY_STATUS	0x00b0	W	0x00000000	The DPHY status
MIPI_DSI_HOST_INT_ST0	0x00bc	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_ST1	0x00c0	W	0x00000000	The status of the interrupt sources
MIPI_DSI_HOST_INT_MSK0	0x00c4	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_MSK1	0x00c8	W	0x00000000	The masks of interrupt sources
MIPI_DSI_HOST_INT_FORCE0	0x00d8	W	0x00000000	Force interrupts
MIPI_DSI_HOST_INT_FORCE1	0x00dc	W	0x00000000	Force interrupts
MIPI_DSI_HOST_VID_SHADOW_CTRL	0x0100	W	0x00000000	Control the DPI shadow register

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_DPI_VCID_ACT	0x010c	W	0x00000000	The virtual channel id for the DPI traffic
MIPI_DSI_HOST_DPI_COLOR_CODING_ACT	0x0110	W	0x00000000	DPI color coding
MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT	0x0118	W	0x00000000	The timing for low-power commands sent while in Video mode
MIPI_DSI_HOST_VID_MODE_CFG_ACT	0x0138	W	0x00000000	Configure several aspects of Video mode operation
MIPI_DSI_HOST_VID_PKT_SIZE_ACT	0x013c	W	0x00000000	Configure the video packet size
MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT	0x0140	W	0x00000000	Configure the number of chunks to use
MIPI_DSI_HOST_VID_NULL_SIZE_ACT	0x0144	W	0x00000000	The size of null packets
MIPI_DSI_HOST_VID_HSA_TIME_ACT	0x0148	W	0x00000000	HSA time
MIPI_DSI_HOST_VID_HBP_TIME_ACT	0x014c	W	0x00000000	HBP time
MIPI_DSI_HOST_VID_HLINE_TIME_ACT	0x0150	W	0x00000000	The overall time for each video line
MIPI_DSI_HOST_VID_VSA_LINES_ACT	0x0154	W	0x00000000	VSA period
MIPI_DSI_HOST_VID_VBP_LINES_ACT	0x0158	W	0x00000000	VBP period
MIPI_DSI_HOST_VID_VFP_LINES_ACT	0x015c	W	0x00000000	VFP period
MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT	0x0160	W	0x00000000	The vertical resolution of video
MIPI_DSI_HOST_SDF_3D_ACT	0x0190	W	0x00000000	Store 3D control information for VSS in video mode

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

29.4.3 Detail Register Description

MIPI_DSI_HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x3133302a	version

MIPI_DSI_HOST_PWR_UP

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	shutdownz This bit configures the core either to power up or to reset. Its default value is 0. After the core configuration, to enable the DSI Host Controller, set this register to 1. 1'b0: Reset 1'b1: Power-up

MIPI_DSI_HOST_CLKMGR_CFG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:8	RW	0x00	to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error
7:0	RW	0x00	tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation

MIPI_DSI_HOST_DPI_VCID

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000: 16-bit configuration 1 4'b0001: 16-bit configuration 2 4'b0010: 16-bit configuration 3 4'b0011: 18-bit configuration 1 4'b0100: 18-bit configuration 2 4'b0101: 24-bit 4'b0110: 20-bit YCbCr 4:2:2 loosely packed 4'b0111: 24-bit YCbCr 4:2:2 4'b1000: 16-bit YCbCr 4:2:2 4'b1001: 30-bit 4'b1010: 36-bit 4'b1011-4'b1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_CFG_POL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved
4	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin (dpicolorm) as active low
3	RW	0x0	shutd_active_low When set to 1, this bit configures the shutdown pin (dpishutdn) as active low
2	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low
1	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low
0	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin (dpidataen) as active low

MIPI_DSI_HOST_DPI_LP_CMD_TIM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved
7:0	RW	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_PCKHDL_CFG

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	Reserved
4	RW	0x0	crc_rx_en When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	ecc_rx_en When set to 1, this bit enables the ECC reception, error correction, and reporting
2	RW	0x0	bta_en When set to 1, this bit enables the Bus Turn-Around (BTA) request
1	RW	0x0	eotp_rx_en When set to 1, this bit enables the EoTp reception
0	RW	0x0	eotp_tx_en When set to 1, this bit enables the EoTp transmission

MIPI_DSI_HOST_GEN_VCID

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	gen_vcid_rx This field indicates the Generic interface read-back virtual channel identification

MIPI_DSI_HOST_MODE_CFG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x1	cmd_video_mode This bit configures the operation mode: 1'b0: Video mode 1'b1: Command mode

MIPI_DSI_HOST_VID_MODE_CFG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved
20	RW	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RW	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RW	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RW	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RW	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RW	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RW	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows

Bit	Attr	Reset Value	Description
8	RW	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_EDPI_CMD_SIZE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled

MIPI_DSI_HOST_CMD_MODE_CFG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 1'b0: High-speed 1'b1: Low-power
23:20	RO	0x0	Reserved
19	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
17	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

Bit	Attr	Reset Value	Description
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
15	RO	0x0	Reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

Bit	Attr	Reset Value	Description
8	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
7:2	RO	0x0	Reserved
1	RW	0x0	ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission
0	RW	0x0	tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request

MIPI_DSI_HOST_GEN_HDR

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RW	0x00	gen_wc_msbyte
15:8	RW	0x00	gen_wc_lsbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets
7:6	RW	0x0	gen_vc This field configures the virtual channel id of the header packet
5:0	RW	0x00	gen_dt This field configures the packet data type of the header packet

MIPI_DSI_HOST_GEN_PLD_DATA

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload

MIPI_DSI_HOST_CMD_PKT_STATUS

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	dbi_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
13	RO	0x0	dbi_pld_r_full This bit indicates the full status of the DBI read payload FIFO
12	RO	0x0	dbi_pld_r_empty This bit indicates the empty status of the DBI read payload FIFO
11	RO	0x0	dbi_pld_w_full This bit indicates the full status of the DBI write payload FIFO
10	RO	0x0	dbi_pld_w_empty This bit indicates the empty status of the DBI write payload FIFO
9	RO	0x0	dbi_cmd_full This bit indicates the full status of the DBI command FIFO
8	RO	0x0	dbi_cmd_empy This bit indicates the empty status of the DBI command FIFO
7	RO	0x0	Reserved
6	RO	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
5	RO	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO

MIPI_DSI_HOST_TO_CNT_CFG

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a can line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in ccordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)
15:0	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles)

MIPI_DSI_HOST_HS_RD_TO_CNT

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_RD_TO_CNT

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_HS_WR_TO_CNT

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	presp_to_mode When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: dpivsync_edpiwms has risen and fallen. Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic or DBI ready to be sent, making it return to stop state. When it does so, PRESP_TO counter is ctivated and only when it finishes does the controller send any other traffic that is ready
23:16	RO	0x0	Reserved
15:0	RW	0x0000	hs_wr_to_cnt This field sets a period for which the DSI Host Controller keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_WR_TO_CNT

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:0	RW	0x0000	lp_wr_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_BTA_TO_CNT

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RW	0x0	bta_to_cnt This field sets a period for which the DSI Host Controller keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_SDF_3D

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	Reserved
5	RW	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RW	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RW	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RW	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

MIPI_DSI_HOST_LPCLK_CTRL

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1	RW	0x0	auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal

MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	Reserved
25:16	RW	0x000	phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles
15:10	RO	0x0	Reserved
9:0	RW	0x000	phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles

MIPI_DSI_HOST_PHY_TMR_CFG

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles
15	RO	0x0	Reserved
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress

MIPI_DSI_HOST_PHY_RSTZ

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	Reserved
3	RW	0x0	phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Dependency: DSI_HOST_FPGA = 0. Otherwise, this bit is Reserved
2	RW	0x0	phy_enableclk When set to1, this bit enables the D-PHY Clock Lane module
1	RW	0x0	phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state
0	RW	0x0	phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state

MIPI_DSI_HOST_PHY_IF_CFG

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Reserved
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state
7:2	RO	0x0	Reserved
1:0	RW	0x3	n_lanes This field configures the number of active data lanes: 2'b00: One data lane (lane 0) 2'b01: Two data lanes (lanes 0 and 1) 2'b10: Three data lanes (lanes 0, 1, and 2) 2'b11: Four data lanes (lanes 0, 1, 2, and 3)

MIPI_DSI_HOST_PHY_STATUS

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12	RO	0x0	phy_ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal
11	RO	0x0	phy_stopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	phy_ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phy_stopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal

Bit	Attr	Reset Value	Description
8	RO	0x0	phy_ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phy_stopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal
6	RO	0x0	phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phy_stopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal
1	RO	0x0	phy_direction This bit indicates the status of phydirection D-PHY signal
0	RO	0x0	phy_lock This bit indicates the status of phylock D-PHY signal

MIPI_DSI_HOST_INT_ST0

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RO	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report

Bit	Attr	Reset Value	Description
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RO	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_ST1

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RO	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RO	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RO	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RO	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RO	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RO	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception

Bit	Attr	Reset Value	Description
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_MSK0

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report

Bit	Attr	Reset Value	Description
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_MSK1

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception

Bit	Attr	Reset Value	Description
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_FORCE0

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	Reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report

Bit	Attr	Reset Value	Description
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the Reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_FORCE1

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception

Bit	Attr	Reset Value	Description
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_VID_SHADOW_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	vid_shadow_pin_req When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored
15:9	RO	0x0	Reserved
8	RW	0x0	vid_shadow_req When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared
7:1	RO	0x0	Reserved
0	RW	0x0	vid_shadow_en When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the id_shadow_req bit, the auxiliary registers are automatically updated

MIPI_DSI_HOST_DPI_VCID_ACT

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	Reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING_ACT

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	Reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	Reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 4'b0000: 16-bit configuration 1 4'b0001: 16-bit configuration 2 4'b0010: 16-bit configuration 3 4'b0011: 18-bit configuration 1 4'b0100: 18-bit configuration 2 4'b0101: 24-bit 4'b0110: 20-bit YCbCr 4:2:2 loosely packed 4'b0111: 24-bit YCbCr 4:2:2 4'b1000: 16-bit YCbCr 4:2:2 4'b1001: 30-bit 4'b1010: 36-bit 4'b1011-4'b1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	Reserved
23:16	RO	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	Reserved
7:0	RO	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_VID_MODE_CFG_ACT

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	Reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 1'b0: Vertical mode 1'b1: Horizontal mode
23:21	RO	0x0	Reserved

Bit	Attr	Reset Value	Description
20	RO	0x0	vpg_mode This field is to select the pattern: 1'b0: Color bar (horizontal or vertical) 1'b1: BER pattern (vertical only)
19:17	RO	0x0	Reserved
16	RO	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RO	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RO	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RO	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RO	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RO	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RO	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RO	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RO	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	Reserved
1:0	RO	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE_ACT
Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RO	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE_ACT

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	Reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME_ACT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RO	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME_ACT

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	Reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME_ACT

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:0	RO	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES_ACT

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RO	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES_ACT

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	Reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES_ACT

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	Reserved
13:0	RO	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_SDF_3D_ACT

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	Reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet

Bit	Attr	Reset Value	Description
15:6	RO	0x0	Reserved
5	RO	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent. 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RO	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RO	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RO	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

29.5 Application Notes

Perform the following steps to configure the DPI packet transmission:

- Step1: Global configuration:
  - Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.
- Step2: Configure the DPI Interface to define how the DPI interface interacts with the controller.
  - Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.
  - Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.
  - Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.
  - Configure vsync_active_low (DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.

- Configure en18_loosely (DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.

- Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.
  - Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.
  - Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.
  - Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.
  - Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DSI Host Controller to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.
    - Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DSI Host Controller.
  - Non-Burst mode: In this mode, the processor uses the partitioning properties of the DSI Host Controller to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b0x.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b00x to enable the transmission of sync pulses.
    - Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b01to enable the transmission of sync events.
    - Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.
    - Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.
    - Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.
    - Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.
    - The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.
    - Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.

- Step4: Define the DPI Horizontal timing configuration as follows:
  - Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DSI Host Controller is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DSI Host Controller can have a number of errors that can cause a malfunction of the video transmission.
  - Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).
  - Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a

period of 8ns). Special attention should be given to the calculation of this parameter.

- Step5: Define the Vertical line configuration:
  - Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.
  - Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.
  - Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.
  - Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

Chapter 30 MIPI_TX_DPHY

30.1 Overview

The MIPI TX DPHY supports up to 2.5Gbps high speed data transmitter, plus a MIPI low-power low speed transceiver that supports data transfer in the bi-directional mode.

Features

- MIPI
  - One clock lane channel and four data channels
  - Designed to MIPI 1.2 specification
  - Data Channel 0: Bi-directional with Low-Power RX(LP-RX) and Low-Power CD(LP-CD)
  - Channel1~4: High-Speed TX(HS-TX) and a low-Power TX(LP-TX)
  - Maximum HS data rate: 2.5Gbps per lane
  - LP operation rate: 10Mbps per lane
  - Skew-Calibration supported
  - Automatic termination control for HS and LP modes
  - Low-Power dissipation: less than 16mW/lane in MIPI HS TX mode
- LVDS
  - Maximum Support data rate: 1.2Gbps per lane

30.2 Function Description

MIPI TX DPHY configuration contains one clock lane module and four data lane modules. Each of these PHY lane modules communicates via two lines to a complementary part at the other side of the lane interconnect.Figure below shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function.

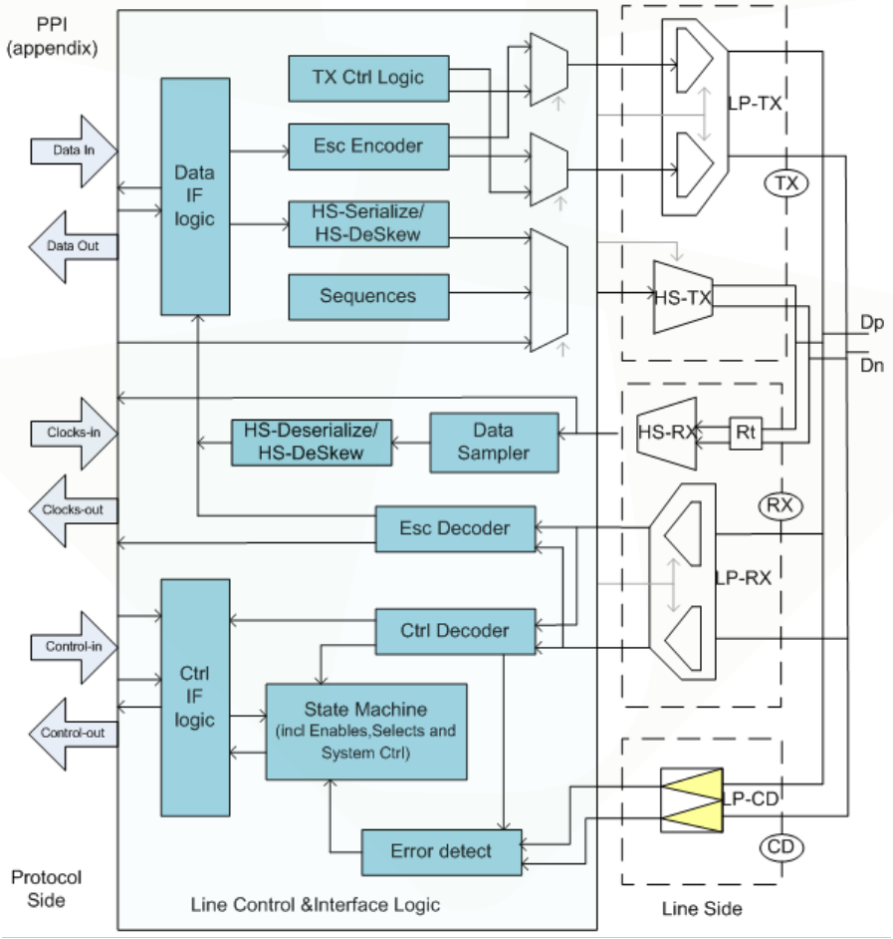


Fig. 30-1 MIPI TX DPHY Architecture

30.2.1 MIPI Mode High Speed Data Transmission

Once the initialization sequence is completed, the TX DPHY remains in control mode. From the transmitter side, high-speed mode is entered when the corresponding txrequesths input

is set high through DSI Host Controller. A burst contains the low-power initialization sequenc, the high-speed data payload,and the end of transmission sequence.

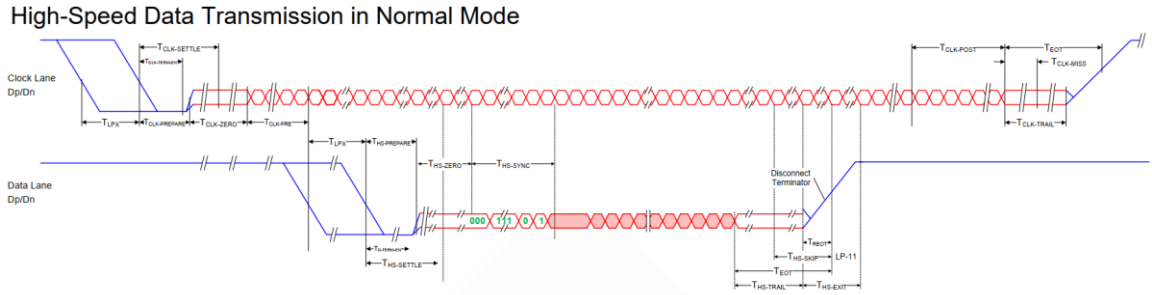


Fig. 30-2 MIPI High Speed Data Transmission in Bursts

30.2.2 LVDS Mode Data Transmission

Figure below shows the LVDS output timing.CLKP is the output clock, whose frequency is the same as the pixel clock. D0P/D0N is a pair differential serial data output.The output serial data is transmitted as MSB first. The rising edge of the output clock is at the transition of bit2 and bit1 of the pin_pdata_*[6:0].

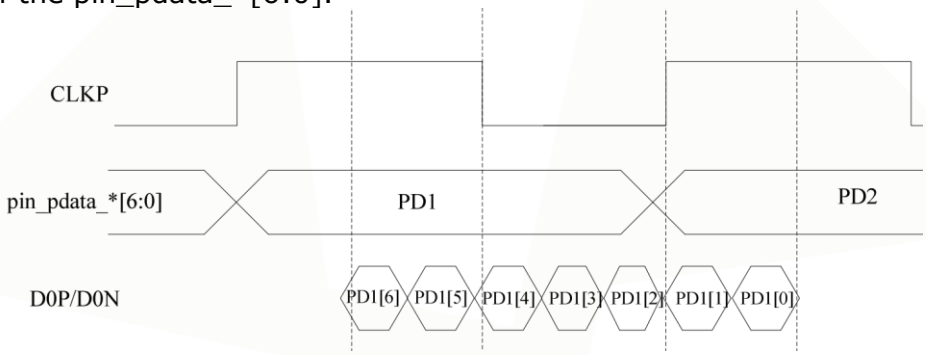


Fig. 30-3 LVDS Data Transmission

30.3 Register Description

30.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

30.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_TX_PHY_ANALOG_REG00	0x0000	B	0x00000001	Power control and lane enable
MIPI_TX_PHY_ANALOG_REG01	0x0001	B	0x000000E3	PLL power control
MIPI_TX_PHY_ANALOG_REG03	0x0003	B	0x00000083	PLL_PREDIV
MIPI_TX_PHY_ANALOG_REG04	0x0004	B	0x000000FA	PLL_FBDIV
MIPI_TX_PHY_ANALOG_REG08	0x0008	B	0x0000004E	PLL post divider
MIPI_TX_PHY_DIGITAL_REG00	0x0020	B	0x0000001F	Digital Reset
MIPI_TX_PHY_DIGITAL_REG01	0x0021	B	0x00000000	Revert clock
MIPI_TX_PHY_LVDS_REG00	0x00E0	B	0x00000045	LVDS MSB mode
MIPI_TX_PHY_LVDS_REG01	0x00E1	B	0x00000012	LVDS digital enable

Name	Offset	Size	Reset Value	Description
MIPI_TX_PHY_LVDS_REG03	0x00E3	B	0x00000001	PHY Mode
MIPI_TX_PHY_LVDS_REG0B	0x00EB	B	0x00000004	LVDS power ctrl and lane enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

30.3.3 Detail Registers Description

MIPI_TX_PHY_ANALOG_REG00

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
7	RW	0x0	bandgap_power bandgap power down enable 1'b1: Power down 1'b0: Power on
6	RW	0x0	lane_en_ck Clock lane enable 1'b1: Enable 1'b0: Disable
5	RW	0x0	lane_en_3 Lane3 enable 1'b1: Enable 1'b0: Disable
4	RW	0x0	lane_en_2 Lane2 enable 1'b1: Enable 1'b0: Disable
3	RW	0x0	lane_en_1 Lane1 enable 1'b1: Enable 1'b0: Disable
2	RW	0x0	lane_en_0 Lane0 enable 1'b1: Enable 1'b0: Disable
1:0	RW	0x1	power 3'b00/3'b01: Power work enable 3'b10: Power work disable 3'b11: Reserved

MIPI_TX_PHY_ANALOG_REG01

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
7:3	RW	0x1c	Reserved Reserved
2	RW	0x0	syncrst 1'b1: Reset 1'b0: Normal
1	RW	0x1	ldopd 1'b1: Power down 1'b0: Power on
0	RW	0x1	pllpd 1'b1: Power down 1'b0: Power on

MIPI_TX_PHY_ANALOG_REG03

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
7:6	RW	0x2	Reserved Reserved
5	RW	0x0	fbdiv_msb Interger value programmed into feedback fbdiv[8]
4:0	RW	0x03	pll_prediv PLL input reference clock divider

MIPI_TX_PHY_ANALOG_REG04

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
7:0	RW	0xfa	pll_fbdiv PLL feedback divider[7:0]

MIPI_TX_PHY_ANALOG_REG08

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
7	RW	0x0	Pre_emphasis Pre-emphasis enable 1'b1: Enable 1'b0: Disable(default)
6	RW	0x1	Reserved Reserved
5	RW	0x0	pll_postdiv 1'b1: Enable 1'b0: Disable
4	RO	0x0	reserved
3:0	RW	0xe	data_lane_vod Data lanes Vod range set 4'h0: Min-range 4'h1: Mid-range 4'h3: Bigger-range(default value) 4'hf: Max-range

MIPI_TX_PHY_DIGITAL_REG00

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
7:1	RW	0x0f	Reserved Reserved
0	RW	0x1	dig_rstn PHY digital logic reset 1'b1: Normal 1'b0: Reset

MIPI_TX_PHY_DIGITAL_REG01

Address: Operational Base + offset (0x0021)

Bit	Attr	Reset Value	Description
7:2	RO	0x0	reserved
1	RW	0x0	txclkesc_revert Inverting pin_txclkesc enable 1'b1: Enable 1'b0: Disable

Bit	Attr	Reset Value	Description
0	RW	0x0	txbyteclk_revert Inverting pin_txbyteclkhs enable 1'b1: Enable 1'b0: Disable

MIPI_TX_PHY_LVDS_REG00

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
7:3	RW	0x08	Reserved Reserved
2	RW	0x1	lvds_digital_reset Digital internal reset 1'b1: Normal(default) 1'b0: Reset
1	RO	0x0	reserved
0	RW	0x1	msb_mode Selection for MSB and LSB 1'b1: MSB 1'b0: LSB

MIPI_TX_PHY_LVDS_REG01

Address: Operational Base + offset (0x00E1)

Bit	Attr	Reset Value	Description
7	RW	0x0	lvds_dig_internal_enable lvds_dig_internal_enable 1'b1: Active 1'b0: Off
6:0	RW	0x12	Reserved Reserved

MIPI_TX_PHY_LVDS_REG03

Address: Operational Base + offset (0x00E3)

Bit	Attr	Reset Value	Description
7:3	RW	0x00	Reserved Reserved
2	RW	0x0	ttl_mode_enable TTL mode enable 1'b1: Enable TTL Mode 1'b0: Disable
1	RW	0x0	lvds_mode_enable LVDS mode enable 1'b1: Enable LVDS Mode 1'b0: Disable
0	RW	0x1	mipi_mode_enable MIPI mode enable 1'b1: Enable MIPI Mode 1'b0: Disable

MIPI_TX_PHY_LVDS_REG0B

Address: Operational Base + offset (0x00EB)

Bit	Attr	Reset Value	Description
7	RW	0x0	lane_en_0 Lane0 enable LVDS mode 1'b1: Enable 1'b0: Disable

Bit	Attr	Reset Value	Description
6	RW	0x0	lane_en_1 Lane1 enable LVDS mode 1'b1: Enable 1'b0: Disable
5	RW	0x0	lane_en_2 Lane2 enable LVDS mode 1'b1: Enable 1'b0: Disable
4	RW	0x0	lane_en_3 Lane3 enable for LVDS mode 1'b1: Enable 1'b0: Disable
3	RW	0x0	lane_en_ck Clock lane enable for LVDS mode 1'b1: Enable 1'b0: Disable
2	RW	0x1	power PLL power for LVDS mode 1'b1: Power off 1'b0: Power on
1:0	RO	0x0	reserved

30.4 Application Notes

30.4.1 MIPI Mode Initialization

Setup Steps:

1. After power on and reset done, set the pin_enable_ck/0/1/2/3 of lanes to be used to high level and the others to low.

2. Send 8'h02 to register 8'h03. Configure PLL PREDIV.

3. Send 8'h53 to register 8'h04. Configure PLL FBDIV.

4. If disable post-divider, send 8'h4e to register 8'h08. Configure PLL POSTDIV.

5. Send 8'he4 to register 8'h01. Enable PLL and LDO.

6. Send 8'h7d to register 8'h00. Enable all lanes on analog part, enable power work, bandgap power on.

7. Send 8'he0 to register 8'h01.Reset analog.

8. Wait a period after analog has been reset.

9. Send 8'h1e to register 8'h20.Reset digital.

10. Send 8'h1f to register 8'h20.Reset digital.

11. Wait some interbal until PLL locked.

30.4.2 LVDS Mode Initialization

1. Set forcerxmode = 1 through *GRF VO_CON2*(for TX DPHY0) register.

2. Configure PLL.Write 8'h01 to the register 8'h03.Write 8'h0e to the register 8'h04.

3. Select LSB mode, default MSB mode. Write 8'h44 to the register 8'he0.(Optional)

4. Enable LVDS digital logic.Write 8'h92 to the register 8'he1.

5. Enable LVDS analog driver.Write 8'hf8 to the register 8'heb.

6. Select LVDS mode.Write 8'h02 to the register 8'he3.

7. Wait a period until PLL locked.

30.4.3 Programmable PLL

The TX DPHY PLL output frequency can be calculated using a sample formula:

$$PLL\_OUTPUT\_FREQUENCY = \frac{((\frac{FREF}{PREDIV}) \times FBDIV)}{POSTDIV}$$

Where PLL_OUTPUT_FREQUENCY equals to the (DDR-Clock-Frequence * 2)
FREF: PLL input reference frequency , 24Mhz.
PREDIV: PLL input reference clock divider which can be configured by the register of reg_prediv.
FBDIV: Integer value programmed into feedback divider which can configured by the register of reg_fbdiv.
POSTDIV: PLL post-divider 2 can be configured by the registers of reg_postdiv.If reg_postdiv is set to 1 , the POSTDIV value is 2. Otherwise, the value is 1.

Chapter 31 EDP TX Controller

31.1 Overview

This eDP TX Controller is compliant with DisplayPort standard 1.2a and eDP 1.3. DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and consumer electronics (CE) industries. It consolidates the internal and external connection methods to reduce device complexity and cost, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

EDP TX Controller supports the following features:

- Compliant with DisplayPort™ Specification, Version 1.2
- Compliant with eDP™ Specification, Version 1.3
- Main link containing 4 physical lanes of 2.7/1.62 Gbps/lane
- Bi-directional auxiliary link with up to 1Mbps speed
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format
- Support HDCP v1.3, integrated HDCP encryption engine for transmitting protected audio and video content
- Support I2S audio interface, the maximum number of channels is 8
- Support S/PDIF audio interface
- 24 Mhz crystal clock
- PRBS or programmable transmitter pattern for main link quality test
- Hot plug and unplug detection and link status monitor

31.2 Block Diagram

EDP TX Controller comprises with:

- Video data capture
- Audio data capture
- DP transmitter

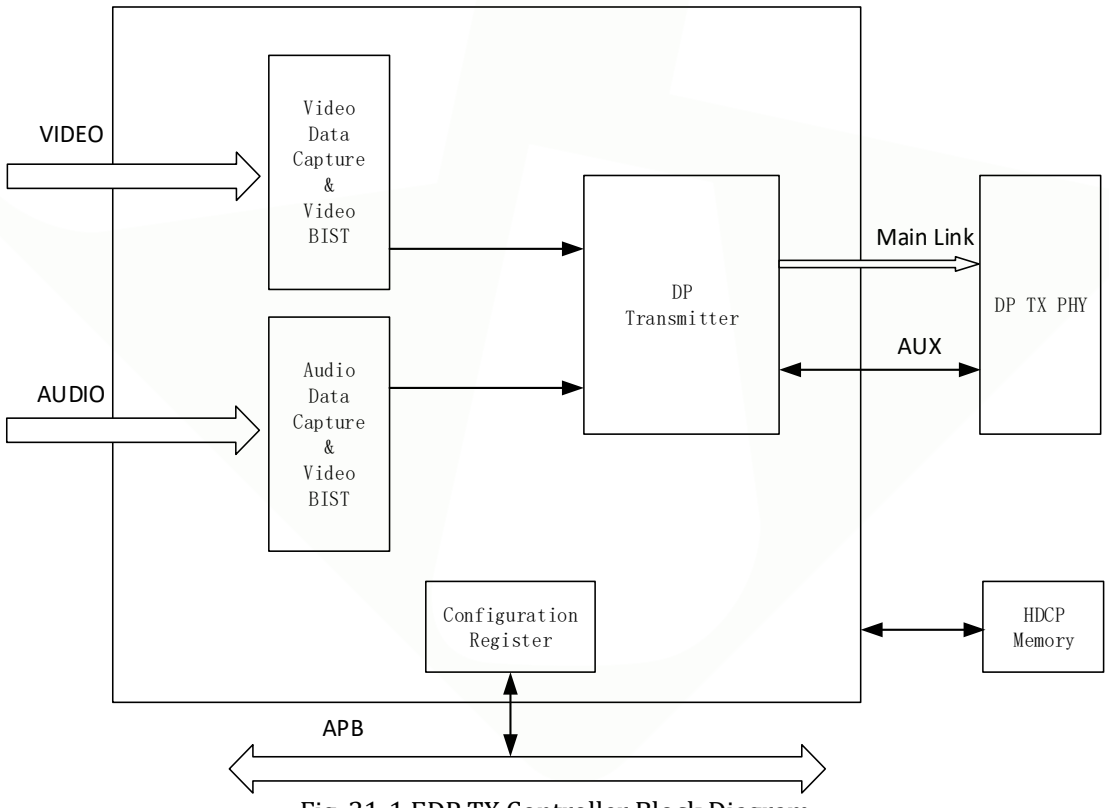


Fig. 31-1 EDP TX Controller Block Diagram

31.3 Function Description

31.3.1 Video data capture

This module capture video data from VOP.

31.3.2 Audio data capture

This module capture audio data from I2S and S/PDIF.

31.3.3 DP transmitter

This is main module in the eDP TX. It contains data packing, main link process, aux process and data process, etc.

31.4 Register Description

31.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

31.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
EDP_TX_DP_TX_VERSION	0x0010	W	0x00000060	DP_TX_VERSION
EDP_TX_FUNC_EN_1	0x0018	W	0x0000007D	Function Enable Register 1
EDP_TX_FUNC_EN_2	0x001C	W	0x00000087	Function Enable Register 2
EDP_TX_VIDEO_CTL_1	0x0020	W	0x00000000	Video Control Register 1
EDP_TX_VIDEO_CTL_2	0x0024	W	0x00000010	Video Control Register 2
EDP_TX_VIDEO_CTL_3	0x0028	W	0x00000000	Video Control Register 3
EDP_TX_VIDEO_CTL_4	0x002C	W	0x00000000	Video Control Register 4
EDP_TX_VIDEO_CTL_8	0x003C	W	0x00000020	Video Control Register 8
EDP_TX_VIDEO_CTL_10	0x0044	W	0x00000000	Video Control Register 10
EDP_TX_TOTAL_LINE_CFG_L	0x0048	W	0x00000000	Total Line Byte Configure Register
EDP_TX_TOTAL_LINE_CFG_H	0x004C	W	0x00000000	Total Line High Byte Configure Register
EDP_TX_ACTIVE_LINE_CFG_L	0x0050	W	0x00000000	Active Line Low Byte Configure Register
EDP_TX_ACTIVE_LINE_CFG_H	0x0054	W	0x00000000	Active Line High Byte Configure Register
EDP_TX_V_F_PORCH_CFG	0x0058	W	0x00000000	Vertical Front Porch Configure Register
EDP_TX_V_SYNC_WIDTH_CFG	0x005C	W	0x00000000	Vertical Sync Width Configure Register
EDP_TX_V_B_PORCH_CFG	0x0060	W	0x00000000	Vertical Back Porch Configure Register
EDP_TX_TOTAL_PIXEL_CFG_L	0x0064	W	0x00000000	Total Pixel Low Byte Configure Register
EDP_TX_TOTAL_PIXEL_CFG_H	0x0068	W	0x00000000	Total Pixel High Byte Configure Register
EDP_TX_ACTIVE_PIXEL_CFG_L	0x006C	W	0x00000000	Active Pixel Low Byte Configure Register
EDP_TX_ACTIVE_PIXEL_CFG_H	0x0070	W	0x00000000	Active Pixel High Byte Configure Register
EDP_TX_H_F_PORCH_CFG_L	0x0074	W	0x00000000	Horizon Front Porch Low Byte Configure Register
EDP_TX_H_F_PORCH_CFG_H	0x0078	W	0x00000000	Horizon Front Porch High Byte Configure Register
EDP_TX_H_SYNC_CFG_L	0x007C	W	0x00000000	Horizon Sync Width Low Byte Configure Register
EDP_TX_H_SYNC_CFG_H	0x0080	W	0x00000000	Horizon Sync Width High Byte Configure Register

Name	Offset	Size	Reset Value	Description
EDP_TX_H_B_PORCH_CFG_L	0x0084	W	0x00000000	Horizon Back Porch Low Byte Configure Register
EDP_TX_H_B_PORCH_CFG_H	0x0088	W	0x00000000	Horizon Back Porch High Byte Configure Register
EDP_TX_VIDEO_STATUS	0x008C	W	0x00000000	Input Video Status Register
EDP_TX_TOTAL_LINE_STA_L	0x0090	W	0x00000000	Total Line Status Low Byte Register
EDP_TX_TOTAL_LINE_STA_H	0x0094	W	0x00000000	Total Line Status High Byte Register
EDP_TX_ACTIVE_LINE_STA_L	0x0098	W	0x00000000	Active Line Status Low Byte Register
EDP_TX_ACTIVE_LINE_STA_H	0x009C	W	0x00000000	Active Line Status High Byte Register
EDP_TX_V_F_PORCH_STA	0x00A0	W	0x00000001	Vertical Front Porch Status Register
EDP_TX_V_SYNC_STA	0x00A4	W	0x00000000	Vertical Sync Width Status Register
EDP_TX_V_B_PORCH_STA	0x00A8	W	0x00000000	Vertical Back Porch Status Register
EDP_TX_TOTAL_PIXEL_STA_L	0x00AC	W	0x00000000	Total Pixel Status Low Byte Register
EDP_TX_TOTAL_PIXEL_STA_H	0x00B0	W	0x00000000	Total Pixel Status High Byte Register
EDP_TX_ACTIVE_PIXEL_STA_L	0x00B4	W	0x00000000	Active Pixel Status Low Byte Register
EDP_TX_ACTIVE_PIXEL_STA_H	0x00B8	W	0x00000000	Active Pixel Status High Byte Register
EDP_TX_H_F_PORCH_STA_L	0x00BC	W	0x00000000	Horizon Front Porch Status Low Byte Register
EDP_TX_H_F_PORCH_STA_H	0x00C0	W	0x00000000	Horizon Front Porch Status High Byte Register
EDP_TX_H_SYNC_STA_L	0x00C4	W	0x00000000	Horizon Sync Width Status Low Byte Register
EDP_TX_H_SYNC_STA_H	0x00C8	W	0x00000000	Horizon Sync Width Status High Byte Register
EDP_TX_H_B_PORCH_STA_L	0x00CC	W	0x00000000	Horizon Back Porch Status Low Byte Register
EDP_TX_H_B_PORCH_STA_H	0x00D0	W	0x00000000	Horizon Back Porch Status High Byte Register
EDP_TX_SPDIF_AUDIO_CTL_0	0x00D8	W	0x00000000	SPDIF Audio Control Register 0
EDP_TX_DP_AUDIO_CTL_1	0x00DC	W	0x00000000	DP Audio Control Register 1
EDP_TX_SPDIF_AUDIO_STA_0	0x00E0	W	0x00000000	SPDIF Audio Status Register 0
EDP_TX_SPDIF_AUDIO_STA_1	0x00E4	W	0x00000000	Audio SPDIF Status Register 1
EDP_TX_SPDIF_ERR_THRD	0x00E8	W	0x00000001	SPDIF Error Threshold Register
EDP_TX_SPDIF_ERR_CNT	0x00EC	W	0x00000000	SPDIF Error Counter Register
EDP_TX_AUDIO_BIST_CTL	0x00F0	W	0x00000000	Audio BIST Control Register

Name	Offset	Size	Reset Value	Description
EDP_TX_AUD_FREQ_CNT_1	0x00F4	W	0x00000000	Audio Input Clock Frequency Counter Register 1
EDP_TX_AUD_FREQ_CNT_2	0x00F8	W	0x00000000	Audio Input Clock Frequency Counter Register 2
EDP_TX_AVI_DB	0x01D0	W	0x00000000	AVI InfoFrame Packet Data Byte, address is Base + 0x01D0 ~ Base + 0x0200, AVI_DB1 ~ AVI_DB13
EDP_TX_AUDIO_DB	0x021C	W	0x00000000	Audio InfoFrame Packet Data Byte, address is Base + 0x021C ~ Base + 0x0240, AUDIO_DB1 ~ AUDIO_DB10
EDP_TX_IF_TYPE	0x0244	W	0x00000000	InfoFrame Packet Type Code.
EDP_TX_IF_PKT_DB	0x0254	W	0x00000000	InfoFrame Packet Data Byte, address is Base + 0x0254 ~ Base + 0x02B4, IF_PKT_DB1 ~ IF_PKT_DB25
EDP_TX_MPEG_DB	0x02D0	W	0x00000000	MPEG Source InfoFrame Packet Data Byte, address is Base + 0x02D0 ~ Base + 0x02F4, MPEG_DB1 ~ MPEG_DB10
EDP_TX_REUSE_SPD_HB	0x02F8	W	0x00000000	Reuse SPD HB0 ~ HB3, address is Base + 0x02F8 ~ Base + 0x0304
EDP_TX_REUSE_SPD_PB	0x0308	W	0x00000000	Reuse SPD PB0 ~ PB3, address is Base + 0x0308 ~ Base + 0x0314
EDP_TX_PSR_FRAME_UPDATA_CTRL	0x0318	W	0x00000000	PSR frame update control
EDP_TX_VSC_SHADOW_DB	0x031C	W	0x00000000	VSC shadow data bytes 0 ~ 7, address is Base+ 0x031C ~ Base+ 0x0338, VSC_SHADOW_DB0 ~ VSC_SHADOW_DB7
EDP_TX_VSC_SHADOW_PB	0x033C	W	0x00000000	VSC shadow parity bytes 0 ~ 1, address is Base+ 0x033C ~ Base+ 0x0340, VSC_SHADOW_PB0 ~ VSC_SHADOW_PB1
EDP_TX_AUDIO_I2S_CH_STA1	0x0344	W	0x00000000	Audio I2S Channel Status Register 1
EDP_TX_AUDIO_I2S_CH_STA2	0x0348	W	0x00000000	Audio I2S Channel Status Register 2
EDP_TX_AUDIO_I2S_CH_STA3	0x034C	W	0x00000000	Audio I2S Channel Status Register 3
EDP_TX_AUDIO_I2S_CH_STA4	0x0350	W	0x00000000	I2S Channel Status Register 4
EDP_TX_AUDIO_I2S_CH_STA5	0x0354	W	0x00000000	Audio Channel Status Register 5
EDP_TX_LANE_MAP	0x035C	W	0x00000055	Lane Map Register
EDP_TX_INT_STATE	0x03C0	W	0x00000000	Interrupt Status Register
EDP_TX_COMMON_INT_STA_1	0x03C4	W	0x00000000	Common Interrupt Status Register 1
EDP_TX_COMMON_INT_STA_2	0x03C8	W	0x00000000	Common Interrupt Status Register 2
EDP_TX_COMMON_INT_STA_3	0x03CC	W	0x00000000	Common Interrupt Status Register 3

Name	Offset	Size	Reset Value	Description
EDP_TX_COMMON_INT_STA_4	0x03D0	W	0x00000000	Common Interrupt Status Register 4
EDP_TX_SPDIF_BIPHASE_INT_STA	0x03D4	W	0x00000000	SPDIF Biphase Interrupt Status Register
EDP_TX_DP_INT_STA	0x03DC	W	0x00000000	DisplayPort Interrupt Status Register
EDP_TX_COMMON_INT_MASK_1	0x03E0	W	0x00000000	Interrupt Mask Register
EDP_TX_COMMON_INT_MASK_2	0x03E4	W	0x00000000	Interrupt Mask Register
EDP_TX_COMMON_INT_MASK_3	0x03E8	W	0x00000000	Interrupt Mask Register
EDP_TX_COMMON_INT_MASK_4	0x03EC	W	0x00000000	Interrupt Mask Register
EDP_TX_DP_INT_STA_MASK	0x03F8	W	0x00000000	Interrupt enable Register
EDP_TX_INT_CTL	0x03FC	W	0x00000001	Interrupt Control Register
EDP_TX_SYS_CTL_1	0x0600	W	0x00000000	System Control Register 1
EDP_TX_SYS_CTL_2	0x0604	W	0x00000000	System Control Register 2
EDP_TX_SYS_CTL_3	0x0608	W	0x00000000	System Control Register 3
EDP_TX_SYS_CTL_4	0x060C	W	0x00000000	System Control Register 4
EDP_TX_DP_VID_CTL	0x0610	W	0x00000000	DP Video Control Register
EDP_TX_PKT_SEND_CTL	0x0640	W	0x00000000	Packet Send Control Register.
EDP_TX_DP_HDCP_CTL	0x0648	W	0x00000000	DisplayPort HDCP Control Register.
EDP_TX_SPDIF_PHASE1_CTL_0	0x0650	W	0x00000000	This register control SPDIF 1 cycle phase counter value [7:0]
EDP_TX_SPDIF_PHASE1_CTL_1	0x0654	W	0x00000000	This register enables force of the 1 cycle phase counter value [8]
EDP_TX_SPDIF_PHASE2_CTL_0	0x0658	W	0x00000000	This register control SPDIF 2 cycle phase counter value [7:0]
EDP_TX_SPDIF_PHASE2_CTL_1	0x065C	W	0x00000000	This register control SPDIF 2 cycle phase counter value [8]
EDP_TX_SPDIF_PHASE3_CTL_0	0x0660	W	0x00000000	This register control SPDIF 3 cycle phase counter value [7:0]
EDP_TX_SPDIF_PHASE3_CTL_1	0x0664	W	0x00000000	This register control SPDIF 3 cycle phase counter value [8]
EDP_TX_LINK_BW_SET	0x0680	W	0x0000000A	Main link bandwidth setting
EDP_TX_LANE_COUNT_SET	0x0684	W	0x00000000	Main link lane count
EDP_TX_DP_TRAINING_PTN_SET	0x0688	W	0x00000000	DP Training Pattern Set Register
EDP_TX_DP_LN0_LINK_TRAINING_CTL	0x068C	W	0x00000000	DP Lane 0 Link Training Control Register.
EDP_TX_DP_LN1_LINK_TRAINING_CTL	0x0690	W	0x00000000	DP Lane 1 Link Training Control Register.
EDP_TX_DP_LN2_LINK_TRAINING_CTL	0x0694	W	0x00000000	DP Lane 2 Link Training Control Register.
EDP_TX_DP_LN3_LINK_TRAINING_CTL	0x0698	W	0x00000000	DP Lane 3 Link Training Control Register.
EDP_TX_DP_HW_LINK_TRAINING_CTL	0x06A0	W	0x00000000	DP hardware training control registers.

Name	Offset	Size	Reset Value	Description
EDP_TX_HPD_DEGLITCH_L	0x06C4	W	0x0000005E	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDP_TX_HPD_DEGLITCH_H	0x06C8	W	0x0000001A	HPD_DEGLITCH is used to de-glitch the HPD signal.
EDP_TX_POLLING_PERIOD	0x06CC	W	0x0000000E	POLLING_PERIOD
EDP_TX_DP_LINK_DEBUG_CTL	0x06E0	W	0x00000000	DP Link Debug Control Register
EDP_TX_DP_SINK_COUNT	0x06E4	W	0x00000000	SINK_COUNT
EDP_TX_DP_IRD_VECTOR	0x06E8	W	0x00000000	IRQ_VECTOR
EDP_TX_DP_LINK_STATUS0	0x06EC	W	0x00000000	DP_LINK_STATUS0
EDP_TX_DP_LINK_STATUS1	0x06F0	W	0x00000000	DP_LINK_STATUS1
EDP_TX_DP_ALIGN_STATUS	0x06F4	W	0x00000000	ALIGN_STATUS
EDP_TX_M_VID_0	0x0700	W	0x00000000	M_VID[7:0]
EDP_TX_M_VID_1	0x0704	W	0x00000000	M_VID[15:8]
EDP_TX_M_VID_2	0x0708	W	0x00000000	M_VID[23:16]
EDP_TX_N_VID_0	0x070C	W	0x00000000	N_VID[7:0]
EDP_TX_N_VID_1	0x0710	W	0x00000000	N_VID[15:8]
EDP_TX_N_VID_2	0x0714	W	0x00000000	N_VID[23:16]
EDP_TX_M_VID_MON	0x0718	W	0x00000000	M_VID value monitoring register
EDP_TX_DP_VIDEO_FIFO_THRD	0x0730	W	0x00000000	DP Video Data FIFO Threshold Register
EDP_TX_DP_GNS_CTRL	0x0734	W	0x00000000	DP GNS CONTROL REGISTER
EDP_TX_DP_AUDIO_MARGIN	0x073C	W	0x00000000	DP Audio Margin Register
EDP_TX_M_AUD_MON	0x0740	W	0x00000000	M_AUD value monitoring register
EDP_TX_M_AUD_0	0x0748	W	0x00000000	M_AUD[7:0]
EDP_TX_M_AUD_1	0x074C	W	0x00000000	M_AUD[15:8]
EDP_TX_M_AUD_2	0x0750	W	0x00000000	M_AUD[23:16]
EDP_TX_N_AUD_0	0x0754	W	0x00000000	N_AUD[7:0]
EDP_TX_N_AUD_1	0x0758	W	0x00000000	N_AUD[15:8]
EDP_TX_N_AUD_2	0x075C	W	0x00000000	N_AUD[23:16]
EDP_TX_DP_M_CAL_CTL	0x0760	W	0x00000000	DP M Value Calculation Control Register
EDP_TX_M_VID_GEN_FILTER_TH	0x0764	W	0x00000004	The threshold of M_VID generation filter
EDP_TX_M_AUD_GEN_FILTER_TH	0x0778	W	0x00000002	The threshold of M_AUD generation filter
EDP_TX_AUX_CH_STA	0x0780	W	0x00000000	AUX Channel Access Status Register
EDP_TX_AUX_ERR_NUM	0x0784	W	0x00000000	AUX Channel Access Error Code Register
EDP_TX_AUX_CH_DEFER_CTL	0x0788	W	0x0000007F	DP AUX CH DEFER Control Register
EDP_TX_AUX_RX_COMM	0x078C	W	0x00000000	AUX CH received command
EDP_TX_BUFFER_DATA_CTL	0x0790	W	0x00000000	DP Buffer Data Count Register
EDP_TX_AUX_CH_CTL_1	0x0794	W	0x00000000	DP AUX Channel Control Register 1
EDP_TX_AUX_ADDR_7_0	0x0798	W	0x00000000	AUX_ADDR[7:0]

Name	Offset	Size	Reset Value	Description
EDP_TX_AUX_ADDR_15_8	0x079C	W	0x00000000	AUX_ADDR[15:8]
EDP_TX_AUX_ADDR_19_16	0x07A0	W	0x00000000	AUX_ADDR[19:16]
EDP_TX_AUX_CH_CTL_2	0x07A4	W	0x00000000	DP AUX CH Control Register 2
EDP_TX_BUF_DATA	0x07C0	W	0x000000FF	AUX CH buffer data 0 ~ 15, address is Base + 0x07C0 ~ Base+0x07FC
EDP_TX_SOC_GENERAL_CTL	0x0800	W	0x00000000	General control register
EDP_TX_DP_TEST_80B_PATTERN0	0x081C	W	0x00000000	DP test 80bit pattern0
EDP_TX_DP_TEST_80B_PATTERN1	0x0820	W	0x00000000	DP test 80bit pattern1
EDP_TX_DP_TEST_80B_PATTERN2	0x0824	W	0x00000000	DP test 80bit pattern2
EDP_TX_AUD_CTL	0x0834	W	0x00000000	Audio Control register
EDP_TX_CRC_CON	0x0890	W	0x00000000	CRC check control
EDP_TX_CRC_RESULT	0x0894	W	0x00000000	CRC result
EDP_TX_I2S_CTRL	0x09C8	W	0x00000000	I2S_CTRL
EDP_TX_I2S_CH_SWAP	0x09CC	W	0x0000000B	I2S channel swap
EDP_TX_I2S_CH_CTRL	0x09D0	W	0x000000E4	I2S channel control
EDP_TX_I2S_CH_CTRL1	0x09D4	W	0x00000000	I2S channel control 1
EDP_TX_LINK_POLICY	0x09D8	W	0x00000050	Link_Policy

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

31.4.3 Detail Registers Description

EDP_TX_DP_TX_VERSION

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	dp_tx_version Version

EDP_TX_FUNC_EN_1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	vid_cap_func_en_n Video capture functions enable. 1'b0: Normal operation 1'b1: Disable video capture
5	RW	0x1	vid_fifo_func_en_n Video FIFO functions enable. 1'b0: Normal operation 1'b1: Disable video FIFO
4	RW	0x1	aud_fifo_func_en_n Audio FIFO functions enable. 1'b0: Normal operation 1'b1: Disable Audio FIFO

Bit	Attr	Reset Value	Description
3	RW	0x1	aud_func_en_n Audio FIFO and capture module function enable. 1'b0: Normal operation 1'b1: Disable Audio FIFO and capture module If audio data (DMA or SPDIF) should be transmitted, AUD_FUNC_EN_N and AUD_FIFO_FUNC_EN_N should be set to 0 (enable).
2	RW	0x1	hdcp_func_en_n HDCP module functions enable. 1'b0: Normal operation 1'b1: Disable HDCP logic By disabling and enabling HDCP, all of registers in HDCP are cleared, except for the HDCP key inside of SPSRAM. Therefore, as an easy way to prepare re-authentication, firmware can disable and enable again to clear all HDCP registers.
1	RO	0x0	reserved
0	RW	0x1	sw_func_en_n Software defined function enable. 1'b0: Normal operation 1'b1: Disable All the function modules The bit has the highest priority, if the bit is 1, other function enable bits does not work.

EDP_TX_FUNC_EN_2

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x1	ssc_func_en_n SSC module enable. 1'b0: Normal mode 1'b1: Disable SSC module To apply updated SSC parameters into SSC operation, firmware must disable and enable this bit.
6:3	RO	0x0	reserved
2	RW	0x1	aux_func_en_n AUX channel module function enable. 1'b0: Normal operation 1'b1: Disable AUX channel module
1	RW	0x1	serdes_fifo_func_en_n Serdes FIFO function enable. 1'b0: Normal mode 1'b1: Disable Serdes FIFO To reset the serdes fifo, firmware must disable and enable this bit.
0	RW	0x1	ls_clk_domain_func_en_n Link symbol clock domain modules functions enable. 1'b0: Normal mode 1'b1: Disable the modules in link symbol clock domain. To reset the modules in link symbol clock domain, firmware must disable and enable this bit.

EDP_TX_VIDEO_CTL_1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	video_en Video data input enable. 1'b0: Disable video data input. 1'b1: Enable video data input. It takes effect at next video frame.
6	RW	0x0	video_mute Video mute enable. In video mute mode, the solid color, specified in Base + 0x04A8 ~ Base + 0x04B0, is displayed. 1'b0: Disable 1'b1: Enable Output video data is changed properly as soon as this bit is configured.
5:0	RO	0x00	reserved

EDP_TX_VIDEO_CTL_2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_d_range Dynamic range. This bit field is used to specify video data format in main stream attribute data. 1'b1: CEA range (16 ~ 235) 1'b0: VESA range (0 ~ 255)
6:4	RW	0x1	in_bpc Video input bit per color/ component (bpc). This bit field is used to specify video data format in main stream attribute data. Note that 6 bpc mode is invalid in YCbCr 422 mode. 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	in_color_f Colorimetric format of input video. This is used to specify video data format in main stream attribute data. 2'b11: Reserved 2'b10: YCbCr444 2'b01: YcbCr422 2'b00: RGB

EDP_TX_VIDEO_CTL_3

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	in_yc_coeffi YCbCr Coefficients of input video. This is used to specify video data format in main stream attribute data. 1'b1: ITU709 1'b0: ITU601
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	vid_chk_update_type Select video format stability check method in video capture block. 1'b1: Check stability with the difference between adjacent frames. 1'b0: Check stability with the difference of differences between adjacent frames. Compares difference of 1st and 2nd to difference of 3rd and 4th frame.
3:0	RO	0x0	reserved

EDP_TX_VIDEO_CTL_4

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	bist_en Video BIST enable. 1'b1: Enable video BIST 1'b0: Normal operation mode
2	RW	0x0	bist_width Control display BIST color bar width. 1'b1: Each bar is 64 pixel width. 1'b0: Each bar is 32 pixel width.
1:0	RW	0x0	bist_type Display BIST type. 2'b00: Color bar 2'b01: White, gray and black bar 2'b10: Mobile white bar 2'b11: Reserved

EDP_TX_VIDEO_CTL_8

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x2	vid_hres_th Video Frame Horizontal Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.
3:0	RW	0x0	vid_vres_th Video Frame Vertical Resolution variation threshold for video capture block. This bit field is used by CAPTURE block to determine whether STRM_VALID should be asserted.

EDP_TX_VIDEO_CTL_10

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	f_sel Video format select. 1'b1: Video format information from register 1'b0: Video format information from video_capture module According to the configuration of this bit field, the values of video format status registers in Base + 0x008C~ 0x00D0 are determined, which are transferred as main stream attribute packet. Note that if BIST_EN is set to 1, F_SEL must be cleared to 0 although video format information comes from registers set by user.
3	RO	0x0	reserved
2	RW	0x0	slave_i_scan_cfg Interlace scan mode configuration. 1'b0: Progressive 1'b1: Interlace When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
1	RW	0x0	slave_vsync_p_cfg Slave mode VSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.
0	RW	0x0	slave_hsync_p_cfg Slave mode HSYNC polarity configuration. 1'b1: Low is active. 1'b0: High is active. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_TOTAL_LINE_CFG_L

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_cfg_l TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_TOTAL_LINE_CFG_H

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	total_line_cfg_h TOTAL_LINE_CFG is used to specify the number of lines in each frame. This register is TOTAL_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When Video BIST_EN is enabled, this bit must be configured right to generate right video format.

EDP_TX_ACTIVE_LINE_CFG_L

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_cfg_l ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_ACTIVE_LINE_CFG_H

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	active_line_cfg_h ACTIVE_LINE_CFG is used to specify the number of active lines in each frame. This register is ACTIVE_LINE_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_V_F_PORCH_CFG

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_f_porch_cfg This is used to specify the number of lines in vertical front porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_V_SYNC_WIDTH_CFG

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_width_cfg This is used to specify the number of lines in VSYNC period. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_V_B_PORCH_CFG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_cfg This is used to specify the number of lines in frame back porch part. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_TOTAL_PIXEL_CFG_L

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_cfg_l TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG[7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_TOTAL_PIXEL_CFG_H

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	total_pixel_cfg_h TOTAL_PIXEL_CFG is used to specify the number of pixels in each line. This register is TOTAL_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_ACTIVE_PIXEL_CFG_L

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_pixel_cfg_l ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_ACTIVE_PIXEL_CFG_H

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	active_pixel_cfg_h ACTIVE_PIXEL_CFG is used to specify the number of active pixels in each line. This register is ACTIVE_PIXEL_CFG [13:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_F_PORCH_CFG_L

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_cfg_l H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG[7:0] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_F_PORCH_CFG_H

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_cfg_h H_F_PORCH_CFG is used to specify the number of pixels in frame horizon front porch part. This register is H_F_PORCH_CFG [11:8] When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_SYNC_CFG_L

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_sync_cfg_l H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_SYNC_CFG_H

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	h_sync_cfg_h H_SYNC_CFG is used to specify the number of pixels in HSYNC period. This register is H_SYNC_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_B_PORCH_CFG_L

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_cfg_l H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [7:0]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_H_B_PORCH_CFG_H

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	h_b_porch_cfg_h H_B_PORCH_CFG is used to specify the number of pixel in frame horizon back porch part. This register is H_B_PORCH_CFG [11:8]. When F_SEL is 1, this value is sent in main stream attribute packet. When BIST_EN is 1, this bit field is used to specify the BIST video stream format.

EDP_TX_VIDEO_STATUS

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	field_s Interlace scan field status. 1'b1: Second field. 1'b0: First field. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
2	RW	0x0	i_scan_s Auto-detect interlace or progressive scan status: 1'b1: Interlace scan. 1'b0: Progressive scan. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.
1	RW	0x0	vsync_p_s Auto-detect VSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

Bit	Attr	Reset Value	Description
0	RW	0x0	hsync_p_s Auto-detect HSYNC polarity: 1'b1: Low is active. 1'b0: High is active. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_TOTAL_LINE_STA_L

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_line_sta_l TOTAL_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_TOTAL_LINE_STA_H

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	total_line_sta_h TOTAL_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_ACTIVE_LINE_STA_L

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	active_line_sta_l ACTIVE_LINE [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_ACTIVE_LINE_STA_H

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	active_line_sta_h ACTIVE_LINE [11:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_V_F_PORCH_STA

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x01	v_f_porch_sta V_F_PORCH (vertical front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_V_SYNC_STA

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_sync_sta V_SYNC_WIDTH (vertical sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_V_B_PORCH_STA

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	v_b_porch_sta V_B_PORCH (vertical back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_TOTAL_PIXEL_STA_L

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	total_pixel_sta_l TOTAL_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_TOTAL_PIXEL_STA_H

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	total_pixel_sta_h TOTAL_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_ACTIVE_PIXEL_STA_L

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	active_pixel_sta_l ACTIVE_PIXEL [7:0] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_ACTIVE_PIXEL_STA_H

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	active_pixel_sta_h ACTIVE_PIXEL [13:8] which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_F_PORCH_STA_L

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_f_porch_sta_l H_F_PORCH [7:0] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_F_PORCH_STA_H

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_f_porch_sta_h H_F_PORCH [11:8] (horizon front porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_SYNC_STA_L

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_sync_sta_l H_SYNC [7:0] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_SYNC_STA_H

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	h_sync_sta_h H_SYNC [11:8] (horizon sync width) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_B_PORCH_STA_L

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	h_b_porch_sta_l H_B_PORCH [7:0] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_H_B_PORCH_STA_H

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	h_b_porch_sta_h H_B_PORCH [11:8] (horizon back porch) which is detected by video capture module. This bit field is valid only when STRM_VALID is high. And STRM_VALID becomes high when two successive frames are determined as stable.

EDP_TX_SPDIF_AUDIO_CTL_0

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	aud_spdif_en Set SPDIF audio stream input enable. 1'b0: Disable 1'b1: Enable
6:4	RO	0x0	reserved
3	RW	0x0	reuse_spd_en Reuse spd inforframe registers.
2	RW	0x0	force_spdif_det Force SPDIF_STREAM_DET, which is SPDIF detect status, to 1. (Test purpose only) 1'b1: Force SPDIF_STREAM_DET to 1. 1'b0: SPDIF_STREAM_DET is set by hardware detector.
1	RW	0x0	spdif_parity_ctrl Control the SPDIF parity generation scheme. In the IEC-60958, audio packet is 28-bit. But in the DP standard v1.1, the audio packet is 32-bit, 4 more control bits have been added. The control bit selects the parity scheme of original 28 bit defined in IEC-60958 or parity scheme of 32 bit defined in DP standard v1.1. 1'b1: Parity of DP link audio sample 32 bit. 1'b0: Parity of SPDIF audio sample 28 bit.

Bit	Attr	Reset Value	Description
0	RW	0x0	spdif_clk_det_reset_bypass Bypass SPDIF clock detect auto reset: 1'b1: Bypass SPDIF clock detect auto reset, SPDIF module will not be reset even SPDIF clock is not detected. 1'b0: If SPDIF clock is not detected, SPDIF module is reset automatically.

EDP_TX_DP_AUDIO_CTL_1

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	aud_mute_en4 Audio data auto mute control enable for audio FIFO under run interrupt. 1'b1: Enable 1'b0: Disable
4	RW	0x0	aud_mute_en3 Audio data auto mute control enable for audio FIFO overrun interrupt. 1'b1: Enable 1'b0: Disable
3	RW	0x0	aud_mute_en2 Audio data auto mute control enable for HDCP failed interrupt. 1'b1: Enable 1'b0: Disable
2	RW	0x0	aud_mute_en1 Audio data auto mute control enable for SPDIF unstable interrupt. 1'b1: Enable 1'b0: Disable
1	RW	0x0	aud_mute_en0 Audio data auto mute control enable for Audio clock change interrupt. 1'b1: Enable 1'b0: Disable
0	RO	0x0	reserved

EDP_TX_SPDIF_AUDIO_STA_0

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_clk_det SPDIF audio clock detected flag. 1'b1: Clock detected 1'b0: Clock not detected
6:1	RO	0x00	reserved
0	RW	0x0	spdif_stream_det SPDIF audio stream detected flag. 1'b1: Input detected 1'b0: No input detected

EDP_TX_SPDIF_AUDIO_STA_1

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	spdif_fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved SPDIF_FS_FREQ can be read when SPDIF_STREAM_DET and VSYNC_DET are high.
3:0	RW	0x0	spdif_word_len Audio word length (corresponding to channel status bits [35:32]). 4'b0010: 16 bits 4'b0011: 20 bits 4'b0100: 18 bits 4'b0101: 22 bits 4'b1000: 19 bits 4'b1001: 23 bits 4'b1010: 20 bits 4'b1011: 24 bits 4'b1100: 17 bits 4'b1101: 21 bits SPDIF_WORD_LEN can be read when SPDIF_STREAM_DET and VSYNC_SET are high.

EDP_TX_SPDIF_ERR_THRD

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	spdif_err_thrd SPDIF parity error threshold for the SPDIF_ERR interrupt. When SPDIF stream data parity error occurs, the SPDIF_ERR_CNT will increase by 1. And when SPDIF_ERR_CNT equals to SPDIF_ERR_THRD, SPDIF_ERR interrupt happens.

EDP_TX_SPDIF_ERR_CNT

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_err_cnt SPDIF parity errors counter. Write any value to clear.

EDP_TX_AUDIO_BIST_CTL

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	sin_ampl Set the Sin wave amplitude for audio BIST data. 4'b0000: 255 4'b0001: 510 4'b0010: 1020 4'b0011: 2040 4'b0100: 4080 4'b0101: 8160 4'b0110: 16320 4'b0111: 32640 4'b1000: 65280 4'b1001: 130560 4'b1010: 261120 4'b1011: 522240 4'b1100: 1044480 4'b1101: 2088960 4'b1110: 4177920 4'b1111: 8355840
3:1	RO	0x0	reserved
0	RW	0x0	aud_bist_en Audio BIST enable. 1'b1: Enable 1'b0: Disable

EDP_TX_AUD_FREQ_CNT_1

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aud_freq_cnt_l Audio input clock frequency counter register. For test purpose only.

EDP_TX_AUD_FREQ_CNT_2

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aud_freq_cnt_h Audio input clock frequency counter register. For test purpose only.

EDP_TX_AVI_DB

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avi_db AVI InfoFrame Packet Data Byte 1 ~ 13

EDP_TX_AUDIO_DB

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	audio_db Audio InfoFrame Packet Data Byte 1 ~ 10

EDP_TX_IF_TYPE

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_type InfoFrame Packet Type Code. It can be set as (0x80 + InfoFrame Type Code) and send any type of infoframe defined in CEA-861C. Commonly, we set it as 0x83(0x80 + 0x03, 0x03 is the type code of SPD InfoFrame) and send SPD infoframe.

EDP_TX_IF_PKT_DB

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	if_pkt_db InfoFrame Packet Data Byte 1 ~ 25. The registers define the data in the InfoFrame and the InfoFrame type is defined by IF_TYPE.

EDP_TX_MPEG_DB

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	mpeg_db MPEG Source InfoFrame Packet Data Byte 1 ~ 10

EDP_TX_REUSE_SPD_HB

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_hb Reuse SPD HB0 ~ HB3

EDP_TX_REUSE_SPD_PB

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	reuse_spd_pb Reuse SPD PB0 ~ PB3

EDP_TX_PSR_FRAME_UPDATA_CTRL

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	psr_frame_up_type Select PSR Frame Update type. 1'b1: Burst single frame update 1'b0: Single frame update
0	RW	0x0	psr_frame_update Enable PSR Frame Update

EDP_TX_VSC_SHADOW_DB

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_db VSC shadow data bytes 0 ~ 7

EDP_TX_VSC_SHADOW_PB

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	vsc_shadow_pb VSC shadow parity bytes 0 ~ 1

EDP_TX_AUDIO_I2S_CH_STA1

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	audio_mode 2'b00: PCM Audio Others: No PCM Audio stream
5:3	RW	0x0	pcm_mode 3'b000: 2 audio channels without pre-emphasis 3'b001: 2 audio channels with 50/15 pre-emphasis
2	RW	0x0	sw_cprgt 1'b0: Software for which copyright is asserted 1'b1: Software for which no copyright is asserted
1	RW	0x0	non_pcm 1'b0: Audio sample word represents linear PCM samples 1'b1: Audio sample word used for other purposes
0	RW	0x0	audio_i2s_ch_sta1 1'b0: Consumer applications 1'b1: Professional applications

EDP_TX_AUDIO_I2S_CH_STA2

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cat_code Category code (corresponding to channel status bits [15:8])

EDP_TX_AUDIO_I2S_CH_STA3

Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ch_num Channel number (corresponding to channel status bits [23:20]). Only 2_channel is supported in BIST mode.
3:0	RW	0x0	source_num Source number (corresponding to channel status bits [19:16]). Only 2_channel is supported in BIST mode.

EDP_TX_AUDIO_I2S_CH_STA4

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	chnl_bit1 Corresponding to channels status bits [31:30].

Bit	Attr	Reset Value	Description
5:4	RW	0x0	clk_accur Clock accuracy (corresponding to channels status bits [29:28]). These two bits define the sampling frequency tolerance. The bits are set in the transmitter.
3:0	RW	0x0	fs_freq Sampling clock frequency (corresponding to channel status bits [27:24]). 4'b0000: 44.1 KHz 4'b0010: 48 KHz 4'b0011: 32 KHz 4'b1000: 88.2 KHz 4'b1010: 96 KHz 4'b1110: 192 KHz Others: Reserved When set SPDIF_FS_OVRWR to "1", the four bits sample clock frequency in channel status is replaced by this register setting. Note that the audio sine wave frequency equals to Audio Sample Frequency/128. For example, if the sampling clock frequency is 44.1K, the sine wave frequency is 44,100/128 = 344.6Hz.

EDP_TX_AUDIO_I2S_CH_STA5

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	chnl_bit2 Corresponding to channels status bits [39:36].
3:1	RW	0x0	word_length Audio word length (corresponding to channel status bits [35:33]). When WORD_MAX: 0, 3'b001: 16 bits 3'b010: 18 bits 3'b100: 19 bits 3'b101: 20 bits 3'b110: 17 bits When WORD_MAX: 1, 3'b001: 20 bits 3'b010: 22 bits 3'b100: 23 bits 3'b101: 24 bits 3'b110: 21 bits
0	RW	0x0	word_max Audio word length Max (corresponding to channel status bits 32). 1'b0: Maximal word length is 20 bits. 1'b1: Maximal word length is 24 bits.

EDP_TX_LANE_MAP

Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x1	lane3_map Control physical lane 3 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0

Bit	Attr	Reset Value	Description
5:4	RW	0x1	lane2_map Control physical lane 2 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
3:2	RW	0x1	lane1_map Control physical lane 1 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0
1:0	RW	0x1	lane0_map Control physical lane 0 will map to which logic lane: 2'b11: Logic lane 3 2'b10: Logic lane 2 2'b01: Logic lane 1 2'b00: Logic lane 0

EDP_TX_INT_STATE

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_state Interrupt request status 1'b1: Interrupt service is requested. 1'b0: No interrupt service is requested.

EDP_TX_COMMON_INT_STA_1

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	vsync_det 1'b1: VSYNC active edge has been detected.
6	RW	0x0	pll_lock_chg 1'b1: PLL lock state is changed. Check PLL_LOCK of register DP_DEBUG_CTL for PLL lock status.
5	RW	0x0	spdif_err 1'b1: SPDIF parity errors Write 1 to clear. Software can change this interrupt generation by setting the register SPDIF_ERR_THRD. When SPDIF_ERR, software shall check SPDIF status on register SPDIF_AUDIO_STA_0.
4	RW	0x0	spdif_unstbl 1'b1: Not find expected preamble for SPDIF input.
3	RW	0x0	vid_format_chg 1'b1: Video input format change is detected.
2	RW	0x0	aud_clk_chg 1'b1: Audio input clock change is detected.
1	RW	0x0	vid_clk_chg 1'b1: Video input clock change is detected.
0	RW	0x0	sw_int 1'b1: Software-induced interrupt.

EDP_TX_COMMON_INT_STA_2

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	enc_en_chg 1'b1: HDCP_ENC_EN changed detected. Write 1 to clear. ENC_EN_CHG happens whenever HDCP_ENC_EN is changed from 1 to 0 or form 0 to 1. This interrupt is generated when the internal HDCP cipher module find out that encryption status is changed. Software can check encryption status on bit ENCRYPT of register HDCP_STA.
5:4	RO	0x0	reserved
3	RW	0x0	hw_bksv_rdy 1'b1: BKSV is ready. Write 1 to clear. It is for H/W HDCP
2	RW	0x0	hw_sha_done 1'b1: HDCP hardware computing V has ended. Write 1 to clear. During H/W HDCP authentication, it is generated after calculating V.
1	RW	0x0	hw_auth_state_chg 1'b1: H/W HDCP authentication state has changed. HW_AUTH_STATE_CHG happens after H/W HDCP is enabled Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA This bit is set only when authentication success or failure status is changed. So, successive authentication failure does not set this bit.
0	RW	0x0	hw_auth_done 1'b1: H/W HDCP authentication has ended. This bit is set when H/W HDCP authentication is finished regardless of success or failure. Software can check hardware authentication status on bit HW_AUTHEN_PASS of register HDCP_STA

EDP_TX_COMMON_INT_STA_3

Address: Operational Base + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	afifo_under 1'b1: Audio FIFO is under run. Write 1 to clear.
6	RW	0x0	afifo_over 1'b1: Audio FIFO is overrun. Write 1 to clear.
5	RW	0x0	r0_chk_flag For hardware authentication (with HDCP repeater): 1'b1: R0 check is finished. For software authentication: 1'b1: R0 is ready for software check. Write 1 to clear. If H/W re-authentication is needed and this bit is set to 1, then this bit must be cleared before H/W re-authentication.
4	RW	0x0	dpcd_specific_irq 1'b1: Sink specific interrupt in DPCD is detected. Write 1 to clear

Bit	Attr	Reset Value	Description
3	RW	0x0	mydp_plug_in 1'b1: MYDP plug out event is detected. Write 1 to clear
2	RW	0x0	mydp_plug_out 1'b1: MYDP plug out event is detected. Write 1 to clear
1	RW	0x0	mydp_hpd_irq 1'b1: MYDP HPD interrupt is detected. Write 1 to clear
0	RW	0x0	hdcp_link_check_fail 1'b1: HDCP link check failure is detected. Write 1 to clear.

EDP_TX_COMMON_INT_STA_4

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	spdif_bi_phase_err 1'b1: SPDIF bi-phase error has occurred. Write 1 to clear. Software reset will not clear this interrupt.
4:3	RO	0x0	reserved
2	RW	0x0	hotplug_chg 1'b1: Hot plug change detected. Write 1 to clear. HOTPLUG_CHG happens whenever the pin I_DP_HDP changes and the change remains for at least hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H. When HOTPLUG_CHG is high, software shall check the status of HPD signal on register HPD_STATUS.
1	RW	0x0	hpd_lost Hot plug detect signal lost timer larger than 2ms, that means cable is plugged out: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	plug Hot plug detect signal lost time is larger than 2ms before cable plugged, it means cable is plugged in: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDP_TX_SPDIF_BIPHASE_INT_STA

Address: Operational Base + offset (0x03D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_biphase_err_clr SPDIF biphase error
6:0	RO	0x00	reserved

EDP_TX_DP_INT_STA

Address: Operational Base + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	int_hpd IRQ (HPD de-asserted less than 2ms) detect interrupt: 1'b1: IRQ interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
5	RW	0x0	hw_training_finish Training FSM module finish link training procedure: 1'b1: Hardware link training finished 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
4	RO	0x0	reserved
3	RW	0x0	sink_lost Sink lost interrupt 1'b1: Sink lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
2	RW	0x0	link_lost Link lost interrupt 1'b1: Link lost occurred 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
1	RW	0x0	rply_receiv AUX channel command reply is received: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.
0	RW	0x0	aux_err AUX channel access error interrupt: 1'b1: Interrupt assert 1'b0: Not interrupt occurred Write 1 to this bit to clear this interrupt source.

EDP_TX_COMMON_INT_MASK_1

Address: Operational Base + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_1 Each bit corresponds to the same bit in Common Interrupt Status Register 1. 0: Mask interrupt 1: Enable interrupt

EDP_TX_COMMON_INT_MASK_2

Address: Operational Base + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_2 Each bit corresponds to the same bit in Common Interrupt Status Register 2. 0: Mask interrupt 1: Enable interrupt

EDP_TX_COMMON_INT_MASK_3

Address: Operational Base + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	common_int_mask_3 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 0: Mask interrupt 1: Enable interrupt

EDP_TX_COMMON_INT_MASK_4

Address: Operational Base + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	common_int_mask_4 Each bit corresponds to the same bit in Common Interrupt Status Register 3. 0: Mask interrupt 1: Enable interrupt

EDP_TX_DP_INT_STA_MASK

Address: Operational Base + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	dp_int_sta_mask Each bit corresponds to the same bit in DisplayPort Interrupt Status Register (DP_INT_STA). 1: Enable interrupt 0: Mask interrupt

EDP_TX_INT_CTL

Address: Operational Base + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	serdes_overflow_clear 1'b1: clear SerDes FIFO overflow flag
4	RW	0x0	serdes_underflow_clear 1'b1: clear SerDes FIFO underflow flag
3	RO	0x0	reserved
2	RW	0x0	soft_int_ctrl Set Software Interrupt: 1'b1: Set interrupt 1'b0: Do not set interrupt
1	RO	0x0	reserved
0	RW	0x1	int_pol INT pin assertion polarity: 1'b1: Assert high 1'b0: Assert low

EDP_TX_SYS_CTL_1

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	hbr2_eye_sy_ctrl HBR2 pattern control

Bit	Attr	Reset Value	Description
2	RW	0x0	det_sta Video stream clock detect status, It will not affect video output. 1'b1: Stream clock detected 1'b0: Stream clock not detected Write any value to update the current status.
1	RW	0x0	force_det Force video stream clock detect, this bit is only active when DET_CTRL is 1 1'b1: Force video stream clock detected 1'b0: Force video stream clock not detected This bit's type is R/W.
0	RW	0x0	det_ctrl Video stream clock detect status control: 1'b1: Use force detect status 1'b0: Use auto-detected status This bit's type is R/W.

EDP_TX_SYS_CTL_2

Address: Operational Base + offset (0x0604)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	cha_cri Pixel clock change detection threshold. The incoming pixel clock input is counted continuously by the 24Mhz reference clock. This register defines a number, if the counter number change is more than this value for 2 pixel clock edges, the CHA_STA bit is asserted. This bit's type is R/W.
3	RO	0x0	reserved
2	RW	0x0	cha_sta Video stream clock change status, It will not affect video output 1'b1: Clock frequency changed. 1'b0: Clock frequency not changed. Write any value to update the current status.
1	RW	0x0	force_cha Force stream clock change status, this bit only active when CHA_CTRL is 1 1'b1: Force clock change. When asserted, CHA_STA is '1'. 1'b0: Force clock not change. This bit's type is R/W.
0	RW	0x0	cha_ctrl Pixel clock frequency change status control 1'b1: Use force change status 1'b0: Use auto-detected status This bit's type is R/W.

EDP_TX_SYS_CTL_3

Address: Operational Base + offset (0x0608)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	hpd_status Hot plug detect status. 1'b1: HPD is 1. 1'b0: HPD is 0. This bit's type is RO. When this bit is 0, AUX CH will not work. Note that the HPD_STATUS is only changed after the change of the pin I_DP_HPD remains for no less than hot plug deglitch time. And the hot plug deglitch time is defined in HPD_DEGLITCH_L and HPD_DEGLITCH_H.
5	RW	0x0	f_hpd Force hot plug detect. 1'b1: Force HPD 1. 1'b0: Force HPD 0. This bit's type is R/W.
4	RW	0x0	hpd_ctrl Hot plug detect manual control. 1'b1: Force HPD with F_HPD. 1'b0: Use PIN_HPD state. This bit's type is R/W.
3	RW	0x0	hdcp_rdy HDCP ready status. 1'b1: HDCP is ready. 1'b0: HDCP is not ready. This bit's type is RO. This bit is an indicator of whether HDCP is ready to perform. Usually, it is set as soon as HPD signal is detected as plugged.
2	RW	0x0	strm_valid Input stream have constant video format, and this stream is valid to send out through link. 1'b1: Input stream is valid. 1'b0: Input stream is not valid. Write any value to update the current status. Hardware will not send out video through link when this bit is 0.
1	RW	0x0	f_valid Force stream valid, this bit only active when VALID_CTRL is 1. 1'b1: Force input video stream valid. 1'b0: Force input video stream not valid. This bit's type is R/W.
0	RW	0x0	valid_ctrl Stream valid control. 1'b1: Use F_VALID bit to control video stream valid status 1'b0: Use video stream valid auto-detect This bit's type is R/W.

EDP_TX_SYS_CTL_4

Address: Operational Base + offset (0x060C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	fix_m_aud Fix M_AUD value 1'b1: Use register M_AUD value to be sent out. 1'b0: Use calculates M_AUD value to be sent out.

Bit	Attr	Reset Value	Description
3	RW	0x0	enhanced DisplayPort Enhanced mode enable 1'b1: Enhanced mode 1'b0: Normal mode
2	RW	0x0	fix_m_vid Fix M_VID value 1'b1: Use register M_VID value to be sent out. 1'b0: Use calculates M_VID value to be sent out.
1:0	RW	0x0	m_vid_update_ctrl Control M_VID update frequency 2'b11: 1/8 X update rate 2'b10: 1/4 X update rate 2'b01: 1/2 X update rate 2'b00: Normal rate

EDP_TX_DP_VID_CTL

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:5	RW	0x0	bpc Bit per color/ component with video which transferred via DP main link 3'b011: 12 bits 3'b010: 10 bits 3'b001: 8 bits 3'b000: 6 bits Other: Reserved
4	RW	0x0	yc_coeff YCbCr Coefficients with video which transferred via DP main link 1'b1: ITU709 1'b0: ITU601
3	RW	0x0	d_range Dynamic range 1'b1: CEA range 1'b0: VESA range (from 0 to the maximum)
2:1	RW	0x0	color_f Colorimetric format with video which transferred via DP main link 2'b11: Reserved 2'b10: YcbCr444 2'b01: YcbCr422 2'b00: RGB
0	RO	0x0	reserved

EDP_TX_PKT_SEND_CTL

Address: Operational Base + offset (0x0640)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	audio_info_up Audio InfoFrame content has been updated. 1'b1: Updated, 1'b0: Don't care. Write 1 to this bit after Audio Packet Content Registers have been configured as Audio InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.

Bit	Attr	Reset Value	Description
6	RW	0x0	avi_info_up AVI InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after AVI Packet Content Registers have been configured as AVI InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
5	RW	0x0	mpeg_info_up MPEG InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after MPEG Packet Content Registers have been configured as MPEG InfoFrame content has been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
4	RW	0x0	if_up Configurable InfoFrame content has been updated. 1'b1: Updated 1'b0: Don't care Write 1 to this bit after IF_TYPE and IF_PKT_DB1~25 Registers have been configured as configurable InfoFrame content have been updated. This bit's type is R/W. This bit is self cleared after the register configured content has been used to update the InfoFrame.
3	RW	0x0	audio_info_en Audio InfoFrame send enable. 1'b1: Send Audio InfoFrame 1'b0: Don't send Audio InfoFrame Make sure that the Audio Packet Content Registers had been configured correctly and the AUDIO_INFO_UP had been written with 1. This bit's type is R/W.
2	RW	0x0	avi_info_en AVI InfoFrame send enable. 1'b1: Send AVI InfoFrame 1'b0: Don't send AVI InfoFrame Make sure that the AVI Packet Content Registers had been configured correctly and the AVI_INFO_UP had been written with 1. This bit's type is R/W.
1	RW	0x0	mpeg_info_en MPEG InfoFrame send enable. 1'b1: Send MPEG InfoFrame 1'b0: Don't send MPEG InfoFrame Make sure that the MPEG Packet Content Registers had been configured correctly and the MPEG_INFO_UP had been written with 1. This bit's type is R/W.
0	RW	0x0	pkt_send_ctl Configurable InfoFrame send enable. 1'b1: Send InfoFrame defined in IF_TYPE and IF_PKT_DB1~25. 1'b0: Don't send InfoFrame. Make sure that the IF_TYPE and IF_PKT_DB1~25 Registers had been configured correctly and the IF_UP had been written with 1. This bit's type is R/W.

EDP_TX_DP_HDCP_CTL

Address: Operational Base + offset (0x0648)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	hdcp_hpd_rst HDCP block reset control. 1'b0: No reset for HDCP block when HPD is low. 1'b1: Reset HDCP when HPD is low.
5:2	RO	0x0	reserved
1	RW	0x0	link_check_mode HDCP link integrity check mode: 1'b1: HDCP polling link integrity check status, and re-start HDCP Authentication automatically when detected link integrity check fail. 1'b0: HDCP don't polling link integrity check status.
0	RW	0x0	hw_hdcp_int The DP receiver initiates a HDCP interrupt through Hot Plug Detect Pin to DP transmitter whenever DP receiver finds R0' calculation done, downstream KSV list is ready and V' calculation done, or HDCP link integrity check failure. A firmware on DP transmitter must set this bit to 1 in order to make H/W HDCP authentication module do some proper action when firmware of DP transmitter find it out that the interrupt about HDCP. This bit is self cleared.

EDP_TX_SPDIF_PHASE1_CTL_0

Address: Operational Base + offset (0x0650)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase1_ctl_0 This register control SPDIF 1 cycle phase counter value [7:0], if bit SPDIF_PHASE1_CTL_EN is 0, the 1 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE1_CTL should be set as Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 135,000,000/ (32*44,100*2*2) = 23.9. SPDIF_PHASE1_CTL should set to 24.

EDP_TX_SPDIF_PHASE1_CTL_1

Address: Operational Base + offset (0x0654)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase1_ctl_en This register enables force of the 1 cycle phase counter value function. 1'b0: SPDIF 1 cycle phase counter value use chip counted value. 1'b1: SPDIF 1 cycle phase counter value use the data written to register SPDIF_PHASE1_CTL_0 and SPDIF_PHASE1_CTL_1.
6:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	spdif_phase1_ctl_1 This register control SPDIF 1 cycle phase counter value [8], if bit PHASE_1_CONTROL_EN is 0, the 1 cycle phase counter value [8] is read out. If the register SPDIF_PHASE1_CTL_EN is 1, firmware can force this value by writing data to this register.

EDP_TX_SPDIF_PHASE2_CTL_0

Address: Operational Base + offset (0x0658)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	spdif_phase2_ctl_0 This register control SPDIF 2 cycle phase counter value [7:0], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE2_CTL should be set as 2*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 2*135,000,000/ (32*44,100*2*2) = 47.8. SPDIF_PHASE2_CTL should set to 48.

EDP_TX_SPDIF_PHASE2_CTL_1

Address: Operational Base + offset (0x065C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase2_ctl_en This register enables force of the 2 cycle phase counter value function. 1'b0: SPDIF 2 cycle phase counter value use chip counted value. 1'b1: SPDIF 2 cycle phase counter value use the data written to register SPDIF_PHASE2_CTL_0 and SPDIF_PHASE2_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase2_ctl_1 This register control SPDIF 2 cycle phase counter value [8], if bit SPDIF_PHASE2_CTL_EN is 0, the 2 cycle phase counter value [8] is read out. If the register SPDIF_PHASE2_CTL_EN is 1, firmware can force this value by writing data to this register.

EDP_TX_SPDIF_PHASE3_CTL_0

Address: Operational Base + offset (0x0660)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	spdif_phase3_ctl_0 This register control SPDIF 3 cycle phase counter value [7:0], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [7:0] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register. The bits can be read only when SPDIF_STREAM_DET is one. SPDIF_PHASE3_CTL should be set as 3*Fls_clk / (32*Faudio_frequency * AudioChannelNum * 2). Here 2 are for biphase encoding and 32 is for each sub frame. For example if audio_frequency is 44.1KHz, Audio Channel Number is 2 and ls_clk frequency is 135M Hz. 3*135,000,000/ (32*44,100*2*2) = 71.7. SPDIF_PHASE3_CTL should set to 72.

EDP_TX_SPDIF_PHASE3_CTL_1

Address: Operational Base + offset (0x0664)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	spdif_phase3_ctl_en This register enables force of the 3 cycle phase counter value function. 1'b0: SPDIF 3 cycle phase counter value use chip counted value. 1'b1: SPDIF 3 cycle phase counter value use the data written to register SPDIF_PHASE3_CTL_0 and SPDIF_PHASE3_CTL_1.
6:1	RO	0x00	reserved
0	RW	0x0	spdif_phase3_ctl_1 This register control SPDIF 3 cycle phase counter value [8], if bit SPDIF_PHASE3_CTL_EN is 0, the 3 cycle phase counter value [8] is read out. If the register SPDIF_PHASE3_CTL_EN is 1, firmware can force this value by writing data to this register.

EDP_TX_LINK_BW_SET

Address: Operational Base + offset (0x0680)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0xa	link_bw_set Main link bandwidth setting: 0x6: 1.62Gpbs per lane 0xa: 2.7Gpbs per lane Other: Reserved

EDP_TX_LANE_COUNT_SET

Address: Operational Base + offset (0x0684)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	lane_count_set Main link lane count 0x1: one lane 0x2: two lanes 0x4: four lanes Other: Reserved

EDP_TX_DP_TRAINING_PTN_SET

Address: Operational Base + offset (0x0688)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	scrambling_disable Disable scramble 1'b1: Disable 1'b0: Normal operation
4:2	RW	0x0	link_qual_pattern_set Link quality pattern setting. 3'b101: HBR2 Compliance 3'b100: 80 bit test pattern 3'b011: PRBS 7 bit 3'b010: symbol error rate measurement pattern is sent 3'b001: D10.2 test pattern is sent 3'b000: link quality test pattern not sent
1:0	RW	0x0	sw_training_pattern_set Link training pattern setting. SW_TRAINING_PATTERN_SET has higher priority than LINK_QUAL_PATTER_SET. 2'b11: Reserved 2'b10: Sending training pattern 2 2'b01: Sending training pattern 1 2'b00: Training pattern not sent

EDP_TX_DP_LN0_LINK_TRAINING_CTL

Address: Operational Base + offset (0x068C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_0 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_0 Lane 0 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_0 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For test purpose only. This bit's type is RO. For more information, refer to MAX_PRE_REACH_0.
1:0	RW	0x0	drive_current_set_0 Lane 0 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDP_TX_DP_LN1_LINK_TRAINING_CTL

Address: Operational Base + offset (0x0690)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_1 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_1 Lane 1 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_1 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_1. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_1 Lane 1 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDP_TX_DP_LN2_LINK_TRAINING_CTL

Address: Operational Base + offset (0x0694)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_2 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.
4:3	RW	0x0	pre_emphasis_set_2 Lane 2 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_2 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_2. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_2 Lane 2 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDP_TX_DP_LN3_LINK_TRAINING_CTL

Address: Operational Base + offset (0x0698)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	max_pre_reach_3 This bit field is set to 1 automatically when max pre-emphasis level of DP Tx is reached.

Bit	Attr	Reset Value	Description
4:3	RW	0x0	pre_emphasis_set_3 Lane 3 pre-emphasis level setting 2'b11: 9.5 dB 2'b10: 6.0 dB 2'b01: 3.5 dB 2'b00: 0 dB (No pre-emphasis) This bit's type is R/W.
2	RW	0x0	max_drive_reach_3 This bit field is set to 1 automatically when max driving current level of DP Tx is reached. For more information, refer to MAX_PRE_REACH_3. For test purpose only. This bit's type is RO.
1:0	RW	0x0	drive_current_set_3 Lane 3 output amplitude setting 2'b11: 1200 mV 2'b10: 800 mV 2'b01: 600 mV 2'b00: 400 mV This bit's type is R/W.

EDP_TX_DP_HW_LINK_TRAINING_CTL

Address: Operational Base + offset (0x06A0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	hw_training_error_code Training error code 3'd0: OK 3'd1: AUX_WRITE_ERROR 3'd2: MAX_DRIVE_REACHED 3'd3: WRONG_LANE_COUNT_SETTING 3'd4: LOOP_SAME_5_TIME 3'd5: CR_FAIL_IN_EQ 3'd6: EQ_LOOP_5_TIME
3:1	RO	0x0	reserved
0	RW	0x0	hw_training_en Link training sequence enable Write 1 to enable training sequence, write 0 to force training sequence stop, this bit will self-clear when training done.

EDP_TX_HPD_DEGLITCH_L

Address: Operational Base + offset (0x06C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5e	hpd_deglitch_l HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal This register is HPD_DEGLITCH [7:0]. The default value is 0x5E for 280.75 us deglitch time.

EDP_TX_HPD_DEGLITCH_H

Address: Operational Base + offset (0x06C8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x1a	hpd_deglitch_h HPD_DEGLITCH, which is counted at 24 MHz, is used to de-glitch the HPD signal. This register is HPD_DEGLITCH [13:8]. The default value is 0x1A for 280.75 us deglitch time.

EDP_TX_POLLING_PERIOD

Address: Operational Base + offset (0x06CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x0e	polling_period This register controls the interval between each time of polling operation. Interval time = POLLING_PERIOD * 2^16 * Period of 24M clock.

EDP_TX_DP_LINK_DEBUG_CTL

Address: Operational Base + offset (0x06E0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	new_prbs7 Control the PRBS 7 formula. 1'b1: Use new PRBS7 formula in DP 1.1 version 1'b0: Use old PRBS7 formula in DP 1.0 version
3	RW	0x0	dis_fifo_rst Disable video FIFO reset every line 1'b1: Disable 1'b0: Reset video FIFO every line
2	RW	0x0	disable_auto_reset_encoder Disable 8b/10 encoder auto reset 1'b1: Disabled auto reset 8b/10 encode before sending Link Training Pattern 2 1'b0: Auto reset 8b/10 encode before sending Link Training Pattern 2
1	RO	0x0	reserved
0	RW	0x0	prbs31_en Enable DisplayPort PRBS 31. 1'b1: Enabled 1'b0: Normal mode

EDP_TX_DP_SINK_COUNT

Address: Operational Base + offset (0x06E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_sink_count Sink Count

EDP_TX_DP_IRD_VECTOR

Address: Operational Base + offset (0x06E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_ird_vector Irq_vector

EDP_TX_DP_LINK_STATUS0

Address: Operational Base + offset (0x06EC)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ln1_sybol_lock Lane1 symbol lock

Bit	Attr	Reset Value	Description
5	RW	0x0	ln1_eq_done Lane1 EQ done
4	RW	0x0	ln1_cr_done Lane1 CR done
3	RO	0x0	reserved
2	RW	0x0	ln0_sybol_lock Lane0 symbol lock
1	RW	0x0	ln0_eq_done Lane0 EQ done
0	RW	0x0	ln0_cr_done Lane0 CR done

EDP_TX_DP_LINK_STATUS1

Address: Operational Base + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	inter_ln_align Interlace align
6	RW	0x0	ln3_sybol_lock Lane3 symbol lock
5	RW	0x0	ln3_eq_done Lane3 EQ done
4	RW	0x0	ln3_cr_done Lane3 CR done
3	RO	0x0	reserved
2	RW	0x0	ln2_sybol_lock Lane2 symbol lock
1	RW	0x0	ln2_eq_done Lane2 EQ done
0	RW	0x0	ln2_cr_done Lane2 CR done

EDP_TX_DP_ALIGN_STATUS

Address: Operational Base + offset (0x06F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dp_align_status ALIGN_STATUS

EDP_TX_M_VID_0

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_0 M_VID [7:0]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDP_TX_M_VID_1

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_1 M_VID [15:8]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDP_TX_M_VID_2

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_vid_2 M_VID [23:16]. If FIX_M_VID is 1, this M_VID is used. Otherwise the M_VID value which chip calculated is used.

EDP_TX_N_VID_0

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_0 N_VID[7:0] The maximum value of M_VID is 0xFFFF in ASYNC mode.

EDP_TX_N_VID_1

Address: Operational Base + offset (0x0710)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_1 N_VID[15:8]

EDP_TX_N_VID_2

Address: Operational Base + offset (0x0714)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_vid_2 N_VID[23:16]

EDP_TX_M_VID_MON

Address: Operational Base + offset (0x0718)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_vid_mon This register shows M_VID value which is actually transmitted to Rx for monitoring purpose.

EDP_TX_DP_VIDEO_FIFO_THRD

Address: Operational Base + offset (0x0730)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	video_th_ctrl Video Data FIFO threshold control enables. 1'b1: Video Data FIFO threshold uses VIDEO_TH_VALUE. 1'b0: Video Data FIFO threshold uses internal calculate value automatically.
3:0	RW	0x0	video_th_value Video Data FIFO threshold value. If VIDEO_TH_CTRL is 1, and data count in video data FIFO have reached FIFO threshold value, video data is read out from FIFO.

EDP_TX_DP_GNS_CTRL

Address: Operational Base + offset (0x0734)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	eq_training_loop_control 1: Enable 0: Disable
5	RO	0x0	reserved
4	RW	0x0	scramble_ctrl Scramble formula control: 1'b1: New formula 1'b0: Old formula
3	RW	0x0	in_ex Control scrambler structure: 1'b1: Internal type 1'b0: External type
2	RW	0x0	disable_serdes_fifo_rset 1'b1: Disable serdes FIFO auto reset. 1'b0: Enable serdes FIFO auto reset.
1	RW	0x0	video_map_ctrl Control use or not the video data map in YCbCr 4:2:2 mode: 1'b1: Use video data map in YCbCr 4:2:2 mode 1'b0: Don't use
0	RW	0x0	rs_ctrl Control RS parameter: 1'b1: parameter define by V1.0 1'b0: parameter in GNS

EDP_TX_DP_AUDIO_MARGIN

Address: Operational Base + offset (0x073C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	force_audio_margin Force audio margin 1'b1: Audio margin use register value AUDIO_MARGIN. 1'b0: Audio margin use hardware calculation. It is the default setting.
6:0	RW	0x00	audio_margin Audio packet is sent out during vertical blank or horizontal blank. This register is used to specify minimum stream clock cycles to transfer audio stream packet. If current remaining stream clock cycles before sending active video data is less than the value, DP postpone sending audio stream packets to the next video blank interval. AUDIO_MARGIN only takes effect when FORCE_AUDIO_MARGIN is set 1.

EDP_TX_M_AUD_MON

Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	m_aud_mon This register shows M_AUD value which is actually transmitted to Rx for monitoring purpose.

EDP_TX_M_AUD_0

Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_aud_0 M_AUD [7:0]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDP_TX_M_AUD_1

Address: Operational Base + offset (0x074C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	m_aud_1 M_AUD [15:8]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDP_TX_M_AUD_2

Address: Operational Base + offset (0x0750)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	m_aud_2 M_AUD [23:16]. If FIX_M_AUD is 1, this M_AUD is used. Otherwise the calculated M_AUD value is used.

EDP_TX_N_AUD_0

Address: Operational Base + offset (0x0754)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_0 N_AUD[7:0]

EDP_TX_N_AUD_1

Address: Operational Base + offset (0x0758)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_1 N_AUD[15:8]

EDP_TX_N_AUD_2

Address: Operational Base + offset (0x075C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	n_aud_2 N_AUD[23:16]

EDP_TX_DP_M_CAL_CTL

Address: Operational Base + offset (0x0760)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	m_aud_gen_filter_en Enable M_AUD value generation filter to reduce the variation of M_AUD value. This filter is a low-pass filter to smooth out the M_AUD variation 1'b1: Enable the filter 1'b0: Disable the filter

Bit	Attr	Reset Value	Description
2	RW	0x0	m_vid_gen_filter_en Enable M_VID value generation filter to reduce the variation of M_VID value. This filter is a low-pass filter to smooth out the M_VID variation 1'b1: Enable the filter 1'b0: Disable the filter
1	RO	0x0	reserved
0	RW	0x0	m_gen_clk_sel Select which link clock is used to generate the M value 1'b1: Clock with down spreading is used 1'b0: Clock without down spreading is used

EDP_TX_M_VID_GEN_FILTER_TH

Address: Operational Base + offset (0x0764)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x04	m_vid_gen_filter_th The threshold of M_VID generation filter.It only takes effect when M_VID_GEN_FILTER_EN is set to 1

EDP_TX_M_AUD_GEN_FILTER_TH

Address: Operational Base + offset (0x0778)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	m_aud_gen_filter_th The threshold of M_AUD generation filter. It only takes effect when M_AUD_GEN_FILTER_EN is set to 1

EDP_TX_AUX_CH_STA

Address: Operational Base + offset (0x0780)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	aux_busy AUX channel status bit. If this bit is read as 1, AUX channel access should be halted. 1'b1: AUX CH is busy 1'b0: AUX CH is idle
3:0	RW	0x0	aux_status This register indicate the AUX channel access status 4'd0: OK 4'd1: NACK_ERROR 4'd2: TIMEOUT_ERROR 4'd3: UNKNOWN_ERROR 4'd4: MUCH_DEFER_ERROR 4'd5: TX_SHORT_ERROR 4'd6: RX_SHORT_ERROR 4'd7: NACK_WITHOUT_M_ERROR 4'd8: I2C_NACK_ERROR Other: Reserved

EDP_TX_AUX_ERR_NUM

Address: Operational Base + offset (0x0784)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	aux_err_num The error number counter of AUX channel counts when AUX channel access failed. In AUX CH reading, this number indicates the number of read back byte. In AUX CH writing, this number indicates the number of reply command.

EDP_TX_AUX_CH_DEFER_CTL

Address: Operational Base + offset (0x0788)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	defer_ctrl_en AUX CH received DEFER command count control enable 1'b1: If the count that AUX CH receive DEFER command equal to (DEFER_COUNT * 64), the AUX CH transaction is terminated, and the AUX_STATUS is 0100 1'b0: The count that AUX CH receive DEFER command is unlimited
6:0	RW	0x7f	defer_count The count is defined to limit the max count AUX CH receive DEFER command When DEFER_CTRL_EN is 1 and AUX CH received (DEFER_COUNT * 64) DEFER command, the AUX CH will terminate the transaction

EDP_TX_AUX_RX_COMM

Address: Operational Base + offset (0x078C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_rx_comm AUX CH received command

EDP_TX_BUFFER_DATA_CTL

Address: Operational Base + offset (0x0790)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	buf_clr Write 1 to this bit to clear AUX CH data buffer (BUF_DATA_0 ~ BUF_DATA_15). Always read back 0 from this bit. This bit's type is R/W. This bit is self cleared. Note: For the write operation, set this bit to 1 before writing data to BUF_DATA_0~15. And for READ operation, this bit has only to be set before starting data transfer by setting AUX_EN.
6:5	RO	0x0	reserved
4	RW	0x0	buf_have_data 1'b0: Buffer have data 1'b1: Buffer have not data
3:0	RW	0x0	buffer_data_count The counts of data AUX CH buffer have.

EDP_TX_AUX_CH_CTL_1

Address: Operational Base + offset (0x0794)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	aux_length Register control AUX CH transaction length.
3:0	RW	0x0	aux_tx_comm Register control AUX CH transaction command.

EDP_TX_AUX_ADDR_7_0

Address: Operational Base + offset (0x0798)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_7_0 AUX_ADDR[7:0], Register control AUX CH address.

EDP_TX_AUX_ADDR_15_8

Address: Operational Base + offset (0x079C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	aux_addr_15_8 AUX_ADDR[15:8], Register control AUX CH address

EDP_TX_AUX_ADDR_19_16

Address: Operational Base + offset (0x07A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	aux_addr_19_16 AUX_ADDR[7:0], Register control AUX CH address.

EDP_TX_AUX_CH_CTL_2

Address: Operational Base + offset (0x07A4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	pd_aux_idle Power down AUX CH when AUX CH is in idle state. 1'b1: Power down AUX CH in idle state. 1'b0: Keep AUX CH power up in idle state.
2	RW	0x0	aux_pn_inv Invert AUX CH PN 1'b1: Invert PN 1'b0: Normal mode
1	RW	0x0	addr_only AUX CH issue "address only" command 1'b1: Issue "address only" command 1'b0: Normal AUX CH command
0	RW	0x0	aux_en Register control AUX CH operation enable Write 1 to this bit to enable AUX CH operation This bit will self-clear when AUX CH operation is finished. This bit is self cleared.

EDP_TX_BUF_DATA

Address: Operational Base + offset (0x07C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xff	buf_data AUX CH buffer data 0 ~ 15

EDP_TX_SOC_GENERAL_CTL

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	audio_bit_mapping_type Audio bit mapping type in 16bit audio mode 2'd0: Type 0 2'd1: Type 1 2'd2: Type 2 2'd3: Reserved
15	RO	0x0	reserved
14:13	RW	0x0	pcm_size PCM data bit size 2'b00: 16 bit 2'b01: 20 bit 2'b10: 24 bit 2'b11: Reserved
12:5	RO	0x00	reserved
4:0	RW	0x00	audio_ch_status_same Select the channel status bits for audio channel 3~8. 1'b1: Use the same data channel status bits from AUDIO_GP0_STATUS_n registers. 1'b0: Use each channel status bits from the corresponding AUDIO_GPx_STATUS_n registers.

EDP_TX_DP_TEST_80B_PATTERN0

Address: Operational Base + offset (0x081C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern0 DP test 80bit pattern0[29:0]

EDP_TX_DP_TEST_80B_PATTERN1

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	dp_test_80b_pattern1 DP test 80bit pattern0[59:30]

EDP_TX_DP_TEST_80B_PATTERN2

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	dp_test_80b_pattern2 DP test 80bit pattern0[79:60]

EDP_TX_AUD_CTL

Address: Operational Base + offset (0x0834)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	aud_channel_count Audio Channel Number 3'b001: 2 channel 3'b011: 4 channel 3'b101: 6 channel

EDP_TX_CRC_CON

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	vid_crc_flush Video CRC flush enable. The video CRC value is initialized at every v-sync.
1	RO	0x0	reserved
0	RW	0x0	vid_crc_enable Video CRC enable. 1'b0: Disable 1'b1: Enable

EDP_TX_CRC_RESULT

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	aud_crc_result Audio CRC result
15:0	RW	0x0000	vid_crc_result Video CRC result

EDP_TX_I2S_CTRL

Address: Operational Base + offset (0x09C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_en I2S enable
3:0	RW	0x0	i2s_fmt_ctrl I2S Format Control

EDP_TX_I2S_CH_SWAP

Address: Operational Base + offset (0x09CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	i2s_ch_swap I2S channel swap
3:0	RW	0xb	i2s_wd_len I2S word length

EDP_TX_I2S_CH_CTRL

Address: Operational Base + offset (0x09D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xe4	i2s_ch_ctrl I2S channel control

EDP_TX_I2S_CH_CTRL1

Address: Operational Base + offset (0x09D4)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	i2s_aud_layout Audio layout
1	RW	0x0	i2s_aud_v_bit Audio v_bit
0	RW	0x0	i2s_aut_ext_sta Audio ext channel status

EDP_TX_LINK_POLICY

Address: Operational Base + offset (0x09D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	alternate_sr_en Alternate SR enable
6:4	RW	0x5	link_train_cr_lp_in Link training CR loop in
3	RW	0x0	link_train_wr_en Training first write en
2	RO	0x0	reserved
1	RW	0x0	link_train_inv Invert training bit enable
0	RW	0x0	frame_change_en Framing change enable

31.5 Interface Description

Table 31-1 EDP TX PHY Interface Description

Module Pin	Direction	Pin Name	Descriptions
EDP_PHY_AUXN	I/O	EDP_PHY_AUXN	Auxiliary channel bidirectional IO, negative terminal
EDP_PHY_AUXP	I/O	EDP_PHY_AUXP	Auxiliary channel bidirectional IO, positive terminal
EDP_PHY_TXM0	O	EDP_PHY_TXM0	Serial data output of channel 0,negative terminal
EDP_PHY_TXP0	O	EDP_PHY_TXP0	Serial data output of channel 0, positive terminal
EDP_PHY_TXM1	O	EDP_PHY_TXM1	Serial data output of channel 1,negative terminal
EDP_PHY_TXP1	O	EDP_PHY_TXP1	Serial data output of channel 1, positive terminal
EDP_PHY_TXM2	O	EDP_PHY_TXM2	Serial data output of channel 2,negative terminal
EDP_PHY_TXP2	O	EDP_PHY_TXP2	Serial data output of channel 2, positive terminal
EDP_PHY_TXM3	O	EDP_PHY_TXM3	Serial data output of channel 3,negative terminal
EDP_PHY_TXP3	O	EDP_PHY_TXP3	Serial data output of channel 3, positive terminal

31.6 Application Notes

31.6.1 START-UP Sequence for PHY

Before power up the PHY, make sure the power supply and the reference clock is ready for operation. A proposed power up sequence is like this:

- step 1

Power up the chip and do power on reset detection. There include a reset detection

function in PHY, the duration for reset detection is less than 100us.

- step 2

Write registers, load parameters, and prepare to power up.

- step 3

Make sure the reference clock source is ready for operation, release pd_pll. Before release tx_pd[N], must set tx_mode[1:0]=11, then release tx_pd[N], set tx_idle[N]=1.

- step 4

When PLL gets locked, the internal clock is ready for use, digital can send data.

- step 5

Set tx_idle[N] = 0 to start normal operation, TXPN/TXMN will change from common-mode to data-mode.

The detail of EDP TX PHY configure register is in CH5 GRF 1.11 EDP_PHY Register Description.

The tx_pd[N] means EDP_PHY_GRF_CON0 bit 7:4

The tx_idle[N] means EDP_PHY_GRF_CON0 bit 11:8

The tx_mode means EDP_PHY_GRF_CON5 bit 9:8

31.6.2 Settings About EDP TX PHY

The more detail of EDP TX PHY configure register is in CH5 GRF 1.11 EDP_PHY Register Description.

The setting of registers is below:

- Link rate 2.7GHz

The default configuration is at 2.7GHz, so it do not need configure anything.

- Link rate 1.62GHz

Set EDP_PHY_GRF_CON1 bit [14:0] = 0x4380

Set EDP_PHY_GRF_CON2 bit [5:4] = 0x1

- Power down lane

EDP_PHY_GRF_CON0 bit [7:4] can power down each lane independently.

31.6.3 Setting for HPD IO

There are HPD 0 and 1 which can be selected by IOMUX.

For HPD 0,

Set GRF_GPIO4C_IOMUX_H bit[2:0] = 0x1

Set GRF_IOFUNC_SEL0 bit [6] = 0x0

For HPD 1,

Set PMU_GRF_GPIO0C_IOMUX_L bit [10:8] = 0x2

Set GRF_IOFUNC_SEL0 bit [6] = 0x1

31.6.4 eDP TX Controller Programming Guide

1.6.4.1 How to initialize DP

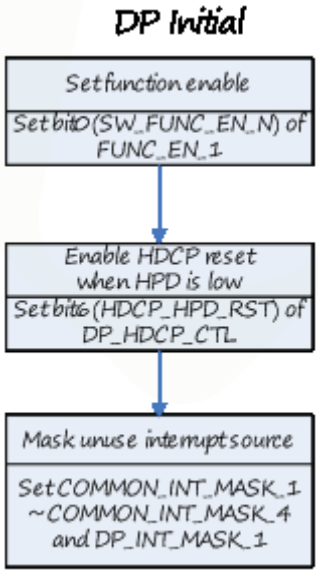


Fig. 31-2 DP Initial

1.6.4.2 How to Detect hot plug insertion

In Wait Hot plug state, chip is in power down status. System only responses to hot plug change interrupt. When a hot plug interrupt is detected, in the interrupt routine, firmware will judge whether it is a receiver plug-in or un-plug or link training request. If plug-in, chip will be powered on and system state will be set to Read and Parse EDID.

1.6.4.3 How to access DPCD space in DP Rx

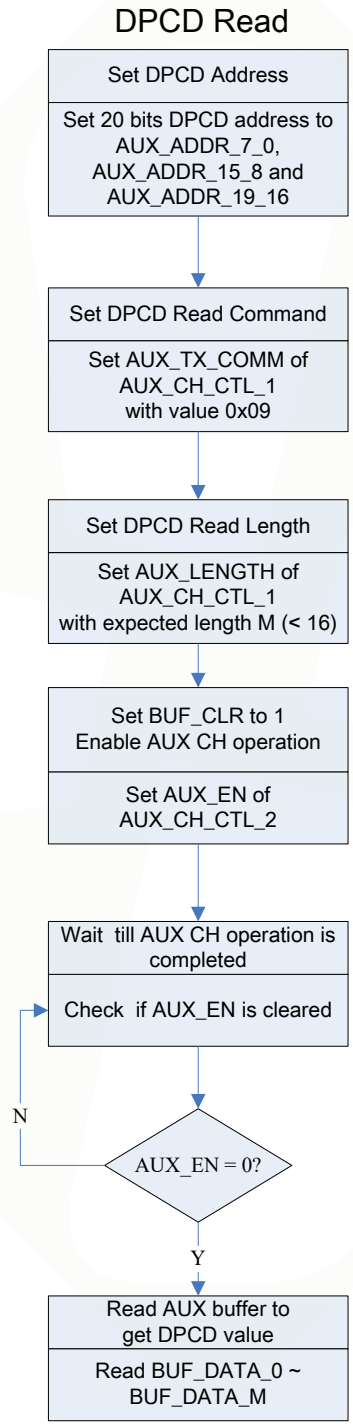


Fig. 31-3 DPCP Read

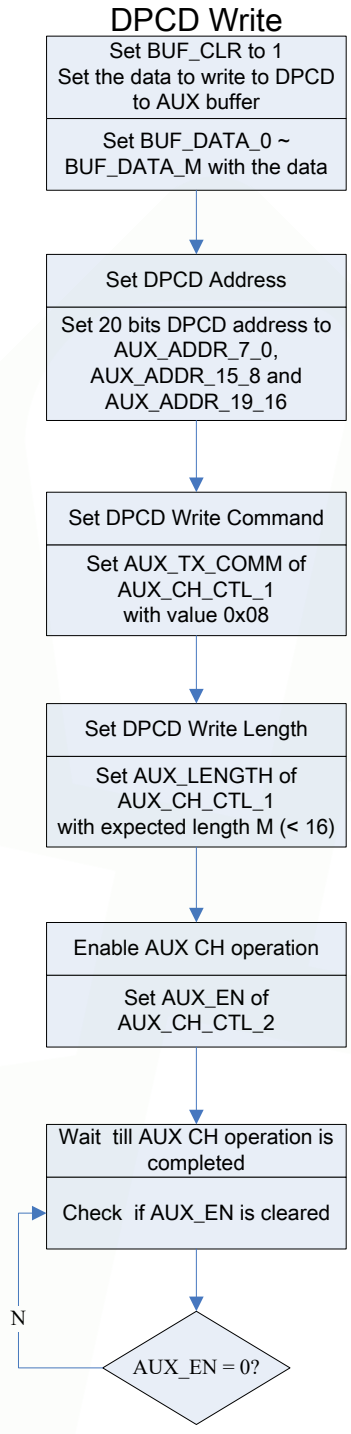


Fig. 31-4 DPCP Write

1.6.4.4 How to Write into EDID space in DP Rx

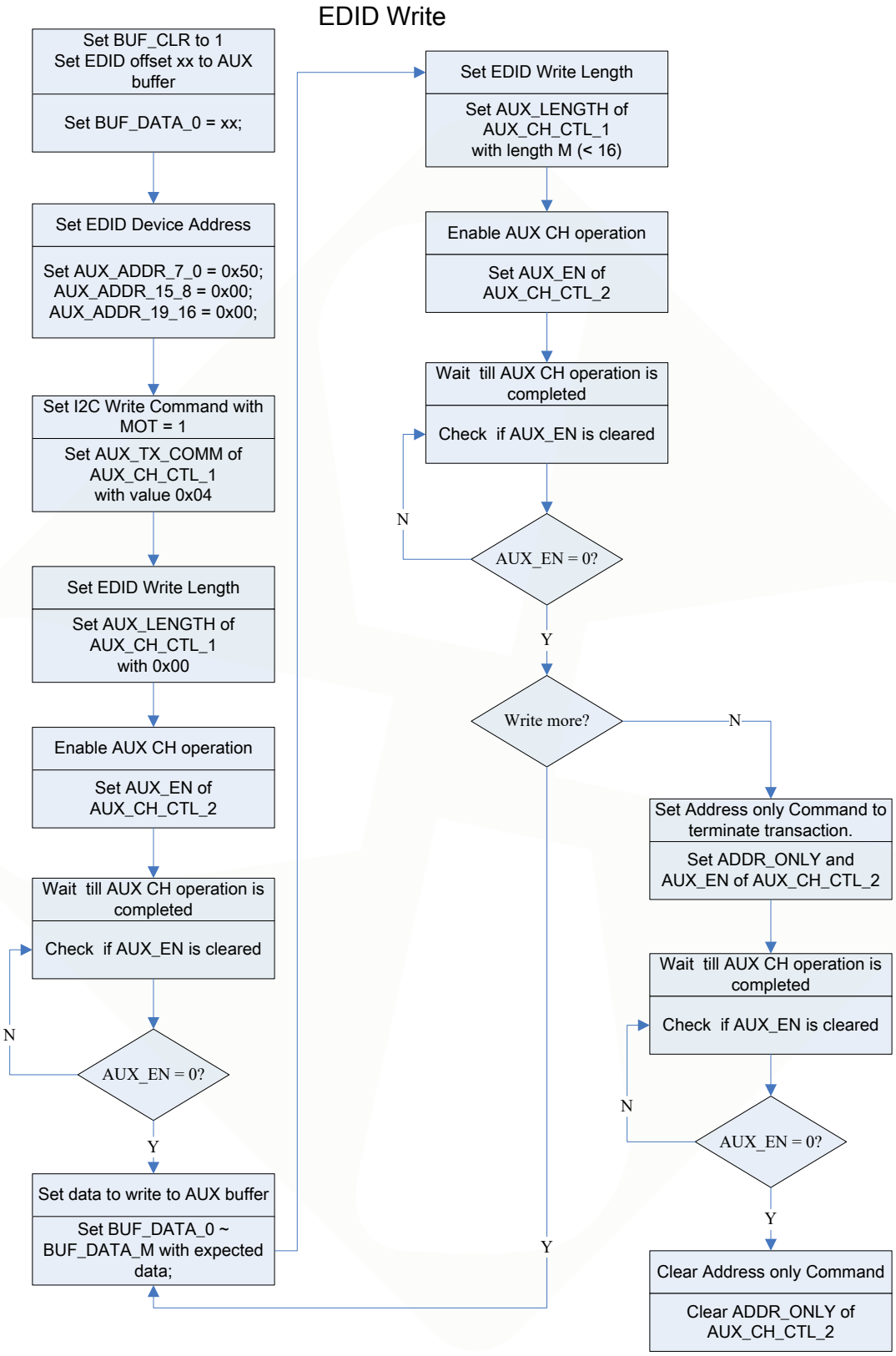


Fig. 31-5 EDID Write

1.6.4.5 How to Read from EDID space in DP Rx

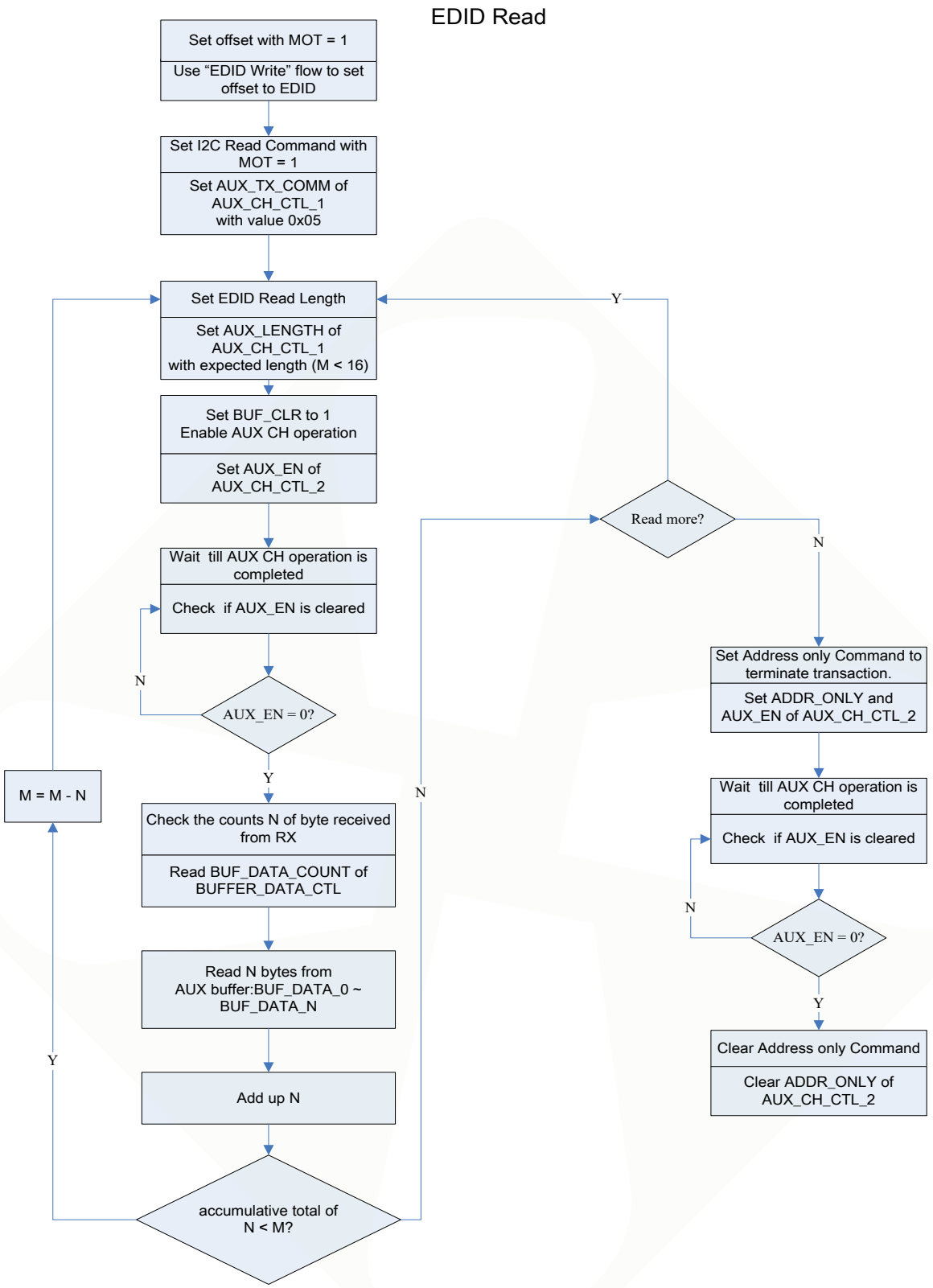


Fig. 31-6 EDID Read

1.6.4.6 How to do SW link training

- State Machine of SW Link Training

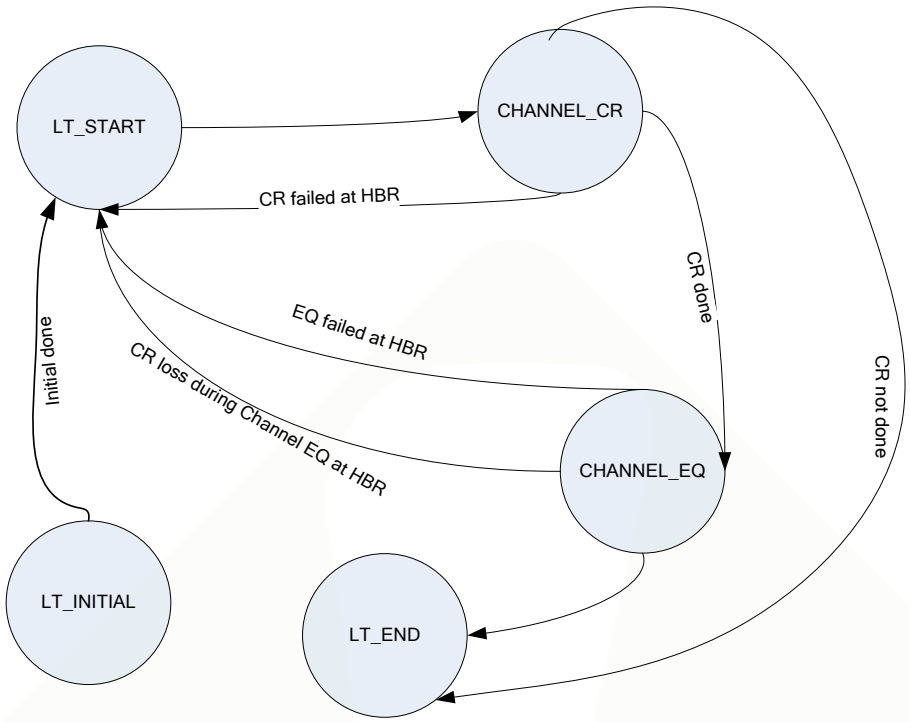


Fig. 31-7 State Machine of SW Link Training

- State LT_INITIAL

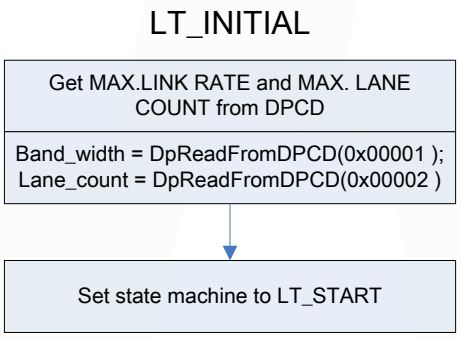


Fig. 31-8 State LT_INITIAL

- State LT_START

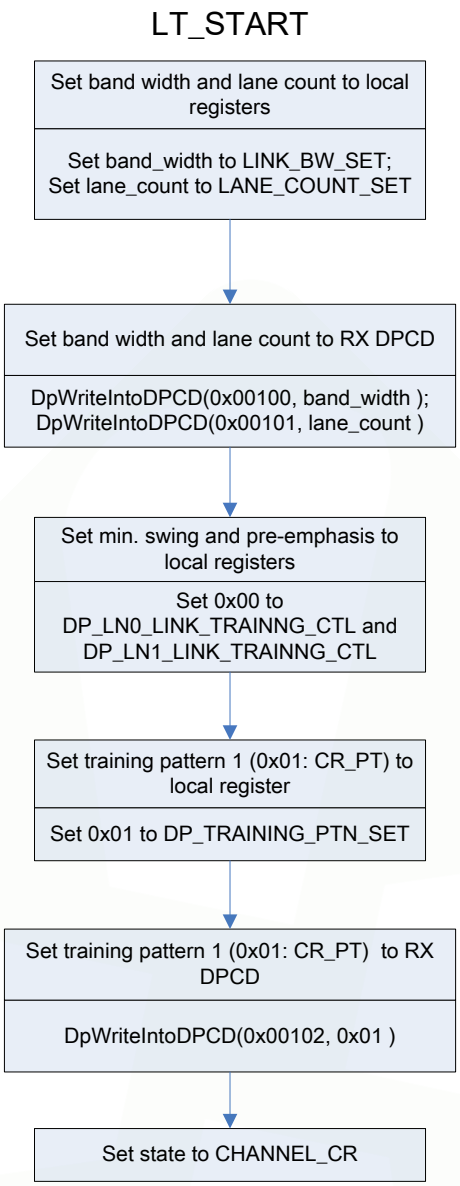


Fig. 31-9 State LT_INITIAL

- State CHANNEL_CR

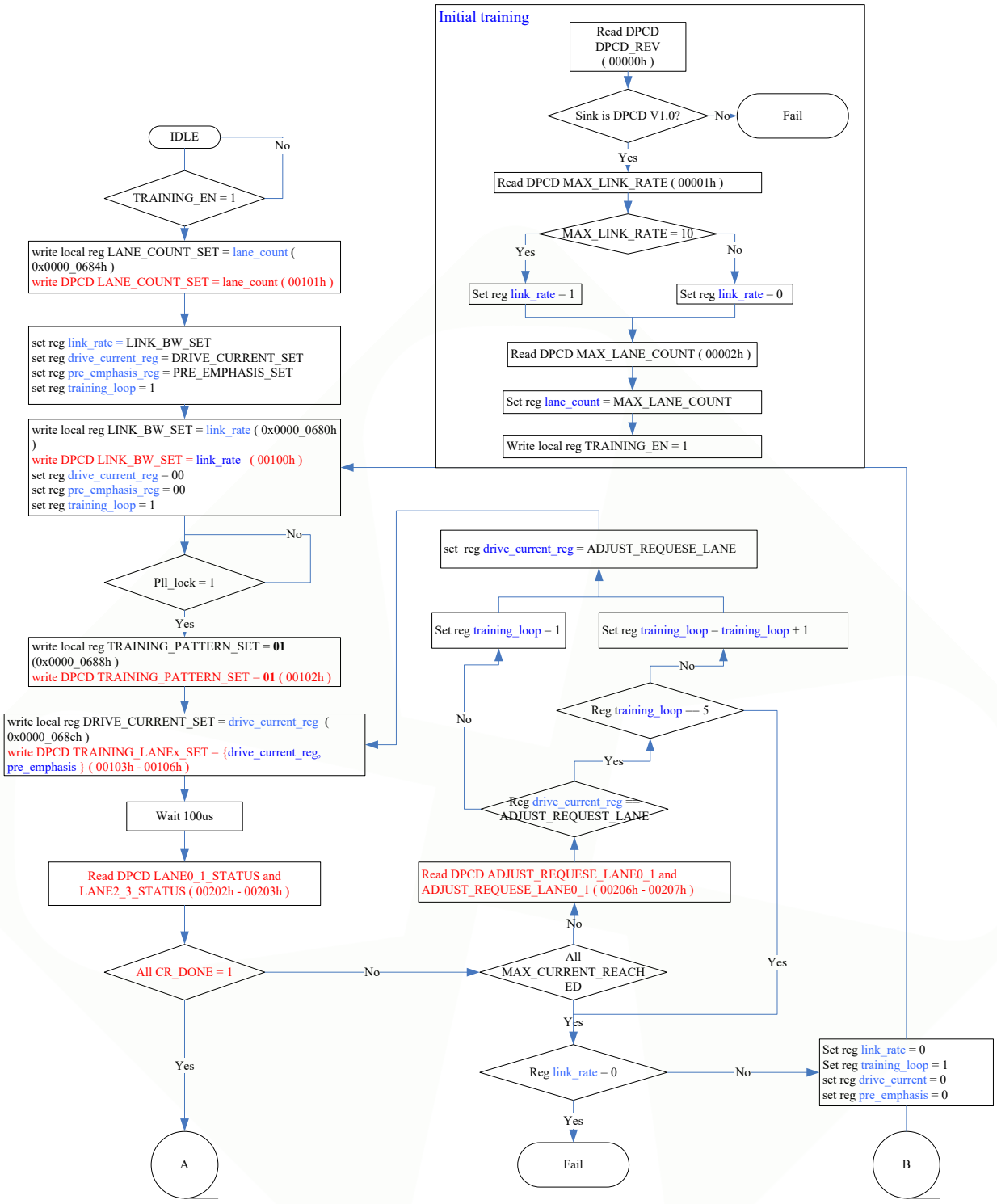
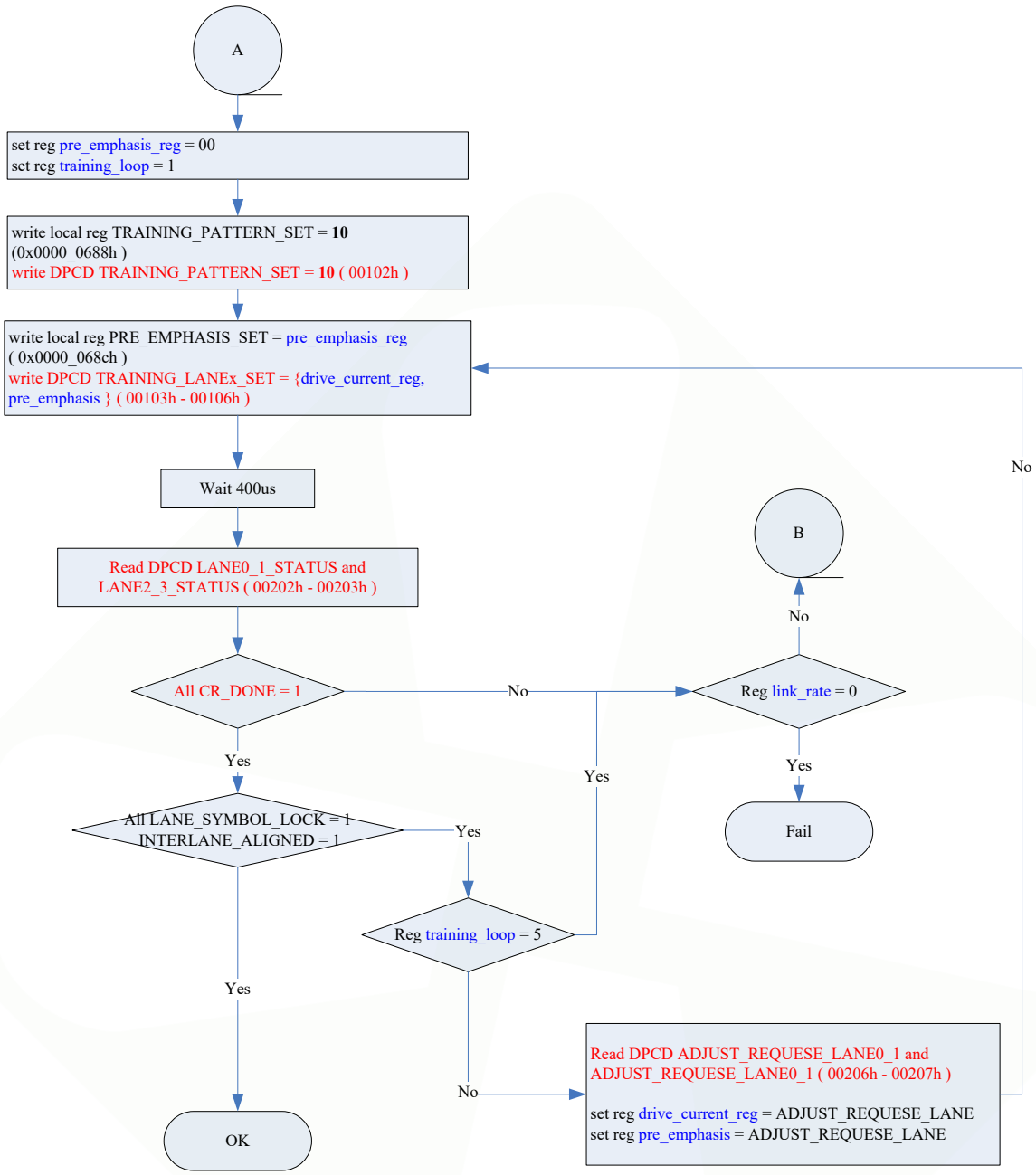


Fig. 31-10 State CHANNEL_CR

- State CHANNEL_EQ



Note : link_rate, lane_count, drive_current_reg, pre_emphasis_reg and training_loop are temporary variables.

Fig. 31-11 State CHANNEL_EQ

1.6.4.7 How to setup main stream attribute data

- Attribute of Video timing

Chip hardware setups attribute of video timing automatically.

- Attribute of Color Depth

Set IN_BPC of with VIDEO_CTL_2 correct value.

- Attribute of Color Space

Set IN_COLOR_F of VIDEO_CTL_2 with correct value.

IN_YC_COEFFI of VIDEO_CTL_3 [7] also must be set.

1.6.4.8 How to do HDCP authentication and encryption

- SW HDCP State Machine

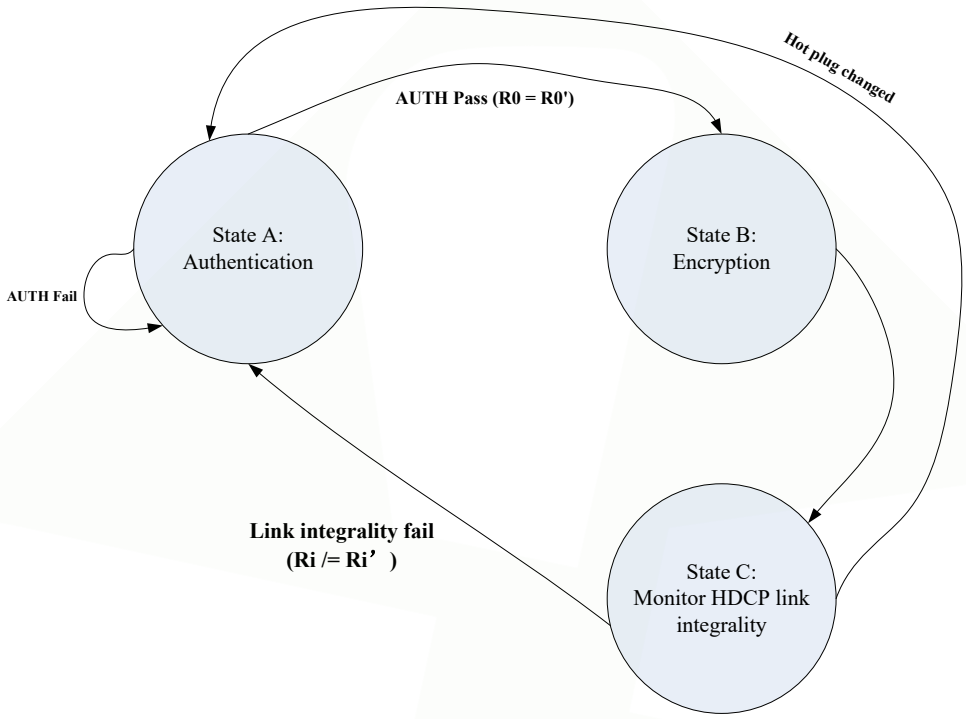


Fig. 31-12 SW HDCP State Machine

- SW HDCP Flowchart

Note that BKSV to BKSV0~BKSV4 are loaded two times in step2 and in step5 in figure 1-13. With the first BKSV writing, AKSV starts to be loaded and SW_STORE_AN function is enabled. As another function, validity of BKSV is possible by the bit filed, BKSV_VALID. In the other hand, the second BKSV writing starts the R0 calculation.

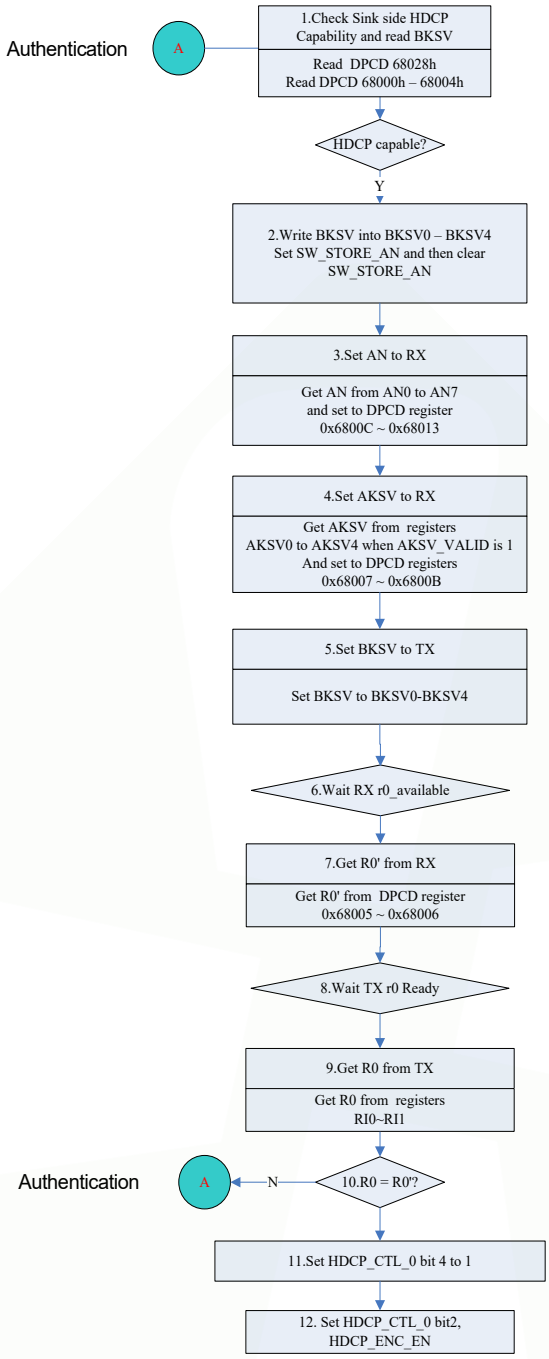


Fig. 31-13 SW HDCP Flowchart 0

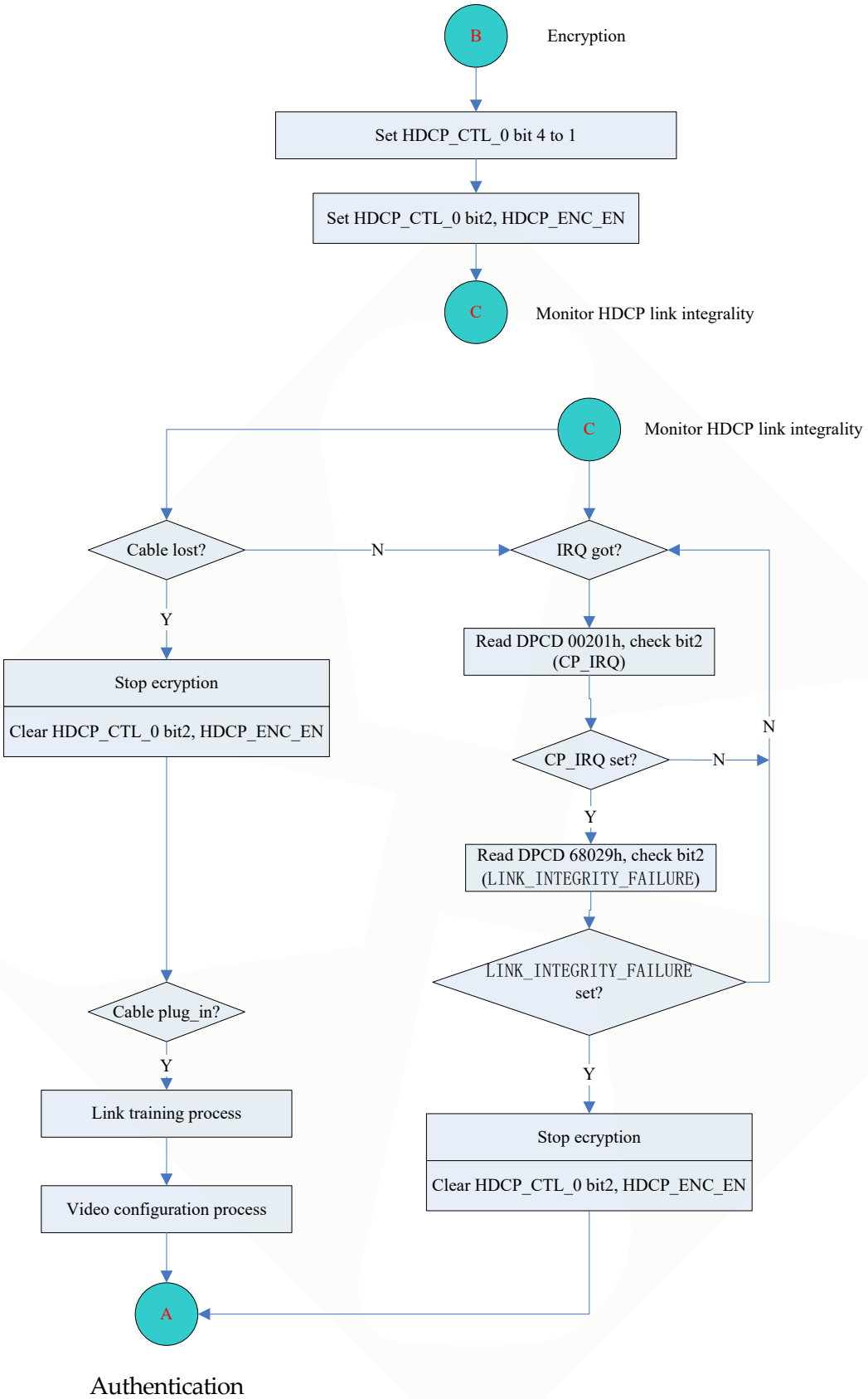


Fig. 31-14 SW HDCP Flowchart 1

1.6.4.9 How to configure video

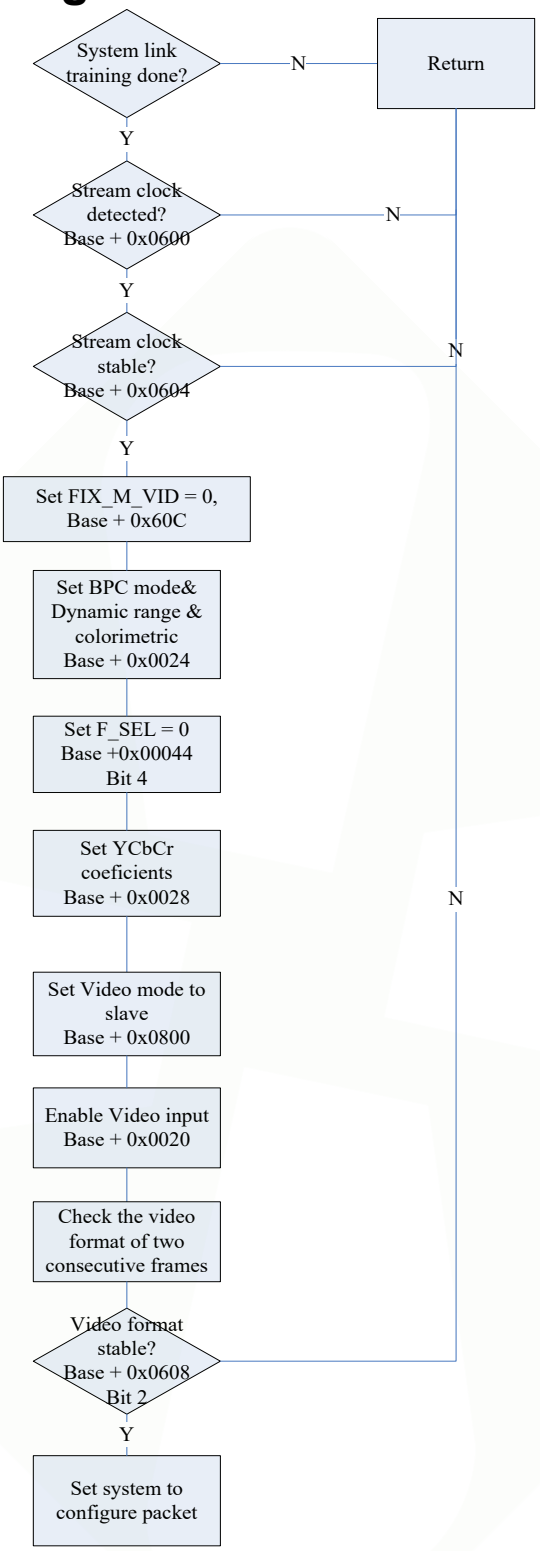


Fig. 31-15 Configure Video Flowchart

Slave mode video configuration process (M value auto-generated)

Note: Usually, you do not need to set FIX_M_VID to 1. If FIX_M_VID is 0, then the hardware calculated M_VID value is used. But, if FIX_M_VID must be set to 1 by any reason, then M_VID_0, M_VID_1 and M_VID_2 should be set by using following formula.

M_VID = FSTRM_CLK * N_VID / FLS_CLK

N_VID must be choose let the result of this equation is an integer, for example N_VID is 13500 (0x34bc) in 2.7G and 8100 (0x1fa4) in 1.62G.

2.7G: M_VID = F_STRM_CLK*0x34BC/135M

1.62G: M_VID = F_STRM_CLK*0x1FA4/81M

For example, if input is 1400x1050/108M, RGB888, 2.7G,
M_VID = 108*0x34BC/135= 0x2A30,
set M_VID_0 = 0x30, set M_VID_1 = 0x2A, set M_VID_2 = 0.

1.6.4.10 How to configure audio

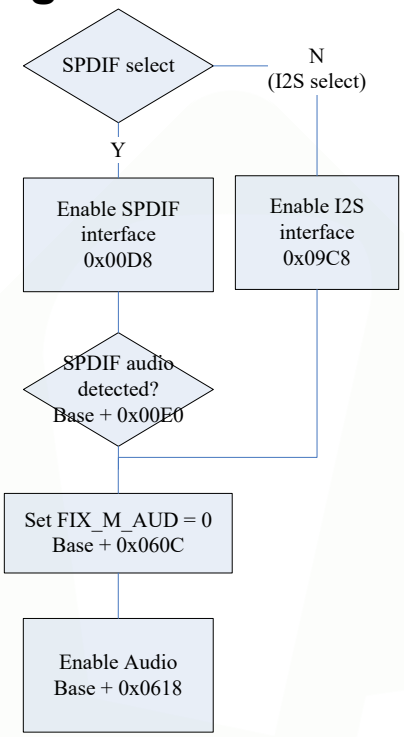


Fig. 31-16 Slave mode audio configuration process (M value auto-generated)

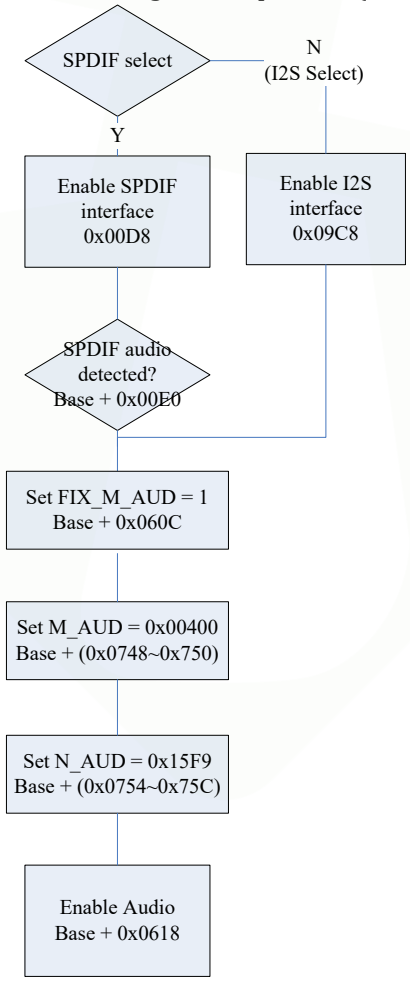


Fig. 31-17 Slave mode audio configuration process (Register defined M value, 48 KHz, 2.7 G)

Note: Usually, you do not need to set FIX_M_AUD to 1. If FIX_M_AUD is 0, then the hardware calculated M_AUD value is used. But, if FIX_M_AUD must be set to 1 by any reason, then M_AUD_0, M_AUD_1, M_AUD_2 and N_AUD_0, N_AUD_1, N_AUD_2 should be set by using following formula.

M_AUD = 512*Faud_sample* N_AUD / 2 * Fls_clk

2.7G M_AUD = 512*Faud_sample *N_AUD/270,000,000

1.62G M_AUD = 512*Faud_sample*N_AUD/162,000,000

1.6.4.11 How to PROCESS interrupt

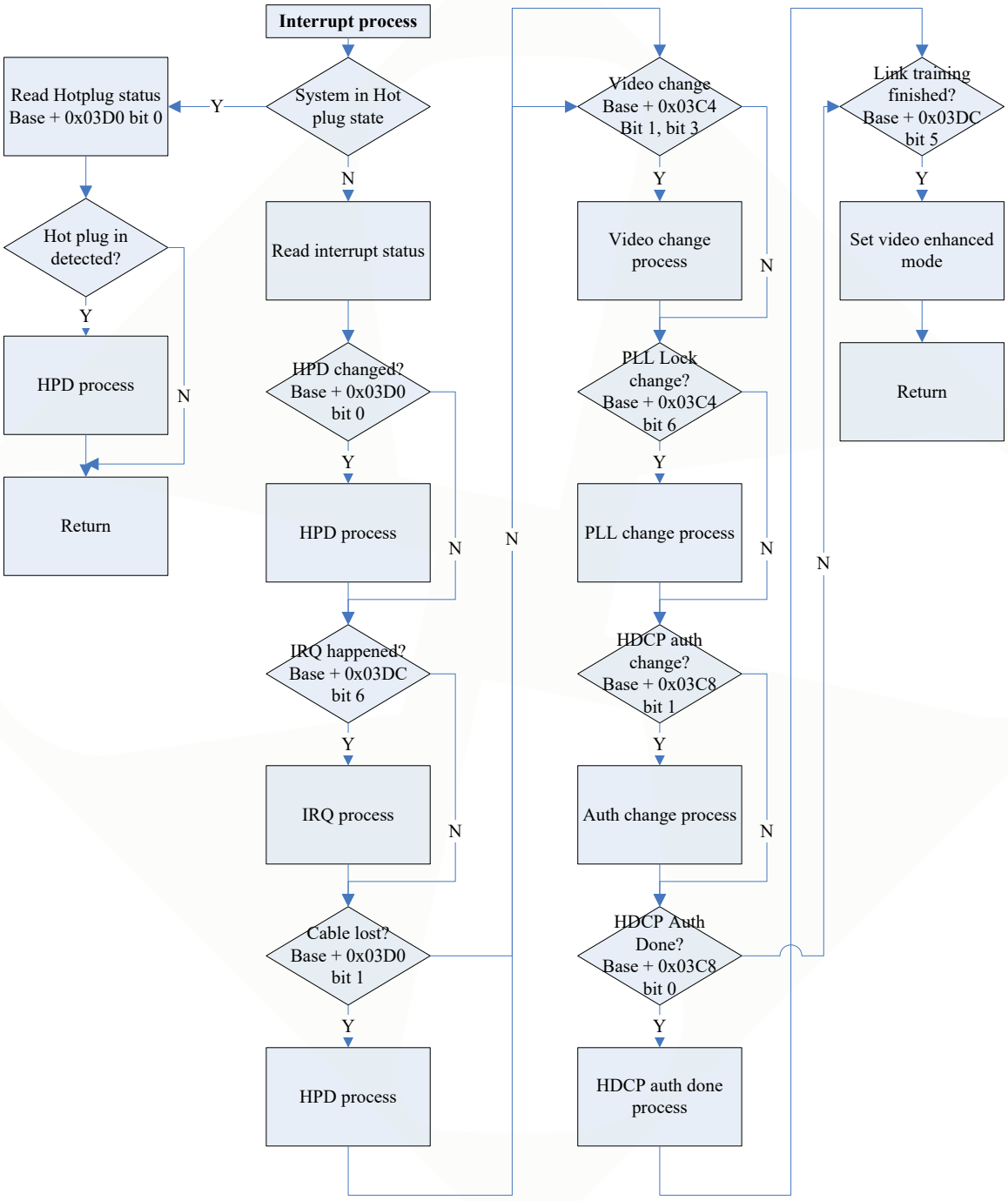


Fig. 31-18 Interrupt process

1.6.4.12 How to Send Secondary-data Packets

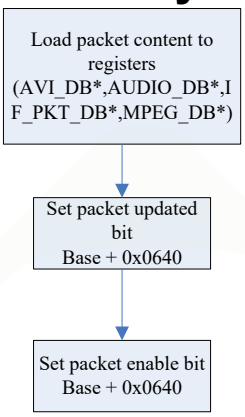


Fig. 31-19 Send Secondary-data Packets

Chapter 32 HDMI TX

32.1 Overview

HDMI TX is fully compliant with HDMI 1.4a and 2.0a specification. It offers a simple implementation for consumer electronics like DVD/player/recorder and camcorder. HDMI TX consists of one HMDI transmitter controller and one HMDI transmitter PHY.

It supports following features:

- Video formats:
  - All CEA-861-E video formats up to 1080p at 60 Hz and 720p/1080i at 120 Hz
  - HDMI 1.4b video formats
    - All CEA-861-E video formats up to 1080p at 120 Hz
    - HDMI 1.4b 4K x 2K video formats
    - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
  - HDMI 2.0 video formats, All CEA-861-F video formats
- Colorimetry, 24-bit RGB 4:4:4
- Pixel clock from 13.5 MHz up to 600 MHz
- Up to 192 kHz IEC60958 audio sampling rate
- Flexible synchronous enable per clock domain to set functional power down modes
- AMBA APB 3.0 register access
- I2C DDC, EDID block read mode
- SCDC I2C DDC access
- TMDS Scrambler to enable support for 2160p@60Hz with RGB 4:4:4
- Integrated CEC hardware engine

32.2 Block Diagram

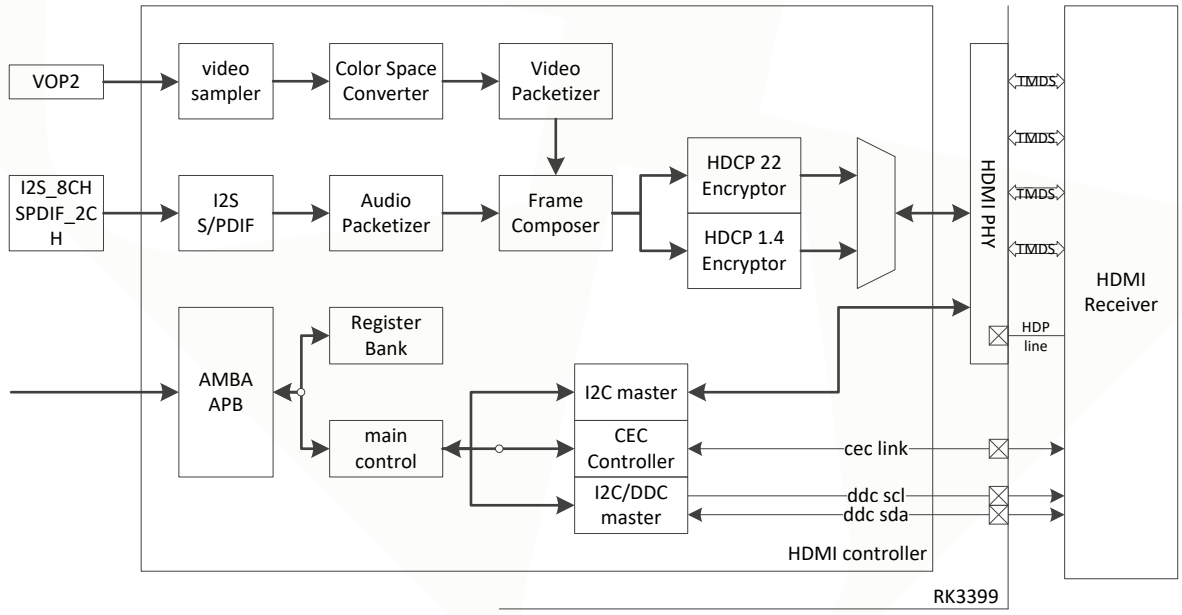


Fig. 32-1 HDMI TX Block Diagram

32.3 Function Description

32.3.1 IOMUX

Customer should notice that CEC channel use IO_HDMITXcecm0_SPI3cs1m1_VCCIO7GPIO4d1 and DDC channel use PAD IO_HDMITXscl_I2C5sclm1_VCCIO7GPIO4c7 and

IO_HDMITXsda_I2C5sdam1_VCCIO7GPIO4d0.

Note: PAD IO_HDMI_DDCCEC is Ground reference for the Hot Plug Detect signal.

32.3.2 Video Data Processing

The video processing contains video format timings, pixel encodings (RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

The input video pixels can be encoded in either RGB, YCBCR 4:4:4 or YCBCR 4:2:2 formats by Color Space Conversion block.

The input Video data can have a pixel size of 24bits. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

Color Space Conversion

HDMI Transmitter Color space conversion (CSC) is responsible for carrying out the following video color space conversion functions:

- RGB to/from YCbCr
- 4:2:2 to/from 4:4:4 up (pixel repetition or linear interpolation)/down-converter
- Limited to/from full quantization range conversion
- The CSC supports all the timings reported in the CEA-861-D specification and the following pixel modes:
- RGB 444 and YCbCr 444: 24, 30, 36, and 48 bits
- YCbCr 422: 16, 20, and 24 bits

The color space conversion matrix is ruled by the following equations listed in below figure.

$$out_1 = (X_1 \times in_1/4096 + X_2 \times in_2/4096 + X_3 \times in_3/4096 + X_4) \times 2^{scale}$$
$$out_2 = (Y_1 \times in_1/4096 + Y_2 \times in_2/4096 + Y_3 \times in_3/4096 + Y_4) \times 2^{scale}$$
$$out_3 = (Z_1 \times in_1/4096 + Z_2 \times in_2/4096 + Z_3 \times in_3/4096 + Z_4) \times 2^{scale}$$

Fig. 32-2 HDMI Color Space Conversion Matrix Equations

Note: Color Space Conversion to and from YCrCb 4:2:0 is not supported.

32.3.3 Audio Data Processing

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks

The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.

The scheme of audio processing as shown in the figure below:

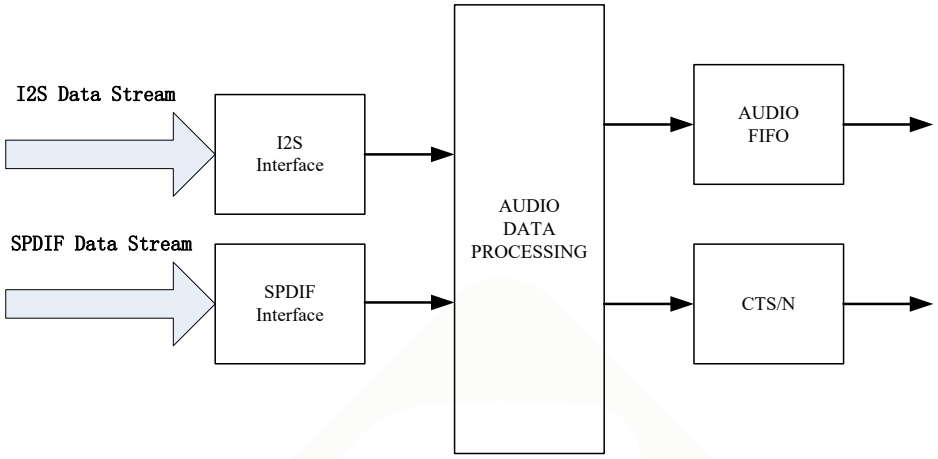


Fig. 32-3 HDMI Audio Data Processing Diagram

1.I2S

The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table 32-1 HDMI TX I2S 2 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 32-2 HDMI TX I2S 8 Channel Audio Sampling Frequency

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.SPDIF

The function of this module is to implement SPDIF audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. SPDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. SPDIF input supports audio sampling rates from 32 to 192 KHz. The following shows the SPDIF audio formats that are supported for each of the video formats

Table 32-3 HDMI SPDIF Sampling Frequency at Each Video Format

Video Format	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz

720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	No	No
1440x480i/ 1440x576i	Yes	Yes	Yes	Yes	Yes	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

3.Audio Sample Clock Capture and Regeneration

Audio data is carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sink then re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be.

$128 \cdot f_s = f_{TMDS\_clock} * N / CTS$.

The scheme of the Audio Sample Clock Capture and Regeneration as shown below:

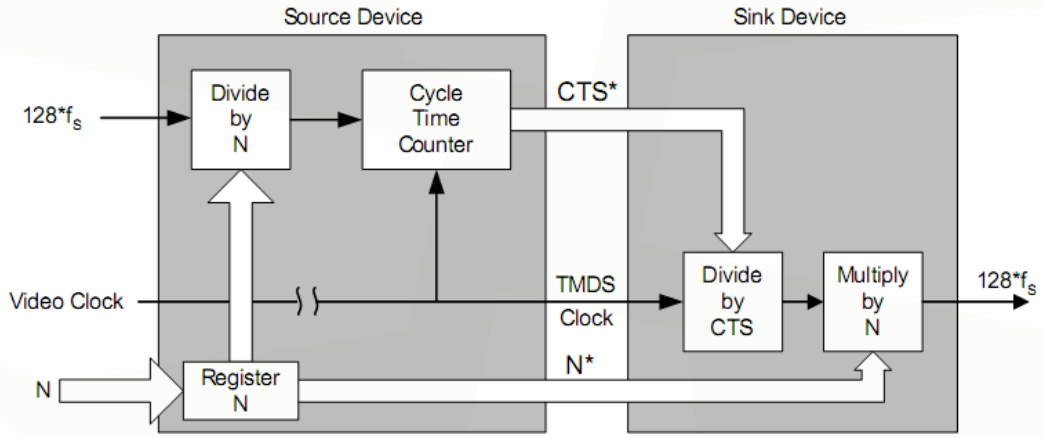


Fig. 32-4 HDMI Audio Clock Regeneration Model

Because there is no audio clock carried through the HDMI link, only the TMDS clock is used. Software sets the CTS/N with a value taken form the below table, which shows the CTS and N value for the supported standard. All other TMDS clocks are not supported; The TMDS clocks divided or multiplied by 1,001 coefficients are not supported.

Table 32-4 HDMI CTS and N table

	TMDS Clock (MHz)													
	25.2		27		54		74.25		148.5		297		597	
Fs (kHZ)	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS	N	CTS
32	4096	25200	4096	27000	4096	54000	4096	74250	4096	148500	3072	222750	3072	445500
44.1	6272	28000	6272	30000	6272	60000	6272	82500	6272	165000	4704	247500	9408	990000
48	6144	25200	6144	27000	6144	54000	6144	74250	6144	148500	5120	247500	6144	495000
88.2	12544	28000	12544	30000	12544	60000	12544	82500	12544	165000	9408	247500	18816	990000
96	12288	25200	12288	27000	12288	54000	12288	74250	12288	148500	10240	247500	12288	495000
176.4	25088	28000	25088	30000	25088	60000	25088	82500	25088	165000	18816	247500	37632	990000
192	24576	25200	24576	27000	24576	54000	24576	74250	24576	148500	20480	247500	24576	4950000

32.3.4 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HMDI Transmitter Controller has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

32.3.5 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

32.3.6 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

It supports up to HDCP 2.2. HDCP 1.4 is done by HDMI Transmitter itself. HDCP22 is descripted in another chapter.

32.3.7 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

32.3.8 TMDS encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data.

HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

32.3.9 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

32.4 HDMI PHY

The HDMI Tx PHY is the physical layer of an HDMI digital transmitter (source), capable of encoding and transmitting high-speed data streams carrying RGB video, audio, and control information.

The HDMI Tx PHY includes one PLL that synthesizes the high-speed serial bit clock (required by the transmitter) from a reference pixel clock with a frequency that can vary between 13.5-600 MHz for HDMI operation. The transmitter is capable of transmitting up to 18 Gbps using three lanes for HDMI operation.The HDMI Tx PHY has one i2c config bus,which is driven by hdmitx controller.

The HDMI Tx PHY drives audio and video across the TMDS data channels. For HDMI operation, each serial TMDS link has a data-rate range of 0.25-6 Gbps. The HDMI Tx PHY also drives the TMDS clock at 1/10th of the serial data rate with a frequency range of 25-340 MHz for data rates below 3.4Gbps. For a serial data rate between 3.4Gbps and 6Gbps, the HDMI Tx PHY drives the TMDS clock at 1/40th of the serial data rate.

Within the HDMI Tx PHY, additional support blocks exist:

- Bandgap block (for blocks biasing)
- Resistor Calibration block
- ADC
- Analog test bus
- Built-in Self-Test(BIST)

An external, 1.62-kΩ reference resistor (connected to ground) is required for precise current and biasing (within each block).

32.4.1 I2C interface

The HDMI Tx PHY's status and configuration is accessed through internal I2C interface. The internal I2C interface is mapped to PHY Configuration Registers in HDMI TX registers at address 0x3000. Customers can access these registers though HDMI controller's Register. Operating to these register can trigger one i2c write process or i2c read process.

32.4.2 PLL Operation

The PLL is responsible for the generation of the high-speed serialization clocks, as well as for the other clocks involved on the data transmission (clocks on the TMDS lanes) or involved on the supported testability.

The PLL can be configured for the video modes required for each of the supported modes of operation. For additional information about the PLL configuration, please refer "PHY MPLL Configuration".

32.4.3 HPD/RXSENSE Operation

For HDMI operation, to detect the presence of an HDMI sink system, the HDMI Tx PHY supports two different mechanisms to determine whether a Hot Plug Detect (HPD) signal is available and whether HDMI sink terminations are present and powered.

If voltage is present on the HPD line provided by the HDMI sink system, the HPD circuit identifies and asserts the SNKDET signal on the PHY's digital interface, provided the voltage level is 2.4-5.3 V, as specified by the HDMI specification. The HPD circuit enables the HDMI Tx PHY to identify whether the HDMI sink system is connected and is providing a correct HPD voltage level.

The RXSENSE circuit determines, for each TMDS data and clock lane for the HDMI operation, whether the HDMI sink terminations are present. Users can observe RXSENSE that reflects the state of the TMDS lanes evaluated from phy_stat0 in HDMI controller register.

32.4.4 Power Collapsing

The HDMI Tx PHY supports power collapsing. This feature enables the HDMI Tx PHY to stay—in any given combination of power supply availability (present, floating, or grounded)—in a known state with low current consumption. This low current consumption remains similar to, or below, the current consumption in power-down mode.

Power collapsing provides customers who require control over the power lines with independent control of the PHY power supplies.

32.4.5 Operating Modes

The HDMI Tx PHY can be placed in two different operating modes: Power-Down and Active. Customers can assert a soft reset through the HDMI control registers 0x302a,with configuration 0. This soft reset clears all system FSMs except I2C, JTAG, and control registers.

For each separate video mode in which the HDMI Tx PHY is set to transmit, due to different operating frequency, color depth and pixel repetition that characterizes each one, you need to configure the HDMI Tx PHY block for correct operation and optimized performance. It is recommended for the PHY configuration through the I2C or JTAG interface to be done while the PHY is in power-down mode.

Configuration involves programming the PLL dividers and analog configuration as well as the analog drivers' source termination value, signals voltage level, pre-emphasis and slope boosting. This programming is done through the I2C interface.

32.5 Register Description

The address offset of the HDMI TX is 0xff9480000,it contains 16 address section. The offset of the table of Register Summary must multiple with 4 when software configure it。Like the Interrupt registers，its base address is 0x0100.If we want to configure it, its real address is 0xff980000+0x0100*4.

32.5.1 Register Summary

Name	Offset	Size	Reset Value	Description
Identification Registers	0x0000	B		Identification releated registers
Interrupt registers	0x0100	B		Interrupt releated registers
Video Sampler registers	0x0200	B		Video Sampler registers
Video Packetizer registers	0x0800	B		Video Packetizer registers
Frame Composer Registers	0x1000	B		Frame Composer Registers
HDMI Source PHY Registers	0x3000	B		HDMI Source PHY Registers
I2C Master PHY Registers	0x3020	B		I2C Master PHY Registers
Audio Sampler Registers	0x3100	B		Audio Sampler Registers

Name	Offset	Size	Reset Value	Description
Main Controller Registers	0x4000	B		Main Controller Registers
Color Space Converter Registers	0x4100	B		Color Space Converter Registers
HDCP Encryption Engine Registers	0x5000	B		HDCP Encryption Engine Registers
HDCP BKSV Registers	0x7800	B		HDCP BKSV Registers
HDCP AN Registers	0x7805	B		HDCP AN Registers
Encrypted DPK Embedded Storage Registers	0x780E	B		Encrypted DPK Embedded Storage Registers
CEC Engine Registers	0x7D00	B		CEC Engine Registers
I2C Master Registers	0x7E00	B		I2C Master Registers for E-DDC/SCDC

Identification Registers

Identification Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: Identification

Register		Description
design_id		Design Identification
revision_id		Revision Identification
product_id0		Product Identification
product_id1		Product Identification
config0_id		Configuration
config1_id		Configuration
config2_id		Configuration
config3_id		Configuration

design_id

Description: Design Identification Register

Size: 8 bits

Offset: 0x0

Bits	Name	Attr	Description
7:0	design_id	R	Design ID code fixed by HDMI that Identifies the instantiated DWC_hdmi_tx controller. For example, DWC_hdmi_tx 2.11a, DESIGN_ID = 21 Value After Reset: 0x21

revision_id

Description: Revision Identification Register
Size: 8 bits
Offset: 0x1

Bits	Name	Attr	Description
7:0	revision_id	R	Revision ID code fixed by HDMI that Identifies the instantiated DWC_hdmi_tx controller. Value After Reset: 0x1a

product_id0

Description: Product Identification Register 0
Size: 8 bits
Offset: 0x2

Bits	Name	Attr	Description
7:0	product_id0	R	This one byte fixed code Identifies HDMI 's product line ("A0h" for DWC_hdmi_tx products). Value After Reset: 0xa0

product_id1

Description: Product Identification Register 1
Size: 8 bits
Offset: 0x3

Bits	Name	Attr	Description
7:6	product_id1_hdcp	R	These bits identify a HDMI Controller with HDCP encryption according to HDMI product line. Value After Reset: "(HDCP== 1) ? 3 : 0"
5:2			Reserved for future use.
1	product_id1_rx	R	This bit Identifies HDMI 's DWC_hdmi_rx Controller according to HDMI product line. Value After Reset: 0x0
0	product_id1_tx	R	This bit Identifies H Controller according to HDMI product line. Value After Reset: 0x1

config0_id

Description: Configuration Identification Register 0
Size: 8 bits
Offset: 0x4

Bits	Name	Attr	Description
7	prepen	R	Indicates if it is possible to use internal pixel repetition Value After Reset: "(HDMI_TX_INTPREPEN== 1) ? 1 : 0"
6			Reserved for future use.
5	audspdif	R	Indicates if the SPDIF audio interface is present Value After Reset: "(SPDIFPORTS== 1) ? 1 : 0"
4	audi2s	R	Indicates if I2S interface is present Value After Reset: "(I2SPORTS== 1) ? 1 : 0"

Bits	Name	Attr	Description
3	hdmi14	R	Indicates if HDMI 1.4 features are present Value After Reset: "(HDMI_TX_14== 1) ? 1 : 0"
2	csc	R	Indicates if Color Space Conversion block is present Value After Reset: "(CSC== 1) ? 1 : 0"
1	cec	R	Indicates if CEC is present Value After Reset: "(CEC== 1) ? 1 : 0"
0	hdcp	R	Indicates if HDCP is present Value After Reset: "(HDCP== 1) ? 1 : 0"

config1_id

Description: Configuration Identification Register 1

Size: 8 bits

Offset: 0x5

Bits	Name	Attr	Description
7	hdcp22_snps	R	Indicates if HDCP 2.2 SNPS solution is present Value After Reset: (HTX_HDCP22_SNPS== 1) ? 1 : 0
6	hdcp22_ext	R	Indicates if external HDCP 2.2 interface support is present Value After Reset: "(HTX_HDCP22_EXTERNAL== 1) ? 1 : 0"
5	hdmi20	R	Indicates if HDMI 2.0 features are present Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
4:2			Reserved for future use.
1	confapb	R	Indicates that configuration interface is APB interface Value After Reset: 0x1
0			Reserved for future use.

config2_id

Description: Configuration Identification Register 2

Size: 8 bits

Offset: 0x6

Bits	Name	Attr	Description
7:0	phytype	R	Indicates the type of PHY interface selected: 0x00: Legacy PHY (HDMI Tx PHY) 0xF2: PHY GEN2 (HDMI 3D TX PHY) 0xE2: PHY GEN2 (HDMI 3D TX PHY) + HEAC PHY 0xC2: PHY MHL COMBO (MHL+HDMI 2.0 TX PHY) 0xB2: PHY MHL COMBO (MHL+HDMI 2.0 TX PHY) + HEAC PHY 0xF3: PHY HDMI 20 (HDMI 2.0 TX PHY) 0xE3: PHY HDMI 20 (HDMI 2.0 TX PHY) + HEAC PHY 0xFE: External PHY Value After Reset: "(PHY_HDMI20==1) ? ((HDMI_HEAC_PHY_EN==1)? 0xE3 : 0xF3) : (PHY_MHL_COMBO==1)

Bits	Name	Attr	Description
			? ((HDMI_HEAC_PHY_EN==1)? 0xB2 : 0xC2) : (PHY_GEN2==1) ? ((HDMI_HEAC_PHY_EN==1)? 0xE2 : 0xF2) : (PHY_EXTERNAL==1)? 0xFE : 0x00"

config3_id

Description: Configuration Identification Register 3

Size: 8 bits

Offset: 0x7

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	confahbauddma	R	Indicates that the audio interface is AHB AUD DMA Value After Reset: "(AHBAUDDMAIF== 1) ? 1 : 0"
0	confgpaud	R	Indicates that the audio interface is Generic Parallel Audio (GPAUD) Value After Reset: "(GPAUDPORTS== 1) ? 1 : 0"

Interrupt Registers

Interrupt Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: Interrupt

Register	Offset	Description
ih_fc_stat0	0x100	Frame Composer Interrupt Status Register 0 (Packet Interrupts)
ih_fc_stat1	0x101	Frame Composer Interrupt Status Register 1 (Packet Interrupts)
ih_fc_stat2	0x102	Frame Composer Interrupt Status Register 2 (Packet Interrupts)
ih_as_stat0	0x103	Audio Sampler Interrupt Status Register (FIFO Threshold, Underflow and Overflow Interrupts)
ih_phy_stat0	0x104	PHY Interface Interrupt Status Register (RXSENSE, PLL Lock and HPD Interrupts)
ih_i2cm_stat0	0x105	E-DDC I2C Master Interrupt Status Register (Done and Error Interrupts)
ih_cec_stat0	0x106	CEC Interrupt Status Register (Functional Operation Interrupts)
ih_vp_stat0	0x107	Video Packetizer Interrupt Status Register (FIFO Full and Empty Interrupts)
ih_i2cmphy_stat0	0x108	PHY GEN2 I2C Master Interrupt Status Register (Done and Error Interrupts)
ih_ahbdmaaud_stat0	0x109	AHB Audio DMA Interrupt Status Register (Functional Operation, Buffer Full and Empty...
ih_decode	0x170	Interruption Handler Decode Assist Register
ih_mute_fc_stat0	0x180	Frame Composer Interrupt Mute Control Register 0
ih_mute_fc_stat1	0x181	Frame Composer Interrupt Mute Control Register 1

Register	Offset	Description
ih_mute_fc_stat2	0x182	Frame Composer Interrupt Mute Control Register 2
ih_mute_as_stat0	0x183	Audio Sampler Interrupt Mute Control Register
ih_mute_phy_stat0	0x184	PHY Interface Interrupt Mute Control Register
ih_mute_i2cm_stat0	0x185	E-DDC I2C Master Interrupt Mute Control Register
ih_mute_cec_stat0	0x186	CEC Interrupt Mute Control Register
ih_mute_vp_stat0	0x187	Video Packetizer Interrupt Mute Control Register
ih_mute_i2cmphy_stat0	0x188	PHY GEN2 I2C Master Interrupt Mute Control Register
ih_mute_ahbdmaaud_stat0	0x189	AHB Audio DMA Interrupt Mute Control Register
ih_mute	0x1ff	Global Interrupt Mute Control Register

ih_fc_stat0

Description: Frame Composer Interrupt Status Register 0 (Packet Interrupts)
Size: 8 bits
Offset: 0x100

Bits	Name	Attr	Description
7	AUDI	R/W1C	Active after successful transmission of an Audio InfoFrame packet. Value After Reset: 0x0
6	ACP	R/W1C	Active after successful transmission of an Audio Content Protection packet. Value After Reset: 0x0
5	HBR	R/W1C	Active after successful transmission of an Audio HBR packet. Value After Reset: 0x0
4	MAS	R/W1C	Active after successful transmission of an MultiStream Audio packet Value After Reset: 0x0
3	NVBI	R/W1C	Active after successful transmission of an NTSC VBI packet Value After Reset: 0x0
2	AUDS	R/W1C	Active after successful transmission of an Audio Sample packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer. Value After Reset: 0x0
1	ACR	R/W1C	Active after successful transmission of an Audio Clock Regeneration (N/ CTS transmission) packet. Value After Reset: 0x0
0	NULL	R/W1C	Active after successful transmission of an Null packet. Due to high number of audio sample packets transmitted, this interrupt is by default masked at frame composer. Value After Reset: 0x0

ih_fc_stat1

Description: Frame Composer Interrupt Status Register 1 (Packet Interrupts)

Size: 8 bits

Offset: 0x101

Bits	Name	Attr	Description
7	GMD	R/W1C	Active after successful transmission of an Gamut metadata packet. Value After Reset: 0x0
6	ISCR1	R/W1C	Active after successful transmission of an International Standard Recording Code 1 packet. Value After Reset: 0x0
5	ISCR2	R/W1C	Active after successful transmission of an International Standard Recording Code 2 packet Value After Reset: 0x0
4	VSD	R/W1C	Active after successful transmission of an Vendor Specific Data InfoFrame packet. Value After Reset: 0x0
3	SPD	R/W1C	Active after successful transmission of an Source Product Descriptor InfoFrame packet. Value After Reset: 0x0
2	AMP	R/W1C	Active after successful transmission of an Audio Metadata packet Value After Reset: 0x0
1	AVI	R/W1C	Active after successful transmission of an AVI InfoFrame packet. Value After Reset: 0x0
0	GCP	R/W1C	Active after successful transmission of an General Control Packet. Value After Reset: 0x0

ih_fc_stat2

Description: Frame Composer Interrupt Status Register 2 (Packet Interrupts)

Size: 8 bits

Offset: 0x102

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W1C	Active after successful transmission of an DRM packet Value After Reset: 0x0
1	LowPriority_overflow	R/W1C	Frame Composer low priority packet queue descriptor overflow indication Value After Reset: 0x0
0	HighPriority_overflow	R/W1C	Frame Composer high priority packet queue descriptor overflow indication Value After Reset: 0x0

ih_as_stat0

Description: Audio Sampler Interrupt Status Register (FIFO Threshold, Underflow and Overflow Interrupts)

Size: 8 bits

Offset: 0x103

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_underrun	R/W1C	Indicates an underrun on the audio FIFO Value After Reset: 0x0
3	fifo_overrun	R/W1C	Indicates an overrun on the audio FIFO. Value After Reset: 0x0
2	Aud_fifo_underflow_thr	R/W1C	Audio Sampler audio FIFO empty threshold (four samples) indication for the legacy HBR audio interface. For AHB_DMA, this bit indicates that the number of samples in the FIFO is equal to (or less) than the number of active audio channels. This bit is not relevant for I2S, SPDIF, and GPA interfaces. Value After Reset: 0x0
1	Aud_fifo_underflow	R/W1C	Audio Sampler audio FIFO empty indication. Value After Reset: 0x0
0	Aud_fifo_overflow	R/W1C	Audio Sampler audio FIFO full indication. Value After Reset: 0x0

ih_phy_stat0

Description: PHY Interface Interrupt Status Register (RXSENSE, PLL Lock and HPD Interrupts)

Size: 8 bits

Offset: 0x104

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	RX_SENSE_3	R/W1C	TX PHY RX_SENSE indication for driver 3. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
4	RX_SENSE_2	R/W1C	TX PHY RX_SENSE indication for driver 2. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
3	RX_SENSE_1	R/W1C	TX PHY RX_SENSE indication for driver 1. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0
2	RX_SENSE_0	R/W1C	TX PHY RX_SENSE indication for driver 0. You may need to mask or change polarity of this interrupt

Bits	Name	Attr	Description
			after it has become active. Value After Reset: 0x0
1	TX_PHY_LOCK	R/W1C	TX PHY PLL lock indication. Value After Reset: 0x0
0	HPD	R/W1C	HDMI Hot Plug Detect indication. You may need to mask or change polarity of this interrupt after it has become active. Value After Reset: 0x0

ih_i2cm_stat0

Description: E-DDC I2C Master Interrupt Status Register (Done and Error Interrupts)

Size: 8 bits

Offset: 0x105

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	scdc_readreq	R/W1C	I2C Master SCDC read request indication. Value After Reset: 0x0
1	I2Cmasterdone	R/W1C	I2C Master done indication Value After Reset: 0x0
0	I2Cmastererror	R/W1C	I2C Master error indication Value After Reset: 0x0

ih_cec_stat0

Description: CEC Interrupt Status Register (Functional Operation Interrupts)

Size: 8 bits

Offset: 0x106

Bits	Name	Attr	Description
7			Reserved for future use.
6	WAKEUP	R/W1C	CEC Wake-up indication Value After Reset: 0x0
5	ERROR_FOLLOW	R/W1C	CEC Error Follow indication Value After Reset: 0x0
4	ERROR_INITIATOR	R/W1C	CEC Error Initiator indication Value After Reset: 0x0
3	ARB_LOST	R/W1C	CEC Arbitration Lost indication Value After Reset: 0x0
2	NACK	R/W1C	CEC Not Acknowledge indication Value After Reset: 0x0
1	EOM	R/W1C	CEC End of Message Indication Value After Reset: 0x0
0	DONE	R/W1C	CEC Done Indication Value After Reset: 0x0

ih_vp_stat0

Description: Video Packetizer Interrupt Status Register (FIFO Full and Empty Interrupts)

Size: 8 bits

Offset: 0x107

Bits	Name	Attr	Description
7	fifofullrepet	R/W1C	Video Packetizer pixel repeater FIFO full interrupt Value After Reset: 0x0
6	fifoemptyrepet	R/W1C	Video Packetizer pixel repeater FIFO empty

			interrupt Value After Reset: 0x0
5	fifofullpp	R/W1C	Video Packetizer pixel packing FIFO full interrupt Value After Reset: 0x0
4	fifoemptypp	R/W1C	Video Packetizer pixel packing FIFO empty interrupt Value After Reset: 0x0
3	fifofullremap	R/W1C	Video Packetizer pixel YCC 422 re-mapper FIFO full interrupt Value After Reset: 0x0
2	fifoemptyremap	R/W1C	Video Packetizer pixel YCC 422 re-mapper FIFO empty interrupt Value After Reset: 0x0
1:0		R/W1C	Reserved and read as zero

ih_i2cmphy_stat0

Description: PHY GEN2 I2C Master Interrupt Status Register (Done and Error Interrupts)
Size: 8 bits
Offset: 0x108

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	I2Cmphydone	R/W1C	I2C Master PHY done indication Value After Reset: 0x0
0	I2Cmphyerror	R/W1C	I2C Master PHY error indication Value After Reset: 0x0

ih_ahbdmaaud_stat0

Description: AHB Audio DMA Interrupt Status Register (Functional Operation, Buffer Full and Empty Interrupts)
Size: 8 bits
Offset: 0x109

Bits	Name	Attr	Description
7			Reserved for future use.
6	ahbdmaaud_intbuffoverrun	R/W1C	AHB audio DMA Buffer overrun interruption Value After Reset: 0x0
5	ahbdmaaud_interror	R/W1C	AHB audio DMA error interrupt Value After Reset: 0x0
4	ahbdmaaud_intlostownership	R/W1C	AHB audio DMA lost ownership interrupt Value After Reset: 0x0
3	ahbdmaaud_intretrysplit	R/W1C	AHB audio DMA RETRY/SPLIT interrupt Value After Reset: 0x0
2	ahbdmaaud_intdone	R/W1C	AHB audio DMA done interrupt Value After Reset: 0x0
1	ahbdmaaud_intbufffull	R/W1C	AHB audio DMA Buffer full interrupt Value After Reset: 0x0

Bits	Name	Attr	Description
0	ahbdmaaud_intbuffempty	R/W1C	AHB audio DMA Buffer empty interrupt Value After Reset: 0x0

ih_decode

Description: Interruption Handler Decode Assist Register

Size: 8 bits

Offset: 0x170

Bits	Name	Attr	Description
7	ih_fc_stat0	R	Interruption active at the ih_fc_stat0 register Value After Reset: 0x0
6	ih_fc_stat1	R	Interruption active at the ih_fc_stat1 register Value After Reset: 0x0
5	ih_fc_stat2_vp	R	Interruption active at the ih_fc_stat2 or ih_vp_stat0 register Value After Reset: 0x0
4	ih_as_stat0	R	Interruption active at the ih_as_stat0 register Value After Reset: 0x0
3	ih_phy	R	Interruption active at the ih_phy_stat0 or ih_i2cmphy_stat0 register Value After Reset: 0x0
2	ih_i2cm_stat0	R	Interruption active at the ih_i2cm_stat0 register Value After Reset: 0x0
1	ih_cec_stat0	R	Interruption active at the ih_cec_stat0 register Value After Reset: 0x0
0	ih_ahbdmaaud_stat0	R	Interruption active at the ih_ahbdmaaud_stat0 register Value After Reset: 0x0

ih_mute_fc_stat0

Description: Frame Composer Interrupt Mute Control Register 0

Size: 8 bits

Offset: 0x180

Bits	Name	Attr	Description
7	AUDI	R/W	When set to 1, mutes ih_fc_stat0[7] Value After Reset: 0x0
6	ACP	R/W	When set to 1, mutes ih_fc_stat0[6] Value After Reset: 0x0
5	HBR	R/W	When set to 1, mutes ih_fc_stat0[5] Value After Reset: 0x0
4	MAS	R/W	When set to 1, mutes ih_fc_stat0[4]. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
3	NVBI	R/W	When set to 1, mutes ih_fc_stat0[3]. Otherwise, this field is a "spare" bit with no associated

Bits	Name	Attr	Description
			functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
2	AUDS	R/W	When set to 1, mutes ih_fc_stat0[2] Value After Reset: 0x0
1	ACR	R/W	When set to 1, mutes ih_fc_stat0[1] Value After Reset: 0x0
0	NULL	R/W	When set to 1, mutes ih_fc_stat0[0] Value After Reset: 0x0

ih_mute_fc_stat1

Description: Frame Composer Interrupt Mute Control Register 1

Size: 8 bits

Offset: 0x181

Bits	Name	Attr	Description
7	GMD	R/W	When set to 1, mutes ih_fc_stat1[7] Value After Reset: 0x0
6	ISCR1	R/W	When set to 1, mutes ih_fc_stat1[6] Value After Reset: 0x0
5	ISCR2	R/W	When set to 1, mutes ih_fc_stat1[5] Value After Reset: 0x0
4	VSD	R/W	When set to 1, mutes ih_fc_stat1[4] Value After Reset: 0x0
3	SPD	R/W	When set to 1, mutes ih_fc_stat1[3] Value After Reset: 0x0
2	AMP	R/W	When set to 1, mutes ih_fc_stat1[2]. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0" Exists: HDMI_TX_20==1
1	AVI	R/W	When set to 1, mutes ih_fc_stat1[1] Value After Reset: 0x0
0	GCP	R/W	When set to 1, mutes ih_fc_stat1[0] Value After Reset: 0x0

ih_mute_fc_stat2

Description: Frame Composer Interrupt Mute Control Register 2

Size: 8 bits

Offset: 0x182

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W	When set to 1, mutes ih_fc_stat2[4]. Value After Reset: (HDMI_TX_20== 1) ? 1 : 0
3:2			Reserved for future use
1	LowPriority_overflow	R/W	When set to 1, mutes ih_fc_stat2[1] Value After Reset: 0x0

0	HighPriority_overflow	R/W	When set to 1, mutes ih_fc_stat2[0] Value After Reset: 0x0

ih_mute_as_stat0

Description: Audio Sampler Interrupt Mute Control Register

Size: 8 bits

Offset: 0x183

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_underrun	R/W	When set to 1, mutes ih_as_stat0[4] Value After Reset: 0x1
3	fifo_overrun	R/W	When set to 1, mutes ih_as_stat0[3] Value After Reset: 0x1
2	Aud_fifo_underflow_thr	R/W	When set to 1, mutes ih_as_stat0[2] Value After Reset: 0x0
1	Aud_fifo_underflow	R/W	When set to 1, mutes ih_as_stat0[1] Value After Reset: 0x0
0	Aud_fifo_overflow	R/W	When set to 1, mutes ih_as_stat0[0] Value After Reset: 0x0

ih_mute_phy_stat0

Description: PHY Interface Interrupt Mute Control Register

Size: 8 bits

Offset: 0x184

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	RX_SENSE_3	R/W	When set to 1, mutes ih_phy_stat0[5] Value After Reset: 0x0
4	RX_SENSE_2	R/W	When set to 1, mutes ih_phy_stat0[4] Value After Reset: 0x0
3	RX_SENSE_1	R/W	When set to 1, mutes ih_phy_stat0[3] Value After Reset: 0x0
2	RX_SENSE_0	R/W	When set to 1, mutes ih_phy_stat0[2] Value After Reset: 0x0
1	TX_PHY_LOCK	R/W	When set to 1, mutes ih_phy_stat0[1] Value After Reset: 0x0
0	HPD	R/W	When set to 1, mutes ih_phy_stat0[0] Value After Reset: 0x0

ih_mute_i2cm_stat0

Description: E-DDC I2C Master Interrupt Mute Control Register

Size: 8 bits

Offset: 0x185

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	scdc_readreq	R/W	When set to 1, mutes ih_i2cm_stat0[2]

			Value After Reset: 0x1
1	I2Cmasterdone	R/W	When set to 1, mutes ih_i2cm_stat0[1] Value After Reset: 0x0
0	I2Cmastererror	R/W	When set to 1, mutes ih_i2cm_stat0[0] Value After Reset: 0x0

ih_mute_cec_stat0

Description: CEC Interrupt Mute Control Register

Size: 8 bits

Offset: 0x186

Bits	Name	Attr	Description
7			Reserved for future use.
6	WAKEUP	R/W	When set to 1, mutes ih_cec_stat0[6] Value After Reset: 0x0
5	ERROR_FOLLOW	R/W	When set to 1, mutes ih_cec_stat0[5] Value After Reset: 0x0
4	ERROR_INITIATOR	R/W	When set to 1, mutes ih_cec_stat0[4] Value After Reset: 0x0
3	ARB_LOST	R/W	When set to 1, mutes ih_cec_stat0[3] Value After Reset: 0x0
2	NACK	R/W	When set to 1, mutes ih_cec_stat0[2] Value After Reset: 0x0
1	EOM	R/W	When set to 1, mutes ih_cec_stat0[1] Value After Reset: 0x0
0	DONE	R/W	When set to 1, mutes ih_cec_stat0[0] Value After Reset: 0x0

ih_mute_vp_stat0

Description: Video Packetizer Interrupt Mute Control Register

Size: 8 bits

Offset: 0x187

Bits	Name	Attr	Description
7	fifofullrepet	R/W	When set to 1, mutes ih_vp_stat0[7] Value After Reset: 0x0
6	fifoemptyrepet	R/W	When set to 1, mutes ih_vp_stat0[6] Value After Reset: 0x0
5	fifofullpp	R/W	When set to 1, mutes ih_vp_stat0[5] Value After Reset: 0x0
4	fifoemptypp	R/W	When set to 1, mutes ih_vp_stat0[4] Value After Reset: 0x0
3	fifofullremap	R/W	When set to 1, mutes ih_vp_stat0[3] Value After Reset: 0x0
2	fifoemptyremap	R/W	When set to 1, mutes ih_vp_stat0[2] Value After Reset: 0x0
1	spare_2	R/W	Reserved as “spare” bit with no associated functionality.

Bits	Name	Attr	Description
			Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

ih_mute_i2cmphy_stat0

Description: PHY GEN2 I2C Master Interrupt Mute Control Register

Size: 8 bits

Offset: 0x188

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	I2Cmphydone	R/W	When set to 1, mutes ih_i2cmphy_stat0[1] Value After Reset: 0x0
0	I2Cmphyerror	R/W	When set to 1, mutes ih_i2cmphy_stat0[0] Value After Reset: 0x0

ih_mute_ahbdmaaud_stat0

Description: AHB Audio DMA Interrupt Mute Control Register

Size: 8 bits

Offset: 0x189

Bits	Name	Attr	Description
7			Reserved for future use.
6	ahbdmaaud_intbuffoverrun	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[6] Value After Reset: 0x1
5	ahbdmaaud_interror	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[5] Value After Reset: 0x0
4	ahbdmaaud_intlostownership	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[4] Value After Reset: 0x0
3	ahbdmaaud_intretrysplit	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[3] Value After Reset: 0x0
2	ahbdmaaud_intdone	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[2] Value After Reset: 0x0
1	ahbdmaaud_intbufffull	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[1] Value After Reset: 0x0
0	ahbdmaaud_intbuffempty	R/W	When set to 1, mutes ih_ahbdmaaud_stat0[0] Value After Reset: 0x0

ih_mute

Description: Global Interrupt Mute Control Register

Size: 8 bits

Offset: 0x1ff

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	mute_wakeup_interrupt	R/W	When set to 1, mutes the main interrupt output port. The sticky bit interrupts continue with their state accessible through the configuration bus,

			only the main interrupt line is muted. Value After Reset: 0x1
0	mute_all_interrupt	R/W	When set to 1, mutes the main interrupt line (where all interrupts are ORed). The sticky bit interrupts continue with their state; only the main interrupt line is muted. Value After Reset: 0x1

VideoSampler Registers

Video Sampler Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: VideoSampler

Register	Offset	Description
tx_invid0	0x200	Video Input Mapping and Internal Data Enable Configuration Register
tx_instuffing	0x201	Video Input Stuffing Enable Register
tx_gydata0	0x202	Video Input gy Data Channel Stuffing Register 0
tx_gydata1	0x203	Video Input gy Data Channel Stuffing Register 1
tx_rcrdata0	0x204	Video Input rcr Data Channel Stuffing Register 0
tx_rcrdata1	0x205	Video Input rcr Data Channel Stuffing Register 1
tx_bcbdata0	0x206	Video Input bcb Data Channel Stuffing Register 0
tx_bcbdata1	0x207	Video Input bcb Data Channel Stuffing Register 1

tx_invid0

Description: Video Input Mapping and Internal Data Enable Configuration Register

Size: 8 bits

Offset: 0x200

Bits	Name	Attr	Description
7	internal_de_generator	R/W	Internal data enable (DE) generator enable. If data enable is not available for the input video, set this bit to one to activate the internal data enable generator. Attention: This feature only works for input video modes that have native repetition (such as, all CEA videos). No desired pixel repetition can be used with this feature because these configurations only affect the Frame Composer and not this block. The DE Generator does not work for the following conditions: Transmission of video with CEA VIC 39 Transmission of 3D video using the field alternative structure Value After Reset: 0x0
6:5			Reserved for future use.
4:0	video_mapping	R/W	Video Input mapping (color space/color depth): 0x01: RGB 4:4:4/8 bits

Bits	Name	Attr	Description
			0x03: RGB 4:4:4/10 bits 0x05: RGB 4:4:4/12 bits 0x07: RGB 4:4:4/16 bits 0x09: YCbCr 4:4:4 or 4:2:0/8 bits 0x0B: YCbCr 4:4:4 or 4:2:0/10 bits 0x0D: YCbCr 4:4:4 or 4:2:0/12 bits 0x0F: YCbCr 4:4:4 or 4:2:0/16 bits 0x16: YCbCr 4:2:2/8 bits 0x14: YCbCr 4:2:2/10 bits 0x12: YCbCr 4:2:2/12 bits 0x17: YCbCr 4:4:4 (IPI)/8 bits 0x18: YCbCr 4:4:4 (IPI)/10 bits 0x19: YCbCr 4:4:4 (IPI)/12 bits 0x1A: YCbCr 4:4:4 (IPI)/16 bits 0x1B: YCbCr 4:2:2 (IPI)/12 bits 0x1C: YCbCr 4:2:0 (IPI)/8 bits 0x1D: YCbCr 4:2:0 (IPI)/10 bits 0x1E: YCbCr 4:2:0 (IPI)/12 bits 0x1F: YCbCr 4:2:0 (IPI)/16 bits Value After Reset: 0x1

tx_instuffing

Description: Video Input Stuffing Enable Register

Size: 8 bits

Offset: 0x201

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	bcbdata_stuffing	R/W	0b: When the dataen signal is low, the value in the bcbdata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the bcbdata[15:0] output is given by the values in the TX_BCBDTA0 and TX_BCBDATA1 registers. Value After Reset: 0x0
1	rcrdata_stuffing	R/W	0b: When the dataen signal is low, the value in the rcrdata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the rcrdata[15:0] output is given by the values in TX_RCRDTA0 and TX_RCRDATA1 registers. Value After Reset: 0x0
0	gydata_stuffing	R/W	0b: When the dataen signal is low, the value in the gydata[15:0] output is the one sampled from the corresponding input data. 1b: When the dataen signal is low, the value in the gydata[15:0] output is given by the values in TX_GYDTA0 and TX_GYDATA1 registers.

Bits	Name	Attr	Description
			Value After Reset: 0x0

tx_gydata0

Description: Video Input gy Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x202

Bits	Name	Attr	Description
7:0	gydata	R/W	This register defines the value of gydata[7:0] when TX_INSTUFFING[0] (gydata_stuffing) is set to 1b. Value After Reset: 0x0

tx_gydata1

Description: Video Input gy Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x203

Bits	Name	Attr	Description
7:0	gydata	R/W	This register defines the value of gydata[15:8] when TX_INSTUFFING[0] (gydata_stuffing) is set to 1b. Value After Reset: 0x0

tx_rcrdata0

Description: Video Input rcr Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x204

Bits	Name	Attr	Description
7:0	rcrdata	R/W	This register defines the value of rcrydata[7:0] when TX_INSTUFFING[1] (rcrdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_rcrdata1

Description: Video Input rcr Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x205

Bits	Name	Attr	Description
7:0	rcrdata	R/W	This register defines the value of rcrydata[15:8] when TX_INSTUFFING[1] (rcrdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_bcbdata0

Description: Video Input bcb Data Channel Stuffing Register 0

Size: 8 bits

Offset: 0x206

Bits	Name	Attr	Description

7:0	bcbdata	R/W	This register defines the value of bcbdata[7:0] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b. Value After Reset: 0x0

tx_bcbdata1

Description: Video Input bcb Data Channel Stuffing Register 1

Size: 8 bits

Offset: 0x207

Bits	Name	Attr	Description
7:0	bcbdata	R/W	This register defines the value of bcbdata[15:8] when TX_INSTUFFING[2] (bcbdata_stuffing) is set to 1b. Value After Reset: 0x0

VideoPacketizer Registers

Video Packetizer Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
vp_status	0x800	Video Packetizer Packing Phase Status Register
vp_pr_cd	0x801	Video Packetizer Pixel Repetition and Color Depth Register
vp_stuff	0x802	Video Packetizer Stuffing and Default Packing Phase Register
vp_remap	0x803	Video Packetizer YCC422 Remapping Register
vp_conf	0x804	Video Packetizer Output and Enable Configuration Register
vp_mask	0x807	Video Packetizer Interrupt Mask Register

vp_status

Description: Video Packetizer Packing Phase Status Register

Size: 8 bits

Offset: 0x800

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	packing_phase	R	Read only register that holds the "packing phase" output of the Video Packetizer block. Value After Reset: 0x0

vp_pr_cd

Description: Video Packetizer Pixel Repetition and Color Depth Register

Size: 8 bits

Offset: 0x801

Bits	Name	Attr	Description
7:4	color_depth	R/W	The Color depth configuration is described as the following, with the action stated corresponding to color_depth[3:0]: 0000b: 24 bits per pixel video (8 bits per component). 8-bit packing mode. 0001b-0011b: Reserved. Not used. 0100b: 24 bits per pixel video (8 bits per

Bits	Name	Attr	Description
			component). 8-bit packing mode. 0101b: 30 bits per pixel video (10 bits per component). 10-bit packing mode. 0110b: 36 bits per pixel video (12 bits per component). 12-bit packing mode. 0111b: 48 bits per pixel video (16 bits per component). 16-bit packing mode. Other: Reserved. Not used. Value After Reset: 0x0
3:0	desired_pr_factor	R/W	Desired pixel repetition factor configuration. The configured value sets H13T PHY PLL to multiply pixel clock by the factor in order to obtain the desired repetition clock. For the CEA modes some are already defined with pixel repetition in the input video. So for CEA modes this shall be always 0. Shall only be used if the user wants to do pixel repetition using H13TCTRL controller. The action is stated corresponding to desired_pr_factor[3:0]: 0000b: No pixel repetition (pixel sent only once) 0001b: Pixel sent two times (pixel repeated once) 0010b: Pixel sent three times 0011b: Pixel sent four times 0100b: Pixel sent five times 0101b: Pixel sent six times 0110b: Pixel sent seven times 0111b: Pixel sent eight times 1000b: Pixel sent nine times 1001b: Pixel sent 10 times Other: Reserved. Not used Value After Reset: 0x0

vp_stuff

Description: Video Packetizer Stuffing and Default Packing Phase Register

Size: 8 bits

Offset: 0x802

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	idefault_phase	R/W	Controls the default phase packing machine used according to HDMI 1.4b specification: "If the transmitted video format has timing such that the phase of the first pixel of every Video Data Period corresponds to pixel packing phase 0 (e.g. 10P0, 12P0, 16P0), the Source may set the Default_Phase bit in the GCP. The Sink may use this bit to optimize its filtering or handling of the PP field."

Bits	Name	Attr	Description
			This means that for 10-bit mode the Htotal must be dividable by 4; for 12- bit mode, the Htotal must be divisible by 2. Value After Reset: 0x0
4	ifix_pp_to_last	R/W	Reserved. Controls packing machine strategy Value After Reset: 0x0
3	icx_goto_p0_st	R/W	Reserved. Controls packing machine strategy Value After Reset: 0x0
2	ycc422_stuffing	R/W	YCC 422 remap stuffing control. For horizontal blanking, the action is stated corresponding to ycc422_stuffing: 0b: YCC 422 remap block in direct mode (input blanking data goes directly to output). 1b: YCC 422 remap block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0
1	pp_stuffing	R/W	Pixel packing stuffing control. The action is stated corresponding to pp_stuffing: 0b: Pixel packing block in direct mode (input blanking data goes directly to output). 1b: Pixel packing block in stuffing mode. When "de_rep" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0

Fields for Register: vp_stuff (Continued)

Bits	Name	Attr	Description
0	pr_stuffing	R/W	Pixel repeater stuffing control. The action is stated corresponding to pp_stuffing: 0b: Pixel repeater block in direct mode (input blanking data goes directly to output). 1b: Pixel repeater block in stuffing mode. When "de" goes to low the outputs are fixed to 0x00. Value After Reset: 0x0

vp_remap

Description: Video Packetizer YCC422 Remapping Register

Size: 8 bits

Offset: 0x803

Bits	Name	Attr	Description
7:2			Reserved for future use.
1:0	ycc422_size	R/W	YCC 422 remap input video size ycc422_size[1:0] 00b: YCC 422 16-bit input video (8 bits per component) 01b: YCC 422 20-bit input video (10 bits per component) 10b: YCC 422 24-bit input

			video (12 bits per component) 11b: Reserved. Not used Value After Reset: 0x0

vp_conf

Description: Video Packetizer Output and Enable Configuration Register

Size: 8 bits

Offset: 0x804

Bits	Name	Attr	Description
7			Reserved for future use.
6	bypass_en	R/W	When set to 1'b1, Pixel packing enable. When set to 1b'0, the pixel packing block is controlled by pp_en. Value After Reset: 0x0
5	pp_en	R/W	Pixel packing enable. When set to 0, the pixel packing block is disabled if bypass_en is 1’b0. Value After Reset: 0x1
4	pr_en	R/W	Pixel repeater enable. When set to 0, the pixel repetition block is disabled. Value After Reset: 0x0
3	ycc422_en	R/W	YCC 422 select enable. Disabling forces bypass module to output always zeros. Value After Reset: 0x0
2	bypass_select	R/W	bypass_select 0b: Data from pixel repeater block 1b: Data from input of Video Packetizer block Value After Reset: 0x1
1	output_selector	R/W	When set to 1'b1, Data from pixel packing block. Value After Reset: 0x0
0	output_selector_0	R/W	Video Packetizer output selection 0b: Data from pixel packing block 1b: Data from YCC422 remap block Value After Reset: 0x0

vp_mask

Description: Video Packetizer Interrupt Mask Register

Size: 8 bits

Offset: 0x807

Bits	Name	Attr	Description
7	ointfullrepet	R/W	Mask bit for Video Packetizer pixel repeater FIFO full Value After Reset: 0x0
6	ointemptyrepet	R/W	Mask bit for Video Packetizer pixel repeater FIFO empty Value After Reset: 0x0
5	ointfullpp	R/W	Mask bit for Video Packetizer pixel packing FIFO full

			Value After Reset: 0x0
4	ointemptypp	R/W	Mask bit for Video Packetizer pixel packing FIFO empty Value After Reset: 0x0
3	ointfullremap	R/W	Mask bit for Video Packetizer pixel YCC 422 re-mapper FIFO full Value After Reset: 0x0
2	ointemptyremap	R/W	Mask bit for Video Packetizer pixel YCC 422 re-mapper FIFO empty Value After Reset: 0x0
1	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

FrameComposer Registers

Frame Composer Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: FrameComposer

Register	**Offset**	**Description**
fc_invidconf	0x1000	Frame Composer Input Video Configuration and HDCP Keepout Register
fc_inhactiv0	0x1001	Frame Composer Input Video HActive Pixels Register 0
fc_inhactiv1	0x1002	Frame Composer Input Video HActive Pixels Register 1
fc_inhblank0	0x1003	Frame Composer Input Video HBlank Pixels Register 0
fc_inhblank1	0x1004	Frame Composer Input Video HBlank Pixels Register 1
fc_invactiv0	0x1005	Frame Composer Input Video VActive Pixels Register 0
fc_invactiv1	0x1006	Frame Composer Input Video VActive Pixels Register 1
fc_invblank	0x1007	Frame Composer Input Video VBlank Pixels Register
fc_hsyncindelay0	0x1008	Frame Composer Input Video HSync Front Porch Register 0
fc_hsyncindelay1	0x1009	Frame Composer Input Video HSync Front Porch Register 1
fc_hsyncinwidth0	0x100a	Frame Composer Input Video HSync Width Register 0
fc_hsyncinwidth1	0x100b	Frame Composer Input Video HSync Width Register 1
fc_vsyncindelay	0x100c	Frame Composer Input Video VSync Front Porch Register
fc_vsyncinwidth	0x100d	Frame Composer Input Video VSync Width Register
fc_infreq0	0x100e	Frame Composer Input Video Refresh Rate Register 0
fc_infreq1	0x100f	Frame Composer Input Video Refresh Rate Register 1

Register	Offset	Description
fc_infreq2	0x1010	Frame Composer Input Video Refresh Rate Register 2
fc_ctrldur	0x1011	Frame Composer Control Period Duration Register
fc_exctrldur	0x1012	Frame Composer Extended Control Period Duration Register
fc_exctrlspac	0x1013	Frame Composer Extended Control Period Maximum Spacing Register
fc_ch0pream	0x1014	Frame Composer Channel 0 Non-Preamble Data Register
fc_ch1pream	0x1015	Frame Composer Channel 1 Non-Preamble Data Register
fc_ch2pream	0x1016	Frame Composer Channel 2 Non-Preamble Data Register
fc_aviconf3	0x1017	Frame Composer AVI Packet Configuration Register 3
fc_gcp	0x1018	Frame Composer GCP Packet Configuration Register
fc_aviconf0	0x1019	Frame Composer AVI Packet Configuration Register 0
fc_aviconf1	0x101a	Frame Composer AVI Packet Configuration Register 1

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_aviconf2	0x101b	Frame Composer AVI Packet Configuration Register 2
fc_avivid	0x101c	Frame Composer AVI Packet VIC Register
fc_avietb[0:1]	0x101d + (i * 0x1)	Frame Composer AVI Packet End of Top Bar Register Array
fc_avisbb[0:1]	0x101f + (i * 0x1)	Frame Composer AVI Packet Start of Bottom Bar Register Array
fc_avielb[0:1]	0x1021 + (i * 0x1)	Frame Composer AVI Packet End of Left Bar Register Array
fc_avisrb[0:1]	0x1023 + (i * 0x1)	Frame Composer AVI Packet Start of Right Bar Register Array
fc_audiconf0	0x1025	Frame Composer AUD Packet Configuration Register 0
fc_audiconf1	0x1026	Frame Composer AUD Packet Configuration Register 1
fc_audiconf2	0x1027	Frame Composer AUD Packet Configuration Register 2
fc_audiconf3	0x1028	Frame Composer AUD Packet Configuration Register 3
fc_vsdieeeid2	0x1029	Frame Composer VSI Packet Data IEEE Register 2
fc_vsdsize	0x102a	Frame Composer VSI Packet Data Size Register
fc_vsdieeeid1	0x1030	Frame Composer VSI Packet Data IEEE Register 1
fc_vsdieeeid0	0x1031	Frame Composer VSI Packet Data IEEE Register 0
fc_vsdpayload[0:23]	0x1032 + (i * 0x1)	Frame Composer VSI Packet Data Payload Register Array
fc_spdvendorname[0:7]	0x104a + (i * 0x1)	Frame Composer SPD Packet Data Vendor Name Register Array
fc_spdproductname[0:15]	0x1052 +	Frame Composer SPD packet Data Product Name

Register	Offset	Description
	(i * 0x1)	Register Array
fc_spddeviceinf	0x1062	Frame Composer SPD Packet Data Source Product Descriptor Register
fc_audsconf	0x1063	Frame Composer Audio Sample Flat and Layout Configuration Register
fc_audsstat	0x1064	Frame Composer Audio Sample Flat and Layout Status Register
fc_audsv	0x1065	Frame Composer Audio Sample Validity Flag Register
fc_audsu	0x1066	Frame Composer Audio Sample User Flag Register
fc_audschnl0	0x1067	Frame Composer Audio Sample Channel Status Configuration Register 0
fc_audschnl1	0x1068	Frame Composer Audio Sample Channel Status Configuration Register 1

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_audschnl2	0x1069	Frame Composer Audio Sample Channel Status Configuration Register 2
fc_audschnl3	0x106a	Frame Composer Audio Sample Channel Status Configuration Register 3
fc_audschnl4	0x106b	Frame Composer Audio Sample Channel Status Configuration Register 4
fc_audschnl5	0x106c	Frame Composer Audio Sample Channel Status Configuration Register 5
fc_audschnl6	0x106d	Frame Composer Audio Sample Channel Status Configuration Register 6
fc_audschnl7	0x106e	Frame Composer Audio Sample Channel Status Configuration Register 7
fc_audschnl8	0x106f	Frame Composer Audio Sample Channel Status Configuration Register 8
fc_ctrlqhigh	0x1073	Frame Composer Number of High Priority Packets Attended Configuration Register
fc_ctrlqlow	0x1074	Frame Composer Number of Low Priority Packets Attended Configuration Register
fc_acp0	0x1075	Frame Composer ACP Packet Type Configuration Register 0
fc_acp16	0x1082	Frame Composer ACP Packet Body Configuration Register 16
fc_acp15	0x1083	Frame Composer ACP Packet Body Configuration Register 15
fc_acp14	0x1084	Frame Composer ACP Packet Body Configuration Register 14
fc_acp13	0x1085	Frame Composer ACP Packet Body Configuration Register 13
fc_acp12	0x1086	Frame Composer ACP Packet Body Configuration Register 12

Register	Offset	Description
fc_acp11	0x1087	Frame Composer ACP Packet Body Configuration Register 11
fc_acp10	0x1088	Frame Composer ACP Packet Body Configuration Register 10
fc_acp9	0x1089	Frame Composer ACP Packet Body Configuration Register 9
fc_acp8	0x108a	Frame Composer ACP Packet Body Configuration Register 8
fc_acp7	0x108b	Frame Composer ACP Packet Body Configuration Register 7
fc_acp6	0x108c	Frame Composer ACP Packet Body Configuration Register 6

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_acp5	0x108d	Frame Composer ACP Packet Body Configuration Register 5
fc_acp4	0x108e	Frame Composer ACP Packet Body Configuration Register 4
fc_acp3	0x108f	Frame Composer ACP Packet Body Configuration Register 3
fc_acp2	0x1090	Frame Composer ACP Packet Body Configuration Register 2
fc_acp1	0x1091	Frame Composer ACP Packet Body Configuration Register 1
fc_iscr1_0	0x1092	Frame Composer ISRC1 Packet Status, Valid, and Continue Configuration Register
fc_iscr1_16	0x1093	Frame Composer ISRC1 Packet Body Register 16
fc_iscr1_15	0x1094	Frame Composer ISRC1 Packet Body Register 15
fc_iscr1_14	0x1095	Frame Composer ISRC1 Packet Body Register 14
fc_iscr1_13	0x1096	Frame Composer ISRC1 Packet Body Register 13
fc_iscr1_12	0x1097	Frame Composer ISRC1 Packet Body Register 12
fc_iscr1_11	0x1098	Frame Composer ISRC1 Packet Body Register 11
fc_iscr1_10	0x1099	Frame Composer ISRC1 Packet Body Register 10
fc_iscr1_9	0x109a	Frame Composer ISRC1 Packet Body Register 9
fc_iscr1_8	0x109b	Frame Composer ISRC1 Packet Body Register 8
fc_iscr1_7	0x109c	Frame Composer ISRC1 Packet Body Register 7
fc_iscr1_6	0x109d	Frame Composer ISRC1 Packet Body Register 6
fc_iscr1_5	0x109e	Frame Composer ISRC1 Packet Body Register 5
fc_iscr1_4	0x109f	Frame Composer ISRC1 Packet Body Register 4
fc_iscr1_3	0x10a0	Frame Composer ISRC1 Packet Body Register 3
fc_iscr1_2	0x10a1	Frame Composer ISRC1 Packet Body Register 2
fc_iscr1_1	0x10a2	Frame Composer ISRC1 Packet Body Register 1
fc_iscr2_15	0x10a3	Frame Composer ISRC2 Packet Body Register 15
fc_iscr2_14	0x10a4	Frame Composer ISRC2 Packet Body Register 14

Register	Offset	Description
fc_iscr2_13	0x10a5	Frame Composer ISRC2 Packet Body Register 13
fc_iscr2_12	0x10a6	Frame Composer ISRC2 Packet Body Register 12
fc_iscr2_11	0x10a7	Frame Composer ISRC2 Packet Body Register 11
fc_iscr2_10	0x10a8	Frame Composer ISRC2 Packet Body Register 10
fc_iscr2_9	0x10a9	Frame Composer ISRC2 Packet Body Register 9
fc_iscr2_8	0x10aa	Frame Composer ISRC2 Packet Body Register 8
fc_iscr2_7	0x10ab	Frame Composer ISRC2 Packet Body Register 7

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_iscr2_6	0x10ac	Frame Composer ISRC2 Packet Body Register 6
fc_iscr2_5	0x10ad	Frame Composer ISRC2 Packet Body Register 5
fc_iscr2_4	0x10ae	Frame Composer ISRC2 Packet Body Register 4
fc_iscr2_3	0x10af	Frame Composer ISRC2 Packet Body Register 3
fc_iscr2_2	0x10b0	Frame Composer ISRC2 Packet Body Register 2
fc_iscr2_1	0x10b1	Frame Composer ISRC2 Packet Body Register 1
fc_iscr2_0	0x10b2	Frame Composer ISRC2 Packet Body Register 0
fc_datauto0	0x10b3	Frame Composer Data Island Auto Packet Scheduling Register 0 Configures the Frame Composer RDRB(1)/ Manual(0)...
fc_datauto1	0x10b4	Frame Composer Data Island Auto Packet Scheduling Register 1 Configures the Frame Composer (FC)...
fc_datauto2	0x10b5	Frame Composer Data Island Auto packet scheduling Register 2 Configures the Frame Composer (FC)...
fc_datman	0x10b6	Frame Composer Data Island Manual Packet Request Register Requests to the Frame Composer the data...
fc_datauto3	0x10b7	Frame Composer Data Island Auto Packet Scheduling Register 3 Configures the Frame Composer Automatic(1)/ RDRB(0)...
fc_rdrb0	0x10b8	Frame Composer Round Robin ACR Packet Insertion Register 0 Configures the Frame Composer (FC) RDRB...
fc_rdrb1	0x10b9	Frame Composer Round Robin ACR Packet Insertion Register 1 Configures the Frame Composer (FC) RDRB...
fc_rdrb2	0x10ba	Frame Composer Round Robin AUDI Packet Insertion Register 2 Configures the Frame Composer (FC)...
fc_rdrb3	0x10bb	Frame Composer Round Robin AUDI Packet Insertion Register 3 Configures the Frame Composer (FC)...
fc_rdrb4	0x10bc	Frame Composer Round Robin GCP Packet Insertion Register 4 Configures the Frame Composer (FC) RDRB...
fc_rdrb5	0x10bd	Frame Composer Round Robin GCP Packet Insertion Register 5 Configures the Frame Composer (FC) RDRB...

Register	Offset	Description
fc_rdrb6	0x10be	Frame Composer Round Robin AVI Packet Insertion Register 6 Configures the Frame Composer (FC) RDRB...
fc_rdrb7	0x10bf	Frame Composer Round Robin AVI Packet Insertion Register 7 Configures the Frame Composer (FC) RDRB...
fc_rdrb8	0x10c0	Frame Composer Round Robin AMP Packet Insertion Register 8

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_rdrb9	0x10c1	Frame Composer Round Robin AMP Packet Insertion Register 9
fc_rdrb10	0x10c2	Frame Composer Round Robin NTSC VBI Packet Insertion Register 10
fc_rdrb11	0x10c3	Frame Composer Round Robin NTSC VBI Packet Insertion Register 11
fc_rdrb12	0x10c4	Frame Composer Round Robin DRM Packet Insertion Register 12
fc_rdrb13	0x10c5	Frame Composer Round Robin DRM Packet Insertion Register 13
fc_mask0	0x10d2	Frame Composer Packet Interrupt Mask Register 0
fc_mask1	0x10d6	Frame Composer Packet Interrupt Mask Register 1
fc_mask2	0x10da	Frame Composer High/Low Priority Overflow Interrupt Mask Register 2
fc_prconf	0x10e0	Frame Composer Pixel Repetition Configuration Register
fc_scrambler_ctrl	0x10e1	Frame Composer Scrambler Control
fc_multistream_ctrl	0x10e2	Frame Composer Multi-Stream Audio Control
fc_packet_tx_en	0x10e3	Frame Composer Packet Transmission Control
fc_actspc_hdlr_cfg	0x10e8	Frame Composer Active Space Control
fc_invact_2d_0	0x10e9	Frame Composer Input Video 2D VActive Pixels Register 0
fc_invact_2d_1	0x10ea	Frame Composer Input Video VActive pixels Register 1
fc_gmd_stat	0x1100	Frame Composer GMD Packet Status Register Gamut metadata packet status bit information for no_current_gmd,...
fc_gmd_en	0x1101	Frame Composer GMD Packet Enable Register This register enables Gamut metadata (GMD) packet transmission....
fc_gmd_up	0x1102	Frame Composer GMD Packet Update Register This register performs an GMD packet content update according...
fc_gmd_conf	0x1103	Frame Composer GMD Packet Schedule

Register	Offset	Description
		Configuration Register This register configures the number of...
fc_gmd_hb	0x1104	Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register This register configures...
fc_gmd_pb[0:27]	0x1105 + (i * 0x1)	Frame Composer GMD Packet Body Register Array Configures the GMD packet body of the GMD...
fc_amp_hb1	0x1128	Frame Composer AMP Packet Header Register 1
fc_amp_hb2	0x1129	Frame Composer AMP Packet Header Register 2

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_amp_pb[0:27]	0x112a + (i * 0x1)	Frame Composer AMP Packet Body Register Array
fc_nvbi_hb1	0x1148	Frame Composer NTSC VBI Packet Header Register 1
fc_nvbi_hb2	0x1149	Frame Composer NTSC VBI Packet Header Register 2
fc_nvbi_pb[0:26]	0x114a + (i * 0x1)	Frame Composer NTSC VBI Packet Body Register Array
fc_drm_up	0x1167	Frame Composer DRM Packet Update Register
fc_drm_hb[0:1]	0x1168 + (i * 0x1)	Frame Composer DRM Packet Header Register Array
fc_drm_pb[0:26]	0x116a + (i * 0x1)	Frame Composer DRM Packet Body Register Array
fc_dbgforce	0x1200	Frame Composer video/audio Force Enable Register This register allows to force the controller to...
fc_dbgaud0ch0	0x1201	Frame Composer Audio Data Channel 0 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch0	0x1202	Frame Composer Audio Data Channel 0 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch0	0x1203	Frame Composer Audio Data Channel 0 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch1	0x1204	Frame Composer Audio Data Channel 1 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch1	0x1205	Frame Composer Audio Data Channel 1 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch1	0x1206	Frame Composer Audio Data Channel 1 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch2	0x1207	Frame Composer Audio Data Channel 2 Register 0

Register	Offset	Description
		Configures the audio fixed data to be used in channel...
fc_dbgaud1ch2	0x1208	Frame Composer Audio Data Channel 2 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch2	0x1209	Frame Composer Audio Data Channel 2 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch3	0x120a	Frame Composer Audio Data Channel 3 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch3	0x120b	Frame Composer Audio Data Channel 3 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch3	0x120c	Frame Composer Audio Data Channel 3 Register 2 Configures the audio fixed data to be used in channel...

Registers for Address Block: FrameComposer (Continued)

Register	Offset	Description
fc_dbgaud0ch4	0x120d	Frame Composer Audio Data Channel 4 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch4	0x120e	Frame Composer Audio Data Channel 4 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch4	0x120f	Frame Composer Audio Data Channel 4 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch5	0x1210	Frame Composer Audio Data Channel 5 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch5	0x1211	Frame Composer Audio Data Channel 5 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch5	0x1212	Frame Composer Audio Data Channel 5 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgaud0ch6	0x1213	Frame Composer Audio Data Channel 6 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch6	0x1214	Frame Composer Audio Data Channel 6 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch6	0x1215	Frame Composer Audio Data Channel 6 Register 2 Configures the audio fixed data to be used in

Register	Offset	Description
		channel...
fc_dbgaud0ch7	0x1216	Frame Composer Audio Data Channel 7 Register 0 Configures the audio fixed data to be used in channel...
fc_dbgaud1ch7	0x1217	Frame Composer Audio Data Channel 7 Register 1 Configures the audio fixed data to be used in channel...
fc_dbgaud2ch7	0x1218	Frame Composer Audio Data Channel 7 Register 2 Configures the audio fixed data to be used in channel...
fc_dbgtmds[0:2]	0x1219 + (i * 0x1)	Frame Composer TMDS Data Channel Register Array Configures the video fixed data to be used in TMDS...

fc_invidconf

Description: Frame Composer Input Video Configuration and HDCP Keepout Register

Size: 8 bits

Offset: 0x1000

Bits	Name	Attr	Description
7	HDCP_keepout	R/W	Start/stop HDCP keepout window generation 1b: Active Value After Reset: 0x0
6	vsync_in_polarity	R/W	Vsync input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
5	hsync_in_polarity	R/W	Hsync input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
4	de_in_polarity	R/W	Data enable input polarity 1b: Active high 0b: Active low Value After Reset: 0x1
3	DVI_modez	R/W	Active low 0b: DVI mode selected 1b: HDMI mode selected Value After Reset: 0x0
2			Reserved for future use.
1	r_v_blank_in_osc	R/W	Used for CEA861-D modes with fractional Vblank (for example, modes 5, 6, 7, 10, 11, 20, 21, and 22). For more modes, see the CEA861-D specification. Note: Set this field to 1 for video mode 39, although there is no Vblank oscillation. 1b: Active high Value After Reset: 0x0

Fields for Register: fc_invidconf (Continued)

Bits	Name	Attr	Description
0	in_I_P	R/W	Input video mode: 1b: Interlaced 0b: Progressive Value After Reset: 0x0

fc_inhactiv0

Description: Frame Composer Input Video HActive Pixels Register 0

Size: 8 bits

Offset: 0x1001

Bits	Name	Attr	Description
7:0	H_in_activ	R/W	Input video Horizontal active pixel region width. Number of Horizontal active pixels [0...8191]. Value After Reset: 0x0

fc_inhactiv1

Description: Frame Composer Input Video HActive Pixels Register 1

Size: 8 bits

Offset: 0x1002

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	H_in_activ_13	R/W	Input video Horizontal active pixel region width (0 .. 16383) If the configuration parameter HDMI_TX_20 = True (1), this bit field holds bit 13. Value After Reset: 0x0

Fields for Register: fc_inhactiv1 (Continued)

Bits	Name	Attr	Description
4	H_in_activ_12	R/W	Input video Horizontal active pixel region width (0 . . 8191) If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12. Value After Reset: 0x0
3:0	H_in_activ	R/W	Input video Horizontal active pixel region width Value After Reset: 0x0

fc_inhblank0

Description: Frame Composer Input Video HBlank Pixels Register 0

Size: 8 bits

Offset: 0x1003

Bits	Name	Attr	Description
7:0	H_in_blank	R/W	Input video Horizontal blanking pixel region width. Number of Horizontal blanking pixels [0...4095]. Value After Reset: 0x0

fc_inhblank1

Description: Frame Composer Input Video HBlank Pixels Register 1

Size: 8 bits
Offset: 0x1004

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:2	H_in_blank_12	R/W	Input video Horizontal blanking pixel region width If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12:10 of number of horizontal blanking pixels. Value After Reset: 0x0
1:0	H_in_blank	R/W	Input video Horizontal blanking pixel region width this bit field holds bits 9:8 of number of Horizontal blanking pixels. Value After Reset: 0x0

fc_invactiv0
Description: Frame Composer Input Video VActive Pixels Register 0
Size: 8 bits
Offset: 0x1005

Bits	Name	Attr	Description
7:0	V_in_activ	R/W	Input video Vertical active pixel region width. This bit field holds bits 7:0 of number of Vertical active pixels. Value After Reset: 0x0

fc_invactiv1
Description: Frame Composer Input Video VActive Pixels Register 1
Size: 8 bits
Offset: 0x1006

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:3	V_in_activ_12_11	R/W	Input video Vertical active pixel region width. If the configuration parameter HDMI_TX_14 = True (1), this bit field holds bits 12:10 of number of Vertical active pixels. Value After Reset: 0x0
2:0	V_in_activ	R/W	Input video Vertical active pixel region width. This bit field holds bits 9:8 of number of Vertical active pixels. Value After Reset: 0x0

fc_invblank
Description: Frame Composer Input Video VBlank Pixels Register
Size: 8 bits
Offset: 0x1007

Bits	Name	Attr	Description
7:0	V_in_blank	R/W	Input video Vertical blanking pixel region width.

			Number of Vertical blanking lines [0...255]. Value After Reset: 0x0

fc_hsyncindelay0

Description: Frame Composer Input Video HSync Front Porch Register 0

Size: 8 bits

Offset: 0x1008

Bits	Name	Attr	Description
7:0	H_in_delay	R/W	Input video Hsync active edge delay. Integer number of pixel clock cycles from "de" non active edge of the last "de" valid period [0...4095]. Value After Reset: 0x0

fc_hsyncindelay1

Description: Frame Composer Input Video HSync Front Porch Register 1

Size: 8 bits

Offset: 0x1009

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:3	H_in_delay_12	R/W	Input video Horizontal active edge delay. If configuration parameter HDMI_TX_14 = True (1), this bit field holds bit 12. Integer number of pixel clock cycles from "de" non-active edge of the last "de" valid period [0...8191]. Value After Reset: 0x0
2:0	H_in_delay	R/W	Input video Horizontal active edge delay. Value After Reset: 0x0

fc_hsyncinwidth0

Description: Frame Composer Input Video HSync Width Register 0

Size: 8 bits

Offset: 0x100a

Bits	Name	Attr	Description
7:0	H_in_width	R/W	Input video Hsync active pulse width. Integer number of pixel clock cycles [0...511]. Value After Reset: 0x0

fc_hsyncinwidth1

Description: Frame Composer Input Video HSync Width Register 1

Size: 8 bits

Offset: 0x100b

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	H_in_width_9	R/W	Input video Hsync active pulse width. If configuration parameter HDMI_TX_14 = True (1), then this bit field holds bit 9. Number of

			Horizontal active pixels [0...1024]. Value After Reset: 0x0
0	H_in_width	R/W	Input video Hsync active pulse width. Value After Reset: 0x0

fc_vsyncindelay

Description: Frame Composer Input Video VSync Front Porch Register

Size: 8 bits

Offset: 0x100c

Bits	Name	Attr	Description
7:0	V_in_delay	R/W	Input video Vsync active edge delay. Integer number of Hsync pulses from "de" non active edge of the last "de" valid period. [0...255]. Value After Reset: 0x0

fc_vsyncinwidth

Description: Frame Composer Input Video VSync Width Register

Size: 8 bits

Offset: 0x100d

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	V_in_width	R/W	Description: Input video Vsync active pulse width. Integer number of video lines [0...63]. Value After Reset: 0x0

fc_infreq0

Description: Frame Composer Input Video Refresh Rate Register 0

Size: 8 bits

Offset: 0x100e

Bits	Name	Attr	Description
7:0	infreq	R/W	Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes. The Hdmi_tx does not write any data to this register; the data written by software is not used by the Hdmi_tx. Value After Reset: 0x0

fc_infreq1

Description: Frame Composer Input Video Refresh Rate Register 1

Size: 8 bits

Offset: 0x100f

Bits	Name	Attr	Description
7:0	infreq	R/W	Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes. The Hdmi_tx does not write any data to this register; the data written by software is not used

			by the Hdmi_tx. Value After Reset: 0x0

fc_infreq2

Description: Frame Composer Input Video Refresh Rate Register 2

Size: 8 bits

Offset: 0x1010

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	infreq	R/W	Video refresh rate in Hz*1E3 format. This register is provided for debug and informative purposes. The Hdmi_tx does not write any data to this register; the data written by software is not used by the Hdmi_tx. Value After Reset: 0x0

fc_ctrldur

Description: Frame Composer Control Period Duration Register

Size: 8 bits

Offset: 0x1011

Bits	Name	Attr	Description
7:0	ctrlperiodduration	R/W	Configuration of the control period minimum duration (minimum of 12 pixel clock cycles; refer to HDMI 1.4b specification). Integer number of pixel clocks cycles [0..223]. Value After Reset: 0x0

fc_exctrldur

Description: Frame Composer Extended Control Period Duration Register

Size: 8 bits

Offset: 0x1012

Bits	Name	Attr	Description
7:0	exctrlperiodduration	R/W	Configuration of the extended control period minimum duration (minimum of 32 pixel clock cycles; refer to HDMI 1.4b specification). Integer number of pixel clocks cycles [0..223]. Value After Reset: 0x0

fc_exctrlspac

Description: Frame Composer Extended Control Period Maximum Spacing Register

Size: 8 bits

Offset: 0x1013

Bits	Name	Attr	Description
7:0	exctrlperiodspacing	R/W	Configuration of the maximum spacing between consecutive extended control periods (maximum of 50ms; refer to the applicable HDMI specification).

			When using the HDMI 2.0 supported features (HDMI_TX_20 = 1): generated spacing = (1/freq tmds clock)*256*512*(extctrlperiodspacing +1) else generated spacing = (1/freq tmds clock)*256*256*(extctrlperiodspacing +1) Value After Reset: 0x0

fc_ch0pream

Description: Frame Composer Channel 0 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1014

Bits	Name	Attr	Description
7:0	ch0_preamble_filter	R/W	When in control mode, configures 8 bits that fill the channel 0 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_ch1pream

Description: Frame Composer Channel 1 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1015

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	ch1_preamble_filter	R/W	When in control mode, configures 6 bits that fill the channel 1 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_ch2pream

Description: Frame Composer Channel 2 Non-Preamble Data Register

Size: 8 bits

Offset: 0x1016

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:0	ch2_preamble_filter	R/W	When in control mode, configures 6 bits that fill the channel 2 data lines not used to transmit the preamble (for more clarification, refer to the HDMI 1.4b specification). Value After Reset: 0x0

fc_aviconf3

Description: Frame Composer AVI Packet Configuration Register 3

Size: 8 bits
Offset: 0x1017

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:2	YQ	R/W	YCC Quantization range according to the CEA specification Value After Reset: 0x0
1:0	CN	R/W	IT content type according to CEA the specification Value After Reset: 0x0

fc_gcp
Description: Frame Composer GCP Packet Configuration Register
Size: 8 bits
Offset: 0x1018

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	default_phase	R/W	Value of "default_phase" in the GCP packet. This data must be equal to the default phase used at Video Packetizer packing machine. Value After Reset: 0x0
1	set_avmute	R/W	Value of "set_avmute" in the GCP packet Once the AVmute is set, the frame composer schedules the GCP packet with AVmute set in the packet scheduler to be sent once (may only be transmitted between the active edge of VSYNC and 384 pixels following this edge). Value After Reset: 0x0
0	clear_avmute	R/W	Value of "clear_avmute" in the GCP packet Value After Reset: 0x0

fc_aviconf0
Description: Frame Composer AVI Packet Configuration Register 0
Size: 8 bits
Offset: 0x1019

Bits	Name	Attr	Description
7	rgc_ycc_indication_2	R/W	Y2, Bit 2 of rgc_ycc_indication Value After Reset: 0x0
6	active_format_present	R/W	Active format present Value After Reset: 0x0
5:4	scan_information	R/W	Scan information Value After Reset: 0x0
3:2	bar_information	R/W	Bar information data valid Value After Reset: 0x0
1:0	rgc_ycc_indication	R/W	Y1,Y0 RGB or YCC indicator Value After Reset: 0x0

fc_aviconf1
Description: Frame Composer AVI Packet Configuration Register 1
Size: 8 bits

Offset: 0x101a

Bits	Name	Attr	Description
7:6	Colorimetry	R/W	Colorimetry Value After Reset: 0x0
5:4	picture_aspect_ratio	R/W	Picture aspect ratio Value After Reset: 0x0
3:0	active_aspect_ratio	R/W	Active aspect ratio Value After Reset: 0x0

fc_aviconf2

Description: Frame Composer AVI Packet Configuration Register 2

Size: 8 bits

Offset: 0x101b

Bits	Name	Attr	Description
7	it_content	R/W	IT content Value After Reset: 0x0
6:4	extended_colorimetry	R/W	Extended colorimetry Value After Reset: 0x0
3:2	quantization_range	R/W	Quantization range Value After Reset: 0x0
1:0	non_uniform_picture_scaling	R/W	Non-uniform picture scaling Value After Reset: 0x0

fc_avivid

Description: Frame Composer AVI Packet VIC Register

Size: 8 bits

Offset: 0x101c

Bits	Name	Attr	Description
7	fc_avivid_7	R/W	Bit 7 of fc_avivid register Value After Reset: 0x0
6:0	fc_avivid	R/W	Configures the AVI InfoFrame Video Identification code. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avietb[0:1]

Description: Frame Composer AVI Packet End of Top Bar Register Array

Size: 8 bits

Offset: 0x101d + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avietb	R/W	Defines the AVI InfoFrame End of Top Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avisbb[0:1]

Description: Frame Composer AVI Packet Start of Bottom Bar Register Array

Size: 8 bits

Offset: 0x101f + (i * 0x1)

Bits	Name	Attr	Description

7:0	fc_avisbb	R/W	This register defines the AVI InfoFrame Start of Bottom Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avielb[0:1]

Description: Frame Composer AVI Packet End of Left Bar Register Array

Size: 8 bits

Offset: 0x1021 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avielb	R/W	This register defines the AVI InfoFrame End of Left Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_avisrb[0:1]

Description: Frame Composer AVI Packet Start of Right Bar Register Array

Size: 8 bits

Offset: 0x1023 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_avisrb	R/W	This register defines the AVI InfoFrame Start of Right Bar value. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_audiconf0

Description: Frame Composer AUD Packet Configuration Register 0

Size: 8 bits

Offset: 0x1025

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	CC	R/W	Channel count Value After Reset: 0x0
3:0	CT	R/W	Coding Type Value After Reset: 0x0

fc_audiconf1

Description: Frame Composer AUD Packet Configuration Register 1

Size: 8 bits

Offset: 0x1026

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:4	SS	R/W	Sampling size Value After Reset: 0x0
3			Reserved for future use.
2:0	SF	R/W	Sampling frequency Value After Reset: 0x0

fc_audiconf2

Description: Frame Composer AUD Packet Configuration Register 2

Size: 8 bits

Offset: 0x1027

Bits	Name	Attr	Description
7:0	CA	R/W	Channel allocation Value After Reset: 0x0

fc_audiconf3

Description: Frame Composer AUD Packet Configuration Register 3

Size: 8 bits

Offset: 0x1028

Bits	Name	Attr	Description
7			Reserved for future use.
6:5	LFEPBL	R/W	LFE playback information LFEPBL1, LFEPBL0 LFE playback level as compared to the other channels. Value After Reset: 0x0
4	DM_INH	R/W	Down mix enable Value After Reset: 0x0
3:0	LSV	R/W	Level shift value (for down mixing) Value After Reset: 0x0

fc_vsdieeeid2

Description: Frame Composer VSI Packet Data IEEE Register 2

Size: 8 bits

Offset: 0x1029

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA- 861-E specification. Value After Reset: 0x0

fc_vsdsize

Description: Frame Composer VSI Packet Data Size Register

Size: 8 bits

Offset: 0x102a

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	VSDSIZE	R/W	Packet size as described in the HDMI Vendor Specific InfoFrame (from the HDMI specification). Value After Reset: 0x1b

fc_vsdieeeid1

Description: Frame Composer VSI Packet Data IEEE Register 1

Size: 8 bits

Offset: 0x1030

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_vsdieeeid0

Description: Frame Composer VSI Packet Data IEEE Register 0

Size: 8 bits

Offset: 0x1031

Bits	Name	Attr	Description
7:0	IEEE	R/W	This register configures the Vendor Specific InfoFrame IEEE registration identifier. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_vsdpayload[0:23]

Description: Frame Composer VSI Packet Data Payload Register Array

Size: 8 bits

Offset: 0x1032 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_vsdpayload	R/W	Frame Composer VSI Packet Data Payload Register Array Configures the Vendor Specific infoFrame 24 bytes specific payload. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spdvendorname[0:7]

Description: Frame Composer SPD Packet Data Vendor Name Register Array

Size: 8 bits

Offset: 0x104a + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_spdvendorname	R/W	Frame Composer SPD Packet Data Vendor Name Register Array Configures the Source Product Descriptor infoFrame 8 bytes Vendor name. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spdproductname[0:15]

Description: Frame Composer SPD packet Data Product Name Register Array

Size: 8 bits

Offset: 0x1052 + (i * 0x1)

Bits	Name	Attr	Description

7:0	fc_spdproductname	R/W	Frame Composer SPD packet Data Product Name Register Array Configures the Source Product Descriptor infoFrame 16 bytes Product name. For more information, refer to the CEA-861-E specification. Value After Reset: 0x0

fc_spddeviceinf

Description: Frame Composer SPD Packet Data Source Product Descriptor Register
Size: 8 bits
Offset: 0x1062

Bits	Name	Attr	Description
7:0	fc_spddeviceinf	R/W	Frame Composer SPD Packet Data Source Product Descriptor Register Value After Reset: 0x0

fc_audsconf

Description: Frame Composer Audio Sample Flat and Layout Configuration Register
Size: 8 bits
Offset: 0x1063

Bits	Name	Attr	Description
7:4	aud_packet_sampflt	R/W	Set the audio packet sample flat value to be sent on the packet. Value After Reset: 0x0
3:1			Reserved for future use.
0	aud_packet_layout	R/W	Set the audio packet layout to be sent in the packet: 1b: layout 1 0b: layout 0 If HDMI_TX_20 is defined and register field fc_multistream_ctrl.fc_mas_packet_en is active, this bit has no effect. Value After Reset: 0x0

fc_audsstat

Description: Frame Composer Audio Sample Flat and Layout Status Register
Size: 8 bits
Offset: 0x1064

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	packet_sampprs	R	Shows the data sample present indication of the last Audio sample packet sent by the HDMI Tx Controller. This register information is at TMDS clock rate. Value After Reset: 0x0

fc_audsv

Description: Frame Composer Audio Sample Validity Flag Register

Size: 8 bits

Offset: 0x1065

Bits	Name	Attr	Description
7	V3r	R/W	Set validity bit "V" for Channel 3, Right Value After Reset: 0x0
6	V2r	R/W	Set validity bit "V" for Channel 2, Right Value After Reset: 0x0
5	V1r	R/W	Set validity bit "V" for Channel 1, Right Value After Reset: 0x0
4	V0r	R/W	Set validity bit "V" for Channel 0, Right Value After Reset: 0x0
3	V3l	R/W	Set validity bit "V" for Channel 3, Left Value After Reset: 0x0
2	V2l	R/W	Set validity bit "V" for Channel 2, Left Value After Reset: 0x0
1	V1l	R/W	Set validity bit "V" for Channel 1, Left Value After Reset: 0x0
0	V0l	R/W	Set validity bit "V" for Channel 0, Left Value After Reset: 0x0

fc_audsu

Description: Frame Composer Audio Sample User Flag Register

Size: 8 bits

Offset: 0x1066

Bits	Name	Attr	Description
7	U3r	R/W	Set user bit "U" for Channel 3, Right Value After Reset: 0x0
6	U2r	R/W	Set user bit "U" for Channel 2, Right Value After Reset: 0x0
5	U1r	R/W	Set user bit "U" for Channel 1, Right Value After Reset: 0x0
4	U0r	R/W	Set user bit "U" for Channel 0, Right Value After Reset: 0x0
3	U3l	R/W	Set user bit "U" for Channel 3, Left Value After Reset: 0x0
2	U2l	R/W	Set user bit "U" for Channel 2, Left Value After Reset: 0x0
1	U1l	R/W	Set user bit "U" for Channel 1, Left Value After Reset: 0x0
0	U0l	R/W	Set user bit "U" for Channel 0, Left Value After Reset: 0x0

fc_audschnl0

Description: Frame Composer Audio Sample Channel Status Configuration Register 0

Size: 8 bits
Offset: 0x1067

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:4	oiec_cgmsa	R/W	CGMS-A Value After Reset: 0x0
3:1			Reserved for future use.
0	oiec_copyright	R/W	IEC Copyright indication Value After Reset: 0x0

fc_audschnl1
Description: Frame Composer Audio Sample Channel Status Configuration Register 1
Size: 8 bits
Offset: 0x1068

Bits	Name	Attr	Description
7:0	oiec_categorycode	R/W	Category code Value After Reset: 0x0

fc_audschnl2
Description: Frame Composer Audio Sample Channel Status Configuration Register 2
Size: 8 bits
Offset: 0x1069

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	oiec_pcmaudiomode	R/W	PCM audio mode Value After Reset: 0x0
3:0	oiec_sourcenumber	R/W	Source number Value After Reset: 0x0

fc_audschnl3
Description: Frame Composer Audio Sample Channel Status Configuration Register 3
Size: 8 bits
Offset: 0x106a

Bits	Name	Attr	Description
7:4	oiec_channelnumcr1	R/W	Channel number for second right sample Value After Reset: 0x0
3:0	oiec_channelnumcr0	R/W	Channel number for first right sample Value After Reset: 0x0

fc_audschnl4
Description: Frame Composer Audio Sample Channel Status Configuration Register 4
Size: 8 bits
Offset: 0x106b

Bits	Name	Attr	Description
7:4	oiec_channelnumcr3	R/W	Channel number for fourth right sample Value After Reset: 0x0
3:0	oiec_channelnumcr2	R/W	Channel number for third right sample

			Value After Reset: 0x0

fc_audschnl5

Description: Frame Composer Audio Sample Channel Status Configuration Register 5

Size: 8 bits

Offset: 0x106c

Bits	Name	Attr	Description
7:4	oiec_channelnumcl1	R/W	Channel number for second left sample Value After Reset: 0x0
3:0	oiec_channelnumcl0	R/W	Channel number for first left sample Value After Reset: 0x0

fc_audschnl6

Description: Frame Composer Audio Sample Channel Status Configuration Register 6

Size: 8 bits

Offset: 0x106d

Bits	Name	Attr	Description
7:4	oiec_channelnumcl3	R/W	Channel number for fourth left sample Value After Reset: 0x0
3:0	oiec_channelnumcl2	R/W	Channel number for third left sample Value After Reset: 0x0

fc_audschnl7

Description: Frame Composer Audio Sample Channel Status Configuration Register 7

Size: 8 bits

Offset: 0x106e

Bits	Name	Attr	Description
7:6	oiec_sampfreq_ext	R/W	Sampling frequency (channel status bits 31 and 30) Value After Reset: 0x0
5:4	oiec_clkaccuracy	R/W	Clock accuracy Value After Reset: 0x0
3:0	oiec_sampfreq	R/W	Sampling frequency Value After Reset: 0x0

fc_audschnl8

Description: Frame Composer Audio Sample Channel Status Configuration Register 8

Size: 8 bits

Offset: 0x106f

Bits	Name	Attr	Description
7:4	oiec_origsampfreq	R/W	Original sampling frequency Value After Reset: 0x0
3:0	oiec_wordlength	R/W	Word length configuration Value After Reset: 0x0

fc_ctrlqhigh

Description: Frame Composer Number of High Priority Packets Attended Configuration Register

Size: 8 bits
Offset: 0x1073

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	onhighattended	R/W	Configures the number of high priority packets or audio sample packets consecutively attended before checking low priority queue status. Valid range is from 5'd1 to 5'd31. Value After Reset: 0xf

fc_ctrlqlow
Description: Frame Composer Number of Low Priority Packets Attended Configuration Register
Size: 8 bits
Offset: 0x1074

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	onlowattended	R/W	Configures the number of low priority packets or null packets consecutively attended before checking high priority queue status or audio samples availability. Valid range is from 5'd1 to 5'd31. Value After Reset: 0x3

fc_acp0
Description: Frame Composer ACP Packet Type Configuration Register 0
Size: 8 bits
Offset: 0x1075

Bits	Name	Attr	Description
7:0	acptype	R/W	Configures the ACP packet type. Value After Reset: 0x0

fc_acp16
Description: Frame Composer ACP Packet Body Configuration Register 16
Size: 8 bits
Offset: 0x1082

Bits	Name	Attr	Description
7:0	fc_acp16	R/W	Frame Composer ACP Packet Body Configuration Register 16 Value After Reset: 0x0

fc_acp15
Description: Frame Composer ACP Packet Body Configuration Register 15
Size: 8 bits
Offset: 0x1083

Bits	Name	Attr	Description

7:0	fc_acp15	R/W	Frame Composer ACP Packet Body Configuration Register 15 Value After Reset: 0x0

fc_acp14

Description: Frame Composer ACP Packet Body Configuration Register 14

Size: 8 bits

Offset: 0x1084

Bits	Name	Attr	Description
7:0	fc_acp14	R/W	Frame Composer ACP Packet Body Configuration Register 14 Value After Reset: 0x0

fc_acp13

Description: Frame Composer ACP Packet Body Configuration Register 13

Size: 8 bits

Offset: 0x1085

Bits	Name	Attr	Description
7:0	fc_acp13	R/W	Frame Composer ACP Packet Body Configuration Register 13 Value After Reset: 0x0

fc_acp12

Description: Frame Composer ACP Packet Body Configuration Register 12

Size: 8 bits

Offset: 0x1086

Bits	Name	Attr	Description
7:0	fc_acp12	R/W	Frame Composer ACP Packet Body Configuration Register 12 Value After Reset: 0x0

fc_acp11

Description: Frame Composer ACP Packet Body Configuration Register 11

Size: 8 bits

Offset: 0x1087

Bits	Name	Attr	Description
7:0	fc_acp11	R/W	Frame Composer ACP Packet Body Configuration Register 11 Value After Reset: 0x0

fc_acp10

Description: Frame Composer ACP Packet Body Configuration Register 10

Size: 8 bits

Offset: 0x1088

Bits	Name	Attr	Description
7:0	fc_acp10	R/W	Frame Composer ACP Packet Body Configuration

			Register 10 Value After Reset: 0x0

fc_acp9
Description: Frame Composer ACP Packet Body Configuration Register 9
Size: 8 bits
Offset: 0x1089

Bits	Name	Attr	Description
7:0	fc_acp9	R/W	Frame Composer ACP Packet Body Configuration Register 9 Value After Reset: 0x0

fc_acp8
Description: Frame Composer ACP Packet Body Configuration Register 8
Size: 8 bits
Offset: 0x108a

Bits	Name	Attr	Description
7:0	fc_acp8	R/W	Frame Composer ACP Packet Body Configuration Register 8 Value After Reset: 0x0

fc_acp7
Description: Frame Composer ACP Packet Body Configuration Register 7
Size: 8 bits
Offset: 0x108b

Bits	Name	Attr	Description
7:0	fc_acp7	R/W	Frame Composer ACP Packet Body Configuration Register 7 Value After Reset: 0x0

fc_acp6
Description: Frame Composer ACP Packet Body Configuration Register 6
Size: 8 bits
Offset: 0x108c

Bits	Name	Attr	Description
7:0	fc_acp6	R/W	Frame Composer ACP Packet Body Configuration Register 6 Value After Reset: 0x0

fc_acp5
Description: Frame Composer ACP Packet Body Configuration Register 5
Size: 8 bits
Offset: 0x108d

Bits	Name	Attr	Description
7:0	fc_acp5	R/W	Frame Composer ACP Packet Body Configuration Register 5

			Value After Reset: 0x0

fc_acp4

Description: Frame Composer ACP Packet Body Configuration Register 4

Size: 8 bits

Offset: 0x108e

Bits	Name	Attr	Description
7:0	fc_acp4	R/W	Frame Composer ACP Packet Body Configuration Register 4 Value After Reset: 0x0

fc_acp3

Description: Frame Composer ACP Packet Body Configuration Register 3

Size: 8 bits

Offset: 0x108f

Bits	Name	Attr	Description
7:0	fc_acp3	R/W	Frame Composer ACP Packet Body Configuration Register 3 Value After Reset: 0x0

fc_acp2

Description: Frame Composer ACP Packet Body Configuration Register 2

Size: 8 bits

Offset: 0x1090

Bits	Name	Attr	Description
7:0	fc_acp2	R/W	Frame Composer ACP Packet Body Configuration Register 2 Value After Reset: 0x0

fc_acp1

Description: Frame Composer ACP Packet Body Configuration Register 1

Size: 8 bits

Offset: 0x1091

Bits	Name	Attr	Description
7:0	fc_acp1	R/W	Frame Composer ACP Packet Body Configuration Register 1 Value After Reset: 0x0

fc_iscr1_0

Description: Frame Composer ISRC1 Packet Status, Valid, and Continue Configuration Register

Size: 8 bits

Offset: 0x1092

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:2	isrc_status	R/W	ISRC1 Status signal Value After Reset: 0x0

1	isrc_valid	R/W	ISRC1 Valid control signal Value After Reset: 0x0
0	isrc_cont	R/W	ISRC1 Indication of packet continuation (ISRC2 will be transmitted) Value After Reset: 0x0

fc_iscr1_16

Description: Frame Composer ISRC1 Packet Body Register 16

Size: 8 bits

Offset: 0x1093

Bits	Name	Attr	Description
7:0	fc_iscr1_16	R/W	Frame Composer ISRC1 Packet Body Register 16; configures ISRC1 packet body of the ISRC1 packet Value After Reset: 0x0

fc_iscr1_15

Description: Frame Composer ISRC1 Packet Body Register 15

Size: 8 bits

Offset: 0x1094

Bits	Name	Attr	Description
7:0	fc_iscr1_15	R/W	Frame Composer ISRC1 Packet Body Register 15 Value After Reset: 0x0

fc_iscr1_14

Description: Frame Composer ISRC1 Packet Body Register 14

Size: 8 bits

Offset: 0x1095

Bits	Name	Attr	Description
7:0	fc_iscr1_14	R/W	Frame Composer ISRC1 Packet Body Register 14 Value After Reset: 0x0

fc_iscr1_13

Description: Frame Composer ISRC1 Packet Body Register 13

Size: 8 bits

Offset: 0x1096

Bits	Name	Attr	Description
7:0	fc_iscr1_13	R/W	Frame Composer ISRC1 Packet Body Register 13 Value After Reset: 0x0

fc_iscr1_12

Description: Frame Composer ISRC1 Packet Body Register 12

Size: 8 bits

Offset: 0x1097

Bits	Name	Attr	Description
7:0	fc_iscr1_12	R/W	Frame Composer ISRC1 Packet Body Register 12 Value After Reset: 0x0

fc_iscr1_11

Description: Frame Composer ISRC1 Packet Body Register 11

Size: 8 bits

Offset: 0x1098

Bits	Name	Attr	Description
7:0	fc_iscr1_11	R/W	Frame Composer ISRC1 Packet Body Register 11 Value After Reset: 0x0

fc_iscr1_10

Description: Frame Composer ISRC1 Packet Body Register 10

Size: 8 bits

Offset: 0x1099

Bits	Name	Attr	Description
7:0	fc_iscr1_10	R/W	Frame Composer ISRC1 Packet Body Register 10 Value After Reset: 0x0

fc_iscr1_9

Description: Frame Composer ISRC1 Packet Body Register 9

Size: 8 bits

Offset: 0x109a

Bits	Name	Attr	Description
7:0	fc_iscr1_9	R/W	Frame Composer ISRC1 Packet Body Register 9 Value After Reset: 0x0

fc_iscr1_8

Description: Frame Composer ISRC1 Packet Body Register 8

Size: 8 bits

Offset: 0x109b

Bits	Name	Attr	Description
7:0	fc_iscr1_8	R/W	Frame Composer ISRC1 Packet Body Register 8 Value After Reset: 0x0

fc_iscr1_7

Description: Frame Composer ISRC1 Packet Body Register 7

Size: 8 bits

Offset: 0x109c

Bits	Name	Attr	Description
7:0	fc_iscr1_7	R/W	Frame Composer ISRC1 Packet Body Register 7 Value After Reset: 0x0

fc_iscr1_6

Description: Frame Composer ISRC1 Packet Body Register 6

Size: 8 bits

Offset: 0x109d

Bits	Name	Attr	Description
7:0	fc_iscr1_6	R/W	Frame Composer ISRC1 Packet Body Register 6

			Value After Reset: 0x0

fc_iscr1_5

Description: Frame Composer ISRC1 Packet Body Register 5

Size: 8 bits

Offset: 0x109e

Bits	Name	Attr	Description
7:0	fc_iscr1_5	R/W	Frame Composer ISRC1 Packet Body Register 5 Value After Reset: 0x0

fc_iscr1_4

Description: Frame Composer ISRC1 Packet Body Register 4

Size: 8 bits

Offset: 0x109f

Bits	Name	Attr	Description
7:0	fc_iscr1_4	R/W	Frame Composer ISRC1 Packet Body Register 4 Value After Reset: 0x0

fc_iscr1_3

Description: Frame Composer ISRC1 Packet Body Register 3

Size: 8 bits

Offset: 0x10a0

Bits	Name	Attr	Description
7:0	fc_iscr1_3	R/W	Frame Composer ISRC1 Packet Body Register 3 Value After Reset: 0x0

fc_iscr1_2

Description: Frame Composer ISRC1 Packet Body Register 2

Size: 8 bits

Offset: 0x10a1

Bits	Name	Attr	Description
7:0	fc_iscr1_2	R/W	Frame Composer ISRC1 Packet Body Register 2 Value After Reset: 0x0

fc_iscr1_1

Description: Frame Composer ISRC1 Packet Body Register 1

Size: 8 bits

Offset: 0x10a2

Bits	Name	Attr	Description
7:0	fc_iscr1_1	R/W	Frame Composer ISRC1 Packet Body Register 1 Value After Reset: 0x0

fc_iscr2_15

Description: Frame Composer ISRC2 Packet Body Register 15

Size: 8 bits

Offset: 0x10a3

Bits	Name	Attr	Description
7:0	fc_iscr2_15	R/W	Frame Composer ISRC2 Packet Body Register 15; configures the ISRC2 packet body of the ISRC2 packet Value After Reset: 0x0

fc_iscr2_14

Description: Frame Composer ISRC2 Packet Body Register 14

Size: 8 bits

Offset: 0x10a4

Bits	Name	Attr	Description
7:0	fc_iscr2_14	R/W	Frame Composer ISRC2 Packet Body Register 14 Value After Reset: 0x0

fc_iscr2_13

Description: Frame Composer ISRC2 Packet Body Register 13

Size: 8 bits

Offset: 0x10a5

Bits	Name	Attr	Description
7:0	fc_iscr2_13	R/W	Frame Composer ISRC2 Packet Body Register 13 Value After Reset: 0x0

fc_iscr2_12

Description: Frame Composer ISRC2 Packet Body Register 12

Size: 8 bits

Offset: 0x10a6

Bits	Name	Attr	Description
7:0	fc_iscr2_12	R/W	Frame Composer ISRC2 Packet Body Register 12 Value After Reset: 0x0

fc_iscr2_11

Description: Frame Composer ISRC2 Packet Body Register 11

Size: 8 bits

Offset: 0x10a7

Bits	Name	Attr	Description
7:0	fc_iscr2_11	R/W	Frame Composer ISRC2 Packet Body Register 11 Value After Reset: 0x0

fc_iscr2_10

Description: Frame Composer ISRC2 Packet Body Register 10

Size: 8 bits

Offset: 0x10a8

Bits	Name	Attr	Description
7:0	fc_iscr2_10	R/W	Frame Composer ISRC2 Packet Body Register 10 Value After Reset: 0x0

fc_iscr2_9

Description: Frame Composer ISRC2 Packet Body Register 9
Size: 8 bits
Offset: 0x10a9

Bits	Name	Attr	Description
7:0	fc_iscr2_9	R/W	Frame Composer ISRC2 Packet Body Register 9 Value After Reset: 0x0

fc_iscr2_8
Description: Frame Composer ISRC2 Packet Body Register 8
Size: 8 bits
Offset: 0x10aa

Bits	Name	Attr	Description
7:0	fc_iscr2_8	R/W	Frame Composer ISRC2 Packet Body Register 8 Value After Reset: 0x0

fc_iscr2_7
Description: Frame Composer ISRC2 Packet Body Register 7
Size: 8 bits
Offset: 0x10ab

Bits	Name	Attr	Description
7:0	fc_iscr2_7	R/W	Frame Composer ISRC2 Packet Body Register 7 Value After Reset: 0x0

fc_iscr2_6
Description: Frame Composer ISRC2 Packet Body Register 6
Size: 8 bits
Offset: 0x10ac

Bits	Name	Attr	Description
7:0	fc_iscr2_6	R/W	Frame Composer ISRC2 Packet Body Register 6 Value After Reset: 0x0

fc_iscr2_5
Description: Frame Composer ISRC2 Packet Body Register 5
Size: 8 bits
Offset: 0x10ad

Bits	Name	Attr	Description
7:0	fc_iscr2_5	R/W	Frame Composer ISRC2 Packet Body Register 5 Value After Reset: 0x0

fc_iscr2_4
Description: Frame Composer ISRC2 Packet Body Register 4
Size: 8 bits
Offset: 0x10ae

Bits	Name	Attr	Description
7:0	fc_iscr2_4	R/W	Frame Composer ISRC2 Packet Body Register 4 Value After Reset: 0x0

fc_iscr2_3
Description: Frame Composer ISRC2 Packet Body Register 3
Size: 8 bits
Offset: 0x10af

Bits	Name	Attr	Description
7:0	fc_iscr2_3	R/W	Frame Composer ISRC2 Packet Body Register 3 Value After Reset: 0x0

fc_iscr2_2
Description: Frame Composer ISRC2 Packet Body Register 2
Size: 8 bits
Offset: 0x10b0

Bits	Name	Attr	Description
7:0	fc_iscr2_2	R/W	Frame Composer ISRC2 Packet Body Register 2 Value After Reset: 0x0

fc_iscr2_1
Description: Frame Composer ISRC2 Packet Body Register 1
Size: 8 bits
Offset: 0x10b1

Bits	Name	Attr	Description
7:0	fc_iscr2_1	R/W	Frame Composer ISRC2 Packet Body Register 1 Value After Reset: 0x0

fc_iscr2_0
Description: Frame Composer ISRC2 Packet Body Register 0
Size: 8 bits
Offset: 0x10b2

Bits	Name	Attr	Description
7:0	fc_iscr2_0	R/W	Frame Composer ISRC2 Packet Body Register 0 Value After Reset: 0x0

fc_datauto0
Description: Frame Composer Data Island Auto Packet Scheduling Register 0
Configures the Frame Composer RDRB(1)/Manual(0) data island packet insertion for SPD, VSD, ISRC2, ISRC1 and ACP packets. On RDRB mode the described packet scheduling is controlled by registers FC_DATAUTO1 and FC_DATAUTO2, while in Manual mode register FC_DATMAN requests to FC the insertion of the requested packet.
Size: 8 bits
Offset: 0x10b3

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	spd_auto	R/W	Enables SPD automatic packet scheduling Value After Reset: 0x0
3	vsd_auto	R/W	Enables VSD automatic packet scheduling

			Value After Reset: 0x0
2	iscr2_auto	R/W	Enables ISRC2 automatic packet scheduling Value After Reset: 0x0
1	iscr1_auto	R/W	Enables ISRC1 automatic packet scheduling Value After Reset: 0x0
0	acp_auto	R/W	Enables ACP automatic packet scheduling Value After Reset: 0x0

fc_datauto1

Description: Frame Composer Data Island Auto Packet Scheduling Register 1
Configures the Frame Composer (FC) RDRB frame interpolation for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.
Size: 8 bits
Offset: 0x10b4

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	auto_frame_interpolation	R/W	Packet frame interpolation for automatic packet scheduling Value After Reset: 0x0

fc_datauto2

Description: Frame Composer Data Island Auto packet scheduling Register 2
Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for SPD, VSD, ISRC2, ISRC1 and ACP packet insertion on data island when FC is on RDRB mode for the listed packets.
Size: 8 bits
Offset: 0x10b5

Bits	Name	Attr	Description
7:4	auto_frame_packets	R/W	Packets per frame, for automatic packet scheduling Value After Reset: 0x0
3:0	auto_line_spacing	R/W	Packets line spacing, for automatic packet scheduling Value After Reset: 0x0

fc_datman

Description: Frame Composer Data Island Manual Packet Request Register
Requests to the Frame Composer the data island packet insertion for NULL, SPD, VSD, ISRC2, ISRC1 and ACP packets when FC_DATAUTO0 bit is in manual mode for the packet requested.
Size: 8 bits
Offset: 0x10b6

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	null_tx	W	Null packet Value After Reset: 0x0
4	spd_tx	W	SPD packet

			Value After Reset: 0x0
3	vsd_tx	W	VSD packet Value After Reset: 0x0
2	iscr2_tx	W	ISRC2 packet Value After Reset: 0x0
1	iscr1_tx	W	ISRC1 packet Value After Reset: 0x0
0	acp_tx	W	ACP packet Value After Reset: 0x0

fc_datauto3

Description: Frame Composer Data Island Auto Packet Scheduling Register 3
Configures the Frame Composer Automatic(1)/RDRB(0) data island packet insertion for AVI, GCP, AUDI and ACR packets. In Automatic mode, the packet is inserted on Vblanking when first line with active Vsync appears.
Size: 8 bits
Offset: 0x10b7

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	nvbi_auto	R/W	Enables NTSC VBI packet insertion Value After Reset: 0x1
4	amp_auto	R/W	Enables AMP packet insertion Value After Reset: 0x1
3	avi_auto	R/W	Enables AVI packet insertion Value After Reset: 0x1
2	gcp_auto	R/W	Enables GCP packet insertion Value After Reset: 0x1
1	audi_auto	R/W	Enables AUDI packet insertion Value After Reset: 0x1
0	acr_auto	R/W	Enables ACR packet insertion Value After Reset: 0x1

fc_rdrb0

Description: Frame Composer Round Robin ACR Packet Insertion Register 0
Configures the Frame Composer (FC) RDRB frame interpolation for ACR packet insertion on data island when FC is on RDRB mode for this packet.
Size: 8 bits
Offset: 0x10b8

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	ACRframeinterpolation	R/W	ACR Frame interpolation Value After Reset: 0x0

fc_rdrb1

Description: Frame Composer Round Robin ACR Packet Insertion Register 1
Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the ACR packet insertion on data island when FC is on RDRB mode this packet.
Size: 8 bits
Offset: 0x10b9

Bits	Name	Attr	Description
7:4	ACRpacketsinframe	R/W	ACR packets in frame Value After Reset: 0x0
3:0	ACRpacketlinespacing	R/W	ACR packet line spacing Value After Reset: 0x0

fc_rdrb2

Description: Frame Composer Round Robin AUDI Packet Insertion Register 2
Configures the Frame Composer (FC) RDRB frame interpolation for AUDI packet insertion on data island when FC is on RDRB mode for this packet.
Size: 8 bits
Offset: 0x10ba

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	AUDIframeinterpolation	R/W	Audio frame interpolation Value After Reset: 0x0

fc_rdrb3

Description: Frame Composer Round Robin AUDI Packet Insertion Register 3
Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AUDI packet insertion on data island when FC is on RDRB mode this packet.
Size: 8 bits
Offset: 0x10bb

Bits	Name	Attr	Description
7:4	AUDIpacketsinframe	R/W	Audio packets per frame Value After Reset: 0x0
3:0	AUDIpacketlinespacing	R/W	Audio packets line spacing Value After Reset: 0x0

fc_rdrb4

Description: Frame Composer Round Robin GCP Packet Insertion Register 4
Configures the Frame Composer (FC) RDRB frame interpolation for GCP packet insertion on data island when FC is on RDRB mode for this packet.
Size: 8 bits
Offset: 0x10bc

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	GCPframeinterpolation	R/W	Frames interpolated between GCP packets Value After Reset: 0x0

fc_rdrb5

Description: Frame Composer Round Robin GCP Packet Insertion Register 5
Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the GCP packet insertion on data island when FC is on RDRB mode this packet.
Size: 8 bits
Offset: 0x10bd

Bits	Name	Attr	Description
7:4	GCPpacketsinframe	R/W	GCP packets per frame Value After Reset: 0x0
3:0	GCPpacketlinespacing	R/W	GCP packets line spacing Value After Reset: 0x0

fc_rdrb6

Description: Frame Composer Round Robin AVI Packet Insertion Register 6
Configures the Frame Composer (FC) RDRB frame interpolation for AVI packet insertion on data island when FC is on RDRB mode for this packet.
Size: 8 bits
Offset: 0x10be

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	AVIframeinterpolation	R/W	Frames interpolated between AVI packets Value After Reset: 0x0

fc_rdrb7
Description: Frame Composer Round Robin AVI Packet Insertion Register 7
Configures the Frame Composer (FC) RDRB line interpolation and number of packets in frame for the AVI packet insertion on data island when FC is on RDRB mode this packet.
Size: 8 bits
Offset: 0x10bf

Bits	Name	Attr	Description
7:4	AVIpacketsinframe	R/W	AVI packets per frame Value After Reset: 0x0
3:0	AVIpacketlinespacing	R/W	AVI packets line spacing Value After Reset: 0x0

fc_rdrb8
Description: Frame Composer Round Robin AMP Packet Insertion Register 8
Size: 8 bits
Offset: 0x10c0

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	AMPframeinterpolation	R/W	AMP frame interpolation Value After Reset: 0x0

fc_rdrb9
Description: Frame Composer Round Robin AMP Packet Insertion Register 9
Size: 8 bits
Offset: 0x10c1

Bits	Name	Attr	Description
7:4	AMPpacketsinframe	R/W	AMP packets per frame Value After Reset: 0x0
3:0	AMPpacketlinespacing	R/W	AMP packets line spacing Value After Reset: 0x0

fc_rdrb10
Description: Frame Composer Round Robin NTSC VBI Packet Insertion Register 10
Size: 8 bits
Offset: 0x10c2

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	NVBIframeinterpolation	R/W	NTSC VBI frame interpolation Value After Reset: 0x0

fc_rdrb11
Description: Frame Composer Round Robin NTSC VBI Packet Insertion Register 11

Size: 8 bits
Offset: 0x10c3

Bits	Name	Attr	Description
7:4	NVBIpacketsinframe	R/W	NTSC VBI packets per frame Value After Reset: 0x0
3:0	NVBIpacketlinespacing	R/W	NTSC VBI packets line spacing Value After Reset: 0x0

fc_rdrb12
Description: Frame Composer Round Robin DRM Packet Insertion Register 12
Size: 8 bits
Offset: 0x10c4

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	DRMframeinterpolation	R/W	Description: DRM frame interpolation Value After Reset: 0x0

fc_rdrb13
Description: Frame Composer Round Robin DRM Packet Insertion Register 13
Size: 8 bits
Offset: 0x10c5

Bits	Name	Attr	Description
7:4	DRMpacketsinframe	R/W	DRM packets per frame Value After Reset: 0x0
3:0	DRMpacketlinespacing	R/W	DRM packets line spacing Value After Reset: 0x0

fc_mask0
Description: Frame Composer Packet Interrupt Mask Register 0
Size: 8 bits
Offset: 0x10d2

Bits	Name	Attr	Description
7	AUDI	R/W	Mask bit for FC_INT0.AUDI interrupt bit Value After Reset: 0x0
6	ACP	R/W	Mask bit for FC_INT0.ACP interrupt bit Value After Reset: 0x0
5	HBR	R/W	Mask bit for FC_INT0.HBR interrupt bit Value After Reset: 0x1
4	MAS	R/W	Mask bit for FC_INT0.MAS interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
3	NVBI	R/W	Mask bit for FC_INT0.NVBI interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
2	AUDS	R/W	Mask bit for FC_INT0.AUDS interrupt bit Value After Reset: 0x1
1	ACR	R/W	Mask bit for FC_INT0.ACR interrupt bit

Bits	Name	Attr	Description
			Value After Reset: 0x0
0	NULL	R/W	Mask bit for FC_INT0.NULL interrupt bit Value After Reset: 0x1

fc_mask1

Description: Frame Composer Packet Interrupt Mask Register 1

Size: 8 bits

Offset: 0x10d6

Bits	Name	Attr	Description
7	GMD	R/W	Mask bit for FC_INT1.GMD interrupt bit Value After Reset: 0x0
6	ISCR1	R/W	Mask bit for FC_INT1.ISRC1 interrupt bit Value After Reset: 0x0
5	ISCR2	R/W	Mask bit for FC_INT1.ISRC2 interrupt bit Value After Reset: 0x0
4	VSD	R/W	Mask bit for FC_INT1.VSD interrupt bit Value After Reset: 0x0
3	SPD	R/W	Mask bit for FC_INT1.SPD interrupt bit Value After Reset: 0x0
2	AMP	R/W	Mask bit for FC_INT1.AMP interrupt bit. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(HDMI_TX_20== 1) ? 1 : 0"
1	AVI	R/W	Mask bit for FC_INT1.AVI interrupt bit Value After Reset: 0x0
0	GCP	R/W	Mask bit for FC_INT1.GCP interrupt bit Value After Reset: 0x0

fc_mask2

Description: Frame Composer High/Low Priority Overflow and DRM Interrupt Mask Register 2

Size: 8 bits

Offset: 0x10da

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	DRM	R/W	Mask bit for FC_INT2.DRM interrupt bit. Value After Reset: (HDMI_TX_20== 1) ? 1 : 0
3:2			Reserved for future use.
1	LowPriority_overflow	R/W	Mask bit for FC_INT2.LowPriority_overflow interrupt bit Value After Reset: 0x0
0	HighPriority_overflow	R/W	Mask bit for FC_INT2.HighPriority_overflow interrupt bit Value After Reset: 0x0

fc_prconf

Description: Frame Composer Pixel Repetition Configuration Register

Size: 8 bits

Offset: 0x10e0

Bits	Name	Attr	Description
7:4	incoming_pr_factor	R/W	Configures the input video pixel repetition. For CEA modes, this value must be extracted from the CEA specification for the video mode being input. incoming_pr_factor[3:0] 0000b: No action. Not used. 0001b: No pixel repetition (pixel sent only once) 0010b: Pixel sent two times (pixel repeated once) 0011b: Pixel sent three times 0100b: Pixel sent four times 0101b: Pixel sent five times 0110b: Pixel sent six times 0111b: Pixel sent seven times 1000b: Pixel sent eight times 1001b: Pixel sent nine times 1010b: Pixel sent 10 times Other: Reserved. Not used Value After Reset: 0x1
3:0	output_pr_factor	R/W	Configures the video pixel repetition ratio to be sent on the AVI InfoFrame. This value must be valid according to the HDMI specification. The output_pr_factor = incoming_pr_factor * (desired_pr_factor + 1) – 1. output_pr_factor[3:0] 0000b: No action. Not used. 0001b: Pixel sent two times (pixel repeated once) 0010b: Pixel sent three times 0011b: Pixel sent four times 0100b: Pixel sent five times 0101b: Pixel sent six times 0110b: Pixel sent seven times 0111b: Pixel sent eight times 1000b: Pixel sent nine times 1001b: Pixel sent 10 times Other: Reserved. Not used Note: When working in YCC422 video, the actual repetition of the stream is Incoming_pr_factor * (desired_pr_factor + 1). This calculation is done internally in the H13TCTRL and no hardware overflow protection is available. Care must be taken to avoid this result passes the maximum number of 10 pixels repeated because no HDMI support is available for this in the specification and the H13TPHY does not support this higher repetition values. Value After Reset: 0x0

fc_scrambler_ctrl

Description: Frame Composer Scrambler Control

Size: 8 bits

Offset: 0x10e1

Bits	Name	Attr	Description

7:5			Reserved for future use.
4	scrambler_ucp_line	R/W	Debug register. When active (1'b1), the Unscrambled Control Period is generated after each active video line (non-compliant behavior). This is quasi-static field which requires a a mc_swrstzreq.tmdsswrst_req reset request to be performed after the change of this configuration bit. Value After Reset: 0x0
3:1			Reserved for future use.
0	scrambler_on	R/W	When set (1'b1), this field activates the HDMI 2.0 scrambler feature. When disabled (1'b0) the scrambler feature is bypassed, placing Hdmi_tx in HDMI 1.4b compatible mode. To activate the scrambler feature, you must ensure that the quasi-static configuration bit fc_invidconf.HDCP_keepout is set (1'b1) at configuration time, before the required mc_swrstzreq.tmdsswrst_req reset request is issued. This is field can be changed in runtime. Value After Reset: 0x0

fc_multistream_ctrl

Description: Frame Composer Multi-Stream Audio Control

Size: 8 bits

Offset: 0x10e2

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	fc_mas_packet_en	R/W	This field, when set (1'b1), activates the HDMI 2.0 Multi- Stream support. The audio stream present at the input of the Hdmi_tx controller is transported using Multi-Stream Audio Sample Packets. Value After Reset: 0x0

fc_packet_tx_en

Description: Frame Composer Packet Transmission Control

Size: 8 bits

Offset: 0x10e3

Bits	Name	Attr	Description
7	drm_tx_en	R/W	DRM transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x0
6	nvbi_tx_en	R/W	NTSC VBI transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x0
5	amp_tx_en	R/W	AMP transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x0

4	aut_tx_en	R/W	ACP, SPD, VSIF, ISRC1, and SRC2 packet transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x1
3	audi_tx_en	R/W	AUDI packet transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x1
2	avi_tx_en	R/W	AVI packet transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x1
1	gcp_tx_en	R/W	GCP transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x1
0	acr_tx_en	R/W	ACR packet transmission control 1b: Transmission enabled 0b: Transmission disabled Value After Reset: 0x1

fc_actspc_hdlr_cfg

Description: Frame Composer Active Space Control

Size: 8 bits

Offset: 0x10e8

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	actspc_hdlr_tgl	R/W	Active Space handler control 1b: Active space 1 value is different from Active Space 2 value. Refer to Figure 8-4: 3D Structure of the HDMI 1.4b specification. 0b: Active space not oscillating Value After Reset: 0x0
0	actspc_hdlr_en	R/W	Active Space Handler Control 1b: Fixed active space value mode enabled. During active space, a fixed value of 0xAA is applied to all TMDS channels. 0b: Fixed active space value mode disabled Value After Reset: 0x0

fc_invact_2d_0

Description: Frame Composer Input Video 2D VActive Pixels Register 0

Size: 8 bits

Offset: 0x10e9

Bits	Name	Attr	Description
7:0	fc_invact_2d_0	R/W	2D Input video vertical active pixel region width. Number of 2D video vertical active lines [7:0]. Value After Reset: 0x0

fc_invact_2d_1

Description: Frame Composer Input Video VActive pixels Register 1

Size: 8 bits

Offset: 0x10ea

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	fc_invact_2d_1	R/W	2D Input video vertical active pixel region width. Number of 2D video vertical active lines [11:8]. Value After Reset: 0x0

fc_gmd_stat

Description: Frame Composer GMD Packet Status Register

Gamut metadata packet status bit information for no_current_gmd, next_gmd_field, gmd_packet_sequence and current_gamut_seq_num. For more information, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x1100

Bits	Name	Attr	Description
7	igmdno_crnt_gbd	R	Gamut scheduling: No current gamut data Value After Reset: 0x0
6	igmddnext_field	R	Gamut scheduling: Gamut Next field Value After Reset: 0x0
5:4	igmdpacket_seq	R	Gamut scheduling: Gamut packet sequence Value After Reset: 0x0
3:0	igmdcurrent_gamut_seq_num	R	Gamut scheduling: Current Gamut packet sequence number Value After Reset: 0x0

fc_gmd_en

Description: Frame Composer GMD Packet Enable Register

This register enables Gamut metadata (GMD) packet transmission. Packets are inserted in the incoming frame, starting in the line where active Vsync indication starts. After enable of GMD packets the outgoing packet is sent with no_current_gmd active indication until update GMD request is performed in the controller.

Size: 8 bits

Offset: 0x1101

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	gmdenabletx	R/W	Gamut Metadata packet transmission enable (1b) Value After Reset: 0x0

fc_gmd_up

Description: Frame Composer GMD Packet Update Register

This register performs an GMD packet content update according to the configured packet body (FC_GMD_PB0 to FC_GMD_PB27) and packet header (FC_GMD_HB). This active high auto clear register reflects the body and header configurations on the GMD packets sent arbitrating the current_gamut_seq_num, gmd_packet_sequence and next_gmd_field bits on packet to correctly indicate to source the Gamut change to be performed. After enable GMD packets the first update request is also responsible for deactivating the no_current_gmd

indication bit.
Attention packet update request must only be done after correct configuration of GMD packet body and header registers. Correct affected_gamut_seq_num and gmd_profile configuration is user responsibility and must convey with HDMI 1.4b standard gamut rules.
Size: 8 bits
Offset: 0x1102

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	gmdupdatepacket	W	Gamut Metadata packet update Value After Reset: 0x0

fc_gmd_conf
Description: Frame Composer GMD Packet Schedule Configuration Register
This register configures the number of GMD packets to be inserted per frame (starting always in the line where the active Vsync appears) and the line spacing between the transmitted GMD packets.
Note that for profile P0 (refer to the HDMI 1.4b specification) this register should only indicate one GMD packet to be inserted per video field.
Size: 8 bits
Offset: 0x1103

Bits	Name	Attr	Description
7:4	gmdpacketsinframe	R/W	Number of GMD packets per frame or video field (profile P0) Value After Reset: 0x1
3:0	gmdpacketlinespacing	R/W	Number of line spacing between the transmitted GMD packets Value After Reset: 0x0

fc_gmd_hb
Description: Frame Composer GMD Packet Profile and Gamut Sequence Configuration Register
This register configures the GMD packet header affected_gamut_seq_num and gmd_profile bits. For more information, refer to the HDMI 1.4b specification.
Size: 8 bits
Offset: 0x1104

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	gmdgbd_profile	R/W	GMD profile bits. Hdmi_tx only supports Profile 0 (P0) of the Gamut Boundary Description Metadata Profiles described in the HDMI 1.4 Specification (which defines four profiles, P0-P4). Value After Reset: 0x0
3:0	gmdaffected_gamut_seq_num	R/W	Affected gamut sequence number Value After Reset: 0x0

fc_gmd_pb[0:27]

Description: Frame Composer GMD Packet Body Register Array Configures the GMD packet body of the GMD packet.
Size: 8 bits
Offset: 0x1105 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_gmd_pb	R/W	Frame Composer GMD Packet Body Register Array Value After Reset: 0x0

fc_amp_hb1
Description: Frame Composer AMP Packet Header Register 1
Size: 8 bits
Offset: 0x1128

Bits	Name	Attr	Description
7:0	fc_amp_hb0	R/W	Frame Composer AMP Packet Header Register 1 Value After Reset: 0x0

fc_amp_hb2
Description: Frame Composer AMP Packet Header Register 2
Size: 8 bits
Offset: 0x1129

Bits	Name	Attr	Description
7:0	fc_amp_hb1	R/W	Frame Composer AMP Packet Header Register 2 Value After Reset: 0x0

fc_amp_pb[0:27]
Description: Frame Composer AMP Packet Body Register Array
Size: 8 bits
Offset: 0x112a + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_amp_pb	R/W	Frame Composer AMP Packet Body Register Array Value After Reset: 0x0

fc_nvbi_hb1
Description: Frame Composer NTSC VBI Packet Header Register 1
Size: 8 bits
Offset: 0x1148

Bits	Name	Attr	description
7:0	fc_nvbi_hb0	R/W	Frame Composer NTSC VBI Packet Header Register 1 Value After Reset: 0x0

fc_nvbi_hb2
Description: Frame Composer NTSC VBI Packet Header Register 2
Size: 8 bits
Offset: 0x1149

Bits	Name	Attr	Description
7:0	fc_nvbi_hb1	R/W	Frame Composer NTSC VBI Packet Header Register 2

			Value After Reset: 0x0

fc_nvbi_pb[0:26]

Description: Frame Composer NTSC VBI Packet Body Register Array

Size: 8 bits

Offset: 0x114a + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_nvbi_pb	R/W	Frame Composer NTSC VBI Packet Body Register Array Value After Reset: 0x0

fc_drm_up

Description: Frame Composer DRM Packet Update Register

This register performs an DRM packet content update according to the configured packet body (FC_DRM_PB0 to FC_DRM_PB27) and packet header (FC_DRM_HB). This active high auto clear register reflects the body and header configurations on the DRM packets change to be performed.

Attention packet update request must only be done after correct configuration of DRM packet body and header registers.

Size: 8 bits

Offset: 0x1167

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	drmpacketupdate	W	DRM packet update Value After Reset: 0x0

fc_drm_hb[0:1]

Description: Frame Composer DRM Packet Header Register Array

Size: 8 bits

Offset: 0x1168 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_drm_hb	R/W	Frame Composer DRM Packet Header Register Array Value After Reset: 0x0

fc_drm_pb[0:26]

Description: Frame Composer DRM Packet Body Register Array

Size: 8 bits

Offset: 0x116a + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_drm_pb	R/W	Frame Composer DRM Packet Body Register Array Value After Reset: 0x0

fc_dbgforce

Description: Frame Composer video/audio Force Enable Register

This register allows to force the controller to output audio and video data the values configured in the FC_DBGAUD and FC_DBGTMDS registers.

Size: 8 bits

Offset: 0x1200

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	forceaudio	R/W	Force fixed audio output with FC_DBGAUDxCHx register contents. Value After Reset: 0x0
3:1			Reserved for future use.
0	forcevideo	R/W	Force fixed video output with FC_DBGTMDSx register contents. Value After Reset: 0x0

fc_dbgaud0ch0

Description: Frame Composer Audio Data Channel 0 Register 0

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1201

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch0	R/W	Frame Composer Audio Data Channel 0 Register 0 Value After Reset: 0x0

fc_dbgaud1ch0

Description: Frame Composer Audio Data Channel 0 Register 1

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1202

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch0	R/W	Frame Composer Audio Data Channel 0 Register 1 Value After Reset: 0x0

fc_dbgaud2ch0

Description: Frame Composer Audio Data Channel 0 Register 2

Configures the audio fixed data to be used in channel 0 when in fixed audio selection.

Size: 8 bits

Offset: 0x1203

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch0	R/W	Frame Composer Audio Data Channel 0 Register 2 Value After Reset: 0x0

fc_dbgaud0ch1

Description: Frame Composer Audio Data Channel 1 Register 0

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1204

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch1	R/W	Frame Composer Audio Data Channel 1 Register 0 Value After Reset: 0x0

fc_dbgaud1ch1

Description: Frame Composer Audio Data Channel 1 Register 1

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1205

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch1	R/W	Frame Composer Audio Data Channel 1 Register 1 Value After Reset: 0x0

fc_dbgaud2ch1

Description: Frame Composer Audio Data Channel 1 Register 2

Configures the audio fixed data to be used in channel 1 when in fixed audio selection.

Size: 8 bits

Offset: 0x1206

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch1	R/W	Frame Composer Audio Data Channel 1 Register 2 Value After Reset: 0x0

fc_dbgaud0ch2

Description: Frame Composer Audio Data Channel 2 Register 0

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits

Offset: 0x1207

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch2	R/W	Frame Composer Audio Data Channel 2 Register 0 Value After Reset: 0x0

fc_dbgaud1ch2

Description: Frame Composer Audio Data Channel 2 Register 1

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits Offset: 0x1208

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch2	R/W	Frame Composer Audio Data Channel 2 Register 1 Value After Reset: 0x0

fc_dbgaud2ch2

Description: Frame Composer Audio Data Channel 2 Register 2

Configures the audio fixed data to be used in channel 2 when in fixed audio selection.

Size: 8 bits

Offset: 0x1209

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch2	R/W	Frame Composer Audio Data Channel 2 Register 2 Value After Reset: 0x0

fc_dbgaud0ch3

Description: Frame Composer Audio Data Channel 3 Register 0
Configures the audio fixed data to be used in channel 3 when in fixed audio selection.
Size: 8 bits
Offset: 0x120a

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch3	R/W	Frame Composer Audio Data Channel 3 Register 0 Value After Reset: 0x0

fc_dbgaud1ch3
Description: Frame Composer Audio Data Channel 3 Register 1
Configures the audio fixed data to be used in channel 3 when in fixed audio selection.
Size: 8 bits
Offset: 0x120b

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch3	R/W	Frame Composer Audio Data Channel 3 Register 1 Value After Reset: 0x0

fc_dbgaud2ch3
Description: Frame Composer Audio Data Channel 3 Register 2
Configures the audio fixed data to be used in channel 3 when in fixed audio selection.
Size: 8 bits
Offset: 0x120c

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch3	R/W	Frame Composer Audio Data Channel 3 Register 2 Value After Reset: 0x0

fc_dbgaud0ch4
Description: Frame Composer Audio Data Channel 4 Register 0
Configures the audio fixed data to be used in channel 4 when in fixed audio selection.
Size: 8 bits
Offset: 0x120d

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch4	R/W	Frame Composer Audio Data Channel 4 Register 0 Value After Reset: 0x0

fc_dbgaud1ch4
Description: Frame Composer Audio Data Channel 4 Register 1
Configures the audio fixed data to be used in channel 4 when in fixed audio selection.
Size: 8 bits
Offset: 0x120e

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch4	R/W	Frame Composer Audio Data Channel 4 Register 1 Value After Reset: 0x0

fc_dbgaud2ch4

Description: Frame Composer Audio Data Channel 4 Register 2

Configures the audio fixed data to be used in channel 4 when in fixed audio selection.

Size: 8 bits

Offset: 0x120f

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch4	R/W	Frame Composer Audio Data Channel 4 Register 2 Value After Reset: 0x0

fc_dbgaud0ch5

Description: Frame Composer Audio Data Channel 5 Register 0

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1210

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch5	R/W	Frame Composer Audio Data Channel 5 Register 0 Value After Reset: 0x0

fc_dbgaud1ch5

Description: Frame Composer Audio Data Channel 5 Register 1

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1211

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch5	R/W	Frame Composer Audio Data Channel 5 Register 1 Value After Reset: 0x0

fc_dbgaud2ch5

Description: Frame Composer Audio Data Channel 5 Register 2

Configures the audio fixed data to be used in channel 5 when in fixed audio selection.

Size: 8 bits

Offset: 0x1212

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch5	R/W	Frame Composer Audio Data Channel 5 Register 2 Value After Reset: 0x0

fc_dbgaud0ch6

Description: Frame Composer Audio Data Channel 6 Register 0

Configures the audio fixed data to be used in channel 6 when in fixed audio selection.

Size: 8 bits

Offset: 0x1213

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch6	R/W	Frame Composer Audio Data Channel 6 Register 0 Value After Reset: 0x0

fc_dbgaud1ch6

Description: Frame Composer Audio Data Channel 6 Register 1
Configures the audio fixed data to be used in channel 6 when in fixed audio selection.
Size: 8 bits
Offset: 0x1214

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch6	R/W	Frame Composer Audio Data Channel 6 Register 1 Value After Reset: 0x0

fc_dbgaud2ch6
Description: Frame Composer Audio Data Channel 6 Register 2
Configures the audio fixed data to be used in channel 6 when in fixed audio selection.
Size: 8 bits
Offset: 0x1215

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch6	R/W	Frame Composer Audio Data Channel 6 Register 2 Value After Reset: 0x0

fc_dbgaud0ch7
Description: Frame Composer Audio Data Channel 7 Register 0
Configures the audio fixed data to be used in channel 7 when in fixed audio selection.
Size: 8 bits
Offset: 0x1216

Bits	Name	Attr	Description
7:0	fc_dbgaud0ch7	R/W	Frame Composer Audio Data Channel 7 Register 0 Value After Reset: 0x0

fc_dbgaud1ch7
Description: Frame Composer Audio Data Channel 7 Register 1
Configures the audio fixed data to be used in channel 7 when in fixed audio selection.
Size: 8 bits
Offset: 0x1217

Bits	Name	Attr	Description
7:0	fc_dbgaud1ch7	R/W	Frame Composer Audio Data Channel 7 Register 1 Value After Reset: 0x0

fc_dbgaud2ch7
Description: Frame Composer Audio Data Channel 7 Register 2
Configures the audio fixed data to be used in channel 7 when in fixed audio selection.
Size: 8 bits
Offset: 0x1218

Bits	Name	Attr	Description
7:0	fc_dbgaud2ch7	R/W	Frame Composer Audio Data Channel 7 Register 2 Value After Reset: 0x0

fc_dbgtmds[0:2]

Description: Frame Composer TMDS Data Channel Register Array

Configures the video fixed data to be used in TMDS channel x (where x is 0 to 2) when in fixed video selection.

For Channel 0, this equals to set B pixel component value in RGB video or Cb pixel component value in YCbCr.

For Channel 1, this equals set G pixel component value in RGB video or Y pixel component value in YCbCr.

For Channel 2, this equals to set R pixel component value in RGB video or Cr pixel component value in YCbCr.

Size: 8 bits

Offset: 0x1219 + (i * 0x1)

Bits	Name	Attr	Description
7:0	fc_dbgtmds	R/W	Frame Composer TMDS Data Channel 0 Register Value After Reset: 0x0

PHYConfiguration Registers

PHY Configuration Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: PHYConfiguration

Register	Offset	Description
phy_conf0	0x3000	PHY Configuration Register This register holds the power down, data enable polarity, and interface...
phy_tst0	0x3001	PHY Test Interface Register 0 PHY TX mapped test interface (control). For more information, refer...
phy_tst1	0x3002	PHY Test Interface Register 1 PHY TX mapped text interface (data in). For more information, refer...
phy_tst2	0x3003	PHY Test Interface Register 2 PHY TX mapped text interface (data out). For more information, refer...
phy_stat0	0x3004	PHY RXSENSE, PLL Lock, and HPD Status Register This register contains the following active high...
phy_int0	0x3005	PHY RXSENSE, PLL Lock, and HPD Interrupt Register This register contains the interrupt indication...
phy_mask0	0x3006	PHY RXSENSE, PLL Lock, and HPD Mask Register Mask register for generation of PHY_INT0...
phy_pol0	0x3007	PHY RXSENSE, PLL Lock, and HPD Polarity Register Polarity register for generation of PHY_INT0...
PHY_PCLFREQ0	0x3008	PHY Test Interface Register 0
PHY_PCLFREQ1	0x3009	PHY Test Interface Register 1
PHY_PLLCFGFREQ0	0x300a	PHY PLL Test Interface Register 0
PHY_PLLCFGFREQ1	0x300b	PHY PLL Test Interface Register 1
PHY_PLLCFGFREQ2	0x300c	PHY PLL Test Interface Register 2
phy_i2cm_slave	0x3020	PHY I2C Slave Address Configuration Register
phy_i2cm_address	0x3021	PHY I2C Address Configuration Register This register writes the address for read and write...
phy_i2cm_datao_1	0x3022	PHY I2C Data Write Register 1

phy_i2cm_datao_0	0x3023	PHY I2C Data Write Register 0
phy_i2cm_datai_1	0x3024	PHY I2C Data Read Register 1
phy_i2cm_datai_0	0x3025	PHY I2C Data Read Register 0
phy_i2cm_operation	0x3026	PHY I2C RD/RD_EXT/WR Operation Register This register requests read and write operations from the...
phy_i2cm_int	0x3027	PHY I2C Done Interrupt Register This register contains and configures I2C master PHY done...

Registers for Address Block: PHYConfiguration (Continued)

Register	Offset	Description
phy_i2cm_ctlint	0x3028	PHY I2C error Interrupt Register This register contains and configures the I2C master PHY error...
phy_i2cm_div	0x3029	PHY I2C Speed control Register This register wets the I2C Master PHY to work in either Fast or...
phy_i2cm_softrstz	0x302a	PHY I2C SW reset control register This register sets the I2C Master PHY software reset.
phy_i2cm_ss_scl_hcnt_1_addr	0x302b	PHY I2C Slow Speed SCL High Level Control Register 1
phy_i2cm_ss_scl_hcnt_0_addr	0x302c	PHY I2C Slow Speed SCL High Level Control Register 0
phy_i2cm_ss_scl_lcnt_1_addr	0x302d	PHY I2C Slow Speed SCL Low Level Control Register 1
phy_i2cm_ss_scl_lcnt_0_addr	0x302e	PHY I2C Slow Speed SCL Low Level Control Register 0
phy_i2cm_fs_scl_hcnt_1_addr	0x302f	PHY I2C Fast Speed SCL High Level Control Register 1
phy_i2cm_fs_scl_hcnt_0_addr	0x3030	PHY I2C Fast Speed SCL High Level Control Register 0
phy_i2cm_fs_scl_lcnt_1_addr	0x3031	PHY I2C Fast Speed SCL Low Level Control Register 1
phy_i2cm_fs_scl_lcnt_0_addr	0x3032	PHY I2C Fast Speed SCL Low Level Control Register 0
phy_i2cm_sda_hold	0x3033	PHY I2C SDA HOLD Control Register
jtag_phy_config	0x3034	PHY I2C/JTAG I/O Configuration Control Register
jtag_phy_tap_tck	0x3035	PHY JTAG Clock Control Register
jtag_phy_tap_in	0x3036	PHY JTAG TAP In Control Register
jtag_phy_tap_out	0x3037	PHY JTAG TAP Out Control Register
jtag_phy_addr	0x3038	PHY JTAG Address Control Register

phy_conf0

Description: PHY Configuration Register

This register holds the power down, data enable polarity, and interface control of the HDMI Source PHY control.

Size: 8 bits

Offset: 0x3000

Bits	Name	Attr	description

7	PDZ	R/W	Power-down enable (active low 0b). Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
6	ENTMDS	R/W	Enable TMDS drivers, bias, and TMDS digital logic. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
5	svsret	R/W	PHY SVSRET signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
4	pddq	R/W	PHY PDDQ signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: "(PHY_MHL_COMBO== 1) ? 1 : 0"
3	txpwron	R/W	PHY TXPWRON signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
2	enhpdrxsense	R/W	PHY ENHPDRXSENSE signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x1
1	seldataenpol	R/W	Select data enable polarity. Value After Reset: 0x1
0	seldipif	R/W	Select interface control. Value After Reset: 0x0

phy_tst0

Description: PHY Test Interface Register 0

PHY TX mapped test interface (control).

Size: 8 bits

Offset: 0x3001

Bits	Name	Attr	Description
7:6	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
5	testclr	R/W	Test Clear signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
4	testen	R/W	Test Enable signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
3:1	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
0	testclk	R/W	Test Clock signal. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_tst1

Description: PHY Test Interface Register 1
PHY TX mapped text interface (data in).
Size: 8 bits
Offset: 0x3002

Bits	Name	Attr	Description
7:0	testdin	R/W	Test Data input Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_tst2
Description: PHY Test Interface Register 2
PHY TX mapped text interface (data out).
Size: 8 bits
Offset: 0x3003

Bits	Name	Attr	Description
7:0	testdout	R	Test Data output. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

phy_stat0
Description: PHY RXSENSE, PLL Lock, and HPD Status Register
This register contains the following active high packet sent status indications.
Size: 8 bits
Offset: 0x3004

Bits	Name	Attr	Description
7	RX_SENSE_3	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 3 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
6	RX_SENSE_2	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 2 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
5	RX_SENSE_1	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 1 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
4	RX_SENSE_0	R	Status bit. TX PHY RX_SENSE indication for TMDS channel 0 driver. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R	Status bit. HDMI Hot Plug Detect indication. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0

Bits	Name	Attr	Description
0	TX_PHY_LOCK	R	Status bit. TX PHY PLL lock indication. You may need to mask or change polarity of this interrupt after it has became active. Value After Reset: 0x0

phy_int0

Description: PHY RXSENSE, PLL Lock, and HPD Interrupt Register

This register contains the interrupt indication of the PHY_STAT0 status interrupts. Interrupt generation is accomplished in the following way:

interrupt = (mask == 1'b0) && (polarity == status);

All these interrupts are forwarded to the Interrupt Handler sticky bit register ih_phy_stat0 and after ORed to a single main interrupt line to micro controller. Assertion of this interrupt implies that data related with the corresponding packet has been sent through the HDMI interface.

Size: 8 bits

Offset: 0x3005

Bits	Name	Attr	Description
7	RX_SENSE_3	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS CLK driver. Value After Reset: 0x0
6	RX_SENSE_2	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 2 driver. Value After Reset: 0x0
5	RX_SENSE_1	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 1 driver. Value After Reset: 0x0
4	RX_SENSE_0	R	Interrupt indication bit. TX PHY RX_SENSE indication interruption for TMDS channel 0 driver. Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R	Interrupt indication bit. HDMI Hot Plug Detect indication interrupt. Value After Reset: 0x0
0	TX_PHY_LOCK	R	Interrupt indication bit. TX PHY PLL lock indication interrupt. Value After Reset: 0x0

phy_mask0

Description: PHY RXSENSE, PLL Lock, and HPD Mask Register Mask register for generation of PHY_INT0 interrupts.

Size: 8 bits

Offset: 0x3006

Bits	Name	Attr	Description
7	RX_SENSE_3	R/W	Mask bit for PHY_INT0.RX_SENSE[3] interrupt bit Value After Reset: 0x0

6	RX_SENSE_2	R/W	Mask bit for PHY_INT0.RX_SENSE[2] interrupt bit Value After Reset: 0x0
5	RX_SENSE_1	R/W	Mask bit for PHY_INT0.RX_SENSE[1] interrupt bit Value After Reset: 0x0
4	RX_SENSE_0	R/W	Mask bit for PHY_INT0.RX_SENSE[0] interrupt bit Value After Reset: 0x0
3:2			Reserved for future use.
1	HPD	R/W	Mask bit for PHY_INT0.HPD interrupt bit Value After Reset: 0x0
0	TX_PHY_LOCK	R/W	Mask bit for PHY_INT0.TX_PHY_LOCK interrupt bit Value After Reset: 0x0

phy_pol0

Description: PHY RXSENSE, PLL Lock, and HPD Polarity Register Polarity register for generation of PHY_INT0 interrupts.

Size: 8 bits

Offset: 0x3007

Bits	Name	Attr	Description
7	RX_SENSE_3	R/W	Polarity bit for PHY_INT0.RX_SENSE[3] interrupt bit Value After Reset: 0x1
6	RX_SENSE_2	R/W	Polarity bit for PHY_INT0.RX_SENSE[2] interrupt bit Value After Reset: 0x1
5	RX_SENSE_1	R/W	Polarity bit for PHY_INT0.RX_SENSE[1] interrupt bit Value After Reset: 0x1
4	RX_SENSE_0	R/W	Polarity bit for PHY_INT0.RX_SENSE[0] interrupt bit Value After Reset: 0x1
3:2			Reserved for future use.
1	HPD	R/W	Polarity bit for PHY_INT0.HPD interrupt bit Value After Reset: 0x1
0	TX_PHY_LOCK	R/W	Polarity bit for PHY_INT0.TX_PHY_LOCK interrupt bit Value After Reset: 0x1

PHY_PCLFREQ0

Description: PHY Test Interface Register 0

Size: 8 bits

Offset: 0x3008

Bits	Name	Attr	Description
7:0	pclk_freq	R/W	Pixel Clock Frequency (pclk_freq[7:0]). Value After Reset: 0x32

PHY_PCLFREQ1

Description: PHY Test Interface Register 1

Size: 8 bits

Offset: 0x3009

Bits	Name	Attr	Description

7:2			Reserved for future use.
1:0	pclk_freq	R/W	Pixel Clock Frequency (pclk_freq[9:8]). Value After Reset: 0x0

PHY_PLLCFGFREQ0

Description: PHY PLL Test Interface Register 0

Size: 8 bits

Offset: 0x300a

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[7:0]). Value After Reset: 0x20

PHY_PLLCFGFREQ1

Description: PHY PLL Test Interface Register 1

Size: 8 bits

Offset: 0x300b

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[15:8]). Value After Reset: 0x27

PHY_PLLCFGFREQ2

Description: PHY PLL Test Interface Register 2

Size: 8 bits

Offset: 0x300c

Bits	Name	Attr	Description
7:0	pllcfgfreq	R/W	PLL Configuration Frequency (pllcfgfreq[23:16]). Value After Reset: 0x0

phy_i2cm_slave

Description: PHY I2C Slave Address Configuration Register

Size: 8 bits

Offset: 0x3020

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	slaveaddr	R/W	Slave address to be sent during read and write operations. PHY Gen2 slave address: 7'h69 HEAC PHY slave address: 7'h49 Value After Reset: 0x0

phy_i2cm_address

Description: PHY I2C Address Configuration Register

This register writes the address for read and write operations.

Size: 8 bits

Offset: 0x3021

Bits	Name	Attr	Description

7:0	address	R/W	Register address for read and write operations Value After Reset: 0x0

phy_i2cm_datao_1
Description: PHY I2C Data Write Register 1
Size: 8 bits
Offset: 0x3022

Bits	Name	Attr	Description
7:0	datao	R/W	Data MSB (datao[15:8]) to be written on register pointed by phy_i2cm_address [7:0]. Value After Reset: 0x0

phy_i2cm_datao_0
Description: PHY I2C Data Write Register 0
Size: 8 bits
Offset: 0x3023

Bits	Name	Attr	Description
7:0	datao	R/W	Data LSB (datao[7:0]) to be written on register pointed by phy_i2cm_address [7:0]. Value After Reset: 0x0

phy_i2cm_datai_1
Description: PHY I2C Data Read Register 1
Size: 8 bits
Offset: 0x3024

Bits	Name	Attr	Description
7:0	datai	R	Data MSB (datai[15:8]) read from register pointed by phy_i2cm_address[7:0]. Value After Reset: 0x0

phy_i2cm_datai_0
Description: PHY I2C Data Read Register 0
Size: 8 bits
Offset: 0x3025

Bits	Name	Attr	Description
7:0	datai	R	Data LSB (datai[7:0]) read from register pointed by phy_i2cm_address[7:0]. Value After Reset: 0x0

phy_i2cm_operation
Description: PHY I2C RD/RD_EXT/WR Operation Register
This register requests read and write operations from the I2C Master PHY. This register can only be written; reading this register always results in 00h. Writing 1'b1 simultaneously to read and write requests is considered a read request.
Size: 8 bits

Offset: 0x3026

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	wr	W	Write operation request Value After Reset: 0x0
3:1			Reserved for future use.
0	rd	W	Read operation request Value After Reset: 0x0

phy_i2cm_int

Description: PHY I2C Done Interrupt Register

This register contains and configures I2C master PHY done interrupt.

Size: 8 bits

Offset: 0x3027

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	done_pol	R/W	Done interrupt polarity configuration Value After Reset: 0x1
2	done_mask	R/W	Done interrupt mask signal Value After Reset: 0x0
1	done_interrupt	R	Operation done interrupt bit. Only lasts for 1 SFR clock cycle and is auto cleared after it. {done_interrupt = (done_mask==0b) && (done_status==done_pol)} Value After Reset: 0x0
0	done_status	R	Operation done status bit. Marks the end of a read or write operation. Value After Reset: 0x0

phy_i2cm_ctlint

Description: PHY I2C error Interrupt Register

This register contains and configures the I2C master PHY error interrupts.

Size: 8 bits

Offset: 0x3028

Bits	Name	Attr	Description
7	nack_pol	R/W	Not acknowledge error interrupt polarity configuration Value After Reset: 0x1
6	nack_mask	R/W	Not acknowledge error interrupt mask signal Value After Reset: 0x0
5	nack_interrupt	R	Not acknowledge error interrupt bit. Only lasts for one SFR clock cycle and is auto cleared after it. {nack_interrupt = (nack_mask==0b) && (nack_status==nack_pol)}. Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0
4	nack_status	R	Not acknowledge error status bit. Error on I2C not acknowledge. Note: This bit field is read by the sticky

Bits	Name	Attr	Description
			bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0
3	arbitration_pol	R/W	Arbitration error interrupt polarity configuration. Value After Reset: 0x1
2	arbitration_mask	R/W	Arbitration error interrupt mask signal. Value After Reset: 0x0
1	arbitration_interrupt	R	Arbitration error interrupt bit {arbitration_interrupt = (arbitration_mask==0b) && (arbitration_status==arbitration_pol)} Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0

Fields for Register: phy_i2cm_ctlint (Continued)

Bits	Name	Attr	Description
0	arbitration_status	R	Arbitration error status bit. Error on master I2C protocol arbitration. Only lasts for one SFR clock cycle and is auto cleared after it. Note: This bit field is read by the sticky bits present on the ih_i2cmphy_stat0 register. Value After Reset: 0x0

phy_i2cm_div

Description: PHY I2C Speed control Register

This register wets the I2C Master PHY to work in either Fast or Standard mode.

Size: 8 bits

Offset: 0x3029

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fast_std_mode	R/W	Sets the I2C Master to work in Fast Mode or Standard Mode: 1: Fast Mode 0: Standard Mode Value After Reset: 0x1
2:0	spare	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x3

phy_i2cm_softrstz

Description: PHY I2C SW reset control register

This register sets the I2C Master PHY software reset.

Size: 8 bits

Offset: 0x302a

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	i2c_softrstz	R/W	I2C Master Software Reset. Active by writing a zero and auto cleared to one in the following cycle.

Bits	Name	Attr	Description
			Value After Reset: 0x1

phy_i2cm_ss_scl_hcnt_1_addr

Description: PHY I2C Slow Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x302b

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt1	R/W	PHY I2C Slow Speed SCL High Level Control Register 1 Value After Reset: 0x0

phy_i2cm_ss_scl_hcnt_0_addr

Description: PHY I2C Slow Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x302c

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt0	R/W	PHY I2C Slow Speed SCL High Level Control Register 0 Value After Reset: 0x6c

phy_i2cm_ss_scl_lcnt_1_addr

Description: PHY I2C Slow Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x302d

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt1	R/W	PHY I2C Slow Speed SCL Low Level Control Register 1 Value After Reset: 0x0

phy_i2cm_ss_scl_lcnt_0_addr

Description: PHY I2C Slow Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x302e

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt0	R/W	PHY I2C Slow Speed SCL Low Level Control Register 0 Value After Reset: 0x7f

phy_i2cm_fs_scl_hcnt_1_addr

Description: PHY I2C Fast Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x302f

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt1	R/W	PHY I2C Fast Speed SCL High Level Control Register 1

			Value After Reset: 0x0

phy_i2cm_fs_scl_hcnt_0_addr
Description: PHY I2C Fast Speed SCL High Level Control Register 0
Size: 8 bits
Offset: 0x3030

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt0	R/W	PHY I2C Fast Speed SCL High Level Control Register 0 Value After Reset: 0x11

phy_i2cm_fs_scl_lcnt_1_addr
Description: PHY I2C Fast Speed SCL Low Level Control Register 1
Size: 8 bits
Offset: 0x3031

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt1	R/W	PHY I2C Fast Speed SCL Low Level Control Register 1 Value After Reset: 0x0

phy_i2cm_fs_scl_lcnt_0_addr
Description: PHY I2C Fast Speed SCL Low Level Control Register 0
Size: 8 bits
Offset: 0x3032

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt0	R/W	PHY I2C Fast Speed SCL Low Level Control Register 0 Value After Reset: 0x24

phy_i2cm_sda_hold
Description: PHY I2C SDA HOLD Control Register
Size: 8 bits
Offset: 0x3033

Bits	Name	Attr	Description
7:0	osda_hold	R/W	Defines the number of SFR clock cycles to meet tHD:DAT (300 ns) osda_hold = round_to_high_integer (300 ns / (1/ isfrclk_frequency)) Value After Reset: 0x9

jtag_phy_config
Description: PHY I2C/JTAG I/O Configuration Control Register
Size: 8 bits
Offset: 0x3034

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	i2c_jtagz	R/W	Configures the JTAG PHY interface output pin I2C_JTAGZ to select the PHY configuration interface

Bits	Name	Attr	Description
			when in internal control mode (iphy_ext_ctrl=1'b0) or ophyext_jtag_i2c_jtagz when PHY_EXTERNAL=1. 1'b0: JTAG configuration Interface 1'b1: I2C configuration Interface Value After Reset: 0x1
3:1			Reserved for future use.
0	jtag_trst_n	R/W	Configures the JTAG PHY interface output pin JTAG_TRST_N when in internal control mode (iphy_ext_ctrl=1'b0) or ophyext_jtag_trst_n when PHY_EXTERNAL=1. Value After Reset: 0x1

jtag_phy_tap_tck

Description: PHY JTAG Clock Control Register

Size: 8 bits

Offset: 0x3035

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	jtag_tck	R/W	Configures the JTAG PHY interface pin JTAG_TCK when in internal control mode (iphy_ext_ctrl=1'b0) or ophyext_jtag_tck when PHY_EXTERNAL=1. Value After Reset: 0x0

jtag_phy_tap_in

Description: PHY JTAG TAP In Control Register

Size: 8 bits

Offset: 0x3036

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	jtag_tms	R/W	Configures the JTAG PHY interface pin JTAG_TMS when in internal control mode (iphy_ext_ctrl=1'b0) or ophyext_jtag_tms when PHY_EXTERNAL=1. Value After Reset: 0x1
3:1			Reserved for future use.
0	jtag_tdi	R/W	Configures the JTAG PHY interface pin JTAG_TDI when in internal control mode (iphy_ext_ctrl=1'b0) or ophyext_jtag_tdi when PHY_EXTERNAL=1. Value After Reset: 0x0

jtag_phy_tap_out

Description: PHY JTAG TAP Out Control Register

Size: 8 bits

Offset: 0x3037

Bits	Name	Attr	Description
7:5			Reserved for future use.

Bits	Name	Attr	Description
4	jtag_tdo_en	R	Read JTAG PHY interface input pin JTAG_TDO_EN when in internal control mode (iphy_ext_ctrl=1'b0) or iphyext_jtag_tdo_en when PHY_EXTERNAL=1 Value After Reset: 0x0
3:1			Reserved for future use.
0	jtag_tdo	R	Read JTAG PHY interface input pin JTAG_TDO when in internal control mode (iphy_ext_ctrl=1'b0) or iphyext_jtag_tdo when PHY_EXTERNAL=1 Value After Reset: 0x0

jtag_phy_addr

Description: PHY JTAG Address Control Register

Size: 8 bits

Offset: 0x3038

Bits	Name	Attr	Description
7:0	jtag_addr	R/W	Configures the JTAG PHY interface pin JTAG_ADDR[7:0] when in internal control mode (iphy_ext_ctrl=1'b0) or iphyext_jtag_addr[7:0] when PHY_EXTERNAL=1 Value After Reset: 0x0

AudioSample Registers

Audio Sample Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: AudioSample

Register	Offset	Description
aud_conf0	0x3100	Audio I2S Software FIFO Reset, Select, and Enable Control Register 0 This register configures the...
aud_conf1	0x3101	Audio I2S Width Configuration Register 1 This register configures the data width of the input...
aud_int	0x3102	I2S FIFO status and interrupts. This register configures the I2S FIFO status and interrupts.
aud_conf2	0x3103	Audio I2S PCUV, NLPCM and HBR configuration Register 2 This register configures the I2S Audio
aud_int1	0x3104	I2S Mask Interrupt Register This register masks the interrupts present in the I2S module.

aud_conf0

Description: Audio I2S Software FIFO Reset, Select, and Enable Control Register 0

This register configures the I2S input enable that indicates which input I2S channels have valid data. It also allows the system processor to reset audio FIFOs upon underflow/overflow error detection.

Size: 8 bits

Offset: 0x3100

Bits	Name	Attr	Description
7	sw_audio_fifo_rst	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b. Note: If a FIFO reset request (via SFR command) lands in the middle of an I2S transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated I2S reset must be issued (writing 8'hF7 to MC_SWRSTZ register). Value After Reset: 0x0
6	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
5	i2s_select	R/W	1b: Selects I2S Audio Interface 0b: Selects the second (SPDIF/GPA) interface, in configurations with more that one audio interface (DOUBLE/GDOUBLE) Value After Reset: 0x1
4	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
3:0	I2S_in_en	R/W	Action I2S_in_en[0] - I2Sdata[0] enable I2S_in_en[1] - I2Sdata[1] enable I2S_in_en[2] - I2Sdata[2] enable I2S_in_en[3] - I2Sdata[3] enable Value After Reset: 0xf

aud_conf1

Description: Audio I2S Width Configuration Register 1 This register configures the data width of the input data.

Size: 8 bits

Offset: 0x3101

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	I2S_width	R/W	I2S input data width I2S_width[4:0] | Action 00000b-01111b | Not used 10000b | 16 bit data samples at input 10001b | 17 bit data samples at input 10010b | 18 bit data samples at input 10011b | 19 bit data samples at input 10100b | 20 bit data samples at input 10101b | 21 bit data samples at input 10110b | 22 bit data samples at input 10111b | 23 bit data samples at input 11000b | 24 bit data samples at input 11001b-11111b

			| Not Used Value After Reset: 0x18

aud_int

Description: I2S FIFO status and interrupts.

This register configures the I2S FIFO status and interrupts.

Size: 8 bits

Offset: 0x3102

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fifo_empty_mask	R/W	FIFO empty mask. Value After Reset: 0x0
2	fifo_full_mask	R/W	FIFO full mask. Value After Reset: 0x0
1:0			Reserved for future use.

aud_conf2

Description: Audio I2S PCUV, NLPCM and HBR configuration Register 2

This register configures the I2S Audio Data mapping. By default, audio data mapping is the standard I2S Linear PCM (L-PCM) mapping. You can choose to use the I2S interface to transport HBR or Non- Linear PCM (NL-PCM) audio, by setting the relevant bit in this register.

Size: 8 bits

Offset: 0x3103

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	insert_pcuv	R/W	When set (1'b1), this bit enables the insertion of the PCUV (Parity, Channel Status, User bit and Validity) bits on the incoming audio stream (support limited to Linear PCM audio). If disabled, the incoming audio stream must contain the PCUV bits, mapped according to Databook. Value After Reset: 0x1
1	NLPCM	R/W	I2S NLPCM Mode Enable. When enabled, this bit assumes that PCUV data is included on the I2S audio stream according to the description located in the "I2S Interface" section of Chapter 2, "Functional Description." Value After Reset: 0x0
0	HBR	R/W	I2S HBR Mode Enable. When enabled, the I2S audio stream is transmitted using HBR packets. Value After Reset: 0x0

aud_int1

Description: I2S Mask Interrupt Register

This register masks the interrupts present in the I2S module.

Size: 8 bits

Offset: 0x3104

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:0			Reserved for future use.

AudioPacketizer Registers

Audio Packetizer Registers. Follow the link for the register to see a detailed description of the register.

Registers for Address Block: AudioPacketizer

Register	Offset	Description
aud_n1	0x3200	Audio Clock Regenerator N Value Register 1 For N expected values, refer to the HDMI 1.4b...
aud_n2	0x3201	Audio Clock Regenerator N Value Register 2 For N expected values, refer to the HDMI 1.4b...
aud_n3	0x3202	Audio Clock Regenerator N Value Register 3 For N expected values, refer to the HDMI 1.4b...
aud_cts1	0x3203	Audio Clock Regenerator CTS Value Register 1 For CTS expected values, refer to the HDMI 1.4b...
aud_cts2	0x3204	Audio Clock Regenerator CTS Register 2 For CTS expected values, refer to the HDMI 1.4b...
aud_cts3	0x3205	Audio Clock Regenerator CTS value Register 3. For CTS expected values, refer to the HDMI 1.4b...
aud_inputclkfs	0x3206	Audio Input Clock FS Factor Register
aud_cts_dither	0x3207	Audio CTS Dither Register

aud_n1

Description: Audio Clock Regenerator N Value Register 1 For N expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3200

Bits	Name	Attr	Description
7:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_n2

Description: Audio Clock Regenerator N Value Register 2 For N expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3201

Bits	Name	Attr	Description
7:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_n3

Description: Audio Clock Regenerator N Value Register 3 For N expected values, refer to the HDMI 1.4b specification.
Size: 8 bits
Offset: 0x3202

Bits	Name	Attr	Description
7	ncts_atomic_write	R/W	When set, the new N and CTS values are only used when aud_n1 register is written. If clear, N and CTS data is updated each time a new N or CTS byte is written. The following write sequence is recommended: aud_n3 (set bit ncts_atomic_write if desired) aud_cts3 (set CTS_manual and CTS value if desired/enabled) aud_cts2 (required in CTS_manual) aud_cts1 (required in CTS_manual) aud_n3 (bit ncts_atomic_write with same value as in step 1.) aud_n2 aud_n1 For dynamic N/CTS changes, perform only steps from 2-7 or 5-7 depending on the state of CTS_manual. Value After Reset: 0x0
6:4			Reserved for future use.
3:0	AudN	R/W	HDMI Audio Clock Regenerator N value Value After Reset: 0x0

aud_cts1
Description: Audio Clock Regenerator CTS Value Register 1 For CTS expected values, refer to the HDMI 1.4b specification.
Size: 8 bits
Offset: 0x3203

Bits	Name	Attr	Description
7:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism. Value After Reset: 0x0

aud_cts2
Description: Audio Clock Regenerator CTS Register 2
For CTS expected values, refer to the HDMI 1.4b specification.
Size: 8 bits
Offset: 0x3204

Bits	Name	Attr	Description
7:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual

			(AUD_CTS3) mechanism. Value After Reset: 0x0

aud_cts3

Description: Audio Clock Regenerator CTS value Register 3. For CTS expected values, refer to the HDMI 1.4b specification.

Size: 8 bits

Offset: 0x3205

Bits	Name	Attr	Description
7:5	Spare_bits	R/W	Reserved as "spare" bits with no associated functionality. Value After Reset: 0x0
4	CTS_manual	R/W	If the CTS_manual bit equals 0b, this registers contains audCTS[19:0] generated by the Cycle time counter according to the specified timing. If the CTS_manual bit equals 1b, this register is configured with the audCTS[7:0] value that is output by the Audio Packetizer. Note: When the General Parallel Audio Interface (GPAUD) is enabled (AUDIO_IF = 6) or the AHB DMA Audio Interface is enabled (AUDIO_IF = 8), writing to these bits has no effect; reading these bits always return 0. Value After Reset: 0x0
3:0	AudCTS	R/W	HDMI Audio Clock Regenerator CTS calculated value. This value can be manually set using the CTS_manual (AUD_CTS3) mechanism. Value After Reset: 0x0

aud_inputclkfs

Description: Audio Input Clock FS Factor Register

Size: 8 bits

Offset: 0x3206

Bits	Name	Attr	Description
7:3			Reserved for future use.
2:0	ifsfactor	R/W	Fs factor configuration: ifsfactor[2:0] | Audio Clock | Action 0 | 128xFs | If you select the Bypass SPDIF DRU unit in coreConsultant, the input audio clock (either I2S or SPDIF according to configuration) is used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. | 256xFs | The input audio clock (I2S only) is divided by 2 and then used at audio packetizer to calculate the CTS value and ACR packet insertion rate. | 512xFs | The input audio clock (either I2S or

Bits	Name	Attr	Description
			SPDIF according to configuration) used divided by 4 and then used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. Note: When the SPDIF interface is receiving an HBR audio stream ("Support for HBR over SDPIF" parameter must be enabled), it is required that the selected IFSFACTOR to be set at 512xFs in order to comply with the HDMI ACR requirements for HBR audio streams. | Reserved | 64xFs | The input audio clock (I2S only) is multiplied by 2 and then used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. others | 128xFs | If you select the Bypass SPDIF DRU unit in coreConsultant, the input audio clock (either I2S or SPDIF according to configuration) is used at the audio packetizer to calculate the CTS value and ACR packet insertion rate. The SPDIF interface, for non HBR audio, requires that the configured oversampling value to be 128xFs when HTX_SPDIFBYPDRU is enabled and 512xFs if not. When the SPDIF interface is receiving HBR audio (HBR_ON_SPDIF must be enabled), in order to comply with the HDMI ACR requirements for HBR audio streams. Value After Reset: 0x0

aud_cts_dither

Description: Audio CTS Dither Register

Size: 8 bits

Offset: 0x3207

Bits	Name	Attr	Description
7:4	divisor	R/W	Dither divisor (4'd1 if no CTS Dither). This field should be configured with the value of divisor from the HDMI specification. Value After Reset: 0x1
3:0	dividend	R/W	Dither dividend (4'd1 if no CTS Dither). This field should be configured with the value of dividend from the HDMI specification. Value After Reset: 0x1

AudioSampleSPDIF Registers

Audio Sample SPDIF Registers. Follow the link for the register to see a detailed description

of the register.

Registers for Address Block: AudioSampleSPDIF

Register	Offset	Description
aud_spdif0	0x3300	Audio SPDIF Software FIFO Reset Control Register 0 This register allows the system processor to...
aud_spdif1	0x3301	Audio SPDIF NLPCM and Width Configuration Register 1 This register configures the SPDIF data...
aud_spdifint	0x3302	Audio SPDIF FIFO Empty/Full Mask Register
aud_spdifint1	0x3303	Audio SPDIF Mask Interrupt Register 1 This register masks interrupts present in the SPDIF...
aud_spdif2	0x3304	Audio SPDIF Enable Confiiguration Register 2 This register configures the SPDIF input enable that...

aud_spdif0

Description: Audio SPDIF Software FIFO Reset Control Register 0

This register allows the system processor to reset audio FIFOs upon underflow/overflow error detection.

Size: 8 bits

Offset: 0x3300

Bits	Name	Attr	Description
7	sw_audio_fifo_rst	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b. Note: If a FIFO reset request (via register write command) lands in the middle of an SPDIF audio transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated SPDIF reset must be issued (writing 8'hEF to MC_SWRSTZ register). Value After Reset: 0x0
6:0	spare	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0xf

aud_spdif1

Description: Audio SPDIF NLPCM and Width Configuration Register 1 This register configures the SPDIF data width.

Size: 8 bits

Offset: 0x3301

Bits	Name	Attr	Description
7	setnlpcm	R/W	Select Non-Linear (1b) / Linear (0b) PCM mode Value After Reset: 0x0
6	spdif_hbr_mode	R/W	When set to 1'b1, this bit field indicates that the input stream has a High Bit Rate (HBR) to be transmitted in HDMI HBR packets. When clear (1b'0), the audio is

			transmitted in HDMI AUDS packets.Note:< Otherwise, this field is a "spare" bit with no associated functionality.

aud_spdifint

Description: Audio SPDIF FIFO Empty/Full Mask Register

Size: 8 bits

Offset: 0x3302

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	spdif_fifo_empty_mask	R/W	Description: SPDIF FIFO empty mask Value After Reset: 0x0
2	spdif_fifo_full_mask	R/W	Description: SPDIF FIFO full mask Value After Reset: 0x0
1:0			Reserved for future use.

aud_spdifint1

Description: Audio SPDIF Mask Interrupt Register 1

This register masks interrupts present in the SPDIF module.

Size: 8 bits

Offset: 0x3303

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:0			Reserved for future use.

aud_spdif2

Description: Audio SPDIF Enable Confiiguration Register 2

This register configures the SPDIF input enable that indicates which input SPDIF channels have valid data.

Size: 8 bits

Offset: 0x3304

Bits	Name	Attr	Description
7:4			Reserved for future use.
3:0	SPDIF_in_en	R/W	Action SPDIF_in_en[0] - ispdifdata[0] enable SPDIF_in_en[1] - ispdifdata[1] enable SPDIF_in_en[2] - ispdifdata[2] enable SPDIF_in_en[3] - ispdifdata[3] enable Value After Reset: 0x1

AudioSampleGP Registers

Audio Sample GP Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
gp_conf0	0x3500	Audio GPA Software FIFO Reset Control Register 0
gp_conf1	0x3501	Audio GPA Channel Enable Configuration Register 1

gp_conf2	0x3502	Audio GPA HBR Enable Register 2
gp_mask	0x3506	Audio GPA FIFO Full and Empty Mask Interrupt Register

gp_conf0

Description: Audio GPA Software FIFO Reset Control Register 0

Size: 8 bits

Offset: 0x3500

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	sw_audio_fifo_rst	R/W	Audio FIFOs software reset Writing 0b: no action taken Writing 1b: Resets all audio FIFOs Reading from this register always returns 0b. Note: If a FIFO reset request (via register write command) lands in the middle of an GPAUD audio transaction, the samples become misaligned (left-right sequence lost). As a solution, for each FIFO reset, an associated SPDIF reset must be issued (writing 8'h7F to MC_SWRSTZ register). Value After Reset: 0x0

gp_conf1

Description: Audio GPA Channel Enable Configuration Register 1

Size: 8 bits

Offset: 0x3501

Bits	Name	Attr	Description
7:0	ch_in_en	R/W	Each bit controls the enabling of the respective audio channel. For instance, bit 1, when set (1'b1), the audio Channel 1 is enabled. When cleared, the referred channel is disabled. Value After Reset: 0x0

gp_conf2

Description: Audio GPA HBR Enable Register 2

Size: 8 bits

Offset: 0x3502

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	insert_pcuv	R/W	When set (1'b1), this bit enables the insertion of the PCUV (Parity, Channel Status, User bit and Validity) bits on the incoming audio stream (support limited to Linear PCM audio). If disabled, the incoming audio stream must contain the PCUV bits, mapped according to 2.6.4.2 Data Mapping Examples.

			Value After Reset: 0x0
0	HBR	R/W	HBR packets enable. The Hdmi_tx sends the HBR packets. This bit is enabled when the audio frequency is higher than 192 kHz. If this bit is enabled, the number of channels configured in GP_CONF1 must be set to 8'hFF. Value After Reset: 0x0

gp_mask

Description: Audio GPA FIFO Full and Empty Mask Interrupt Register

Size: 8 bits

Offset: 0x3506

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	fifo_overrun_mask	R/W	FIFO overrun mask Value After Reset: 0x1
3:2			Reserved for future use.
1	fifo_empty_mask	R/W	FIFO empty flag mask Value After Reset: 0x0
0	fifo_full_mask	R/W	FIFO full flag mask Value After Reset: 0x0

AudioDMA Registers

Audio DMA Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
ahb_dma_conf0	0x3600	Audio DMA SW FIFO reset and DMA Configuration Register 0 This register contains the software reset...
ahb_dma_start	0x3601	Audio DMA Start Register The start_dma_transaction bit field signals the AHB audio DMA to start...
ahb_dma_stop	0x3602	Audio DMA Stop Register The stop_dma_transaction bit field signals the AHB audio DMA to stop current...
ahb_dma_thrsld	0x3603	Audio DMA FIFO Threshold Register This register defines the FIFO medium threshold occupation value....
ahb_dma_straddr_set0[0:3]	0x3604 + (i * 0x1)	Audio DMA Start Address Set0 Register Array Address offset: i = 0 to 3 These registers define...
ahb_dma_stpaddr_set0[0:3]	0x3608 + (i * 0x1)	Audio DMA Stop Address Set0 Register Array Address offset: i = 0 to 3 This registers define the...
ahb_dma_bstraddr[0:3]	0x360c + (i * 0x1)	Audio DMA Burst Start Address Register Array Address offset: i = 0 to 3 These read-only registers...
ahb_dma_mblength0	0x3610	Audio DMA Burst Length Register 0 This registers holds the length of the current burst operation....
ahb_dma_mblength	0x3611	Audio DMA Burst Length Register 1 This registers holds

Register	Offset	Description
		the length of the current burst operation....
ahb_dma_mask	0x3614	Audio DMA Mask Interrupt Register This register masks each of the interrupts present in the AHB...
ahb_dma_conf	0x3616	Audio DMA Channel Enable Configuration Register 1 In AUDS packet configuration with layout 0 selected,...
ahb_dma_buffmask	0x3619	Audio DMA Buffer Mask Interrupt Register
ahb_dma_mask1	0x361b	Audio DMA Mask Interrupt Register 1 This register masks interrupts present in the AHB audio DMA...
ahb_dma_status	0x361c	Audio DMA Status
ahb_dma_conf2	0x361d	Audio DMA Configuration Register 2
ahb_dma_straddr_set1[0:3]	0x3620 + (i * 0x1)	Audio DMA Start Address Set 1 Register Array Address offset: i = 0 to 3 These registers define...
ahb_dma_stpaddr_set1[0:3]	0x3624 + (i * 0x1)	Audio DMA Stop Address Set 1 Register Array Address offset: i = 0 to 3 These registers define...

ahb_dma_conf0

Description: Audio DMA SW FIFO reset and DMA Configuration Register 0

This register contains the software reset bit for the audio FIFOs. It also configures operating modes of the AHB master.

Size: 8 bits

Offset: 0x3600

Bits	Name	Attr	Description
7	sw_fifo_rst	R/W	This is the software reset bit for the audio and FIFO clear. Writing 0'b does not result in any action. Writing 1'b to this register resets all audio FIFOs. Reading from this register always returns 0'b. Value After Reset: 0x0
6	insert_pcuv	R/W	Enables the insertion of PCUV data Value After Reset: 0x0
5			Reserved for future use.
4	hbr	R/W	HBR packet enable The Hdmi_tx sends the HBR packets. This bit must be enabled when transmitting non-linear audio of frequency higher than 192 kHz. If this bit is enabled, the number of channels configured in AHB_DMA_CONF1 is always 8. Value After Reset: 0x0
3	enable_hlock	R/W	Enable request of locked burst AHB mechanism. 1'b: Enables the usage of hlock for master request to arbiter of a locked complete burst. 0'b: Disables request of locked burst AHB mechanism Value After Reset: 0x0
2:1	incr_type	R/W	Selects the preferred burst length size

			00'b: Corresponds to INCR4 fixed four beat, incremental AHB burst mode. Only valid when burst_mode is high. 01'b: Corresponds to INCR8 fixed eight beat incremental AHB burst mode. Only valid when burst_mode is high. 10'b: Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high. 11'b: Corresponds to INCR16 fixed 16 beat incremental AHB burst mode. Only valid when burst_mode is high. Value After Reset: 0x0
0	burst_mode	R/W	1'b: Forces the burst mode to be fixed beat, incremental burst mode designated by the incr_type[1:0] signal. 0'b: Normal operation is unspecified length, incremental burst. It corresponds to INCR AHB burst mode. Value After Reset: 0x0

ahb_dma_start

Description: Audio DMA Start Register

The start_dma_transaction bit field signals the AHB audio DMA to start accessing system memory in order to fetch data samples to store in the FIFO. After the operation starts, a new request for a DMA start is ignored until the DMA is stopped or it reaches the end address. Only in one of these situations is a new start request acknowledged.

The first DMA burst request after start_dma_transaction configuration uses initial_addr[31:0] as ohaddr[31:0] value; mburstlength[8:0] is set to the maximum admissible value. This maximum value is constrained by the size of buffer provided, the instantiated FIFO depth, or/and the number of words up to the next 1 Kbyte boundary.

Size: 8 bits

Offset: 0x3601

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	start_dma_transaction	R/W	Start DMA transaction This register is auto-cleared when the transfer operation is completed (done). Value After Reset: 0x0

ahb_dma_stop

Description: Audio DMA Stop Register

The stop_dma_transaction bit field signals the AHB audio DMA to stop current Attr. After it stops, if a new start DMA operation is requested, the DMA engine restarts the Attr using the initial_addr[31:0], which is programmed at ahb_dma_straddr0 to ahb_dma_straddr3.

Size: 8 bits

Offset: 0x3602

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	stop_dma_transaction	R/W	Stop DMA transaction This register is auto-cleared when the transfer operation is stopped (done).

			Value After Reset: 0x0

ahb_dma_thrsld

Description: Audio DMA FIFO Threshold Register

This register defines the FIFO medium threshold occupation value.

After the AHB master completes a burst transaction successfully, the FIFO may remain full till the data fetch interface requests samples. Each data fetch operation reduces the number of samples stored in the FIFO by the number of channels enabled.

Therefore, the fifo_threshold[7:0] is the medium number of samples that should be available in the audio FIFO across the DMA operation.

As soon as the number of samples in the FIFO drops lower than the fifo_threshold[7:0], the DMA engine requests a new burst of samples for the AHB master. The length is constrained by the size of buffer provided, the instantiated FIFO depth minus fifo_threshold[7:0], and/or the number of words up to the next 1 kbyte boundary.

Size: 8 bits

Offset: 0x3603

Bits	Name	Attr	Description
7:0	fifo_threshold	R/W	FIFO medium threshold occupation value Value After Reset: 0x0

ahb_dma_straddr_set0[0:3]

Description: Audio DMA Start Address Set0 Register Array Address offset: i = 0 to 3

These registers define the initial_addr[31:0] used to initiate the DMA burst read transactions upon start_dma_transaction configuration.

Size: 8 bits

Offset: 0x3604 + (i * 0x1)

Bits	Name	Attr	Description
7:0	initial_addr	R/W	Defines init_addr[7:0] to initiate DMA burst transactions Value After Reset: 0x0

ahb_dma_stpaddr_set0[0:3]

Description: Audio DMA Stop Address Set0 Register Array Address offset: i = 0 to 3

This registers define the final_addr[31:0] used as the final point to the DMA burst read transactions.

Upon start_dma_transaction configuration, the DMA engine starts requesting burst reads from the external system memory. Each burst read can have a maximum theoretical length of 256 words (due to the AMBA AHB specification 1 Kbyte boundary burst limitation).

The DMA engine is responsible for incrementing the burst starting address and defining its corresponding burst length to reach the final_addr[31:0] address. The last burst request issued by the DMA engine takes into account that it should only request data until the final_addr[31:0] address (included) and for that should calculate the correct burst length.

After reaching the final_addr[31:0] address, the done interrupt is active to signal completion of DMA operation.

Size: 8 bits

Offset: 0x3608 + (i * 0x1)

Bits	Name	Attr	Description

7:0	final_addr	R/W	Defines final_addr[7:0] to end DMA burst transactions Value After Reset: 0x0

ahb_dma_bstraddr[0:3]

Description: Audio DMA Burst Start Address Register Array Address offset: i = 0 to 3

These read-only registers compose the start address of the current burst operation.

burst_start_addr[31:0] = haddr[31:0] = initial_addr[31:0] + 16.

Size: 8 bits

Offset: 0x360c + (i * 0x1)

Bits	Name	Attr	Description
7:0	burst_addr	R	Start address for the current burst operation Value After Reset: 0x0

ahb_dma_mblength0

Description: Audio DMA Burst Length Register 0

This registers holds the length of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA is a length of 8, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 32.

Size: 8 bits

Offset: 0x3610

Bits	Name	Attr	Description
7:0	mburstlength	R	Requested burst length (mburstlength[7:0]) Value After Reset: 0x0

ahb_dma_mblength1

Description: Audio DMA Burst Length Register 1

This registers holds the length of the current burst operation. As an example, if the first burst transaction of the AHB audio DMA is a length of 8, then the second burst should start at address ohaddr[31:0] = initial_addr[31:0] + 32.

Size: 8 bits

Offset: 0x3611

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	mburstlength	R	Requested burst length Value After Reset: 0x0

ahb_dma_mask

Description: Audio DMA Mask Interrupt Register

This register masks each of the interrupts present in the AHB audio DMA module.

Size: 8 bits

Offset: 0x3614

Bits	Name	Attr	Description
7	done_mask	R/W	DMA end of operation interrupt mask. Active when DMA engine reaches final_addr[15:0] or when stop DMA operation is activated. Value After Reset: 0x1
6	retrysplit_mask	R/W	Retry/split interrupt mask. Active when AHB master receives a RETRY or SPLIT response from slave.

			Value After Reset: 0x1
5	lostownership_mask	R/W	Master lost ownership interrupt mask when in burst transfer. Active when AHB master loses BUS ownership within the course of a burst transfer. Value After Reset: 0x1
4	error_mask	R/W	Error interrupt mask. Active when slave indicates error through the isresp[1:0]. Value After Reset: 0x1
3			Reserved for future use.
2	fifo_thrempty_mask	R/W	Audio FIFO empty interrupt mask when audio FIFO has less than the number of enabled audio channels. Value After Reset: 0x1
1	fifo_full_mask	R/W	Audio FIFO full interrupt mask. Value After Reset: 0x1
0	fifo_empty_mask	R/W	Audio FIFO empty interrupt mask. Value After Reset: 0x1

ahb_dma_conf1

Description: Audio DMA Channel Enable Configuration Register 1

In AUDS packet configuration with layout 0 selected, the maximum number of active channels is 2.

Size: 8 bits

Offset: 0x3616

Bits	Name	Attr	Description
7:0	ch_in_en	R/W	Each bit controls the enabling of the respective audio channel. For instance, when bit 1 is set (1'b1) the audio Channel 1 is enabled. When cleared, the referred channel is disabled. Value After Reset: 0x0

ahb_dma_buffmask

Description: Audio DMA Buffer Mask Interrupt Register

Size: 8 bits

Offset: 0x3619

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	mask_fifo_overrun	R/W	Buffer overrun flag mask Value After Reset: 0x1
3:2			Reserved for future use.
1	mask_buff_full	R/W	Buffer full flag mask Value After Reset: 0x1
0	mask_buff_empty	R/W	Buffer empty flag mask Value After Reset: 0x1

ahb_dma_mask1

Description: Audio DMA Mask Interrupt Register 1

This register masks interrupts present in the AHB audio DMA module.

Size: 8 bits

Offset: 0x361b

Bits	Name	Attr	Description

7:2			Reserved for future use.
1	fifo_underrun_mask	R/W	AHB DMA FIFO underrun mask Value After Reset: 0x1
0	fifo_overrun_mask	R/W	AHB DMA FIFO overrun mask Value After Reset: 0x1

ahb_dma_status

Description: Audio DMA Status

Size: 8 bits

Offset: 0x361c

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	autostart_status	R	Indicates the set of start and stop addresses currently used by the AHB audio DMA. If cleared (1'b0), the start and stop addresses configured in the address range 0x3604 to 0x360B are being used. When set (1'b1), the configurations at address range 0x3620 to 0x3627 are being used. This bit is always at zero when autostart_enable is cleared (1'b0). Value After Reset: 0x0

ahb_dma_conf2

Description: Audio DMA Configuration Register 2

Size: 8 bits

Offset: 0x361d

Bits	Name	Attr	Description
7:2			Reserved for future use.
1	autostart_loop	R/W	Enables the AHB audio DMA auto-start loop mode Value After Reset: 0x1
0	autostart_enable	R/W	Enables the AHB audio DMA auto-start feature Value After Reset: 0x0

ahb_dma_straddr_set1[0:3]

Description: Audio DMA Start Address Set 1 Register Array Address offset: i = 0 to 3

These registers define the initial_addr_1[31:0] used to initiate the DMA burst read transactions upon start_dma_transaction configuration.

Size: 8 bits

Offset: 0x3620 + (i * 0x1)

Bits	Name	Attr	Description
7:0	initial_addr_1	R/W	Defines init_addr_1[7:0] to initiate DMA burst transactions Value After Reset: 0x0

ahb_dma_stpaddr_set1[0:3]

Description: Audio DMA Stop Address Set 1 Register Array Address offset: i = 0 to 3

These registers define the final_addr_1[31:0] used as the final point to the DMA burst read

transactions. Upon start_dma_transaction configuration, the DMA engine starts requesting burst reads from the external system memory. Each burst read can have a maximum theoretical length of 256 words (due to the AMBA AHB specification 1 Kbyte boundary burst limitation).
The DMA engine is responsible for incrementing the burst starting address and defining its corresponding burst length to reach the final_addr[31:0] address. The last burst request issued by the DMA engine takes into account that it should only request data until the final_addr[31:0] address (included) and for that should calculate the correct burst length. After reaching the final_addr_1[31:0] address, the done interrupt is active to indicate completion of the DMA operation.
Size: 8 bits
Offset: 0x3624 + (i * 0x1)

Bits	Name	Attr	Description
7:0	final_addr_1	R/W	Defines final_addr_1[7:0] to end DMA burst transactions Value After Reset: 0x0

MainController Registers
Main Controller Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
mc_clkdis	0x4001	Main Controller Synchronous Clock Domain Disable Register
mc_swrstzreq	0x4002	Main Controller Software Reset Register Main controller software reset request per clock domain....
mc_opctrl	0x4003	Main Controller HDCP Bypass Control Register
mc_flowctrl	0x4004	Main Controller Feed Through Control Register
mc_phyrstz	0x4005	Main Controller PHY Reset Register
mc_lockonclock	0x4006	Main Controller Clock Present Register
mc_heacphy_rst	0x4007	Main Controller HEAC PHY Reset Register
mc_lockonclock_2	0x4009	Main Controller Clock Present Register 2
mc_swrstzreq_2	0x400a	Main Controller Software Reset Register 2 Main controller software reset request per clock domain....
mc_opsts	0x4010	Main Controller Status Register This register contains the information regarding the status of...
base_sfrdivlow	0x4018	SFR Clock Base Time Register Low
base_sfrdivhigh	0x4019	SFR Clock Base Time Register High

mc_clkdis
Description: Main Controller Synchronous Clock Domain Disable Register
Size: 8 bits
Offset: 0x4001

Bits	Name	Attr	Description
7	h22sclk_disable	R/W	HDCP22 clock synchronous disable signal. When active (1b), simultaneously bypasses HDCP22. Value After Reset: 0x0
6	hdcpclk_disable	R/W	HDCP clock synchronous disable signal. When active

Bits	Name	Attr	Description
			(1b), simultaneously bypasses HDCP. Value After Reset: 0x0
5	cecclk_disable	R/W	CEC Engine clock synchronous disable signal. Value After Reset: 0x0
4	cscclk_disable	R/W	Color Space Converter clock synchronous disable signal. Value After Reset: 0x0
3	audclk_disable	R/W	Audio Sampler clock synchronous disable signal. Value After Reset: 0x0
2	prepclk_disable	R/W	Pixel Repetition clock synchronous disable signal. Value After Reset: 0x0
1	tmdsclk_disable	R/W	TMDS clock synchronous disable signal. It is required to perform a write action on one of the following registers: fc_invidconf, fc_inhactiv0, fc_inhactiv1, fc_inhblank0, fc_inhblank1, fc_invactiv0 fc_invactiv1, fc_invblank, fc_hsyncindelay0, fc_hsyncindelay1, fc_hsyncinwidth0 fc_hsyncinwidth1, fc_vsyncindelay, fc_vsyncinwidth, fc_ctrldur, fc_exctrldur, fc_exctrlspac Value After Reset: 0x0
0	pixelclk_disable	R/W	Pixel clock synchronous disable signal. Value After Reset: 0x0

mc_swrstzreq

Description: Main Controller Software Reset Register

Main controller software reset request per clock domain. Writing zero to a bit of this register results in an NRZ signal toggle at sfrclk rate to an output signal that indicates a software reset request. This toggle must be used to generate a synchronized reset to de corresponding domain, with at least 1 clock cycle.

Size: 8 bits

Offset: 0x4002

Bits	Name	Attr	Description
7	igpaswrst_req	R/W	GPAUD interface soft reset request. This bit is enabled when the Generic Parallel Audio (GPAUD) interface is enabled (AUDIO_IF = 6). Otherwise, this bit returns zero. Value After Reset: 0x1
6	cecswrst_req	R/W	CEC software reset request. Defaults back to 1b after reset request. Note: After you configure cecswrst_req, set the value of the bit csc_clk_disable of the register mc_clkdis to 1, 0, and then 1 again. Value After Reset: 0x1
5			Reserved for future use.
4	ispdifswrst_req	R/W	SPDIF audio software reset request.

			Value After Reset: 0x1
3	ii2sswrst_req	R/W	I2S audio software reset request. Value After Reset: 0x1
2	prepswrst_req	R/W	Pixel Repetition software reset request. Value After Reset: 0x1
1	tmdsswrst_req	R/W	TMDS software reset request. It is required to perform a write action on one of the following registers: fc_invidconf, fc_inhactiv0, fc_inhactiv1, fc_inhblank0, fc_inhblank1, fc_invactiv0 fc_invactiv1, fc_invblank, fc_hsyncindelay0, fc_hsyncindelay1, fc_hsyncinwidth0 fc_hsyncinwidth1, fc_vsyncindelay, fc_vsyncinwidth, fc_ctrldur, fc_exctrldur, fc_exctrlspac Value After Reset: 0x1
0	pixelswrst_req	R/W	Pixel software reset request. Value After Reset: 0x1

mc_opctrl

Description: Main Controller HDCP Bypass Control Register

Size: 8 bits

Offset: 0x4003

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	h22s_ovr_val	R/W	HDCP SNPS 2.2 versus 1.4 switch override value 1'b0: The switch is routed to HDCP 1.4 signals when hdcp22snps_switch_lock is not set to 1'b1. 1'b1: The switch is routed to HDCP 2.2 SNPS signals when hdcp22snps_switch_lock is not set to 1'b1. Value After Reset: 0x1
4	h22s_switch_lck	R/W	HDCP 2.2 SNPS switch lock 1'b0: Enables you to change the direction of the HDCP 2.2 SNPS versus 1.4 switch by using the hdcp22snps_ovr_val. 1'b1: You can still write to hdcp22snps_ovr_val but has no effect over the HDCP 2.2 SNPS versus 1.4 switch, that keeps as it was configured by hdcp22snps_ovr_val at the time the 1'b1 was written to this bit field. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Value After Reset: 0x0
3:1			Reserved for future use.
0	hdcp_block_byp	R/W	Block HDCP bypass mechanism 1'b0: This is the default value. You can write to the hdcp_clkdisable bit of the register mc_clkdis and bypass

Bits	Name	Attr	Description
			HDCP by acting on the register mc_clkdis bit 6 (hdcp_clkdisable) 1'b1: You can still write to the hdcp_clkdisable bit of the register mc_clkdis but this action disables the HDCP module and blocks the bypass mechanism. The output data is frozen and the HDMI Tx and RX fail authentication. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0

mc_flowctrl

Description: Main Controller Feed Through Control Register

Size: 8 bits

Offset: 0x4004

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	Feed_through_off	R/W	Video path Feed Through enable bit: 1b: Color Space Converter is in the video data path. 0b: Color Space Converter is bypassed (not in the video data path). Value After Reset: 0x0

mc_phyrstz

Description: Main Controller PHY Reset Register

Size: 8 bits

Offset: 0x4005

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	phyrstz	R/W	HDMI Source PHY active low reset control for PHY GEN1, active high reset control for PHY GEN2. Value After Reset: "(PHY_GEN2== 1) ? 1 : 0"

mc_lockonclock

Description: Main Controller Clock Present Register

Size: 8 bits

Offset: 0x4006

Bits	Name	Attr	Description
7	igpaclk	R/W1C	GPAUD interface clock status. This bit is enabled when the Generic Parallel Audio (GPAUD) interface is enabled (AUDIO_IF = 6). Otherwise, this bit returns zero. This bit indicates the clock is present in the system. It is cleared by writing 1 to this bit.

			Value After Reset: 0x0
6	pclk	R/W1C	Pixel clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
5	tclk	R/W1C	TMDS clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
4	prepclk	R/W1C	Pixel Repetition clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
3	i2sclk	R/W1C	I2S clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
2	audiospdifclk	R/W1C	SPDIF clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0
1			Reserved for future use.
0	cecclk	R/W1C	CEC clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0

mc_heacphy_rst

Description: Main Controller HEAC PHY Reset Register

Size: 8 bits

Offset: 0x4007

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	heacphyrst	R/W	HEAC PHY reset (active high) Value After Reset: 0x1

mc_lockonclock_2

Description: Main Controller Clock Present Register 2

Size: 8 bits

Offset: 0x4009

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	ahbdmaclk	R/W1C	AHB audio DMA clock status. Indicates that the clock is present in the system. Cleared by WR 1 to this position. Value After Reset: 0x0

mc_swrstzreq_2

Description: Main Controller Software Reset Register 2

Main controller software reset request per clock domain. Writing zero to a bit of this register results in a signal toggle that indicates a software reset request. This toggle is used to generate a synchronized reset to the corresponding domain, with one or more clock cycles.

Size: 8 bits

Offset: 0x400a

Bits	Name	Attr	Description

7:1			Reserved for future use.
0	ahbdmaswrst_req	R/W	AHB audio DMA software reset request. Writing 1'b1 does not result in any action. Writing 1'b0 to this register resets all AHB audio logic. Value After Reset: 0x0

mc_opsts

Description: Main Controller Status Register

This register contains the information regarding the status of the HDCP SNPS 2.2 versus 1.4 switch.

Size: 8 bits

Offset: 0x4010

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	h22s_switch_sts	R	HDCP SNPS 2.2 versus 1.4 switch value status. 1'b0: HDCP 1.4 selected 1'b1: HDCP 2.2 selected Value After Reset: 0x1

base_sfrdivlow

Description: SFR Clock Base Time Register Low

Size: 8 bits

Offset: 0x4018

Bits	Name	Attr	Description
7:0	base_sfrdiv_lo	R/W	SFR clock divider Low This register must be configured with the 8 least-significant bits of the value sfrclk frequency divided by 1000 (for example, for 27 MHz base_sfrdiv[14:0] = 27027). The configured data is used to generate a reference pulse of 1ms period that is needed by several timers within the controller. Value After Reset: 0x93

base_sfrdivhigh

Description: SFR Clock Base Time Register High

Size: 8 bits

Offset: 0x4019

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	base_sfrdiv_hi	R/W	SFR clock divider High This register must be configured with the 7 most-significant bits of the value sfrclk frequency divided by 1000 (for example, for 27 MHz base_sfrdiv[14:0] = 27027). The configured data is used to generate a reference pulse of 1ms period that is needed by several timers within the controller. Value After Reset: 0x69

ColorSpaceConverter Registers

Color Space Converter Registers Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
csc_cfg	0x4100	Color Space Converter Interpolation and Decimation Configuration Register
csc_scale	0x4101	Color Space Converter Scale and Deep Color Configuration Register
csc_coef_a1_msb	0x4102	Color Space Converter Matrix A1 Coefficient Register MSB Notes: - The coefficients used in the...
csc_coef_a1_lsb	0x4103	Color Space Converter Matrix A1 Coefficient Register LSB Notes: - The coefficients used in the...
csc_coef_a2_msb	0x4104	Color Space Converter Matrix A2 Coefficient Register MSB Color Space Conversion A2...
csc_coef_a2_lsb	0x4105	Color Space Converter Matrix A2 Coefficient Register LSB Color Space Conversion A2...
csc_coef_a3_msb	0x4106	Color Space Converter Matrix A3 Coefficient Register MSB Color Space Conversion A3...
csc_coef_a3_lsb	0x4107	Color Space Converter Matrix A3 Coefficient Register LSB Color Space Conversion A3...
csc_coef_a4_msb	0x4108	Color Space Converter Matrix A4 Coefficient Register MSB Color Space Conversion A4...
csc_coef_a4_lsb	0x4109	Color Space Converter Matrix A4 Coefficient Register LSB Color Space Conversion A4...
csc_coef_b1_msb	0x410a	Color Space Converter Matrix B1 Coefficient Register MSB Color Space Conversion B1...
csc_coef_b1_lsb	0x410b	Color Space Converter Matrix B1 Coefficient Register LSB Color Space Conversion B1...
csc_coef_b2_msb	0x410c	Color Space Converter Matrix B2 Coefficient Register MSB Color Space Conversion B2...
csc_coef_b2_lsb	0x410d	Color Space Converter Matrix B2 Coefficient Register LSB Color Space Conversion B2...
csc_coef_b3_msb	0x410e	Color Space Converter Matrix B3 Coefficient Register MSB Color Space Conversion B3...
csc_coef_b3_lsb	0x410f	Color Space Converter Matrix B3 Coefficient Register LSB Color Space Conversion B3...
csc_coef_b4_msb	0x4110	Color Space Converter Matrix B4 Coefficient Register MSB Color Space Conversion B4...

Registers for Address Block: ColorSpaceConverter (Continued)

Register	Offset	Description
csc_coef_b4_lsb	0x4111	Color Space Converter Matrix B4 Coefficient Register LSB Color Space Conversion B4...
csc_coef_c1_msb	0x4112	Color Space Converter Matrix C1 Coefficient Register MSB Color Space Conversion C1...
csc_coef_c1_lsb	0x4113	Color Space Converter Matrix C1 Coefficient Register LSB

		Color Space Conversion C1...
csc_coef_c2_msb	0x4114	Color Space Converter Matrix C2 Coefficient Register MSB Color Space Conversion C2...
csc_coef_c2_lsb	0x4115	Color Space Converter Matrix C2 Coefficient Register LSB Color Space Conversion C2...
csc_coef_c3_msb	0x4116	Color Space Converter Matrix C3 Coefficient Register MSB Color Space Conversion C3...
csc_coef_c3_lsb	0x4117	Color Space Converter Matrix C3 Coefficient Register LSB Color Space Conversion C3...
csc_coef_c4_msb	0x4118	Color Space Converter Matrix C4 Coefficient Register MSB Color Space Conversion C4...
csc_coef_c4_lsb	0x4119	Color Space Converter Matrix C4 Coefficient Register LSB Color Space Conversion C4...
csc_limit_up_msb	0x411a	Color Space Converter Matrix Output Up Limit Register MSB For more details, refer to the HDMI 1.4...
csc_limit_up_lsb	0x411b	Color Space Converter Matrix output Up Limit Register LSB For more details, refer to the HDMI 1.4...
csc_limit_dn_msb	0x411c	Color Space Converter Matrix output Down Limit Register MSB For more details, refer to the HDMI...
csc_limit_dn_lsb	0x411d	Color Space Converter Matrix output Down Limit Register LSB For more details, refer to the HDMI...

csc_cfg

Description: Color Space Converter Interpolation and Decimation Configuration Register
Size: 8 bits
Offset: 0x4100

Bits	Name	Attr	Description
7	csc_limit	R/W	When set (1'b1), the range limitation values defined in registers csc_mat_uplim and csc_mat_dnlim are applied to the output of the Color Space Conversion matrix. This feature ensures that the video output range is always respected, independently of the matrix coefficient configuration or of the video input stream. Value After Reset: 0x0
6	spare_2	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
5:4	intmode	R/W	Chroma interpolation configuration: intmode[1:0] | Chroma Interpolation 00 | interpolation disabled 01 | Hu (z) =1 + z^(-1) 10 | Hu(z)=1/ 2 + z^(-11)+1/2 z^(-2) 11 | interpolation disabled Value After Reset: 0x0
3:2	spare_1	R/W	Reserved as "spare" register with no associated functionality.

			Value After Reset: 0x0
1:0	decmode	R/W	Chroma decimation configuration: decmode[1:0] | Chroma Decimation 00 | decimation disabled 01 | Hd (z) =1 10 | Hd(z)=1/ 4 + 1/2z^(-1)+1/4 z^(-2) 11 | Hd(z)x2^(11)= -5+12z^(-2) - 22z^(-4)+39z^(-8) +109z^(-10) -204z^(-12)+648z^(-14) + 1024z^(-15) +648z^(-16) - 204z^(-18) +109z^(-20)- 65z^(-22) +39z^(-24) - 22z^(-26) +12z^(- 28)-5z^(-30) Value After Reset: 0x0

csc_scale

Description: Color Space Converter Scale and Deep Color Configuration Register

Size: 8 bits

Offset: 0x4101

Bits	Name	Attr	Description
7:4	csc_color_depth	R/W	Color space converter color depth configuration: csc_colordepth[3:0] | Action 0000 | 24 bit per pixel video (8 bit per component). 0001-0011 | Reserved. Not used. 0100 | 24 bit per pixel video (8 bit per component). 0101 | 30 bit per pixel video (10 bit per component). 0110 | 36 bit per pixel video (12 bit per component). 0111 | 48 bit per pixel video (16 bit per component). other | Reserved. Not used. Value After Reset: 0x0
3:2	spare	R/W	The is a Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
1:0	cscscale	R/W	Defines the cscscale[1:0] scale factor to apply to all coefficients in Color Space Conversion. This scale factor is expressed in the number of left shifts to apply to each of the coefficients, ranging from 0 to 2. Value After Reset: 0x1

csc_coef_a1_msb

Description: Color Space Converter Matrix A1 Coefficient Register MSB Notes:
The coefficients used in the CSC matrix use only 15 bits for the internal computations.
Coefficients are represented in 2's complementary format and stored in two registers:
csc_coef_*_lsb[7:0]: coefficient bits 7 to 0
csc_coef_*_msb[7]: spare bit
csc_coef_*_msb[6:0]: coefficient bits 14 to 8
Examples for standard ITU601 and ITU709 RGB/YCC conversion CSC coefficients exist in the Video Datapath Application Note.
Size: 8 bits
Offset: 0x4102

Bits	Name	Attr	Description
7:0	csc_coef_a1_msb	R/W	Color Space Converter Matrix A1 Coefficient Register MSB Value After Reset: 0x20

csc_coef_a1_lsb

Description: Color Space Converter Matrix A1 Coefficient Register LSB Notes:
The coefficients used in the CSC matrix use only 15 bits for the internal computations.
Coefficients are represented in 2's complementary format and stored in two registers:
csc_coef_*_lsb[7:0]: coefficient bits 7 to 0
csc_coef_*_msb[7]: spare bit
csc_coef_*_msb[6:0]: coefficient bits 14 to 8
Examples for standard ITU601 and ITU709 RGB/YCC conversion CSC coefficients exist in the Video Datapath Application Note.
Size: 8 bits
Offset: 0x4103

Bits	Name	Attr	Description
7:0	csc_coef_a1_lsb	R/W	Color Space Converter Matrix A1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a2_msb

Description: Color Space Converter Matrix A2 Coefficient Register MSB Color Space Conversion A2 coefficient.
Size: 8 bits
Offset: 0x4104

Bits	Name	Attr	Description
7:0	csc_coef_a2_msb	R/W	Color Space Converter Matrix A2 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a2_lsb

Description: Color Space Converter Matrix A2 Coefficient Register LSB Color Space Conversion A2 coefficient.
Size: 8 bits

Offset: 0x4105

Bits	Name	Attr	Description
7:0	csc_coef_a2_lsb	R/W	Color Space Converter Matrix A2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a3_msb

Description: Color Space Converter Matrix A3 Coefficient Register MSB Color Space Conversion A3 coefficient.

Size: 8 bits

Offset: 0x4106

Bits	Name	Attr	Description
7:0	csc_coef_a3_msb	R/W	Color Space Converter Matrix A3 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a3_lsb

Description: Color Space Converter Matrix A3 Coefficient Register LSB Color Space Conversion A3 coefficient.

Size: 8 bits

Offset: 0x4107

Bits	Name	Attr	Description
7:0	csc_coef_a3_lsb	R/W	Color Space Converter Matrix A3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_a4_msb

Description: Color Space Converter Matrix A4 Coefficient Register MSB Color Space Conversion A4 coefficient.

Size: 8 bits

Offset: 0x4108

Bits	Name	Attr	Description
7:0	csc_coef_a4_msb	R/W	Color Space Converter Matrix A4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_a4_lsb

Description: Color Space Converter Matrix A4 Coefficient Register LSB Color Space Conversion A4 coefficient.

Size: 8 bits

Offset: 0x4109

Bits	Name	Attr	Description
7:0	csc_coef_a4_lsb	R/W	Color Space Converter Matrix A4 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b1_msb
Description: Color Space Converter Matrix B1 Coefficient Register MSB Color Space Conversion B1 coefficient.
Size: 8 bits
Offset: 0x410a

Bits	Name	Attr	Description
7:0	csc_coef_b1_msb	R/W	Color Space Converter Matrix B1 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b1_lsb
Description: Color Space Converter Matrix B1 Coefficient Register LSB Color Space Conversion B1 coefficient.
Size: 8 bits
Offset: 0x410b

Bits	Name	Attr	Description
7:0	csc_coef_b1_lsb	R/W	Color Space Converter Matrix B1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b2_msb
Description: Color Space Converter Matrix B2 Coefficient Register MSB Color Space Conversion B2 coefficient.
Size: 8 bits
Offset: 0x410c

Bits	Name	Attr	Description
7:0	csc_coef_b2_msb	R/W	Color Space Converter Matrix B2 Coefficient Register MSB Value After Reset: 0x20

csc_coef_b2_lsb
Description: Color Space Converter Matrix B2 Coefficient Register LSB Color Space Conversion B2 coefficient.
Size: 8 bits
Offset: 0x410d

Bits	Name	Attr	Description
7:0	csc_coef_b2_lsb	R/W	Color Space Converter Matrix B2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b3_msb
Description: Color Space Converter Matrix B3 Coefficient Register MSB Color Space Conversion B3 coefficient.

Size: 8 bits
Offset: 0x410e

Bits	Name	Attr	Description
7:0	csc_coef_b3_msb	R/W	Color Space Converter Matrix B3 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b3_lsb
Description: Color Space Converter Matrix B3 Coefficient Register LSB Color Space Conversion B3 coefficient.
Size: 8 bits
Offset: 0x410f

Bits	Name	Attr	Description
7:0	csc_coef_b3_lsb	R/W	Color Space Converter Matrix B3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_b4_msb
Description: Color Space Converter Matrix B4 Coefficient Register MSB Color Space Conversion B4 coefficient.
Size: 8 bits
Offset: 0x4110

Bits	Name	Attr	Description
7:0	csc_coef_b4_msb	R/W	Color Space Converter Matrix B4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_b4_lsb
Description: Color Space Converter Matrix B4 Coefficient Register LSB Color Space Conversion B4 coefficient.
Size: 8 bits
Offset: 0x4111

Bits	Name	Attr	Description
7:0	csc_coef_b4_lsb	R/W	Color Space Converter Matrix B4 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c1_msb
Description: Color Space Converter Matrix C1 Coefficient Register MSB Color Space Conversion C1 coefficient.
Size: 8 bits
Offset: 0x4112

Bits	Name	Attr	Description
7:0	csc_coef_c1_msb	R/W	Color Space Converter Matrix C1 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c1_lsb
Description: Color Space Converter Matrix C1 Coefficient Register LSB Color Space Conversion C1 coefficient.
Size: 8 bits
Offset: 0x4113

Bits	Name	Attr	Description
7:0	csc_coef_c1_lsb	R/W	Color Space Converter Matrix C1 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c2_msb
Description: Color Space Converter Matrix C2 Coefficient Register MSB Color Space Conversion C2 coefficient.
Size: 8 bits
Offset: 0x4114

Bits	Name	Attr	Description
7:0	csc_coef_c2_msb	R/W	Color Space Converter Matrix C2 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c2_lsb
Description: Color Space Converter Matrix C2 Coefficient Register LSB Color Space Conversion C2 coefficient.
Size: 8 bits
Offset: 0x4115

Bits	Name	Attr	Description
7:0	csc_coef_c2_lsb	R/W	Color Space Converter Matrix C2 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c3_msb
Description: Color Space Converter Matrix C3 Coefficient Register MSB Color Space Conversion C3 coefficient.
Size: 8 bits
Offset: 0x4116

Bits	Name	Attr	Description
7:0	csc_coef_c3_msb	R/W	Color Space Converter Matrix C3 Coefficient Register MSB Value After Reset: 0x20

csc_coef_c3_lsb
Description: Color Space Converter Matrix C3 Coefficient Register LSB Color Space Conversion C3 coefficient.
Size: 8 bits
Offset: 0x4117

Bits	Name	Attr	Description
7:0	csc_coef_c3_lsb	R/W	Color Space Converter Matrix C3 Coefficient Register LSB Value After Reset: 0x0

csc_coef_c4_msb

Description: Color Space Converter Matrix C4 Coefficient Register MSB Color Space Conversion C4 coefficient.

Size: 8 bits

Offset: 0x4118

Bits	Name	Attr	Description
7:0	csc_coef_c4_msb	R/W	Description: Color Space Converter Matrix C4 Coefficient Register MSB Value After Reset: 0x0

csc_coef_c4_lsb

Description: Color Space Converter Matrix C4 Coefficient Register LSB Color Space Conversion C4 coefficient.

Size: 8 bits

Offset: 0x4119

Bits	Name	Attr	Description
7:0	csc_coef_c4_lsb	R/W	Color Space Converter Matrix C4 Coefficient Register LSB Value After Reset: 0x0

csc_limit_up_msb

Description: Color Space Converter Matrix Output Up Limit Register MSB

For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges. For an RGB output of 8 bits, the expected limit is 254, and this register must be configured with 0x00.

Size: 8 bits

Offset: 0x411a

Bits	Name	Attr	Description
7:0	csc_limit_up_msb	R/W	Color Space Converter Matrix Output Upper Limit Register MSB Value After Reset: 0xff

csc_limit_up_lsb

Description: Color Space Converter Matrix output Up Limit Register LSB

For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges. For an RGB output of 8 bits, the expected limit is 254, and this register must be configured with 0xFE.

Size: 8 bits

Offset: 0x411b

Bits	Name	Attr	Description
7:0	csc_limit_up_lsb	R/W	Color Space Converter Matrix Output Upper Limit

			Register LSB Value After Reset: 0xff

csc_limit_dn_msb

Description: Color Space Converter Matrix output Down Limit Register MSB
For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges. For an RGB output of 8 bits, the expected limit is 1, and this register must be configured with 0x00.
Size: 8 bits
Offset: 0x411c

Bits	Name	Attr	Description
7:0	csc_limit_dn_msb	R/W	Color Space Converter Matrix output Down Limit Register MSB Value After Reset: 0x0

csc_limit_dn_lsb

Description: Color Space Converter Matrix output Down Limit Register LSB
For more details, refer to the HDMI 1.4 specification, paragraph 6.6 Video Quantization Ranges. For an RGB output of 8 bits, the expected limit is 1, and this register must be configured with 0x01.
Size: 8 bits
Offset: 0x411d

Bits	Name	Attr	Description
7:0	csc_limit_dn_lsb	R/W	Color Space Converter Matrix Output Down Limit Register LSB Value After Reset: 0x0

HDCP Registers

HDCP Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
a_hdcpcfg0	0x5000	HDCP Enable and Functional Control Configuration Register 0
a_hdcpcfg1	0x5001	HDCP Software Reset and Functional Control Configuration Register 1
a_hdcpobs0	0x5002	HDCP Observation Register 0
a_hdcpobs1	0x5003	HDCP Observation Register 1
a_hdcpobs2	0x5004	HDCP Observation Register 2
a_hdcpobs3	0x5005	HDCP Observation Register 3
a_apiintclr	0x5006	HDCP Interrupt Clear Register Write only register, active high and auto cleared, cleans the respective...
a_apiintstat	0x5007	HDCP Interrupt Status Register Read only register, reports the interruption which caused the activation...
a_apiintmsk	0x5008	HDCP Interrupt Mask Register The configuration of this register mask a given setup of interruption,...

Register	Offset	Description
a_vidpolcfg	0x5009	HDCP Video Polarity Configuration Register
a_oesswcfg	0x500a	HDCP OESS WOO Configuration Register Pulse width of the encryption enable (CTL3) signal in the...
a_coreverlsb	0x5014	HDCP Controller Version Register LSB Design ID number.
a_corevermsb	0x5015	HDCP Controller Version Register MSB Revision ID number.
a_ksvmemctrl	0x5016	HDCP KSV Memory Control Register The KSVCTRLupd bit is a notification flag. This flag changes polarity...
hdcp_bstatus[0:1]	0x5020 + (i * 0x1)	HDCP BStatus Register Array
hdcp_m0[0:7]	0x5022 + (i * 0x1)	HDCP M0 Register Array
hdcp_ksv[0:634]	0x502a + (i * 0x1)	HDCP KSV Registers
hdcp_vh[0:19]	0x52a5 + (i * 0x1)	HDCP SHA-1 VH Registers
hdcp_revoc_size_0	0x52b9	HDCP Revocation KSV List Size Register 0
hdcp_revoc_size_1	0x52ba	HDCP Revocation KSV List Size Register 1
hdcp_revoc_list[0:5059]	0x52bb + (i * 0x1)	HDCP Revocation KSV Registers
hdcpreg_bksv0	0x7800	HDCP KSV Status Register 0

Registers for Address Block: HDCP (Continued)

Register	Offset	Description
hdcpreg_bksv1	0x7801	HDCP KSV Status Register 1
hdcpreg_bksv2	0x7802	HDCP KSV Status Register 2
hdcpreg_bksv3	0x7803	HDCP KSV Status Register 3
hdcpreg_bksv4	0x7804	HDCP KSV Status Register 4
hdcpreg_anconf	0x7805	HDCP AN Bypass Control Register
hdcpreg_an0	0x7806	HDCP Forced AN Register 0
hdcpreg_an1	0x7807	HDCP Forced AN Register 1
hdcpreg_an2	0x7808	HDCP forced AN Register 2
hdcpreg_an3	0x7809	HDCP Forced AN Register 3
hdcpreg_an4	0x780a	HDCP Forced AN Register 4

Register	Offset	Description
hdcpreg_an5	0x780b	HDCP Forced AN Register 5
hdcpreg_an6	0x780c	HDCP Forced AN Register 6
hdcpreg_an7	0x780d	HDCP Forced AN Register 7
hdcpreg_rmlctl	0x780e	HDCP Encrypted Device Private Keys Control Register This register is the control register for the...
hdcpreg_rmlsts	0x780f	HDCP Encrypted DPK Status Register The required software configuration sequence is documented in...
hdcpreg_seed0	0x7810	HDCP Encrypted DPK Seed Register 0 This register contains a byte of the HDCP Encrypted DPK seed...
hdcpreg_seed1	0x7811	HDCP Encrypted DPK Seed Register 1 This register contains a byte of the HDCP Encrypted DPK seed...
hdcpreg_dpk0	0x7812	HDCP Encrypted DPK Data Register 0 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk1	0x7813	HDCP Encrypted DPK Data Register 1 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk2	0x7814	HDCP Encrypted DPK Data Register 2 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk3	0x7815	HDCP Encrypted DPK Data Register 3 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk4	0x7816	HDCP Encrypted DPK Data Register 4 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk5	0x7817	HDCP Encrypted DPK Data Register 5 This register contains an HDCP DPK byte. The required software...
hdcpreg_dpk6	0x7818	HDCP Encrypted DPK Data Register 6 This register contains an HDCP DPK byte. The required software...

a_hdcpcfg0

Description: HDCP Enable and Functional Control Configuration Register 0

Size: 8 bits

Offset: 0x5000

Bits	Name	Attr	Description
7	ELVena	R/W	Enables the Enhanced Link Verification from the transmitter's side Value After Reset: 0x0
6	I2Cfastmode	R/W	Enable the I2C fast mode option from the transmitter's side. Value After Reset: 0x0

5	bypencryption	R/W	Bypasses all the data encryption stages Value After Reset: "(HDMI_HDCP_BYPASS== 1) ? 1 : 0"
4	syncricheck	R/W	Configures if the Ri check should be done at every 2s even or synchronously to every 128 encrypted frame. Value After Reset: 0x0
3	avmute	R	This register holds the current AVMUTE state of the Hdmi_tx controller, as expected to be perceived by the connected HDMI/HDCP sink device. Value After Reset: 0x0
2	rxdetect	R/W	Information that a sink device was detected connected to the HDMI port Value After Reset: 0x0
1	en11feature	R/W	Enable the use of features 1.1 from the transmitter's side Value After Reset: 0x0
0	hdmidvi	R/W	Configures the transmitter to operate with a HDMI capable device or with a DVI device. Value After Reset: 0x0

a_hdcpcfg1

Description: HDCP Software Reset and Functional Control Configuration Register 1

Size: 8 bits

Offset: 0x5001

Bits	Name	Attr	Description
7:5	spare	R/W	Reserved as "spare" register with no associated functionality. Value After Reset: 0x0
4	hdcp_lock	R/W	Lock the HDCP bypass and encryption disable mechanisms: 1'b0: The default 1'b0 value enables you to bypass HDCP through bit 5 (bypencryption) of the A_HDCPCFG0 register or to disable the encryption through bit 1 (encryptiondisable) of A_HDCPCFG1. 1'b1: You can still write to the bit bypencryption of A_HDCPCFG0 or encryptiondisable bit of A_HDCPCFG1 but you cannot enable the bypass. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Value After Reset: 0x0
3	dissha1check	R/W	Disables the request to the API processor to verify the SHA1 message digest of a received KSV List Value After Reset: 0x0
2	ph2upshftenc	R/W	Enables the encoding of packet header in the

Bits	Name	Attr	Description
			tmdsch0 bit[0] with cipher[2] instead of the tmdsch0 bit[2] Note: This bit must always be set to 1 for all PHYs. Value After Reset: 0x0
1	encryptiondisable	R/W	Disable encryption without losing authentication Value After Reset: 0x0
0	swreset	R/W	Software reset signal, active by writing a zero and auto cleared to 1 in the following cycle. Value After Reset: 0x1

a_hdcpobs0

Description: HDCP Observation Register 0

Size: 8 bits

Offset: 0x5002

Bits	Name	Attr	Description
7:4	STATEA	R	Observability register informs in which state the authentication machine is on. Value After Reset: 0x0
3:1	SUBSTATEA	R	Observability register informs in which sub-state the authentication is on. Value After Reset: 0x0
0	hdcpengaged	R	Informs that the current HDMI link has the HDCP protocol fully engaged. Value After Reset: 0x0

a_hdcpobs1

Description: HDCP Observation Register 1

Size: 8 bits

Offset: 0x5003

Bits	Name	Attr	Description
7			Reserved for future use.
6:4	STATEOEG	R	Observability register informs in which state the OESS machine is on. Value After Reset: 0x0
3:0	STATER	R	Observability register informs in which state the revocation machine is on. Value After Reset: 0x0

a_hdcpobs2

Description: HDCP Observation Register 2

Size: 8 bits

Offset: 0x5004

Bits	Name	Attr	Description
7:6			Reserved for future use.
5:3	STATEE	R	Observability register informs in which state the

			cipher machine is on. Value After Reset: 0x0
2:0	STATEEEG	R	Observability register informs in which state the EESS machine is on. Value After Reset: 0x0

a_hdcpobs3

Description: HDCP Observation Register 3

Size: 8 bits

Offset: 0x5005

Bits	Name	Attr	Description
7	HDMI_RESERVED_1	R	Register read from attached sink device: Bcap(0x40) bit 7. Value After Reset: 0x0
6	REPEATER	R	Register read from attached sink device: Bcap(0x40) bit 6. Value After Reset: 0x0
5	KSV_FIFO_READY	R	Register read from attached sink device: Bcap(0x40) bit 5. Value After Reset: 0x0
4	FAST_I2C	R	Register read from attached sink device: Bcap(0x40) bit 4. Value After Reset: 0x0
3	HDMI_RESERVED_2	R	Register read from attached sink device: Bstatus(0x41) bit 13. Value After Reset: 0x0
2	HDMI_MODE	R	Register read from attached sink device: Bstatus(0x41) bit 12. Value After Reset: 0x0
1	FEATURES_1_1	R	Register read from attached sink device: Bcap(0x40) bit 1. Value After Reset: 0x0
0	FAST_REAUTHENTICATION	R	Register read from attached sink device: Bcap(0x40) bit 0. Value After Reset: 0x0

a_apiintclr

Description: HDCP Interrupt Clear Register

Write only register, active high and auto cleared, cleans the respective interruption in the interrupt status register.

Size: 8 bits

Offset: 0x5006

Bits	Name	Attr	Description
7	HDCP_engaged	W	Clears the interruption related to HDCP authentication process successful. Value After Reset: 0x0

6	HDCP_failed	W	Clears the interruption related to HDCP authentication process failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	W	Clears the interruption related to SHA1 verification has been done Value After Reset: 0x0
4	I2Cnack	W	Clears the interruption related to I2C NACK reception. Value After Reset: 0x0
3	Lostarbitration	W	Clears the interruption related to I2C arbitration lost. Value After Reset: 0x0
2	Keepouterrorint	W	Clears the interruption related to keep out window error. Value After Reset: 0x0
1	KSVsha1calcint	W	Clears the interruption related to KSV list update in memory that needs to be SHA1 verified. Value After Reset: 0x0
0	KSVaccessint	W	Clears the interruption related to KSV Attr grant for Read-Write access. Value After Reset: 0x0

a_apiintstat

Description: HDCP Interrupt Status Register

Read only register, reports the interruption which caused the activation of the interruption output pin.

Size: 8 bits

Offset: 0x5007

Bits	Name	Attr	Description
7	HDCP_engaged	R	Notifies that the HDCP authentication process was successful Value After Reset: 0x0
6	HDCP_failed	R	Notifies that the HDCP authentication process was failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	R	Notifies that the HDCP13TCTRL controller SHA1 verification has been done. The status ready to be read. Value After Reset: 0x0
4	I2Cnack	R	Notifies that the I2C received a NACK from slave device. Value After Reset: 0x0
3	Lostarbitration	R	Notifies that the I2C lost the arbitration to communicate. Another master gained arbitration. Value After Reset: 0x0
2	Keepouterrorint	R	Notifies that during the keep out window, the

Bits	Name	Attr	Description
			ctlout[3:0] bus was used besides control period. Value After Reset: 0x0
1	KSVsha1calcint	R	Notifies that the HDCP13TCTRL controller as updated a KSV list in memory that needs to be SHA1 verified. Value After Reset: 0x0
0	KSVaccessint	R	Notifies that the KSV Attr as been guaranteed for Read-Write access. Value After Reset: 0x0

a_apiintmsk

Description: HDCP Interrupt Mask Register

The configuration of this register mask a given setup of interruption, disabling them from generating interruption pulses in the interruption output pin.

Size: 8 bits

Offset: 0x5008

Bits	Name	Attr	Description
7	HDCP_engaged	R/W	Masks the interruption related to HDCP authentication process successful. Value After Reset: 0x0
6	HDCP_failed	R/W	Masks the interruption related to HDCP authentication process failed. Value After Reset: 0x0
5	KSVsha1calcdoneint	R/W	Masks the interruption related to SHA1 verification has been done Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
4	I2Cnack	R/W	Masks the interruption related to I2C NACK reception. Value After Reset: 0x0
3	Lostarbitration	R/W	Masks the interruption related to I2C arbitration lost. Value After Reset: 0x0
2	Keepouterrorint	R/W	Masks the interruption related to keep out window error. Value After Reset: 0x0
1	KSVsha1calcint	R/W	Masks the interruption related to KSV list update in memory that needs to be SHA1 verified. Otherwise, this field is a "spare" bit with no associated functionality. Value After Reset: 0x0
0	KSVaccessint	R/W	Masks the interruption related to KSV Attr grant for Read-Write access. Value After Reset: 0x0

a_vidpolcfg

Description: HDCP Video Polarity Configuration Register

Size: 8 bits

Offset: 0x5009

Bits	Name	Attr	Description
7			Reserved for future use.
6:5	unencryptconf	R/W	Configuration of the color sent when sending unencrypted video data Value After Reset: 0x0
4	dataenpol	R/W	Configuration of the video data enable polarity Value After Reset: 0x0
3	vsyncpol	R/W	Configuration of the video Vertical synchronism polarity Value After Reset: 0x0
2	spare_2	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0
1	hsyncpol	R/W	Configuration of the video Horizontal synchronism polarity. Value After Reset: 0x0
0	spare_1	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x0

a_oesswcfg

Description: HDCP OESS WOO Configuration Register

Pulse width of the encryption enable (CTL3) signal in the HDCP OESS mode. The window of opportunity for the Original Encryption Status Signaling starts at the active edge of the Vertical synchronism and stops after oesswindowoffset[7:0]*4 clock cycles of TMDS clock. According to the HDCP specification, the CTL3 signal must be asserted at least for eight TMDS clock cycles (oesswindowoffset[7:0] must be greater than 1), and it is recommended to transmit a larger pulse width for enhanced link reliability.

Size: 8 bits

Offset: 0x500a

Bits	Name	Attr	Description
7:0	a_oesswcfg	R/W	HDCP OESS WOO Configuration Register Value After Reset: 0x80

a_coreverlsb

Description: HDCP Controller Version Register LSB Design ID number.

Size: 8 bits

Offset: 0x5014

Bits	Name	Attr	Description
7:0	a_coreverlsb	R	HDCP Controller Version Register LSB Value After Reset: 0x2

a_corevermsb

Description: HDCP Controller Version Register MSB Revision ID number.

Size: 8 bits

Offset: 0x5015

Bits	Name	Attr	Description
7:0	a_corevermsb	R	HDCP Controller Version Register MSB Value After Reset: 0x3

a_ksvmemctrl

Description: HDCP KSV Memory Control Register

The KSVCTRLupd bit is a notification flag. This flag changes polarity whenever the register is written. This flag acts as a trigger to other blocks that processes this data. Upon reset the flag returns to low default value.

Size: 8 bits

Offset: 0x5016

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	KSVsha1status	R	Notification whether the KSV list message digest is correct from the controller: 1'b1 if digest message verification failed 1'b0 if digest message verification succeeded Value After Reset: 0x0
3	SHA1fail	R/W	Notification whether the KSV list message digest is correct. Value After Reset: 0x0
2	KSVCTRLupd	R/W	Set to inform that the KSV list in memory has been analyzed and the response to the Message Digest has been updated if on configurations on software SHA-1 calculation. Value After Reset: 0x0
1	KSVMEMaccess	R	Notification that the KSV Attr as been guaranteed. Value After Reset: 0x0
0	KSVMEMrequest	R/W	Request access to the KSV memory; must be de-asserted after the access is completed by the system. Value After Reset: 0x0

hdcp_bstatus[0:1]

Description: HDCP BStatus Register Array

Size: 8 bits

Offset: 0x5020 + (i * 0x1)

Bits	Name	Attr	Description
7:0	bstatus	R/W	HDCP BSTATUS[15:0]. If Attr has not been granted (see register a_ksvmemctrl), the value read will be 8'hff. Value After Reset: 0xff

hdcp_m0[0:7]

Description: HDCP M0 Register Array

Size: 8 bits

Offset: 0x5022 + (i * 0x1)

Bits	Name	Attr	Description
7:0	M0	R/W	HDCP M0[32:0]. If Attr has not been granted (see register a_ksvmemctrl) , the value read will be 8'hff. These values are only available on a configuration that has the SHA1 calculation by software. Value After Reset: 0xff

hdcp_ksv[0:634]

Description: HDCP KSV Registers.

Size: 8 bits

Offset: 0x502a + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_ksv_byte	R/W	Sink KSV FIFO byte, ordered in little endian (byte at address 0x502a belongs to byte 0 of KSV0). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space, 635 KSV FIFO bytes are mapped, which allow for 127 KSV values, each with 5 bytes (40 bits). Value After Reset: 0xff

hdcp_vh[0:19]

Description: HDCP SHA-1 VH Registers.

Size: 8 bits

Offset: 0x52a5 + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_vh_byte	R/W	Sink VH' byte, ordered in little endian (byte at address 0x525a belongs to byte 0 of VH0). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space 20 VH bytes are mapped, which allow for 5 VH values, each with 4 bytes (32bits). Value After Reset: 0xff

hdcp_revoc_size_0

Description: HDCP Revocation KSV List Size Register 0

Size: 8 bits

Offset: 0x52b9

Bits	Name	Attr	Description

7:0	hdcp_revoc_size_0	R/W	Register containing the LSB of KSV list size (ksv_list_size[7:0]). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. Value After Reset: 0xff

hdcp_revoc_size_1

Description: HDCP Revocation KSV List Size Register 1

Size: 8 bits

Offset: 0x52ba

Bits	Name	Attr	Description
7:0	hdcp_revoc_size_1	R/W	Register containing the MSB of KSV list size (ksv_list_size[15:8]). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. Value After Reset: 0xff

hdcp_revoc_list[0:5059]

Description: HDCP Revocation KSV Registers.

Size: 8 bits

Offset: 0x52bb + (i * 0x1)

Bits	Name	Attr	Description
7:0	hdcp_revoc_list_ksv_byte	R/W	Revocation KSV byte, ordered in little endian (byte at address 0x52bb belongs to byte 0 of the first revoked KSV). If Attr has not been granted (see register a_ksvmemctrl), the value read is 8'hff. In this address space 5060 revoked KSV bytes are mapped, which allow for 1012 KSV values, each with 5 bytes (40 bits). Value After Reset: 0xff

hdcpreg_bksv0

Description: HDCP KSV Status Register 0

Size: 8 bits

Offset: 0x7800

Bits	Name	Attr	Description
7:0	hdcpreg_bksv0	R	Contains the value of BKSV[7:0]. Value After Reset: 0x0

hdcpreg_bksv1

Description: HDCP KSV Status Register 1

Size: 8 bits

Offset: 0x7801

Bits	Name	Attr	Description
7:0	hdcpreg_bksv1	R	Description: Contains the value of BKSV[15:8]. Value After Reset: 0x0

hdcpreg_bksv2

Description: HDCP KSV Status Register 2
Size: 8 bits
Offset: 0x7802

Bits	Name	Attr	Description
7:0	hdcpreg_bksv2	R	Contains the value of BKSV[23:16]. Value After Reset: 0x0

hdcpreg_bksv3
Description: HDCP KSV Status Register 3
Size: 8 bits
Offset: 0x7803

Bits	Name	Attr	Description
7:0	hdcpreg_bksv3	R	Contains the value of BKSV[31:24]. Value After Reset: 0x0

hdcpreg_bksv4
Description: HDCP KSV Status Register 4
Size: 8 bits
Offset: 0x7804

Bits	Name	Attr	Description
7:0	hdcpreg_bksv4	R	Contains the value of BKSV[39:32]. Value After Reset: 0x0

hdcpreg_anconf
Description: HDCP AN Bypass Control Register
Size: 8 bits
Offset: 0x7805

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	oanbypass	R/W	When oanbypass=1, the value of AN used in the HDCP engine comes from the hdcpreg_an0 to hdcpreg_an7 registers. When oanbypass=0, the value of AN used in the HDCP engine comes from the random number input. Value After Reset: 0x0

hdcpreg_an0
Description: HDCP Forced AN Register 0
Size: 8 bits
Offset: 0x7806

Bits	Name	Attr	Description
7:0	hdcpreg_an0	R/W	Contains the value of AN[7:0] Value After Reset: 0x0

hdcpreg_an1
Description: HDCP Forced AN Register 1

Size: 8 bits
Offset: 0x7807

Bits	Name	Attr	Description
7:0	hdcpreg_an1	R/W	Contains the value of AN[15:8] Value After Reset: 0x0

hdcpreg_an2
Description: HDCP forced AN Register 2
Size: 8 bits
Offset: 0x7808

Bits	Name	Attr	Description
7:0	hdcpreg_an2	R/W	Contains the value of AN[23:16] Value After Reset: 0x0

hdcpreg_an3
Description: HDCP Forced AN Register 3
Size: 8 bits
Offset: 0x7809

Bits	Name	Attr	Description
7:0	hdcpreg_an3	R/W	Contains the value of AN[31:24] Value After Reset: 0x0

hdcpreg_an4
Description: HDCP Forced AN Register 4
Size: 8 bits
Offset: 0x780a

Bits	Name	Attr	Description
7:0	hdcpreg_an4	R/W	Contains the value of AN[39:32] Value After Reset: 0x0

hdcpreg_an5
Description: HDCP Forced AN Register 5
Size: 8 bits
Offset: 0x780b

Bits	Name	Attr	Description
7:0	hdcpreg_an5	R/W	Contains the value of AN[47:40] Value After Reset: 0x0

hdcpreg_an6
Description: HDCP Forced AN Register 6
Size: 8 bits
Offset: 0x780c

Bits	Name	Attr	Description
7:0	hdcpreg_an6	R/W	Contains the value of AN[55:48] Value After Reset: 0x0

hdcpreg_an7

Description: HDCP Forced AN Register 7

Size: 8 bits

Offset: 0x780d

Bits	Name	Attr	Description
7:0	hdcpreg_an7	R/W	Contains the value of BKSV[63:56] Value After Reset: 0x0

hdcpreg_rmlctl

Description: HDCP Encrypted Device Private Keys Control Register

This register is the control register for the software programmable encrypted DPK embedded storage feature. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x780e

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	odpk_decrypt_enable	R/W	When set (1'b1), this bit activates the decryption of the Device Private keys. Value After Reset: 0x0

hdcpreg_rmlsts

Description: HDCP Encrypted DPK Status Register

The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x780f

Bits	Name	Attr	Description
7			Reserved for future use.
6	idpk_wr_ok_sts	R	When high (1'b1), it indicates that a DPK write is allowed. Value After Reset: 0x0
5:0	idpk_data_index	R	Current Device Private Key being written plus one. Position 0 is occupied by the AKSV. Value After Reset: 0x0

hdcpreg_seed0

Description: HDCP Encrypted DPK Seed Register 0

This register contains a byte of the HDCP Encrypted DPK seed value used to encrypt the Device Private Keys. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7810

Bits	Name	Attr	Description

7:0	hdcpreg_seed0	W	Least significant byte of the decryption seed value (dpk_decrypt_seed[7:0]). Value After Reset: 0x0

hdcpreg_seed1

Description: HDCP Encrypted DPK Seed Register 1

This register contains a byte of the HDCP Encrypted DPK seed value used to encrypt the Device Private Keys. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7811

Bits	Name	Attr	Description
7:0	hdcpreg_seed1	W	Most significant byte of the decryption seed value (dpk_decrypt_seed[15:8]). Value After Reset: 0x0

hdcpreg_dpk0

Description: HDCP Encrypted DPK Data Register 0

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7812

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[7:0] When this byte is written, a strobe signal is generated that triggers the decryption and/or storage of the DPK word on the DPK internal RAM memory. Value After Reset: 0x0

hdcpreg_dpk1

Description: HDCP Encrypted DPK Data Register 1

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."

Size: 8 bits

Offset: 0x7813

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[15:8] Value After Reset: 0x0

hdcpreg_dpk2

Description: HDCP Encrypted DPK Data Register 2

This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter,

Section 3.2.4, "Configure HDCP."
Size: 8 bits
Offset: 0x7814

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[23:16] Value After Reset: 0x0

hdcpreg_dpk3
Description: HDCP Encrypted DPK Data Register 3
This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."
Size: 8 bits
Offset: 0x7815

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[31:24] Value After Reset: 0x0

hdcpreg_dpk4
Description: HDCP Encrypted DPK Data Register 4
This register contains an HDCP DPK byte.
Size: 8 bits
Offset: 0x7816

Bits	Name	Attr	Description
7:0	dpk_data	W	Byte of the encrypted DPK value. dpk[39:32] Value After Reset: 0x0

hdcpreg_dpk5
Description: HDCP Encrypted DPK Data Register 5
This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."
Size: 8 bits
Offset: 0x7817

Bits	Name	Attr	Description
7:0	dpk_data	W	Contains the value of DPK[x][47:40] Value After Reset: 0x0

hdcpreg_dpk6
Description: HDCP Encrypted DPK Data Register 6
This register contains an HDCP DPK byte. The required software configuration sequence is documented in the Cores HDMI Transmitter User Guide in the "Programming" chapter, Section 3.2.4, "Configure HDCP."
Size: 8 bits
Offset: 0x7818

Bits	Name	Attr	Description

7:0	dpk_data	W	Contains the value of DPK[x][55:48] Value After Reset: 0x0

HDCP22 Registers

HDCP22 Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
hdcp22reg_id	0x7900	HDCP 2.2 Identification Register
hdcp22reg_ctrl	0x7904	HDCP 2.2 Control Register
hdcp22reg_ctrl1	0x7905	HDCP 2.2 Control Register 1
hdcp22reg_sts	0x7908	HDCP 2.2 Status Register
hdcp22reg_mask	0x790c	HDCP 2.2 Interrupt Mask Register
hdcp22reg_stat	0x790d	HDCP 2.2 interrupt Sticky Bit Status Register
hdcp22reg_mute	0x790e	HDCP 2.2 Interrupt Mute Vector

hdcp22reg_id

Description: HDCP 2.2 Identification Register
Size: 8 bits
Offset: 0x7900

Bits	Name	Attr	Description
7:3			Reserved for future use.
2	hdcp22_3rdparty	R	Indicates that External HDCP 2.2 interface is present and 3rd party HDCP 2.2 module is connected to this interface. Value After Reset: "(HTX_HDCP22_EXTERNAL_ELLP== 1) ? 1 : 0"
1	hdcp22_externalif	R	Indicates that External HDCP 2.2 interface is present. Value After Reset: "(HTX_HDCP22_EXTERNAL_NONE== 1) ? 1 : 0"
0			Reserved for future use.

hdcp22reg_ctrl

Description: HDCP 2.2 Control Register
Size: 8 bits
Offset: 0x7904

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	hpd_ovr_val	R/W	HPD Override Value 1'b0: If hpd_ovr_en is 1'b1 the HPD value to the HDCP 2.2 external interface is set to 1'b0. 1'b1: If hpd_ovr_en is 1'b1 the HPD value to the HDCP 2.2 external interface is set to 1'b1. Value After Reset: 0x0
4	hpd_ovr_en	R/W	HPD Override enable

Bits	Name	Attr	Description
			1'b0: The HPD value to the HDCP 2.2 external interface comes from the PHY as in phy_stat0.HPD. 1'b1: The HPD value to the HDCP 2.2 external interface comes from hpd_ovr_val bit field. Value After Reset: 0x0
3			Reserved for future use.
2	hdcp22_ovr_val	R/W	HDCP 2.2 versus 1.4 switch override value 1'b0: The switch is routed to HDCP 1.4 signals when hdcp22_ovr_en is 1'b1 and hdcp22_switch_lock is not set to 1'b1. 1'b1: The switch is routed to HDCP 2.2 signals when hdcp22_ovr_en is 1'b1 and hdcp22_switch_lock is not set to 1'b1. Value After Reset: 0x0
1	hdcp22_ovr_en	R/W	HDCP 2.2 versus 1.4 switch override enable 1'b0: The switch is automatically controlled by the HDCP 2.2 controller using the ist_hdcp2_capable and ist_hdcp2_not_capable status level indications. If the HDCP 2.2 controller indicates ist_hdcp2_capable at 1'b1, the switch is routed to HDCP 2.2 signals. If the HDCP 2.2 controller indicates ist_hdcp2_not_capable at 1'b1, the switch is routed to HDCP 1.4 signals. 1'b1: The HDCP 2.2 ist_hdcp2_capable and ist_hdcp2_not_capable values are ignored, and the direction of the HDCP 2.2 versus 1.4 switch is directly controlled by the hdcp22_ovr_val. Value After Reset: 0x0
0	hdcp22_switch_lck	R/W	HDCP 2.2 switch lock 1'b0: Enables you to change the direction of the HDCP 2.2 versus 1.4 switch by using the hdcp22_ovr_en and hdcp22_ovr_val. 1'b1: You can still write to hdcp22_ovr_en and hdcp22_ovr_val but has no effect over the HDCP 2.2 versus 1.4 switch, that keeps as it was configured by hdcp22_ovr_en and hdcp22_ovr_val at the time the 1'b1 was written to this bit field. Once you set the value to 1'b1, you can change the value back to 1'b0 only by issuing a master reset to the Hdmi_tx. Value After Reset: 0x0

hdcp22reg_ctrl1

Description: HDCP 2.2 Control Register 1

Size: 8 bits
Offset: 0x7905

Bits	Name	Attr	Description
7:4	hdcp22_cd_ovr_val	R/W	HDCP color depth override value, which is sent through the HDCP 2.2 external interface when hdcp22reg_ctrl1.hdcp22_cd_ovr_en is set. For reference on the HDMI allowed values consult the HDMI 1.4b specification, Table 6-1. Value After Reset: 0x0
3	hdcp22_cd_ovr_en	R/W	HDCP 2.2 versus 1.4 color depth override enable: 1'b0: The default 1'b0 value indicates that the color depth sent to the external interface is the one configured in the vp_pr_cd.color_depth register field. 1'b1: Although the used color depth for pixel encoding is defined by the field vp_pr_cd.color_depth register, the color depth sent to the external interface is the one defined in register field hdcp22reg_ctrl1.hdcp22_cd_ovr_val. Value After Reset: 0x0
2			Reserved for future use.
1	hdcp22_avmute_ovr_val	R/W	HDCP AV_MUTE override value, which is sent through the HDCP 2.2 external interface when hdcp22reg_ctrl1.hdcp22_avmute_ovr_en is set. Value After Reset: 0x0
0	hdcp22_avmute_ovr_en	R/W	HDCP 2.2 versus 1.4 avmute override enable 1'b0: The default 1'b0 value indicates that the AVMUTE sent to the external interface is the one configured through register fields fc_gcp.set_avmute and fc_gcp.clear_avmute. 1'b1: Although the GCP packet sends the set_avmute or clear_avmute as configured in register fc_gcp, the AV_MUTE sent to the external interface is the one defined in register field hdcp22reg_ctrl1.hdcp22_avmute_ovr_val. Value After Reset: 0x0

hdcp22reg_sts

Description: HDCP 2.2 Status Register
Size: 8 bits
Offset: 0x7908

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	hdcp_decrypted_sts	R	Value of HDCP 2.2 ist_hdcp_decrypted line. Provided for debug only

Bits	Name	Attr	Description
			Value After Reset: 0x0
2	hdcp22_switch_sts	R	HDCP 2.2 HDCP 2.2 versus 1.4 switch status after lock mechanism (hdcp22reg_ctrl.hdcp22_switch_lock, hdcp22reg_ctrl.hdcp22_ovr_en and hdcp22reg_ctrl.hdcp22_ovr_val). 1'b0: HDCP 1.4 selected 1'b1: HDCP 2.2 selected Value After Reset: 0x0
1	hdcp_avmute_sts	R	HDCP 2.2 AVMUTE external interface status. 1'b0: External HDCP used AVMUTE is clear 1'b1: External HDCP AVMUTE is set (audio/video should be muted) Value After Reset: 0x0
0	hdmi_hpd_sts	R	HDCP 2.2 HPD external interface status after lock mechanism (hdcp22reg_ctrl.hdcp22_switch_lock, hdcp22reg_ctrl.hdcp22_ovr_en and hdcp22reg_ctrl.hdcp22_ovr_val). 1'b0: Sink not detected (HPD line clear) 1'b1: Sink detected (HPD line set) Value After Reset: 0x0

hdcp22reg_mask

Description: HDCP 2.2 Interrupt Mask Register

Size: 8 bits

Offset: 0x790c

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	mask_hdcp_decrypted_chg	R/W	Active high interrupt mask to HDCP 2.2 decrypted value change interrupt status Value After Reset: 0x1
4	mask_hdcp_authentication_fail	R/W	Active high interrupt mask to HDCP 2.2 authentication fail interrupt status Value After Reset: 0x1
3	mask_hdcp_authenticated	R/W	Active high interrupt mask to HDCP 2.2 authenticated interrupt status Value After Reset: 0x1
2	mask_hdcp_authentication_lost	R/W	Active high interrupt mask to HDCP 2.2 authentication lost interrupt status Value After Reset: 0x1
1	mask_hdcp2_not_capable	R/W	Active high interrupt mask to HDCP 2.2 not capable rise interrupt status Value After Reset: 0x1
0	mask_hdcp2_capable	R/W	Active high interrupt mask to HDCP 2.2 capable rise interrupt status Value After Reset: 0x1

hdcp22reg_stat

Description: HDCP 2.2 interrupt Sticky Bit Status Register

Size: 8 bits

Offset: 0x790d

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	st_hdcp_decrypted_chg	R/W1C	HDCP 2.2 decrypted value change interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0
4	st_hdcp_authentication_fail	R/W1C	HDCP 2.2 authentication fail interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0
3	st_hdcp_authenticated	R/W1C	HDCP 2.2 authenticated interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0
2	st_hdcp_authentication_lost	R/W1C	HDCP 2.2 authentication lost interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0
1	st_hdcp2_not_capable	R/W1C	HDCP 2.2 not capable rise interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0
0	st_hdcp2_capable	R/W1C	HDCP 2.2 capable rise interrupt status sticky bit. Clear by Write 1 to this bit field Value After Reset: 0x0

hdcp22reg_mute

Description: HDCP 2.2 Interrupt Mute Vector

Size: 8 bits

Offset: 0x790e

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	mute_hdcp_decrypted_chg	R/W	Active high interrupt mute to HDCP 2.2 decrypted value change interrupt status Value After Reset: 0x1
4	mute_hdcp_authentication_fail	R/W	Active high interrupt mute to HDCP 2.2 authentication fail interrupt status Value After Reset: 0x1
3	mute_hdcp_authenticated	R/W	Active high interrupt mute to HDCP 2.2 authenticated interrupt status Value After Reset: 0x1
2	mute_hdcp_authentication_lost	R/W	Active high interrupt mute to HDCP 2.2 authentication lost interrupt status Value After Reset: 0x1
1	mute_hdcp2_not_capable	R/W	Active high interrupt mute to HDCP 2.2 not capable rise interrupt status

Bits	Name	Attr	Description
			Value After Reset: 0x1
0	mute_hdcp2_capable	R/W	Active high interrupt mute to HDCP 2.2 capable rise interrupt status Value After Reset: 0x1

CEC Registers

CEC Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
cec_ctrl	0x7d00	CEC Control Register This register handles the main control of the CEC initiator.
cec_mask	0x7d02	CEC Interrupt Mask Register This read/write register masks/unmasks the interrupt events. When the...
cec_addr_l	0x7d05	CEC Logical Address Register Low This register indicates the logical address(es) allocated to the...
cec_addr_h	0x7d06	CEC Logical Address Register High This register indicates the logical address(es) allocated to...
cec_tx_cnt	0x7d07	CEC TX Frame Size Register This register indicates the size of the frame in bytes (including header...
cec_rx_cnt	0x7d08	CEC RX Frame Size Register This register indicates the size of the frame in bytes (including header...
cec_tx_data[0:15]	0x7d10 + (i * 0x1)	CEC TX Data Register Array Address offset: i = 0 to 15 These registers (8 bits each) are the buffers...
cec_rx_data[0:15]	0x7d20 + (i * 0x1)	CEC RX Data Register Array Address offset: i =0 to 15 These registers (8 bit each) are the buffers...
cec_lock	0x7d30	CEC Buffer Lock Register
cec_wakeupctrl	0x7d31	CEC Wake-up Control Register After receiving a message in the CEC_RX_DATA1 (OPCODE) registers,...

cec_ctrl

Description: CEC Control Register

This register handles the main control of the CEC initiator.

Size: 8 bits

Offset: 0x7d00

Bits	Name	Attr	Description
7:5			Reserved for future use.
4	standby	R/W	1: CEC controller responds with a NACK to all messages and generates a wakeup status for opcode. It only responds with a NACK when the EOM is received. This means only the last block of a frame responds with NACK. The follower sends an ACK to the message when there is only one head block pointed to the follower, if the follower is in the standby mode. 0: CEC controller responds the ACK to all messages.

Bits	Name	Attr	Description
			Value After Reset: 0x0
3	bc_nack	R/W	1'b1: Set by software to NACK the received broadcast message. This bit holds until software resets. The broadcasts is answered with 1'b0, indicating the follower reject the message. 1'b0: Reset by software to ACK the received broadcast message. Value After Reset: 0x0
2:1	frame_typ	R/W	2'b00: Signal Free Time = 3-bit periods. Previous attempt to send frame is unsuccessful. 2'b01: Signal Free Time = 5-bit periods. New initiator wants to send a frame. 2'b10: Signal Free Time = 7-bit periods. Present initiator wants to send another frame immediately after its previous frame. (specification CEC 9.1). 2'b11: Illegal value. If software writes this value, hardware sets the value to the default 2'b01. Value After Reset: 0x1
0	send	R/W	1'b1: Set by software to trigger CEC sending a frame as an initiator. This bit keeps at 1'b1 while the transmission is going on. 1'b0: Reset to 1'b0 by hardware when the CEC transmission is done (no matter successful or failed). It can also work as an indicator checked by software to see whether the transmission is finished. Value After Reset: 0x0

cec_mask

Description: CEC Interrupt Mask Register

This read/write register masks/unmasks the interrupt events. When the bit is set to 1 (masked), the corresponding event does not trigger an interrupt signal at the system interface. When the bit is reset to 0, the interrupt event is unmasked.

Size: 8 bits

Offset: 0x7d02

Bits	Name	Attr	Description
7			Reserved for future use.
6	wakeup	R/W	Follower wake-up signal mask Value After Reset: 0x0
5	error_flow	R/W	An error is notified by a follower. Abnormal logic data bit error (for follower) Value After Reset: 0x0
4	error_initiator	R/W	An error is detected on a CEC line (for initiator only). Value After Reset: 0x0
3	arb_lost	R/W	The initiator losses the CEC line arbitration to a second initiator. (specification CEC 9) Value After Reset: 0x0

Bits	Name	Attr	Description
2	nack	R/W	A frame is not acknowledged in a directly addressed message. Or a frame is negatively acknowledged in a broadcast message (for initiator only) Value After Reset: 0x0
1	eom	R/W	EOM is detected so that the received data is ready in the receiver data buffer (for follower only) Value After Reset: 0x0
0	done	R/W	The current transmission is successful (for initiator only) Value After Reset: 0x0

cec_addr_l

Description: CEC Logical Address Register Low

This register indicates the logical address(es) allocated to the CEC device.

This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

Size: 8 bits

Offset: 0x7d05

Bits	Name	Attr	Description
7	cec_addr_l_7	R/W	Logical address 7 - Tuner 3 Value After Reset: 0x0
6	cec_addr_l_6	R/W	Logical address 6 - Tuner 2 Value After Reset: 0x0
5	cec_addr_l_5	R/W	Logical address 5 - Audio System Value After Reset: 0x0
4	cec_addr_l_4	R/W	Logical address 4 - Playback Device 1 Value After Reset: 0x0
3	cec_addr_l_3	R/W	Logical address 3 - Tuner 1 Value After Reset: 0x0
2	cec_addr_l_2	R/W	Logical address 2 - Recording Device 2 Value After Reset: 0x0
1	cec_addr_l_1	R/W	Logical address 1 - Recording Device 1 Value After Reset: 0x0
0	cec_addr_l_0	R/W	Logical address 0 - Device TV Value After Reset: 0x0

cec_addr_h

Description: CEC Logical Address Register High

This register indicates the logical address(es) allocated to the CEC device.

This register is written by software when the logical allocation is finished. Bit value 1 means the corresponding logical address is allocated to this device. Bit value 0 means the corresponding logical address is not allocated to this device.

Size: 8 bits

Offset: 0x7d06

Bits	Name	Attr	Description
7	cec_addr_h_7	R/W	Logical address 15 - Unregistered (as initiator address), Broadcast (as destination address) Value After Reset: 0x1

6	cec_addr_h_6	R/W	Logical address 14 - Free use Value After Reset: 0x0
5	cec_addr_h_5	R/W	Logical address 13 - Reserved Value After Reset: 0x0
4	cec_addr_h_4	R/W	Logical address 12 - Reserved Value After Reset: 0x0
3	cec_addr_h_3	R/W	Logical address 11 - Playback Device 3 Value After Reset: 0x0
2	cec_addr_h_2	R/W	Logical address 10 - Tuner 4 Value After Reset: 0x0
1	cec_addr_h_1	R/W	Logical address 9 - Playback Device 3 Value After Reset: 0x0
0	cec_addr_h_0	R/W	Logical address 8 - Playback Device 2 Value After Reset: 0x0

cec_tx_cnt

Description: CEC TX Frame Size Register

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the transmitter data buffer.

Note: When the value is zero, the CEC controller ignores the send command triggered by software. When the transmission is done (no matter success or not), the current value is held until it is overwritten by software.

Size: 8 bits

Offset: 0x7d07

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	cec_tx_cnt	R/W	CEC Transmitter Counter register 5'd0: No data needs to be transmitted 5'd1: Frame size is 1 byte 5'd16: Frame size is 16 bytes Value After Reset: 0x0

cec_rx_cnt

Description: CEC RX Frame Size Register

This register indicates the size of the frame in bytes (including header and data blocks), which are available in the receiver data buffer.

Note: Only after the whole receiving process is finished successfully, the counter is refreshed to the value which indicates the total number of data bytes in the Receiver Data Register.

Size: 8 bits

Offset: 0x7d08

Bits	Name	Attr	Description
7:5			Reserved for future use.
4:0	cec_rx_cnt	R	CEC Receiver Counter register: 5'd0: No data received 5'd1: 1-byte data is received 5'd16: 16-byte data is received Value After Reset: 0x0

cec_tx_data[0:15]

Description: CEC TX Data Register Array Address offset: i = 0 to 15

These registers (8 bits each) are the buffers used for storing the data waiting for transmission (including header and data blocks).

Size: 8 bits

Offset: 0x7d10 + (i * 0x1)

Bits	Name	Attr	Description
7:0	databyte	R/W	Data byte[x], where x is 0 to 15 Value After Reset: 0x0

cec_rx_data[0:15]

Description: CEC RX Data Register Array Address offset: i =0 to 15

These registers (8 bit each) are the buffers used for storing the received data (including header and data blocks).

Size: 8 bits

Offset: 0x7d20 + (i * 0x1)

Bits	Name	Attr	Description
7:0	databyte	R	Data byte[x], where x is 0 to 15 Value After Reset: 0x0

cec_lock

Description: CEC Buffer Lock Register

Size: 8 bits

Offset: 0x7d30

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	locked_buffer	R/W	When a frame is received, this bit would be active. The CEC controller answers to all the messages with NACK until the CPU writes it to '0'. Value After Reset: 0x0

cec_wakeupctrl

Description: CEC Wake-up Control Register

After receiving a message in the CEC_RX_DATA1 (OPCODE) registers, the CEC engine verifies the message opcode[7:0] against one of the previously defined values to generate the wake-up status:

Wakeupstatus is 1 when:

received opcode is 0x04 and opcode0x04en is 1 or

received opcode is 0x0D and opcode0x0Den is 1 or

received opcode is 0x41 and opcode0x41en is 1 or

received opcode is 0x42 and opcode0x42en is 1 or

received opcode is 0x44 and opcode0x44en is 1 or

received opcode is 0x70 and opcode0x70en is 1 or

received opcode is 0x82 and opcode0x82en is 1 or

received opcode is 0x86 and opcode0x86en is 1

Wakeupstatus is 0 when none of the previous conditions are true.

This formula means that the wake-up status (on CEC_STAT[6] register) is only '1' if the opcode[7:0] received is equal to one of the defined values and the corresponding enable bit of that defined value is set to '1'.

Size: 8 bits

Offset: 0x7d31

Bits	Name	Attr	Description
7	opcode0x86en	R/W	OPCODE 0x86 wake up enable Value After Reset: 0x1
6	opcode0x82en	R/W	OPCODE 0x82 wake up enable

Bits	Name	Attr	Description
			Value After Reset: 0x1
5	opcode0x70en	R/W	OPCODE 0x70 wake up enable Value After Reset: 0x1
4	opcode0x44en	R/W	OPCODE 0x44 wake up enable Value After Reset: 0x1
3	opcode0x42en	R/W	OPCODE 0x42 wake up enable Value After Reset: 0x1
2	opcode0x41en	R/W	OPCODE 0x41 wake up enable Value After Reset: 0x1
1	opcode0x0Den	R/W	OPCODE 0x0D wake up enable Value After Reset: 0x1
0	opcode0x04en	R/W	OPCODE 0x04 wake up enable Value After Reset: 0x1

EDDC Registers

E-DDC Registers. Follow the link for the register to see a detailed description of the register.

Register	Offset	Description
i2cm_slave	0x7e00	I2C DDC Slave address Configuration Register
i2cm_address	0x7e01	I2C DDC Address Configuration Register
i2cm_datao	0x7e02	I2C DDC Data Write Register
i2cm_datai	0x7e03	I2C DDC Data read Register
i2cm_operation	0x7e04	I2C DDC RD/RD_EXT/WR Operation Register Read and write operation request. This register can only...
i2cm_int	0x7e05	I2C DDC Done Interrupt Register This register configures the I2C master interrupts.
i2cm_ctlint	0x7e06	I2C DDC error Interrupt Register This register configures the I2C master arbitration lost and not...
i2cm_div	0x7e07	I2C DDC Speed Control Register This register configures the division relation between master and...
i2cm_segaddr	0x7e08	I2C DDC Segment Address Configuration Register This register configures the segment address for...
i2cm_softrstz	0x7e09	I2C DDC Software Reset Control Register This register resets the I2C master.
i2cm_segptr	0x7e0a	I2C DDC Segment Pointer Register This register configures the segment pointer for extended RD/WR...
i2cm_ss_scl_hcnt_1_addr	0x7e0b	I2C DDC Slow Speed SCL High Level Control Register 1
i2cm_ss_scl_hcnt_0_addr	0x7e0c	I2C DDC Slow Speed SCL High Level Control Register 0
i2cm_ss_scl_lcnt_1_addr	0x7e0d	I2C DDC Slow Speed SCL Low Level Control Register 1
i2cm_ss_scl_lcnt_0_addr	0x7e0e	I2C DDC Slow Speed SCL Low Level Control Register 0
i2cm_fs_scl_hcnt_1_addr	0x7e0f	I2C DDC Fast Speed SCL High Level Control Register 1
i2cm_fs_scl_hcnt_0_addr	0x7e10	I2C DDC Fast Speed SCL High Level Control Register 0
i2cm_fs_scl_lcnt_1_addr	0x7e11	I2C DDC Fast Speed SCL Low Level Control Register 1
i2cm_fs_scl_lcnt_0_addr	0x7e12	I2C DDC Fast Speed SCL Low Level Control Register 0

Register	Offset	Description
i2cm_sda_hold	0x7e13	I2C DDC SDA Hold Register
i2cm_scdc_read_update	0x7e14	SCDC Control Register This register configures the SCDC update status read through the I2C master...
i2cm_read_buff0	0x7e20	I2C Master Sequential Read Buffer Register 0
i2cm_read_buff1	0x7e21	I2C Master Sequential Read Buffer Register 1

Registers for Address Block: EDDC (Continued)

Register	Offset	Description
i2cm_read_buff2	0x7e22	I2C Master Sequential Read Buffer Register 2
i2cm_read_buff3	0x7e23	I2C Master Sequential Read Buffer Register 3
i2cm_read_buff4	0x7e24	I2C Master Sequential Read Buffer Register 4
i2cm_read_buff5	0x7e25	I2C Master Sequential Read Buffer Register 5
i2cm_read_buff6	0x7e26	I2C Master Sequential Read Buffer Register 6
i2cm_read_buff7	0x7e27	I2C Master Sequential Read Buffer Register 7
i2cm_scdc_update0	0x7e30	I2C SCDC Read Update Register 0
i2cm_scdc_update1	0x7e31	I2C SCDC Read Update Register 1

i2cm_slave

Description: I2C DDC Slave address Configuration Register

Size: 8 bits

Offset: 0x7e00

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	slaveaddr	R/W	Slave address to be sent during read and write normal operations. Value After Reset: 0x0

i2cm_address

Description: I2C DDC Address Configuration Register

Size: 8 bits

Offset: 0x7e01

Bits	Name	Attr	Description
7:0	address	R/W	Register address for read and write operations Value After Reset: 0x0

i2cm_datao

Description: I2C DDC Data Write Register

Size: 8 bits

Offset: 0x7e02

Bits	Name	Attr	Description
7:0	datao	R/W	Data to be written on register pointed by address[7:0]. Value After Reset: 0x0

i2cm_datai

Description: I2C DDC Data read Register

Size: 8 bits
Offset: 0x7e03

Bits	Name	Attr	Description
7:0	datai	R	Data read from register pointed by address[7:0]. Value After Reset: 0x0

i2cm_operation

Description: I2C DDC RD/RD_EXT/WR Operation Register
Read and write operation request. This register can only be written; reading this register always results in 00h. Writing 1'b1 simultaneously to rd, rd_ext and wr requests is considered as a read (rd) request.
Size: 8 bits
Offset: 0x7e04

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	busclear	W	Bus clear operation request. Value After Reset: 0x0
4	wr	W	Single byte write operation request. Value After Reset: 0x0
3	rd8_ext	W	Extended sequential read operation request. Eight bytes are read starting at the address defined in register field i2cm_address.address and stored in registers i2cm_read_buffx. Value After Reset: 0x0
2	rd8	W	Sequential read operation request. Eight bytes are read starting at the address defined in the i2cm_address.address register field and stored in the i2cm_read_buffx registers. Value After Reset: 0x0
1	rd_ext	W	After writing 1'b1 to rd_ext bit a extended data read operation is started (E-DDC read operation). Value After Reset: 0x0
0	rd	W	Single byte read operation request Value After Reset: 0x0

i2cm_int

Description: I2C DDC Done Interrupt Register This register configures the I2C master interrupts.
Size: 8 bits
Offset: 0x7e05

Bits	Name	Attr	Description
7			Reserved for future use.
6	read_req_mask	R/W	Read request interruption mask signal. Value After Reset: 0x1
5:3			Reserved for future use.
2	done_mask	R/W	Done interrupt mask signal. Value After Reset: 0x0
1:0			Reserved for future use.

i2cm_ctlint

Description: I2C DDC error Interrupt Register

This register configures the I2C master arbitration lost and not acknowledge error interrupts.

Size: 8 bits

Offset: 0x7e06

Bits	Name	Attr	Description
7			Reserved for future use.
6	nack_mask	R/W	Not acknowledge error interrupt mask signal. Value After Reset: 0x0
5:3			Reserved for future use.
2	arbitration_mask	R/W	Arbitration error interrupt mask signal. Value After Reset: 0x0
1:0			Reserved for future use.

i2cm_div

Description: I2C DDC Speed Control Register

This register configures the division relation between master and scl clock.

Size: 8 bits

Offset: 0x7e07

Bits	Name	Attr	Description
7:4			Reserved for future use.
3	fast_std_mode	R/W	Sets the I2C Master to work in Fast Mode or Standard Mode: 1: Fast Mode 0: Standard Mode Value After Reset: 0x1
2:0	spare	R/W	Reserved as "spare" bit with no associated functionality. Value After Reset: 0x3

i2cm_segaddr

Description: I2C DDC Segment Address Configuration Register

This register configures the segment address for extended R/W destination and is used for EDID reading operations, particularly for the Extended Data Read Operation for Enhanced DDC.

Size: 8 bits

Offset: 0x7e08

Bits	Name	Attr	Description
7			Reserved for future use.
6:0	seg_addr	R/W	I2C DDC Segment Address Configuration Register Value After Reset: 0x0

i2cm_softrstz

Description: I2C DDC Software Reset Control Register This register resets the I2C master.

Size: 8 bits

Offset: 0x7e09

Bits	Name	Attr	Description
7:1			Reserved for future use.
0	i2c_softrstz	R/W	I2C Master Software Reset. Active by writing a zero and auto cleared to one in the following cycle. Value After Reset: 0x1

i2cm_segptr

Description: I2C DDC Segment Pointer Register

This register configures the segment pointer for extended RD/WR request.

Size: 8 bits

Offset: 0x7e0a

Bits	Name	Attr	Description
7:0	segptr	R/W	I2C DDC Segment Pointer Register Value After Reset: 0x0

i2cm_ss_scl_hcnt_1_addr

Description: I2C DDC Slow Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x7e0b

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt1	R/W	I2C DDC Slow Speed SCL High Level Control Register 1 Value After Reset: 0x0

i2cm_ss_scl_hcnt_0_addr

Description: I2C DDC Slow Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x7e0c

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_hcnt0	R/W	I2C DDC Slow Speed SCL High Level Control Register 0 Value After Reset: 0x6c

i2cm_ss_scl_lcnt_1_addr

Description: I2C DDC Slow Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x7e0d

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt1	R/W	I2C DDC Slow Speed SCL Low Level Control Register 1 Value After Reset: 0x0

i2cm_ss_scl_lcnt_0_addr

Description: I2C DDC Slow Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x7e0e

Bits	Name	Attr	Description
7:0	i2cmp_ss_scl_lcnt0	R/W	I2C DDC Slow Speed SCL Low Level Control Register 0 Value After Reset: 0x7f

i2cm_fs_scl_hcnt_1_addr

Description: I2C DDC Fast Speed SCL High Level Control Register 1

Size: 8 bits

Offset: 0x7e0f

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt1	R/W	I2C DDC Fast Speed SCL High Level Control Register 1 Value After Reset: 0x0

i2cm_fs_scl_hcnt_0_addr

Description: I2C DDC Fast Speed SCL High Level Control Register 0

Size: 8 bits

Offset: 0x7e10

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_hcnt0	R/W	I2C DDC Fast Speed SCL High Level Control Register 0 Value After Reset: 0x11

i2cm_fs_scl_lcnt_1_addr

Description: I2C DDC Fast Speed SCL Low Level Control Register 1

Size: 8 bits

Offset: 0x7e11

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt1	R/W	I2C DDC Fast Speed SCL Low Level Control Register 1 Value After Reset: 0x0

i2cm_fs_scl_lcnt_0_addr

Description: I2C DDC Fast Speed SCL Low Level Control Register 0

Size: 8 bits

Offset: 0x7e12

Bits	Name	Attr	Description
7:0	i2cmp_fs_scl_lcnt0	R/W	I2C DDC Fast Speed SCL Low Level Control Register 0 Value After Reset: 0x24

i2cm_sda_hold

Description: I2C DDC SDA Hold Register

Size: 8 bits

Offset: 0x7e13

Bits	Name	Attr	Description
7:0	osda_hold	R/W	Defines the number of SFR clock cycles to meet tHD;DAT (300 ns) osda_hold = round_to_high_integer (300 ns / (1 / isfrclk_frequency)) Value After Reset: 0x9

i2cm_scdc_read_update

Description: SCDC Control Register

This register configures the SCDC update status read through the I2C master interface.
Size: 8 bits
Offset: 0x7e14

Bits	Name	Attr	Description
7:6			Reserved for future use.
5	updtrd_vsyncpoll_en	R/W	Update read polling enabled. When active (1'b1), an SCDC Update Read is performed at the fall of the active edge of the vertical sync pulse. Value After Reset: 0x0
4	read_request_en	R/W	Read request enabled. When active (1'b1) an SCDC Update Read shall be performed whenever a SCDC read request is detected. Value After Reset: 0x0
3:1			Reserved for future use.
0	read_update	W	When set to 1'b1, a SCDC Update Read is performed and the read data loaded into registers i2cm_scdc_update0 and i2cm_scdc_update1. Value After Reset: 0x0

i2cm_read_buff0
Description: I2C Master Sequential Read Buffer Register 0
Size: 8 bits
Offset: 0x7e20

Bits	Name	Attr	Description
7:0	i2cm_read_buff0	R	Byte 0 of a I2C read buffer sequential read (from address i2cm_address) Value After Reset: 0x0

i2cm_read_buff1
Description: I2C Master Sequential Read Buffer Register 1
Size: 8 bits
Offset: 0x7e21

Bits	Name	Attr	Description
7:0	i2cm_read_buff1	R	Byte 1 of a I2C read buffer sequential read (from address i2cm_address+1) Value After Reset: 0x0

i2cm_read_buff2
Description: I2C Master Sequential Read Buffer Register 2
Size: 8 bits
Offset: 0x7e22

Bits	Name	Attr	Description
7:0	i2cm_read_buff2	R	Byte 2 of a I2C read buffer sequential read (from address i2cm_address+2) Value After Reset: 0x0

i2cm_read_buff3

Description: I2C Master Sequential Read Buffer Register 3

Size: 8 bits

Offset: 0x7e23

Bits	Name	Attr	Description
7:0	i2cm_read_buff3	R	Byte 3 of a I2C read buffer sequential read (from address i2cm_address+3) Value After Reset: 0x0

i2cm_read_buff4

Description: I2C Master Sequential Read Buffer Register 4

Size: 8 bits

Offset: 0x7e24

Bits	Name	Attr	Description
7:0	i2cm_read_buff4	R	Byte 4 of a I2C read buffer sequential read (from address i2cm_address+4) Value After Reset: 0x0

i2cm_read_buff5

Description: I2C Master Sequential Read Buffer Register 5

Size: 8 bits

Offset: 0x7e25

Bits	Name	Attr	Description
7:0	i2cm_read_buff5	R	Byte 5 of a I2C read buffer sequential read (from address i2cm_address+5) Value After Reset: 0x0

i2cm_read_buff6

Description: I2C Master Sequential Read Buffer Register 6

Size: 8 bits

Offset: 0x7e26

Bits	Name	Attr	Description
7:0	i2cm_read_buff6	R	Byte 6 of a I2C read buffer sequential read (from address i2cm_address+6) Value After Reset: 0x0

i2cm_read_buff7

Description: I2C Master Sequential Read Buffer Register 7

Size: 8 bits

Offset: 0x7e27

Bits	Name	Attr	Description
7:0	i2cm_read_buff7	R	Byte 7 of a I2C read buffer sequential read (from address i2cm_address+7) Value After Reset: 0x0

i2cm_scdc_update0

Description: I2C SCDC Read Update Register 0
Size: 8 bits
Offset: 0x7e30

Bits	Name	Attr	Description
7:0	i2cm_scdc_update0	R	Byte 0 of a SCDC I2C update sequential read Value After Reset: 0x0

i2cm_scdc_update1
Description: I2C SCDC Read Update Register 1
Size: 8 bits
Offset: 0x7e31

Bits	Name	Attr	Description
7:0	i2cm_scdc_update1	R	Byte 1 of a SCDC I2C update sequential read Value After Reset: 0x0

32.5.2 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Just do the step, reset the HDMI TX.

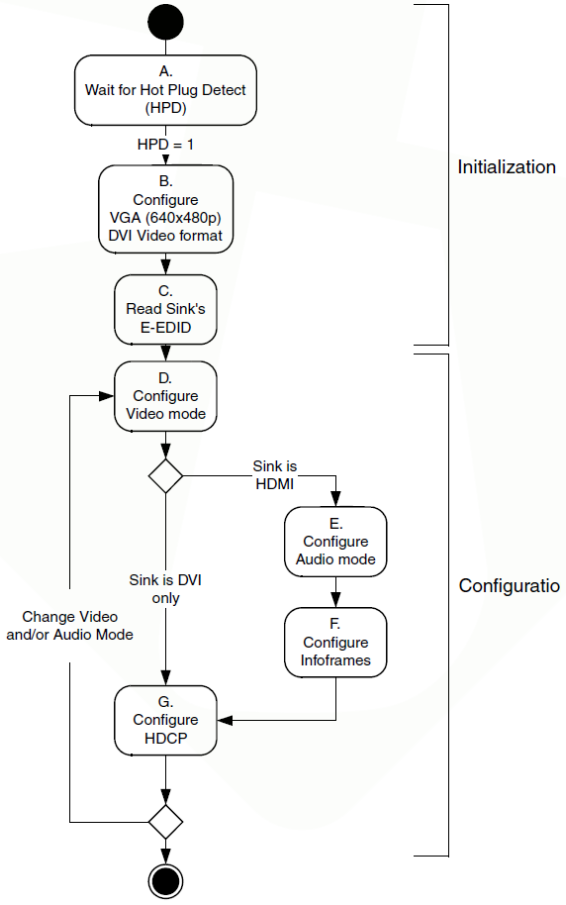


Fig. 32-5 HDMI programming sequence

32.5.3 Step A: Hot Plug Detection

The Hot Plug Detect information notifies the HDMI TX controller when the cable is plugged into a Sink (Receiver) device and when the device is ready to receive video content.

The Hot-Plug Detection indication is a +5V signal on the HDMI cable. The HDMI TX PHY performs level-shifting to a low-level digital signal.

For this step, registers are used on the HDMI TX PHY.

To check the Hot Plug Detect status, the following steps have to be followed:

1. Power-on the HDMI TX PHY HPD Detector. Write 1'b1 in the phy_conf0.enhpdrxsense bit field register.

2. Check the HPD status bit.

- Read the phy_stat0.HPD bit field register.
  - If HPD = 0, the Hot Plug signal is low (no Sink (Receiver) detected).
  - If HPD = 1, the Hot Plug signal is high (Sink (Receiver) detected).

Note: Some receivers may turn off the Hot-Plug Detect indication when the HDMI input is not selected, even when the cable is plugged in.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

32.5.4 Step B: Configure Video Mode

Once a receiver is detected, it is necessary to start sending video content in DVI mode. Because some receivers need to receive a video signal (TMDS clock more precisely), it is important to clock all the digital logic and be able to reply on an E-EDID read access (Step C). Following flow is a configuration example of VGA (640x480p).

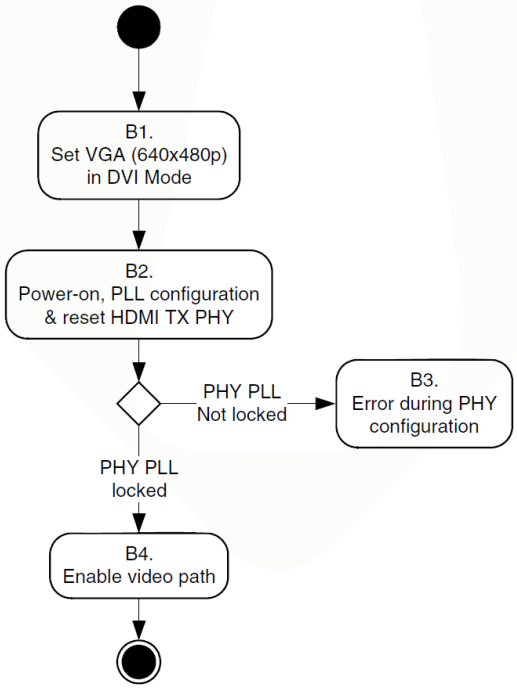


Fig. 32-6 Configure Video Mode

The VGA (640x480p) mode is mandatory for all receivers and transmitters, because it requires the lowest data rate possible on the HDMI specification.

1. Set VGA (640x480p) in DVI mode.

- To select the Video Mapping input RGB444, 8-bits per color components (24-bits RGB), write "1" in the tx_invid0.video_mapping register.
- To configure VGA timing information (CEA mode 1):
  - Write "0" in the fc_invidconf.vsync_in_polarity register.
  - Write "0" in the fc_invidconf.hsync_in_polarity register.
  - Write "1" in the fc_invidconf.de_in_polarity register.
  - Write "0" in the fc_invidconf.r_v_blank_in_osc register.
  - Write "0" in the fc_invidconf.in_I_P register.
  - 640 H active pixels: 0x280
    - Write "2" in the fc_inhactiv1.H_in_activ register.
    - Write "0x80" in the fc_inhactiv0.H_in_activ register.
  - 480 V active pixels: 0x1E0
    - Write "1" in the fc_invactiv1.V_in_activ register.
    - Write "0xE0" in the fc_invactiv0.V_in_activ register.
  - 160 H blanking pixels: 0xA0

    Write "0xA0" in thefc_inhblank0.H_in_blank.
  - 45 V blanking pixels: 0x2D

    Write "0x2D" in the fc_invblank.V_in_blank register.
  - 16 Sync offset: 0x10

    Write "0x10" in the fc_hsyncindelay0.H_in_delay register.
  - 10 Vsync offset: 0x0A

    Write "0x0A" in the fc_vsyncindelay0.V_in_delay register.
  - 96 HSync pulse width: 0x60

    Write "0x60" in the fc_hsyncinwidth0.H_in_width register.
  - 2 VSync pulse width: 0x02

    Write "0x02" in the fc_vsyncinwidth0.V_in_width register.
- To select the HDMI mode:

  Write "1" in the fc_invidconf.DVI_modez register.

2. Power-on, configure the PLL, and reset the HDMI TX PHY.

The HDMI TX PHY has an internal PLL that generates TMDS clock from Pixel clock input. The

power-on sequence and PLL configuration is part of the HDMI TX PHY documentation.

To configure HDMI TX PHY, you are generally required to:

a. Place the PHY in reset by writing 0x01 in the mc_phyrstz register.

b. Write the desired color depth and the pixel repetition in the vp_pr_cd register.

c. After a PHY-dependent time, it is required to lift the reset by writing 0x00 to the mc_phyrstz register.

d. Clear the pddq, txpwron configuration bits, define the data enable polarity and clear the interface control selection by writing these values in the phy_cfg0 register.

e. Set the PHY slave address by writing 0x69 in the phy_i2cm_slave register.

f. You are required to look up the configuration for your intended video mode and write those values on the PHY I2C interface. The baseline flow to write to the PHY through the I2C interface is:

- Write register address in the phy_i2cm_address register.
- Write data in the phy_i2cm_datao_1 (MSB, [15:8]) and phy_i2cm_datao_0 (LSB, [7:0]) registers.
- Initialize the write operation by writing 8'h10 in the phy_i2cm_operation register.
- Wait for a done interruption from the I2C master.

g. After all of the required PHY I2C registers have been configured, you now need to set the txpwron bit in the PHY_CONF0 register, leaving the remaining bits in the state defined previously.

3. Handle errors during PHY configuration.

If the PHY is not correctly configured, the PLL does not lock and no activity can happen on the HDMI output.

4. Enable the video path.

a. Set default parameters in the HDMI TX Controller, Control period duration: 12: 0x0C.

Write "0x0C" in the fc_ctrldur.ctrlperiodduration bit field register.

b. Set default parameters in the HDMI TX Controller, Extended Control period duration: 32: 0x20.

Write "0x20" in the fc_exctrldur.exctrlperiodduration bit field register.

c. Set default parameters in the HDMI TX Controller, Max spacing between extended Control period duration: 1: 0x1.

Write "0x01" in the fc_exctrlspac.exctrlperiodspacing bit field register.

d. Set default parameters in the HDMI TX Controller, Preamble filters to fill TMDS data channels.

- Write "0x0B" in the fc_ch0pream.ch0_preamble_filter bit field register.
- Write "0x16" in the fc_ch1pream.ch1_preamble_filter bit field register.
- Write "0x21" in the fc_ch2pream.ch2_preamble_filter bit field register.

e. Enable pixel clock data path:

Write "0" in the mc_clkdis.pixelclk_disable bit field register.

f. Enable TMDS clock data path:

i. Write "0" in the mc_clkdis.tmdsclk_disable bit field register.

ii. Re-Write the VSync pulse width in the fc_vsyncinwidth0.V_in_width bit field register.

After these steps, it is expected to observe a video picture in VGA mode on the receiver side.

32.5.5 Step C: Reading E-EDID

The E-EDID is a memory present on the receiver side. It contains the video and audio capabilities of the receiver. It is important to read this information and parse it in order to configure the transmitter system in accordance to what the receiver supports. The E-EDID is read using the E-DDC channel present on the HDMI cable.

The E-DDC channel protocol is based on I2C, with segment pointer addressing extension (such as, Extended Read). The hdmi tx controller has an I2C Master controller for this purpose.

1. To perform a "normal" read operation

- Set I2C slave address.

  Write i2cm_slave.slaveaddr[6:0] bit field register.

- Set I2C register address.

  Write i2cm_address.address[7:0] bit field register.

- Activate Read operation.

  Write "1" in the i2cm_operation.rd bit field register.

- Wait for interruption.

  Wait for the ii2cmasterdone interrupt in the ih_i2cm_stat0 register.

- Read data result.

  Read data in the i2cm_datai.datai[7:0] bit field.

2. To perform an E-DDC extended read operation

- Set I2C slave address.

  Write i2cm_slave.slaveaddr[6:0] bit field register.

- Set I2C segment address.

  Write the i2cm_segaddr.seg_addr bit field register.

- Set I2C segment pointer.

  Write i2cm_segptr.segptr bit field register.

- Activate Read operation.

Write "1"in the i2cm_operation.rd_ext bit field register.

- Wait for interruption.

  Wait for the ii2cmasterdone interrupt in the ih_i2cm_stat0 register.

- Read data result.

  Read data in the i2cm_datai.datai[7:0] bit field register.

32.5.6 Step D: Configure Video Mode

The video mode selected has to match what is supported by the source of the video (Transmitter side) and the sink of the video (receiver side). The video capabilities of the receiver are extracted from the E-EDID information (refer to step C).

To configure any video mode, a similar procedure in step B has to be followed.

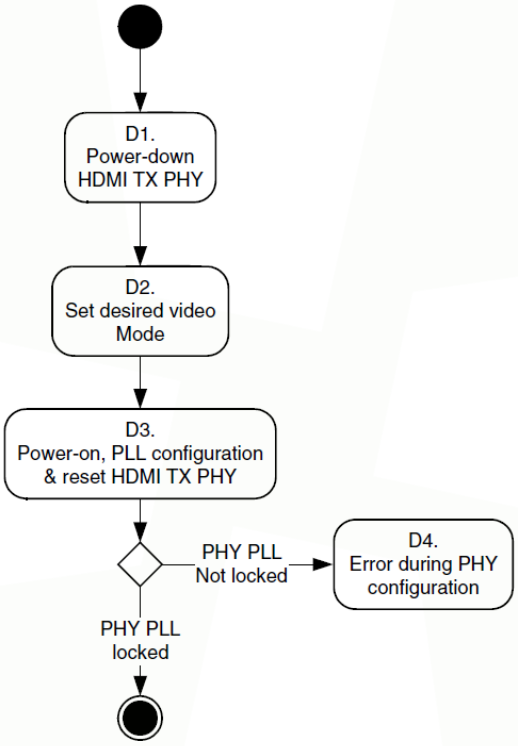


Fig. 32-7 Video Mode Configuration

Before any change is made on the video modes, is it recommended you power-down the HDMI TX PHY to avoid any unexpected behavior on the receiver side.

1. Power-down HDMI TX PHY Detector

- Place the PHY in reset by writing 0x01 in the mc_phyrstz register.
- Then proceed to set SVSRET_MODEZ to 1'b0, PDDQ to 1'b1 and TX_PWRON to 1b0, by writing 2'h12 in the phy_conf0 register.

2. Set desired video mode.

- To select the Video Mapping input mode (RGB444, YCC444, YCC422). Write the video code in the tx_invid0.video_mapping bit field register.
- Set video timing information configuration:
  - Write the fc_invidconf.vsync_in_polarity register.
  - Write the fc_invidconf.hsync_in_polarity register.

- Write the fc_invidconf.de_in_polarity register.
- Write the fc_invidconf.r_v_blank_in_osc register.
- Write the fc_invidconf.in_I_P register.
- H active pixels

  - Write the fc_inhactiv1.H_in_activ register.

  - Write the fc_inhactiv0.H_in_activ register.

- V active pixels

  If the desired video mode is 3D, the fc_invact_2d_1, fc_invact_2d_0, and all registers in the following table must be written.

Table 32-5 HDMI 3D structure table

3D STRUCTURE	fc_actspc_hdlr_cfg	
	fc_actspc_hdlr_tgl	fc_actspc_hdlr_en
Frame Packing for interlaced format	1	1
Frame Packing for progressive format	0	1
Field alternative	0	0
Line Alternative	0	0
Side-by-Side(FULL)	0	0
L+depth	0	1
L+depth+graphics +graphics-depth	0	1
Top-and-Bottom	0	0
Reserved for Future Use	0	0
Side-by-Side(FULL)	0	0
Reserved for Future Use	0	0
Not in use	0	0

  - Write the fc_invact_2D_1 register with the 2D Vertical video active[11:8].

  - Write the fc_invact_2D_0 register with the 2D Vertical video active[7:0]

  The following registers must always be written with the full V active of the desired video

  regardless of the type of the video mode.

  - Write the fc_invactiv1.V_in_activ register.

  - Write the fc_invactiv0.V_in_activ register.

  ■ H blanking pixels

  Write the fc_inhblank0.H_in_blank register.

■ V blanking pixels

Write the fc_invblank.V_in_blank register.

■ HSync offset

Write the fc_hsyncindelay0.H_in_delay register.

■ VSync offset

Write the fc_vsyncindelay0.V_in_delay register.

■ HSync pulse width

Write the fc_hsyncinwidth0.H_in_width register.

■ VSync pulse width

Write the fc_vsyncinwidth0.V_in_width register.

- Select DVI or HDMI mode:

  Write "1" for HDMI in the fc_invidconf.DVI_modez bit field register.

3. Power-on, configure the PLL, and reset the HDMI TX PHY (same as Step B2).

The HDMI TX PHY has an internal PLL that generates TMDS clock from Pixel clock input. All the power-on sequence and PLL configuration is part of the HDMI TX PHY documentation.

The HDMI TX Controller provides all registers necessary for the PHY sequence implementation, which are presented in the "HDMI PHY Registers".

- Place the PHY in reset by writing 0x01 in the mc_phyrstz register.
- Write in the desired color depth and the pixel repetition in the vp_pr_cd register.
- After a PHY-dependent time, it is required to lift the reset by writing 0x00 to the mc_phyrstz register.
- Clear the pddq, txpwron configuration bits, define the data enable polarity and clear the interface control selection by writing these values in the phy_conf0 register.
- Set the PHY slave address by writing 0x69 to the phy_i2cm_slave register.
- Look up the configuration for your intended video mode and write those values on the PHY I2C interface. The baseline flow to write in the PHY through the I2C interface is

  ■ Write the register address in the phy_i2cm_address register.

  ■ Write data into phy_i2cm_datao_1 (MSB, [7:0]) and phy_i2cm_datao_0 (LSB, [7:0]) registers.

  ■ Initialize the write operation by writing 8'h10 in the phy_i2cm_operation register.

  ■ Wait for a done interrupt signal I2Cmphydone which in register ih_i2cmphy_stat0 bit 1 from the I2C master.

- After all of the required PHY I2C registers have been configured, you now need to set the phy_conf0.txpwron register, leaving the remaining bits in the state defined previously.

32.5.7 Step E: Audio input configuration

HDMI transmitter audio support either SPDIF or four channel I2S input. SPDIF input

supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 48K.

- Configure Audio Input Format with I2S Steps:
  - ■ Select I2S input.
  Write "1" in the aud_conf0.i2s_select bit field register.
  - ■ Enable I2S inputs:
  Write "1" in the aud_conf0.i2s_in_en[3:0] bit field register.
  - ■ Set I2S Mode [Standard | Right-justified | Left-justified | Burst1 | Burst2]:
  Write the aud_conf1.i2s_mode[2:0] bit field register.
  - ■ Set I2S data width [16 bits up to 24 bits]:
  Write the aud_conf1.i2s_width[4:0] bit field.
- Configure Audio Input Format with SPDIF Steps:
  - ■ Select SPDIF input.
  Write "0" in the aud_conf0.i2s_select bit field register.
  - ■ Set S/PDIF Linear-PCM or Non-Linear PCM audio samples:
  Write the aud_spdif1.setnlpcm bit field register.
  - ■ Set SPDIF data width [16 bits up to 24 bits]:
  Write the aud_spdif1.spdif_width[4:0] bit field.
- Configure Audio Parameters Steps:
  - ■ Set Audio input frequency clock FS ratio factor [128 Fs | 256 Fs |512 Fs]:
  Write the aud_inputclkfs.lfsfactor bit field register.
  - ■ Set Audio fixed N factor for Audio Clock Regeneration. This factor depends on the audio sampling rate and video mode.
  Write the aud_n1.audN, aud_n2.audN, and aud_n3.audN bit field registers.
  - ■ Set Audio CTS factor for Audio Clock Regeneration. This factor can be generated automatically or manually.
  For Automatic CTS generation
  Write "0" on the bit field "CTS_manual", Register 0x3205: AUD_CTS3
  For Manual CTS setting
  Write "1" in the aud_cts3.CTS_manual register bit field.
  Write the aud_cts1.audCTS, aud_cts2.audCTS, aud_cts3.audCTS bit field registers.
  - ■ Enable Audio sampler block:
  Write "0" in the mc_clkdis.audclk_disable bit field register.

32.5.8 Step F: Configure Infoframes

This step is only relevant when the HDMI TX controller is configured in HDMI mode (refer to "Step D: Configure Video Mode"). In DVI mode, no Infoframes are transmitted. The configuration of the Infoframes is essential to correctly inform the HDMI Receiver about the content of the video and audio format been transmitted. All the detailed information is provided in the HDMI 1.4b Specification.

32.5.9 Step G: Configure HDCP 1.4

Following flow is an initialization of HDCP 1.4. To detect if the HDMI TX Controller is HDCP capable:

1. Read the product_id1.product_id1 bit field register:

- If product_id1 = 01, HDCP is not present.
- If product_id1 = C1, HDCP is present.

2. Select HDMI mode:

- Write "1" for HDMI in the a_hdcpcfg0.hdmidvi bit field register.

3. Set the Data enable, Hsync and VSync polarity:

Write the dataenpol, vsyncpol, and hsyncpol bit fields of the a_vidpolcfg register.

4. Set encryption on:

- Write "64 (0x40)" for "OesswindowSize" in the a_oesswcfg register.
- Write "0" for "no HDCP bypass" a_hdcpcfg0.BypassEncryption bit field register.
- Write "0" for "HDCP enable" in the a_hdcpcfg1.encryptiondisable bit field register.

5. Reset HDCP engine:

- Write "0" in the a_hdcpcfg1.swreset bit field register.

6. Configure Device Private Keys, which is illustrated in the flow chart Figure 3-6

7. Enable the encryption:

- Write "1" in the a_hdcpcfg0.rxdetect bit field register.

8. When connected to a repeater the SHA-1 calculation is needed to be done by software, which are indicated in the following steps

a. Wait for an interrupt to be triggered (a_apiintstat.KSVSha1calcint).

b. Request access to KSV memory through setting a_ksvmemctrl.KSVMEMrequest to 1'b1 and pool a_ksvmemctrl.KSVMEMaccess until this value is 1'b1 (access granted).

c. Read VH', M0, Bstatus, and the KSV FIFO.

The data is stored in the revocation memory.

d. Calculate the SHA-1 checksum (VH) over M0, Bstatus, and the KSV FIFO.

e. If the calculated VH equals the VH`, set a_ksvmemctrl.SHA1fail to 0 and set a_ksvmemctrl.KSVCTRLupd to 1. If the calculated VH is different from VH` then set a_ksvmemctrl.SHA1fail to 1 and set a_ksvmemctrl.KSVCTRLupd to 1, forcing the controller to re-authenticate from the beginning.

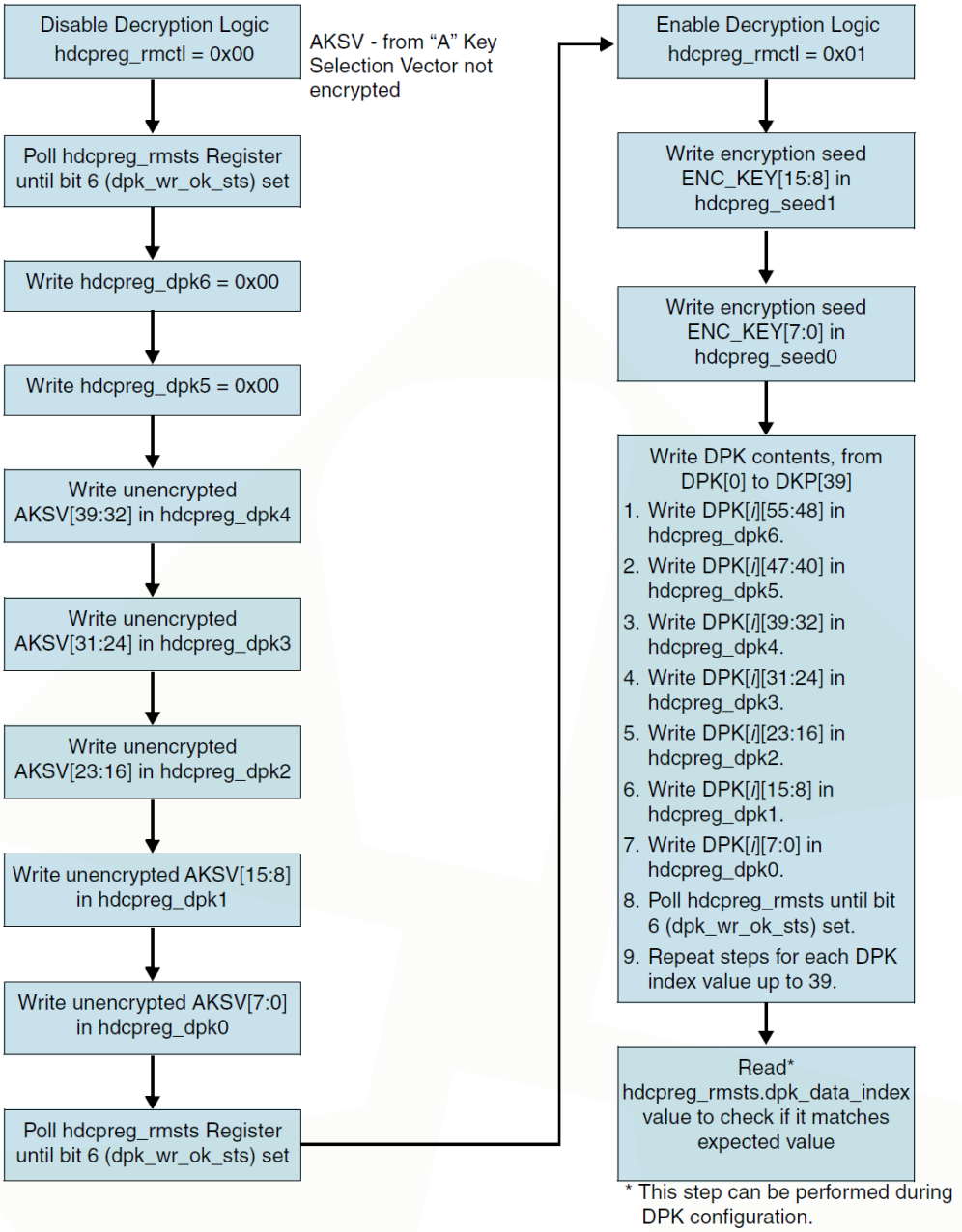


Fig. 32-8 Configuring Device Protection Key Process

32.5.10 CEC OPERATION

The CEC line is used for high-level user control of HDMI-connected devices.The HDMI TX contain CEC TX operations and CEC RX operations.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The register offset is from 0x7D00.

- Configure The CEC Step:
  - ■ Write the CEC logical address to cec_addr_l,cec_addr_h register
  - ■ Write the size of the frame in bytes which are available in the transmitter data buffer to cec_tx_cnt register

■ Write the desired CEC data(including header and data blocks) to cec_tx_data0 to cec_tx_data15

■ Write 1 to cec_ctrl.send register, to start the cec transmit.

32.5.11 HDMI PHY MPLL configuration

Table 32-6 HDMI PHY MPLL Generic Configuration Settings

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
13.5	1	8	1.4	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	0	27
13.5	1	10	1.4	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	1	1	0	0	1	1	0	33.75
13.5	1	12	1.4	1	0	0	0	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	1	0	40.5
13.5	1	16	1.4	1	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	1	1	0	0	1	1	0	54
13.5	3	8	1.4	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	1	1	1	0	0	1	1	0	54
13.5	3	10	1.4	0	1	0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	67.5
13.5	3	12	1.4	1	0	0	0	0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	0	81
13.5	3	16	1.4	1	1	0	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1	0	0	1	1	0	108
13.5	7	8	1.4	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1	0	0	1	1	0	108
13.5	7	10	1.4	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1	1	1	1	0	0	1	1	0	135
13.5	7	12	1.4	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1	1	1	1	1	0	1	1	0	162
13.5	7	16	1.4	1	1	0	0	0	0	1	0	0	1	1	0	0	0	0	1	1	1	0	0	1	1	0	216
18	2	8	1.4	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	0	0	0	1	0	54
18	2	10	1.4	0	1	0	0	0	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0	1	1	0	67.5
18	2	12	1.4	1	0	0	0	0	0	1	1	0	1	0	0	0	1	0	1	1	1	0	0	1	1	0	81
18	2	16	1.4	1	1	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1	0	108

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
18	5	8	1.4	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1	0	108
18	5	10	1.4	0	1	0	0	0	0	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	0	135
18	5	12	1.4	1	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	1	1	0	0	1	1	0	162
18	5	16	1.4	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	216
21.6	4	8	1.4	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	0	0	0	0	1	0	108
21.6	4	12	1.4	1	0	0	0	0	0	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	0	162
21.6	4	16	1.4	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	216
21.6	9	8	1.4	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	216
21.6	9	12	1.4	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	324
21.6	9	16	2	1	1	1	1	0	1	1	0	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1	432
24	8	8	1.4	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	216
24	8	16	2	1	1	1	1	0	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	1	1	1	432
25.175	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	25.175
25.175	No	10	1.4	0	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	0	0	0	0	1	0	31.46875
25.175	No	12	1.4	1	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	0	37.7625
25.175	No	16	1.4	1	1	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	50.35
27	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	27
27	No	10	1.4	0	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	0	0	0	0	1	0	33.75
27	No	12	1.4	1	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	0	40.5
27	No	16	1.4	1	1	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	54
27	1	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	54
27	1	10	1.4	0	1	0	0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	0	0	1	0	67.5
27	1	12	1.4	1	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	0	0	0	1	0	81

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
27	1	16	1.4	1	1	0	0	0	0	0	1	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	108
27	3	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	108
27	3	10	1.4	0	1	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	0	0	0	0	1	0	135
27	3	12	1.4	1	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1	0	162
27	3	16	1.4	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	1	0	216
27	7	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	1	0	216
27	7	10	1.4	0	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	270
27	7	12	1.4	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	324
27	7	16	2	1	1	1	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	1	432
31.5	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	31.5
33.75	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	33.75
35.5	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	35.5
36	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	36
36	2	8	1.4	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	108
36	2	10	1.4	0	1	0	0	0	0	1	0	1	1	0	0	1	0	1	1	1	1	0	0	1	1	0	135
36	2	12	1.4	1	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	0	0	0	1	0	162
36	2	16	1.4	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	216
36	5	8	1.4	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	216
36	5	10	1.4	0	1	0	0	0	0	1	0	1	1	0	0	1	0	0	1	1	1	0	0	1	1	0	270
36	5	12	1.4	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	324
36	5	16	2	1	1	1	1	0	1	0	1	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1	432
40	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	40
43.2	4	8	1.4	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	216

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl		fbdiv1_c ntrl		ref_cnt rl		n_cntrl		prop_cntrl		int_cntrl				gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
43.2	4	12	1.4	1	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	1	1	0	0	1	1	0	324
43.2	4	16	2	1	1	1	1	0	1	1	0	1	0	1	0	0	0	0	1	1	0	0	0	1	1	1	432
44.9	No	8	1.4	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	1	0	0	0	1	0	44.9
49.5	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	49.5
50	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	50
50.35	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	50.35
50.35	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	62.9375
50.35	No	12	1.4	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	75.525
50.35	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	100.7
54	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	54
54	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	67.5
54	No	12	1.4	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	81
54	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	108
54	1	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	108
54	1	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	1	0	1	0	1	0	135
54	1	12	1.4	1	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	162
54	1	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	1	0	1	0	216
54	3	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	1	0	1	0	216
54	3	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	270
54	3	12	1.4	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	324
54	3	16	2	1	1	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1	0	0	0	1	1	1	432
56.25	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	56.25
59.4	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	59.4

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
59.4	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	74.25
59.4	No	12	1.4	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	89.1
59.4	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	118.8
65	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	65
68.25	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	68.25
71	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	71
72	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	72
72	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	0	90
72	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	108
72	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	144
72	2	8	1.4	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	216
72	2	10	1.4	0	1	0	0	0	0	1	0	1	1	0	1	1	0	0	1	1	1	0	0	1	1	0	270
72	2	12	1.4	1	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	0	1	0	0	0	1	0	324
72	2	16	2	1	1	1	1	0	1	0	1	0	1	0	0	0	0	0	1	1	0	0	0	1	1	1	432
73.25	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	73.25
74.25	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	74.25
74.25	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	92.8125
74.25	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	111.375
74.25	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	148.5
75	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	75
78.75	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	78.75
79.5	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	79.5
82.5	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	82.5

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
82.5	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	103.125
82.5	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	123.75
82.5	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	165
83.5	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	83.5
85.5	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	85.5
88.75	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	88.75
90	No	8	1.4	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	1	0	90
90	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	112.5
90	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	135
90	No	16	1.4	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1	0	180
94.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	94.5
99	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	99
99	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	123.75
99	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	148.5
99	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	198
100.7	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	100.7
100.7	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	125.875
100.7	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	151.05
100.7	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	201.4
101	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	101
102.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	102.25
106.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	106.5
108	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	108

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl			ref_cnt rl		n_cntrl		prop_cntrl			int_cntrl			gmp_cntrl	
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
108	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	135
108	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	162
108	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	216
108	1	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	216
108	1	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	1	0	1	0	1	0	270
108	1	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	324
108	1	16	2	1	1	1	1	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0	1	1	1	432
115.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	115.5
117.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	117.5
118.8	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	118.8
118.8	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	148.5
118.8	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	178.2
118.8	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	237.6
119	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	119
121.75	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	121.75
122.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	122.5
135	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	135
136.75	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	136.75
140.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	140.25
144	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	144
144	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	180
144	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	216
144	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	288

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
146.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	146.25
148.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	148.25
148.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	148.5
148.5	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	185.625
148.5	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	222.75
148.5	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	297
154	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	154
156	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	156
157	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	157
157.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	157.5
162	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	162
165	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	165
165	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	206.25
165	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	247.5
165	No	16	1.4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	330
175.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	175.5
179.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	179.5
180	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	180
180	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	225
180	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	270
180	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	360
182.75	No	8	1.4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	182.75
185.625	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	185.625

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl		fbdiv1_c ntrl		ref_cnt rl		n_cntrl		prop_cntrl		int_cntrl				gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
185.625	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	232.03125
185.625	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	278.4375
185.625	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	371.25
187	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	187
187.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	187.25
189	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	189
193.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	193.25
198	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	198
198	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	247.5
198	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	297
198	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	396
202.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	202.5
204.75	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	204.75
208	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	208
214.75	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	214.75
216	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	216
216	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	270
216	No	12	1.4	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	324
216	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	432
218.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	218.25
229.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	229.5
234	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	234
237.6	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	237.6

				Divider Settings				Op Mode		Divider Settings								MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode		fbdiv2_cntrl			fbdiv1_c ntrl		ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
237.6	No	10	1.4	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	297
237.6	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	356.4
237.6	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	475.2
245.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	245.25
245.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	245.5
261	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	261
268.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	268.25
268.5	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	268.5
281.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	281.25
288	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	288
288	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	360
288	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	432
288	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	576
297	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	297
297	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	371.25
297	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	445.5
297	No	16	2	1	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	1	1	594
317	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	317
330	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	330
330	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	412.5
330	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	495
333.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	333.25
340	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	340

				Divider Settings				Op Mode	Divider Settings									MPLL Charge Pump Settings								
				0x06														0x10						0x15		
				prep_div		tmds_cntrl		opmode	fbdiv2_cntrl			fbdiv1_c ntrl			ref_cnt rl		n_cntrl	prop_cntrl			int_cntrl			gmp_cntrl		
				0006:Bit 14	0006:Bit 13	0006:Bit 12	0006:Bit 11	0006:Bit 10	0006:Bit 9	0006:Bit 8	0006:Bit 7	0006:Bit 6	0006:Bit 5	0006:Bit 4	0006:Bit 3	0006:Bit 2	0006:Bit 1	0006:Bit 0	0010: Bit 5	0010: Bit 4	0010: Bit 3	0010: Bit 2	0010: Bit 1	0010: Bit 0	0015: Bit 1	0015: Bit 0	
Pixel Clock(Mhz)	Pixel Repetition	Color depth [bits]	OPMODE	prep_div<1>	prep_div<0>	tmds_cntrl<1>	tmds_cntrl<0>	opmode<1>	opmode<0>	fbdiv2_cntrl<2>	fbdiv2_cntrl<1>	fbdiv2_cntrl<0>	fbdiv1_cntrl<1>	fbdiv1_cntrl<0>	ref_cntrl<1>	ref_cntrl<0>	n_cntrl<1>	n_cntrl<0>	prop_cntrl<2>	prop_cntrl<1>	prop_cntrl<0>	int_cntrl<2>	int_cntrl<1>	int_cntrl<0>	gmp_cntrl<1>	gmp_cntrl<0>	TMDSCLKSRC (MHz)
348.5	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	348.5
356.5	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	356.5
360	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	360
360	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	450
360	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	540
371.25	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	371.25
371.25	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	464.0625
371.25	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	556.875
281.25	No	8	1.4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	281.25
396	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	396
396	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	495
396	No	12	2	1	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	1	594
432	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	432
432	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	540
380.5	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	380.5
475.2	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	475.2
475.2	No	10	2	0	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	1	594
495	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	495
505.25	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	505.25
552.75	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	552.75
594	No	8	2	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	594

Chapter 33 HDCP22 Controller

33.1 Overview

The HDCP22 controller is an Embedded Security Module (ESM). This module is a self-contained module that can be integrated with HDMI cores to ensure DCP robustness rules for HDCP.

The ESM has a small MCU inside. It reads ESM Image for operation through the AXI interface.

The HDCP22 Controller supports following features:

- Supports HDCP Revision 2.2
- Bus Interface Features:
  - An AXI port for instruction fetch and shared R/W memory
  - An Identity Interface for secret keys used to secure the ESM
  - An Entropy Interface to a true random number generator
  - A Host Port Interface for an external host processor to send commands and get status from the ESM.
    (APB Interface)
- The Tx ports contain interfaces to a HDMI controller, where each port is factory configurable for HDMI support. The HDMI portion of the port contains the following interfaces:
  - HDMI video data and associated control
  - I2C interface for access to the remote end of the HDCP link
  - A GPIO interface for direct hardware signaling between the ESM and the controller
- MMU:
  - 4k/64k page size
  - TLB pre-fetch

33.2 Block Diagram

The following figure illustrates the HDMI controller connections with external interfaces. The ESM executes firmware from system memory external to the ESM which must be processed with the supplied tools as the firmware image is encrypted to the keys you created to present on the ID Interface. A host library (supplied in source code) is compiled with your application software running on the host processor to send commands to the ESM and monitor its status for results.

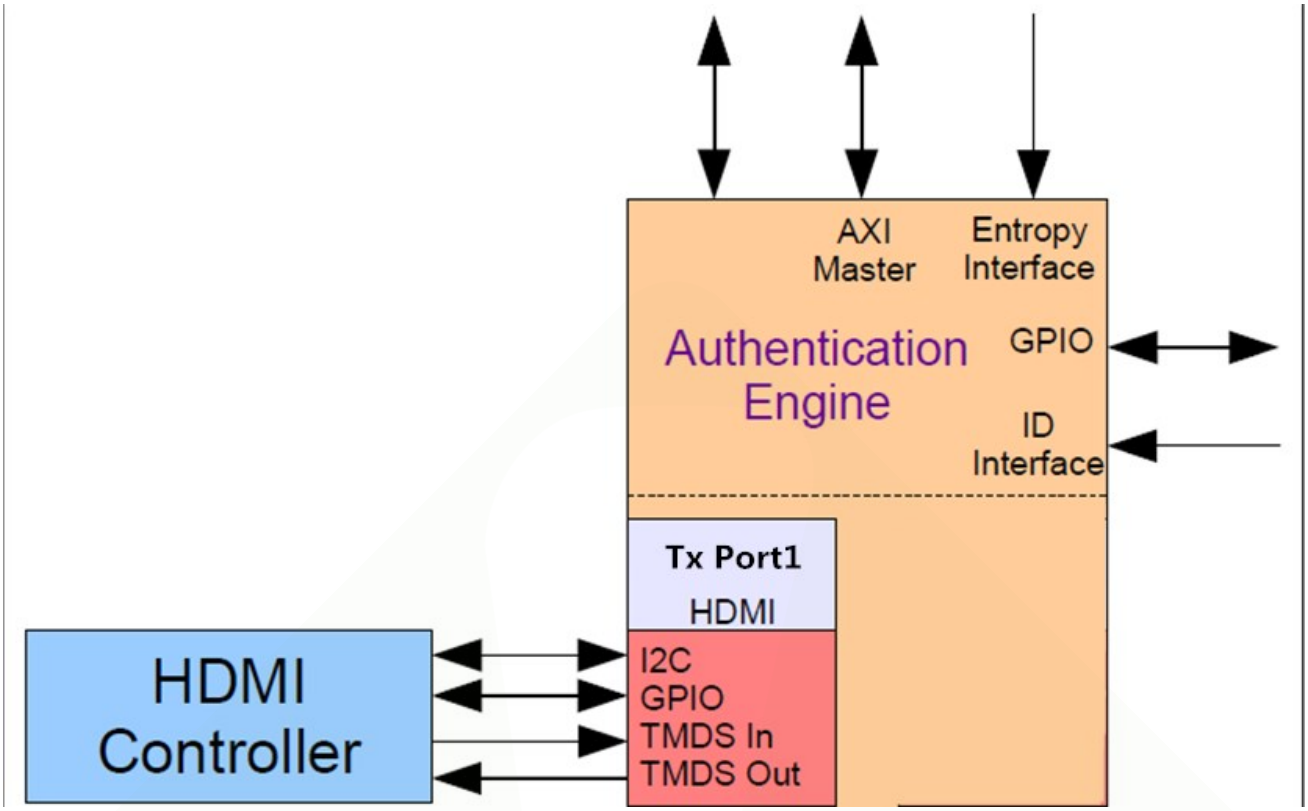


Fig. 33-1 hdcp22 Controller Block Diagram

The embedded security module is composed of two parts:

- The Authentication Engine (AE) contains a controller that runs the HDCP authentication process.
- The Content Encryption Engine (CEE) is an ESM component that encrypts data for the HDCP transmitter.

The following figure represents how the ESM is typically integrated in a SoC.

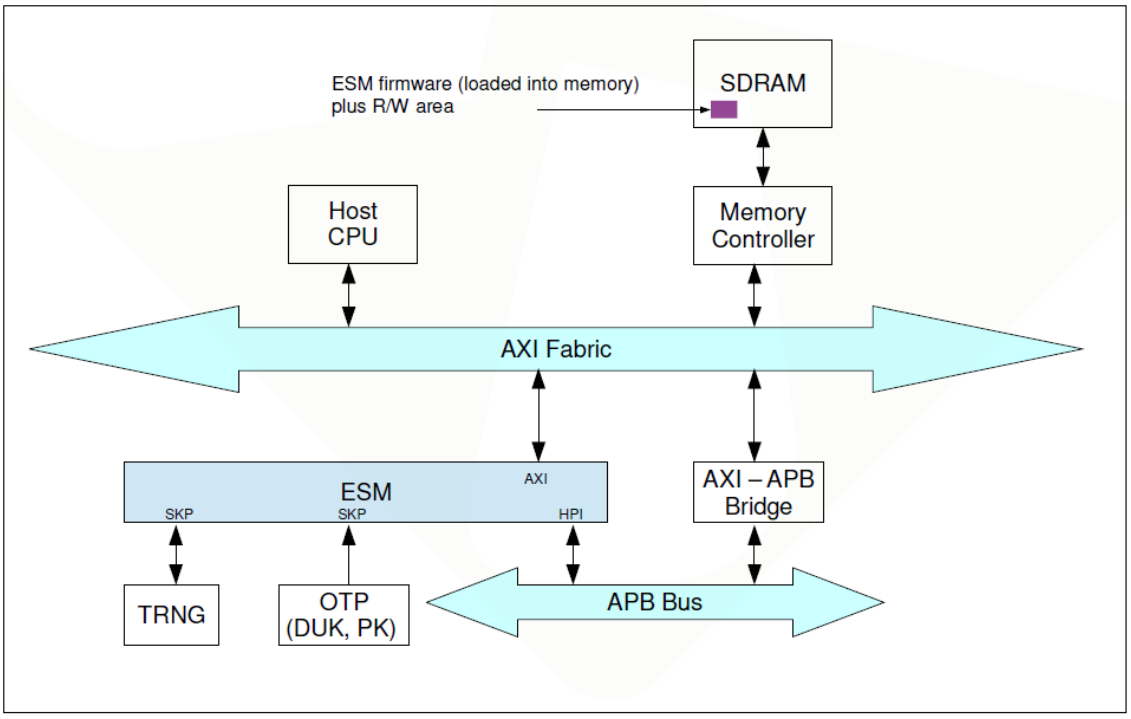


Fig. 33-2 Typical ESM Integration in a SoC

33.3 Function Description

33.3.1 AXI interface

The ESM requires continuous access to its firmware for operation, which is accessed through

the AXI interface and usually placed a reserved portion of SDRAM. It also uses this interface for communicating messages with the external host processor to pass content such as SRM data, pairing information, and debug/logging information.
The ESM requires access to relatively fast and low latency external memory as it randomly accesses its firmware periodically to perform operations. For AXI transactions the average initial access latency may be up to 1000ns.
Note: *The ESM still functions in higher latency systems; however, the ESM may experience intermittent errors, such as failing to authenticate, as there are fixed timeout requirements during the authentication process which must be met. A system with persistent high latency memory accesses may prevent the ESM from fetching its firmware in a timely fashion resulting in protocol timeouts.Following Table summarizes the various requirements the ESM places on the RK3399's memory, assuming an AXI interface clock of 261 MHz and an average latency of 1000 ns.*

Table 33-1 ESM average memory bandwidth usage

Phase	Duration (ms)	Appropriate Bandwidth (Mbytes/sec)	Description
Bootup	100 (maximum)	5.0	Initial startup of ESM to Idle state.
Tx Authentication	525ms	1.5	ESM transmitter authentication phase including capability check.
Rx Authentication	525 ms	1.0	ESM receiver authentication phase.
Idle, authenticated	n/a	< 1.0, 4.0	ESM is either in the Idle state waiting to start authentication or in the authenticated state. The second number is when the ESM has debug logging enabled.

The external host memory required by the ESM must be physically contiguous and allocated before the ESM can be started. The ESM Image and R/W memory buffer addresses must be 4K aligned otherwise the ESM cannot properly access the memory. Following table describes the requirements.

Table 33-2 ESM average memory bandwidth usage

Size (bytes)	ESM Access	Purpose
~256K	Read Only	Contains the ESM firmware. This size varies depending on the particular configuration of the ESM you are using.
16K + p*n*256 (Tx) (p is the number of transmitters and n is the number of paired devices supported)	Read / Write	Bidirectional communication buffer to exchange data with the Host. Messages such as SRM updates, pairing data, and logging information are placed in this area by the host and the ESM. The number of pairs supported by this parameter is defined in the configuration file.

In RK3399 the provided ESM host application library allocates a small amount of the processor's memory space, which is accessible by the ESM. Communication with this interface is provided by the ESM host application library.

33.3.2 HPI Interface

The external host issues commands to the ESM through the HPI which supports a limited set of commands such as:

- Enabling and disabling of security on the link

- Enabling debugging/logging
- Retrieving pairing information
- Updating the SRM
- ESM status

Communication with this interface is provided by the ESM host application library.

33.3.3 APB interface (HPI)

The external host issues commands to the ESM through the HPI. The ESM supports a limited set of commands such as:

- Enabling and disabling of security on the link
- Enabling debugging/logging
- Retrieving pairing information
- Updating the SRM
- ESM status

The external host must issue a SRM list to the ESM when one is available, according to the requirements of DCP LLC.

Communication with this interface is provided by the ESM host application library.

33.3.4 Identity Interface

This interface contains the secret keys the ESM requires to implement its security. The KPf and

DUK signals on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for operation.

When integrating the ESM into your design, you must take to ensure that these requirements are met otherwise the operation of the ESM can be compromised.

Table 33-3 Secure Key for ESM

Description	Purpose
Platform Key (PKf)	A customer created secret random key used to decrypt the ESM firmware. The KPf is intended to be common across a deployed model of a product.
Device Unique Key (DUK)	A customer created secret random key used to decrypt the DCP key data and to encrypt and decrypt content unique to the ESM such as the pairing message content. It is strongly recommended this value should be unique for every unit.
Device Number (Devnum)	This is a non-secret device number and is currently not used.

Note: *The PKf and DUK must be kept confidential as exposing either one compromises the security of the ESM.*

33.3.5 Entropy Interface

This interface connects to a True Random Number Generator (TRNG). The nonce data on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for operation.

Table 33-4 Entropy Interface

Description	Purpose
Entropy Valid	This is the nonce data from the TRNG. The value is used to seed the ESM's PRNG which is used to generate keys for the authentication process and session keys. The value must be truly random and not generated by another PRNG, as per the HDCP for HDMI specification, Section 2.13 (Random Number Generation).

33.3.6 GPIO Interface

This interface contains a number of general purpose inputs and outputs which can be used by the host to monitor the status of the ESM.

33.3.7 HDMI Interface

The HDMI interface contains logic to apply content protection to the Data and Video Islands as the TMDS data passes through the ESM.

Table 33-5 Entropy Interface

Description	Purpose
I2C	A standard I2C serial interface for HDCP protocol communication with the remote device, mapped by the controller onto the DDC interface.
GPIO	Direct signals between the controller and the ESM to indicate the status of the ESM to the controller, and to signal the ESM
TMDS In	TMDS data output from the controller. For a Tx this is the unencrypted data, for the Rx this is the encrypted data.
TMDS Out	TMDS data input to the controller. For a Tx this is the encrypted data, for the Rx this is the decrypted data.

33.3.8 HDCP22 Controller Behavior

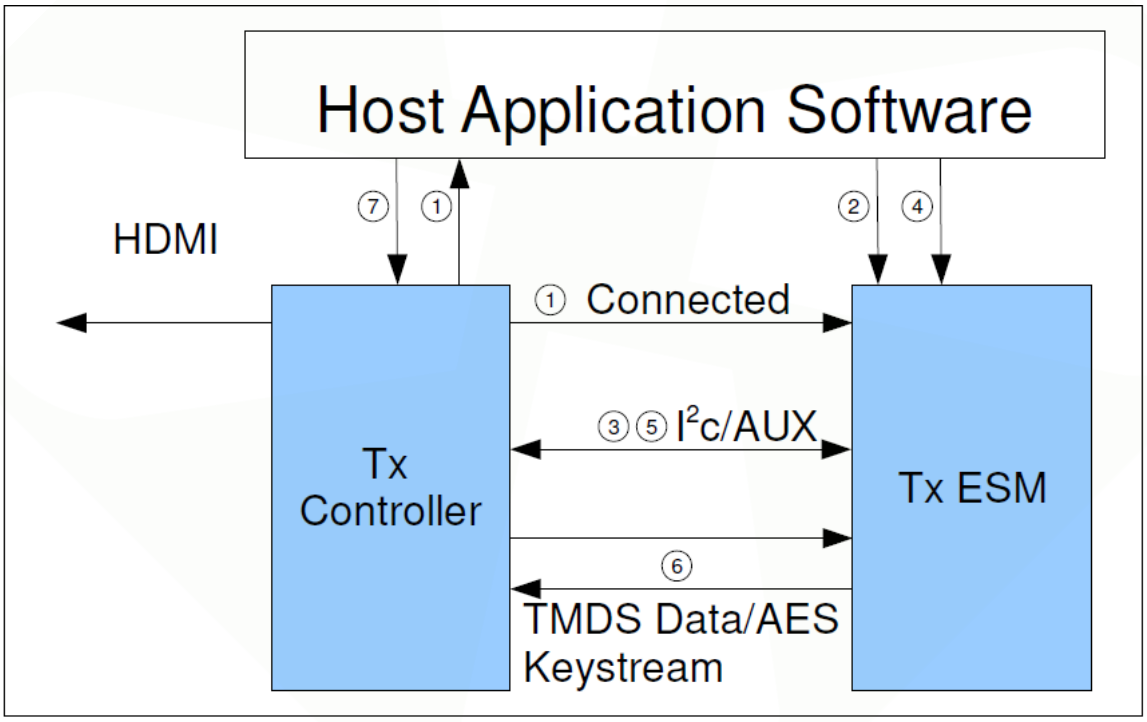


Fig. 33-3 Transmitter Authentication

Hdcp22 controller in RK3399 is a transmitter, it works as following steps:

1. The controller asserts the Connected signal to the ESM. The application software1 receives the notification from the controller. For HDMI operation the ESM outputs a fixed pattern (the BSOD value) on the TMDS data output.
2. The application software issues the HLC_HDCPTX_SetCapability() command which causes the ESM to perform a capability check with the receiver. Before this point in time the ESM does not know the capability of the Rx so the port's capable GPIO output signal is not asserted.
3. The ESM queries the receiver. If the receiver does not support HDCP 2.2 then the port's not_capable GPIO output is asserted. The application software should then check if the

receiver supports HDCP 1.4 (or no link protection) and take appropriate action; the ESM is no longer required. If the receiver supports HDCP 2.2 then the capable GPIO output is asserted and the ESM transitions to a pre-authorized state. For HDMI operation this means unencrypted low value content is permitted on the video path (TMDS interface).
4. If the receiver supports HDCP 2.2 the application software issues the HLC_HDCP_Authenticate() command to the ESM. As a security feature the ESM enforces a timeout (set in the configuration file) after the receiver indicates it is HDCP 2.2 capable to the time the HLC_HDCP_Authenticate() command must be issued. If you exceed this timeout you must repeat the process from step #2. (When the port is configured for HDMI it will switch its TMDS output back to the fixed pattern output).
5. The ESM initiates authentication with the receiver and successfully completes authentication (or not). The application software and the HDMI controller are appropriately notified (authenticated and authentication_failed outputs asserted accordingly).
6. If authentication is successful the ESM starts to encrypt the TMDS data (HDMI).
7. The application software can now send high value content securely on the link.
Following successful authentication the ESM periodically checks the status of the connected receiver. If a response is not received, or the receiver requests re-authentication the ESM immediately outputs a fixed pattern on the TMDS output (HDMI), asserts the outputs authentication_failed along with a reath_req, and returns to the Idle state. To re-authenticate you must call HLC_HDCP_Authenticate() to drop authentication and then call the function again to start authentication.

33.3.9 HDCP22 Software Initialization

An external host controller (ARM Core or MCU) allocates memory, initializes the ESM, and enables the ESM controller. The general reset and startup sequence is:

a. Configure clocks for hdcp controller.
b. Load PKF & DUK from effuse to gasket.
c. The ESM reset is de-asserted and the ESM enters a reset state.
d. The host allocates contiguous memory for the firmware and R/W areas. The buffers are 4K aligned.
e. The host configures the ESM's HPI interface, defining the physical memory pointer for the
ESM firmware.
f. The host copies the ESM firmware from persistent storage to the firmware memory location.
g. The host enables the ESM controller, putting it in a running state. At this point the ESM initiates transactions on the AXI bus to fetch its firmware.
h. ESM asserts a GPIO to indicate it is booted to indicate it can accept commands. The status
can also be monitored from the HPI interface.

The ESM host application library provides the startup sequence from steps d through h.

33.3.10 Autostart

The autostart feature is an option which permits a transmitter or receiver port (configurable per port) on the ESM to autonomously take over the detection of a connection and run through the authentication process without intervention from the external host. In the event of an error the port automatically retries up to a specified number of attempts (configuration based) before idling requiring intervention from the host.
For a transmitter this feature automates the capability checking and authentication along with any reauthentication which may be required due to link errors. For a receiver this feature enables the port to immediately respond to authentication requests without host

intervention.

33.3.11 Key Usage

There are two secret, 128 bit keys you are responsible for creating for use by the ESM.
The Platform Key (KPf) is used by the ESM to decrypt its firmware. It is recommended this key be common for all ESMs deployed for a particular product as it permits a common (encrypted) firmware image to be deployed.
The Device Unique Key (DUK) is used by the ESM to protect secrets unique to the device such as HDCP receiver keys and locally generated data such as pairing information. Although it is not required, it is strongly recommended this key be unique for every different unit deployed in a product so that if the kPf is and DUK are compromised, device specific secrets for only that unit are exposed. Using a common DUK for all devices could permit device specific secrets for all devices to be exposed.
As shipped from the factory, the firmware cannot be used as-is and must be processed with tools that are provided with the ESM software package. Figure 1-3 illustrates the tools and the flow that are required to produce encrypted ESM firmware. You edit the firmware.aic file supplied with the firmware image and replace the factory test/simulation values with your secret KPf and DUK keys.

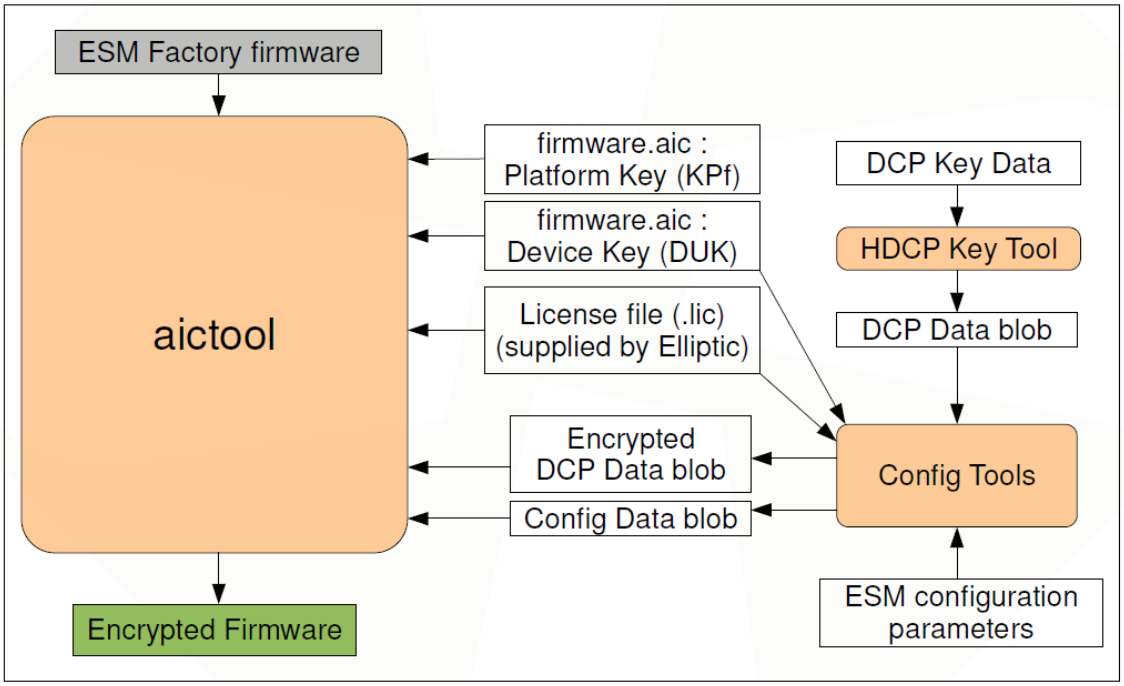


Fig. 33-4 ESM Image tool flow

The DCP Tx key data is common for all transmitter ports whereas the DCP Rx key data is unique for each receiver port.
To facilitate manufacturing it is highly desirable to build and deploy a common software image for all units. If your ESM only contains transmitter ports then it is possible to do this, however if you also have receiver ports you are required by DCP to have a unique receiver key for each receiver in your design.

33.4 Application Notes

33.4.1 Host Application Software

The ESM package contains a series of tools and a run-time library as bellow:

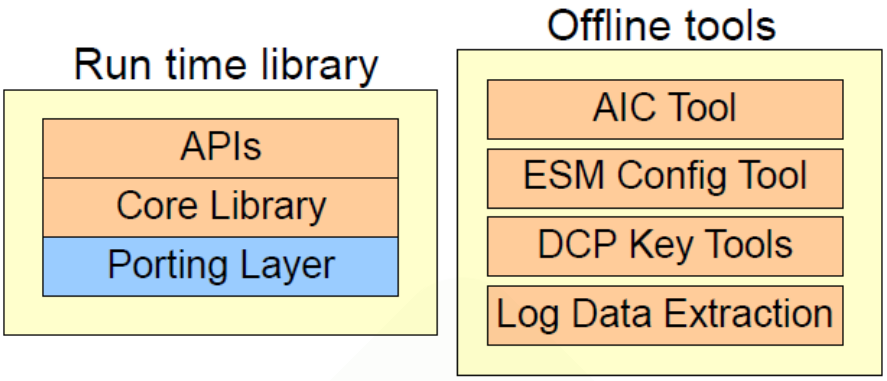


Fig. 33-5 ESM software

33.4.2 Run Time Library

This library is provided as source code and is used by the host application processor to control the ESM.
Setting the configurable options of the ESM is not provided through APIs for security reasons. It is instead embedded into the ESM's Image as part of the process of building a deployable image.
The APIs provide a minimal interface to the ESM, which include the following:

- Load/Initialize firmware image
- Start authentication to secure a link
- Terminate an authenticated link
- Collect logging data
- Get/Set pairing information
- Update SRM data
- Status updates

Sample code is provided and demonstrates how to use the various APIs. In addition, a software API reference guide is included and provides details on the API calls and their parameters.

33.4.3 Offline Tools

There are three separate offline tools that are required to build a deployable image for the ESM as shown in Figure ESM Image tool flow and one tool for logging information. All of these tools are developed to run on a 32 bit Linux system.

33.4.4 Configuration Tool

The troot_base_config_interface tool is used to convert the various configuration files into a data blob to be used by the aictool which creates the encrypted ESM firmware. There are a number of different configuration files which the tools reads, with each configuration file containing a mix of factory configured parameters, and user-adjustable parameters.
This tool also requires the firmware.aic file in order to generate the data blob.

User Parameters for Configuration Files

The following table indicates which parameters in the configuration files are user-adjustable and other non-described parameters should not be changed. A basic description of the parameter is included below, see the configuration file's comments for a more complete description.

Table 33-6 Configuration files

File Name	Parameter	Description
troot_base_config.cfg	[LOGGING_MODE]	Logging on/off
	[LOGGING_LEVEL]	Sets the verbosity of the output log messages.
	[RESEED_TIMEOUT]	Specifies the time the ESM will wait for the TRNG to supply a new nonce before reporting an error

File Name	Parameter	Description
	[RESEED_AUTO_INTERVAL]	By default the ESM will periodically query the TRNG for a new nonce at the period specified.
	[CPU_FREQ]	Sets the frequency of the esm_clk input. Mandatory to change.
troot_hdcpmgr_tx.cfg	[SRM_VERSION]	Denotes whether the SRM is to be checked or not and the minimum version number permitted.
troot_hdcptx.cfg	[I2C_FREQ]	(HDMI) Sets the default I2C frequency. Can be changed via an API.
	[I2C_USE_SHORT_READ]	(HDMI) Sets whether the interface uses short reads for status requests. Can be changed via an API.
	[CEE_BSOD]	(HDMI) Sets the 24 bit fixed pattern value output by the ESM. See the description following this table for more details.
	[AUTO_START]	Sets the default startup state of the Autostart feature
	[HDCP_TIMEOUTS]	Sets whether the ESM enforces the HDCP timeout periods. Should be enabled only for testing and/or debugging.
	[CEE_FRAME_CNT_DEBUG]	(HDMI) The ESM emits periodic log messages once authenticated, based on the number of VSYNC pulses counted by this parameter.
	[PAIRING_ENABLED]	Sets whether pairing will be enabled or not
	[MAX_PAIRING_DEVICES]	Sets the maximum number of paired devices supported per port. Note the external R/W memory requirements increase based on this setting, and the number of Tx ports in your design.
	[MEM_PAIRING_SIZE]	Sets the amount of R/W memory the pairing data will occupy.
	[CAPABLE_BYPASS_TIME]	(HDMI) Sets the maximum amount of time the ESM will enable low value content after a capability

File Name	Parameter	Description
		check before switching back to a fixed pattern output. See HLC_HDCPTX_SetCapability in the API guide.
	[LVC_TIMEOUT]	(HDMI) Sets the maximum amount of time the ESM will enable low value content without a capability check. See HLC_HDCPTX_EnableLowValueContent in the API guide.
	[LVC_EXPIRED_CNT]	(HDMI) Sets the maximum number of LVC timeouts permitted.

The [CEE_BSOD] is a 32 bit decimal value which parameter represents fixed data output on the TMDS data bus if the ESM encounters an authentication issue or detects attempts have been made to tamper with it. The value is only relevant for ports configured for HDMI. This 32 bit value is output as follows:

Table 33-7 ESM BSOD Output Mapping

BSOD Bit Positions	HDMI Controller TMDS Data Channel
7..0	O_tmds_ch0 [7..0]
15..8	O_tmds_ch1 [7..0]
23..16	O_tmds_ch2 [7..0]
32..24	Not used

33.4.5 HDCP Key Tools

This tool (hdcpkeys) is used to create a DCP key data file, which is required to build the encrypted DCP data blob needed for creating the encrypted ESM firmware. The tool reads a configuration file that contains the Rx or Tx key information from DCP in clear text and outputs a structured data file for the configuration interface tool to encrypt with the appropriate secret keys.

The tools can also accept the DCP published key files themselves.

33.4.6 AIC Tool

The aictool tool is used to create the encrypted ESM firmware. To build the encrypted firmware, you must first create the data files for the DCP keys and the configuration. These files, along with an input configuration file for this tool are used to build an image that can be used by the ESM. In addition to specifying the Platform and Device Unique Keys in the configuration file, there are additional keys that also must be specified as noted below.

Content Randomization

There are two separate values in the firmware.aic file, IK and IVc (128 bits and 96 bits respectively), which you must randomly generate to create a new encrypted ESM firmware image. Failure to do this puts secret data in the ESM firmware at risk of being compromised.

33.4.7 Log Data Extraction

The logging information from the ESM is output in a proprietary format. This tool is used to produce readable output of captured logging data content.

The Host Library contains a core library component which includes all the functions necessary to use the ESM. The library is built using portable C code and uses various abstraction functions to allow for migration to different platforms. Before using the ESM in

your system you must properly implement the abstraction components specific to your platform.
There are two distinct abstraction components used by the Host Library, the System Abstraction Layer and the Host Library Driver (HLD) component. The System Abstraction Layer (or Common Component) defines system level functions used by the Host Library, such as malloc, memcpy, etc.
These functions are linked into the Host Library when it is built.
The Host Library Driver (HLD) component establishes a communication between the library and the physical ESM hardware, including managing the memory required for the ESM Image and the read/write area. This is a run-time plug-in module that is defined in your application and specified as a parameter to the ESM initialization function.
The figure below illustrates the abstraction components used by the Host Library package. This figure demonstrates one example where there are three separate ESMs in the system, requiring (typically) three separate HLD instantiations. Consult the ESM Host Library API guide for more details on the HLD implementation.

33.4.8 Host Library

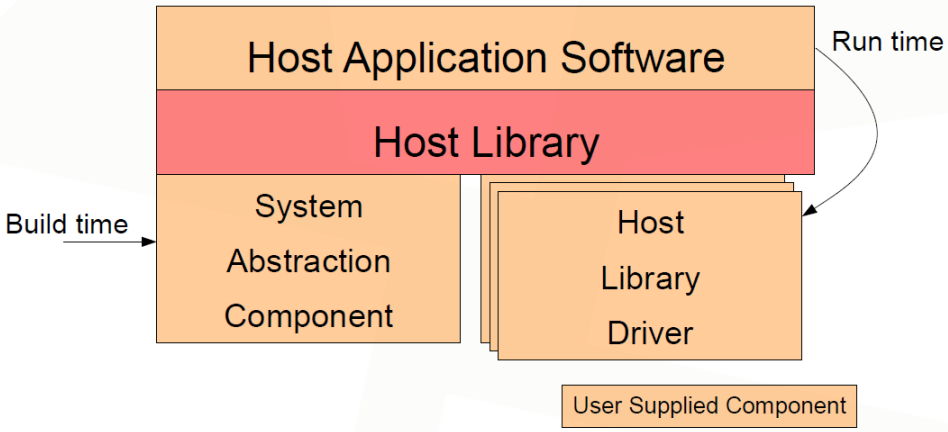


Fig. 33-6 Host Library Layers

The Host Library provides a number of sample applications using the ESM with the library. The
applications demonstrate using the library in a User Space Linux application:

- Repeater/Converter (Linux) [Planned in later releases – not currently available]
- Transmitter (Linux)

All the sample applications demonstrate API usage, loading the ESM firmware, and running a specific ESM application.

The sample applications provided as a Linux User Space application communicate to the ESM hardware through a Linux Kernel driver which is implemented as a Host Library Driver (HLD) plug-in.

Transmitter

There is a sample transmitter applications provided in the samples folder:
hdcp_tx.c is a Linux based example and utilizes file IO and threads.