Rockchip
RK3568
Technical Reference Manual

Revision 1.1
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Revision History

Date	Revision	Description
2021-03-01	1.1	Cancel the wrong information
2021-01-11	1.0	Initial Release

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Chapter 1 System Overview

1.1 Address Mapping

RK3568 boot from internal BootRom, which supports remap function by software programming. Remap is controlledbyPMU_SGRF_SOC_CON1[12:11]. When remap is set to 2'b01, the BootRom is un-accessible and PMU_SRAM is mapped to address 0xFFFF0000. When remap is set to 2'b10, the BootRom is un-accessible andSYSTEM_SRAM is mapped to address 0xFFFF0000.

Table 1-1Address Mapping

Module	Start Address	Size	Module	Start Address	Size
PCIe3x2_S	0xF0000000	32MB	Reserved	0xFE290000	64KB
PCIe3x1_S	0xF2000000	32MB	GMAC0	0xFE2A0000	64KB
PCIe2x1_S	0xF4000000	32MB	SDMMC0	0xFE2B0000	64KB
PCIe3x2_DBI	0xF6000000	4MB	SDMMC1	0xFE2C0000	64KB
PCIe3x1_DBI	0xF6400000	4MB	Reserved	0xFE2D0000	192KB
PCIe2x1_DBI	0xF6800000	4MB	FSPI	0xFE300000	64KB
Reserved	0xF6C00000	84MB	EMMC	0xFE310000	64KB
SATA0	0xFC000000	4MB	Reserved	0xFE320000	64KB
SATA1	0xFC400000	4MB	NANDC	0xFE330000	64KB
SATAx2	0xFC800000	4MB	Reserved	0xFE340000	128KB
USB3_0	0xFCC00000	4MB	KEYLADDER_S	0xFE360000	64KB
USB3_1	0xFD000000	4MB	TRNG_S	0xFE370000	64KB
GIC600	0xFD400000	4MB	CRYPTO_NS	0xFE380000	32KB
USB20HOST0	0xFD800000	512KB	TRNG_NS	0xFE388000	16KB
USB20HOST1	0xFD880000	512KB	OTP_NS	0xFE38C000	16KB
DAPLITE	0xFD900000	512KB	Reserved	0xFE390000	64KB
Rreserved	0xFD980000	512KB	OTP_S	0xFE3A0000	32KB
QSGMII_PCS	0xFDA00000	2MB	DCF_S	0xFE3A8000	32KB
PMU_SGRF	0xFDC00000	64KB	Reserved	0xFE3B0000	32KB
Reserved	0xFDC10000	64KB	KEY_READER	0xFE3B8000	32KB
PMU_GRF	0xFDC20000	64KB	WDT_S	0xFE3C0000	64KB
CPU_GRF	0xFDC30000	64KB	SEC_TRNG_CHK	0xFE3D0000	64KB
DDR_GRF	0xFDC40000	64KB	JBG_USR	0xFE3E0000	64KB
PIPE_GRF	0xFDC50000	64KB	JBG_OTP	0xFE3F0000	64KB
SYS_GRF	0xFDC60000	64KB	I2S0_8CH	0xFE400000	64KB
PIPE_PHY_GRF0	0xFDC70000	64KB	I2S1_8CH	0xFE410000	64KB
PIPE_PHY_GRF1	0xFDC80000	64KB	I2S2_2CH	0xFE420000	64KB
PIPE_PHY_GRF2	0xFDC90000	64KB	I2S3_2CH	0xFE430000	64KB
USBPHY_U3_GRF	0xFDCA0000	32KB	PDM	0xFE440000	64KB
USBPHY_U2_GRF	0xFDCA8000	32KB	VAD	0xFE450000	64KB
EDP_PHY_GRF	0xFDCB0000	32KB	SPDIF_8CH	0xFE460000	64KB
PCIE30_PHY_GRF	0xFDCB8000	32KB	AUDPWM	0xFE470000	32KB
SYSTEM_SRAM(64K)	0xFDCC0000	64KB	DIG_ACODEC	0xFE478000	32KB
PMU_MEM	0xFDCD0000	128KB	SDMMC_BUF	0xFE480000	64KB
USB_GRF	0xFDCF0000	64KB	Reserved	0xFE490000	448KB

Module	Start Address	Size	Module	Start Address	Size
PMU_CRU	0xFDD00000	64KB	Reserved	0xFE500000	64KB
CRU_S	0xFDD10000	32KB	DMAC0_S	0xFE510000	64KB
SYS_SGRF	0xFDD18000	16KB	Reserved	0xFE520000	64KB
Stimer	0xFDD1C000	16KB	DMAC0_NS	0xFE530000	64KB
CRU_NS	0xFDD20000	64KB	DMAC1_S	0xFE540000	64KB
PMU_CRU_S	0xFDD30000	64KB	DMAC1_NS	0xFE550000	64KB
I2C0	0xFDD40000	64KB	SCR	0xFE560000	64KB
UART0	0xFDD50000	64KB	CAN0	0xFE570000	64KB
GPIO0	0xFDD60000	64KB	CAN1	0xFE580000	64KB
PWM0	0xFDD70000	64KB	CAN2	0xFE590000	64KB
PVTM_PMU	0xFDD80000	64KB	I2C1	0xFE5A0000	64KB
PMU_NS	0xFDD90000	64KB	I2C2	0xFE5B0000	64KB
Reserved	0xFDDA0000	128KB	I2C3	0xFE5C0000	64KB
DDR_SCRAMBLE_KEY	0xFDDC0000	32KB	I2C4	0xFE5D0000	64KB
OSC_CHK	0xFDDC8000	32KB	I2C5	0xFE5E0000	64KB
Reserved	0xFDDD0000	192KB	TIMER_NS	0xFE5F0000	64KB
PVTM_CORE	0xFDE00000	64KB	WDT_NS	0xFE600000	64KB
Reserved	0xFDE10000	128KB	SPI0	0xFE610000	64KB
GIC600	0xFDE30000	0KB	SPI1	0xFE620000	64KB
SPINLOCK	0xFDE30000	64KB	SPI2	0xFE630000	64KB
NPU	0xFDE40000	128KB	SPI3	0xFE640000	64KB
MALIG52	0xFDE60000	128KB	UART1	0xFE650000	64KB
PVTM_GPU	0xFDE80000	64KB	UART2	0xFE660000	64KB
PVTM_NPU	0xFDE90000	64KB	UART3	0xFE670000	64KB
VDPU	0xFDEA0000	64KB	UART4	0xFE680000	64KB
RGA	0xFDEB0000	64KB	UART5	0xFE690000	64KB
EBC	0xFDEC0000	64KB	UART6	0xFE6A0000	64KB
JPEG_DEC	0xFDED0000	64KB	UART7	0xFE6B0000	64KB
JPEG_ENC	0xFDEE0000	64KB	UART8	0xFE6C0000	64KB
IEP	0xFDEF0000	64KB	UART9	0xFE6D0000	64KB
Eink	0xFDF00000	128KB	PWM1	0xFE6E0000	64KB
Reserved	0xFDF20000	128KB	PWM2	0xFE6F0000	64KB
RKVENC	0xFDF40000	128KB	PWM3	0xFE700000	64KB
Reserved	0xFDF60000	128KB	TSADC	0xFE710000	64KB
RKVDEC	0xFDF80000	128KB	SARADC	0xFE720000	64KB
CSI_RX_CTRL0	0xFDFA0000	64KB	Reserved	0xFE730000	64KB
CSI_RX_CTRL1	0xFDFB0000	64KB	GPIO1	0xFE740000	64KB
Reserved	0xFDFC0000	64KB	GPIO2	0xFE750000	64KB
VICAP0	0xFDFD0000	64KB	GPIO3	0xFE760000	64KB
VICAP1	0xFDFE0000	64KB	GPIO4	0xFE770000	64KB
ISP	0xFDFF0000	64KB	Mailbox	0xFE780000	64KB
SDMMC2	0xFE000000	64KB	MCU_INTC	0xFE790000	64KB
GMAC1	0xFE010000	64KB	Reserved	0xFE7A0000	384KB
Reserved	0xFE020000	128KB	DDR_PHY	0xFE800000	64KB

Module	Start Address	Size	Module	Start Address	Size
VOP	0xFE040000	64KB	Reserved	0xFE810000	64KB
HDCP_AHB	0xFE050000	64KB	PIPE_PHY0	0xFE820000	64KB
DSITX0	0xFE060000	64KB	PIPE_PHY1	0xFE830000	64KB
DSITX1	0xFE070000	64KB	PIPE_PHY2	0xFE840000	64KB
HDCP_APB	0xFE080000	128KB	DSI_TX_PHY0	0xFE850000	64KB
HDMI	0xFE0A0000	128KB	DSI_TX_PHY1	0xFE860000	64KB
eDP	0xFE0C0000	64KB	CSI_RX_PHY	0xFE870000	64KB
HDCP_KEY	0xFE0D0000	64KB	OTP_PHY	0xFE880000	64KB
Reserved	0xFE0E0000	128KB	CPU_BOOST	0xFE890000	64KB
Reserved	0xFE100000	1024KB	USB2PHY_U3OTG	0xFE8A0000	64KB
FIREWALL_DDR	0xFE200000	64KB	USB2PHY_U2HOST	0xFE8B0000	64KB
Reserved	0xFE210000	64KB	PCIE30_PHY	0xFE8C0000	128KB
DMA2DDR	0xFE220000	64KB	PCIe2x1_S	0x300000000	1024MB
DFIMON	0xFE230000	64KB	PCIe3x1_S	0x340000000	1024MB
DFICTRL	0xFE240000	64KB	PCIe3x2_S	0x380000000	1024MB
UPCTL2	0xFE250000	64KB	PCIe2x1_DBI	0x3C0000000	4MB
PCIe2x1_APB	0xFE260000	64KB	PCIe3x1_DBI	0x3C0400000	4MB
PCIe3x1_APB	0xFE270000	64KB	PCIe3x2_DBI	0x3C0800000	4MB
PCIe3x2_APB	0xFE280000	64KB			

The following table show the boot address when before remap and after remap

Table 1-2Address Remapping

remap[1:0]=2'b00		remap[1:0]=2'b11		remap[1:0]=2'b10	
		not accessible	BootRom(20KB)	not accessible	BootRom(20KB)
0xFFFF0000	BootRom(20KB)	0xFFFF0000	PMU_SRAM(8KB)	0xFF000000	SYSTEM_SRAM (64KB)
0xFDCD0000	PMU_SRAM(8KB)	0xFDCD0000	PMU_SRAM(8KB)	0xFDCD0000	PMU_SRAM(8KB)
0xFDCC0000	SYSTEM_SRAM (64KB)	0xFDCC0000	SYSTEM_SRAM (64KB)	0xFDCC0000	SYSTEM_SRAM (64KB)

1.2 System Boot

RK3568 provides system boot from off-chip devices such as SDMMC card, eMMC memory, serial Nandor Norflash. When boot code is not ready in these devices, also provide system code download into them by USB OTGinterface. All of the boot code will be stored in internal BootRom. The following is the whole boot procedure for boot code, which will be stored in BootRomin advance.

The following features are supported.

- Support system boot from the following device:
  - Serial Nor Flash, 1bit or 4bits data width(device layout in FSPI IO)
  - Serial Nand Flash, 1bit data width(device layout in FSPI IO)
  - Asynchronous Flash Interface, 8bits data width
  - eMMC Interface, 8bits data width
  - SDMMC Card, 4bits data width
- Support system code download by USB OTG

Following figure shows RK3568boot procedure flow.

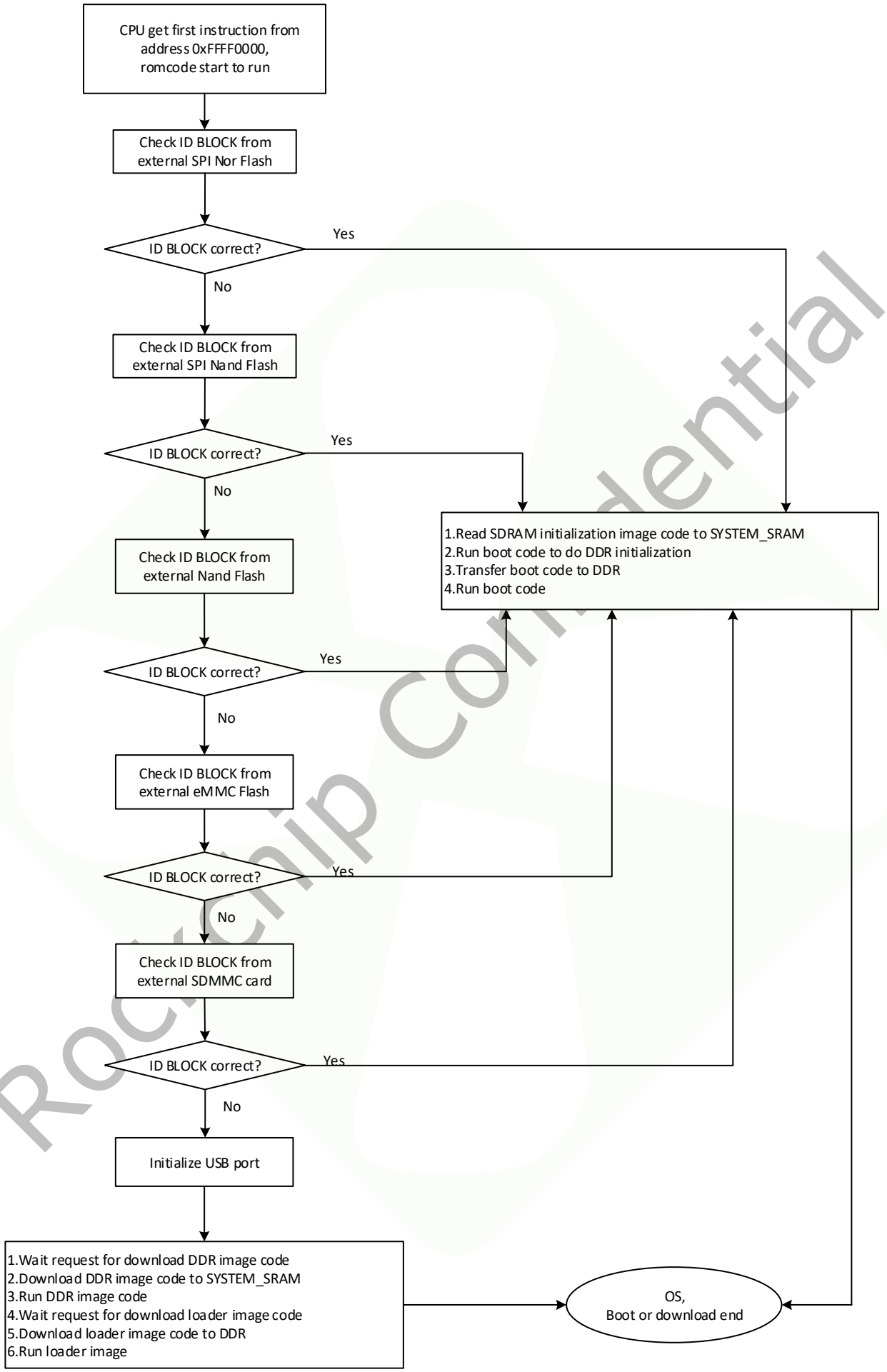


Fig. 1-1RK3568Boot Procedure Flow

1.3 System Interrupt Connection

RK3568 provides an general interrupt controller (GIC) for CPU, which has 256 SPI (shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupt is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-3RK3568 Interrupt Connection List

Number	Source	Polarity	Number	Source	Polarity
0-31 PPI		High level	141	timer0	High level
32	audpwm	High level	142	timer1	High level
33	can0	High level	143	timer2	High level
34	can1	High level	144	timer3	High level
35	can2	High level	145	timer4	High level
36	crypto_ns	High level	146	timer5	High level
37	Reserved	High level	147	tsadc	High level
38	csirx0_1	High level	148	uart0_pmu	High level
39	csirx0_2	High level	149	uart1	High level
40	csirx1_1	High level	150	uart2	High level
41	csirx1_2	High level	151	uart3	High level
42	dcf	High level	152	uart4	High level
43	ddrmon	High level	153	uart5	High level
44	dma2ddr	High level	154	uart6	High level
45	dmac0_abort	High level	155	uart7	High level
46	|dmac0	High level	156	uart8	High level
47	dmac1_abort	High level	157	uart9	High level
48	|dmac1	High level	158	upctl_alert_err	High level
49	ebc	High level	159	upctl_arpoison	High level
50	edp	High level	160	upctl_awpoison	High level
51	emmc	High level	161	usb2host0_arb	High level
52	gic_err	High level	162	usb2host0_ehci	High level
53	gic_fault	High level	163	usb2host0_ohci	High level
54	gic_pmu	High level	164	usb2host1_arb	High level
55	gmac0_lpi	High level	165	usb2host1_ehci	High level
56	gmac0_pmt	High level	166	usb2host1_ohci	High level
57	gmac0_sbd_perch_rx	High level	167	usbphy0_grf	High level
58	gmac0_sbd_perch_tx	High level	168	usbphy1_grf	High level
59	gmac0_sbd	High level	169	vad	High level
60	gmac1_lpi	High level	170	vdpu_mmu	High level
61	gmac1_pmt	High level	171	vdpu_xintdec	High level
62	gmac1_sbd_perch_rx	High level	172	rkvenc_enc	High level
63	gmac1_sbd_perch_tx	High level	173	rkvenc_mmu0	High level
64	gmac1_sbd	High level	174	rkvenc_mmu2	High level
65	gpio0_pmu	High level	175	Reserved	High level
66	gpio1	High level	176	vop_lb	High level
67	gpio2	High level	177	vicap0	High level

Number	Source	Polarity	Number	Source	Polarity
68	gpio3	High level	178	vicap1	High level
69	gpio4	High level	179	vop_ddr	High level
70	gpu_event	High level	180	vop	High level
71	gpu_gpu	High level	181	wdtns	High level
72	gpu_job	High level	182	wdts	High level
73	gpu_mmu	High level	183	npu	High level
74	hdcp	High level	184	sdmmc0_detectn_grf	High level
75	Reserved	High level	185	sdmmc1_detectn_grf	High level
76	hdmi_wakeup	High level	186	sdmmc2_detectn_grf	High level
77	hdmi	High level	187	sdmmc0_dectn_in_flt_grf	High level
78	i2c0_pmu	High level	188	pcie30x1_err	High level
79	i2c1	High level	189	pcie30x1_legacy	High level
80	i2c2	High level	190	pcie30x1_msg_rx	High level
81	i2c3	High level	191	pcie30x1_pmc	High level
82	i2c4	High level	192	pcie30x1_sys	High level
83	i2c5	High level	193	pcie30x2_err	High level
84	i2s0_8ch	High level	194	pcie30x2_legacy	High level
85	i2s1_8ch	High level	195	pcie30x2_msg_rx	High level
86	i2s2_2ch	High level	196	pcie30x2_pmc	High level
87	i2s3_2ch	High level	197	pcie30x2_sys	High level
88	iep	High level	198	key_reader	High level
89	isp_mipi	High level	199	otpc_ns	High level
90	isp_mi	High level	200	otp_s	High level
91	isp_mmu	High level	201	usb3otg0	High level
92	isp	High level	202	usb3otg1	High level
93	jpeg_dec_mmu	High level	203	sbr_done_intr	High level
94	jpeg_dec	High level	204	ecc_corrected_err_intr	High level
95	jpeg_enc_mmu	High level	205	ecc_corrected_err_intr_fault	High level
96	jpeg_enc	High level	206	ecc_uncorrected_err_intr	High level
97	lfps_beacon_multi_phy0	High level	207	ecc_uncorrected_err_intr_fault	High level
98	lfps_beacon_multi_phy1	High level	208	derate_temp_limit_intr	High level
99	lfps_beacon_multi_phy2	High level	209	derate_temp_limit_intr_fault	High level
100	mipi_dsi_0	High level	210	eink	High level
101	mipi_dsi_1	High level	211	Reserved	High level
102	nandc	High level	212	hwffc	High level
103	pcie20_err	High level	213	ahb2axi_i	High level
104	pcie20_legacy	High level	214	ahb2axi_d	High level
105	pcie20_msg_rx	High level	215	mailbox_ca55[0]	High level
106	pcie20_pmc	High level	216	mailbox_ca55[1]	High level
107	pcie20_sys	High level	217	mailbox_ca55[2]	High level
108	pdm	High level	218	mailbox_ca55[3]	High level
109	pmu	High level	219	mailbox_mcu[0]	High level
110	pvtm_core	High level	220	mailbox_mcu[1]	High level

Number	Source	Polarity	Number	Source	Polarity
111	pvtm_gpu	High level	221	mailbox_mcu[2]	High level
112	pvtm_npu	High level	222	mailbox_mcu[3]	High level
113	pvtm_pmu	High level	223	trng_chk	High level
114	pwm_pmu	High level	224	xpcs_sbd	High level
115	pwm1	High level	225	otp_mask	High level
116	pwm2	High level	259:226	Reserved	High level
117	pwm3	High level	260	ca55_pmuirq[0]	High level
118	pwr_pwm_pmu	High level	261	ca55_pmuirq[1]	High level
119	pwr_pwm1	High level	262	ca55_pmuirq[2]	High level
120	pwr_pwm2	High level	263	ca55_pmuirq[3]	High level
121	pwr_pwm3	High level	264	nvcpumntirq[0]	High level
122	rga	High level	265	nvcpumntirq[1]	High level
123	rkvdec_m_dec	High level	266	nvcpumntirq[2]	High level
124	rkvdec_m_mmu	High level	267	nvcpumntirq[3]	High level
125	saradc	High level	268	ncommirq[0]	High level
126	sata0	High level	269	ncommirq[1]	High level
127	sata1	High level	270	ncommirq[2]	High level
128	sata2	High level	271	ncommirq[3]	High level
129	scr	High level	272	nfaultirq[0]	High level
130	sdmmc0	High level	273	nfaultirq[1]	High level
131	sdmmc1	High level	274	nfaultirq[2]	High level
132	sdmmc2	High level	275	nfaultirq[3]	High level
133	fspi	High level	276	nfaultirq[4]	High level
134	spdif_8ch	High level	277	nerrirq[0]	High level
135	spi0	High level	278	nerrirq[1]	High level
136	spi1	High level	279	nerrirq[2]	High level
137	spi2	High level	280	nerrirq[3]	High level
138	spi3	High level	281	nerrirq[4]	High level
139	stimer0	High level	282	nclusterpmuirq	High level
140	stimer1	High level			

1.4 System DMA Hardware Request Connection

RK3568 provides two DMA controller (DMAC) inside the system, the following table is the DMA hardware request list.

Table 1-4RK3568 DMAC Hardware Request Connection List

DMAC0			DMAC1		
Req Number	Source	Polarity	Req Number	Source	Polarity
0	Uart0 tx	High level	0	I2S0_8ch_tx	High level
1	uart0 rx	High level	1	spdif	High level
2	uart1 tx	High level	2	I2S1_8ch_tx	High level
3	uart1 rx	High level	3	I2S1_8ch_rx	High level
4	uart2 tx	High level	4	I2S2_2ch_tx	High level
5	uart2 rx	High level	5	I2S2_2ch_rx	High level
6	uart3 tx	High level	6	I2S3_2ch_tx	High level

DMAC0			DMAC1		
Req Number	**Source**	**Polarity**	**Req Number**	**Source**	**Polarity**
7	uart3 rx	High level	7	I2S3_2ch_rx	High level
8	uart4 tx	High level	8	aupwm	High level
9	uart4 rx	High level	9	pdm	High level
10	uart5 tx	High level	10	sdmmc_buffer	High level
11	uart5 rx	High level	11	can0_tx	High level
12	uart6 tx	High level	12	can0_rx	High level
13	uart6 rx	High level	13	can1_tx	High level
14	uart7 tx	High level	14	can1_rx	High level
15	uart7 rx	High level	15	can2_tx	High level
16	uart8 tx	High level	16	can2_rx	High level
17	uart8 rx	High level	17	Reserved	
18	uart9 tx	High level	18	Reserved	
19	uart9 rx	High level	19	Reserved	
20	spi0_tx	High level	20	Reserved	
21	spi0_rx	High level	21	Reserved	
22	spi1_tx	High level	22	Reserved	
23	spi1_rx	High level	23	Reserved	
24	spi2_tx	High level	24	Reserved	
25	spi2_rx	High level	25	Reserved	
26	spi3_tx	High level	26	Reserved	
27	spi3_rx	High level	27	Reserved	
28	pwm0	High level	28	Reserved	
29	pwm1	High level	29	Reserved	
30	pwm2	High level	30	Reserved	
31	pwm3	High level	31	Reserved	

Chapter 2 Clock & Reset Unit (CRU)

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets in the chip. CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset or temperature sensor.
The CRU islocated at several addresses.

- PMUCRU, used for always on system, with base address 0xFDD00000
- PMUSCRU, used for always on secure system, with base address 0xFDD30000
- CRU, used for general system except always on system, with base address 0xFDD20000
- SCRU, used for general secure system except always on system, with base address 0xFDD10000

The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 6 fractional PLLs and 3 integer PLLs
- Flexible selection of clock source
- Support dividing clock separately
- Support gatingclock separately
- Supportsoftware reset each module separately

2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

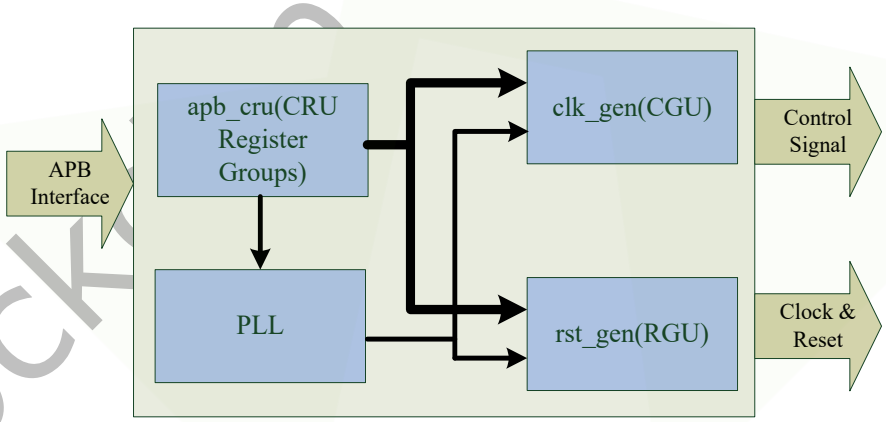


Fig.2-1 CRU Block Diagram

2.3 Function Description

2.3.1 System Clock Solution

There are 6 fractional PLLs in RK3568: APLL, PPLL, HPLL, DPLL, CPLL and GPLL.There are also 3 integer PLLs: MPLL, NPLL and VPLL. Each PLL can only receive 24MHz oscillator as input reference clock and can be set to three work modes: normal mode, slow mode and deep slow mode. When power on or changing PLL setting, we must program PLL into slow mode or deep slow mode.
To maximize the flexibility, some of clocks can select divider source from multiple PLLs.To provide some specific frequency, another solution is integrated: fractional divider. Divfree50

divider and divfreeNP5 divider are also provided for some modules.All clocks can be gated by software.
The basic units for clock generation are:

- Gating
- MUX(multiplexer)
- Divfree(Glitch free divider)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even, the clock duty cycle of clk_out is 50%
  - When divisor is odd, the clock duty cycle of clk_out is not 50%
- Fracdiv(Fractional divider)
  - clk_out_freq=clk_in_freq*numerator/denominator, both numerator and denominator are 16 bits
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even or odd, the clock duty cycle of clk_out is 50%
- DivFreeNP5(Glitch free divider for null point 5)
  - clk_out_freq= 2*clk_in_freq/(2*div_con+3)
  - The clock duty cycle of clk_out is not 50%

The settings of all basic units are controlled by CRU registers.

2.3.2 System Reset Solution

Almost all module have these reset source as the following figure shows. The 'xxx' in the figure is the module name.

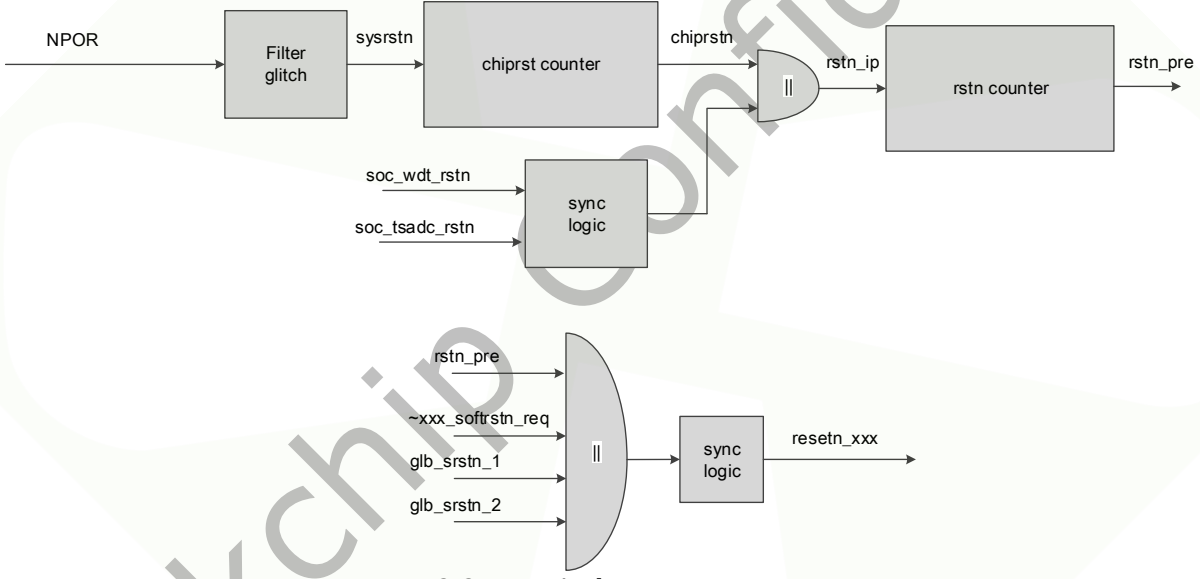


Fig.2-2 Reset Architecture Diagram

Reset source of each reset signal includes:

- NPOR: External power on reset
- soc_wdt_rstn: Reset from WDT module
- soc_tsadc_rstn:Reset from TSADCmodule
- softrstn_req:Software resetrequest by programming CRU_SOFTRST_CON
- glb_srstn_1:First global softwarereset by programming CRU_GLB_SRST_FST as 0xfdb9
- glb_srstn_2:Second global software reset by programming CRU_GLB_SRST_SNDas 0xeca8

2.3.3 Fractional PLL Introduction

The fractional PLLs inside RK3568 output clock's frequency up to 3.8GHz. The PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments.
The PLL supports the following features:

- Inputfrequencyrange:1MHzto 1200MHz for integer modeand10MHzto 1200MHz for fractional mode
- PFD minimum reference frequency range: 1MHz for integer modeand10MHz for fractional mode
- Output frequency range: 19MHzto3.8GHz
- VCO output frequency range:950MHzto3.8GHz
- 24bitfractionalaccuracy,andfractionalmodejitterperformancetonearlymatchintegermodeperformance.
- 4:1VCOfrequencyrangeallowsPLLtobeoptimizedforminimumjitterorminimumpower
- Isolatedanalogsupply(1.8V)allowsforexcellentsupplyrejectioninnoisySoCapplications
- Lock detect signalindicateswhenfrequencylockhasbeenachieved

PLL block diagram is shown below.

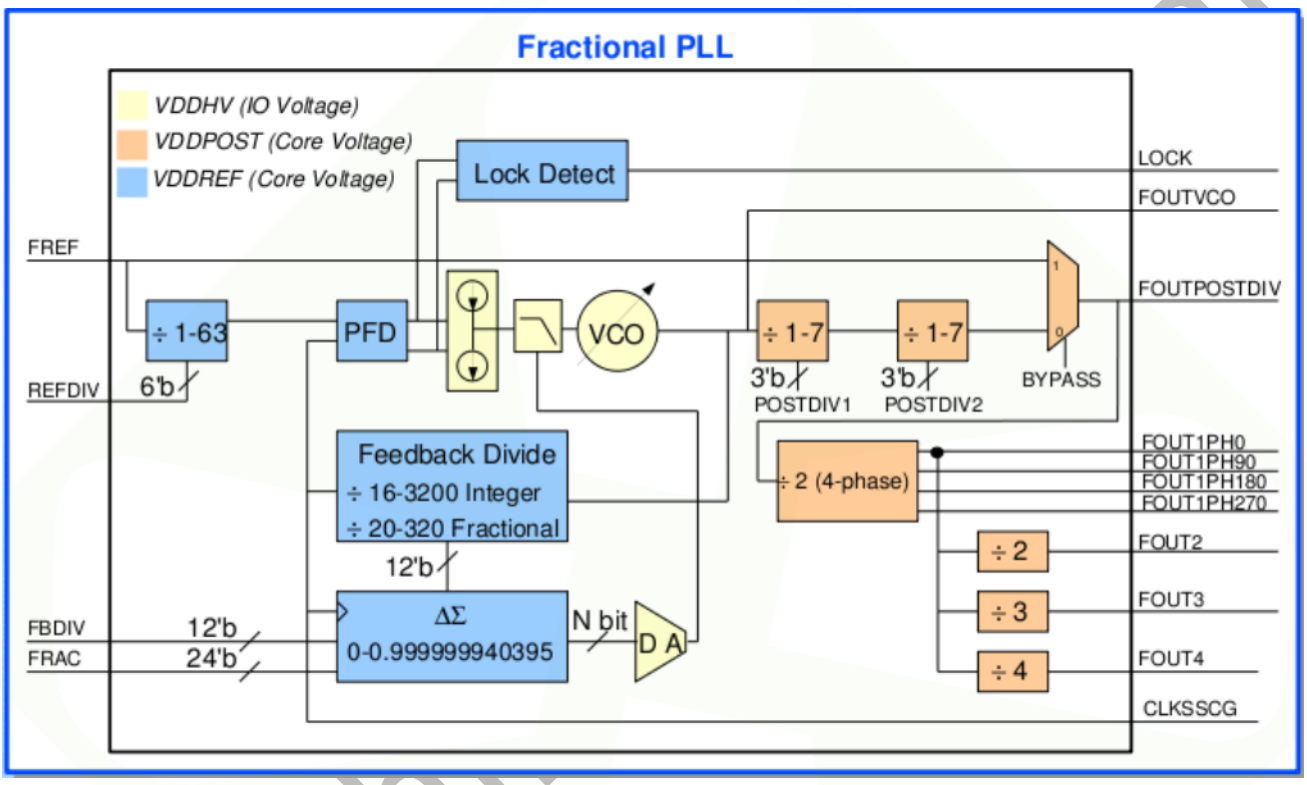


Fig.2-3PLLBlockDiagram

2.3.4 Integer PLL Introduction

The integer PLLs inside RK3568 output clock's frequency up to 1.9GHz. The PLL is a multi-function, general purpose frequency synthesizer optimized for low power digital clocking. Wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for a variety of different application. With excellent supply noise immunity, the PLL is ideal for use in noisy SoC environments.

The PLL supports the following features:

- Inputfrequencyrange:10MHzto800MHz
- PFD minimum reference frequency range: 10MHz
- Output frequency range:9MHzto1.9GHz
- VCO output frequency range:475MHzto1.9GHz
- 4:1VCOfrequencyrangeallowsPLLtobeoptimizedforminimumjitterorminimumpower
- Low period jitter provides maximum timing margin in high frequency designs
- Lock detect signalindicateswhenfrequencylockhasbeenachieved

PLL block diagram is shown below.

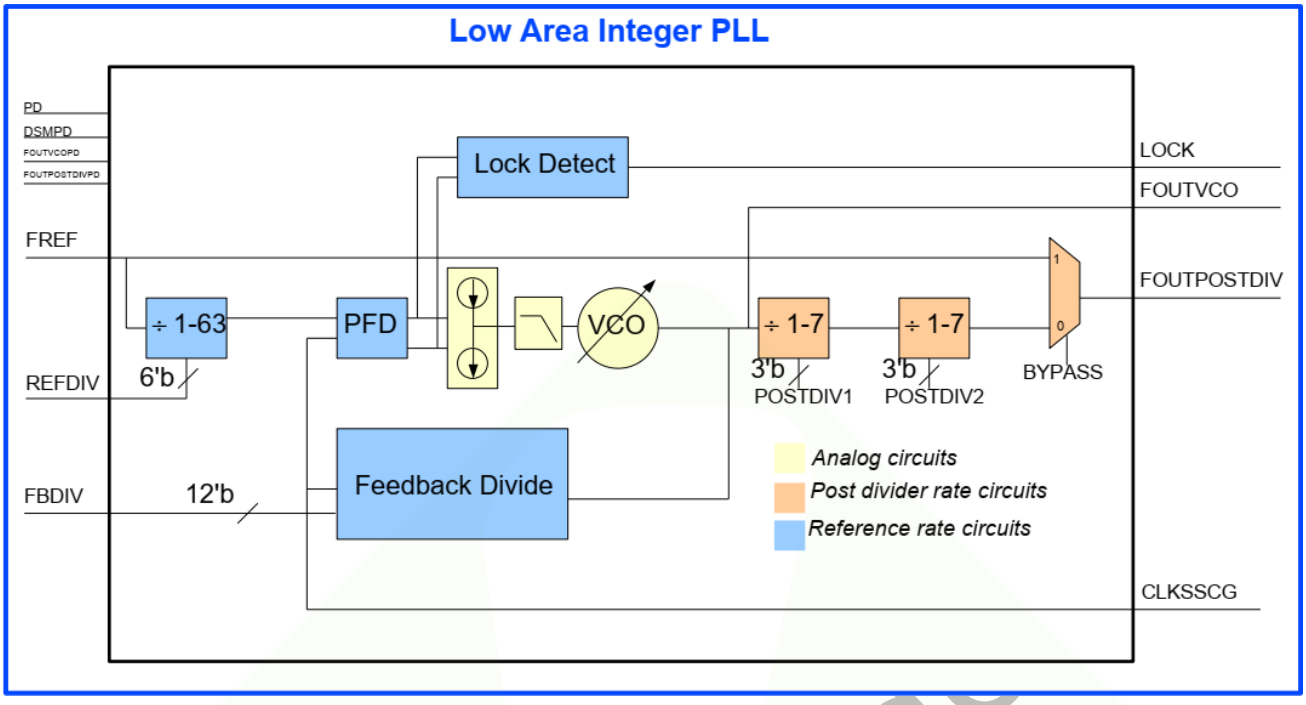


Fig.2-4PLLBlockDiagram

2.4 CRU Register Description

2.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_APLL_CON0	0x0000	W	0x0000107D	APLL configuration register0
CRU_APLL_CON1	0x0004	W	0x00001043	APLL configuration register1
CRU_APLL_CON2	0x0008	W	0x00000000	APLL configuration register2
CRU_APLL_CON3	0x000C	W	0x00000007	APLL configuration register3
CRU_APLL_CON4	0x0010	W	0x00007F00	APLL configuration register4
CRU_DPLL_CON0	0x0020	W	0x000020C8	DPLL configuration register0
CRU_DPLL_CON1	0x0024	W	0x00001083	DPLL configuration register1
CRU_DPLL_CON2	0x0028	W	0x00000000	DPLL configuration register2
CRU_DPLL_CON3	0x002C	W	0x00000007	DPLL configuration register3
CRU_DPLL_CON4	0x0030	W	0x00007F00	DPLL configuration register4
CRU_GPLL_CON0	0x0040	W	0x00001032	GPLL configuration register0
CRU_GPLL_CON1	0x0044	W	0x00001041	GPLL configuration register1
CRU_GPLL_CON2	0x0048	W	0x00000000	GPLL configuration register2
CRU_GPLL_CON3	0x004C	W	0x00000007	GPLL configuration register3
CRU_GPLL_CON4	0x0050	W	0x00007F00	GPLL configuration register4
CRU_CPLL_CON0	0x0060	W	0x0000107D	CPLL configuration register0
CRU_CPLL_CON1	0x0064	W	0x00001043	CPLL configuration register1
CRU_CPLL_CON2	0x0068	W	0x00000000	CPLL configuration register2
CRU_CPLL_CON3	0x006C	W	0x00000007	CPLL configuration register3
CRU_CPLL_CON4	0x0070	W	0x00007F00	CPLL configuration register4
CRU_NPLL_CON0	0x0080	W	0x00001032	NPLL configuration register0
CRU_NPLL_CON1	0x0084	W	0x00001041	NPLL configuration register1
CRU_VPLL_CON0	0x00A0	W	0x0000307D	VPLL configuration register0
CRU_VPLL_CON1	0x00A4	W	0x00001042	VPLL configuration register1
CRU_MODE_CON00	0x00C0	W	0x00000000	Mode register
CRU_MISC_CON0	0x00C4	W	0x00000000	Misc register 0
CRU_MISC_CON1	0x00C8	W	0x00000000	Misc register 1

Name	Offset	Size	Reset Value	Description
CRU_MISC_CON2	0x00CC	W	0x00000000	Misc register 2
CRU_GLB_CNT_TH	0x00D0	W	0x00640064	GLB_CNT_TH
CRU_GLB_SRST_FST	0x00D4	W	0x00000000	GLB_SRST_FST
CRU_GLB_SRST_SND	0x00D8	W	0x00000000	GLB_SRST_SND
CRU_GLB_RST_CON	0x00DC	W	0x00000000	GLB_RST_CON
CRU_GLB_RST_ST	0x00E0	W	0x00000000	GLB_RST_ST
CRU_CLKSEL_CON00	0x0100	W	0x00000000	Internal clock select and division register 0
CRU_CLKSEL_CON01	0x0104	W	0x00000000	Internal clock select and division register 1
CRU_CLKSEL_CON02	0x0108	W	0x00000000	Internal clock select and division register 2
CRU_CLKSEL_CON03	0x010C	W	0x00000303	Internal clock select and division register 3
CRU_CLKSEL_CON04	0x0110	W	0x00000303	Internal clock select and division register 4
CRU_CLKSEL_CON05	0x0114	W	0x00000111	Internal clock select and division register 5
CRU_CLKSEL_CON06	0x0118	W	0x00004081	Internal clock select and division register 6
CRU_CLKSEL_CON07	0x011C	W	0x00000011	Internal clock select and division register 7
CRU_CLKSEL_CON08	0x0120	W	0x00000053	Internal clock select and division register 8
CRU_CLKSEL_CON09	0x0124	W	0x00000000	Internal clock select and division register 9
CRU_CLKSEL_CON10	0x0128	W	0x00000001	Internal clock select and division register 10
CRU_CLKSEL_CON11	0x012C	W	0x00008113	Internal clock select and division register 11
CRU_CLKSEL_CON12	0x0130	W	0x00000000	Internal clock select and division register 12
CRU_CLKSEL_CON13	0x0134	W	0x00008113	Internal clock select and division register 13
CRU_CLKSEL_CON14	0x0138	W	0x00000000	Internal clock select and division register 14
CRU_CLKSEL_CON15	0x013C	W	0x00008113	Internal clock select and division register 15
CRU_CLKSEL_CON16	0x0140	W	0x00000000	Internal clock select and division register 16
CRU_CLKSEL_CON17	0x0144	W	0x00008113	Internal clock select and division register 17
CRU_CLKSEL_CON18	0x0148	W	0x00000000	Internal clock select and division register 18
CRU_CLKSEL_CON19	0x014C	W	0x00008113	Internal clock select and division register 19
CRU_CLKSEL_CON20	0x0150	W	0x00000000	Internal clock select and division register 20
CRU_CLKSEL_CON21	0x0154	W	0x00008113	Internal clock select and division register 21
CRU_CLKSEL_CON22	0x0158	W	0x00000000	Internal clock select and division register 22

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON23	0x015C	W	0x00000013	Internal clock select and division register 23
CRU_CLKSEL_CON24	0x0160	W	0x00000000	Internal clock select and division register 24
CRU_CLKSEL_CON25	0x0164	W	0x0000000B	Internal clock select and division register 25
CRU_CLKSEL_CON26	0x0168	W	0x00000000	Internal clock select and division register 26
CRU_CLKSEL_CON27	0x016C	W	0x00000000	Internal clock select and division register 27
CRU_CLKSEL_CON28	0x0170	W	0x00000000	Internal clock select and division register 28
CRU_CLKSEL_CON29	0x0174	W	0x00000030	Internal clock select and division register 29
CRU_CLKSEL_CON30	0x0178	W	0x00000020	Internal clock select and division register 30
CRU_CLKSEL_CON31	0x017C	W	0x00000000	Internal clock select and division register 31
CRU_CLKSEL_CON32	0x0180	W	0x00000020	Internal clock select and division register 32
CRU_CLKSEL_CON33	0x0184	W	0x00000000	Internal clock select and division register 33
CRU_CLKSEL_CON34	0x0188	W	0x00000310	Internal clock select and division register 34
CRU_CLKSEL_CON35	0x018C	W	0x0000C001	Internal clock select and division register 35
CRU_CLKSEL_CON36	0x0190	W	0x0000C0C0	Internal clock select and division register 36
CRU_CLKSEL_CON37	0x0194	W	0x00003100	Internal clock select and division register 37
CRU_CLKSEL_CON38	0x0198	W	0x00000001	Internal clock select and division register 38
CRU_CLKSEL_CON39	0x019C	W	0x00000000	Internal clock select and division register 39
CRU_CLKSEL_CON40	0x01A0	W	0x00000001	Internal clock select and division register 40
CRU_CLKSEL_CON41	0x01A4	W	0x00000003	Internal clock select and division register 41
CRU_CLKSEL_CON42	0x01A8	W	0x00000103	Internal clock select and division register 42
CRU_CLKSEL_CON43	0x01AC	W	0x00002100	Internal clock select and division register 43
CRU_CLKSEL_CON44	0x01B0	W	0x00000203	Internal clock select and division register 44
CRU_CLKSEL_CON45	0x01B4	W	0x00000003	Internal clock select and division register 45
CRU_CLKSEL_CON47	0x01BC	W	0x00000102	Internal clock select and division register 47
CRU_CLKSEL_CON48	0x01C0	W	0x00000003	Internal clock select and division register 48
CRU_CLKSEL_CON49	0x01C4	W	0x00000301	Internal clock select and division register 49

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON50	0x01C8	W	0x00000000	Internal clock select and division register 50
CRU_CLKSEL_CON51	0x01CC	W	0x00001300	Internal clock select and division register 51
CRU_CLKSEL_CON52	0x01D0	W	0x0000200B	Internal clock select and division register 52
CRU_CLKSEL_CON53	0x01D4	W	0x00000000	Internal clock select and division register 53
CRU_CLKSEL_CON54	0x01D8	W	0x0000200B	Internal clock select and division register 54
CRU_CLKSEL_CON55	0x01DC	W	0x00000000	Internal clock select and division register 55
CRU_CLKSEL_CON56	0x01E0	W	0x0000200B	Internal clock select and division register 56
CRU_CLKSEL_CON57	0x01E4	W	0x00000000	Internal clock select and division register 57
CRU_CLKSEL_CON58	0x01E8	W	0x0000200B	Internal clock select and division register 58
CRU_CLKSEL_CON59	0x01EC	W	0x00000000	Internal clock select and division register 59
CRU_CLKSEL_CON60	0x01F0	W	0x0000200B	Internal clock select and division register 60
CRU_CLKSEL_CON61	0x01F4	W	0x00000000	Internal clock select and division register 61
CRU_CLKSEL_CON62	0x01F8	W	0x0000200B	Internal clock select and division register 62
CRU_CLKSEL_CON63	0x01FC	W	0x00000000	Internal clock select and division register 63
CRU_CLKSEL_CON64	0x0200	W	0x0000200B	Internal clock select and division register 64
CRU_CLKSEL_CON65	0x0204	W	0x00000000	Internal clock select and division register 65
CRU_CLKSEL_CON66	0x0208	W	0x0000200B	Internal clock select and division register 66
CRU_CLKSEL_CON67	0x020C	W	0x00000000	Internal clock select and division register 67
CRU_CLKSEL_CON68	0x0210	W	0x0000200B	Internal clock select and division register 68
CRU_CLKSEL_CON69	0x0214	W	0x00000000	Internal clock select and division register 69
CRU_CLKSEL_CON70	0x0218	W	0x00000303	Internal clock select and division register 70
CRU_CLKSEL_CON71	0x021C	W	0x00000203	Internal clock select and division register 71
CRU_CLKSEL_CON72	0x0220	W	0x00001500	Internal clock select and division register 72
CRU_CLKSEL_CON73	0x0224	W	0x00000000	Internal clock select and division register 73
CRU_CLKSEL_CON74	0x0228	W	0x0000001F	Internal clock select and division register 74
CRU_CLKSEL_CON75	0x022C	W	0x00000302	Internal clock select and division register 75

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON76	0x0230	W	0x00000705	Internal clock select and division register 76
CRU_CLKSEL_CON77	0x0234	W	0x00000F0B	Internal clock select and division register 77
CRU_CLKSEL_CON78	0x0238	W	0x0000013B	Internal clock select and division register 78
CRU_CLKSEL_CON79	0x023C	W	0x00000302	Internal clock select and division register 79
CRU_CLKSEL_CON80	0x0240	W	0x00000F07	Internal clock select and division register 80
CRU_CLKSEL_CON81	0x0244	W	0x00002713	Internal clock select and division register 81
CRU_CLKSEL_CON82	0x0248	W	0x00001F09	Internal clock select and division register 82
CRU_CLKSEL_CON83	0x024C	W	0x00008113	Internal clock select and division register 83
CRU_CLKSEL_CON84	0x0250	W	0x00000000	Internal clock select and division register 84
CRU_GATE_CON00	0x0300	W	0x00000000	Internal clock gate and division register 0
CRU_GATE_CON01	0x0304	W	0x00000000	Internal clock gate and division register 1
CRU_GATE_CON02	0x0308	W	0x00000000	Internal clock gate and division register 2
CRU_GATE_CON03	0x030C	W	0x00000000	Internal clock gate and division register 3
CRU_GATE_CON04	0x0310	W	0x00000000	Internal clock gate and division register 4
CRU_GATE_CON05	0x0314	W	0x00000000	Internal clock gate and division register 5
CRU_GATE_CON06	0x0318	W	0x00000000	Internal clock gate and division register 6
CRU_GATE_CON07	0x031C	W	0x00000000	Internal clock gate and division register 7
CRU_GATE_CON08	0x0320	W	0x00000000	Internal clock gate and division register 8
CRU_GATE_CON09	0x0324	W	0x00000000	Internal clock gate and division register 9
CRU_GATE_CON10	0x0328	W	0x00000000	Internal clock gate and division register 10
CRU_GATE_CON11	0x032C	W	0x00000000	Internal clock gate and division register 11
CRU_GATE_CON12	0x0330	W	0x00000000	Internal clock gate and division register 12
CRU_GATE_CON13	0x0334	W	0x00000000	Internal clock gate and division register 13
CRU_GATE_CON14	0x0338	W	0x00000000	Internal clock gate and division register 14
CRU_GATE_CON15	0x033C	W	0x00000000	Internal clock gate and division register 15
CRU_GATE_CON16	0x0340	W	0x00000000	Internal clock gate and division register 16

Name	Offset	Size	Reset Value	Description
CRU_GATE_CON17	0x0344	W	0x00000000	Internal clock gate and division register 17
CRU_GATE_CON18	0x0348	W	0x00000000	Internal clock gate and division register 18
CRU_GATE_CON19	0x034C	W	0x00000000	Internal clock gate and division register 19
CRU_GATE_CON20	0x0350	W	0x00000000	Internal clock gate and division register 20
CRU_GATE_CON21	0x0354	W	0x00000000	Internal clock gate and division register 21
CRU_GATE_CON22	0x0358	W	0x00000000	Internal clock gate and division register 22
CRU_GATE_CON23	0x035C	W	0x00000000	Internal clock gate and division register 23
CRU_GATE_CON24	0x0360	W	0x00000000	Internal clock gate and division register 24
CRU_GATE_CON25	0x0364	W	0x00000000	Internal clock gate and division register 25
CRU_GATE_CON26	0x0368	W	0x00000000	Internal clock gate and division register 26
CRU_GATE_CON27	0x036C	W	0x00000000	Internal clock gate and division register 27
CRU_GATE_CON28	0x0370	W	0x00000000	Internal clock gate and division register 28
CRU_GATE_CON29	0x0374	W	0x00000000	Internal clock gate and division register 29
CRU_GATE_CON30	0x0378	W	0x00000000	Internal clock gate and division register 30
CRU_GATE_CON31	0x037C	W	0x00000000	Internal clock gate and division register 31
CRU_GATE_CON32	0x0380	W	0x00000000	Internal clock gate and division register 32
CRU_GATE_CON33	0x0384	W	0x00000000	Internal clock gate and division register 33
CRU_GATE_CON34	0x0388	W	0x00000000	Internal clock gate and division register 34
CRU_GATE_CON35	0x038C	W	0x00000000	Internal clock gate and division register 35
CRU_SOFTRST_CON00	0x0400	W	0x00000000	Internal clock reset register 0
CRU_SOFTRST_CON01	0x0404	W	0x00000000	Internal clock reset register 1
CRU_SOFTRST_CON02	0x0408	W	0x00000000	Internal clock reset register 2
CRU_SOFTRST_CON03	0x040C	W	0x00000000	Internal clock reset register 3
CRU_SOFTRST_CON04	0x0410	W	0x00000000	Internal clock reset register 4
CRU_SOFTRST_CON05	0x0414	W	0x00000000	Internal clock reset register 5
CRU_SOFTRST_CON06	0x0418	W	0x00000000	Internal clock reset register 6
CRU_SOFTRST_CON07	0x041C	W	0x00000000	Internal clock reset register 7
CRU_SOFTRST_CON08	0x0420	W	0x00000000	Internal clock reset register 8
CRU_SOFTRST_CON09	0x0424	W	0x00000000	Internal clock reset register 9
CRU_SOFTRST_CON10	0x0428	W	0x00000000	Internal clock reset register 10
CRU_SOFTRST_CON11	0x042C	W	0x00000000	Internal clock reset register 11
CRU_SOFTRST_CON12	0x0430	W	0x00000000	Internal clock reset register 12
CRU_SOFTRST_CON13	0x0434	W	0x00000000	Internal clock reset register 13
CRU_SOFTRST_CON14	0x0438	W	0x00000000	Internal clock reset register 14

Name	Offset	Size	Reset Value	Description
CRU_SOFTRST_CON15	0x043C	W	0x00000000	Internal clock reset register 15
CRU_SOFTRST_CON16	0x0440	W	0x00000000	Internal clock reset register 16
CRU_SOFTRST_CON17	0x0444	W	0x00000000	Internal clock reset register 17
CRU_SOFTRST_CON18	0x0448	W	0x00000000	Internal clock reset register 18
CRU_SOFTRST_CON19	0x044C	W	0x00000000	Internal clock reset register 19
CRU_SOFTRST_CON20	0x0450	W	0x00000000	Internal clock reset register 20
CRU_SOFTRST_CON21	0x0454	W	0x00000000	Internal clock reset register 21
CRU_SOFTRST_CON22	0x0458	W	0x00000000	Internal clock reset register 22
CRU_SOFTRST_CON23	0x045C	W	0x00000000	Internal clock reset register 23
CRU_SOFTRST_CON24	0x0460	W	0x00000000	Internal clock reset register 24
CRU_SOFTRST_CON25	0x0464	W	0x00000000	Internal clock reset register 25
CRU_SOFTRST_CON26	0x0468	W	0x00000400	Internal clock reset register 26
CRU_SOFTRST_CON27	0x046C	W	0x00000000	Internal clock reset register 27
CRU_SOFTRST_CON28	0x0470	W	0x00000000	Internal clock reset register 28
CRU_SOFTRST_CON29	0x0474	W	0x00000000	Internal clock reset register 29
CRU_SSGTBL0_3	0x0480	W	0x00000000	External wave table register0
CRU_SSGTBL4_7	0x0484	W	0x00000000	External wave table register1
CRU_SSGTBL8_11	0x0488	W	0x00000000	External wave table register2
CRU_SSGTBL12_15	0x048C	W	0x00000000	External wave table register3
CRU_SSGTBL16_19	0x0490	W	0x00000000	External wave table register4
CRU_SSGTBL20_23	0x0494	W	0x00000000	External wave table register5
CRU_SSGTBL24_27	0x0498	W	0x00000000	External wave table register6
CRU_SSGTBL28_31	0x049C	W	0x00000000	External wave table register7
CRU_SSGTBL32_35	0x04A0	W	0x00000000	External wave table register8
CRU_SSGTBL36_39	0x04A4	W	0x00000000	External wave table register9
CRU_SSGTBL40_43	0x04A8	W	0x00000000	External wave table register10
CRU_SSGTBL44_47	0x04AC	W	0x00000000	External wave table register11
CRU_SSGTBL48_51	0x04B0	W	0x00000000	External wave table register12
CRU_SSGTBL52_55	0x04B4	W	0x00000000	External wave table register13
CRU_SSGTBL56_59	0x04B8	W	0x00000000	External wave table register14
CRU_SSGTBL60_63	0x04BC	W	0x00000000	External wave table register15
CRU_SSGTBL64_67	0x04C0	W	0x00000000	External wave table register16
CRU_SSGTBL68_71	0x04C4	W	0x00000000	External wave table register17
CRU_SSGTBL72_75	0x04C8	W	0x00000000	External wave table register18
CRU_SSGTBL76_79	0x04CC	W	0x00000000	External wave table register19
CRU_SSGTBL80_83	0x04D0	W	0x00000000	External wave table register20
CRU_SSGTBL84_87	0x04D4	W	0x00000000	External wave table register21
CRU_SSGTBL88_91	0x04D8	W	0x00000000	External wave table register22
CRU_SSGTBL92_95	0x04DC	W	0x00000000	External wave table register23
CRU_SSGTBL96_99	0x04E0	W	0x00000000	External wave table register24
CRU_SSGTBL100_103	0x04E4	W	0x00000000	External wave table register25
CRU_SSGTBL104_107	0x04E8	W	0x00000000	External wave table register26
CRU_SSGTBL108_111	0x04EC	W	0x00000000	External wave table register27
CRU_SSGTBL112_115	0x04F0	W	0x00000000	External wave table register28
CRU_SSGTBL116_119	0x04F4	W	0x00000000	External wave table register29
CRU_SSGTBL120_123	0x04F8	W	0x00000000	External wave table register30
CRU_SSGTBL124_127	0x04FC	W	0x00000000	External wave table register31
CRU_AUTOCS_CORE_CON0	0x0500	W	0x00040020	Pdcore auto clock swith control 0
CRU_AUTOCS_CORE_CON1	0x0504	W	0x00000000	Pdcore auto clock swith control 1
CRU_AUTOCS_GPU_CON0	0x0508	W	0x00040020	Pdgpu auto clock swith control 0

Name	Offset	Size	Reset Value	Description
CRU_AUTOCS_GPU_CON1	0x050C	W	0x00000000	Pdgpu auto clock swith control 1
CRU_AUTOCS_BUS_CON0	0x0510	W	0x00040020	Pdbus auto clock swith control 0
CRU_AUTOCS_BUS_CON1	0x0514	W	0x00000000	Pdbus auto clock swith control 1
CRU_AUTOCS_TOP_CON0	0x0518	W	0x00040020	Top auto clock swith control 0
CRU_AUTOCS_TOP_CON1	0x051C	W	0x00000000	Top auto clock swith control 1
CRU_AUTOCS_RKVDEC_CON0	0x0520	W	0x00040020	Rkvdec auto clock swith control 0
CRU_AUTOCS_RKVDEC_CON1	0x0524	W	0x00000000	Rkvdec auto clock swith control 1
CRU_AUTOCS_RKVENC_CON0	0x0528	W	0x00040020	Rkvenc auto clock swith control 0
CRU_AUTOCS_RKVENC_CON1	0x052C	W	0x00000000	Rkvenc auto clock swith control 1
CRU_AUTOCS_VPU_CON0	0x0530	W	0x00040020	Vpu auto clock swith control 0
CRU_AUTOCS_VPU_CON1	0x0534	W	0x00000000	Vpu auto clock swith control 1
CRU_AUTOCS_PERI_CON0	0x0538	W	0x00040020	Pdperi auto clock swith control 0
CRU_AUTOCS_PERI_CON1	0x053C	W	0x00000000	Pdperi auto clock swith control 1
CRU_AUTOCS_GPLL_CON0	0x0540	W	0x00040020	Gpll auto clock swith control 0
CRU_AUTOCS_GPLL_CON1	0x0544	W	0x00000000	Gpll auto clock swith control 1
CRU_AUTOCS_CPLL_CON0	0x0548	W	0x00040020	Cpll auto clock swith control 0
CRU_AUTOCS_CPLL_CON1	0x054C	W	0x00000000	Cpll auto clock swith control 1
CRU_SDMMC0_CON0	0x0580	W	0x00000004	SDMMC control0
CRU_SDMMC0_CON1	0x0584	W	0x00000000	SDMMC control1
CRU_SDMMC1_CON0	0x0588	W	0x00000004	SDMMC control0
CRU_SDMMC1_CON1	0x058C	W	0x00000000	SDMMC control1
CRU_SDMMC2_CON0	0x0590	W	0x00000004	SDMMC2 control0
CRU_SDMMC2_CON1	0x0594	W	0x00000000	SDMMC2 control1
CRU_EMMC_CON0	0x0598	W	0x00000004	EMMC control0
CRU_EMMC_CON1	0x059C	W	0x00000000	EMMC control1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2 Detail Registers Description

CRU_APLL_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)

Bit	Attr	Reset Value	Description
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_APLL_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x03	refdiv Reference Clock Divide Value, (1-63)

CRU_APLL_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down

Bit	Attr	Reset Value	Description
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_APLL_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_APLL_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_DPLL_CON0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x0c8	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_DPLL_CON1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable, 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:6	RW	0x2	postdiv2 Second Post Divide Value (1-7)
5:0	RW	0x03	refdiv Reference Clock Divide Value (1-63)

CRU_DPLL_CON2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_DPLL_CON3

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset

Bit	Attr	Reset Value	Description
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_DPLL_CON4

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs, (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_GPLL_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x032	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_GPLL_CON1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted

Bit	Attr	Reset Value	Description
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value (1-63)

CRU_GPLL_CON2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_GPLL_CON3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_GPLL_CON4

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_CPLL_CON0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass

Bit	Attr	Reset Value	Description
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_CPLL_CON1

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x03	refdiv Reference Clock Divide Value, (1-63)

CRU_CPLL_CON2

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down

Bit	Attr	Reset Value	Description
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_CPLL_CON3

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

CRU_CPLL_CON4

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

CRU_NPLL_CON0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x032	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_NPLL_CON1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down

Bit	Attr	Reset Value	Description
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

CRU_VPLL_CON0

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

CRU_VPLL_CON1

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down

Bit	Attr	Reset Value	Description
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

CRU_MODE_CON00

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	usbphy480m_pll_mode usbphy480m_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: usbphy480m 2'b10: clk_rtc_32k
13:12	RW	0x0	clk_vpll_mode clk_vpll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_vpll 2'b10: clk_rtc_32k
11:10	RW	0x0	clk_npll_mode clk_npll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_npll 2'b10: clk_rtc_32k
9:8	RO	0x0	reserved
7:6	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_gpll 2'b10: clk_rtc_32k
5:4	RW	0x0	clk_cpll_mode clk_cpll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_cpll 2'b10: clk_rtc_32k

Bit	Attr	Reset Value	Description
3:2	RW	0x0	clk_dpll_mode clk_dpll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_dpll 2'b10: clk_rtc_32k
1:0	RW	0x0	clk_apll_mode clk_apll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_apll 2'b10: clk_rtc_32k

CRU_MISC_CON0

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gpu_clk_gate_ema_ena When enable, gate gpu clock when change pd_gpu ema value 1'b1: enable 1'b0: disable
14	RW	0x0	cpu_clk_gate_ema_ena When enable, gate cpu clock when change pd_core ema value 1'b1: enable 1'b0: disable
13	RW	0x0	hwffc_clk_switch2cru_ena DDR hwffc clock switch enable 1'b1: enable 1'b0: disable
12	RW	0x0	dbgrst_en core dbgrst request enable 1'b1: enable 1'b0: disable
11	RW	0x0	qchannel_gating_enable When enable, clock will be gated when q-channel handshake completed 1'b1: enable clock gating 1'b0: only q-channel handshake occurs, clock will not be gated
10	RW	0x0	qchannel_ena_clk_gic600 clk_gic600 q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
9	RW	0x0	qchannel_ena_clk_pdgic_gic2core clk_pdgic_gic2core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
8	RW	0x0	qchannel_ena_clk_pdgic_core2gic clk_pdgic_core2gic q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
7	RW	0x0	qchannel_ena_clk_pdcore_gic2core clk_pdcore_gic2core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel

Bit	Attr	Reset Value	Description
6	RW	0x0	qchannel_ena_clk_pdcore_core2gic clk_pdcore_core2gic q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
5	RW	0x0	qchannel_ena_clk_gpu clk_gpu q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
4	RW	0x0	qchannel_ena_pdbgclk_core Pdbgclk_core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
3	RW	0x0	qchannel_ena_gicclk_core Gicclk_core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
2	RW	0x0	qchannel_ena_atclk_core Atclk_core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
1	RW	0x0	qchannel_ena_pclk_core Pclk_core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel
0	RW	0x0	qchannel_ena_sclk_core Sclk_core q-channel handshake enable 1'b1: enable clock q-channel 1'b0: disable clock q-channel

CRU_MISC_CON1

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pd_bus_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
14	RW	0x0	pd_rkvdec_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
13	RW	0x0	pd_rkvenc_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
12	RW	0x0	pd_vpu_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off

Bit	Attr	Reset Value	Description
11	RW	0x0	pd_rga_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
10	RW	0x0	pd_vo_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
9	RW	0x0	pd_vi_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
8	RW	0x0	pd_usb_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
7:6	RO	0x0	reserved
5	RW	0x0	pd_pipe_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
4	RW	0x0	pd_peri_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
3	RW	0x0	pd_ddr_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
2	RW	0x0	pd_npu_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
1	RW	0x0	pd_gpu_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off
0	RW	0x0	pd_core_dwn_clk_en_mask Clock on when power domain is power off 1'b1: clock on when power off 1'b0: clock off when power off

CRU_MISC_CON2

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usbphy480m_src_sel usbphy480m source select 1'b1: usbphy1 1'b0: usbphy0
14:10	RO	0x00	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_rkvdec_hevc_ca_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
8	RW	0x0	clk_rkvdec_ca_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
7	RW	0x0	clk_rkvdec_core_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
6	RW	0x0	aclk_rkvdec_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
5	RW	0x0	clk_rkvenc_core_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
4	RW	0x0	hclk_rkvenc_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
3	RW	0x0	aclk_rkvenc_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
2	RW	0x0	aclk_vpu_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
1	RW	0x0	clk_iep_core_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable
0	RW	0x0	clk_rga_core_idle_enable clock will be gated when idle 1'b1: enable 1'b0: disable

CRU_GLB_CNT_TH

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0064	Reserved
15:0	RW	0x0064	global_reset_counter_threshold Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles

CRU_GLB_SRST_FST

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	GLB_SRST_FST The first global software reset config value

CRU_GLB_SRST_SND

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	GLB_SRST_SND The second global software reset config value

CRU_GLB_RST_CON

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	pmusgrf_crc_chk_glb_srst_ctrl 1'b0: Pmusgrf crc chk trigger second global reset 1'b1: Pmusgrf crc chk trigger first global reset effective when glb_rst_con[11] enable
14	RW	0x0	sgrf_crc_chk_glb_srst_ctrl 1'b0: Sgrf crc chk trigger second global reset 1'b1: Sgrf crc chk trigger first global reset effective when glb_rst_con[10] enable
13	RW	0x0	osc_chk_glb_srst_ctrl 1'b0: Osc chk trigger second global reset 1'b1: Osc chk trigger first global reset effective when glb_rst_con[9] enable
12	RW	0x0	jdb_glb_srst_ctrl 1'b0: Jdb trigger second global reset 1'b1: Jdb trigger first global reset effective when glb_rst_con[8] enable
11	RW	0x0	pmusgrf_crc_chk_glb_srst_ctrl_enable 1'b0: Pmusgrf crc chk dont trigger global reset 1'b1: Pmusgrf crc chk trigger global reset
10	RW	0x0	sgrf_crc_chk_glb_srst_ctrl_enable 1'b0: Sgrf crc chk dont trigger global reset 1'b1: Sgrf crc chk trigger global reset
9	RW	0x0	osc_chk_glb_srst_ctrl_enable 1'b0: Osc chk dont trigger global reset 1'b1: Osc chk trigger global reset
8	RW	0x0	jdb_glb_srst_ctrl_enable 1'b0: Jdb dont trigger global reset 1'b1: Jdb trigger global reset
7	RW	0x0	wdt_reset_ext_en 1: Enable wdt reset extend, reset extend time depend on bit15~0 of GLB_CNT_TH 0: Disable wdt reset extend
6	RW	0x0	tsadc_shut_reset_ext_en 1: Enable tsadc_shut reset extend, reset extend time depend on bit15~0 of GLB_CNT_TH 0: Disable tsadc_shut reset extend
5	RO	0x0	reserved
4	RW	0x0	pmu_srst_wdt_en 0: Enable Wdt reset as pmu reset source 1: Disable Wdt reset as pmu reset source

Bit	Attr	Reset Value	Description
3	RW	0x0	pmu_srst_glb_en 1'b0: global reset trigger pmu reset 1'b1: global reset dont trigger pmu reset
2	RW	0x0	pmu_srst_glb_ctrl 0: Enable first global reset as pmu reset source 1: Enable second global reset as pmu reset source effective when glb_rst_con[3] enable
1	RW	0x0	wdt_glb_srst_ctrl 1'b0: Wdt trigger second global reset 1'b1: Wdt trigger first global reset
0	RW	0x0	tsadc_glb_srst_ctrl 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

CRU_GLB_RST_ST

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	glb_pmusgrf_crc_rst_st global PMUSGRF CRC CHK triggered reset flag 1'b0: Last hot reset is not global PMUSGRF CRC CHK triggered reset 1'b1: Last hot reset is global PMUSGRF CRC CHK triggered reset
8	RW	0x0	glb_sgrf_crc_rst_st global SGRF CRC CHK triggered reset flag 1'b0: Last hot reset is not global SGRF CRC CHK triggered reset 1'b1: Last hot reset is global SGRF CRC CHK triggered reset
7	RW	0x0	glb_osc_chk_rst_st global OSC CHK triggered reset flag 1'b0: Last hot reset is not global OSC CHK triggered reset 1'b1: Last hot reset is global OSC CHK triggered reset
6	RW	0x0	glb_jdb_rst_st global JDB triggered reset flag 1'b0: Last hot reset is not global JDB triggered reset 1'b1: Last hot reset is global JDB triggered reset
5	RW	0x0	snd_glb_wdt_rst_st sencond global WDT triggered reset flag 1'b0: Last hot reset is not sencond global WDT triggered reset 1'b1: Last hot reset is sencond global WDT triggered reset
4	RW	0x0	fst_glb_wdt_rst_st first global WDT triggered reset flag 1'b0: Last hot reset is not first global WDT triggered reset 1'b1: Last hot reset is first global WDT triggered reset
3	RW	0x0	snd_glb_tsadc_rst_st sencond global TSADC triggered reset flag 1'b0: Last hot reset is not sencond global TSADC triggered reset 1'b1: Last hot reset is sencond global TSADC triggered reset
2	RW	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: Last hot reset is not first global TSADC triggered reset 1'b1: Last hot reset is first global TSADC triggered reset
1	RW	0x0	snd_glb_rst_st second global rst flag 1'b0: Last hot reset is not sencond global reset 1'b1: Last hot reset is sencond global reset

Bit	Attr	Reset Value	Description
0	RW	0x0	fst_glb_rst_st first global rst flag 1'b0: Last hot reset is not first global reset 1'b1: Last hot reset is first global reset

CRU_CLKSEL_CON00

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_core_ndft_mux_sel clk_core_ndft_mux clock mux. 1'b0: clk_core 1'b1: core_pvtpll_out
14:13	RO	0x0	reserved
12:8	RW	0x00	clk_core1_div Divide clk_core1 by (div_con + 1)
7	RW	0x0	clk_core_ndft_sel clk_core_ndft clock mux. 1'b0: clk_core_i 1'b1: clk_apll_core
6	RW	0x0	clk_core_i_sel clk_core_i clock mux. 1'b0: clk_apll_mux 1'b1: clk_gpll_mux
5	RO	0x0	reserved
4:0	RW	0x00	clk_core0_div Divide clk_core0 by (div_con + 1)

CRU_CLKSEL_CON01

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	clk_core3_div Divide clk_core3 by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x00	clk_core2_div Divide clk_core2 by (div_con + 1)

CRU_CLKSEL_CON02

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	sclk_core_pre_sel sclk_core_pre clock mux. 1'b0: sclk_core_src 1'b1: clk_npll_core
14:10	RO	0x00	reserved
9:8	RW	0x0	sclk_core_src_sel sclk_core_src clock mux. 2'b00: clk_apll_mux 2'b01: clk_gpll_mux 2'b10: clk_npll_mux
7:4	RO	0x0	reserved
3:0	RW	0x0	sclk_core_src_div Divide sclk_core_src by (div_con + 1)

CRU_CLKSEL_CON03

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	gicclk_core_div Divide gicclk_core by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x03	atclk_core_div Divide atclk_core by (div_con + 1)

CRU_CLKSEL_CON04

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	periphclk_core_pre_div Divide periphclk_core_pre by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x03	pclk_core_pre_div Divide pclk_core_pre by (div_con + 1)

CRU_CLKSEL_CON05

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	aclk_core_biu2bus_sel aclk_core_biu2bus clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux

Bit	Attr	Reset Value	Description
13	RO	0x0	reserved
12:8	RW	0x01	aclk_core_ndft_div Divide aclk_core_ndft by (div_con + 1)
7:0	RW	0x11	Reserved

CRU_CLKSEL_CON06

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x4	pclk_gpu_pre_div Divide pclk_gpu_pre by (div_con + 1)
11	RW	0x0	clk_gpu_pre_mux_sel clk_gpu_pre_mux clock mux. 1'b0: clk_gpu_pre 1'b1: gpu_pvtpll_out
10	RO	0x0	reserved
9:8	RW	0x0	aclk_gpu_pre_div Divide aclk_gpu_pre by (div_con + 1)
7:6	RW	0x2	clk_gpu_pre_sel clk_gpu_pre clock mux. 2'b00: clk_mpll_mux 2'b01: clk_gpll_mux 2'b10: clk_cpll_mux 2'b11: clk_npll_mux
5:4	RO	0x0	reserved
3:0	RW	0x1	clk_gpu_pre_div Divide clk_gpu_pre by (div_con + 1)

CRU_CLKSEL_CON07

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_npu_pre_mux_sel clk_npu_pre_mux clock mux. 1'b0: clk_npu_pre 1'b1: npu_pvtpll_out
14:9	RO	0x00	reserved
8	RW	0x0	clk_npu_pre_ndft_sel clk_npu_pre_ndft clock mux. 1'b0: clk_npu_src 1'b1: clk_npu_np5
7	RW	0x0	clk_npu_np5_sel clk_npu_np5 clock mux. 1'b0: clk_npll_mux 1'b1: clk_gpll_mux

Bit	Attr	Reset Value	Description
6	RW	0x0	clk_npu_src_sel clk_npu_src clock mux. 1'b0: clk_npll_mux 1'b1: clk_gpll_mux
5:4	RW	0x1	clk_npu_np5_div Divide clk_npu_np5 by (div_con + 1)
3:0	RW	0x1	clk_npu_src_div Divide clk_npu_src by (div_con + 1)

CRU_CLKSEL_CON08

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x5	pclk_npu_pre_div Divide pclk_npu_pre by (div_con + 1)
3:0	RW	0x3	hclk_npu_pre_div Divide hclk_npu_pre by (div_con + 1)

CRU_CLKSEL_CON09

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_ddrphy1x_sel clk_ddrphy1x clock mux. 1'b0: clk_ddrphy1x_src 1'b1: clk_dpll_ddr
14:8	RO	0x00	reserved
7:6	RW	0x0	clk_ddrphy1x_src_sel clk_ddrphy1x_src clock mux. 2'b00: clk_dpll_mux 2'b01: clk_gpll_mux 2'b10: clk_cpll_mux
5	RO	0x0	reserved
4:0	RW	0x00	clk_ddrphy1x_src_div Divide clk_ddrphy1x_src by (div_con + 1)

CRU_CLKSEL_CON10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	dclk_sdmmc_buffer_sel dclk_sdmmc_buffer clock mux. 2'b00: clk_gpll_div_100m 2'b01: clk_gpll_div_75m 2'b10: clk_cpll_div_50m
11:10	RW	0x0	hclk_gic_audio_sel hclk_gic_audio clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
9:8	RW	0x0	aclk_gic_audio_sel aclk_gic_audio clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux
7:6	RW	0x0	hclk_perimid_sel hclk_perimid clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
5:4	RW	0x0	aclk_perimid_sel aclk_perimid clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux
3:2	RO	0x0	reserved
1:0	RW	0x1	clk_msch_div Divide clk_msch by (div_con + 1)

CRU_CLKSEL_CON11

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s0_mclkout_tx_sel i2s0_mclkout_tx clock mux. 1'b0: mclk_i2s0_8ch_tx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s0_8ch_tx_sel mclk_i2s0_8ch_tx clock mux. 2'b00: clk_i2s0_8ch_tx_src 2'b01: clk_i2s0_8ch_tx_frac 2'b10: i2s0_mclkin 2'b11: xin_osc0_half

Bit	Attr	Reset Value	Description
9:8	RW	0x1	clk_i2s0_8ch_tx_src_sel clk_i2s0_8ch_tx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s0_8ch_tx_src_div Divide clk_i2s0_8ch_tx_src by (div_con + 1)

CRU_CLKSEL_CON12

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s0_8ch_tx_frac_div clk_i2s0_8ch_tx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s0_mclkout_rx_sel i2s0_mclkout_rx clock mux. 1'b0: mclk_i2s0_8ch_rx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s0_8ch_rx_sel mclk_i2s0_8ch_rx clock mux. 2'b00: clk_i2s0_8ch_rx_src 2'b01: clk_i2s0_8ch_rx_frac 2'b10: i2s0_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s0_8ch_rx_src_sel clk_i2s0_8ch_rx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s0_8ch_rx_src_div Divide clk_i2s0_8ch_rx_src by (div_con + 1)

CRU_CLKSEL_CON14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s0_8ch_rx_frac_div clk_i2s0_8ch_rx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON15

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s1_mclkout_tx_sel i2s1_mclkout_tx clock mux. 1'b0: mclk_i2s1_8ch_tx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s1_8ch_tx_sel mclk_i2s1_8ch_tx clock mux. 2'b00: clk_i2s1_8ch_tx_src 2'b01: clk_i2s1_8ch_tx_frac 2'b10: i2s1_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s1_8ch_tx_src_sel clk_i2s1_8ch_tx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s1_8ch_tx_src_div Divide clk_i2s1_8ch_tx_src by (div_con + 1)

CRU_CLKSEL_CON16

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s1_8ch_tx_frac_div clk_i2s1_8ch_tx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s1_mclkout_rx_sel i2s1_mclkout_rx clock mux. 1'b0: mclk_i2s1_8ch_rx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s1_8ch_rx_sel mclk_i2s1_8ch_rx clock mux. 2'b00: clk_i2s1_8ch_rx_src 2'b01: clk_i2s1_8ch_rx_frac 2'b10: i2s1_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s1_8ch_rx_src_sel clk_i2s1_8ch_rx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s1_8ch_rx_src_div Divide clk_i2s1_8ch_rx_src by (div_con + 1)

CRU_CLKSEL_CON18

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s1_8ch_rx_frac_div clk_i2s1_8ch_rx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON19

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s2_mclkout_sel i2s2_mclkout clock mux. 1'b0: mclk_i2s2_2ch 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s2_2ch_sel mclk_i2s2_2ch clock mux. 2'b00: clk_i2s2_2ch_src 2'b01: clk_i2s2_2ch_frac 2'b10: i2s2_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s2_2ch_src_sel clk_i2s2_2ch_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s2_2ch_src_div Divide clk_i2s2_2ch_src by (div_con + 1)

CRU_CLKSEL_CON20

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s2_2ch_frac_div clk_i2s2_2ch_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON21

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x1	i2s3_mclkout_tx_sel i2s3_mclkout_tx clock mux. 1'b0: mclk_i2s3_2ch_tx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s3_2ch_tx_sel mclk_i2s3_2ch_tx clock mux. 2'b00: clk_i2s3_2ch_tx_src 2'b01: clk_i2s3_2ch_tx_frac 2'b10: i2s3_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s3_2ch_tx_src_sel clk_i2s3_2ch_tx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s3_2ch_tx_src_div Divide clk_i2s3_tx_2ch_src by (div_con + 1)

CRU_CLKSEL_CON22

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s3_2ch_tx_frac_div clk_i2s3_2ch_tx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON23

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_spdif_8ch_sel mclk_spdif_8ch clock mux. 1'b0: mclk_spdif_8ch_src 1'b1: mclk_spdif_8ch_frac
14	RW	0x0	mclk_spdif_8ch_src_sel mclk_spdif_8ch_src clock mux. 1'b0: clk_cpll_mux 1'b1: clk_gpll_mux
13:12	RO	0x0	reserved
11:10	RW	0x0	clk_acdcdig_i2c_sel clk_acdcdig_i2c clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_100m 2'b10: xin_osc0_func_mux 2'b11: clk_cpll_div_100m

Bit	Attr	Reset Value	Description
9:8	RW	0x0	mclk_pdm_sel mclk_pdm clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_cpll_div_250m 2'b10: clk_gpll_div_200m 2'b11: clk_gpll_div_100m
7	RO	0x0	reserved
6:0	RW	0x13	mclk_spdif_8ch_src_div Divide mclk_spdif_8ch_src by (div_con + 1)

CRU_CLKSEL_CON24

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mclk_spdif_8ch_frac_div mclk_spdif_8ch_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON25

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_audpwm_sel sclk_audpwm clock mux. 1'b0: sclk_audpwm_src 1'b1: sclk_audpwm_frac
14	RW	0x0	sclk_audpwm_src_sel sclk_audpwm_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
13:6	RO	0x00	reserved
5:0	RW	0x0b	sclk_audpwm_src_div Divide sclk_audpwm_src by (div_con + 1)

CRU_CLKSEL_CON26

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sclk_audpwm_frac_div sclk_audpwm_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON27

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	clk_crypto_ns_pka_sel clk_crypto_ns_pka clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_gpll_div_100m
5:4	RW	0x0	clk_crypto_ns_core_sel clk_crypto_ns_core clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_gpll_div_100m
3:2	RW	0x0	hclk_secure_flash_sel hclk_secure_flash clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
1:0	RW	0x0	aclk_secure_flash_sel aclk_secure_flash clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON28

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	cclk_emmc_sel cclk_emmc clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_gpll_div_200m 3'b010: clk_gpll_div_150m 3'b011: clk_cpll_div_100m 3'b100: clk_cpll_div_50m 3'b101: clk_osc0_div_375k
11:10	RO	0x0	reserved
9:8	RW	0x0	bclk_emmc_sel bclk_emmc clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_cpll_div_125m
7	RO	0x0	reserved
6:4	RW	0x0	sclk_sfc_sel sclk_sfc clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_cpll_div_50m 3'b010: clk_gpll_div_75m 3'b011: clk_gpll_div_100m 3'b100: clk_cpll_div_125m 3'b101: clk_gpll_div_150m
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	nclk_nandc_sel nclk_nandc clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_cpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON29

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_xpcs_eee_sel clk_xpcs_eee clock mux. 1'b0: clk_gpll_div_200m 1'b1: clk_cpll_div_125m
12:10	RO	0x0	reserved
9	RW	0x0	clk_usb3otg1_suspend_sel clk_usb3otg1_suspend clock mux. 1'b0: xin_osc0_func_mux 1'b1: clk_rtc_32k
8	RW	0x0	clk_usb3otg0_suspend_sel clk_usb3otg0_suspend clock mux. 1'b0: xin_osc0_func_mux 1'b1: clk_rtc_32k
7:4	RW	0x3	pclk_pipe_div Divide pclk_pipe by (div_con + 1)
3:2	RO	0x0	reserved
1:0	RW	0x0	aclk_pipe_sel aclk_pipe clock mux. 2'b00: clk_gpll_div_400m 2'b01: clk_gpll_div_300m 2'b10: clk_gpll_div_200m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON30

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	clk_sdmmc1_sel clk_sdmmc0 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_gpll_div_400m 3'b010: clk_gpll_div_300m 3'b011: clk_cpll_div_100m 3'b100: clk_cpll_div_50m 3'b101: clk_osc0_div_750k
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	clk_sdmmc0_sel clk_sdmmc0 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_gpll_div_400m 3'b010: clk_gpll_div_300m 3'b011: clk_cpll_div_100m 3'b100: clk_cpll_div_50m 3'b101: clk_osc0_div_750k
7:4	RW	0x2	pclk_php_div Divide pclk_php by (div_con + 1)
3:2	RW	0x0	hclk_php_sel hclk_php clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
1:0	RW	0x0	aclk_php_sel aclk_php clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON31

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_mac0_out_sel clk_mac0_out clock mux. 2'b00: clk_cpll_div_125m 2'b01: clk_cpll_div_50m 2'b10: clk_cpll_div_25m 2'b11: xin_osc0_func_mux
13:12	RW	0x0	clk_gmac0_ptp_ref_sel clk_gmac0_ptp_ref clock mux. 2'b00: clk_cpll_div_62p5 2'b01: clk_gpll_div_100m 2'b10: clk_cpll_div_50m 2'b11: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_mac0_2top_sel clk_mac0_2top clock mux. 2'b00: clk_cpll_div_125m 2'b01: clk_cpll_div_50m 2'b10: clk_cpll_div_25m 2'b11: clk_ppll_mux
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	rgmii0_clk_sel clock speed in rgmii mode 2'b00: 125M 2'b01: 125M 2'b10: 2.5M 2'b11: 25M
3	RW	0x0	rmii0_clk_sel clock speed in rmii mode 1'b0: 2.5M 1'b1: 25M
2	RW	0x0	rmii0_extclk_sel rmii0_extclk_sel 1'b0: mac0 clock from SOC 1'b1: mac0 clock from IO
1:0	RW	0x0	rmii0_mode rmii0_mode 2'b00: rgmii mode 2'b01: rmii mode 2'b10: gmii mode

CRU_CLKSEL_CON32

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	clk_sdmmc2_sel clk_sdmmc0 clock mux. 3'b000: xin_osc0_func_mux 3'b001: clk_gpll_div_400m 3'b010: clk_gpll_div_300m 3'b011: clk_cpll_div_100m 3'b100: clk_cpll_div_50m 3'b101: clk_osc0_div_750k
7:4	RW	0x2	pclk_usb_div Divide pclk_usb by (div_con + 1)
3:2	RW	0x0	hclk_usb_sel hclk_usb clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
1:0	RW	0x0	aclk_usb_sel aclk_usb clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON33

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_mac1_out_sel clk_mac1_out clock mux. 2'b00: clk_cpll_div_125m 2'b01: clk_cpll_div_50m 2'b10: clk_cpll_div_25m 2'b11: xin_osc0_func_mux
13:12	RW	0x0	clk_gmac1_ptp_ref_sel clk_gmac1_ptp_ref clock mux. 2'b00: clk_cpll_div_62p5 2'b01: clk_gpll_div_100m 2'b10: clk_cpll_div_50m 2'b11: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_mac1_2top_sel clk_mac1_2top clock mux. 2'b00: clk_cpll_div_125m 2'b01: clk_cpll_div_50m 2'b10: clk_cpll_div_25m 2'b11: clk_ppll_mux
7:6	RO	0x0	reserved
5:4	RW	0x0	rgmii1_clk_sel clock speed in rgmii mode 2'b00: 125M 2'b01: 125M 2'b10: 2.5M 2'b11: 25M
3	RW	0x0	rmii1_clk_sel clock speed in rmii mode 1'b0: 2.5M 1'b1: 25M
2	RW	0x0	rmii1_extclk_sel rmii1_extclk_sel 1'b0: mac1 clock from SOC 1'b1: mac1 clock from IO
1:0	RW	0x0	rmii1_mode rmii1_mode 2'b00: rgmii mode 2'b01: rmii mode 2'b10: gmii mode

CRU_CLKSEL_CON34

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	dclk_vicap1_sel dclk_vicap1 clock mux. 2'b00: clk_cpll_div_333m 2'b01: clk_gpll_div_300m 2'b10: clk_gpll_div_200m
13:12	RO	0x0	reserved
11:8	RW	0x3	pclk_vi_div Divide pclk_vi by (div_con + 1)
7:4	RW	0x1	hclk_vi_div Divide hclk_vi by (div_con + 1)
3:2	RO	0x0	reserved
1:0	RW	0x0	aclk_vi_sel aclk_vi clock mux. 2'b00: clk_gpll_div_400m 2'b01: clk_gpll_div_300m 2'b10: clk_gpll_div_200m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON35

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	clk_cif_out_sel clk_cif_out clock mux. 2'b00: clk_gpll_mux 2'b01: usbphy480m_mux 2'b10: xin_osc0_func_mux
13:8	RW	0x00	clk_cif_out_div Divide clk_cif_out by (div_con + 1)
7:6	RW	0x0	clk_isp_sel clk_isp clock mux. 2'b00: clk_cpll_mux 2'b01: clk_gpll_mux 2'b10: clk_hpll_mux
5	RO	0x0	reserved
4:0	RW	0x01	clk_isp_div Divide clk_isp by (div_con + 1)

CRU_CLKSEL_CON36

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	clk_cam1_out_sel clk_cam1_out clock mux. 2'b00: clk_gpll_mux 2'b01: usbphy480m_mux 2'b10: xin_osc0_func_mux
13:8	RW	0x00	clk_cam1_out_div Divide clk_cam1_out by (div_con + 1)

Bit	Attr	Reset Value	Description
7:6	RW	0x3	clk_cam0_out_sel clk_cam0_out clock mux. 2'b00: clk_gpll_mux 2'b01: usbphy480m_mux 2'b10: xin_osc0_func_mux
5:0	RW	0x00	clk_cam0_out_div Divide clk_cam0_out by (div_con + 1)

CRU_CLKSEL_CON37

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x3	pclk_vo_div Divide pclk_vo by (div_con + 1)
11:8	RW	0x1	hclk_vo_div Divide hclk_vo by (div_con + 1)
7:2	RO	0x00	reserved
1:0	RW	0x0	aclk_vo_sel aclk_vo clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_cpll_div_250m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON38

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	clk_edp_200m_sel clk_edp_200m clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_cpll_div_125m
7:6	RW	0x0	aclk_vop_pre_sel aclk_vop_pre clock mux. 2'b00: clk_cpll_mux 2'b01: clk_gpll_mux 2'b10: clk_hpll_mux 2'b11: clk_vpll_mux
5	RO	0x0	reserved
4:0	RW	0x01	aclk_vop_pre_div Divide aclk_vop_pre by (div_con + 1)

CRU_CLKSEL_CON39

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	dclk0_vop_sel dclk0_vop clock mux. 2'b00: clk_hpll_mux 2'b01: clk_vpll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux
9:8	RO	0x0	reserved
7:0	RW	0x00	dclk0_vop_div Divide dclk0_vop by (div_con + 1)

CRU_CLKSEL_CON40

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	dclk1_vop_sel dclk1_vop clock mux. 2'b00: clk_hpll_mux 2'b01: clk_vpll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux
9:8	RO	0x0	reserved
7:0	RW	0x01	dclk1_vop_div Divide dclk1_vop by (div_con + 1)

CRU_CLKSEL_CON41

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	dclk2_vop_sel dclk2_vop clock mux. 2'b00: clk_hpll_mux 2'b01: clk_vpll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux
9:8	RO	0x0	reserved
7:0	RW	0x03	dclk2_vop_div Divide dclk2_vop by (div_con + 1)

CRU_CLKSEL_CON42

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	hclk_vpu_pre_div Divide hclk_vpu_pre by (div_con + 1)
7	RW	0x0	aclk_vpu_pre_sel aclk_vpu_pre clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x03	aclk_vpu_pre_div Divide aclk_vpu_pre by (div_con + 1)

CRU_CLKSEL_CON43

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x2	pclk_rga_pre_div Divide pclk_rga_pre by (div_con + 1)
11:8	RW	0x1	hclk_rga_pre_div Divide hclk_rga_pre by (div_con + 1)
7:6	RW	0x0	dclk_ebc_sel dclk_ebc clock mux. 2'b00: clk_gpll_div_400m 2'b01: clk_cpll_div_333m 2'b10: clk_gpll_div_200m
5:4	RW	0x0	clk_iep_core_sel clk_iep_core clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_cpll_div_100m
3:2	RW	0x0	clk_rga_core_sel clk_rga_core clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_gpll_div_200m 2'b10: clk_cpll_div_100m
1:0	RW	0x0	aclk_rga_pre_sel aclk_rga_pre clock mux. 2'b00: clk_gpll_div_300m 2'b01: clk_cpll_div_250m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON44

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:8	RW	0x2	hclk_rkvenc_pre_div Divide hclk_rkvenc_pre by (div_con + 1)
7:6	RW	0x0	aclk_rkvenc_pre_sel aclk_rkvenc_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
5	RO	0x0	reserved
4:0	RW	0x03	aclk_rkvenc_pre_div Divide aclk_rkvenc_pre by (div_con + 1)

CRU_CLKSEL_CON45

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_rkvenc_core_sel clk_rkvenc_core clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux 2'b11: clk_vpll_mux
13:5	RO	0x000	reserved
4:0	RW	0x03	clk_rkvenc_core_div Divide clk_rkvenc_core by (div_con + 1)

CRU_CLKSEL_CON47

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x1	hclk_rkvdec_pre_div Divide hclk_rkvdec_pre by (div_con + 1)
7	RW	0x0	aclk_rkvdec_pre_sel aclk_rkvdec_pre clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x02	aclk_rkvdec_pre_div Divide aclk_rkvdec_pre by (div_con + 1)

CRU_CLKSEL_CON48

Address: Operational Base + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	clk_rkvdec_ca_sel clk_rkvdec_ca clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux 2'b11: clk_vpll_mux
5	RO	0x0	reserved
4:0	RW	0x03	clk_rkvdec_ca_div Divide clk_rkvdec_ca by (div_con + 1)

CRU_CLKSEL_CON49

Address: Operational Base + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_rkvdec_core_sel clk_rkvdec_core clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux 2'b11: clk_vpll_mux
13	RO	0x0	reserved
12:8	RW	0x03	clk_rkvdec_core_div Divide clk_rkvdec_core by (div_con + 1)
7:6	RW	0x0	clk_rkvdec_hevc_ca_sel clk_rkvdec_hevc_ca clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux 2'b11: clk_vpll_mux
5	RO	0x0	reserved
4:0	RW	0x01	clk_rkvdec_hevc_ca_div Divide clk_rkvdec_hevc_ca by (div_con + 1)

CRU_CLKSEL_CON50

Address: Operational Base + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	pclk_bus_sel pclk_bus clock mux. 2'b00: clk_gpll_div_100m 2'b01: clk_gpll_div_75m 2'b10: clk_cpll_div_50m 2'b11: xin_osc0_func_mux
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	aclk_bus_sel aclk_bus clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_150m 2'b10: clk_gpll_div_100m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON51

Address: Operational Base + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:8	RW	0x13	clk_tsadc_div Divide clk_tsadc by (div_con + 1)
7:6	RO	0x0	reserved
5:4	RW	0x0	clk_tsadc_tsen_sel clk_tsadc_tsen clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_gpll_div_100m 2'b10: clk_cpll_div_100m
3	RO	0x0	reserved
2:0	RW	0x0	clk_tsadc_tsen_div Divide clk_tsadc_tsen by (div_con + 1)

CRU_CLKSEL_CON52

Address: Operational Base + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart1_sel sclk_uart1 clock mux. 2'b00: clk_uart1_src 2'b01: clk_uart1_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart1_src_sel clk_uart1_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart1_src_div Divide clk_uart1_src by (div_con + 1)

CRU_CLKSEL_CON53

Address: Operational Base + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart1_frac_div clk_uart1_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON54

Address: Operational Base + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart2_sel sclk_uart2 clock mux. 2'b00: clk_uart2_src 2'b01: clk_uart2_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart2_src_sel clk_uart2_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart2_src_div Divide clk_uart2_src by (div_con + 1)

CRU_CLKSEL_CON55

Address: Operational Base + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart2_frac_div clk_uart2_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON56

Address: Operational Base + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart3_sel sclk_uart3 clock mux. 2'b00: clk_uart3_src 2'b01: clk_uart3_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart3_src_sel clk_uart3_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart3_src_div Divide clk_uart3_src by (div_con + 1)

CRU_CLKSEL_CON57

Address: Operational Base + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart3_frac_div clk_uart3_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON58

Address: Operational Base + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart4_sel sclk_uart4 clock mux. 2'b00: clk_uart4_src 2'b01: clk_uart4_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart4_src_sel clk_uart4_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart4_src_div Divide clk_uart4_src by (div_con + 1)

CRU_CLKSEL_CON59

Address: Operational Base + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart4_frac_div clk_uart4_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON60

Address: Operational Base + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x2	sclk_uart5_sel sclk_uart5 clock mux. 2'b00: clk_uart5_src 2'b01: clk_uart5_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart5_src_sel clk_uart5_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart5_src_div Divide clk_uart5_src by (div_con + 1)

CRU_CLKSEL_CON61

Address: Operational Base + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart5_frac_div clk_uart5_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON62

Address: Operational Base + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart6_sel sclk_uart6 clock mux. 2'b00: clk_uart6_src 2'b01: clk_uart6_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart6_src_sel clk_uart6_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart6_src_div Divide clk_uart6_src by (div_con + 1)

CRU_CLKSEL_CON63

Address: Operational Base + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart6_frac_div clk_uart6_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON64

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart7_sel sclk_uart7 clock mux. 2'b00: clk_uart7_src 2'b01: clk_uart7_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart7_src_sel clk_uart7_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart7_src_div Divide clk_uart7_src by (div_con + 1)

CRU_CLKSEL_CON65

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart7_frac_div clk_uart7_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON66

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart8_sel sclk_uart8 clock mux. 2'b00: clk_uart8_src 2'b01: clk_uart8_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart8_src_sel clk_uart8_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart8_src_div Divide clk_uart8_src by (div_con + 1)

CRU_CLKSEL_CON67

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart8_frac_div clk_uart8_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON68

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x2	sclk_uart9_sel sclk_uart9 clock mux. 2'b00: clk_uart9_src 2'b01: clk_uart9_frac 2'b10: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_uart9_src_sel clk_uart9_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: usbphy480m_mux
7	RO	0x0	reserved
6:0	RW	0x0b	clk_uart9_src_div Divide clk_uart9_src by (div_con + 1)

CRU_CLKSEL_CON69

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_uart9_frac_div clk_uart9_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON70

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_can1_sel clk_can1 clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
14:13	RO	0x0	reserved
12:8	RW	0x03	clk_can1_div Divide clk_can1 by (div_con + 1)
7	RW	0x0	clk_can0_sel clk_can0 clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	clk_can0_div Divide clk_can0 by (div_con + 1)

CRU_CLKSEL_CON71

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x2	clk_i2c_sel clk_i2c clock mux. 2'b00: clk_gpll_div_200m 2'b01: clk_gpll_div_100m 2'b10: xin_osc0_func_mux 2'b11: clk_cpll_div_100m
7	RW	0x0	clk_can2_sel clk_can2 clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x03	clk_can2_div Divide clk_can2 by (div_con + 1)

CRU_CLKSEL_CON72

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dbclk_gpio_sel dbclk_gpio clock mux. 1'b0: xin_osc0_func_mux 1'b1: clk_rtc_32k
13:12	RW	0x1	clk_pwm3_sel clk_pwm3 clock mux. 2'b00: clk_gpll_div_100m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m
11:10	RW	0x1	clk_pwm2_sel clk_pwm2 clock mux. 2'b00: clk_gpll_div_100m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m
9:8	RW	0x1	clk_pwm1_sel clk_pwm1 clock mux. 2'b00: clk_gpll_div_100m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m

Bit	Attr	Reset Value	Description
7:6	RW	0x0	clk_spi3_sel clk_spi3 clock mux. 2'b00: clk_gpll_div_200m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m
5:4	RW	0x0	clk_spi2_sel clk_spi2 clock mux. 2'b00: clk_gpll_div_200m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m
3:2	RW	0x0	clk_spi1_sel clk_spi1 clock mux. 2'b00: clk_gpll_div_200m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m
1:0	RW	0x0	clk_spi0_sel clk_spi0 clock mux. 2'b00: clk_gpll_div_200m 2'b01: xin_osc0_func_mux 2'b10: clk_cpll_div_100m

CRU_CLKSEL_CON73

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_otpc_arb_sel clk_optc_arb clock mux. 1'b0: xin_osc0_func_mux 1'b1: clk_cpll_div_100m
14	RO	0x0	reserved
13:12	RW	0x0	pclk_top_sel pclk_top clock mux. 2'b00: clk_gpll_div_100m 2'b01: clk_gpll_div_75m 2'b10: clk_cpll_div_50m 2'b11: xin_osc0_func_mux
11:10	RO	0x0	reserved
9:8	RW	0x0	hclk_top_sel hclk_top clock mux. 2'b00: clk_gpll_div_150m 2'b01: clk_gpll_div_100m 2'b10: clk_gpll_div_75m 2'b11: xin_osc0_func_mux
7:6	RO	0x0	reserved
5:4	RW	0x0	aclk_top_low_sel aclk_top_low clock mux. 2'b00: clk_gpll_div_400m 2'b01: clk_gpll_div_300m 2'b10: clk_gpll_div_200m 2'b11: xin_osc0_func_mux
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	aclk_top_high_sel aclk_top_high clock mux. 2'b00: clk_cpll_div_500m 2'b01: clk_gpll_div_400m 2'b10: clk_gpll_div_300m 2'b11: xin_osc0_func_mux

CRU_CLKSEL_CON74

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	clk_testout_sel clk_testout clock mux. 5'd0 : xin_osc0_func_mux 5'd1 : clk_rtc_32k 5'd2 : clk_core_ndft 5'd3 : sclk_core_pre_ndft 5'd4 : clk_gpu_pre_ndft 5'd5 : clk_npu_pre_ndft 5'd6 : clk_ddrphy1x 5'd7 : aclk_vpu_pre_ndft 5'd8 : clk_isp_core_ndft 5'd9 : aclk_vop_pre_ndft 5'd10: dclk0_vop_ndft 5'd11: otp_ips_osc_out 5'd12: clk_rkvenc_core_ndft 5'd13: clk_rkvdec_hevc_ca_ndft 5'd14: clk_mac0_top 5'd15: clk_mac1_top 5'd16: clk_core_pvtpll_out 5'd17: clk_gpu_pvtpll_out 5'd18: clk_npu_pvtpll_out 5'd19: aclk_bus_ndft 5'd20: aclk_gic_audio_ndft 5'd21: aclk_php_ndft 5'd22: aclk_secure_flash_ndft 5'd23: mclk_pdm_ndft 5'd24: mclk_i2s0_8ch_rx_ndft 5'd25: sclk_uart1_ndft 5'd26: cclk_emmc_ndft 5'd27: clk_pipephy0_pipe_ndft 5'd28: clk_pipephy1_pipe_ndft 5'd29: clk_pipephy0_ref 5'd30: clk_usbphy0_ref 5'd31: usbphy480m_i
7:0	RW	0x1f	clk_testout_div Divide clk_testout by (div_con + 1)

CRU_CLKSEL_CON75

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	clk_gpll_div_300m_div Divide clk_gpll_div_300m by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x02	clk_gpll_div_400m_div Divide clk_gpll_div_400m by (div_con + 1)

CRU_CLKSEL_CON76

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x07	clk_gpll_div_150m_div Divide clk_gpll_div_150m by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x05	clk_gpll_div_200m_div Divide clk_gpll_div_200m by (div_con + 1)

CRU_CLKSEL_CON77

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x0f	clk_gpll_div_75m_div Divide clk_gpll_div_75m by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x0b	clk_gpll_div_100m_div Divide clk_gpll_div_100m by (div_con + 1)

CRU_CLKSEL_CON78

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x01	clk_cpll_div_500m_div Divide clk_cpll_div_500m by (div_con + 1)
7:6	RO	0x0	reserved
5:0	RW	0x3b	clk_gpll_div_20m_div Divide clk_gpll_div_20m by (div_con + 1)

CRU_CLKSEL_CON79

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	clk_cpll_div_250m_div Divide clk_cpll_div_250m by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x02	clk_cpll_div_333m_div Divide clk_cpll_div_333m by (div_con + 1)

CRU_CLKSEL_CON80

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x0f	clk_cpll_div_62p5_div Divide clk_cpll_div_62p5 by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x07	clk_cpll_div_125m_div Divide clk_cpll_div_125m by (div_con + 1)

CRU_CLKSEL_CON81

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x27	clk_cpll_div_25m_div Divide clk_cpll_div_25m by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x13	clk_cpll_div_50m_div Divide clk_cpll_div_50m by (div_con + 1)

CRU_CLKSEL_CON82

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x1f	clk_osc0_div_750k_div Divide clk_osc0_div_750k by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x09	clk_cpll_div_100m_div Divide clk_osc0_div_750k by (div_con + 1)

CRU_CLKSEL_CON83

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	i2s3_mclkout_rx_sel i2s3_mclkout_rx clock mux. 1'b0: mclk_i2s3_2ch_rx 1'b1: xin_osc0_half
14:12	RO	0x0	reserved
11:10	RW	0x0	mclk_i2s3_2ch_rx_sel mclk_i2s3_2ch_rx clock mux. 2'b00: clk_i2s3_2ch_rx_src 2'b01: clk_i2s3_2ch_rx_frac 2'b10: i2s3_mclkin 2'b11: xin_osc0_half
9:8	RW	0x1	clk_i2s3_2ch_rx_src_sel clk_i2s3_2ch_rx_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: clk_npll_mux
7	RO	0x0	reserved
6:0	RW	0x13	clk_i2s3_2ch_rx_src_div Divide clk_i2s3_rx_2ch_src by (div_con + 1)

CRU_CLKSEL_CON84

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_i2s3_2ch_rx_frac_div clk_i2s3_2ch_rx_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

CRU_GATE_CON00

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cntclk_core_en cntclk_core clock gating control. When high, disable clock
14	RW	0x0	tsclk_core_en tsclk_core clock gating control. When high, disable clock
13	RW	0x0	periphclk_core_en periphclk_core clock gating control. When high, disable clock
12	RW	0x0	pclk_core_en pclk_core clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
11	RW	0x0	periphclk_core_pre_en periphclk_core_pre clock gating control. When high, disable clock
10	RW	0x0	pclk_core_pre_en pclk_core_pre clock gating control. When high, disable clock
9	RW	0x0	gicclk_core_en gicclk_core clock gating control. When high, disable clock
8	RW	0x0	atclk_core_en atclk_core clock gating control. When high, disable clock
7	RW	0x0	sclk_core_en sclk_core clock gating control. When high, disable clock
6	RW	0x0	clk_npll_core_en clk_npll_core clock gating control. When high, disable clock
5	RW	0x0	sclk_core_src_en sclk_core_src clock gating control. When high, disable clock
4	RW	0x0	clk_core3_en clk_core3 clock gating control. When high, disable clock
3	RW	0x0	clk_core2_en clk_core2 clock gating control. When high, disable clock
2	RW	0x0	clk_core1_en clk_core1 clock gating control. When high, disable clock
1	RW	0x0	clk_core0_en clk_core0 clock gating control. When high, disable clock
0	RW	0x0	clk_core_en clk_core_ndft clock gating control. When high, disable clock

CRU_GATE_CON01

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_jtag_en clk_jtag clock gating control. When high, disable clock
14	RW	0x0	clk_apll_core_en clk_apll_core clock gating control. When high, disable clock
13	RW	0x0	clk_core_div2_en clk_core_div2 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_core_pvtpll_en clk_core_pvtpll clock gating control. When high, disable clock
11	RW	0x0	clk_core_pvtm_core_en clk_core_pvtm_core clock gating control. When high, disable clock
10	RW	0x0	clk_core_pvtm_en clk_core_pvtm clock gating control. When high, disable clock
9	RW	0x0	pclk_core_pvtm_en pclk_core_pvtm clock gating control. When high, disable clock
8	RW	0x0	pclk_core_grf_en pclk_core_grf clock gating control. When high, disable clock
7	RW	0x0	aclk_adb400_gic2core_en aclk_adb400_gic2core clock gating control. When high, disable clock
6	RW	0x0	aclk_adb400_core2gic_en aclk_adb400_core2gic clock gating control. When high, disable clock
5	RW	0x0	pclk_dbg_daplite_en pclk_dbg_daplite clock gating control. When high, disable clock
4	RW	0x0	pclk_dbg_en pclk_dbg clock gating control. When high, disable clock
3	RW	0x0	pclk_dbg_biu_en pclk_dbg_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_core_biu2bus_en aclk_core_biu2bus clock gating control. When high, disable clock
1	RW	0x0	aclk_core_biu2ddr_en aclk_core_biu2ddr clock gating control. When high, disable clock
0	RW	0x0	aclk_core_en aclk_core_ndft clock gating control. When high, disable clock

CRU_GATE_CON02

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	aclk_gpu_pre_en aclk_gpu_pre clock gating control. When high, disable clock
10	RW	0x0	clk_gpu_div2_en clk_gpu_div2 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_gpu_pvtpll_en clk_gpu_pvtpll clock gating control. When high, disable clock
8	RW	0x0	clk_gpu_pvtm_core_en clk_gpu_pvtm_core clock gating control. When high, disable clock
7	RW	0x0	clk_gpu_pvtm_en clk_gpu_pvtm clock gating control. When high, disable clock
6	RW	0x0	pclk_gpu_pvtm_en pclk_gpu_pvtm clock gating control. When high, disable clock
5	RW	0x0	pclk_gpu_biu_en pclk_gpu_biu clock gating control. When high, disable clock
4	RW	0x0	aclk_gpu_biu_en aclk_gpu_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_gpu_en clk_gpu clock gating control. When high, disable clock
2	RW	0x0	pclk_gpu_pre_en pclk_gpu_pre clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	clk_gpu_src_en clk_gpu_src clock gating control. When high, disable clock

CRU_GATE_CON03

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_npu_div2_en clk_npu_div2 clock gating control. When high, disable clock
12	RW	0x0	clk_npu_pvtpll_en clk_npu_pvtpll clock gating control. When high, disable clock
11	RW	0x0	clk_npu_pvtm_core_en clk_npu_pvtm_core clock gating control. When high, disable clock
10	RW	0x0	clk_npu_pvtm_en clk_npu_pvtm clock gating control. When high, disable clock
9	RW	0x0	pclk_npu_pvtm_en pclk_npu_pvtm clock gating control. When high, disable clock
8	RW	0x0	hclk_npu_en hclk_npu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	aclk_npu_en aclk_npu clock gating control. When high, disable clock
6	RW	0x0	pclk_npu_biu_en pclk_npu_biu clock gating control. When high, disable clock
5	RW	0x0	hclk_npu_biu_en hclk_npu_biu clock gating control. When high, disable clock
4	RW	0x0	aclk_npu_biu_en aclk_npu_biu clock gating control. When high, disable clock
3	RW	0x0	pclk_npu_pre_en pclk_npu_pre clock gating control. When high, disable clock
2	RW	0x0	hclk_npu_pre_en hclk_npu_pre clock gating control. When high, disable clock
1	RW	0x0	clk_npu_np5_en clk_npu_np5 clock gating control. When high, disable clock
0	RW	0x0	clk_npu_src_en clk_npu_src clock gating control. When high, disable clock

CRU_GATE_CON04

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk24_ddrmon_en clk24_ddrmon clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	clk_ddrmon_en clk_ddrmon clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	aclk_dma2ddr_en aclk_dma2ddr clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_ddrdfi_ctl_en clk_ddrdfi_ctl clock gating control. When high, disable clock
8	RW	0x0	aclk_ddrsplit_en aclk_ddrsplit clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	clk_ddr_alwayson_en clk_ddr_alwayson clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_msch_en aclk_msch clock gating control. When high, disable clock
4	RW	0x0	aclk_ddrscramble_en aclk_ddrscramble clock gating control. When high, disable clock
3	RW	0x0	clk_hwffc_ctrl_en clk_hwffc_ctrl clock gating control. When high, disable clock
2	RW	0x0	aclk_msch_div2_en clk_msch clock gating control. When high, disable clock
1	RW	0x0	clk_dpll_ddr_en clk_dpll_ddr clock gating control. When high, disable clock
0	RW	0x0	clk_ddrphy1x_en clk_ddrphy1x_src clock gating control. When high, disable clock

CRU_GATE_CON05

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_pdm_en mclk_pdm clock gating control. When high, disable clock
14	RW	0x0	hclk_pdm_en hclk_pdm clock gating control. When high, disable clock
13	RW	0x0	hclk_i2s3_2ch_en hclk_i2s3_2ch clock gating control. When high, disable clock
12	RW	0x0	hclk_i2s2_2ch_en hclk_i2s2_2ch clock gating control. When high, disable clock
11	RW	0x0	hclk_i2s1_8ch_en hclk_i2s1_8ch clock gating control. When high, disable clock
10	RW	0x0	hclk_i2s0_8ch_en hclk_i2s0_8ch clock gating control. When high, disable clock
9	RW	0x0	dclk_sdmmc_buffer_en dclk_sdmmc_buffer clock gating control. When high, disable clock
8	RW	0x0	hclk_sdmmc_buffer_en hclk_sdmmc_buffer clock gating control. When high, disable clock
7	RW	0x0	aclk_spinlock_en aclk_spinlock clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	aclk_gicadb_gic2core_en aclk_gicadb_gic2core clock gating control. When high, disable clock
5	RW	0x0	aclk_gicadb_core2gic_en aclk_gicadb_core2gic clock gating control. When high, disable clock
4	RW	0x0	aclk_gic600_en aclk_gic600 clock gating control. When high, disable clock
3	RW	0x0	hclk_gic_audio_biu_en hclk_gic_audio_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_gic_audio_biu_en aclk_gic_audio_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_gic_audio_en hclk_gic_audio clock gating control. When high, disable clock
0	RW	0x0	aclk_gic_audio_en aclk_gic_audio clock gating control. When high, disable clock

CRU_GATE_CON06

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	i2s1_mclkout_rx_en i2s1_mclkout_rx clock gating control. When high, disable clock
14	RW	0x0	mclk_i2s1_8ch_rx_en mclk_i2s1_8ch_rx clock gating control. When high, disable clock
13	RW	0x0	clk_i2s1_8ch_rx_frac_en clk_i2s1_8ch_rx_frac clock gating control. When high, disable clock
12	RW	0x0	clk_i2s1_8ch_rx_src_en clk_i2s1_8ch_rx_src clock gating control. When high, disable clock
11	RW	0x0	i2s1_mclkout_tx_en i2s1_mclkout_tx clock gating control. When high, disable clock
10	RW	0x0	mclk_i2s1_8ch_tx_en mclk_i2s1_8ch_tx clock gating control. When high, disable clock
9	RW	0x0	clk_i2s1_8ch_tx_frac_en clk_i2s1_8ch_tx_frac clock gating control. When high, disable clock
8	RW	0x0	clk_i2s1_8ch_tx_src_en clk_i2s1_8ch_tx_src clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	i2s0_mclkout_rx_en i2s0_mclkout_rx clock gating control. When high, disable clock
6	RW	0x0	mclk_i2s0_8ch_rx_en mclk_i2s0_8ch_rx clock gating control. When high, disable clock
5	RW	0x0	clk_i2s0_8ch_rx_frac_en clk_i2s0_8ch_rx_frac clock gating control. When high, disable clock
4	RW	0x0	clk_i2s0_8ch_rx_src_en clk_i2s0_8ch_rx_src clock gating control. When high, disable clock
3	RW	0x0	i2s0_mclkout_tx_en i2s0_mclkout_tx clock gating control. When high, disable clock
2	RW	0x0	mclk_i2s0_8ch_tx_en mclk_i2s0_8ch_tx clock gating control. When high, disable clock
1	RW	0x0	clk_i2s0_8ch_tx_frac_en clk_i2s0_8ch_tx_frac clock gating control. When high, disable clock
0	RW	0x0	clk_i2s0_8ch_tx_src_en clk_i2s0_8ch_tx_src clock gating control. When high, disable clock

CRU_GATE_CON07

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mclk_spdif_8ch_frac_en mclk_spdif_8ch_frac clock gating control. When high, disable clock
14	RW	0x0	mclk_spdif_8ch_src_en mclk_spdif_8ch_src clock gating control. When high, disable clock
13	RW	0x0	hclk_spdif_8ch_en hclk_spdif_8ch clock gating control. When high, disable clock
12	RW	0x0	hclk_vad_en hclk_vad clock gating control. When high, disable clock
11	RW	0x0	i2s3_mclkout_rx _en i2s3_mclkout_rx clock gating control. When high, disable clock
10	RW	0x0	mclk_i2s3_2ch_rx_en mclk_i2s3_2ch_rx clock gating control. When high, disable clock
9	RW	0x0	clk_i2s3_2ch_rx_frac_en clk_i2s3_2ch_rx_frac clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
8	RW	0x0	clk_i2s3_2ch_rx_src_en clk_i2s3_2ch_rx_src clock gating control. When high, disable clock
7	RW	0x0	i2s3_mclkout_tx _en i2s3_mclkout_tx clock gating control. When high, disable clock
6	RW	0x0	mclk_i2s3_2ch_tx_en mclk_i2s3_2ch_tx clock gating control. When high, disable clock
5	RW	0x0	clk_i2s3_2ch_tx_frac_en clk_i2s3_2ch_tx_frac clock gating control. When high, disable clock
4	RW	0x0	clk_i2s3_2ch_tx_src_en clk_i2s3_2ch_tx_src clock gating control. When high, disable clock
3	RW	0x0	i2s2_mclkout_en i2s2_mclkout clock gating control. When high, disable clock
2	RW	0x0	mclk_i2s2_2ch_en mclk_i2s2_2ch clock gating control. When high, disable clock
1	RW	0x0	clk_i2s2_2ch_frac_en clk_i2s2_2ch_frac clock gating control. When high, disable clock
0	RW	0x0	clk_i2s2_2ch_src_en clk_i2s2_2ch_src clock gating control. When high, disable clock

CRU_GATE_CON08

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_crypto_ns_rng_en clk_crypto_ns_rng clock gating control. When high, disable clock
14	RW	0x0	clk_crypto_ns_pka_en clk_crypto_ns_pka clock gating control. When high, disable clock
13	RW	0x0	clk_crypto_ns_core_en clk_crypto_ns_core clock gating control. When high, disable clock
12	RW	0x0	hclk_crypto_ns_en hclk_crypto_ns clock gating control. When high, disable clock
11	RW	0x0	aclk_crypto_ns_en aclk_crypto_ns clock gating control. When high, disable clock
10	RW	0x0	hclk_secure_flash_biu_en hclk_secure_flash_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	aclk_secure_flash_biu_en aclk_secure_flash_biu clock gating control. When high, disable clock
8	RW	0x0	hclk_secure_flash_en hclk_secure_flash clock gating control. When high, disable clock
7	RW	0x0	aclk_secure_flash_en aclk_secure_flash clock gating control. When high, disable clock
6	RW	0x0	clk_acdcdig_adc_en clk_acdcdig_adc clock gating control. When high, disable clock
5	RW	0x0	clk_acdcdig_dac_en clk_acdcdig_dac clock gating control. When high, disable clock
4	RW	0x0	clk_acdcdig_i2c_en clk_acdcdig_i2c clock gating control. When high, disable clock
3	RW	0x0	hclk_acdcdig_en hclk_acdcdig clock gating control. When high, disable clock
2	RW	0x0	sclk_audpwm_frac_en sclk_audpwm_frac clock gating control. When high, disable clock
1	RW	0x0	sclk_audpwm_src_en sclk_audpwm_src clock gating control. When high, disable clock
0	RW	0x0	hclk_audpwm_en hclk_audpwm clock gating control. When high, disable clock

CRU_GATE_CON09

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_trng_ns_en clk_trng_ns clock gating control. When high, disable clock
10	RW	0x0	hclk_trng_ns_en hclk_trng_ns clock gating control. When high, disable clock
9	RW	0x0	tclk_emmc_en tclk_emmc clock gating control. When high, disable clock
8	RW	0x0	cclk_emmc_en cclk_emmc clock gating control. When high, disable clock
7	RW	0x0	bclk_emmc_en bclk_emmc clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	hclk_emmc_en hclk_emmc clock gating control. When high, disable clock
5	RW	0x0	aclk_emmc_en aclk_emmc clock gating control. When high, disable clock
4	RW	0x0	sclk_sfc_en sclk_sfc clock gating control. When high, disable clock
3	RW	0x0	hclk_sfc_xip_en hclk_sfc_xip clock gating control. When high, disable clock
2	RW	0x0	hclk_sfc_en hclk_sfc clock gating control. When high, disable clock
1	RW	0x0	nclk_nandc_en nclk_nandc clock gating control. When high, disable clock
0	RW	0x0	hclk_nandc_en hclk_nandc clock gating control. When high, disable clock

CRU_GATE_CON10

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_usb3otg1_pipe_en clk_usb3otg1_pipe_dft clock gating control. When high, disable clock
14	RW	0x0	clk_usb3otg1_suspend_en clk_usb3otg1_suspend clock gating control. When high, disable clock
13	RW	0x0	clk_usb3otg1_ref_en clk_usb3otg1_ref clock gating control. When high, disable clock
12	RW	0x0	aclk_usb3otg1_en aclk_usb3otg1 clock gating control. When high, disable clock
11	RW	0x0	clk_usb3otg0_pipe_en clk_usb3otg0_pipe_dft clock gating control. When high, disable clock
10	RW	0x0	clk_usb3otg0_suspend_en clk_usb3otg0_suspend clock gating control. When high, disable clock
9	RW	0x0	clk_usb3otg0_ref_en clk_usb3otg0_ref clock gating control. When high, disable clock
8	RW	0x0	aclk_usb3otg0_en aclk_usb3otg0 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	pclk_pipe_grf_en pclk_pipe_grf clock gating control. When high, disable clock
6	RW	0x0	clk_xpcs_tx_div10_en clk_xpcs_tx_div10 clock gating control. When high, disable clock
5	RW	0x0	clk_xpcs_rx_div10_en clk_xpcs_rx_div10 clock gating control. When high, disable clock
4	RW	0x0	clk_xpcs_eee_en clk_xpcs_eee clock gating control. When high, disable clock
3	RW	0x0	pclk_pipe_biu_en pclk_pipe_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_pipe_biu_en aclk_pipe_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_pipe_en pclk_pipe clock gating control. When high, disable clock
0	RW	0x0	aclk_pipe_en aclk_pipe clock gating control. When high, disable clock

CRU_GATE_CON11

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_sata2_pipe_en clk_sata2_pipe_dft clock gating control. When high, disable clock
10	RW	0x0	clk_sata2_rxoob_en clk_sata2_rxoob clock gating control. When high, disable clock
9	RW	0x0	clk_sata2_pmalive_en clk_sata2_pmalive clock gating control. When high, disable clock
8	RW	0x0	aclk_sata2_en aclk_sata2 clock gating control. When high, disable clock
7	RW	0x0	clk_sata1_pipe_en clk_sata1_pipe_dft clock gating control. When high, disable clock
6	RW	0x0	clk_sata1_rxoob_en clk_sata1_rxoob clock gating control. When high, disable clock
5	RW	0x0	clk_sata1_pmalive_en clk_sata1_pmalive clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
4	RW	0x0	aclk_sata1_en aclk_sata1 clock gating control. When high, disable clock
3	RW	0x0	clk_sata0_pipe_en clk_sata0_pipe_dft clock gating control. When high, disable clock
2	RW	0x0	clk_sata0_rxoob_en clk_sata0_rxoob clock gating control. When high, disable clock
1	RW	0x0	clk_sata0_pmalive_en clk_sata0_pmalive clock gating control. When high, disable clock
0	RW	0x0	aclk_sata0_en aclk_sata0 clock gating control. When high, disable clock

CRU_GATE_CON12

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_pcie30x1_pipe_en clk_pcie30x1_pipe_dft clock gating control. When high, disable clock
12	RW	0x0	clk_pcie30x1_aux_en clk_pcie30x1_aux_ndft clock gating control. When high, disable clock
11	RW	0x0	pclk_pcie30x1_en pclk_pcie30x1 clock gating control. When high, disable clock
10	RW	0x0	aclk_pcie30x1_dbi_en aclk_pcie30x1_dbi clock gating control. When high, disable clock
9	RW	0x0	aclk_pcie30x1_slv_en aclk_pcie30x1_slv clock gating control. When high, disable clock
8	RW	0x0	aclk_pcie30x1_mst_en aclk_pcie30x1_mst clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	clk_pcie20_pipe_en clk_pcie20_pipe_dft clock gating control. When high, disable clock
4	RW	0x0	clk_pcie20_aux_en clk_pcie20_aux_ndft clock gating control. When high, disable clock
3	RW	0x0	pclk_pcie20_en pclk_pcie20 clock gating control. When high, disable clock
2	RW	0x0	aclk_pcie20_dbi_en aclk_pcie20_dbi clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_pcie20_slv_en aclk_pcie20_slv clock gating control. When high, disable clock
0	RW	0x0	aclk_pcie20_mst_en aclk_pcie20_mst clock gating control. When high, disable clock

CRU_GATE_CON13

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_xpcs_mii1_rx_en clk_xpcs_mii1_rx clock gating control. When high, disable clock
14	RW	0x0	clk_xpcs_mii1_tx_en clk_xpcs_mii1_tx clock gating control. When high, disable clock
13	RW	0x0	clk_xpcs_mii0_rx_en clk_xpcs_mii0_rx clock gating control. When high, disable clock
12	RW	0x0	clk_xpcs_mii0_tx_en clk_xpcs_mii0_tx clock gating control. When high, disable clock
11	RW	0x0	clk_xpcs_xgxs_rx_en clk_xpcs_xgxs_rx clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_xpcs_xgxs_tx_en clk_xpcs_xgxs_tx clock gating control. When high, disable clock
8	RW	0x0	clk_xpcs_qsgmii_rx_en clk_xpcs_qsgmii_rx clock gating control. When high, disable clock
7	RW	0x0	clk_xpcs_qsgmii_tx_en clk_xpcs_qsgmii_tx clock gating control. When high, disable clock
6	RW	0x0	pclk_xpcs_en pclk_xpcs clock gating control. When high, disable clock
5	RW	0x0	clk_pcie30x2_pipe_en clk_pcie30x2_pipe_dft clock gating control. When high, disable clock
4	RW	0x0	clk_pcie30x2_aux_en clk_pcie30x2_aux_ndft clock gating control. When high, disable clock
3	RW	0x0	pclk_pcie30x2_en pclk_pcie30x2 clock gating control. When high, disable clock
2	RW	0x0	aclk_pcie30x2_dbi_en aclk_pcie30x2_dbi clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_pcie30x2_slv_en aclk_pcie30x2_slv clock gating control. When high, disable clock
0	RW	0x0	aclk_pcie30x2_mst_en aclk_pcie30x2_mst clock gating control. When high, disable clock

CRU_GATE_CON14

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pclk_php_biu_en pclk_php_biu clock gating control. When high, disable clock
12	RW	0x0	hclk_php_biu_en hclk_php_biu clock gating control. When high, disable clock
11	RW	0x0	aclk_php_biu_en aclk_php_biu clock gating control. When high, disable clock
10	RW	0x0	pclk_php_en pclk_php clock gating control. When high, disable clock
9	RW	0x0	hclk_php_en hclk_php clock gating control. When high, disable clock
8	RW	0x0	aclk_php_en aclk_php clock gating control. When high, disable clock
7:4	RO	0x0	reserved
3	RW	0x0	hclk_perimid_biu_en hclk_perimid_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_perimid_biu_en aclk_perimid_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_perimid_en hclk_perimid clock gating control. When high, disable clock
0	RW	0x0	aclk_perimid_en aclk_perimid clock gating control. When high, disable clock

CRU_GATE_CON15

Address: Operational Base + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_mac0_refout_en clk_mac0_refout clock gating control. When high, disable clock
11:9	RO	0x0	reserved
8	RW	0x0	clk_mac0_out_en clk_mac0_out clock gating control. When high, disable clock
7	RW	0x0	clk_mac0_2top_en clk_mac0_2top clock gating control. When high, disable clock
6	RW	0x0	pclk_gmac0_en pclk_gmac0 clock gating control. When high, disable clock
5	RW	0x0	aclk_gmac0_en aclk_gmac0 clock gating control. When high, disable clock
4	RW	0x0	clk_gmac0_ptp_ref_en clk_gmac0_ptp_ref clock gating control. When high, disable clock
3	RW	0x0	clk_sdmmc1_en clk_sdmmc1 clock gating control. When high, disable clock
2	RW	0x0	hclk_sdmmc1_en hclk_sdmmc1 clock gating control. When high, disable clock
1	RW	0x0	clk_sdmmc0_en clk_sdmmc0 clock gating control. When high, disable clock
0	RW	0x0	hclk_sdmmc0_en hclk_sdmmc0 clock gating control. When high, disable clock

CRU_GATE_CON16

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_usb2host1_arb_en hclk_usb2host1_arb clock gating control. When high, disable clock
14	RW	0x0	hclk_usb2host1_en hclk_usb2host1 clock gating control. When high, disable clock
13	RW	0x0	hclk_usb2host0_arb_en hclk_usb2host0_arb clock gating control. When high, disable clock
12	RW	0x0	hclk_usb2host0_en hclk_usb2host0 clock gating control. When high, disable clock
11:7	RO	0x00	reserved
6	RW	0x0	pclk_usb_grf_en pclk_usb_grf_en clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
5	RW	0x0	pclk_usb_biu_en pclk_usb_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_usb_biu_en hclk_usn_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_usb_biu_en aclk_usb_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_usb_en pclk_usb clock gating control. When high, disable clock
1	RW	0x0	hclk_usb_en hclk_usb clock gating control. When high, disable clock
0	RW	0x0	aclk_usb_en aclk_usb clock gating control. When high, disable clock

CRU_GATE_CON17

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	clk_mac1_refout_en clk_mac1_refout clock gating control. When high, disable clock
9:7	RO	0x0	reserved
6	RW	0x0	clk_mac1_out_en clk_mac1_out clock gating control. When high, disable clock
5	RW	0x0	clk_mac1_2top_en clk_mac1_2top clock gating control. When high, disable clock
4	RW	0x0	pclk_gmac1_en pclk_gmac1 clock gating control. When high, disable clock
3	RW	0x0	aclk_gmac1_en aclk_gmac1 clock gating control. When high, disable clock
2	RW	0x0	clk_gmac1_ptp_ref_en clk_gmac1_ptp_ref clock gating control. When high, disable clock
1	RW	0x0	clk_sdmmc2_en clk_sdmmc2 clock gating control. When high, disable clock
0	RW	0x0	hclk_sdmmc2_en hclk_sdmmc2 clock gating control. When high, disable clock

CRU_GATE_CON18

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	dclk_vicap1_en dclk_vicap1 clock gating control. When high, disable clock
10	RW	0x0	hclk_vicap1_en hclk_vicap1 clock gating control. When high, disable clock
9	RW	0x0	aclk_vicap1_en aclk_vicap1 clock gating control. When high, disable clock
8:6	RO	0x0	reserved
5	RW	0x0	pclk_vi_biu_en pclk_vi_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vi_biu_en hclk_vi_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vi_biu_en aclk_vi_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vi_en pclk_vi clock gating control. When high, disable clock
1	RW	0x0	hclk_vi_en hclk_vi clock gating control. When high, disable clock
0	RW	0x0	aclk_vi_en aclk_vi clock gating control. When high, disable clock

CRU_GATE_CON19

Address: Operational Base + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	clk_cam1_out_en clk_cam1_out clock gating control. When high, disable clock
9	RW	0x0	clk_cam0_out_en clk_cam0_out clock gating control. When high, disable clock
8	RW	0x0	clk_cif_out_en clk_cif_out clock gating control. When high, disable clock
7:5	RO	0x0	reserved
4	RW	0x0	pclk_csi2host1_en pclk_csi2host1 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2	RW	0x0	clk_isp_en clk_isp clock gating control. When high, disable clock
1	RW	0x0	hclk_isp_en hclk_isp clock gating control. When high, disable clock
0	RW	0x0	aclk_isp_en aclk_isp clock gating control. When high, disable clock

CRU_GATE_CON20

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_vop_pwm_en clk_vop_pwm clock gating control. When high, disable clock
12	RW	0x0	dclk2_vop_en dclk2_vop clock gating control. When high, disable clock
11	RW	0x0	dclk1_vop_en dclk1_vop clock gating control. When high, disable clock
10	RW	0x0	dclk0_vop_en dclk0_vop clock gating control. When high, disable clock
9	RW	0x0	hclk_vop_en hclk_vop clock gating control. When high, disable clock
8	RW	0x0	aclk_vop_en aclk_vop clock gating control. When high, disable clock
7	RW	0x0	aclk_vop_biu_en aclk_vop_biu clock gating control. When high, disable clock
6	RW	0x0	aclk_vop_pre_en aclk_vop_pre clock gating control. When high, disable clock
5	RW	0x0	pclk_vo_biu_en pclk_vo_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vo_biu_en hclk_vo_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vo_biu_en aclk_vo_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vo_en pclk_vo clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
1	RW	0x0	hclk_vo_en hclk_vo clock gating control. When high, disable clock
0	RO	0x0	reserved

CRU_GATE_CON21

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_edp_200m_en clk_edp_200m clock gating control. When high, disable clock
8	RW	0x0	pclk_edp_ctrl_en pclk_edp_ctrl clock gating control. When high, disable clock
7	RW	0x0	pclk_dsitx_1_en pclk_dsitx_1 clock gating control. When high, disable clock
6	RW	0x0	pclk_dsitx_0_en pclk_dsitx_0 clock gating control. When high, disable clock
5	RW	0x0	clk_hdmi_cec_en clk_hdmi_cec clock gating control. When high, disable clock
4	RW	0x0	clk_hdmi_sfr_en clk_hdmi_sfr clock gating control. When high, disable clock
3	RW	0x0	pclk_hdmi_host_en pclk_hdmi_host clock gating control. When high, disable clock
2	RW	0x0	pclk_hdcp_en pclk_hdcp clock gating control. When high, disable clock
1	RW	0x0	hclk_hdcp_en hclk_hdcp clock gating control. When high, disable clock
0	RW	0x0	aclk_hdcp_en aclk_hdcp clock gating control. When high, disable clock

CRU_GATE_CON22

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_eink_en hclk_eink clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
14	RW	0x0	pclk_eink_en pclk_eink clock gating control. When high, disable clock
13	RW	0x0	pclk_rga_biu_en pclk_rga_biu clock gating control. When high, disable clock
12	RW	0x0	pclk_rga_pre_en pclk_rga_pre clock gating control. When high, disable clock
11:6	RO	0x00	reserved
5	RW	0x0	hclk_vpu_en hclk_vpu clock gating control. When high, disable clock
4	RW	0x0	aclk_vpu_en aclk_vpu clock gating control. When high, disable clock
3	RW	0x0	hclk_vpu_biu_en hclk_vpu_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_vpu_biu_en aclk_vpu_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_vpu_pre_en hclk_vpu_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_vpu_pre_en aclk_vpu_pre clock gating control. When high, disable clock

CRU_GATE_CON23

Address: Operational Base + offset (0x035C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_jenc_en hclk_jenc clock gating control. When high, disable clock
14	RW	0x0	aclk_jenc_en aclk_jenc clock gating control. When high, disable clock
13	RW	0x0	hclk_jdec_en hclk_jdec clock gating control. When high, disable clock
12	RW	0x0	aclk_jdec_en aclk_jdec clock gating control. When high, disable clock
11	RW	0x0	dclk_ebc_en dclk_ebc clock gating control. When high, disable clock
10	RW	0x0	hclk_ebc_en hclk_ebc clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_iep_core_en clk_iep_core clock gating control. When high, disable clock
8	RW	0x0	hclk_iep_en hclk_iep clock gating control. When high, disable clock
7	RW	0x0	aclk_iep_en aclk_iep clock gating control. When high, disable clock
6	RW	0x0	clk_rga_core_en clk_rga_core clock gating control. When high, disable clock
5	RW	0x0	hclk_rga_en hclk_rga clock gating control. When high, disable clock
4	RW	0x0	aclk_rga_en aclk_rga clock gating control. When high, disable clock
3	RW	0x0	hclk_rga_biu_en hclk_rga_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_rga_biu_en aclk_rga_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_rga_pre_en hclk_rga_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_rga_pre_en aclk_rga_pre clock gating control. When high, disable clock

CRU_GATE_CON24

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	clk_rkvenc_core_en clk_rkvenc_core clock gating control. When high, disable clock
7	RW	0x0	hclk_rkvenc_en hclk_rkvenc clock gating control. When high, disable clock
6	RW	0x0	aclk_rkvenc_en aclk_rkvenc clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_rkvenc_biu_en hclk_rkvenc_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_rkvenc_biu_en aclk_rkvenc_biu clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
2	RO	0x0	reserved
1	RW	0x0	hclk_rkvenc_pre_en hclk_rkvenc_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_rkvenc_pre_en aclk_rkvenc_pre clock gating control. When high, disable clock

CRU_GATE_CON25

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	clk_rkvdec_hevc_ca_en clk_rkvdec_hevc_ca clock gating control. When high, disable clock
7	RW	0x0	clk_rkvdec_core_en clk_rkvdec_core clock gating control. When high, disable clock
6	RW	0x0	clk_rkvdec_ca_en clk_rkvdec_ca clock gating control. When high, disable clock
5	RW	0x0	hclk_rkvdec_en hclk_rkvdec clock gating control. When high, disable clock
4	RW	0x0	aclk_rkvdec_en aclk_rkvdec clock gating control. When high, disable clock
3	RW	0x0	hclk_rkvdec_biu_en hclk_rkvdec_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_rkvdec_biu_en aclk_rkvdec_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_rkvdec_pre_en hclk_rkvdec_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_rkvdec_pre_en aclk_rkvdec_pre clock gating control. When high, disable clock

CRU_GATE_CON26

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	tclk_wdt_ns_en tclk_wdt_ns clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
13	RW	0x0	pclk_wdt_ns_en pclk_wdt_ns clock gating control. When high, disable clock
12	RW	0x0	pclk_scr_en pclk_scr clock gating control. When high, disable clock
11	RW	0x0	clk_otpc_ns_usr_en clk_otpc_ns_usr clock gating control. When high, disable clock
10	RW	0x0	clk_otpc_ns_sbpi_en clk_otpc_ns_sbpi clock gating control. When high, disable clock
9	RW	0x0	pclk_otpc_ns_en pclk_otpc_ns clock gating control. When high, disable clock
8	RW	0x0	clk_saradc_en clk_saradc clock gating control. When high, disable clock
7	RW	0x0	pclk_saradc_en pclk_saradc clock gating control. When high, disable clock
6	RW	0x0	clk_tsadc_en clk_tsadc clock gating control. When high, disable clock
5	RW	0x0	clk_tsadc_tsen_en clk_tsadc_tsen clock gating control. When high, disable clock
4	RW	0x0	pclk_tsadc_en pclk_tsadc clock gating control. When high, disable clock
3	RW	0x0	pclk_bus_biu_en pclk_bus_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_bus_biu_en aclk_bus_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_bus_en pclk_bus clock gating control. When high, disable clock
0	RW	0x0	aclk_bus_en aclk_bus clock gating control. When high, disable clock

CRU_GATE_CON27

Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_uart1_en sclk_uart1 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
14	RW	0x0	clk_uart1_frac_en clk_uart1_frac clock gating control. When high, disable clock
13	RW	0x0	clk_uart1_en clk_uart1_src clock gating control. When high, disable clock
12	RW	0x0	pclk_uart1_en pclk_uart1 clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	clk_can2_en clk_can2 clock gating control. When high, disable clock
9	RW	0x0	pclk_can2_en pclk_can2 clock gating control. When high, disable clock
8	RW	0x0	clk_can1_en clk_can1 clock gating control. When high, disable clock
7	RW	0x0	pclk_can1_en pclk_can1 clock gating control. When high, disable clock
6	RW	0x0	clk_can0_en clk_can0 clock gating control. When high, disable clock
5	RW	0x0	pclk_can0_en pclk_can0 clock gating control. When high, disable clock
4	RW	0x0	pclk_dft2apb_en pclk_dft2apb clock gating control. When high, disable clock
3	RW	0x0	pclk_grf_vccio567_en pclk_grf_vccio567 clock gating control. When high, disable clock
2	RW	0x0	pclk_grf_vccio34_en pclk_grf_vccio34 clock gating control. When high, disable clock
1	RW	0x0	pclk_grf_vccio12_en pclk_grf_vccio12 clock gating control. When high, disable clock
0	RW	0x0	pclk_grf_en pclk_grf clock gating control. When high, disable clock

CRU_GATE_CON28

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclk_uart5_en sclk_uart5 clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
14	RW	0x0	clk_uart5_frac_en clk_uart5_frac clock gating control. When high, disable clock
13	RW	0x0	clk_uart5_en clk_uart5_src clock gating control. When high, disable clock
12	RW	0x0	pclk_uart5_en pclk_uart5 clock gating control. When high, disable clock
11	RW	0x0	sclk_uart4_en sclk_uart4 clock gating control. When high, disable clock
10	RW	0x0	clk_uart4_frac_en clk_uart4_frac clock gating control. When high, disable clock
9	RW	0x0	clk_uart4_en clk_uart4_src clock gating control. When high, disable clock
8	RW	0x0	pclk_uart4_en pclk_uart4 clock gating control. When high, disable clock
7	RW	0x0	sclk_uart3_en sclk_uart3 clock gating control. When high, disable clock
6	RW	0x0	clk_uart3_frac_en clk_uart3_frac clock gating control. When high, disable clock
5	RW	0x0	clk_uart3_en clk_uart3_src clock gating control. When high, disable clock
4	RW	0x0	pclk_uart3_en pclk_uart3 clock gating control. When high, disable clock
3	RW	0x0	sclk_uart2_en sclk_uart2 clock gating control. When high, disable clock
2	RW	0x0	clk_uart2_frac_en clk_uart2_frac clock gating control. When high, disable clock
1	RW	0x0	clk_uart2_en clk_uart2_src clock gating control. When high, disable clock
0	RW	0x0	pclk_uart2_en pclk_uart2 clock gating control. When high, disable clock

CRU_GATE_CON29

Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	sclk_uart9_en sclk_uart9 clock gating control. When high, disable clock
14	RW	0x0	clk_uart9_frac_en clk_uart9_frac clock gating control. When high, disable clock
13	RW	0x0	clk_uart9_en clk_uart9_src clock gating control. When high, disable clock
12	RW	0x0	pclk_uart9_en pclk_uart9 clock gating control. When high, disable clock
11	RW	0x0	sclk_uart8_en sclk_uart8 clock gating control. When high, disable clock
10	RW	0x0	clk_uart8_frac_en clk_uart8_frac clock gating control. When high, disable clock
9	RW	0x0	clk_uart8_en clk_uart8_src clock gating control. When high, disable clock
8	RW	0x0	pclk_uart8_en pclk_uart8 clock gating control. When high, disable clock
7	RW	0x0	sclk_uart7_en sclk_uart7 clock gating control. When high, disable clock
6	RW	0x0	clk_uart7_frac_en clk_uart7_frac clock gating control. When high, disable clock
5	RW	0x0	clk_uart7_en clk_uart7_src clock gating control. When high, disable clock
4	RW	0x0	pclk_uart7_en pclk_uart7 clock gating control. When high, disable clock
3	RW	0x0	sclk_uart6_en sclk_uart6 clock gating control. When high, disable clock
2	RW	0x0	clk_uart6_frac_en clk_uart6_frac clock gating control. When high, disable clock
1	RW	0x0	clk_uart6_en clk_uart6_src clock gating control. When high, disable clock
0	RW	0x0	pclk_uart6_en pclk_uart6 clock gating control. When high, disable clock

CRU_GATE_CON30

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_spi2_en clk_spi2 clock gating control. When high, disable clock
14	RW	0x0	pclk_spi2_en pclk_spi2 clock gating control. When high, disable clock
13	RW	0x0	clk_spi1_en clk_spi1 clock gating control. When high, disable clock
12	RW	0x0	pclk_spi1_en pclk_spi1 clock gating control. When high, disable clock
11	RW	0x0	clk_spi0_en clk_spi0 clock gating control. When high, disable clock
10	RW	0x0	pclk_spi0_en pclk_spi0 clock gating control. When high, disable clock
9	RW	0x0	clk_i2c5_en clk_i2c5 clock gating control. When high, disable clock
8	RW	0x0	pclk_i2c5_en pclk_i2c5 clock gating control. When high, disable clock
7	RW	0x0	clk_i2c4_en clk_i2c4 clock gating control. When high, disable clock
6	RW	0x0	pclk_i2c4_en pclk_i2c4 clock gating control. When high, disable clock
5	RW	0x0	clk_i2c3_en clk_i2c3 clock gating control. When high, disable clock
4	RW	0x0	pclk_i2c3_en pclk_i2c3 clock gating control. When high, disable clock
3	RW	0x0	clk_i2c2_en clk_i2c2 clock gating control. When high, disable clock
2	RW	0x0	pclk_i2c2_en pclk_i2c2 clock gating control. When high, disable clock
1	RW	0x0	clk_i2c1_en clk_i2c1 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c1_en pclk_i2c1 clock gating control. When high, disable clock

CRU_GATE_CON31

Address: Operational Base + offset (0x037C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_pwm2_capture_en clk_pwm2_capture clock gating control. When high, disable clock
14	RW	0x0	clk_pwm2_en clk_pwm2 clock gating control. When high, disable clock
13	RW	0x0	pclk_pwm2_en pclk_pwm2 clock gating control. When high, disable clock
12	RW	0x0	clk_pwm1_capture_en clk_pwm1_capture clock gating control. When high, disable clock
11	RW	0x0	clk_pwm1_en clk_pwm1 clock gating control. When high, disable clock
10	RW	0x0	pclk_pwm1_en pclk_pwm1 clock gating control. When high, disable clock
9	RW	0x0	dbclk_gpio4_en dbclk_gpio4 clock gating control. When high, disable clock
8	RW	0x0	pclk_gpio4_en pclk_gpio4 clock gating control. When high, disable clock
7	RW	0x0	dbclk_gpio3_en dbclk_gpio3 clock gating control. When high, disable clock
6	RW	0x0	pclk_gpio3_en pclk_gpio3 clock gating control. When high, disable clock
5	RW	0x0	dbclk_gpio2_en dbclk_gpio2 clock gating control. When high, disable clock
4	RW	0x0	pclk_gpio2_en pclk_gpio2 clock gating control. When high, disable clock
3	RW	0x0	dbclk_gpio1_en dbclk_gpio1 clock gating control. When high, disable clock
2	RW	0x0	pclk_gpio1_en pclk_gpio1 clock gating control. When high, disable clock
1	RW	0x0	clk_spi3_en clk_spi3 clock gating control. When high, disable clock
0	RW	0x0	pclk_spi3_en pclk_spi3 clock gating control. When high, disable clock

CRU_GATE_CON32

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_mailbox_en pclk_mailbox clock gating control. When high, disable clock
14	RW	0x0	pclk_intmux_en pclk_intmux clock gating control. When high, disable clock
13	RW	0x0	aclk_mcu_en aclk_mcu clock gating control. When high, disable clock
12	RW	0x0	clk_timer_en clk_timer clock gating control. When high, disable clock
11	RW	0x0	dbclk_gpio_en dbclk_gpio clock gating control. When high, disable clock
10	RW	0x0	clk_i2c_en clk_i2c clock gating control. When high, disable clock
9	RW	0x0	clk_timer5_en clk_timer5 clock gating control. When high, disable clock
8	RW	0x0	clk_timer4_en clk_timer4 clock gating control. When high, disable clock
7	RW	0x0	clk_timer3_en clk_timer3 clock gating control. When high, disable clock
6	RW	0x0	clk_timer2_en clk_timer2 clock gating control. When high, disable clock
5	RW	0x0	clk_timer1_en clk_timer1 clock gating control. When high, disable clock
4	RW	0x0	clk_timer0_en clk_timer0 clock gating control. When high, disable clock
3	RW	0x0	pclk_timer_en pclk_timer clock gating control. When high, disable clock
2	RW	0x0	clk_pwm3_capture_en clk_pwm3_capture clock gating control. When high, disable clock
1	RW	0x0	clk_pwm3_en clk_pwm3 clock gating control. When high, disable clock
0	RW	0x0	pclk_pwm3_en pclk_pwm3 clock gating control. When high, disable clock

CRU_GATE_CON33

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_mipidsiphy1_en pclk_mipidsiphy1 clock gating control. When high, disable clock
14	RW	0x0	pclk_mipidsiphy0_en pclk_mipidsiphy0 clock gating control. When high, disable clock
13	RW	0x0	pclk_mipicsiphy_en pclk_mipicsiphy clock gating control. When high, disable clock
12	RW	0x0	pclk_top_cru_en pclk_top_cru clock gating control. When high, disable clock
11:10	RO	0x0	reserved
9	RW	0x0	clk_otpc_arb_en clk_otpc_arb clock gating control. When high, disable clock
8	RW	0x0	pclk_pcie30phy_en pclk_pcie30phy clock gating control. When high, disable clock
7	RW	0x0	pclk_top_biu_en pclk_top_biu clock gating control. When high, disable clock
6	RW	0x0	hclk_top_biu_en hclk_top_biu clock gating control. When high, disable clock
5	RW	0x0	aclk_top_low_biu_en aclk_top_low_biu clock gating control. When high, disable clock
4	RW	0x0	aclk_top_high_biu_en aclk_top_high_biu clock gating control. When high, disable clock
3	RW	0x0	pclk_top_en pclk_top clock gating control. When high, disable clock
2	RW	0x0	hclk_top_en hclk_top clock gating control. When high, disable clock
1	RW	0x0	aclk_top_low_en aclk_top_low clock gating control. When high, disable clock
0	RW	0x0	aclk_top_high_en aclk_top_high clock gating control. When high, disable clock

CRU_GATE_CON34

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	clk_testout_en clk_testout clock gating control. When high, disable clock
14	RW	0x0	pclk_edpphy_grf_en pclk_edpphy_grf clock gating control. When high, disable clock
13	RW	0x0	pclk_otpphy_en pclk_otpphy clock gating control. When high, disable clock
12	RW	0x0	clk_cpu_boost_en clk_cpu_boost clock gating control. When high, disable clock
11	RW	0x0	pclk_cpu_boost_en pclk_cpu_boost clock gating control. When high, disable clock
10	RW	0x0	clk_ddrphy_en clk_ddrphy clock gating control. When high, disable clock
9	RW	0x0	pclk_ddrphy_en pclk_ddrphy clock gating control. When high, disable clock
8	RW	0x0	pclk_usb2phy1_grf_en pclk_usb2phy1_grf clock gating control. When high, disable clock
7	RW	0x0	pclk_usb2phy0_grf_en pclk_usb2phy0_grf clock gating control. When high, disable clock
6	RW	0x0	pclk_pipephy2_en pclk_pipephy2 clock gating control. When high, disable clock
5	RW	0x0	pclk_pipephy1_en pclk_pipephy1 clock gating control. When high, disable clock
4	RW	0x0	pclk_pipephy0_en pclk_pipephy0 clock gating control. When high, disable clock
3	RW	0x0	pclk_asb2apb_chip_bottom_en pclk_asb2apb_chip_bottom clock gating control. When high, disable clock
2	RW	0x0	pclk_asb2apb_chip_left_en pclk_asb2apb_chip_left clock gating control. When high, disable clock
1	RW	0x0	pclk_apb2asb_chip_bottom_en pclk_apb2asb_chip_bottom clock gating control. When high, disable clock
0	RW	0x0	pclk_apb2asb_chip_left_en pclk_apb2asb_chip_left clock gating control. When high, disable clock

CRU_GATE_CON35

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_osc0_div_750k_en clk_osc0_div_750k clock gating control. When high, disable clock
14	RW	0x0	clk_cpll_div_25m_en clk_cpll_div_25m clock gating control. When high, disable clock
13	RW	0x0	clk_cpll_div_50m_en clk_cpll_div_50m clock gating control. When high, disable clock
12	RW	0x0	clk_cpll_div_62p5_en clk_cpll_div_62p5 clock gating control. When high, disable clock
11	RW	0x0	clk_cpll_div_100m_en clk_cpll_div_100m clock gating control. When high, disable clock
10	RW	0x0	clk_cpll_div_125m_en clk_cpll_div_125m clock gating control. When high, disable clock
9	RW	0x0	clk_cpll_div_250m_en clk_cpll_div_250m clock gating control. When high, disable clock
8	RW	0x0	clk_cpll_div_333m_en clk_cpll_div_333m clock gating control. When high, disable clock
7	RW	0x0	clk_cpll_div_500m_en clk_cpll_div_500m clock gating control. When high, disable clock
6	RW	0x0	clk_gpll_div_20m_en clk_gpll_div_20m clock gating control. When high, disable clock
5	RW	0x0	clk_gpll_div_75m_en clk_gpll_div_75m clock gating control. When high, disable clock
4	RW	0x0	clk_gpll_div_100m_en clk_gpll_div_100m clock gating control. When high, disable clock
3	RW	0x0	clk_gpll_div_150m_en clk_gpll_div_150m clock gating control. When high, disable clock
2	RW	0x0	clk_gpll_div_200m_en clk_gpll_div_200m clock gating control. When high, disable clock
1	RW	0x0	clk_gpll_div_300m_en clk_gpll_div_300m clock gating control. When high, disable clock
0	RW	0x0	clk_gpll_div_400m_en clk_gpll_div_400m clock gating control. When high, disable clock

CRU_SOFTRST_CON00

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	nperiphreset When high, reset relative logic
12	RW	0x0	npreset When high, reset relative logic
11	RW	0x0	ngicreset When high, reset relative logic
10	RW	0x0	natreset When high, reset relative logic
9	RW	0x0	nsporeset When high, reset relative logic
8	RW	0x0	nsreset When high, reset relative logic
7	RW	0x0	ncpuporeset3 When high, reset relative logic
6	RW	0x0	ncpuporeset2 When high, reset relative logic
5	RW	0x0	ncpuporeset1 When high, reset relative logic
4	RW	0x0	ncpuporeset0 When high, reset relative logic
3	RW	0x0	ncorereset3 When high, reset relative logic
2	RW	0x0	ncorereset2 When high, reset relative logic
1	RW	0x0	ncorereset1 When high, reset relative logic
0	RW	0x0	ncorereset0 When high, reset relative logic

CRU_SOFTRST_CON01

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	resetn_core_pvtpll When high, reset relative logic
10	RW	0x0	resetn_core_pvtm When high, reset relative logic
9	RW	0x0	presetn_core_pvtm When high, reset relative logic
8	RW	0x0	presetn_core_grf When high, reset relative logic
7	RW	0x0	aresetn_adb400_gic2core When high, reset relative logic
6	RW	0x0	aresetn_adb400_core2gic When high, reset relative logic

Bit	Attr	Reset Value	Description
5	RW	0x0	resetn_dap When high, reset relative logic
4	RW	0x0	presetn_dbg_daplite When high, reset relative logic
3	RW	0x0	presetn_dbg When high, reset relative logic
2	RW	0x0	presetn_dbg_biu When high, reset relative logic
1	RW	0x0	aresetn_core_biu2bus When high, reset relative logic
0	RW	0x0	aresetn_core_biu2ddr When high, reset relative logic

CRU_SOFTRST_CON02

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_npu_pvtpll When high, reset relative logic
14	RW	0x0	resetn_npu_pvtm When high, reset relative logic
13	RW	0x0	presetn_npu_pvtm When high, reset relative logic
12	RW	0x0	hresetn_npu When high, reset relative logic
11	RW	0x0	aresetn_npu When high, reset relative logic
10	RW	0x0	presetn_npu_biu When high, reset relative logic
9	RW	0x0	hresetn_npu_biu When high, reset relative logic
8	RW	0x0	aresetn_npu_biu When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	resetn_gpu_pvtpll When high, reset relative logic
4	RW	0x0	resetn_gpu_pvtm When high, reset relative logic
3	RW	0x0	presetn_gpu_pvtm When high, reset relative logic
2	RW	0x0	presetn_gpu_biu When high, reset relative logic
1	RW	0x0	aresetn_gpu_biu When high, reset relative logic
0	RW	0x0	resetn_gpu When high, reset relative logic

CRU_SOFTRST_CON03

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	aresetn_dma2ddr When high, reset relative logic
8	RO	0x0	reserved
7	RW	0x0	resetn_ddrdfi_ctl When high, reset relative logic
6	RW	0x0	aresetn_ddrsplit When high, reset relative logic
5	RW	0x0	resetn_ddr_alwayson When high, reset relative logic
4	RW	0x0	resetn_hwffc_ctrl When high, reset relative logic
3	RW	0x0	aresetn_msch When high, reset relative logic
2:0	RO	0x0	reserved

CRU_SOFTRST_CON04

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hresetn_i2s3_2ch When high, reset relative logic
13	RW	0x0	hresetn_i2s2_2ch When high, reset relative logic
12	RW	0x0	hresetn_i2s1_8ch When high, reset relative logic
11	RW	0x0	hresetn_i2s0_8ch When high, reset relative logic
10	RW	0x0	dresetn_sdmmc_buffer When high, reset relative logic
9	RW	0x0	hresetn_sdmmc_buffer When high, reset relative logic
8	RW	0x0	aresetn_spinlock When high, reset relative logic
7	RW	0x0	aresetn_gicadb_gic2core When high, reset relative logic
6	RW	0x0	aresetn_gicadb_core2gic When high, reset relative logic
5	RW	0x0	aresetn_gic600_debug When high, reset relative logic
4	RW	0x0	aresetn_gic600 When high, reset relative logic
3	RW	0x0	hresetn_gic_audio_biu When high, reset relative logic
2	RW	0x0	aresetn_gic_audio_biu When high, reset relative logic

Bit	Attr	Reset Value	Description
1	RW	0x0	hresetn_perimid_biu When high, reset relative logic
0	RW	0x0	aresetn_perimid_biu When high, reset relative logic

CRU_SOFTRST_CON05

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_acdcdig When high, reset relative logic
14	RW	0x0	hresetn_acdcdig When high, reset relative logic
13	RW	0x0	sresetn_audpwm When high, reset relative logic
12	RW	0x0	hresetn_audpwm When high, reset relative logic
11	RW	0x0	mresetn_spdif_8ch When high, reset relative logic
10	RW	0x0	hresetn_spdif_8ch When high, reset relative logic
9	RW	0x0	hresetn_vad When high, reset relative logic
8	RW	0x0	mresetn_pdm When high, reset relative logic
7	RW	0x0	hresetn_pdm When high, reset relative logic
6	RW	0x0	mresetn_i2s3_2ch_rx When high, reset relative logic
5	RW	0x0	mresetn_i2s3_2ch_tx When high, reset relative logic
4	RW	0x0	mresetn_i2s2_2ch When high, reset relative logic
3	RW	0x0	mresetn_i2s1_8ch_rx When high, reset relative logic
2	RW	0x0	mresetn_i2s1_8ch_tx When high, reset relative logic
1	RW	0x0	mresetn_i2s0_8ch_rx When high, reset relative logic
0	RW	0x0	mresetn_i2s0_8ch_tx When high, reset relative logic

CRU_SOFTRST_CON06

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	resetn_trng_ns When high, reset relative logic
12	RW	0x0	hresetn_trng_ns When high, reset relative logic
11	RW	0x0	resetn_crypto_ns_rng When high, reset relative logic
10	RW	0x0	resetn_crypto_ns_pka When high, reset relative logic
9	RW	0x0	resetn_crypto_ns_core When high, reset relative logic
8	RW	0x0	hresetn_crypto_ns When high, reset relative logic
7	RW	0x0	aresetn_crypto_ns When high, reset relative logic
6:2	RO	0x00	reserved
1	RW	0x0	hresetn_secure_flash_biu When high, reset relative logic
0	RW	0x0	aresetn_secure_flash_biu When high, reset relative logic

CRU_SOFTRST_CON07

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	tresetn_emmc When high, reset relative logic
8	RW	0x0	cresetn_emmc When high, reset relative logic
7	RW	0x0	bresetn_emmc When high, reset relative logic
6	RW	0x0	hresetn_emmc When high, reset relative logic
5	RW	0x0	aresetn_emmc When high, reset relative logic
4	RW	0x0	sresetn_sfc When high, reset relative logic
3	RW	0x0	hresetn_sfc_xip When high, reset relative logic
2	RW	0x0	hresetn_sfc When high, reset relative logic
1	RW	0x0	nresetn_nandc When high, reset relative logic
0	RW	0x0	hresetn_nandc When high, reset relative logic

CRU_SOFTRST_CON08

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_sata1_rxoob When high, reset relative logic
12	RW	0x0	resetn_sata1_pmalive When high, reset relative logic
11	RW	0x0	resetn_sata1_pipe When high, reset relative logic
10	RW	0x0	aresetn_sata1 When high, reset relative logic
9	RW	0x0	resetn_sata0_rxoob When high, reset relative logic
8	RW	0x0	resetn_sata0_pmalive When high, reset relative logic
7	RW	0x0	resetn_sata0_pipe When high, reset relative logic
6	RW	0x0	aresetn_sata0 When high, reset relative logic
5	RW	0x0	presetn_pipe_grf When high, reset relative logic
4:3	RO	0x0	reserved
2	RW	0x0	presetn_pipe_biu When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	aresetn_pipe_biu When high, reset relative logic

CRU_SOFTRST_CON09

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_xpcs_xgxs_rx When high, reset relative logic
8	RW	0x0	resetn_xpcs_rx_div10 When high, reset relative logic
7	RW	0x0	resetn_xpcs_tx_div10 When high, reset relative logic
6	RW	0x0	resetn_xpcs When high, reset relative logic
5	RW	0x0	resetn_usb3otg1 When high, reset relative logic
4	RW	0x0	resetn_usb3otg0 When high, reset relative logic
3	RW	0x0	resetn_sata2_rxoob When high, reset relative logic
2	RW	0x0	resetn_sata2_pmalive When high, reset relative logic

Bit	Attr	Reset Value	Description
1	RW	0x0	resetn_sata2_pipe When high, reset relative logic
0	RW	0x0	aresetn_sata2 When high, reset relative logic

CRU_SOFTRST_CON10

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	pwr_rst_pcie20_req When high, reset relative logic
9	RW	0x0	sticky_rst_pcie20_req When high, reset relative logic
8	RW	0x0	nsticky_rst_pcie20_req When high, reset relative logic
7	RW	0x0	core_rst_pcie20_req When high, reset relative logic
6	RW	0x0	perst_pcie20_req When high, reset relative logic
5	RW	0x0	breset_pcie20_req When high, reset relative logic
4	RW	0x0	dbi_areset_pcie20_req When high, reset relative logic
3	RW	0x0	slv_areset_pcie20_req When high, reset relative logic
2	RW	0x0	mstr_areset_pcie20_req When high, reset relative logic
1	RW	0x0	resetn_pcie20_powerup_req When high, reset relative logic
0	RW	0x0	presetn_pcie20 When high, reset relative logic

CRU_SOFTRST_CON11

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	pwr_rst_pcie30x1_req When high, reset relative logic
9	RW	0x0	sticky_rst_pcie30x1_req When high, reset relative logic
8	RW	0x0	nsticky_rst_pcie30x1_req When high, reset relative logic
7	RW	0x0	core_rst_pcie30x1_req When high, reset relative logic
6	RW	0x0	perst_pcie30x1_req When high, reset relative logic

Bit	Attr	Reset Value	Description
5	RW	0x0	breset_pcie30x1_req When high, reset relative logic
4	RW	0x0	dbi_areset_pcie30x1_req When high, reset relative logic
3	RW	0x0	slv_areset_pcie30x1_req When high, reset relative logic
2	RW	0x0	mstr_areset_pcie30x1_req When high, reset relative logic
1	RW	0x0	resetn_pcie30x1_powerup_req When high, reset relative logic
0	RW	0x0	presetn_pcie30x1 When high, reset relative logic

CRU_SOFTRST_CON12

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	pwr_rst_pcie30x2_req When high, reset relative logic
9	RW	0x0	sticky_rst_pcie30x2_req When high, reset relative logic
8	RW	0x0	nsticky_rst_pcie30x2_req When high, reset relative logic
7	RW	0x0	core_rst_pcie30x2_req When high, reset relative logic
6	RW	0x0	perst_pcie30x2_req When high, reset relative logic
5	RW	0x0	breset_pcie30x2_req When high, reset relative logic
4	RW	0x0	dbi_areset_pcie30x2_req When high, reset relative logic
3	RW	0x0	slv_areset_pcie30x2_req When high, reset relative logic
2	RW	0x0	mstr_areset_pcie30x2_req When high, reset relative logic
1	RW	0x0	resetn_pcie30x2_powerup_req When high, reset relative logic
0	RW	0x0	presetn_pcie30x2 When high, reset relative logic

CRU_SOFTRST_CON13

Address: Operational Base + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	resetn_gmac0_timestamp When high, reset relative logic

Bit	Attr	Reset Value	Description
7	RW	0x0	aresetn_gmac0 When high, reset relative logic
6	RW	0x0	resetn_sdmmc1 When high, reset relative logic
5	RW	0x0	hresetn_sdmmc1 When high, reset relative logic
4	RW	0x0	resetn_sdmmc0 When high, reset relative logic
3	RW	0x0	hresetn_sdmmc0 When high, reset relative logic
2	RW	0x0	presetn_php_biu When high, reset relative logic
1	RW	0x0	hresetn_php_biu When high, reset relative logic
0	RW	0x0	aresetn_php_biu When high, reset relative logic

CRU_SOFTRST_CON14

Address: Operational Base + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_gmac1_timestamp When high, reset relative logic
12	RW	0x0	aresetn_gmac1 When high, reset relative logic
11	RW	0x0	resetn_sdmmc2 When high, reset relative logic
10	RW	0x0	hresetn_sdmmc2 When high, reset relative logic
9	RW	0x0	resetn_usb2host1_utmi When high, reset relative logic
8	RW	0x0	hresetn_usb2host1_arb When high, reset relative logic
7	RW	0x0	hresetn_usb2host1 When high, reset relative logic
6	RW	0x0	resetn_usb2host0_utmi When high, reset relative logic
5	RW	0x0	hresetn_usb2host0_arb When high, reset relative logic
4	RW	0x0	hresetn_usb2host0 When high, reset relative logic
3	RW	0x0	presetn_usb_grf When high, reset relative logic
2	RW	0x0	presetn_usb_biu When high, reset relative logic
1	RW	0x0	hresetn_usb_biu When high, reset relative logic
0	RW	0x0	aresetn_usb_biu When high, reset relative logic

CRU_SOFTRST_CON15

Address: Operational Base + offset (0x043C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_csi2host1 When high, reset relative logic
14	RO	0x0	reserved
13	RW	0x0	resetn_isp When high, reset relative logic
12	RW	0x0	hresetn_isp When high, reset relative logic
11	RW	0x0	presetn_vicap1 When high, reset relative logic
10	RW	0x0	iresetn_vicap1 When high, reset relative logic
9	RW	0x0	dresetn_vicap1 When high, reset relative logic
8	RW	0x0	hresetn_vicap1 When high, reset relative logic
7	RW	0x0	aresetn_vicap1 When high, reset relative logic
6:3	RO	0x0	reserved
2	RW	0x0	presetn_vi_biu When high, reset relative logic
1	RW	0x0	hresetn_vi_biu When high, reset relative logic
0	RW	0x0	aresetn_vi_biu When high, reset relative logic

CRU_SOFTRST_CON16

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_hdmi_host When high, reset relative logic
14	RW	0x0	presetn_hdmi_host When high, reset relative logic
13	RO	0x0	reserved
12	RW	0x0	presetn_hdcp When high, reset relative logic
11	RW	0x0	hresetn_hdcp When high, reset relative logic
10	RW	0x0	aresetn_hdcp When high, reset relative logic
9	RW	0x0	resetn_vop_pwm When high, reset relative logic
8	RW	0x0	dresetn2_vop When high, reset relative logic

Bit	Attr	Reset Value	Description
7	RW	0x0	dresetn1_vop When high, reset relative logic
6	RW	0x0	dresetn0_vop When high, reset relative logic
5	RW	0x0	hresetn_vop When high, reset relative logic
4	RW	0x0	aresetn_vop When high, reset relative logic
3	RW	0x0	aresetn_vop_biu When high, reset relative logic
2	RW	0x0	presetn_vo_biu When high, reset relative logic
1	RW	0x0	hresetn_vo_biu When high, reset relative logic
0	RW	0x0	aresetn_vo_biu When high, reset relative logic

CRU_SOFTRST_CON17

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_eink When high, reset relative logic
14	RW	0x0	hresetn_eink When high, reset relative logic
13:12	RO	0x0	reserved
11	RW	0x0	hresetn_vpu When high, reset relative logic
10	RW	0x0	aresetn_vpu When high, reset relative logic
9	RW	0x0	hresetn_vpu_biu When high, reset relative logic
8	RW	0x0	aresetn_vpu_biu When high, reset relative logic
7:4	RO	0x0	reserved
3	RW	0x0	resetn_edp_24m When high, reset relative logic
2	RW	0x0	presetn_edp_ctrl When high, reset relative logic
1	RW	0x0	presetn_dsitx_1 When high, reset relative logic
0	RW	0x0	presetn_dsitx_0 When high, reset relative logic

CRU_SOFTRST_CON18

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	hresetn_jenc When high, reset relative logic
14	RW	0x0	aresetn_jenc When high, reset relative logic
13	RW	0x0	hresetn_jdec When high, reset relative logic
12	RW	0x0	aresetn_jdec When high, reset relative logic
11	RW	0x0	dresetn_ebc When high, reset relative logic
10	RW	0x0	hresetn_ebc When high, reset relative logic
9	RW	0x0	resetn_iep_core When high, reset relative logic
8	RW	0x0	hresetn_iep When high, reset relative logic
7	RW	0x0	aresetn_iep When high, reset relative logic
6	RW	0x0	resetn_rga_core When high, reset relative logic
5	RW	0x0	hresetn_rga When high, reset relative logic
4	RW	0x0	aresetn_rga When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	presetn_rga_biu When high, reset relative logic
1	RW	0x0	hresetn_rga_biu When high, reset relative logic
0	RW	0x0	aresetn_rga_biu When high, reset relative logic

CRU_SOFTRST_CON19

Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	resetn_rkvenc_core When high, reset relative logic
4	RW	0x0	hresetn_rkvenc When high, reset relative logic
3	RW	0x0	aresetn_rkvenc When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	hresetn_venc_biu When high, reset relative logic
0	RW	0x0	aresetn_venc_biu When high, reset relative logic

CRU_SOFTRST_CON20

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_rkvdec_hevc_ca When high, reset relative logic
5	RW	0x0	resetn_rkvdec_core When high, reset relative logic
4	RW	0x0	resetn_rkvdec_ca When high, reset relative logic
3	RW	0x0	hresetn_rkvdec When high, reset relative logic
2	RW	0x0	aresetn_rkvdec When high, reset relative logic
1	RW	0x0	hresetn_rkvdec_biu When high, reset relative logic
0	RW	0x0	aresetn_rkvdec_biu When high, reset relative logic

CRU_SOFTRST_CON21

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dbresetn_gpio3 When high, reset relative logic
14	RW	0x0	presetn_gpio3 When high, reset relative logic
13	RW	0x0	dbresetn_gpio2 When high, reset relative logic
12	RW	0x0	presetn_gpio2 When high, reset relative logic
11	RW	0x0	dbresetn_gpio1 When high, reset relative logic
10	RW	0x0	presetn_gpio1 When high, reset relative logic
9	RW	0x0	resetn_can2 When high, reset relative logic
8	RW	0x0	presetn_can2 When high, reset relative logic
7	RW	0x0	resetn_can1 When high, reset relative logic
6	RW	0x0	presetn_can1 When high, reset relative logic
5	RW	0x0	resetn_can0 When high, reset relative logic
4	RW	0x0	presetn_can0 When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	presetn_bus_biu When high, reset relative logic

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	aresetn_bus_biu When high, reset relative logic

CRU_SOFTRST_CON22

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	resetn_otpc_ns_usr When high, reset relative logic
13	RW	0x0	resetn_otpc_ns_sbpi When high, reset relative logic
12	RW	0x0	presetn_otpc_ns When high, reset relative logic
11	RW	0x0	resetn_i2c5 When high, reset relative logic
10	RW	0x0	presetn_i2c5 When high, reset relative logic
9	RW	0x0	resetn_i2c4 When high, reset relative logic
8	RW	0x0	presetn_i2c4 When high, reset relative logic
7	RW	0x0	resetn_i2c3 When high, reset relative logic
6	RW	0x0	presetn_i2c3 When high, reset relative logic
5	RW	0x0	resetn_i2c2 When high, reset relative logic
4	RW	0x0	presetn_i2c2 When high, reset relative logic
3	RW	0x0	resetn_i2c1 When high, reset relative logic
2	RW	0x0	presetn_i2c1 When high, reset relative logic
1	RW	0x0	dbresetn_gpio4 When high, reset relative logic
0	RW	0x0	presetn_gpio4 When high, reset relative logic

CRU_SOFTRST_CON23

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_spi3 When high, reset relative logic

Bit	Attr	Reset Value	Description
12	RW	0x0	presetn_spi3 When high, reset relative logic
11	RW	0x0	resetn_spi2 When high, reset relative logic
10	RW	0x0	presetn_spi2 When high, reset relative logic
9	RW	0x0	resetn_spi1 When high, reset relative logic
8	RW	0x0	presetn_spi1 When high, reset relative logic
7	RW	0x0	resetn_spi0 When high, reset relative logic
6	RW	0x0	presetn_spi0 When high, reset relative logic
5	RW	0x0	resetn_pwm3 When high, reset relative logic
4	RW	0x0	presetn_pwm3 When high, reset relative logic
3	RW	0x0	resetn_pwm2 When high, reset relative logic
2	RW	0x0	presetn_pwm2 When high, reset relative logic
1	RW	0x0	resetn_pwm1 When high, reset relative logic
0	RW	0x0	presetn_pwm1 When high, reset relative logic

CRU_SOFTRST_CON24

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	sresetn_uart1 When high, reset relative logic
10	RW	0x0	presetn_uart1 When high, reset relative logic
9	RW	0x0	resetn_timer5 When high, reset relative logic
8	RW	0x0	resetn_timer4 When high, reset relative logic
7	RW	0x0	resetn_timer3 When high, reset relative logic
6	RW	0x0	resetn_timer2 When high, reset relative logic
5	RW	0x0	resetn_timer1 When high, reset relative logic
4	RW	0x0	resetn_timer0 When high, reset relative logic
3	RW	0x0	presetn_timer When high, reset relative logic

Bit	Attr	Reset Value	Description
2	RW	0x0	resetn_tsadc When high, reset relative logic
1	RW	0x0	presetn_tsadc When high, reset relative logic
0	RW	0x0	presetn_saradc When high, reset relative logic

CRU_SOFTRST_CON25

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sresetn_uart9 When high, reset relative logic
14	RW	0x0	presetn_uart9 When high, reset relative logic
13	RW	0x0	sresetn_uart8 When high, reset relative logic
12	RW	0x0	presetn_uart8 When high, reset relative logic
11	RW	0x0	sresetn_uart7 When high, reset relative logic
10	RW	0x0	presetn_uart7 When high, reset relative logic
9	RW	0x0	sresetn_uart6 When high, reset relative logic
8	RW	0x0	presetn_uart6 When high, reset relative logic
7	RW	0x0	sresetn_uart5 When high, reset relative logic
6	RW	0x0	presetn_uart5 When high, reset relative logic
5	RW	0x0	sresetn_uart4 When high, reset relative logic
4	RW	0x0	presetn_uart4 When high, reset relative logic
3	RW	0x0	sresetn_uart3 When high, reset relative logic
2	RW	0x0	presetn_uart3 When high, reset relative logic
1	RW	0x0	sresetn_uart2 When high, reset relative logic
0	RW	0x0	presetn_uart2 When high, reset relative logic

CRU_SOFTRST_CON26

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	presetn_mailbox When high, reset relative logic
11	RW	0x0	presetn_intmux When high, reset relative logic
10	RW	0x1	aresetn_mcu When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	presetn_dft2apb When high, reset relative logic
6	RW	0x0	tresetn_wdt_ns When high, reset relative logic
5	RW	0x0	presetn_wdt_ns When high, reset relative logic
4	RW	0x0	presetn_scr When high, reset relative logic
3	RW	0x0	presetn_grf_vccio567 When high, reset relative logic
2	RW	0x0	presetn_grf_vccio34 When high, reset relative logic
1	RW	0x0	presetn_grf_vccio12 When high, reset relative logic
0	RW	0x0	presetn_grf When high, reset relative logic

CRU_SOFTRST_CON27

Address: Operational Base + offset (0x046C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_pcie30phy_grf When high, reset relative logic
14	RW	0x0	resetn_pcie30phy When high, reset relative logic
13	RW	0x0	presetn_pcie30phy When high, reset relative logic
12	RW	0x0	presetn_mipidsiphy1 When high, reset relative logic
11	RW	0x0	presetn_mipidsiphy0 When high, reset relative logic
10	RW	0x0	presetn_mipicsiphy When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	resetn_ddrphy When high, reset relative logic
7	RW	0x0	presetn_ddrphy When high, reset relative logic
6	RW	0x0	presetn_top_cru When high, reset relative logic
5:4	RO	0x0	reserved
3	RW	0x0	presetn_top_biu When high, reset relative logic

Bit	Attr	Reset Value	Description
2	RW	0x0	hresetn_top_biu When high, reset relative logic
1	RW	0x0	aresetn_top_low_biu When high, reset relative logic
0	RW	0x0	aresetn_top_high_biu When high, reset relative logic

CRU_SOFTRST_CON28

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_otpphy When high, reset relative logic
14	RW	0x0	presetn_otpphy When high, reset relative logic
13	RW	0x0	resetn_cpu_boost When high, reset relative logic
12	RW	0x0	presetn_cpu_boost When high, reset relative logic
11	RW	0x0	presetn_usb2phy1_grf When high, reset relative logic
10	RW	0x0	presetn_usb2phy0_grf When high, reset relative logic
9	RW	0x0	resetn_pipephy2 When high, reset relative logic
8	RW	0x0	presetn_pipephy2 When high, reset relative logic
7	RW	0x0	resetn_pipephy1 When high, reset relative logic
6	RW	0x0	presetn_pipephy1 When high, reset relative logic
5	RW	0x0	resetn_pipephy0 When high, reset relative logic
4	RW	0x0	presetn_pipephy0 When high, reset relative logic
3	RW	0x0	presetn_asb2apb_chip_bottom When high, reset relative logic
2	RW	0x0	presetn_asb2apb_chip_left When high, reset relative logic
1	RW	0x0	presetn_apb2asb_chip_bottom When high, reset relative logic
0	RW	0x0	presetn_apb2asb_chip_left When high, reset relative logic

CRU_SOFTRST_CON29

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	presetn_pipephy2_grf When high, reset relative logic
12	RW	0x0	presetn_pipephy1_grf When high, reset relative logic
11	RW	0x0	presetn_pipephy0_grf When high, reset relative logic
10	RW	0x0	resetn_otpc_arb When high, reset relative logic
9	RW	0x0	resetn_gmac1_delayline When high, reset relative logic
8	RW	0x0	resetn_gmac0_delayline When high, reset relative logic
7	RW	0x0	resetn_tsadcphy When high, reset relative logic
6	RW	0x0	presetn_edpphy_grf When high, reset relative logic
5	RW	0x0	resetn_usb2phy1_usb2host1 When high, reset relative logic
4	RW	0x0	resetn_usb2phy1_usb2host0 When high, reset relative logic
3	RW	0x0	resetn_usb2phy1_por When high, reset relative logic
2	RW	0x0	resetn_usb2phy0_usb3otg1 When high, reset relative logic
1	RW	0x0	resetn_usb2phy0_usb3otg0 When high, reset relative logic
0	RW	0x0	resetn_usb2phy0_por When high, reset relative logic

CRU_SSGTBL0_3

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl0_3 Extern wave table 0-3 7-0: table0 15-8: table1 23-16: table2 31-24: table3

CRU_SSGTBL4_7

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl4_7 Extern wave table 4-7 7-0: table4 15-8: table5 23-16: table6 31-24: table7

CRU_SSGTBL8_11

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl8_11 Extern wave table 8-11 7-0: table8 15-8: table9 23-16: table10 31-24: table11

CRU_SSGTBL12_15

Address: Operational Base + offset (0x048C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl12_15 Extern wave table 12-15 7-0: table12 15-8: table13 23-16: table14 31-24: table15

CRU_SSGTBL16_19

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl16_19 Extern wave table 16-19 7-0: table16 15-8: table17 23-16: table18 31-24: table19

CRU_SSGTBL20_23

Address: Operational Base + offset (0x0494)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl20_23 Extern wave table 20-23 7-0: table20 15-8: table21 23-16: table22 31-24: table23

CRU_SSGTBL24_27

Address: Operational Base + offset (0x0498)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl24_27 Extern wave table 24-27 7-0: table24 15-8: table25 23-16: table26 31-24: table27

CRU_SSGTBL28_31

Address: Operational Base + offset (0x049C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl28_31 Extern wave table 28-31 7-0: table28 15-8: table29 23-16: table30 31-24: table31

CRU_SSGTBL32_35

Address: Operational Base + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl32_35 Extern wave table 32-35 7-0: table32 15-8: table33 23-16: table34 31-24: table35

CRU_SSGTBL36_39

Address: Operational Base + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl36_39 Extern wave table 36-39 7-0: table36 15-8: table37 23-16: table38 31-24: table39

CRU_SSGTBL40_43

Address: Operational Base + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl40_43 Extern wave table 40-43 7-0: table40 15-8: table41 23-16: table42 31-24: table43

CRU_SSGTBL44_47

Address: Operational Base + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl44_47 Extern wave table 44-47 7-0: table44 15-8: table45 23-16: table46 31-24: table47

CRU_SSGTBL48_51

Address: Operational Base + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl48_51 Extern wave table 48-51 7-0: table48 15-8: table49 23-16: table50 31-24: table51

CRU_SSGTBL52_55

Address: Operational Base + offset (0x04B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl52_55 Extern wave table 52-55 7-0: table52 15-8: table53 23-16: table54 31-24: table55

CRU_SSGTBL56_59

Address: Operational Base + offset (0x04B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl56_59 Extern wave table 56-59 7-0: table56 15-8: table57 23-16: table58 31-24: table59

CRU_SSGTBL60_63

Address: Operational Base + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl60_63 Extern wave table 60-63 7-0: table60 15-8: table61 23-16: table62 31-24: table63

CRU_SSGTBL64_67

Address: Operational Base + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl64_67 Extern wave table 64-67 7-0: table64 15-8: table65 23-16: table66 31-24: table67

CRU_SSGTBL68_71

Address: Operational Base + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl68_71 Extern wave table 68-71 7-0: table68 15-8: table69 23-16: table70 31-24: table71

CRU_SSGTBL72_75

Address: Operational Base + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl72_75 Extern wave table 72-75 7-0: table72 15-8: table73 23-16: table74 31-24: table75

CRU_SSGTBL76_79

Address: Operational Base + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl76_79 Extern wave table 76-79 7-0: table76 15-8: table77 23-16: table78 31-24: table79

CRU_SSGTBL80_83

Address: Operational Base + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl80_83 Extern wave table 76-79 7-0: table80 15-8: table81 23-16: table82 31-24: table83

CRU_SSGTBL84_87

Address: Operational Base + offset (0x04D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl84_87 Extern wave table 84-87 7-0: table84 15-8: table85 23-16: table86 31-24: table87

CRU_SSGTBL88_91

Address: Operational Base + offset (0x04D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl88_91 Extern wave table 88-91 7-0: table88 15-8: table89 23-16: table90 31-24: table91

CRU_SSGTBL92_95

Address: Operational Base + offset (0x04DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl92_95 Extern wave table 92-95 7-0: table92 15-8: table93 23-16: table94 31-24: table95

CRU_SSGTBL96_99

Address: Operational Base + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl96_99 Extern wave table 96-99 7-0: table96 15-8: table97 23-16: table98 31-24: table99

CRU_SSGTBL100_103

Address: Operational Base + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl100_103 Extern wave table 100-103 7-0: table100 15-8: table101 23-16: table102 31-24: table103

CRU_SSGTBL104_107

Address: Operational Base + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl104_107 Extern wave table 104-107 7-0: table104 15-8: table105 23-16: table106 31-24: table107

CRU_SSGTBL108_111

Address: Operational Base + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl108_111 Extern wave table 108-111 7-0: table108 15-8: table109 23-16: table110 31-24: table111

CRU_SSGTBL112_115

Address: Operational Base + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl112_115 Extern wave table 112-115 7-0: table112 15-8: table113 23-16: table114 31-24: table115

CRU_SSGTBL116_119

Address: Operational Base + offset (0x04F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl116_119 Extern wave table 116-119 7-0: table116 15-8: table117 23-16: table118 31-24: table119

CRU_SSGTBL120_123

Address: Operational Base + offset (0x04F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl120_123 Extern wave table 120-123 7-0: table120 15-8: table121 23-16: table122 31-24: table123

CRU_SSGTBL124_127

Address: Operational Base + offset (0x04FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl124_127 Extern wave table 124-127 7-0: table124 15-8: table125 23-16: table126 31-24: table127

CRU_AUTOCS_CORE_CON0

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	pdcore_wait_th pdcore wait time threshold, measured by original clk_core
15:0	RW	0x0020	pdcore_idle_th pdcore idle time threshold, measured by original clk_core

CRU_AUTOCS_CORE_CON1

Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg pdcore auto switch clock selection as clk_core 2'b00: original clk_core 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:11	RO	0x0	reserved
10:8	RW	0x0	step change core_div by step when clk_core automatically switched to higher frequency. acs_div = (pre_div+1)<<step -1
7	RO	0x0	reserved
6	RW	0x0	biu_active_en 1'b1: enable pdcore biu active signals as pdcore active status 1'b0: disable
5	RW	0x0	vfiqirq_en 1'b1: enable core vFIQ or vIRQ as pdcore active status 1'b0: disable
4	RW	0x0	fiqirq_en 1'b1: enable core FIQ or IRQ as pdcore active status 1'b0: disable
3	RW	0x0	wfil3_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
2	RW	0x0	wfi_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
1	RW	0x0	dsu_switch_en 1'b1: enable sclk_core automatically switched to lower frequency when pdcore is inactive 1'b0: disable
0	RW	0x0	cpu_switch_en 1'b1: enable clk_core automatically switched to lower frequency when pdcore is inactive 1'b0: disable

CRU_AUTOCS_GPU_CON0

Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_GPU_CON1

Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:2	RO	0x000	reserved
1	RW	0x0	clk_en 1'b1: enable clk_gpu switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable clk_gpu automatically switched to lower frequency when pdgpu is inactive 1'b0: disable auto switch function

CRU_AUTOCS_BUS_CON0

Address: Operational Base + offset (0x0510)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_BUS_CON1

Address: Operational Base + offset (0x0514)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:8	RO	0x00	reserved
7	RW	0x0	dmac_m_en 1'b1: enable dmac axi master active signals as pdbus active/inactive status 1'b0: disable
6	RO	0x0	reserved
5	RW	0x0	slave_en 1'b1: enable biu slave active signals as pdbus active/inactive status 1'b0: disable
4	RW	0x0	master_en 1'b1: enable biu master active signals as pdbus active/inactive status 1'b0: disable
3	RW	0x0	pclk_en 1'b1: enable pclk_bus switch to lower frequency 1'b0: disable

Bit	Attr	Reset Value	Description
2	RO	0x0	reserved
1	RW	0x0	aclk_en 1'b1: enable aclk_bus switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable aclk_bus/pclk_bus automatically switched to lower frequency when pdbus is inactive 1'b0: disable auto switch function

CRU_AUTOCS_TOP_CON0

Address: Operational Base + offset (0x0518)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_TOP_CON1

Address: Operational Base + offset (0x051C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:8	RO	0x00	reserved
7	RW	0x0	dmac_m_en 1'b1: enable dmac axi master active signals as active/inactive status 1'b0: disable
6	RO	0x0	reserved
5	RW	0x0	slave_en 1'b1: enable biu slave active signals as active/inactive status 1'b0: disable
4	RW	0x0	master_en 1'b1: enable biu master active signals as active/inactive status 1'b0: disable
3	RW	0x0	pclk_en 1'b1: enable pclk_top switch to lower frequency 1'b0: disable
2	RW	0x0	hclk_en 1'b1: enable hclk_top_biu switch to lower frequency 1'b0: disable
1	RW	0x0	aclk_en 1'b1: enable aclk_top_high_biu/aclk_top_low_biu switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable aclk_top/hclk_top/pclk_top automatically switched to lower frequency when top is inactive 1'b0: disable auto switch function

CRU_AUTOCS_RKVDEC_CON0

Address: Operational Base + offset (0x0520)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_RKVDEC_CON1

Address: Operational Base + offset (0x0524)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	aclksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:12	RW	0x0	clk_hevc_sel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
11:10	RW	0x0	clk_core_sel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
9:8	RW	0x0	clk_ca_sel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
7:5	RO	0x0	reserved
4	RW	0x0	rkvdec_clk_hevc_en 1'b1: enable clk_rkvdec_hevc switch to lower frequency 1'b0: disable
3	RW	0x0	rkvdec_clk_core_en 1'b1: enable clk_rkvdec_core switch to lower frequency 1'b0: disable
2	RW	0x0	rkvdec_clk_ca_en 1'b1: enable clk_rkvdec_ca switch to lower frequency 1'b0: disable
1	RW	0x0	rkvdec_aclk_en 1'b1: enable aclk_rkvdec switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable pdrkvdec clock automatically switched to lower frequency when pd_rkvdec is inactive 1'b0: disable auto switch function

CRU_AUTOCS_RKVENC_CON0

Address: Operational Base + offset (0x0528)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_RKVENC_CON1

Address: Operational Base + offset (0x052C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:2	RO	0x000	reserved
1	RW	0x0	clk_en 1'b1: enable aclk_rkvenc switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable aclk_rkvenc automatically switched to lower frequency when pd_rkvenc is inactive 1'b0: disable auto switch function

CRU_AUTOCS_VPU_CON0

Address: Operational Base + offset (0x0530)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_VPU_CON1

Address: Operational Base + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13:2	RO	0x000	reserved
1	RW	0x0	clk_en 1'b1: enable aclk_vpu switch to lower frequency 1'b0: disable
0	RW	0x0	switch_en 1'b1: enable aclk_vpu automatically switched to lower frequency when pd_vpu is inactive 1'b0: disable auto switch function

CRU_AUTOCS_PERI_CON0

Address: Operational Base + offset (0x0538)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_PERI_CON1

Address: Operational Base + offset (0x053C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clksel_cfg auto switch clock selection 2'b00: original clk 2'b01: xin_osc0_func_div 2'b10: clk_rtc_32k
13	RO	0x0	reserved
12	RW	0x0	dcf_m_en 1'b1: enable dcf master active signals as active/inactive status 1'b0: disable
11	RW	0x0	sf_hclk_en 1'b1: enable hclk_secure_flash switch to lower frequency 1'b0: disable
10	RW	0x0	sf_aclk_en 1'b1: enable aclk_secure_flash switch to lower frequency 1'b0: disable
9	RW	0x0	sf_switch_en 1'b1: enable aclk_secure_flash/hclk_secure_flash automatically switched to lower frequency when pd_secure_flash is inactive 1'b0: disable auto switch function
8	RW	0x0	ga_hclk_en 1'b1: enable hclk_gic_audio switch to lower frequency 1'b0: disable
7	RW	0x0	ga_aclk_en 1'b1: enable aclk_gic_audio switch to lower frequency 1'b0: disable
6	RW	0x0	ga_switch_en 1'b1: enable aclk_gic_audio/hclk_gic_audio automatically switched to lower frequency when pd_gic_audio is inactive 1'b0: disable auto switch function
5	RW	0x0	php_hclk_en 1'b1: enable hclk_php switch to lower frequency 1'b0: disable
4	RW	0x0	php_aclk_en 1'b1: enable aclk_php switch to lower frequency 1'b0: disable
3	RW	0x0	php_switch_en 1'b1: enable aclk_php/hclk_php automatically switched to lower frequency when pdphp is inactive 1'b0: disable auto switch function

Bit	Attr	Reset Value	Description
2	RW	0x0	peri_hclk_en 1'b1: enable hclk_peri switch to lower frequency 1'b0: disable
1	RW	0x0	peri_aclk_en 1'b1: enable aclk_peri switch to lower frequency 1'b0: disable
0	RW	0x0	peri_switch_en 1'b1: enable aclk_peri/hclk_peri automatically switched to lower frequency when pdperi is inactive 1'b0: disable auto switch function

CRU_AUTOCS_GPLL_CON0

Address: Operational Base + offset (0x0540)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_GPLL_CON1

Address: Operational Base + offset (0x0544)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	vfiqirq_en 1'b1: enable core vFIQ or vIRQ as pdcore active status 1'b0: disable
4	RW	0x0	fiqirq_en 1'b1: enable core FIQ or IRQ as pdcore active status 1'b0: disable
3	RW	0x0	wfil3_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
2	RW	0x0	wfi_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
1	RO	0x0	reserved
0	RW	0x0	switch_en 1'b1: enable GPLL automatically switched to lower frequency when pdcore is inactive 1'b0: disable

CRU_AUTOCS_CPLL_CON0

Address: Operational Base + offset (0x0548)

Bit	Attr	Reset Value	Description
31:16	RW	0x0004	wait_th wait time threshold, measured by original clk
15:0	RW	0x0020	idle_th idle time threshold, measured by original clk

CRU_AUTOCS_CPLL_CON1

Address: Operational Base + offset (0x054C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	vfiqirq_en 1'b1: enable core vFIQ or vIRQ as pdcore active status 1'b0: disable
4	RW	0x0	fiqirq_en 1'b1: enable core FIQ or IRQ as pdcore active status 1'b0: disable
3	RW	0x0	wfil3_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
2	RW	0x0	wfi_en 1'b1: enable standby_wfi as pdcore active/inactive status 1'b0: disable
1	RO	0x0	reserved
0	RW	0x0	switch_en 1'b1: enable CPLL automatically switched to lower frequency when pdcore is inactive 1'b0: disable

CRU_SDMMC0_CON0

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel drv_sel
10:3	RW	0x00	drv_delaynum drv_delaynum
2:1	RW	0x2	drv_degree drv_degree
0	RW	0x0	init_state init_state

CRU_SDMMC0_CON1

Address: Operational Base + offset (0x0584)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	sample_sel sample_sel
9:2	RW	0x00	sample_delaynum sample_delaynum
1:0	RW	0x0	sample_degree sample_degree

CRU_SDMMC1_CON0

Address: Operational Base + offset (0x0588)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel drv_sel
10:3	RW	0x00	drv_delaynum drv_delaynum
2:1	RW	0x2	drv_degree drv_degree
0	RW	0x0	init_state init_state

CRU_SDMMC1_CON1

Address: Operational Base + offset (0x058C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	sample_sel sample_sel
9:2	RW	0x00	sample_delaynum sample_delaynum
1:0	RW	0x0	sample_degree sample_degree

CRU_SDMMC2_CON0

Address: Operational Base + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel drv_sel
10:3	RW	0x00	drv_delaynum drv_delaynum
2:1	RW	0x2	drv_degree drv_degree
0	RW	0x0	init_state init_state

CRU_SDMMC2_CON1

Address: Operational Base + offset (0x0594)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	sample_sel sample_sel
9:2	RW	0x00	sample_delaynum sample_delaynum
1:0	RW	0x0	sample_degree sample_degree

CRU_EMMC_CON0

Address: Operational Base + offset (0x0598)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel drv_sel
10:3	RW	0x00	drv_delaynum drv_delaynum
2:1	RW	0x2	drv_degree drv_degree
0	RW	0x0	init_state init_state

CRU_EMMC_CON1

Address: Operational Base + offset (0x059C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	sample_sel sample_sel
9:2	RW	0x00	sample_delaynum sample_delaynum
1:0	RW	0x0	sample_degree sample_degree

2.5 SCRU Register Description

2.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SCRU_MPLL_CON0	0x0000	W	0x00003096	MPLL configuration register0
SCRU_MPLL_CON1	0x0004	W	0x00001042	MPLL configuration register1
SCRU_MODE_CON00	0x0020	W	0x00000000	Internal clock select and division register 0
SCRU_CLKSEL_CON00	0x0100	W	0x00000302	Internal clock select and division register 0
SCRU_CLKSEL_CON01	0x0104	W	0x00000005	Internal clock select and division register 1

Name	Offset	Size	Reset Value	Description
SCRU_CLKSEL_CON04	0x0110	W	0x00000305	Internal clock select and division register 4
SCRU_CLKSEL_CON05	0x0114	W	0x00000005	Internal clock select and division register 5
SCRU_GATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
SCRU_GATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
SCRU_GATE_CON02	0x0188	W	0x00000000	Internal clock gate and division register 2
SCRU_SOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
SCRU_SOFTRST_CON01	0x0204	W	0x00000000	Internal clock reset register 1
SCRU_SOFTRST_CON02	0x0208	W	0x00000000	Internal clock reset register 2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.5.2 Detail Registers Description

SCRU_MPLL_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x096	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

SCRU_MPLL_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down

Bit	Attr	Reset Value	Description
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

SCRU_MODE_CON00

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_spll_mode clk_spll_mux clock mux. 1'b0: clk_mpll_mux 1'b1: clk_gpll_mux
14:2	RO	0x0000	reserved
1:0	RW	0x0	clk_mpll_mode clk_mpll_mux clock mux. 2'b00: xin_osc0_func_mux 2'b01: clk_mpll 2'b10: clk_rtc_32k

SCRU_CLKSEL_CON00

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	hclk_secure_flash_s_div Divide hclk_secure_flash_s by (div_con + 1)
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x02	aclk_secure_flash_s_div Divide aclk_secure_flash_s by (div_con + 1)

SCRU_CLKSEL_CON01

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x05	pclk_secure_flash_s_div Divide pclk_secure_flash_s by (div_con + 1)

SCRU_CLKSEL_CON04

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x03	hclk_vo_s_div Divide hclk_vo_s by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x05	pclk_top_s_div Divide pclk_top_s by (div_con + 1)

SCRU_CLKSEL_CON05

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x05	pclk_ddr_div Divide pclk_ddr by (div_con + 1)

SCRU_GATE_CON00

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_sgrf_en pclk_sgrf clock gating control. When high, disable clock
14:8	RO	0x00	reserved
7	RW	0x0	clk_trng_s_en clk_trng_s clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	hclk_trng_s_en hclk_trng_s clock gating control. When high, disable clock
5	RW	0x0	pclk_secure_flash_s_biu_en pclk_secure_flash_s_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_secure_flash_s_biu_en hclk_secure_flash_s_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_secure_flash_s_biu_en aclk_secure_flash_s_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_secure_flash_s_en pclk_secure_flash_s clock gating control. When high, disable clock
1	RW	0x0	hclk_secure_flash_s_en hclk_secure_flash_s clock gating control. When high, disable clock
0	RW	0x0	aclk_secure_flash_s_en aclk_secure_flash_s clock gating control. When high, disable clock

SCRU_GATE_CON01

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_dcf_en pclk_dcf clock gating control. When high, disable clock
14	RW	0x0	aclk_dcf_en aclk_dcf clock gating control. When high, disable clock
13	RW	0x0	hclk_ahbrom_en hclk_ahbrom clock gating control. When high, disable clock
12	RW	0x0	aclk_intmem_en aclk_intmem clock gating control. When high, disable clock
11	RW	0x0	clk_trng_en clk_trng clock gating control. When high, disable clock
10	RW	0x0	pclk_trng_en pclk_trng clock gating control. When high, disable clock
9	RW	0x0	clk_jdb_en clk_jdb clock gating control. When high, disable clock
8	RW	0x0	pclk_jdb_en pclk_jdb clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	clk_otpc_s_usr_en clk_otpc_s_usr clock gating control. When high, disable clock
6	RW	0x0	clk_otpc_s_sbpi_en clk_otpc_s_sbpi clock gating control. When high, disable clock
5	RW	0x0	pclk_otpc_s_en pclk_otpc_s clock gating control. When high, disable clock
4	RW	0x0	clk_stimer1_en clk_stimer1 clock gating control. When high, disable clock
3	RW	0x0	clk_stimer0_en clk_stimer0 clock gating control. When high, disable clock
2	RW	0x0	pclk_stimer_en pclk_stimer clock gating control. When high, disable clock
1	RW	0x0	tclk_wdt_s_en tclk_wdt_s clock gating control. When high, disable clock
0	RW	0x0	pclk_wdt_s_en pclk_wdt_s clock gating control. When high, disable clock

SCRU_GATE_CON02

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_ddrdfi_ctl_en pclk_ddrdfi_ctl clock gating control. When high, disable clock
13	RW	0x0	pclk_dma2ddr_en pclk_dma2ddr clock gating control. When high, disable clock
12	RW	0x0	pclk_ddrmon_en pclk_ddrmon clock gating control. When high, disable clock
11	RW	0x0	pclk_ddrgrf_en pclk_ddrgrf clock gating control. When high, disable clock
10	RW	0x0	pclk_ddr_upctl_en pclk_ddr_upctl clock gating control. When high, disable clock
9	RW	0x0	pclk_msch_en pclk_msch clock gating control. When high, disable clock
8	RW	0x0	pclk_ddr_en pclk_ddr clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	pclk_hwffc_ctrl_en pclk_hwffc_ctrl clock gating control. When high, disable clock
6	RW	0x0	hclk_hdcp_key_en hclk_hdcp_key clock gating control. When high, disable clock
5	RW	0x0	hclk_vo_s_biu_en hclk_vo_s_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vo_s_en hclk_vo_s clock gating control. When high, disable clock
3	RW	0x0	pclk_top_scru_en pclk_top_scru clock gating control. When high, disable clock
2	RW	0x0	pclk_top_s_biu_en pclk_top_s_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_top_s_en pclk_top_s clock gating control. When high, disable clock
0	RW	0x0	pclk_key_reader_en pclk_key_reader clock gating control. When high, disable clock

SCRU_SOFTRST_CON00

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	resetn_trng When high, reset relative logic
14	RW	0x0	presetn_trng When high, reset relative logic
13	RW	0x0	resetn_jdb When high, reset relative logic
12	RW	0x0	presetn_jdb When high, reset relative logic
11:3	RO	0x000	reserved
2	RW	0x0	presetn_secure_flash_s_biu When high, reset relative logic
1	RW	0x0	hresetn_secure_flash_s_biu When high, reset relative logic
0	RW	0x0	aresetn_secure_flash_s_biu When high, reset relative logic

SCRU_SOFTRST_CON01

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	presetn_top_scru When high, reset relative logic
14	RW	0x0	presetn_top_s_biu When high, reset relative logic
13	RW	0x0	presetn_key_reader When high, reset relative logic
12	RW	0x0	presetn_dcf When high, reset relative logic
11	RW	0x0	aresetn_dcf When high, reset relative logic
10	RW	0x0	hresetn_ahbrom When high, reset relative logic
9	RW	0x0	aresetn_intmem When high, reset relative logic
8	RW	0x0	resetn_stimer1 When high, reset relative logic
7	RW	0x0	resetn_stimer0 When high, reset relative logic
6	RW	0x0	presetn_stimer When high, reset relative logic
5	RW	0x0	resetn_otpc_s_usr When high, reset relative logic
4	RW	0x0	resetn_otpc_s_sbpi When high, reset relative logic
3	RW	0x0	presetn_otpc_s When high, reset relative logic
2	RW	0x0	tresetn_wdt_s When high, reset relative logic
1	RW	0x0	presetn_wdt_s When high, reset relative logic
0	RW	0x0	presetn_sgrf When high, reset relative logic

SCRU_SOFTRST_CON02

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	resetn_trng_s When high, reset relative logic
10	RW	0x0	hresetn_trng_s When high, reset relative logic
9	RW	0x0	hresetn_hdcp_key When high, reset relative logic
8	RW	0x0	hresetn_vo_s_biu When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	presetn_hwffc_ctrl When high, reset relative logic
5	RW	0x0	presetn_ddrdfi_ctl When high, reset relative logic

Bit	Attr	Reset Value	Description
4	RW	0x0	presetn_dma2ddr When high, reset relative logic
3	RW	0x0	presetn_ddrmon When high, reset relative logic
2	RW	0x0	presetn_ddrgrf When high, reset relative logic
1	RW	0x0	presetn_ddr_upctl When high, reset relative logic
0	RW	0x0	presetn_msch When high, reset relative logic

2.6 PMUCRU Register Description

2.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMUCRU_PPLL_CON0	0x0000	W	0x00004064	PPLL configuration register0
PMUCRU_PPLL_CON1	0x0004	W	0x000010C1	PPLL configuration register1
PMUCRU_PPLL_CON2	0x0008	W	0x00000000	PPLL configuration register2
PMUCRU_PPLL_CON3	0x000C	W	0x00000007	PPLL configuration register3
PMUCRU_PPLL_CON4	0x0010	W	0x00007F00	PPLL configuration register4
PMUCRU_HPLL_CON0	0x0040	W	0x00002063	HPLL configuration register0
PMUCRU_HPLL_CON1	0x0044	W	0x00001081	HPLL configuration register1
PMUCRU_HPLL_CON2	0x0048	W	0x00000000	HPLL configuration register2
PMUCRU_HPLL_CON3	0x004C	W	0x00000007	HPLL configuration register3
PMUCRU_HPLL_CON4	0x0050	W	0x00007F00	HPLL configuration register4
PMUCRU_MODE_CON00	0x0080	W	0x00000000	Internal clock select and division register 0
PMUCRU_PMUCLKSEL_CON00	0x0100	W	0x00000080	Internal clock select and division register 0
PMUCRU_PMUCLKSEL_CON01	0x0104	W	0x00000000	Internal clock select and division register 1
PMUCRU_PMUCLKSEL_CON02	0x0108	W	0x00008001	Internal clock select and division register 2
PMUCRU_PMUCLKSEL_CON03	0x010C	W	0x00000001	Internal clock select and division register 3
PMUCRU_PMUCLKSEL_CON04	0x0110	W	0x00000800	Internal clock select and division register 4
PMUCRU_PMUCLKSEL_CON05	0x0114	W	0x00000000	Internal clock select and division register 5
PMUCRU_PMUCLKSEL_CON06	0x0118	W	0x00000001	Internal clock select and division register 6
PMUCRU_PMUCLKSEL_CON07	0x011C	W	0x00000009	Internal clock select and division register 7
PMUCRU_PMUCLKSEL_CON08	0x0120	W	0x0000058F	Internal clock select and division register 8
PMUCRU_PMUCLKSEL_CON09	0x0124	W	0x00000BBB	Internal clock select and division register 9
PMUCRU_PMUGATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
PMUCRU_PMUGATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
PMUCRU_PMUGATE_CON02	0x0188	W	0x00000000	Internal clock gate and division register 2

Name	Offset	Size	Reset Value	Description
PMUCRU_PMUSOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.6.2 Detail Registers Description

PMUCRU_PPLL_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x4	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x064	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

PMUCRU_PPLL_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:6	RW	0x3	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

PMUCRU_PPLL_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

PMUCRU_PPLL_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass

Bit	Attr	Reset Value	Description
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

PMUCRU_PPLL_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

PMUCRU_HPLL_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x063	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

PMUCRU_HPLL_CON1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted

Bit	Attr	Reset Value	Description
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable, 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x2	postdiv2 Second Post Divide Value (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value (1-63)

PMUCRU_HPLL_CON2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

PMUCRU_HPLL_CON3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

PMUCRU_HPLL_CON4

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs, (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

PMUCRU_MODE_CON00

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x0	clk_hpll_mode clk_hpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_hpll 2'b10: clk_rtc_32k

Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_ppll_mode clk_ppll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_ppll 2'b10: clk_rtc_32k

PMUCRU_PMUCLKSEL_CON00

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x2	clk_rtc_32k_sel clk_rtc_32k clock mux. 2'b00: clk_32k_from_pvtm 2'b01: clk_32k_from_io 2'b10: clk_osc0_div32k
5	RO	0x0	reserved
4:0	RW	0x00	xin_osc0_div_div Divide xin_osc0_div by (div_con + 1)

PMUCRU_PMUCLKSEL_CON01

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	clk_osc0_div32k_div clk_osc0_div32k fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMUCRU_PMUCLKSEL_CON02

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_pdpmu_mux_sel clk_pdpmu_mux clock mux. 1'b0: clk_ppll_mux 1'b1: clk_gpll_mux
14:5	RO	0x000	reserved
4:0	RW	0x01	pclk_pdpmu_pre_div Divide pclk_pdpmu_pre by (div_con + 1)

PMUCRU_PMUCLKSEL_CON03

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x01	clk_i2c0_div Divide clk_i2c0 by (div_con + 1)

PMUCRU_PMUCLKSEL_CON04

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x2	sclk_uart0_sel sclk_uart0 clock mux. 2'b00: sclk_uart0_div 2'b01: sclk_uart0_fracdiv 2'b10: xin_osc0_func
9:8	RW	0x0	sclk_uart0_div_sel sclk_uart0_div clock mux. 2'b00: clk_ppll_mux 2'b01: usbphy_clk480m_mux 2'b10: clk_cpll_mux 2'b11: clk_gpll_mux
7	RO	0x0	reserved
6:0	RW	0x00	sclk_uart0_div_div Divide sclk_uart0_div by (div_con + 1)

PMUCRU_PMUCLKSEL_CON05

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sclk_uart0_fracdiv_div sclk_uart0_fracdiv fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMUCRU_PMUCLKSEL_CON06

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dbclk_gpio0_sel dbclk_gpio0 clock mux. 1'b0: xin_osc0_func 1'b1: clk_rtc_32k
14:8	RO	0x00	reserved
7	RW	0x0	clk_pwm0_sel clk_pwm0 clock mux. 1'b0: xin_osc0_func 1'b1: clk_pdpmu_mux
6:0	RW	0x01	clk_pwm0_div Divide clk_pwm0 by (div_con + 1)

PMUCRU_PMUCLKSEL_CON07

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x09	clk_ref24m_div Divide clk_ref24m by (div_con + 1)

PMUCRU_PMUCLKSEL_CON08

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_wifi_sel clk_wifi clock mux. 1'b0: clk_wifi_osc0 1'b1: clk_wifi_div
14	RO	0x0	reserved
13:8	RW	0x05	clk_wifi_div_div Divide clk_wifi_div by (div_con + 1)
7	RW	0x1	clk_hdmiphy_ref_sel clk_hdmiphy_ref clock mux. 1'b0: clk_hpll 1'b1: clk_hpll_ph0
6:4	RO	0x0	reserved
3	RW	0x1	clk_mipidsiphy1_ref_sel clk_mipidsiphy1_ref clock mux. 1'b0: clk_ref24m 1'b1: xin_osc0_mipidsiphy1_g
2	RW	0x1	clk_mipidsiphy0_ref_sel clk_mipidsiphy0_ref clock mux. 1'b0: clk_ref24m 1'b1: xin_osc0_mipidsiphy0_g
1	RW	0x1	clk_usbphy1_ref_sel clk_usbphy1_ref clock mux. 1'b0: clk_ref24m 1'b1: xin_osc0_usbphy1_g
0	RW	0x1	clk_usbphy0_ref_sel clk_usbphy0_ref clock mux. 1'b0: clk_ref24m 1'b1: xin_osc0_usbphy0_g

PMUCRU_PMUCLKSEL_CON09

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x1	clk_pciephy2_ref_sel clk_pciephy2_ref clock mux. 1'b0: clk_pciephy2_osc0 1'b1: clk_pciephy2_div
10:8	RW	0x3	clk_pciephy2_div_div Divide clk_pciephy2_div by (div_con + 1)
7	RW	0x1	clk_pciephy1_ref_sel clk_pciephy1_ref clock mux. 1'b0: clk_pciephy1_osc0 1'b1: clk_pciephy1_div
6:4	RW	0x3	clk_pciephy1_div_div Divide clk_pciephy1_div by (div_con + 1)
3	RW	0x1	clk_pciephy0_ref_sel clk_pciephy0_ref clock mux. 1'b0: clk_pciephy0_osc0 1'b1: clk_pciephy0_div
2:0	RW	0x3	clk_pciephy0_div_div Divide clk_pciephy0_div by (div_con + 1)

PMUCRU_PMUGATE_CON00

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_pmu_en clk_pmu clock gating control. When high, disable clock
6	RW	0x0	pclk_pmu_en pclk_pmu clock gating control. When high, disable clock
5	RW	0x0	pclk_pmugrf_en pclk_pmugrf clock gating control. When high, disable clock
4	RW	0x0	pclk_pmucru_en pclk_pmucru clock gating control. When high, disable clock
3	RW	0x0	pclk_pdpmu_biu_en pclk_pdpmu_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_pdpmu_en pclk_pdpmu_pre clock gating control. When high, disable clock
1	RW	0x0	clk_osc0_div32k_en clk_osc0_div32k clock gating control. When high, disable clock
0	RW	0x0	xin_osc0_div_en xin_osc0_div clock gating control. When high, disable clock

PMUCRU_PMUGATE_CON01

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_core_pmupvtm_en clk_core_pmupvtm clock gating control. When high, disable clock
12	RW	0x0	clk_pmupvtm_en clk_pmupvtm clock gating control. When high, disable clock
11	RW	0x0	pclk_pmupvtm_en pclk_pmupvtm clock gating control. When high, disable clock
10	RW	0x0	dbclk_gpio0_en dbclk_gpio0 clock gating control. When high, disable clock
9	RW	0x0	pclk_gpio0_en pclk_gpio0 clock gating control. When high, disable clock
8	RW	0x0	clk_capture_pwm0_en clk_capture_pwm0_ndft clock gating control. When high, disable clock
7	RW	0x0	clk_pwm0_en clk_pwm0 clock gating control. When high, disable clock
6	RW	0x0	pclk_pwm0_en pclk_pwm0 clock gating control. When high, disable clock
5	RW	0x0	sclk_uart0_en sclk_uart0 clock gating control. When high, disable clock
4	RW	0x0	sclk_uart0_fracdiv_en sclk_uart0_fracdiv clock gating control. When high, disable clock
3	RW	0x0	sclk_uart0_div_en sclk_uart0_div clock gating control. When high, disable clock
2	RW	0x0	pclk_uart0_en pclk_uart0 clock gating control. When high, disable clock
1	RW	0x0	clk_i2c0_en clk_i2c0 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c0_en pclk_i2c0 clock gating control. When high, disable clock

PMUCRU_PMUGATE_CON02

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	xin_osc0_edpphy_en xin_osc0_edpphy clock gating control. When high, disable clock
14	RW	0x0	clk_pcie30phy_ref_n_en clk_pcie30phy_ref_n clock gating control. When high, disable clock
13	RW	0x0	clk_pcie30phy_ref_m_en clk_pcie30phy_ref_m clock gating control. When high, disable clock
12	RW	0x0	clk_pciephy2_osc0_en clk_pciephy2_osc0 clock gating control. When high, disable clock
11	RW	0x0	clk_pciephy2_div_en clk_pciephy2_div clock gating control. When high, disable clock
10	RW	0x0	clk_pciephy1_osc0_en clk_pciephy1_osc0 clock gating control. When high, disable clock
9	RW	0x0	clk_pciephy1_div_en clk_pciephy1_div clock gating control. When high, disable clock
8	RW	0x0	clk_pciephy0_osc0_en clk_pciephy0_osc0 clock gating control. When high, disable clock
7	RW	0x0	clk_pciephy0_div_en clk_pciephy0_div clock gating control. When high, disable clock
6	RW	0x0	clk_wifi_osc0_en clk_wifi_osc0 clock gating control. When high, disable clock
5	RW	0x0	clk_wifi_div_en clk_wifi_div clock gating control. When high, disable clock
4	RW	0x0	xin_osc0_mipidsiphy1_en xin_osc0_mipidsiphy1_g clock gating control. When high, disable clock
3	RW	0x0	xin_osc0_mipidsiphy0_en xin_osc0_mipidsiphy0_g clock gating control. When high, disable clock
2	RW	0x0	xin_osc0_usbphy1_en xin_osc0_usbphy1_g clock gating control. When high, disable clock
1	RW	0x0	xin_osc0_usbphy0_en xin_osc0_usbphy0_g clock gating control. When high, disable clock
0	RW	0x0	clk_ref24m_en clk_ref24m clock gating control. When high, disable clock

PMUCRU_PMUSOFTRST_CON00

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	resetn_pmupvtm When high, reset relative logic
11	RW	0x0	presetn_pmupvtm When high, reset relative logic
10	RW	0x0	dbresetn_gpio0 When high, reset relative logic
9	RW	0x0	presetn_gpio0 When high, reset relative logic
8	RW	0x0	resetn_pwm0 When high, reset relative logic
7	RW	0x0	presetn_pwm0 When high, reset relative logic
6	RW	0x0	sresetn_uart0 When high, reset relative logic
5	RW	0x0	presetn_uart0 When high, reset relative logic
4	RW	0x0	resetn_i2c0 When high, reset relative logic
3	RW	0x0	presetn_i2c0 When high, reset relative logic
2	RW	0x0	presetn_pmugrf When high, reset relative logic
1	RW	0x0	presetn_pmucru When high, reset relative logic
0	RW	0x0	presetn_pdpmu_biu When high, reset relative logic

2.7 PMUSCRU Register Description

2.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMUSCRU_PMUCLKSEL_CON00	0x0100	W	0x00000101	Internal clock select and division register 0
PMUSCRU_PMUGATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
PMUSCRU_PMUSOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.7.2 Detail Registers Description

PMUSCRU_PMUCLKSEL_CON00

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x01	hclk_pdpmu_s_div Divide hclk_pdpmu_s by (div_con + 1)
7:5	RO	0x0	reserved
4:0	RW	0x01	pclk_pdpmu_s_div Divide pclk_pdpmu_s by (div_con + 1)

PMUSCRU_PMUGATE_CON00

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pclk_osc_ck_en pclk_osc_ck clock gating control. When high, disable clock
8	RW	0x0	pclk_scrkeygen_en pclk_scrkeygen clock gating control. When high, disable clock
7	RW	0x0	pclk_pmusgrf_en pclk_pmusgrf clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_pmucru_s_en pclk_pmucru_s clock gating control. When high, disable clock
4	RW	0x0	pclk_pmu_s_biu_en pclk_pmu_s_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_pmumem_en hclk_pmumem clock gating control. When high, disable clock
2	RW	0x0	hclk_pmu_s_biu_en hclk_pmu_s_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_pdpmu_s_en hclk_pdpmu_s clock gating control. When high, disable clock
0	RW	0x0	pclk_pdpmu_s_en pclk_pdpmu_s clock gating control. When high, disable clock

PMUSCRU_PMUSOFTRST_CON00

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	resetn_ddr_fail_safe When high, reset relative logic
6	RW	0x0	presetn_osc_ck When high, reset relative logic

Bit	Attr	Reset Value	Description
5	RW	0x0	presetn_pmusgrf_remap When high, reset relative logic
4	RW	0x0	presetn_pmusgrf When high, reset relative logic
3	RW	0x0	presetn_pmucru When high, reset relative logic
2	RW	0x0	presetn_pdpmu_biu When high, reset relative logic
1	RW	0x0	hresetn_pmumem When high, reset relative logic
0	RW	0x0	hresetn_pdpmu_biu When high, reset relative logic

2.8 Application Notes

2.8.1 Fractional PLL Usage

2.8.1.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1.
FRAC can be configured by programming CRU_xPLL_CON2.(x=A,D,C,P,H,G)
If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=700/1/1=700
If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24))
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24)) = 983.04
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=983.04/(2*1)=491.52
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.8.1.2 PLL Setting Consideration

- If the POSTDIV value is changed during operation, a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.
- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used.

The normal operating range for the VCO is described above in.

- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
  - DSMPD=1 (Integer Mode)
  - DSMPD=0 (Fractional Mode)
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

2.8.1.3 PLL Frequency Change And Lock Check

The PLL programming supports changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be checked in CRU_xPLL_CON1[10] (x=A,D,C,P,H,G) register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 500*REFDIV/FREF.
PLL locking consists of three phases.

- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.
- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 128 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 128*REFDIV/FREF.

2.8.2 Integer PLL Usage

2.8.2.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1(x=M,N,V).

DSMPD should always be set to 1 (CLKSSCG is power down), and REFDIV can only be 1 or 2.
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.8.2.2 PLL Frequency Change And Lock Check

The PLL programming supports changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be checked in CRU_xPLL_CON1[10] (x=M,N,V) register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 1500*REFDIV/FREF.

2.8.3 Divider Usage

CRU supports multi-dividers for different clock requirement.

- Divider free divider
- Fractional divider
- Divfree50 divider
- DivfreeNP5 divider

2.8.3.1 Fractional Divider Usage

To get specific frequency, clocks of I2S, audioPWM, UARTand SPDIF can be generated by fractional divider. Generally you should set that denominator 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock. For implementation issue, the input source clocks of fractional divider should limit to less than 1200MHz.

2.8.3.2 Divfree50 Divider Usage

Some moduleslikePDM, EMMC, SDIO, SDMMC, FSPI and NANDC need clock of 50% duty cycle, divfree50 can generate clock of 50% duty cycle even in odd value divisor.

2.8.3.3 DivFreeNP5 Divider Usage

Some modules likeNPU, ISPP and ISP need some special frequency can use this divider. Frequency of this divider=clk_src/((2*n+1)/2).

2.8.4 Global Software Reset

Two global software resets are designed in RK3568, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-de-asserted by hardware. Resetting hold timing of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 1ms.

glb_srstn_1 resets almost all logic except some registers just supporting hardware reset.

glb_srstn_2 resets almost all logic except GRFs and GPIOs.

Reset for IP in PD_PMU can be hold if its reset_hold_enable in PMUGRF_PMU_SOC_CON1 or PMUGRF_PMU_SOC_CON2 is high even if glb_srstn_1 or glb_srstn_2 active.

2.8.5 SSCG Usage

There are some scenes where SSCG should be enabled. One scene is in communication where a fixed frequency is required. Another scene is a system requiring a clock with low long-term jitter. When SSCG is used, the PLL should be configured to fractional mode firstly for spread spectrum capability.

2.8.5.1 SSCG Use InternalPoint Table

User can use SSCG with internal point table as following steps:

- Setting ssmod_spread(CRU_XPLL_CON3[12:8]) andssmod_downspread(CRU_XPLL_CON3[3])

The modulation amplitude is controlled by the value of ssmod_spread. A ssmod_spread value of5’d0 turns off the modulation. A ssmod_spread value of 5’d31 (5’b11111) gives maximummodulation while a value of 5’d1gives minimum modulation.

The modulation amplitude can be calculated from the value of modulation by:

Modulation Amplitude = ±5’d(ssmod_spread)*0.1%

The modulation direction is determined by thessmod_downspread bit.

- ssmod_downspread=1’b1, down spread mode is used. If ssmod_spread = 5’d29, the maximum PLL frequency is the nominallyprogrammed value FNOM, and the minimumvalue is given by FNOM* (1–0.029).
- ssmod_downspread=1’b0,center spread modeis used. If ssmod_spread = 5’d29, the maximum PLL frequency would be determined by FNOM*(1+0.029) and theminimum frequency by FNOM* (1–0.029).

Setting the style of modulation (center versus down) and the modulation amplitude depend on the amount of EMI reduction desired and the timing margin for circuits running on the spread clock domain. The larger the spread value, the greater the reduction in EMI amplitude. However, the larger the spread value, the more timing margin needed for correct circuit operation.

- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1’b0

When use internal point table, the frequency will change as following during 128 point:

- Change from minimum value to maximum value uniformly within 64 points
- Change from maximum value to minimum value uniformly within 64 points

Spread spectrum modulator is implemented by repeating as above.

- Setting ssmod_divval(CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF / (Point number*REFDIV*ssmod_divval). The FMOD is typically set above 32KHz and below the maximum frequency for modulation fidelity, which isdetermined by the PLL bandwidth. The maximum modulation frequency is conservativelyset at FREF/(200*REFDIV).

When FREF=24MHz and REFDIV= 1, the value of ssmod_divval can be 5, then the FMOD is 37.5KHz.

- Setting ssmod_bp(CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg(CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset(CRU_XPLL_CON3[2])=1'b0

2.8.5.2 SSCG Use External Point Table

In addition to the internal shape table, an external shape table can be used.

This enables customization tables in both shape and the number of sample points for theenvelope wave formup to 128 data points. The external table of 128 data points can be configured from CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31.

User can use SSMOD with external point table as following steps:

- Setting ssmod_spread(CRU_XPLL_CON3[12:8]) andssmod_downspread(CRU_XPLL_CON3[3]), same with internal point table usage.
- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1'b1
- Setting ssmod_ext_maxaddr(CRU_XPLL_CON4[15:8]) and table0~table127(CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31)

ssmod_ext_maxaddr is the maximum table address. For example, if the number of points describing the envelope shape is 128, the ssmod_ext_maxaddr should be configured to 127. The table address circulate over the range 0 to 127.

The table0~table127 must be 8 bit numbers in the form of sign and magnitude.

- 1.00 is represented by 8'b01111111, it is corresponded to maximum frequency.
- -1.00 is represented in the table by8'b11111111, it is corresponded to minimum frequency.
- 0.5 is represented in the table by 8'b00111111.
- -0.5is represented in the table by 8'b10111111.

The frequency will change base table0~table127 within 128 points, and then repeat.

- Setting ssmod_divval(CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF/(Point number*REFDIV*ssmod_divval). The point number equals to ssmod_ext_maxaddr+1.

- Setting ssmod_bp(CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg(CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset(CRU_XPLL_CON3[2])=1'b0

2.8.6 NIU Clock gating reliance

A part of niu clocks have a dependence on another niu clock in order to sharing the internal bus. When these clocks are in use, another niu clock must be opened, and cannot be gated. These clocks and the special clock on which they are relied are as following:

Table 2-1NIU Clocks dependency

Clocks which have dependency	The clock which can not be gated
hclk_secure_flash_s_niu pclk_secure_flash_s_niu hclk_secure_flash_niu aclk_secure_flash_s_niu	aclk_secure_flash_niu
pclk_npu_niu	hclk_npu_niu
pclk_pipe_niu	aclk_pipe_niu
pclk_php_niu	hclk_php_niu
pclk_vo_niu hclk_vo_s_niu	hclk_vo_niu
hclk_ga_niu	aclk_ga_niu
pclk_rga_niu	hclk_rga_niu
pclk_gpu_niu	aclk_gpu_niu
pclk_core_niu	hclk_core_niu
pclk_usb_niu	hclk_usb_niu
pclk_vi_niu	hclk_vi_niu

Clocks which have dependency	The clock which can not be gated
hclk_pmu_niu pclk_pmu_s_niu	pclk_pmu_niu
pclk_top_niu_s	pclk_top_niu
pclk_bus_niu	aclk_bus_niu

Chapter 3 General Register Files (GRF)

3.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

- PMU_GRF, used for always on logic control
- CPU_GRF, used for always on system
- DDR_GRF, used for DDR system
- PIPE_GRF, used for pipe interface controller ,
- SYS_GRF, used for general system
- PIPEPHY_GRF,used for pipe interface phy
- USBPHY_U3_GRF,used for usb3 phy
- USBPHY_U2_GRF,used for usb2 phy
- EDP_PHY_GRF,used for eDP PHY control
- PCIEPHY_GRF,used for pcie3.0 phy
- USB_GRF,used for usb2 host controller

3.2 Function Description

The function of general register file is:

- GPIO IOMUX control
- GPIO PAD pull down and pull up control
- Common system control
- Record the system state

Table 3-1GRF Adress Mapping Table

Name	Address Base
PMU_GRF	0xFDC20000
CPU_GRF	0xFDC30000
DDR_GRF	0xFDC40000
PIPE_GRF	0xFDC50000
SYS_GRF	0xFDC60000
PIPE_PHY_GRF0	0xFDC70000
PIPE_PHY_GRF1	0xFDC80000
PIPE_PHY_GRF2	0xFDC90000
USBPHY_U3_GRF	0xFDCA0000
USBPHY_U2_GRF	0xFDCA8000
EDP_PHY_GRF	0xFDCB0000
PCIE30_PHY_GRF	0xFDCB8000
USB_GRF	0xFDCF0000

3.3 PMU_GRF Register Description

3.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_GRF_GPIO0A_IOMUX_L	0x0000	W	0x00000000	GPIO0A IOMUX control low bits
PMU_GRF_GPIO0A_IOMUX_H	0x0004	W	0x00001000	GPIO0A IOMUX control high bits
PMU_GRF_GPIO0B_IOMUX_L	0x0008	W	0x00000000	GPIO0B IOMUX control low bits
PMU_GRF_GPIO0B_IOMUX_H	0x000C	W	0x00000000	GPIO0B IOMUX control high bits

Name	Offset	Size	Reset Value	Description
PMU_GRF_GPIO0C_IOMUX_L	0x0010	W	0x00000000	GPIO0C IOMUX control low bits
PMU_GRF_GPIO0C_IOMUX_H	0x0014	W	0x00000000	GPIO0C IOMUX control high bits
PMU_GRF_GPIO0D_IOMUX_L	0x0018	W	0x00000000	GPIO0D IOMUX control low bits
PMU_GRF_GPIO0D_IOMUX_H	0x001C	W	0x00000000	GPIO0D IOMUX control high bits
PMU_GRF_GPIO0A_P	0x0020	W	0x00006962	GPIO0A PU/PD control
PMU_GRF_GPIO0B_P	0x0024	W	0x00009555	GPIO0B PU/PD control
PMU_GRF_GPIO0C_P	0x0028	W	0x0000AAAA	GPIO0C PU/PD control
PMU_GRF_GPIO0D_P	0x002C	W	0x00002A85	GPIO0D PU/PD control
PMU_GRF_GPIO0A_IE	0x0030	W	0x0000FFFF	GPIO0A PAD input enable control
PMU_GRF_GPIO0B_IE	0x0034	W	0x0000FFFF	GPIO0B PAD input enable control
PMU_GRF_GPIO0C_IE	0x0038	W	0x0000FFFF	GPIO0C PAD input enable control
PMU_GRF_GPIO0D_IE	0x003C	W	0x0000FFFF	GPIO0D PAD input enable control
PMU_GRF_GPIO0A_OPD	0x0040	W	0x00000000	GPIO0A PAD open drain functionality enable
PMU_GRF_GPIO0B_OPD	0x0044	W	0x00000000	GPIO0B PAD open drain functionality enable
PMU_GRF_GPIO0C_OPD	0x0048	W	0x00000000	GPIO0C PAD open drain functionality enable
PMU_GRF_GPIO0D_OPD	0x004C	W	0x00000000	GPIO0D PAD open drain functionality enable
PMU_GRF_GPIO0A_SUS	0x0050	W	0x00000000	GPIO0A PAD weak Pull Keeper enable
PMU_GRF_GPIO0B_SUS	0x0054	W	0x00000000	GPIO0B PAD weak Pull Keeper enable
PMU_GRF_GPIO0C_SUS	0x0058	W	0x00000000	GPIO0C PAD weak Pull Keeper enable
PMU_GRF_GPIO0D_SUS	0x005C	W	0x00000000	GPIO0D PAD weak Pull Keeper enable
PMU_GRF_GPIO0A_SL	0x0060	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD
PMU_GRF_GPIO0B_SL	0x0064	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD
PMU_GRF_GPIO0C_SL	0x0068	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD
PMU_GRF_GPIO0D_SL	0x006C	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD
PMU_GRF_GPIO0A_DS_0	0x0070	W	0x00000101	GPIO0A driver strength control
PMU_GRF_GPIO0A_DS_1	0x0074	W	0x00000101	GPIO0A driver strength control
PMU_GRF_GPIO0A_DS_2	0x0078	W	0x00000101	GPIO0A driver strength control
PMU_GRF_GPIO0A_DS_3	0x007C	W	0x00000101	GPIO0A driver strength control
PMU_GRF_GPIO0B_DS_0	0x0080	W	0x00000101	GPIO0B driver strength control
PMU_GRF_GPIO0B_DS_1	0x0084	W	0x00000101	GPIO0B driver strength control
PMU_GRF_GPIO0B_DS_2	0x0088	W	0x00000101	GPIO0B driver strength control
PMU_GRF_GPIO0B_DS_3	0x008C	W	0x00000101	GPIO0B driver strength control
PMU_GRF_GPIO0C_DS_0	0x0090	W	0x00000101	GPIO0C driver strength control
PMU_GRF_GPIO0C_DS_1	0x0094	W	0x00000101	GPIO0C driver strength control
PMU_GRF_GPIO0C_DS_2	0x0098	W	0x00000101	GPIO0C driver strength control
PMU_GRF_GPIO0C_DS_3	0x009C	W	0x00000101	GPIO0C driver strength control
PMU_GRF_GPIO0D_DS_0	0x00A0	W	0x00000101	GPIO0D driver strength control

Name	Offset	Size	Reset Value	Description
PMU_GRF_SOC_CON0	0x0100	W	0x00000000	SOC control register0
PMU_GRF_SOC_CON1	0x0104	W	0x00000000	SOC control register1
PMU_GRF_SOC_CON2	0x0108	W	0x00000000	SOC control register2
PMU_GRF_SOC_CON3	0x010C	W	0x0000821C	SOC control register3
PMU_GRF_SOC_CON4	0x0110	W	0x0000401B	SOC control register4
PMU_GRF_SOC_CON5	0x0114	W	0x0000081B	SOC control register5
PMU_GRF_SOC_STATUS	0x0120	R	0x00000000	SOC status
PMU_GRF_IO_VSEL0	0x0140	W	0x00000000	IO voltage seletion register0
PMU_GRF_IO_VSEL1	0x0144	W	0x000000FF	IO voltage seletion register0
PMU_GRF_IO_VSEL2	0x0148	W	0x00000030	IO voltage seletion register0
PMU_GRF_DLL_CON0	0x0180	W	0x00000003	Register0000 Description
PMU_GRF_OS_REG0	0x0200	W	0x00000000	PMU GRF OS register0
PMU_GRF_OS_REG1	0x0204	W	0x00000000	PMU GRF OS register1
PMU_GRF_OS_REG2	0x0208	W	0x00000000	PMU GRF OS register2
PMU_GRF_OS_REG3	0x020C	W	0x00000000	PMU GRF OS register3
PMU_GRF_OS_REG4	0x0210	W	0x00000000	PMU GRF OS register4
PMU_GRF_OS_REG5	0x0214	W	0x00000000	PMU GRF OS register5
PMU_GRF_OS_REG6	0x0218	W	0x00000000	PMU GRF OS register6
PMU_GRF_OS_REG7	0x021C	W	0x00000000	PMU GRF OS register7
PMU_GRF_OS_REG8	0x0220	W	0x00000000	PMU GRF OS register8
PMU_GRF_OS_REG9	0x0224	W	0x00000000	PMU GRF OS register9
PMU_GRF_OS_REG10	0x0228	W	0x00000000	PMU GRF OS register10
PMU_GRF_OS_REG11	0x022C	W	0x00000000	PMU GRF OS register11
PMU_GRF_RESET_FUNCTION_STATUS	0x0230	W	0x00000000	system reset status register
PMU_GRF_RESET_FUNCTION_CLR	0x0234	W	0x00000000	system reset status clear register
PMU_GRF_SIG_DETECT_CON	0x0380	W	0x00000000	sdmmc detect control reg
PMU_GRF_SIG_DETECT_STATUS	0x0390	W	0x00000000	sdmmc detect status reg
PMU_GRF_SIG_DETECT_STATUS_CLEAR	0x03A0	W	0x00000000	sdmmcirq clear reg
PMU_GRF_SDMMC_DET_COUNTER	0x03B0	W	0x000003E8	sdmmc detect counter reg

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.3.2 Detail Registers Description

PMU_GRF_GPIO0A_IOMUX_L

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0a3_sel 3'h0: GPIO0_A3
11	RO	0x0	reserved
10:8	RW	0x0	gpio0a2_sel 3'h0: GPIO0_A2 3'h1: PMIC_SLEEP 3'h2: TSADC_SHUTM1

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:4	RW	0x0	gpio0a1_sel 3'h0: GPIO0_A1 3'h1: TSADC_SHUTM0 3'h2: TSADC_SHUTORG
3	RO	0x0	reserved
2:0	RW	0x0	gpio0a0_sel 3'h0: GPIO0_A0 3'h1: REFCLK_OU

PMU_GRF_GPIO0A_IOMUX_H

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x1	gpio0a7_sel 3'h0: GPIO0_A7 3'h1: FLASH_VOLSEL
11	RO	0x0	reserved
10:8	RW	0x0	gpio0a6_sel 3'h0: GPIO0_A6 3'h1: SATA_CPPOD 3'h2: PCIE30X2_CLKREQNM0 3'h3: PMU_DEBUG1 3'h4: GPU_PWREN
7	RO	0x0	reserved
6:4	RW	0x0	gpio0a5_sel 3'h0: GPIO0_A5 3'h1: SDMMC0_PWREN 3'h2: SATA_MPSWITCH 3'h3: PCIE20_CLKREQNM0 3'h4: PMU_DEBUG0
3	RO	0x0	reserved
2:0	RW	0x0	gpio0a4_sel 3'h0: GPIO0_A4 3'h1: SDMMC0_DET 3'h2: SATA_CPDET 3'h3: PCIE30X1_CLKREQNM0

PMU_GRF_GPIO0B_IOMUX_L

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio0b3_sel 3'h0: GPIO0_B3 3'h1: I2C1_SCL 3'h2: CAN0_TXM0 3'h3: PCIE30X1_BUTTONRSTN 3'h4: MCU_JTAGTDO
11	RO	0x0	reserved
10:8	RW	0x0	gpio0b2_sel 3'h0: GPIO0_B2 3'h1: I2C0_SDA
7	RO	0x0	reserved
6:4	RW	0x0	gpio0b1_sel 3'h0: GPIO0_B1 3'h1: I2C0_SCL
3	RO	0x0	reserved
2:0	RW	0x0	gpio0b0_sel 3'h0: GPIO0_B0 3'h1: CLK32K_IN 3'h2: CLK32K_OUT0 3'h3: PCIE30X2_BUTTONRSTN

PMU_GRF_GPIO0B_IOMUX_H

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0b7_sel 3'h0: GPIO0_B7 3'h1: PWM0_M0 3'h2: CPU_AVS
11	RO	0x0	reserved
10:8	RW	0x0	gpio0b6_sel 3'h0: GPIO0_B6 3'h1: I2C2_SDAM0 3'h2: SPI0_MOSIM0 3'h3: PCIE20_PERSTNM0 3'h4: PWM2_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio0b5_sel 3'h0: GPIO0_B5 3'h1: I2C2_SCLM0 3'h2: SPI0_CLKM0 3'h3: PCIE20_WAKENM0 3'h4: PWM1_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio0b4_sel 3'h0: GPIO0_B4 3'h1: I2C1_SDA 3'h2: CAN0_RXM0 3'h3: PCIE20_BUTTONRSTN 3'h4: MCU_JTAGTCK

PMU_GRF_GPIO0C_IOMUX_L

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0c3_sel 3'h0: GPIO0_C3 3'h1: PWM4 3'h2: VOP_PWMM0 3'h3: PCIE30X1_PERSTNM0 3'h4: MCU_JTAGTRSTN
11	RO	0x0	reserved
10:8	RW	0x0	gpio0c2_sel 3'h0: GPIO0_C2 3'h1: PWM3 3'h2: EDPDP_HPDINM1 3'h3: PCIE30X1_WAKENM0 3'h4: MCU_JTAGTMS
7	RO	0x0	reserved
6:4	RW	0x0	gpio0c1_sel 3'h0: GPIO0_C1 3'h1: PWM2_M0 3'h2: NPU_AVS 3'h3: UART0_TX 3'h4: MCU_JTAGTDI
3	RO	0x0	reserved
2:0	RW	0x0	gpio0c0_sel 3'h0: GPIO0_C0 3'h1: PWM1_M0 3'h2: GPU_AVS 3'h3: UART0_RX

PMU_GRF_GPIO0C_IOMUX_H

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0c7_sel 3'h0: GPIO0_C7 3'h1: HDMITX_CECM1 3'h2: PWM0_M1 3'h3: UART0_CTSN 3'h4: PMU_DEBUG5
11	RO	0x0	reserved
10:8	RW	0x0	gpio0c6_sel 3'h0: GPIO0_C6 3'h1: PWM7 3'h2: SPI0_CS0M0 3'h3: PCIE30X2_PERSTNM0 3'h4: PMU_DEBUG4

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:4	RW	0x0	gpio0c5_sel 3'h0: GPIO0_C5 3'h1: PWM6 3'h2: SPI0_MISOM0 3'h3: PCIE30X2_WAKENM0 3'h4: PMU_DEBUG3
3	RO	0x0	reserved
2:0	RW	0x0	gpio0c4_sel 3'h0: GPIO0_C4 3'h1: PWM5 3'h2: SPI0_CS1M0 3'h3: UART0_RTSN 3'h4: PMU_DEBUG2

PMU_GRF_GPIO0D_IOMUX_L

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0d3_sel 3'h0: GPIO0_D3
11:7	RO	0x0	reserved
6:4	RW	0x0	gpio0d1_sel 3'h0: GPIO0_D1 3'h1: UART2_TXM0
3	RO	0x0	reserved
2:0	RW	0x0	gpio0d0_sel 3'h0: GPIO0_D0 3'h1: UART2_RXM0

PMU_GRF_GPIO0D_IOMUX_H

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x0	reserved
10:8	RW	0x0	gpio0d6_sel 3'h0: GPIO0_D6
7	RO	0x0	reserved
6:4	RW	0x0	gpio0d5_sel 3'h0: GPIO0_D5
3	RO	0x0	reserved
2:0	RW	0x0	gpio0d4_sel 3'h0: GPIO0_D4

PMU_GRF_GPIO0A_P

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio0a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio0a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio0a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio0a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio0a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio0a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x0	gpio0a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio0a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

PMU_GRF_GPIO0B_P

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x2	gpio0b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio0b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio0b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio0b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio0b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x1	gpio0b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x1	gpio0b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio0b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

PMU_GRF_GPIO0C_P

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio0c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio0c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio0c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio0c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio0c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio0c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio0c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

PMU_GRF_GPIO0D_P

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	Reserved;
13:12	RW	0x2	gpio0d6_p 2'b00: Z(Normal operation); 2'b01: Reserved; 2'b10: Weak 0(pull-down); 2'b11: Weak 1(pull-up);
11:10	RW	0x2	gpio0d5_p 2'b00: Z(Normal operation); 2'b01: Reserved; 2'b10: Weak 0(pull-down); 2'b11: Weak 1(pull-up);

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio0d4_p 2'b00: Z(Normal operation); 2'b01: Reserved; 2'b10: Weak 0(pull-down); 2'b11: Weak 1(pull-up);
7:6	RW	0x2	gpio0d3_p 2'b00: Z(Normal operation); 2'b01: Reserved; 2'b10: Weak 0(pull-down); 2'b11: Weak 1(pull-up);
5:4	RW	0x0	Reserved;
3:2	RW	0x1	gpio0d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio0d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

PMU_GRF_GPIO0A_IE

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x3	gpio0a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x3	gpio0a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x3	gpio0a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

PMU_GRF_GPIO0B_IE

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x3	gpio0b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x3	gpio0b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x3	gpio0b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

PMU_GRF_GPIO0C_IE

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x3	gpio0c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x3	gpio0c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x3	gpio0c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

PMU_GRF_GPIO0D_IE

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RW	0xFFF	Reserved
3:2	RW	0x3	gpio0d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x3	gpio0d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

PMU_GRF_GPIO0A_OPD

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0B_OPD

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0b6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0b5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0b4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0b3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0b2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0b1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0b0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0C_OPD

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0c6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0c5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	gpio0c4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0c3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0c2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0c1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0c0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0D_OPD

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio0d1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0d0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0A_SUS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0B_SUS

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio0b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x1	gpio0b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0C_SUS

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x1	gpio0c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0D_SUS

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x00	reserved
1	RW	0x0	gpio0d1_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0d0_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

PMU_GRF_GPIO0A_SL

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio0a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio0a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
5:4	RW	0x3	gpio0a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

PMU_GRF_GPIO0B_SL

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio0b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
7:6	RW	0x3	gpio0b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio0b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

PMU_GRF_GPIO0C_SL

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
9:8	RW	0x3	gpio0c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio0c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio0c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

PMU_GRF_GPIO0D_SL

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RW	0xFFF	reserved
3:2	RW	0x3	gpio0d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

PMU_GRF_GPIO0A_DS_0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0A_DS_1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	gpio0a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0A_DS_2

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0A_DS_3

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x01	gpio0a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0B_DS_0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0B_DS_1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0B_DS_2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	gpio0b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0B_DS_3

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0C_DS_0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x01	gpio0c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0C_DS_1

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0C_DS_2

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0C_DS_3

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	gpio0c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_GPIO0D_DS_0

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio0d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio0d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

PMU_GRF_SOC_CON0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ddrphy_bufferen_core 1'b0: Enable ddrphy io retention; 1'b1: Disable ddrphy io retention;
12	RW	0x0	ddrphy_bufferen_sel 1'b0: Ddrphy_bufferen from pmu and ddr_fail_safe 1'b1: Ddrphy_bufferen from ddrphy_bufferen_core

Bit	Attr	Reset Value	Description
11:8	RO	0x0	reserved
7	RW	0x0	grf_con_pmic_sleep_sel pmic sleep function selection 1'b0: From reset pulse generator, can reset external PMIC 1'b1: From pmu block, only suppport sleep function for external PMIC
6	RW	0x0	uart0_cts_sel uart0_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
5	RW	0x0	uart0_rts_sel uart0_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
4	RO	0x0	reserved
3	RW	0x0	dpll_osc_source_sel DPLL osc input source select 1'b0: from more clock buffer path 1'b1: from less clock buffer path
2	RW	0x0	apll_osc_source_sel APLL osc input source select 1'b0: from more clock buffer path 1'b1: from less clock buffer path
1	RW	0x0	i2c0_iomux_sel i2c0 IO controller select 1'b0: from acdcdig 1'b1: from i2c0 controller
0	RW	0x0	con_32k_ioe 1'b0: Output mode 1'b1: Input mode;

PMU_GRF_SOC_CON1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	resetn_hold Please refer to pmucru_softrst_con0. Each bit has a hold

PMU_GRF_SOC_CON2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	reserved
7:0	RW	0x00	resetn_hold Please refer to pmucru_s_softrst_con0[7:0]. Each bit has a hold

PMU_GRF_SOC_CON3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	dsu_pactive_en cpudsupactive enable
14	RW	0x0	dsu_ret_en cpudsu retention enable
13	RW	0x0	dsu_off_en cpudsu power off en
12	RW	0x0	core_pactive_en cpu core pactive enable
11	RW	0x0	core_ret_en cpu core retention enable
10	RW	0x0	core_off_en cpu core power off en
9	RW	0x1	core_wfi_en CPU core wif enable
8	RW	0x0	upctl_c_sysreq_cfg 1'b0: After ddr failsafe module enters self-refresh status, then request DDR controller to enter low power state 1'b1: Always enable requesting DDR controller to enter low power state, when ddr failsafe module is working
7	RW	0x0	ddr_io_ret_oen_cfg ddr_io_ret_oen_cfg bit control 1'b0: ddr_io_ret output enable 1'b1: ddr_io_ret_output disable
6	RW	0x0	ddr_io_ret_cfg 1'b0: DDR io retention managed by hardware automatically; 1'b1: Enable ddr io retention manually
5	RW	0x0	ddr_io_ret_de_req Request to enter retention, during system failure 1'b0: Disable 1'b1: Enable
4	RW	0x1	ddrc_gating_en 1'b0: Disable ddr clock gating during system failure 1'b1: Enable ddr clock gating during system failure
3	RW	0x1	sref_enter_en 1'b0: Disable ddr self-refresh enter when system is failed 1'b1: Enable ddr self-refresh enter when system is failed
2	RW	0x1	ddrio_ret_en 1'b0: Remain ddr io status when system is failed 1'b1: Enable ddr io retension when system is failed
1	RW	0x0	wdt_shut_reset_trigger_en Enable failsafe wdt input 1'b0: Disable; 1'b1: Enable;
0	RW	0x0	tsadc_shut_reset_trigger_en Enable failsafe tsadc input 1'b0: Disable; 1'b1: Enable;

PMU_GRF_SOC_CON4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	spra_hd_rtsel Timing adjustment setting for debug purpose
13:12	RW	0x0	spra_hd_wtsel Timing adjustment setting for debug purpose
11:10	RW	0x0	gpu_pwren_pol gpu power control polariy control 1'b0: high power down asserted 1'b1: low power down asserted
9:6	RO	0x0	reserved
5:4	RW	0x1	pwm2_iomux_sel PWM2 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10: Reserved 2'b11: Reserved
3:2	RW	0x2	pwm1_iomux_sel PWM1 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10: Reserved 2'b11: Reserved
1:0	RW	0x3	pwm0_iomux_sel PWM0 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10: Reserved 2'b11: Reserved

PMU_GRF_SOC_CON5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:0	RW	0x081b	out2chip_rst_init out2chip rst counter initial value

PMU_GRF_SOC_STATUS

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RO	0x0	wfi status a55 standbywfi

PMU_GRF_IO_VSEL0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	poc_vccio7_sel25 VCCIO7 2.5V control 1'b0: Disable 1'b1: Enable
13	RW	0x0	poc_vccio6_sel25 VCCIO6 2.5V control 1'b0: Disable 1'b1: Enable
12	RW	0x0	poc_vccio5_sel25 VCCIO5 2.5V control 1'b0: Disable 1'b1: Enable
11	RW	0x0	poc_vccio4_sel25 VCCIO4 2.5V control 1'b0: Disable 1'b1: Enable
10	RW	0x0	poc_vccio3_sel25 VCCIO3 2.5V control 1'b0: Disable 1'b1: Enable
9	RW	0x0	poc_vccio2_sel25 VCCIO2 2.5V control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio1_sel25 VCCIO1 .25V control 1'b0: Disable 1'b1: Enable
7	RW	0x0	poc_vccio7_sel18 VCCIO7 1.8V control 1'b0: Disable 1'b1: Enable
6	RW	0x0	poc_vccio6_sel18 VCCIO6 1.8V control 1'b0: Disable 1'b1: Enable
5	RW	0x0	poc_vccio5_sel18 VCCIO5 1.8V control 1'b0: Disable 1'b1: Enable
4	RW	0x0	poc_vccio4_sel18 VCCIO4 1.8V control 1'b0: Disable 1'b1: Enable
3	RW	0x0	poc_vccio3_sel18 VCCIO3 1.8V control 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	poc_vccio2_sel18 VCCIO2 1.8V control 1'b0: Disable 1'b1: Enable
1	RW	0x0	poc_vccio1_sel18 VCCIO1 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	vccio2 voltage control select VCCIO2 voltage control selection 1'b0: from GPIO_0A7 1'b1: from GRF

PMU_GRF_IO_VSEL1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	poc_vccio7_iddq VCCIO7 iddq control 1'b0: Disable 1'b1: Enable
13	RW	0x0	poc_vccio6_iddq VCCIO6 iddq control 1'b0: Disable 1'b1: Enable
12	RW	0x0	poc_vccio5_iddq VCCIO5 iddq control 1'b0: Disable 1'b1: Enable
11	RW	0x0	poc_vccio4_iddq VCCIO4 iddq control 1'b0: Disable 1'b1: Enable
10	RW	0x0	poc_vccio3_iddq VCCIO3 iddq control 1'b0: Disable 1'b1: Enable
9	RW	0x0	poc_vccio2_iddq VCCIO2 iddq control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio1_iddq VCCIO1 iddq control 1'b0: Disable 1'b1: Enable
7	RW	0x1	poc_vccio7_sel33 VCCIO7 3.3V control 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x1	poc_vccio6_sel33 VCCIO6 3.3V control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_vccio5_sel33 VCCIO5 3.3V control 1'b0: Disable 1'b1: Enable
4	RW	0x1	poc_vccio4_sel33 VCCIO4 3.3V control 1'b0: Disable 1'b1: Enable
3	RW	0x1	poc_vccio3_sel33 VCCIO3 3.3V control 1'b0: Disable 1'b1: Enable
2	RW	0x1	poc_vccio2_sel33 VCCIO2 3.3V control 1'b0: Disable 1'b1: Enable
1	RW	0x1	poc_vccio1_sel33 VCCIO1 3.3V control 1'b0: Disable 1'b1: Enable
0	RO	0x1	reserved

PMU_GRF_IO_VSEL2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	poc_pmuio2_iddq PMUIO2 iddq control 1'b0: Disable 1'b1: Enable
6	RW	0x0	poc_pmuio1_iddq PMUIO1 iddq control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_pmuio2_sel33 PMUIO2 3.3V control 1'b0: Disable 1'b1: Enable
4	RW	0x1	reserved
3	RW	0x0	poc_pmuio2_sel25 PMUIO2 2.5V control 1'b0: Disable 1'b1: Enable
2	RW	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	poc_pmuio2_sel18 PMUIO2 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	reserved

PMU_GRF_DLL_CON0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x003	pvtm_clkout_div pvtmclkout divider value

PMU_GRF_OS_REG0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg0 OS register

PMU_GRF_OS_REG1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg1 OS register

PMU_GRF_OS_REG2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg2 OS register

PMU_GRF_OS_REG3

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg3 OS register

PMU_GRF_OS_REG4

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg4 OS register

PMU_GRF_OS_REG5

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg5 OS register

PMU_GRF_OS_REG6

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg6 OS register

PMU_GRF_OS_REG7

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg7 OS register

PMU_GRF_OS_REG8

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg8 OS register

PMU_GRF_OS_REG9

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg9 OS register

PMU_GRF_OS_REG10

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg10 OS register

PMU_GRF_OS_REG11

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg11 OS register

PMU_GRF_RESET_FUNCTION_STATUS

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ddr_fail_safe_src ddr_fail_safe is active
2	RW	0x0	tsadc_shut_reset_src Reset by tsadc shut trigger
1	RW	0x0	wdt_reset_src Reset by wdt trigger
0	RW	0x0	first_reset_src Reset by first reset trigger

PMU_GRF_RESET_FUNCTION_CLR

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	ddr_fail_safe_src_clr Clear bit for ddr_fail_safe is active 1'b1: Clear enable 1'b0: Clear disable
2	RW	0x0	tsadc_shut_reset_src_clr Clear bit for reset by tsadc shut trigger 1'b1: Clear enable 1'b0: Clear disable
1	RW	0x0	wdt_reset_src_clr Clear bit for reset by wdt trigger 1'b1: Clear enable 1'b0: Clear disable
0	RW	0x0	first_reset_src_clr Clear bit for reset by first reset trigger 1'b1: Clear enable 1'b0: Clear disable

PMU_GRF_SIG_DETECT_CON

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	sdmmc2_detectn_neg_irq_msk Enable sdmmcdetectnnegedgeirq 1'b0: Disable 1'b1: Enable
4	RW	0x0	sdmmc2_detectn_pos_irq_msk Enable sdmmcdetectnposedgeirq 1'b0: Disable 1'b1: Enable
3	RW	0x0	sdmmc1_detectn_neg_irq_msk Enable sdmmcdetectnnegedgeirq 1'b0: Disable 1'b1: Enable
2	RW	0x0	sdmmc1_detectn_pos_irq_msk Enable sdmmcdetectnposedgeirq 1'b0: Disable 1'b1: Enable
1	RW	0x0	sdmmc0_detectn_neg_irq_msk Enable sdmmcdetectnnegedgeirq 1'b0: Disable 1'b1: Enable
0	RW	0x0	sdmmc0_detectn_pos_irq_msk Enable sdmmcdetectnposedgeirq 1'b0: Disable 1'b1: Enable

PMU_GRF_SIG_DETECT_STATUS

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	sdmmc2_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
4	RW	0x0	sdmmc2_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq
3	RW	0x0	sdmmc1_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
2	RW	0x0	sdmmc1_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq
1	RW	0x0	sdmmc0_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
0	RW	0x0	sdmmc0_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq

PMU_GRF_SIG_DETECT_STATUS_CLEAR

Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sdmmc2_detectn_neg_irq_clr 1'b1: Clear irq
4	RW	0x0	sdmmc2_detectn_pos_irq_clr 1'b1: Clear irq
3	RW	0x0	sdmmc1_detectn_neg_irq_clr 1'b1: Clear irq
2	RW	0x0	sdmmc1_detectn_pos_irq_clr 1'b1: Clear irq
1	RW	0x0	sdmmc0_detectn_neg_irq_clr 1'b1: Clear irq
0	RW	0x0	sdmmc0_detectn_pos_irq_clr 1'b1: Clear irq

PMU_GRF_SDMMC_DET_COUNTER

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x003e8	sdmmc_detectn_count sdmmc_detectn_count bit register

3.4 CPU_GRF Register Description

3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_CPU_COREPVTPLL_CON0	0x0010	W	0x00000000	CORE PVTPLL control register0
GRF_CPU_COREPVTPLL_CON1	0x0014	W	0x00000000	CORE PVTPLL control register1
GRF_CPU_COREPVTPLL_CON2	0x0018	W	0x00000000	CORE PVTPLL control register0

Name	Offset	Size	Reset Value	Description
GRF_CPU_COREPVTPLL_CON3	0x001C	W	0x00000000	CORE PVTPLL control register3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.2 Detail Registers Description

GRF_CPU_COREPVTPLL_CON0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:11	RW	0x0	core_pvtpll_clk_div_cnt core pvtpll clock out divided nuber
10	RO	0x0	reserved
9:8	RW	0x0	core_pvtpll_osc_sel osc_ring selection. 2'b00: osc_ring 0 2'b01: osc_ring 1 2'b10: osc_ring 2 2'b11: osc_ring 3
7:3	RW	0x00	core_pvtpll_ring_length_sel core pvtpll delay cell element number control 5'b00000: 10 5'b00001: 20 5'b00010: 30 5'b00011: 40 5'b00100: 50 5'b00101: 60 5'b00110: 70 5'b00111: 80 ... 5'b11111:320
2	RW	0x0	core_pvtpll_out_polar PVTPLL output polarity
1	RW	0x0	core_pvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	core_pvtpll_start Set high to start PVTPLL

GRF_CPU_COREPVTPLL_CON1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	core_pvtpll_cal_cnt pvtpll calculation counter

GRF_CPU_COREPVTPLL_CON2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	core_pvtpll_threshold Set high to start PVTPLL

GRF_CPU_COREPVTPLL_CON3

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	core_pvtpll_ref_cnt Reference clock frequency counter value.

3.5 DDR_GRF Register Description

3.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR_GRF_CON0	0x0000	W	0x00000000	DDR Control Register0
DDR_GRF_CON1	0x0004	W	0x00000600	DDR Control Register1
DDR_GRF_CON2	0x0008	W	0x0000FBFF	DDR Control Register2
DDR_GRF_CON3	0x000C	W	0x0000E410	DDR Control Register3
DDR_GRF_CON4	0x0010	W	0x00000000	DDR Control Register4
DDR_GRF_SPLIT_CON	0x0014	W	0x00000110	DDR AXI SPLIT Control Register
DDR_GRF_LP_CON	0x0020	W	0x00001101	DDR PHY Lower Power Control Register
DDR_GRF_STATUS0	0x0100	W	0x00000000	DDR Status Register0
DDR_GRF_STATUS1	0x0104	W	0x00000000	DDR Status Register1
DDR_GRF_STATUS2	0x0108	W	0x00000000	DDR Status Register2
DDR_GRF_STATUS3	0x010C	W	0x00000000	DDR Status Register3
DDR_GRF_STATUS4	0x0110	W	0x00000000	DDR Status Register4
DDR_GRF_STATUS5	0x0114	W	0x00000000	DDR Status Register5
DDR_GRF_STATUS6	0x0118	W	0x00000000	DDR Status Register6
DDR_GRF_STATUS7	0x011C	W	0x00000000	DDR Status Register7
DDR_GRF_STATUS8	0x0120	W	0x00000000	DDR Status Register8
DDR_GRF_STATUS9	0x0124	W	0x00000000	DDR Status Register9
DDR_GRF_STATUS10	0x0130	W	0x00000000	DDR Status Register10
DDR_GRF_STATUS11	0x0134	W	0x00000000	DDR Status Register11
DDR_GRF_STATUS12	0x0138	W	0x00000000	DDR Status Register12

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.5.2 Detail Registers Description

DDR_GRF_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	awpoison AXI write poison control
13	RW	0x0	awurgent AXI write urgent control
12	RW	0x0	arpoison AXI read poison control
11	RW	0x0	arurgent AXI bus read urgent control
10	RW	0x0	pa_wmask When asserted(active high), it will prevent the corresponding write to PA

Bit	Attr	Reset Value	Description
9:8	RW	0x0	pa_rmask When asserted(active high), it will prevent the corresponding read to PA
7	RW	0x0	arautopre AXI auto-precharge signal for read command.
6	RW	0x0	awautopre AXI auto-precharge signal for write command
5	RW	0x0	csysreq_upctl_ddrstdby 1'b0: Disable stdby controls upctlcsysreq_ddrc 1'b1: Enable stdby control upctlcsysreq_ddrc
4	RO	0x0	reserved
3	RW	0x0	csysreq_aclk 1'b0: Request upctlaclk enter low power 1'b1: Request upctlaclk exit low power
2	RW	0x0	dfi_init_start dfi_init start value
1	RW	0x0	dfi_init_start_sel 1'b0: Upctl controls dfi_init_start 1'b1: Grf_dfi_init_start controls dfi_init_start
0	RW	0x0	upctl_slverr_enable 1'b0: Disable upctlapbslverr response 1'b1: Enable upcttlapbslverr response

DDR_GRF_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x6	ddrc_auto_sr_dly The delay of auto gated ddrc_core_clk. It should be to be 0x6
7:6	RO	0x0	reserved
5	RW	0x0	upctl2_pdsrlp_cg_en DDR clock gating control after enter PD/SR state 1'b0: Enable clock gating 1'b1: Disable clock gating
4	RW	0x0	upctl2_syscreq_cg_en 1'b0: Disable force ddrc_core_clkungating when external ddrc_csysreq asserted 1'b1: Enable force ddrc_coreungating when external ddrc_csysreq asserted
3	RW	0x0	selfref_type2_en 1'b0: Disable ddrc_core_clk auto gating in type2 selfrefresh 1'b1: Enable ddrc_core_clk auto gating in type2 selfrefresh
2	RW	0x0	upctl_core_cg_en 1'b0: Disable ddrc_core_clk auto gating 1'b1: Enable ddrc_core_clk auto gating
1	RW	0x0	upctl_apb_cg_en 1'b0: Disable function of force aclk/ddrc_core_clk ungated when apb access is going 1'b1: Enable function of force aclk/ddrc_core_clk ungated when apb access is going

Bit	Attr	Reset Value	Description
0	RW	0x0	upctl_axi_cg_en 1'b0: Disable aclk auto gating 1'b1: Enable aclk auto gating

DDR_GRF_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	ddrc_lpi_cg_en 1'b0 enable ddrc LPI auto gating function 1'b1 disable ddrc LPI auto gating function
14:11	RW	0xf	dfi_phymstr_cs_state DFI PHY Master CS State: Indicates the state of the DRAM when the PHY becomes the master: 1'b0: The PHY specifies the required state, using the dfi_phymstr_state_sel signal 1'b1: The PHY does not specify the state Each memory rank uses one bit.
10	RO	0x0	reserved
9:0	RW	0x3ff	ddr_clk_gate each bit is dedicated for a subblock auto gating function inside ddr control 1'b0 enable auto gating 1'b1 disable auto gating

DDR_GRF_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	dq_swap_sel3 select which dfidq byte is used for dq byte 0 in IO 2'b00 dfidq byte 0 is used for byte3 2'b01 dfidq byte 1 is used for byte3 2'b10 dfidq byte 2 is used for byte3 2'b11 dfidq byte 3 is used for byte3
13:12	RW	0x2	dq_swap_sel2 select which dfidq byte is used for dq byte 0 in IO 2'b00 dfidq byte 0 is used for byte2 2'b01 dfidq byte 1 is used for byte2 2'b10 dfidq byte 2 is used for byte2 2'b11 dfidq byte 3 is used for byte2
11:10	RW	0x1	dq_swap_sel1 select which dfidq byte is used for dq byte 0 in IO 2'b00 dfidq byte 0 is used for byte1 2'b01 dfidq byte 1 is used for byte1 2'b10 dfidq byte 2 is used for byte1 2'b11 dfidq byte 3 is used for byte1

Bit	Attr	Reset Value	Description
9:8	RW	0x0	dq_swap_sel0 select which dfidq byte is used for dq byte 0 in IO 2'b00 dfidq byte 0 is used for byte0 2'b01 dfidq byte 1 is used for byte0 2'b10 dfidq byte 2 is used for byte0 2'b11 dfidq byte 3 is used for byte0
7	RW	0x0	dq_swap_en ddrdfidq swap enable 1'b1 enable 1'b0 disalbe
6:5	RW	0x0	csysreq_ddrc_sel csysreq_ddrc source select 2'b00: grf_con_csysreq_ddrc 2'b01: csysreq_upctl_pmu 2'b10: csysreq_ddrc_autogate 2'b11: hwffc_csysreq_ddrc
4	RW	0x1	csysreq_ddrc DDRC Hardware Low-Power Request. Request from the system clock controller for the peripheral (DDRC) to enter a low-power state.
3:2	RW	0x0	dfi_phymstr_type DFI PHY Master Type: Indicates which of the 4 types of PHY master interface times the dfi_phymstr_req signal is requesting: 2'b00: tphymstr_type0 2'b01: tphymstr_type1 2'b10: tphymstr_type2 2'b11: tphymstr_type3
1	RW	0x0	dfi_phymstr_state_sel DFI PHY Master State Select: Indicates the state requested by the PHY: 1'b0: IDLE 1'b1: Self-Refresh
0	RO	0x0	reserved

DDR_GRF_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	silent_threshold silent threshold for how many idle cycles before LPI machin send request to DDRC

DDR_GRF_SPLIT_CON

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

Bit	Attr	Reset Value	Description
10:9	RW	0x0	SPMODE Split mode select. 2'b00:DDR controller and phy works at 32 bits mode. Low 16 bits are valid if access address is above split address. 2'b01:DDR controller and phy works at 32 bits mode. High 16 bits are valid if access address is above split address. 2'b10:DDR controller and phy works at 16 bits mode. Low 8 bits are valid if access address is above split address. 2'b11:DDR controller and phy works at 16 bits mode. High 8 bits are valid if access address is above split address
8	RW	0x1	BYPASS 1'b0: Enable axi split 1'b1: Bypass axi split
7:0	RW	0x10	SPADDR Split address high 8 bits of 32bit address. For example, if SPADDR=0x10, then the split address is 0x10000000. The axi_split module will be bypassed if reading or writing DDR below split address, otherwise axi burst will be split

DDR_GRF_LP_CON

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sr_ctl_en 1'b0: Disable sr exit/enter reload/inverse lpckdis_ini 1'b1: Enable sr exit/eneter reload/inverse lpckdis_ini
12	RW	0x1	pd_ctl_en 1'b0: Disable pd exit/enter reload/inverse lpckdis_ini 1'b1: Enable pd exit/eneter reload/inverse lpckdis_ini
11:10	RO	0x0	reserved
9	RW	0x0	lpckdis_en 1'b0: Disable ddrphy low power fuction 1'b1: Enable ddrphy low power function
8	RW	0x1	lpckdis_ini lpckdisintial value
7:3	RO	0x00	reserved
2	RW	0x0	lp23_mode 1'b0: Disable LPDDR2/LPDDR3 mode 1'b1: Enable LPDDR2/LPDDR3 mode
1	RO	0x0	reserved
0	RW	0x1	ddr23_mode 1'b0: Disable DDR2/DDR3 mode 1'b1: Enable DDR2/DDR3 mode

DDR_GRF_STATUS0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[31:0] DDR_STATUS0~DDR_STATUS7 are Mode Register Read Data. mrr_data0[31:0] data status.

DDR_GRF_STATUS1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[63:32] mrr_data0[63:32] data status. See DDR_STATUS0

DDR_GRF_STATUS2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[95:64] mrr_data0[95:64] data status. See DDR_STATUS0

DDR_GRF_STATUS3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[127:96] mrr_data0[127:96] data status. See DDR_STATUS0

DDR_GRF_STATUS4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[159:128] mrr_data0[159:128] data status. See DDR_STATUS0

DDR_GRF_STATUS5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[31:0] mrr_data1[31:0] data status. See DDR_STATUS0

DDR_GRF_STATUS6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[63:32] mrr_data1[63:32] data status. See DDR_STATUS0

DDR_GRF_STATUS7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[95:64] mrr_data1[95:64] data status. See DDR_STATUS0

DDR_GRF_STATUS8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	dfi_scramble_shift_ready The status of dfi_scramble_shift_ready
7:6	RO	0x0	ddrc_reg_selfref_type The status of ddrc_reg_selfref_type
5	RO	0x0	cactive_aclk The status of cactive_aclk
4	RO	0x0	csysaclk_aclk The status of csysaclk_aclk

Bit	Attr	Reset Value	Description
3	RO	0x0	con_csysreq_aclk The status of con_csysreq_aclk
2	RO	0x0	cactive_ddrc The status of external cactive_ddrc
1	RO	0x0	csysack_ddrc The status of external csysack_ddrc
0	RO	0x0	csysreq_ddrc The status of external csysreq_ddrc

DDR_GRF_STATUS9

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	dfi_lp_ck_disable The status of low power of ddrphy
30:23	RO	0x00	reserved
22:16	RO	0x00	wr_credit_cnt Indicates the number of available write CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the write CAM.
15	RO	0x0	reserved
14:8	RO	0x00	hpr_credit_cnt Indicates the number of available High priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (HPR store).
7	RO	0x0	reserved
6:0	RO	0x00	lpr_credit_cnt Indicates the number of available Low priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (LPR store).

DDR_GRF_STATUS10

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[127:96] mrr_data1[127:96] data status. See DDR_STATUS0

DDR_GRF_STATUS11

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[159:128] mrr_data1[159:128] data status. See DDR_STATUS0

DDR_GRF_STATUS12

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
18:7	RO	0x000	hif_refresh_req_bank Indicates the next bank that is refreshed; for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal.
6:0	RO	0x00	wrecc_credit_cnt Indicates the number of available write ECC CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the write ECC CAM

3.6 PIPE_GRF Register Description

3.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PIPE_GRF_PIPE_CON0	0x0000	W	0x00008D80	PIPE control register0
PIPE_GRF_SATA_CON0	0x0010	W	0x00000200	SATA control register0
PIPE_GRF_SATA_CON1	0x0014	W	0x00000200	SATA control register1
PIPE_GRF_SATA_CON2	0x0018	W	0x00000200	SATA control register0
PIPE_GRF_XPCS_CON0	0x0040	W	0x00000200	XPCS control register0
PIPE_GRF_XPCS_STATUS0	0x0080	W	0x00000000	XPCS status register
PIPE_GRF_USB3OTG0_CON0	0x0100	W	0x00002000	usb3otg0 control register0
PIPE_GRF_USB3OTG0_CON1	0x0104	W	0x00001100	usb3otg0 control register1
PIPE_GRF_USB3OTG0_CON2	0x0108	W	0x00000000	usb3otg0 control register2
PIPE_GRF_USB3OTG0_STATUS_LAT0	0x0110	W	0x00000000	usb3otg0 status_lat0 register
PIPE_GRF_USB3OTG0_STATUS_LAT1	0x0114	W	0x00000000	usb3otg0 status_lat1 register
PIPE_GRF_USB3OTG0_STATUS_CB	0x0118	W	0x00000000	usb3otg0 status_cb register
PIPE_GRF_USB3OTG0_STATUS	0x011C	W	0x00000000	usb3otg0 status register
PIPE_GRF_USB3OTG1_CON0	0x0140	W	0x00002000	usb3otg1 control register0
PIPE_GRF_USB3OTG1_CON1	0x0144	W	0x00001100	usb3otg1 control register1
PIPE_GRF_USB3OTG1_CON2	0x0148	W	0x00000000	usb3otg1 control register2
PIPE_GRF_USB3OTG1_STATUS_LAT0	0x0150	W	0x00000000	usb3otg1 status_lat0 register
PIPE_GRF_USB3OTG1_STATUS_LAT1	0x0154	W	0x00000000	usb3otg1 status_lat1 register
PIPE_GRF_USB3OTG1_STATUS_CB	0x0158	W	0x00000000	usb3otg1 status_cb register
PIPE_GRF_USB3OTG1_STATUS	0x0160	W	0x00000000	usb3otg1 status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.6.2 Detail Registers Description

PIPE_GRF_PIPE_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x1	sata2_pclkreq_n sata2_pclkreq_n input port control
14	RW	0x0	sata2_phy_rx_err sata2 phy_rx_err input control
13:12	RW	0x0	sata2_phy_spdmode sata2 phy_spdmode input control 2'b00: 1.5Gb/s 2'b01: 3.0Gb/s 2'b10: 6.0Gb/s 2'b11: Reserved
11	RW	0x1	sata1_pclkreq_n sata1_pclkreq_n input port control
10	RW	0x1	sata1_phy_rx_err sata1 phy_rx_err input control
9:8	RW	0x1	sata1_phy_spdmode sata1 phy_spdmode input control 2'b00: 1.5Gb/s 2'b01: 3.0Gb/s 2'b10: 6.0Gb/s 2'b11: Reserved
7	RW	0x1	sata0_pclkreq_n sata0_pclkreq_n input port control
6	RW	0x0	sata0_phy_rx_err sata0 phy_rx_err input control
5:4	RW	0x0	sata0_phy_spdmode sata0 phy_spdmode input control, 2'b00: 1.5Gb/s 2'b01: 3.0Gb/s 2'b10: 6.0Gb/s 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	pcie30x2_link_rst_grt PCIe30x2 link rest grant control
1	RW	0x0	pcie30x1_link_rst_grt PCIe30x1 link rest grant control
0	RW	0x0	pcie20_link_rst_grt PCIe20 link rest grant control

PIPE_GRF_SATA_CON0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x0	sata0_txcommonmode_disable TX common mode disable

Bit	Attr	Reset Value	Description
14	RW	0x0	sata0_rxelecidle_disable TX output to electrical idle disable
13:11	RW	0x0	sata0_txmargin TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude
10:9	RW	0x1	sata0_txdeemph Transmitter de-emphasis level configuration
8	RW	0x0	sata0_txswing phy TX_SWING control When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV,the 800mV to 1200mV output has no difference with the cases when TX_SWING =0.
7	RW	0x0	sata0_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. In PCIE and SATA mode, this signal should be tied to low
6	RW	0x0	sata0_compliance This signal is used in PCIE mode only; in other application it should be tied to low. TX_COMPLIANCE become high will set the running disparity to negative. The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative. When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. Refer to PIPE spec for detail description
5	RW	0x0	sata0_rxtermination Connect/Remove of receiver termination resistor. 0 C RX termination removed 1 C RX termination connected This signal is used in USB3.0 mode only, in other application it should be tied to high
4	RW	0x0	sata0_rxpolarity PHY RX polarity inversion control When this signal set to high, it instructs a polarity inversion in RX_DATA. RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low
3	RW	0x0	sata0_rxeqtrain RX EQ training mode enable signal: This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application.

Bit	Attr	Reset Value	Description
2	RW	0x0	sata0_l1sub_entreq L1 sub-state entry request. When set to high, it instructs PHY to do power transition to L1 This signal is used in PCIE mode only, in other application it should be tied to low This signal could connected to the L1 sub-state enable/request signal from controller
1	RW	0x0	sata0_encodedecodebypass Controls whether the PHY performs 8b/10b encode and decode. 1'b0 : 8b/10b encode/decode performed normally by the PHY. 1'b1 : 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01
0	RW	0x0	sata0_elasbuffermode 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode

PIPE_GRF_SATA_CON1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x0	sata1_txcommonmode_disable TX common mode disable
14	RW	0x0	sata1_rxelecidle_disable TX output to electrical idle disable
13:11	RW	0x0	sata1_txmargin TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude
10:9	RW	0x1	sata1_txdeemph Transmitter de-emphasis level configuration
8	RW	0x0	sata1_txswing phy TX_SWING control When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV,the 800mV to 1200mV output has no difference with the cases when TX_SWING =0.
7	RW	0x0	sata1_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. In PCIE and SATA mode, this signal should be tied to low

Bit	Attr	Reset Value	Description
6	RW	0x0	sata1_compliance This signal is used in PCIE mode only; in other application it should be tied to low. TX_COMPLIANCE become high will set the running disparity to negative. The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative. When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. Refer to PIPE spec for detail description
5	RW	0x0	sata1_rxtermination Connect/Remove of receiver termination resistor. 0 C RX termination removed 1 C RX termination connected This signal is used in USB3.0 mode only, in other application it should be tied to high
4	RW	0x0	sata1_rxpolarity PHY RX polarity inversion control When this signal set to high, it instructs a polarity inversion in RX_DATA. RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low
3	RW	0x0	sata1_rxeqtrain RX EQ training mode enable signal: This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application.
2	RW	0x0	sata1_l1sub_entreq L1 sub-state entry request. When set to high, it instructs PHY to do power transition to L1 This signal is used in PCIE mode only, in other application it should be tied to low This signal could connected to the L1 sub-state enable/request signal from controller
1	RW	0x0	sata1_encodedecodebypass Controls whether the PHY performs 8b/10b encode and decode. 1'b0 : 8b/10b encode/decode performed normally by the PHY. 1'b1 : 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01
0	RW	0x0	sata1_elasbuffermode 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode

PIPE_GRF_SATA_CON2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x0	sata2_txcommonmode_disable TX common mode disable

Bit	Attr	Reset Value	Description
14	RW	0x0	sata2_rxelecidle_disable TX output to electrical idle disable
13:11	RW	0x0	sata2_txmargin TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude
10:9	RW	0x1	sata2_txdeemph Transmitter de-emphasis level configuration
8	RW	0x0	sata2_txswing phy TX_SWING control When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV,the 800mV to 1200mV output has no difference with the cases when TX_SWING =0.
7	RW	0x0	sata2_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. In PCIE and SATA mode, this signal should be tied to low
6	RW	0x0	sata2_compliance This signal is used in PCIE mode only; in other application it should be tied to low. TX_COMPLIANCE become high will set the running disparity to negative. The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative. When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. Refer to PIPE spec for detail description
5	RW	0x0	sata2_rxtermination Connect/Remove of receiver termination resistor. 0 C RX termination removed 1 C RX termination connected This signal is used in USB3.0 mode only, in other application it should be tied to high
4	RW	0x0	sata2_rxpolarity PHY RX polarity inversion control When this signal set to high, it instructs a polarity inversion in RX_DATA. RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low
3	RW	0x0	sata2_rxeqtrain RX EQ training mode enable signal: This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application.

Bit	Attr	Reset Value	Description
2	RW	0x0	sata2_l1sub_entreq L1 sub-state entry request. When set to high, it instructs PHY to do power transition to L1 This signal is used in PCIE mode only, in other application it should be tied to low This signal could connected to the L1 sub-state enable/request signal from controller
1	RW	0x0	sata2_encodedecodebypass Controls whether the PHY performs 8b/10b encode and decode. 1'b0 : 8b/10b encode/decode performed normally by the PHY. 1'b1 : 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01
0	RW	0x0	sata2_elasbuffermode 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode

PIPE_GRF_XPCS_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	xpcs_mii1_rx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
8	RW	0x0	xpcs_mii0_rx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
7	RW	0x0	xpcs_qsgmii_rx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
6	RW	0x0	xpcs_xgxs_rx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
5	RW	0x0	xpcs_qsgmii_tx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
4	RW	0x0	xpcs_xgxs_tx_clk_gate_en auto-clock gating control 1'b0: Auto-clock gating disable 1'b1: Auto-clock agting enable
3	RO	0x0	reserved
2	RW	0x0	xpcs_phy_rdy_i Input indicating all clocks from PHY are stable
1	RW	0x0	sgmii_mac_sel 1'b0: gmac1 be selected to used as SGMII controller 1'b1: gmac0 be selected to used as SGMII controller

Bit	Attr	Reset Value	Description
0	RW	0x0	xpcs_los It indicates the loss of signal from the PCS-X PHY. 1'b0: Link restored. 1'b1: Receive side is unable to receive data, indicating loss of signal.

PIPE_GRF_XPCS_STATUS0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	xpcs_lpirx_quiet Receive Path in Quiet State. It is asserted when the EEE controller in Rx path is in the Quiet (power-save) state. When it is asserted, you can disable the Rx path of the PHY or the PMD.
28	RW	0x0	xpcs_lrx_active Receive Path in EEE Mode. It is asserted when the DWC_xpcs receives LPI Idle the Rx path. It is deactivated when it receives the normal Idle or Data. It provides an additional status to the PHY or the PMD.
27	RW	0x0	xpcs_lpitx_quite Transmit Path in Quiet State. It is asserted when the EEE controller in Tx path is in the Quiet (power-save) state. When it is asserted, you can disable the Tx data path of the PHY or the PMD. In addition, you can use this signal to stop the Transmit clocks to the DWC_xpcs and the PHY.
26	RW	0x0	xpcs_qsgmii3_full_duplex QSGMII full duplex of port3. It signal indicates the whether QSGMII supports full duplex or halfduplex
25	RW	0x0	xpcs_qsgmii3_link_sts QSGMII Link Status of port3
24	RW	0x0	xpcs_mii3_ctrl MII Data Width Control of port3. This signal controls the data width of the MII interface.This signal is applicable only if the MAC is working at 10 Mbps or 100Mbps speed. The following is the encoded data width: 1'b0: 4-bit MII 1'b1: 8-bit MII
23:22	RW	0x0	xpcs_link3_speed SGMII MAC Speed Control of port3. It indicates the current operating speed of the DWC_xpcs in the SGMII mode. This signal is used for selecting the frequency of the clk_mii_tx_i and clk_mii_rx_i signals. This signal is derived from the Speed Select bits (Bit 13 and Bit 6) of the SR MII MMD Control Register. The following is the encoded speed: 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps
21	RW	0x0	xpcs_qsgmii2_full_duplex QSGMII full duplex of port2. It signal indicates the whether QSGMII supports full duplex or halfduplex

Bit	Attr	Reset Value	Description
20	RW	0x0	xpcs_qsgmii2_link_sts QSGMII Link Status of port2
19	RW	0x0	xpcs_mii2_ctrl MII Data Width Control of port2. This signal controls the data width of the MII interface.This signal is applicable only if the MAC is working at 10 Mbps or 100Mbps speed. The following is the encoded data width: 1'b0: 4-bit MII 1'b1: 8-bit MII
18:17	RW	0x0	xpcs_link2_speed SGMII MAC Speed Control of Port2. It indicates the current operating speed of the DWC_xpcs in the SGMII mode. This signal is used for selecting the frequency of the clk_mii_tx_i and clk_mii_rx_i signals. This signal is derived from the Speed Select bits (Bit 13 and Bit 6) of the SR MII MMD Control Register. The following is the encoded speed: 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps
16	RW	0x0	xpcs_qsgmii1_full_duplex QSGMII full duplex. It signal indicates the whether QSGMII supports full duplex or halfduplex
15	RW	0x0	xpcs_qsgmii1_link_sts QSGMII Link Status
14	RW	0x0	xpcs_mii1_ctrl_p1 MII Data Width Control along Port1. This signal controls the data width of the MII interface when operating in 10Mbps/100Mbps.The following is the encoded data width: 1'b0: 4-bit MII 1'b1: 8-bit MII
13:12	RW	0x0	xpcs_link1_speed_p1 QSGMII MAC Speed Control along Port1. It indicates the current operating speed of the DWC_xpcs in the QSGMII mode. It is used for selecting the frequency of the clk_mii_tx_p1_i and clk_mii_rx_p1_i signals. It is derived from the Speed Select bits (Bit 13 and Bit 6) of the SR MII MMD P1 Control Register. The following is the encoded speed: 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps
11	RW	0x0	xpcs_sgmii0_full_duplex SGMII full duplex. It indicates the whether SGMII supports full duplex or halfduplex.
10	RW	0x0	xpcs_sgmii0_link_sts SGMII Link Status.
9	RW	0x0	xpcs_mii0_ctrl MII Data Width Control. This signal controls the data width of the MII interface.This signal is applicable only if the MAC is working at 10 Mbps or 100Mbps speed. The following is the encoded data width: 1'b0: 4-bit MII 1'b1: 8-bit MII

Bit	Attr	Reset Value	Description
8:7	RW	0x0	xpcs_link0_speed SGMII MAC Speed Control. It indicates the current operating speed of the DWC_xpcs in the SGMII mode. This signal is used for selecting the frequency of the clk_mii_tx_i and clk_mii_rx_i signals. This signal is derived from the Speed Select bits (Bit 13 and Bit 6) of the SR MII MMD Control Register. The following is the encoded speed: 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps
6	RW	0x0	xpcs_loopback_en_o Enable Loopback (Tx-to-Rx) in the PHY This signal indicates that software wants to enable loopback mode.
5	RW	0x0	xpcs_pdown_o Power-Down Enable. It indicates that the host programmed the device for the power-down mode.
4	RW	0x0	xpcs_qsgmii_mode QSGMII mode control output 1'b0: Not QSGMII mode 1'b1: QSGMII mode
3	RW	0x0	xpcs_2pt5g_mode 2.5G GMII Mode Control. This signal is used to switch between 1G and 2.5G GMII Modes. When this signal is set, it indicates that current mode of operation is 2.5G.This signal can be used for clock multiplexing to enable switching between 1G and 2.5G Modes.
2	RW	0x0	xpcs_link_status PCS Receive Link Status. This signal indicates whether the receive link of the PCS is up or down.
1	RW	0x0	xpcs_rx_en Enable Receive Data
0	RW	0x0	xpcs_tx_en_o Transmit Lane Enable or Disable Control Status. Values: 1'b0: Corresponding Transmit lane is disabled. 1'b1: Corresponding Transmit lane is enabled (default).

PIPE_GRF_USB3OTG0_CON0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3otg0_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state

Bit	Attr	Reset Value	Description
14	RW	0x0	usb3otg0_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches. 1'b1: Indicates that the port has port power switches
13:8	RW	0x20	usb3otg0_fladj_30mhz_reg usb3otg_fladj_30mhz_reg bit control
7:6	RW	0x0	usb3otg0_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port
5:4	RW	0x0	usb3otg0_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3otg0_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

PIPE_GRF_USB3OTG0_CON1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RW	0x1	usb3otg0_host_num_u3_port xHCI usb3 port number, default as 1
11:8	RW	0x1	usb3otg0_host_num_u2_port xHCI host USB2 Port number, default as 1
7	RW	0x0	usb3otg0_pipe_clk_sel usb3otg0_pipe3_rx_pclk/tx_pclk input source clk select 1'b0: select clk_usb3otg0_pipe for source clk 1'b0: select clk_usb3otg0_utmi for source clk
6	RO	0x0	reserved
5	RW	0x0	usb3otg0_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. SW must set this register, then clear this register to indicate Base Address Register written

Bit	Attr	Reset Value	Description
4	RW	0x0	usb3otg0_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. SW must set this register, then clear this register to indicate PCI command register written
3:2	RW	0x0	usb3otg0_pipe_rate 2'b00: Use 5.0GT/s signaling rate 2'b01: Not allowed 2'b10: Not allowed 2'b11: Not allowed
1	RW	0x0	usb3otg0_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation
0	RW	0x0	usb3otg0_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

PIPE_GRF_USB3OTG0_CON2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	usb3otg0_pme_generation_irq_en usb3otg0_pme_generation_irq_en 1'b0: irq disable 1'b1: irqenableable
0	RW	0x0	usb3otg0_host_sys_err_irq_en usb3otg0_host_sys_err_irq_en 1'b0: irq disable 1'b1: irqenableable

PIPE_GRF_USB3OTG0_STATUS_LAT0

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace0 usb3otg_logic_analyzer_trace[31:0] bit status

PIPE_GRF_USB3OTG0_STATUS_LAT1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace1 usb3otg_logic_analyzer_trace[63:32] bit status

PIPE_GRF_USB3OTG0_STATUS_CB

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	usb3otg_host_current_belt[11:0] usb3otg_host_current_belt[11:0] bit status

PIPE_GRF_USB3OTG0_STATUS

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	usb3otg0_pme_generation Used to generate the pme.
0	RO	0x0	usb3otg0_host_sys_err usb3otg0 host system error status

PIPE_GRF_USB3OTG1_CON0

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3otg1_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state
14	RW	0x0	usb3otg1_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches. 1'b1: Indicates that the port has port power switches
13:8	RW	0x20	usb3otg1_fladj_30mhz_reg usb3otg_fladj_30mhz_reg bit control
7:6	RW	0x0	usb3otg1_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port
5:4	RW	0x0	usb3otg1_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3otg1_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

PIPE_GRF_USB3OTG1_CON1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RW	0x1	usb3otg1_host_num_u3_port xHCI usb3 port number, default as 1
11:8	RW	0x1	usb3otg1_host_num_u2_port xHCI host USB2 Port number, default as 1
7	RW	0x0	usb3otg1_pipe_clk_sel usb3otg1_pipe3_rx_pclk/tx_pclk input source clk select 1'b0: select clk_usb3otg0_pipe for source clk 1'b0: select clk_usb3otg0_utmi for source clk
6	RO	0x0	reserved
5	RW	0x0	usb3otg1_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. SW must set this register, then clear this register to indicate Base Address Register written
4	RW	0x0	usb3otg1_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. SW must set this register, then clear this register to indicate PCI command register written
3:2	RW	0x0	usb3otg1_pipe_rate 2'b00: Use 5.0GT/s signaling rate 2'b01: Not allowed 2'b10: Not allowed 2'b11: Not allowed
1	RW	0x0	usb3otg1_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation
0	RW	0x0	usb3otg1_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

PIPE_GRF_USB3OTG1_CON2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	usb3otg1_pme_generation_irq_en usb3otg1_pme_generation_irq_en 1'b0: irq disable 1'b1: irqenableable
0	RW	0x0	usb3otg1_host_sys_err_irq_en usb3otg1_host_sys_err_irq_en 1'b0: irq disable 1'b1: irqenableable

PIPE_GRF_USB3OTG1_STATUS_LAT0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace0 usb3otg_logic_analyzer_trace[31:0] bit status

PIPE_GRF_USB3OTG1_STATUS_LAT1

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace1 usb3otg_logic_analyzer_trace[63:32] bit status

PIPE_GRF_USB3OTG1_STATUS_CB

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	usb3otg_host_current_belt[11:0] usb3otg_host_current_belt[11:0] bit status

PIPE_GRF_USB3OTG1_STATUS

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	usb3otg0_pme_generation Used to generate the pme.
0	RO	0x0	usb3otg0_host_sys_err usb3otg0 host system error status

3.7 SYS_GRF Register Description

3.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO1A_IOMUX_L	0x0000	W	0x00000000	GPIO1A IOMUX control low bits
GRF_GPIO1A_IOMUX_H	0x0004	W	0x00000000	GPIO1A IOMUX control high bits
GRF_GPIO1B_IOMUX_L	0x0008	W	0x00000000	GPIO1B IOMUX control low bits
GRF_GPIO1B_IOMUX_H	0x000C	W	0x00000000	GPIO1B IOMUX control high bits
GRF_GPIO1C_IOMUX_L	0x0010	W	0x00000000	GPIO1C IOMUX control low bits
GRF_GPIO1C_IOMUX_H	0x0014	W	0x00000000	GPIO1C IOMUX control high bits
GRF_GPIO1D_IOMUX_L	0x0018	W	0x00000000	GPIO1B IOMUX control low bits
GRF_GPIO1D_IOMUX_H	0x001C	W	0x00002000	GPIO1B IOMUX control high bits
GRF_GPIO2A_IOMUX_L	0x0020	W	0x00000002	GPIO2A IOMUX control low bits
GRF_GPIO2A_IOMUX_H	0x0024	W	0x00000000	GPIO2A IOMUX control high bits
GRF_GPIO2B_IOMUX_L	0x0028	W	0x00000000	GPIO2B IOMUX control low bits
GRF_GPIO2B_IOMUX_H	0x002C	W	0x00000000	GPIO2B IOMUX control high bits
GRF_GPIO2C_IOMUX_L	0x0030	W	0x00000000	GPIO2C IOMUX control low bits
GRF_GPIO2C_IOMUX_H	0x0034	W	0x00000000	GPIO2C IOMUX control high bits
GRF_GPIO2D_IOMUX_L	0x0038	W	0x00002000	GPIO2D IOMUX control low bits
GRF_GPIO2D_IOMUX_H	0x003C	W	0x00000222	GPIO2D IOMUX control low bits
GRF_GPIO3A_IOMUX_L	0x0040	W	0x00000000	GPIO3A IOMUX control low bits
GRF_GPIO3A_IOMUX_H	0x0044	W	0x00000000	GPIO3A IOMUX control high bits
GRF_GPIO3B_IOMUX_L	0x0048	W	0x00000000	GPIO3B IOMUX control low bits
GRF_GPIO3B_IOMUX_H	0x004C	W	0x00000000	GPIO3B IOMUX control high bits
GRF_GPIO3C_IOMUX_L	0x0050	W	0x00000000	GPIO3C IOMUX control low bits
GRF_GPIO3C_IOMUX_H	0x0054	W	0x00000000	GPIO3C IOMUX control high bits

Name	Offset	Size	Reset Value	Description
GRF_GPIO3D_IOMUX_L	0x0058	W	0x00000000	GPIO3D IOMUX control low bits
GRF_GPIO3D_IOMUX_H	0x005C	W	0x00000000	GPIO3D IOMUX control low bits
GRF_GPIO4A_IOMUX_L	0x0060	W	0x00000000	GPIO4A IOMUX control low bits
GRF_GPIO4A_IOMUX_H	0x0064	W	0x00000000	GPIO4A IOMUX control high bits
GRF_GPIO4B_IOMUX_L	0x0068	W	0x00000000	GPIO4B IOMUX control low bits
GRF_GPIO4B_IOMUX_H	0x006C	W	0x00000000	GPIO4B IOMUX control high bits
GRF_GPIO4C_IOMUX_L	0x0070	W	0x00000000	GPIO4C IOMUX control low bits
GRF_GPIO4C_IOMUX_H	0x0074	W	0x00000000	GPIO4C IOMUX control high bits
GRF_GPIO4D_IOMUX_L	0x0078	W	0x00000000	GPIO4C IOMUX control low bits
GRF_GPIO1A_P	0x0080	W	0x0000AAA5	GPIO1A PU/PD control
GRF_GPIO1B_P	0x0084	W	0x000055AA	GPIO1B PU/PD control
GRF_GPIO1C_P	0x0088	W	0x0000A955	GPIO1C PU/PD control
GRF_GPIO1D_P	0x008C	W	0x00005559	GPIO1D PU/PD control
GRF_GPIO2A_P	0x0090	W	0x0000AA65	GPIO2A PU/PD control
GRF_GPIO2B_P	0x0094	W	0x0000955A	GPIO2B PU/PD control
GRF_GPIO2C_P	0x0098	W	0x0000AAAA	GPIO2C PU/PD control
GRF_GPIO2D_P	0x009C	W	0x0000AAAA	GPIO2D PU/PD control
GRF_GPIO3A_P	0x00A0	W	0x0000AAAA	GPIO3A PU/PD control
GRF_GPIO3B_P	0x00A4	W	0x0000AAAA	GPIO3B PU/PD control
GRF_GPIO3C_P	0x00A8	W	0x0000AAAA	GPIO3C PU/PD control
GRF_GPIO3D_P	0x00AC	W	0x0000AAAA	GPIO3D PU/PD control
GRF_GPIO4A_P	0x00B0	W	0x0000AAAA	GPIO4A PU/PD control
GRF_GPIO4B_P	0x00B4	W	0x0000AAAA	GPIO4B PU/PD control
GRF_GPIO4C_P	0x00B8	W	0x00005AAA	GPIO4C PU/PD control
GRF_GPIO4D_P	0x00BC	W	0x00000159	GPIO4C PU/PD control
GRF_GPIO1A_IE	0x00C0	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO1B_IE	0x00C4	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO1C_IE	0x00C8	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO1D_IE	0x00CC	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO2A_IE	0x00D0	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO2B_IE	0x00D4	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO2C_IE	0x00D8	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO2D_IE	0x00DC	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO3A_IE	0x00E0	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO3B_IE	0x00E4	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO3C_IE	0x00E8	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO3D_IE	0x00EC	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO4A_IE	0x00F0	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO4B_IE	0x00F4	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO4C_IE	0x00F8	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO4D_IE	0x00FC	W	0x00000000	GPIO1A PAD input enable control
GRF_GPIO1A_OPD	0x0100	W	0x00000000	GPIO1A PAD open drain functionality enable
GRF_GPIO1B_OPD	0x0104	W	0x00000000	GPIO1B PAD open drain functionality enable
GRF_GPIO1C_OPD	0x0108	W	0x00000000	GPIO1C PAD open drain functionality enable
GRF_GPIO1D_OPD	0x010C	W	0x00000000	GPIO1D PAD open drain functionality enable
GRF_GPIO2A_OPD	0x0110	W	0x00000000	GPIO2A PAD open drain functionality enable

Name	Offset	Size	Reset Value	Description
GRF_GPIO2B_OPD	0x0114	W	0x00000000	GPIO2B PAD open drain functionality enable
GRF_GPIO2C_OPD	0x0118	W	0x00000000	GPIO2C PAD open drain functionality enable
GRF_GPIO2D_OPD	0x011C	W	0x00000000	GPIO2D PAD open drain functionality enable
GRF_GPIO3A_OPD	0x0120	W	0x00000000	GPIO3A PAD open drain functionality enable
GRF_GPIO3B_OPD	0x0124	W	0x00000000	GPIO3B PAD open drain functionality enable
GRF_GPIO3C_OPD	0x0128	W	0x00000000	GPIO3C PAD open drain functionality enable
GRF_GPIO3D_OPD	0x012C	W	0x00000000	GPIO3D PAD open drain functionality enable
GRF_GPIO4A_OPD	0x0130	W	0x00000000	GPIO4A PAD open drain functionality enable
GRF_GPIO4B_OPD	0x0134	W	0x00000000	GPIO4B PAD open drain functionality enable
GRF_GPIO4C_OPD	0x0138	W	0x00000000	GPIO3C PAD open drain functionality enable
GRF_GPIO4D_OPD	0x013C	W	0x00000000	GPIO4D PAD open drain functionality enable
GRF_GPIO1A_SUS	0x0140	W	0x00000000	GPIO1A PAD weak Pull Keeper enable
GRF_GPIO1B_SUS	0x0144	W	0x00000000	GPIO1B PAD weak Pull Keeper enable
GRF_GPIO1C_SUS	0x0148	W	0x00000000	GPIO1C PAD weak Pull Keeper enable
GRF_GPIO1D_SUS	0x014C	W	0x00000000	GPIO1D PAD weak Pull Keeper enable
GRF_GPIO2A_SUS	0x0150	W	0x00000000	GPIO2A PAD weak Pull Keeper enable
GRF_GPIO2B_SUS	0x0154	W	0x00000000	GPIO2B PAD weak Pull Keeper enable
GRF_GPIO2C_SUS	0x0158	W	0x00000000	GPIO2C PAD weak Pull Keeper enable
GRF_GPIO2D_SUS	0x015C	W	0x00000000	GPIO2D PAD weak Pull Keeper enable
GRF_GPIO3A_SUS	0x0160	W	0x00000000	GPIO3A PAD weak Pull Keeper enable
GRF_GPIO3B_SUS	0x0164	W	0x00000000	GPIO3B PAD weak Pull Keeper enable
GRF_GPIO3C_SUS	0x0168	W	0x00000000	GPIO3C PAD weak Pull Keeper enable
GRF_GPIO3D_SUS	0x016C	W	0x00000000	GPIO3D PAD weak Pull Keeper enable
GRF_GPIO4A_SUS	0x0170	W	0x00000000	GPIO4A PAD weak Pull Keeper enable
GRF_GPIO4B_SUS	0x0174	W	0x00000000	GPIO4B PAD weak Pull Keeper enable
GRF_GPIO4C_SUS	0x0178	W	0x00000000	GPIO3C PAD weak Pull Keeper enable

Name	Offset	Size	Reset Value	Description
GRF_GPIO4D_SUS	0x017C	W	0x00000000	GPIO4D PAD weak Pull Keeper enable
GRF_GPIO1A_SL	0x0180	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO1B_SL	0x0184	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO1C_SL	0x0188	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO1D_SL	0x018C	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO2A_SL	0x0190	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO2B_SL	0x0194	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO2C_SL	0x0198	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO2D_SL	0x019C	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO3A_SL	0x01A0	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO3B_SL	0x01A4	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO3C_SL	0x01A8	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO3D_SL	0x01AC	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO4A_SL	0x01B0	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO4B_SL	0x01B4	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO4C_SL	0x01B8	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO4D_SL	0x01BC	W	0x00000000	Slew Rate Control for the driver secton while driving PAD.
GRF_GPIO1A_DS_0	0x0200	W	0x00000101	GPIO1A driver strength control
GRF_GPIO1A_DS_1	0x0204	W	0x00000303	GPIO1A driver strength control
GRF_GPIO1A_DS_2	0x0208	W	0x00000303	GPIO1A driver strength control
GRF_GPIO1A_DS_3	0x020C	W	0x00000303	GPIO1A driver strength control
GRF_GPIO1B_DS_0	0x0210	W	0x00000303	GPIO1B driver strength control
GRF_GPIO1B_DS_1	0x0214	W	0x00000103	GPIO1B driver strength control
GRF_GPIO1B_DS_2	0x0218	W	0x00000F0F	GPIO1B driver strength control
GRF_GPIO1B_DS_3	0x021C	W	0x00000F0F	GPIO1B driver strength control
GRF_GPIO1C_DS_0	0x0220	W	0x00000F0F	GPIO1C driver strength control
GRF_GPIO1C_DS_1	0x0224	W	0x00000F0F	GPIO1C driver strength control
GRF_GPIO1C_DS_2	0x0228	W	0x00000F0F	GPIO1C driver strength control
GRF_GPIO1C_DS_3	0x022C	W	0x00000000	GPIO1C driver strength control
GRF_GPIO1D_DS_0	0x0230	W	0x0000010F	GPIO1D driver strength control
GRF_GPIO1D_DS_1	0x0234	W	0x0000010F	GPIO1D driver strength control
GRF_GPIO1D_DS_2	0x0238	W	0x0000010F	GPIO1D driver strength control
GRF_GPIO1D_DS_3	0x023C	W	0x0000010F	GPIO1D driver strength control
GRF_GPIO2A_DS_0	0x0240	W	0x00000F0F	GPIO2A driver strength control
GRF_GPIO2A_DS_1	0x0244	W	0x00000F0F	GPIO2A driver strength control
GRF_GPIO2A_DS_2	0x0248	W	0x00000F0F	GPIO2A driver strength control

Name	Offset	Size	Reset Value	Description
GRF_GPIO2A_DS_3	0x024C	W	0x00000F0F	GPIO2A driver strength control
GRF_GPIO2B_DS_0	0x0250	W	0x0000030F	GPIO2B driver strength control
GRF_GPIO2B_DS_1	0x0254	W	0x00000F03	GPIO2B driver strength control
GRF_GPIO2B_DS_2	0x0258	W	0x00000F0F	GPIO2B driver strength control
GRF_GPIO2B_DS_3	0x025C	W	0x00000303	GPIO2B driver strength control
GRF_GPIO2C_DS_0	0x0260	W	0x00000303	GPIO2C driver strength control
GRF_GPIO2C_DS_1	0x0264	W	0x00000303	GPIO2C driver strength control
GRF_GPIO2C_DS_2	0x0268	W	0x00000303	GPIO2C driver strength control
GRF_GPIO2C_DS_3	0x026C	W	0x00000303	GPIO2C driver strength control
GRF_GPIO2D_DS_0	0x0270	W	0x00000303	GPIO2D driver strength control
GRF_GPIO2D_DS_1	0x0274	W	0x00000303	GPIO2D driver strength control
GRF_GPIO2D_DS_2	0x0278	W	0x00000303	GPIO2D driver strength control
GRF_GPIO2D_DS_3	0x027C	W	0x00000303	GPIO2D driver strength control
GRF_GPIO3A_DS_0	0x0280	W	0x00000303	GPIO3A driver strength control
GRF_GPIO3A_DS_1	0x0284	W	0x00000303	GPIO3A driver strength control
GRF_GPIO3A_DS_2	0x0288	W	0x00000303	GPIO3A driver strength control
GRF_GPIO3A_DS_3	0x028C	W	0x00000303	GPIO3A driver strength control
GRF_GPIO3B_DS_0	0x0290	W	0x00000303	GPIO3B driver strength control
GRF_GPIO3B_DS_1	0x0294	W	0x00000303	GPIO3B driver strength control
GRF_GPIO3B_DS_2	0x0298	W	0x00000303	GPIO3B driver strength control
GRF_GPIO3B_DS_3	0x029C	W	0x00000303	GPIO3B driver strength control
GRF_GPIO3C_DS_0	0x02A0	W	0x00000003	GPIO3C driver strength control
GRF_GPIO3C_DS_1	0x02A4	W	0x00000303	GPIO3C driver strength control
GRF_GPIO3C_DS_2	0x02A8	W	0x00000303	GPIO3C driver strength control
GRF_GPIO3C_DS_3	0x02AC	W	0x00000303	GPIO3C driver strength control
GRF_GPIO3D_DS_0	0x02B0	W	0x00000303	GPIO3D driver strength control
GRF_GPIO3D_DS_1	0x02B4	W	0x00000303	GPIO3D driver strength control
GRF_GPIO3D_DS_2	0x02B8	W	0x00000303	GPIO3D driver strength control
GRF_GPIO3D_DS_3	0x02BC	W	0x00000303	GPIO3D driver strength control
GRF_GPIO4A_DS_0	0x02C0	W	0x00000303	GPIO4A driver strength control
GRF_GPIO4A_DS_1	0x02C4	W	0x00000303	GPIO4A driver strength control
GRF_GPIO4A_DS_2	0x02C8	W	0x00000303	GPIO3A driver strength control
GRF_GPIO4A_DS_3	0x02CC	W	0x00000303	GPIO4A driver strength control
GRF_GPIO4B_DS_0	0x02D0	W	0x00000303	GPIO4B driver strength control
GRF_GPIO4B_DS_1	0x02D4	W	0x00000303	GPIO4B driver strength control
GRF_GPIO4B_DS_2	0x02D8	W	0x00000303	GPIO4B driver strength control
GRF_GPIO4B_DS_3	0x02DC	W	0x00000303	GPIO4B driver strength control
GRF_GPIO4C_DS_0	0x02E0	W	0x00000303	GPIO4C driver strength control
GRF_GPIO4C_DS_1	0x02E4	W	0x00000303	GPIO4C driver strength control
GRF_GPIO4C_DS_2	0x02E8	W	0x00000303	GPIO4C driver strength control
GRF_GPIO4C_DS_3	0x02EC	W	0x00000103	GPIO4C driver strength control
GRF_GPIO4D_DS_0	0x02F0	W	0x00000101	GPIO4D driver strength control
GRF_GPIO4D_DS_1	0x02F4	W	0x00000101	GPIO4D driver strength control
GRF_GPIO4D_DS_2	0x02F8	W	0x00000101	GPIO4D driver strength control
GRF_GPIO4D_DS_3	0x02FC	W	0x00000101	GPIO4D driver strength control
GRF_IOFUNC_SEL0	0x0300	W	0x00000000	muti-IOMUX function control register0
GRF_IOFUNC_SEL1	0x0304	W	0x00000000	muti-IOMUX function control register1
GRF_IOFUNC_SEL2	0x0308	W	0x00000000	muti-IOMUX function control register2

Name	Offset	Size	Reset Value	Description
GRF_IOFUNC_SEL3	0x030C	W	0x00000000	muti-IOMUX function control register3
GRF_IOFUNC_SEL4	0x0310	W	0x00000000	muti-IOMUX function control register4
GRF_IOFUNC_SEL5	0x0314	W	0x00000000	muti-IOMUX function control register4
GRF_VI_CON0	0x0340	W	0x00000000	video input block register0
GRF_VI_CON1	0x0344	W	0x00000000	video input block register1
GRF_VI_STATUS0	0x0348	W	0x00000000	video input block status register
GRF_VO_CON0	0x0360	W	0x00008000	disphy control register0
GRF_VO_CON1	0x0364	W	0x00000000	disphy control register1
GRF_VO_CON2	0x0368	W	0x00000000	disphy control register2
GRF_MAC0_CON0	0x0380	W	0x00000000	GMAC control register0
GRF_MAC0_CON1	0x0384	W	0x00000000	GMAC control register1
GRF_MAC1_CON0	0x0388	W	0x00000000	GMAC control register1
GRF_MAC1_CON1	0x038C	W	0x00000000	GMAC control register1
GRF_BIU_CON0	0x03A0	W	0x00000000	NOC control register0
GRF_BIU_CON1	0x03A4	W	0x00000000	NOC control register2
GRF_BIU_CON2	0x03A8	W	0x00000000	NOC control register2
GRF_GIC_CON0	0x03C0	W	0x0000FD40	GIC control register0
GRF_GIC_CON1	0x03C4	W	0x0000FD45	GIC control register0
GRF_GIC_CON2	0x03C8	W	0x0000000F	GIC control register0
GRF_GPU_CON0	0x03F0	W	0x00000000	GMAC control register0
GRF_GPU_CON1	0x03F4	W	0xFFFFFFFF	GMAC control register0
GRF_CPU_CON0	0x0400	W	0x00000300	SOC control register0
GRF_CPU_STATUS0	0x0420	W	0x00000000	SOC status register0
GRF_SOC_CON0	0x0500	W	0x00000000	SOC control register0
GRF_SOC_CON1	0x0504	W	0x00000188	SOC control register1
GRF_SOC_CON2	0x0508	W	0x00000020	SOC control register2
GRF_SOC_CON3	0x050C	W	0x00000000	SOC control register3
GRF_SOC_CON4	0x0510	W	0x00000000	Register0000 Description
GRF_SOC_CON5	0x0514	W	0x0003A980	SOC control register5
GRF_SOC_CON6	0x0518	W	0x000000FF	SOC control register3
GRF_SOC_STATUS0	0x0580	W	0x00000000	SOC status register0
GRF_RAM_CON	0x05C0	W	0x00005401	SRAM control register0
GRF_CORE_RAM_CON	0x05C4	W	0x00000044	CORE SRAM control register
GRF_TSADC_CON	0x0600	W	0x00000000	TSADC Control Regesters
GRF_SARADC_CON	0x0610	W	0x00000007	SARADC Contronl Registers
GRF_GPUPVTPLL_CON0	0x0700	W	0x00000000	GPU PVTM control register0
GRF_GPUPVTPLL_CON1	0x0704	W	0x00000000	GPU PVTM control register1
GRF_GPUPVTPLL_CON2	0x0708	W	0x00000000	GPU PVTM status register0
GRF_GPUPVTPLL_CON3	0x070C	W	0x00000000	GPU PVTM status register0
GRF_NPUPVTPLL_CON0	0x0740	W	0x00000000	NPU PVTM control register0
GRF_NPUPVTPLL_CON1	0x0744	W	0x00000000	NPU PVTM control register1
GRF_NPUPVTPLL_CON2	0x0748	W	0x00000000	NPU PVTM status register0
GRF_NPUPVTPLL_CON3	0x074C	W	0x00000000	NPU PVTM status register0
GRF_CHIP_ID	0x0800	W	0x00003566	CHIP ID
GRF_GPIO1C5_DS	0x0840	W	0x00000001	GPIO1C5 driver strength control
GRF_GPIO2A2_DS	0x0844	W	0x00000001	GPIO2A2 driver strength control
GRF_GPIO2B0_DS	0x0848	W	0x00000001	GPIO2B0 driver strength control
GRF_GPIO3A0_DS	0x084C	W	0x00000001	GPIO3A0 driver strength control
GRF_GPIO3A6_DS	0x0850	W	0x00000001	GPIO3A6 driver strength control

Name	Offset	Size	Reset Value	Description
GRF_GPIO4A0_DS	0x0854	W	0x00000001	GPIO4A0 driver strength control
GRF_DMAC0_CON0	0x0900	W	0x0000FFFF	dma0 control register0
GRF_DMAC0_CON1	0x0904	W	0x0000FFFF	dma0 control register1
GRF_DMAC0_CON2	0x0908	W	0x0000FFFF	dma0 control register2
GRF_DMAC0_CON3	0x090C	W	0x00000001	dma control register3
GRF_DMAC0_CON4	0x0910	W	0x00005555	dma control register4
GRF_DMAC0_CON5	0x0914	W	0x00005555	dma control register5
GRF_DMAC0_CON6	0x0918	W	0x00005555	dma control register6
GRF_DMAC0_CON7	0x091C	W	0x00005555	dma control register7
GRF_DMAC0_CON8	0x0920	W	0x00000000	dma control register8
GRF_DMAC0_CON9	0x0924	W	0x00000000	dma control register9
GRF_DMAC1_CON0	0x0940	W	0x0000FFFF	dma1 control register0
GRF_DMAC1_CON1	0x0944	W	0x0000FFFF	dma1 control register1
GRF_DMAC1_CON2	0x0948	W	0x0000FFFF	dma1 control register2
GRF_DMAC1_CON3	0x094C	W	0x00000001	dma1 control register3
GRF_DMAC1_CON4	0x0950	W	0x00005555	dma1 control register4
GRF_DMAC1_CON5	0x0954	W	0x00000001	dma1 control register5
GRF_DMAC1_CON6	0x0958	W	0x00005555	dma control register6
GRF_DMAC1_CON7	0x095C	W	0x00000001	dma control register7
GRF_DMAC1_CON8	0x0960	W	0x00000000	dma1 control register8
GRF_DMAC1_CON9	0x0964	W	0x00000000	dma1 control register9

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.7.2 Detail Registers Description

GRF_GPIO1A_IOMUX_L

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1a3_sel 3'h0: GPIO1_A3 3'h1: I2S1_SCLKTXM0 3'h2: UART3_CTSNM0 3'h3: SCR_IO 3'h4: PCIE30X1_WAKENM2 3'h5: ACODEC_DACCLK
11	RO	0x0	reserved
10:8	RW	0x0	gpio1a2_sel 3'h0: GPIO1_A2 3'h1: I2S1_MCLKM0 3'h2: UART3_RTSNM0 3'h3: SCR_CLK 3'h4: PCIE30X1_PERSTNM2
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio1a1_sel 3'h0: GPIO1_A1 3'h1: I2C3_SCLM0 3'h2: UART3_TXM0 3'h3: CAN1_TXM0 3'h4: AUDIOpwmROUT 3'h5: ACODEC_ADCCLK 3'h6: AUDIOpwmLOUTN
3	RO	0x0	reserved
2:0	RW	0x0	gpio1a0_sel 3'h0: GPIO1_A0 3'h1: I2C3_SDAM0 3'h2: UART3_RXM0 3'h3: CAN1_RXM0 3'h4: AUDIOpwmLOUT 3'h5: ACODEC_ADCDATA 3'h6: AUDIOpwmLOUTP

GRF_GPIO1A_IOMUX_H

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1a7_sel 3'h0: GPIO1_A7 3'h1: I2S1_SDO0M0 3'h2: UART4_CTSNM0 3'h3: SCR_DET 3'h4: AUDIOpwmROUTN 3'h5: ACODEC_DAC_DATAL
11	RO	0x0	reserved
10:8	RW	0x0	gpio1a6_sel 3'h0: GPIO1_A6 3'h1: I2S1_LRCKRXM0 3'h2: UART4_TXM0 3'h3: PDM_CLK0M0 3'h4: AUDIOpwmROUTP
7	RO	0x0	reserved
6:4	RW	0x0	gpio1a5_sel 3'h0: GPIO1_A5 3'h1: I2S1_LRCKTXM0 3'h2: UART4_RTSNM0 3'h3: SCR_RST 3'h4: PCIE30X1_CLKREQNM2 3'h5: ACODEC_DACSYNC
3	RO	0x0	reserved
2:0	RW	0x0	gpio1a4_sel 3'h0: GPIO1_A4 3'h1: I2S1_SCLKRXM0 3'h2: UART4_RXM0 3'h3: PDM_CLK1M0 3'h4: SPDIF_TXM0

GRF_GPIO1B_IOMUX_L

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1b3_sel 3'h0: GPIO1_B3 3'h1: I2S1_SDI0M0 3'h2: PDM_SDI0M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio1b2_sel 3'h0: GPIO1_B2 3'h1: I2S1_SDO3M0 3'h2: I2S1_SDI1M0 3'h3: PDM_SDI1M0 3'h4: PCIE20_PERSTNM2
7	RO	0x0	reserved
6:4	RW	0x0	gpio1b1_sel 3'h0: GPIO1_B1 3'h1: I2S1_SDO2M0 3'h2: I2S1_SDI2M0 3'h3: PDM_SDI2M0 3'h4: PCIE20_WAKENM2 3'h5: ACODEC_ADC_SYNC
3	RO	0x0	reserved
2:0	RW	0x0	gpio1b0_sel 3'h0: GPIO1_B0 3'h1: I2S1_SDO1M0 3'h2: I2S1_SDI3M0 3'h3: PDM_SDI3M0 3'h4: PCIE20_CLKREQNM2 3'h5: ACODEC_DAC_DATAR

GRF_GPIO1B_IOMUX_H

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1b7_sel 3'h0: GPIO1_B7 3'h1: EMMC_D3 3'h2: FLASH_D3
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio1b6_sel 3'h0: GPIO1_B6 3'h1: EMMC_D2 3'h2: FLASH_D2
7	RO	0x0	reserved
6:4	RW	0x0	gpio1b5_sel 3'h0: GPIO1_B5 3'h1: EMMC_D1 3'h2: FLASH_D1
3	RO	0x0	reserved
2:0	RW	0x0	gpio1b4_sel 3'h0: GPIO1_B4 3'h1: EMMC_D0 3'h2: FLASH_D0

GRF_GPIO1C_IOMUX_L

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1c3_sel 3'h0: GPIO1_C3 3'h1: EMMC_D7 3'h2: FLASH_D7
11	RO	0x0	reserved
10:8	RW	0x0	gpio1c2_sel 3'h0: GPIO1_C2 3'h1: EMMC_D6 3'h2: FLASH_D6
7	RO	0x0	reserved
6:4	RW	0x0	gpio1c1_sel 3'h0: GPIO1_C1 3'h1: EMMC_D5 3'h2: FLASH_D5
3	RO	0x0	reserved
2:0	RW	0x0	gpio1c0_sel 3'h0: GPIO1_C0 3'h1: EMMC_D4 3'h2: FLASH_D4

GRF_GPIO1C_IOMUX_H

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio1c7_sel 3'h0: GPIO1_C7 3'h1: EMMC_RSTN 3'h2: FSPI_D2 3'h3: FLASH_WPN
11	RO	0x0	reserved
10:8	RW	0x0	gpio1c6_sel 3'h0: GPIO1_C6 3'h1: EMMC_DATASTROBE 3'h2: FSPI_CS1N 3'h3: FLASH_CLE
7	RO	0x0	reserved
6:4	RW	0x0	gpio1c5_sel 3'h0: GPIO1_C5 3'h1: EMMC_CLKOUT 3'h2: FLASH_DQS
3	RO	0x0	reserved
2:0	RW	0x0	gpio1c4_sel 3'h0: GPIO1_C4 3'h1: EMMC_CMD 3'h2: FLASH_WRN

GRF_GPIO1D_IOMUX_L

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1d3_sel 3'h0: GPIO1_D3 3'h1: FSPI_CS0N 3'h2: FLASH_CS0N
11	RO	0x0	reserved
10:8	RW	0x0	gpio1d2_sel 3'h0: GPIO1_D2 3'h1: FSPI_D1 3'h2: FLASH_RDN
7	RO	0x0	reserved
6:4	RW	0x0	gpio1d1_sel 3'h0: GPIO1_D1 3'h1: FSPI_D0 3'h2: FLASH_RDY
3	RO	0x0	reserved
2:0	RW	0x0	gpio1d0_sel 3'h0: GPIO1_D0 3'h1: FSPI_CLK 3'h2: FLASH_ALE

GRF_GPIO1D_IOMUX_H

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x2	gpio1d7_sel 3'h0: GPIO1_D7 3'h1: SDMMC0_D2 3'h2: JTAG_TCK 3'h3: UART5_CTSNM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio1d6_sel 3'h0: GPIO1_D6 3'h1: SDMMC0_D1 3'h2: UART2_RXM1 3'h3: UART6_RXM1 3'h4: PWM9_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio1d5_sel 3'h0: GPIO1_D5 3'h1: SDMMC0_D0 3'h2: UART2_TXM1 3'h3: UART6_TXM1 3'h4: PWM8_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio1d4_sel 3'h0: GPIO1_D4 3'h1: FSPI_D3 3'h2: FLASH_CS1N

GRF_GPIO2A_IOMUX_L

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2a3_sel 3'h0: GPIO2_A3 3'h1: SDMMC1_D0 3'h2: GMAC0_RXD2 3'h3: UART6_RXM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio2a2_sel 3'h0: GPIO2_A2 3'h1: SDMMC0_CLK 3'h2: TEST_CLKOUT 3'h3: UART5_TXM0 3'h4: CAN0_RXM1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2a1_sel 3'h0: GPIO2_A1 3'h1: SDMMC0_CMD 3'h2: PWM10_M1 3'h3: UART5_RXM0 3'h4: CAN0_TXM1
3	RO	0x0	reserved
2:0	RW	0x2	gpio2a0_sel 3'h0: GPIO2_A0 3'h1: SDMMC0_D3 3'h2: JTAG_TMS 3'h3: UART5_RTSNM0

GRF_GPIO2A_IOMUX_H

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2a7_sel 3'h0: GPIO2_A7 3'h1: SDMMC1_CMD 3'h2: GMAC0_TXD3 3'h3: UART9_RXM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio2a6_sel 3'h0: GPIO2_A6 3'h1: SDMMC1_D3 3'h2: GMAC0_TXD2 3'h3: UART7_TXM0
7	RO	0x0	reserved
6:4	RW	0x0	gpio2a5_sel 3'h0: GPIO2_A5 3'h1: SDMMC1_D2 3'h2: GMAC0_RXCLK 3'h3: UART7_RXM0
3	RO	0x0	reserved
2:0	RW	0x0	gpio2a4_sel 3'h0: GPIO2_A4 3'h1: SDMMC1_D1 3'h2: GMAC0_RXD3 3'h3: UART6_TXM0

GRF_GPIO2B_IOMUX_L

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio2b3_sel 3'h0: GPIO2_B3 3'h1: GMAC0_TXD0 3'h2: UART1_RXM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio2b2_sel 3'h0: GPIO2_B2 3'h1: SDMMC1_DET 3'h2: I2C4_SCLM1 3'h3: UART8_CTSNM0 3'h4: CAN2_TXM1
7	RO	0x0	reserved
6:4	RW	0x0	gpio2b1_sel 3'h0: GPIO2_B1 3'h1: SDMMC1_PWREN 3'h2: I2C4_SDAM1 3'h3: UART8_RTSNM0 3'h4: CAN2_RXM1
3	RO	0x0	reserved
2:0	RW	0x0	gpio2b0_sel 3'h0: GPIO2_B0 3'h1: SDMMC1_CLK 3'h2: GMAC0_TXCLK 3'h3: UART9_TXM0

GRF_GPIO2B_IOMUX_H

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2b7_sel 3'h0: GPIO2_B7 3'h1: I2S2_SCLKRXM0 3'h2: GMAC0_RXD1 3'h3: UART6_RTSNM0 3'h4: SPI1_MOSIM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio2b6_sel 3'h0: GPIO2_B6 3'h1: GMAC0_RXD0 3'h2: UART1_CTSNM0 3'h3: SPI1_MISOM0
7	RO	0x0	reserved
6:4	RW	0x0	gpio2b5_sel 3'h0: GPIO2_B5 3'h1: GMAC0_TXEN 3'h2: UART1_RTSNM0 3'h3: SPI1_CLKM0
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	gpio2b4_sel 3'h0: GPIO2_B4 3'h1: GMAC0_TXD1 3'h2: UART1_TXM0

GRF_GPIO2C_IOMUX_L

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2c3_sel 3'h0: GPIO2_C3 3'h1: I2S2_LRCKTXM0 3'h2: GMAC0_MDC 3'h3: UART9_RTSNM0 3'h4: SPI2_MOSIM0
11	RO	0x0	reserved
10:8	RW	0x0	gpio2c2_sel 3'h0: GPIO2_C2 3'h1: I2S2_SCLKTXM0 3'h2: GMAC0_MCLKINOUT 3'h3: UART7_CTSNM0 3'h4: SPI2_MISOM0
7	RO	0x0	reserved
6:4	RW	0x0	gpio2c1_sel 3'h0: GPIO2_C1 3'h1: I2S2_MCLKM0 3'h2: ETH0_REFCLKO25M 3'h3: UART7_RTSNM0 3'h4: SPI2_CLKM0
3	RO	0x0	reserved
2:0	RW	0x0	gpio2c0_sel 3'h0: GPIO2_C0 3'h1: I2S2_LRCKRXM0 3'h2: GMAC0_RXDVCRS 3'h3: UART6_CTSNM0 3'h4: SPI1_CS0M0

GRF_GPIO2C_IOMUX_H

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	gpio2c6_sel 3'h0: GPIO2_C6 3'h1: CLK32K_OUT1 3'h2: UART8_RXM0 3'h3: SPI1_CS1M0
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio2c5_sel 3'h0: GPIO2_C5 3'h1: I2S2_SDIM0 3'h2: GMAC0_RXER 3'h3: UART8_TXM0 3'h4: SPI2_CS1M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio2c4_sel 3'h0: GPIO2_C4 3'h1: I2S2_SDOM0 3'h2: GMAC0_MDIO 3'h3: UART9_CTSNM0 3'h4: SPI2_CS0M0

GRF_GPIO2D_IOMUX_L

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x2	gpio2d3_sel 3'h0: GPIO2_D3 3'h1: LCDC_D3 3'h2: BT656_D3M0 3'h3: SPI0_CLKM1 3'h4: PCIE30X1_WAKENM1 3'h5: I2S1_SDI0M2
11	RO	0x0	reserved
10:8	RW	0x0	gpio2d2_sel 3'h0: GPIO2_D2 3'h1: LCDC_D2 3'h2: BT656_D2M0 3'h3: SPI0_CS0M1 3'h4: PCIE30X1_CLKREQNM1 3'h5: I2S1_LRCKTXM2
7	RO	0x0	reserved
6:4	RW	0x0	gpio2d1_sel 3'h0: GPIO2_D1 3'h1: LCDC_D1 3'h2: BT656_D1M0 3'h3: SPI0_MOSIM1 3'h4: PCIE20_WAKENM1 3'h5: I2S1_SCLKTXM2
3	RO	0x0	reserved
2:0	RW	0x0	gpio2d0_sel 3'h0: GPIO2_D0 3'h1: LCDC_D0 3'h2: BT656_D0M0 3'h3: SPI0_MISOM1 3'h4: PCIE20_CLKREQNM1 3'h5: I2S1_MCLKM2

GRF_GPIO2D_IOMUX_H

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio2d7_sel 3'h0: GPIO2_D7 3'h1: LCDC_D7 3'h2: BT656_D7M0 3'h3: SPI2_MISOM1 3'h4: UART8_TXM1 3'h5: I2S1_SDO0M2
11	RO	0x0	reserved
10:8	RW	0x2	gpio2d6_sel 3'h0: GPIO2_D6 3'h1: LCDC_D6 3'h2: BT656_D6M0 3'h3: SPI2_MOSIM1 3'h4: PCIE30X2_PERSTNM1 3'h5: I2S1_SDI3M2
7	RO	0x0	reserved
6:4	RW	0x2	gpio2d5_sel 3'h0: GPIO2_D5 3'h1: LCDC_D5 3'h2: BT656_D5M0 3'h3: SPI2_CS0M1 3'h4: PCIE30X2_WAKENM1 3'h5: I2S1_SDI2M2
3	RO	0x0	reserved
2:0	RW	0x2	gpio2d4_sel 3'h0: GPIO2_D4 3'h1: LCDC_D4 3'h2: BT656_D4M0 3'h3: SPI2_CS1M1 3'h4: PCIE30X2_CLKREQNM1 3'h5: I2S1_SDI1M2

GRF_GPIO3A_IOMUX_L

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3a3_sel 3'h0: GPIO3_A3 3'h1: LCDC_D10 3'h2: BT1120_D2 3'h3: GMAC1_TXD3M0 3'h4: I2S3_SCLKM0 3'h5: SDMMC2_D2M1

Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:8	RW	0x0	gpio3a2_sel 3'h0: GPIO3_A2 3'h1: LCDC_D9 3'h2: BT1120_D1 3'h3: GMAC1_TXD2M0 3'h4: I2S3_MCLKM0 3'h5: SDMMC2_D1M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3a1_sel 3'h0: GPIO3_A1 3'h1: LCDC_D8 3'h2: BT1120_D0 3'h3: SPI1_CS0M1 3'h4: PCIE30X1_PERSTNM1 3'h5: SDMMC2_D0M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3a0_sel 3'h0: GPIO3_A0 3'h1: LCDC_CLK 3'h2: BT656_CLKM0 3'h3: SPI2_CLKM1 3'h4: UART8_RXM1 3'h5: I2S1_SDO1M2

GRF_GPIO3A_IOMUX_H

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3a7_sel 3'h0: GPIO3_A7 3'h1: LCDC_D14 3'h2: BT1120_D5 3'h3: GMAC1_RXCLKM0 3'h4: SDMMC2_DETM1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3a6_sel 3'h0: GPIO3_A6 3'h1: LCDC_D13 3'h2: BT1120_CLK 3'h3: GMAC1_TXCLKM0 3'h4: I2S3_SDIM0 3'h5: SDMMC2_CLKM1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio3a5_sel 3'h0: GPIO3_A5 3'h1: LCDC_D12 3'h2: BT1120_D4 3'h3: GMAC1_RXD3M0 3'h4: I2S3_SDOM0 3'h5: SDMMC2_CMDM1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3a4_sel 3'h0: GPIO3_A4 3'h1: LCDC_D11 3'h2: BT1120_D3 3'h3: GMAC1_RXD2M0 3'h4: I2S3_LRCKM0 3'h5: SDMMC2_D3M1

GRF_GPIO3B_IOMUX_L

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3b3_sel 3'h0: GPIO3_B3 3'h1: LCDC_D18 3'h2: BT1120_D9 3'h3: GMAC1_RXDVCRSM0 3'h4: I2C5_SCLM0 3'h5: PDM_SDI0M2
11	RO	0x0	reserved
10:8	RW	0x0	gpio3b2_sel 3'h0: GPIO3_B2 3'h1: LCDC_D17 3'h2: BT1120_D8 3'h3: GMAC1_RXD1M0 3'h4: UART4_TXM1 3'h5: PWM9_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio3b1_sel 3'h0: GPIO3_B1 3'h1: LCDC_D16 3'h2: BT1120_D7 3'h3: GMAC1_RXD0M0 3'h4: UART4_RXM1 3'h5: PWM8_M0
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	gpio3b0_sel 3'h0: GPIO3_B0 3'h1: LCDC_D15 3'h2: BT1120_D6 3'h3: ETH1_REFCLKO25MM0 3'h4: SDMMC2_PWRENM1

GRF_GPIO3B_IOMUX_H

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3b7_sel 3'h0: GPIO3_B7 3'h1: LCDC_D22 3'h2: PWM12_M0 3'h3: GMAC1_TXENM0 3'h4: UART3_TXM1 3'h5: PDM_SDI2M2
11	RO	0x0	reserved
10:8	RW	0x0	gpio3b6_sel 3'h0: GPIO3_B6 3'h1: LCDC_D21 3'h2: BT1120_D12 3'h3: GMAC1_TXD1M0 3'h4: I2C3_SDAM1 3'h5: PWM11_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio3b5_sel 3'h0: GPIO3_B5 3'h1: LCDC_D20 3'h2: BT1120_D11 3'h3: GMAC1_TXD0M0 3'h4: I2C3_SCLM1 3'h5: PWM10_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio3b4_sel 3'h0: GPIO3_B4 3'h1: LCDC_D19 3'h2: BT1120_D10 3'h3: GMAC1_RXERM0 3'h4: I2C5_SDAM0 3'h5: PDM_SDI1M2

GRF_GPIO3C_IOMUX_L

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3c3_sel 3'h0: GPIO3_C3 3'h1: LCDC_DEN 3'h2: BT1120_D15 3'h3: SPI1_CLKM1 3'h4: UART5_RXM1 3'h5: I2S1_SCLKRXM2
11	RO	0x0	reserved
10:8	RW	0x0	gpio3c2_sel 3'h0: GPIO3_C2 3'h1: LCDC_VSYNC 3'h2: BT1120_D14 3'h3: SPI1_MISOM1 3'h4: UART5_TXM1 3'h5: I2S1_SDO3M2
7	RO	0x0	reserved
6:4	RW	0x0	gpio3c1_sel 3'h0: GPIO3_C1 3'h1: LCDC_HSYNC 3'h2: BT1120_D13 3'h3: SPI1_MOSIM1 3'h4: PCIE20_PERSTNM1 3'h5: I2S1_SDO2M2
3	RO	0x0	reserved
2:0	RW	0x0	gpio3c0_sel 3'h0: GPIO3_C0 3'h1: LCDC_D23 3'h2: PWM13_M0 3'h3: GMAC1_MCLKINOUTM0 3'h4: UART3_RXM1 3'h5: PDM_SDI3M2

GRF_GPIO3C_IOMUX_H

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3c7_sel 3'h0: GPIO3_C7 3'h1: CIF_D1 3'h2: EBC_SDDO1 3'h3: SDMMC2_D1M0 3'h4: I2S1_SCLKTXM1 3'h5: BT656_D1M1
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio3c6_sel 3'h0: GPIO3_C6 3'h1: CIF_D0 3'h2: EBC_SDDO0 3'h3: SDMMC2_D0M0 3'h4: I2S1_MCLKM1 3'h5: BT656_D0M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3c5_sel 3'h0: GPIO3_C5 3'h1: PWM15_M0 3'h2: SPDIF_TXM1 3'h3: GMAC1_MDIOM0 3'h4: UART7_RXM1 3'h5: I2S1_LRCKRXM2
3	RO	0x0	reserved
2:0	RW	0x0	gpio3c4_sel 3'h0: GPIO3_C4 3'h1: PWM14_M0 3'h2: VOP_PWMM1 3'h3: GMAC1_MDCM0 3'h4: UART7_TXM1 3'h5: PDM_CLK1M2

GRF_GPIO3D_IOMUX_L

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d3_sel 3'h0: GPIO3_D3 3'h1: CIF_D5 3'h2: EBC_SDDO5 3'h3: SDMMC2_CLKM0 3'h4: I2S1_SDI1M1 3'h5: BT656_D5M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d2_sel 3'h0: GPIO3_D2 3'h1: CIF_D4 3'h2: EBC_SDDO4 3'h3: SDMMC2_CMDM0 3'h4: I2S1_SDI0M1 3'h5: BT656_D4M1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio3d1_sel 3'h0: GPIO3_D1 3'h1: CIF_D3 3'h2: EBC_SDDO3 3'h3: SDMMC2_D3M0 3'h4: I2S1_SDO0M1 3'h5: BT656_D3M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d0_sel 3'h0: GPIO3_D0 3'h1: CIF_D2 3'h2: EBC_SDDO2 3'h3: SDMMC2_D2M0 3'h4: I2S1_LRCKTXM1 3'h5: BT656_D2M1

GRF_GPIO3D_IOMUX_H

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d7_sel 3'h0: GPIO3_D7 3'h1: CIF_D9 3'h2: EBC_SDDO9 3'h3: GMAC1_TXD3M1 3'h4: UART1_RXM1 3'h5: PDM_SDI0M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d6_sel 3'h0: GPIO3_D6 3'h1: CIF_D8 3'h2: EBC_SDDO8 3'h3: GMAC1_TXD2M1 3'h4: UART1_TXM1 3'h5: PDM_CLK0M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d5_sel 3'h0: GPIO3_D5 3'h1: CIF_D7 3'h2: EBC_SDDO7 3'h3: SDMMC2_PWRENM0 3'h4: I2S1_SDI3M1 3'h5: BT656_D7M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d4_sel 3'h0: GPIO3_D4 3'h1: CIF_D6 3'h2: EBC_SDDO6 3'h3: SDMMC2_DETM0 3'h4: I2S1_SDI2M1 3'h5: BT656_D6M1

GRF_GPIO4A_IOMUX_L

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a3_sel 3'h0: GPIO4_A3 3'h1: CIF_D13 3'h2: EBC_SDDO13 3'h3: GMAC1_RXCLKM1 3'h4: UART7_RXM2 3'h5: PDM_SDI3M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a2_sel 3'h0: GPIO4_A2 3'h1: CIF_D12 3'h2: EBC_SDDO12 3'h3: GMAC1_RXD3M1 3'h4: UART7_TXM2 3'h5: PDM_SDI2M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio4a1_sel 3'h0: GPIO4_A1 3'h1: CIF_D11 3'h2: EBC_SDDO11 3'h3: GMAC1_RXD2M1 3'h4: PDM_SDI1M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a0_sel 3'h0: GPIO4_A0 3'h1: CIF_D10 3'h2: EBC_SDDO10 3'h3: GMAC1_TXCLKM1 3'h4: PDM_CLK1M1

GRF_GPIO4A_IOMUX_H

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a7_sel 3'h0: GPIO4_A7 3'h1: CAM_CLKOUT0 3'h2: EBC_SDCE1 3'h3: GMAC1_RXD0M1 3'h4: SPI3_CS1M0 3'h5: I2S1_LRCKRXM1
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio4a6_sel 3'h0: GPIO4_A6 3'h1: ISP_FLASHTRIGOUT 3'h2: EBC_SDCE0 3'h3: GMAC1_TXENM1 3'h4: SPI3_CS0M0 3'h5: I2S1_SCLKRXM1
7	RO	0x0	reserved
6:4	RW	0x0	gpio4a5_sel 3'h0: GPIO4_A5 3'h1: CIF_D15 3'h2: EBC_SDDO15 3'h3: GMAC1_TXD1M1 3'h4: UART9_RXM2 3'h5: I2S2_LRCKRXM1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a4_sel 3'h0: GPIO4_A4 3'h1: CIF_D14 3'h2: EBC_SDDO14 3'h3: GMAC1_TXD0M1 3'h4: UART9_TXM2 3'h5: I2S2_LRCKTXM1

GRF_GPIO4B_IOMUX_L

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4b3_sel 3'h0: GPIO4_B3 3'h1: I2C4_SCLM0 3'h2: EBC_GDOE 3'h3: ETH1_REFCLKO25MM1 3'h4: SPI3_CLKM0 3'h5: I2S2_SDOM1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4b2_sel 3'h0: GPIO4_B2 3'h1: I2C4_SDAM0 3'h2: EBC_VCOM 3'h3: GMAC1_RXERM1 3'h4: SPI3_MOSIM0 3'h5: I2S2_SDIM1
7	RO	0x0	reserved
6:4	RW	0x0	gpio4b1_sel 3'h0: GPIO4_B1 3'h1: ISP_PRELIGHTTRIG 3'h2: EBC_SDCE3 3'h3: GMAC1_RXDVCRSM1 3'h4: I2S1_SDO2M1
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	gpio4b0_sel 3'h0: GPIO4_B0 3'h1: CAM_CLKOUT1 3'h2: EBC_SDCE2 3'h3: GMAC1_RXD1M1 3'h4: SPI3_MISOM0 3'h5: I2S1_SDO1M1

GRF_GPIO4B_IOMUX_H

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4b7_sel 3'h0: GPIO4_B7 3'h1: CIF_VSYNC 3'h2: EBC_SDOE 3'h3: GMAC1_MDIOM1 3'h4: I2S2_SCLKTXM1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4b6_sel 3'h0: GPIO4_B6 3'h1: CIF_HREF 3'h2: EBC_SDLE 3'h3: GMAC1_MDCM1 3'h4: UART1_RTSNM1 3'h5: I2S2_MCLKM1
7	RO	0x0	reserved
6:4	RW	0x0	gpio4b5_sel 3'h0: GPIO4_B5 3'h1: I2C2_SCLM1 3'h2: EBC_SDSHR 3'h3: CAN2_TXM0 3'h4: I2S1_SDO3M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4b4_sel 3'h0: GPIO4_B4 3'h1: I2C2_SDAM1 3'h2: EBC_GDSP 3'h3: CAN2_RXM0 3'h4: ISP_FLASHTRIGIN 3'h5: BT656_CLKM1

GRF_GPIO4C_IOMUX_L

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio4c3_sel 3'h0: GPIO4_C3 3'h1: PWM15_M1 3'h2: SPI3_MOSIM1 3'h3: CAN1_TXM1 3'h4: PCIE30X2_WAKENM2 3'h5: I2S3_SCLKM1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4c2_sel 3'h0: GPIO4_C2 3'h1: PWM14_M1 3'h2: SPI3_CLKM1 3'h3: CAN1_RXM1 3'h4: PCIE30X2_CLKREQNM2 3'h5: I2S3_MCLKM1
7	RO	0x0	reserved
6:4	RW	0x0	gpio4c1_sel 3'h0: GPIO4_C1 3'h1: CIF_CLKIN 3'h2: EBC_SDCLK 3'h3: GMAC1_MCLKINOUTM1 3'h4: UART1_CTSNM1 3'h5: I2S2_SCLKRXM1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4c0_sel 3'h0: GPIO4_C0 3'h1: CIF_CLKOUT 3'h2: EBC_GDCLK 3'h3: PWM11_M1

GRF_GPIO4C_IOMUX_H

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4c7_sel 3'h0: GPIO4_C7 3'h1: HDMITX_SCL 3'h2: I2C5_SCLM1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4c6_sel 3'h0: GPIO4_C6 3'h1: PWM13_M1 3'h2: SPI3_CS0M1 3'h3: SATA0_ACTLED 3'h4: UART9_RXM1 3'h5: I2S3_SDIM1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio4c5_sel 3'h0: GPIO4_C5 3'h1: PWM12_M1 3'h2: SPI3_MISOM1 3'h3: SATA1_ACTLED 3'h4: UART9_TXM1 3'h5: I2S3_SDOM1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4c4_sel 3'h0: GPIO4_C4 3'h1: EDPDP_HPDINM0 3'h2: SPDIF_TXM2 3'h3: SATA2_ACTLED 3'h4: PCIE30X2_PERSTNM2 3'h5: I2S3_LRCKM1

GRF_GPIO4D_IOMUX_L

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x0	gpio4d2_sel 3'h0: GPIO4_D2
7	RO	0x0	reserved
6:4	RW	0x0	gpio4d1_sel 3'h0: GPIO4_D1 3'h1: HDMITX_CECM0 3'h2: SPI3_CS1M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4d0_sel 3'h0: GPIO4_D0 3'h1: HDMITX_SDA 3'h2: I2C5_SDAM1

GRF_GPIO1A_P

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio1a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio1a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio1a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio1a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio1a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x1	gpio1a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio1a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO1B_P

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio1b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio1b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
9:8	RW	0x1	gpio1b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio1b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio1b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio1b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio1b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO1C_P

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio1c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio1c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio1c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
7:6	RW	0x1	gpio1c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x1	gpio1c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x1	gpio1c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio1c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO1D_P

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1d7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio1d6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio1d5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio1d4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio1d3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
5:4	RW	0x1	gpio1d2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio1d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio1d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO2A_P

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio2a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio2a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio2a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio2a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio2a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio2a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio2a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio2a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO2B_P

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio2b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio2b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio2b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio2b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio2b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x1	gpio2b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio2b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
1:0	RW	0x2	gpio2b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO2C_P

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio2c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio2c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio2c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio2c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio2c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio2c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio2c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio2c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO2D_P

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio2d7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio2d6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio2d5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio2d4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio2d3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio2d2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio2d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio2d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO3A_P

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x2	gpio3a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO3B_P

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio3b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO3C_P

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio3c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO3D_P

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3d7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3d6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3d5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio3d4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3d3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3d2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO4A_P

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio4a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio4a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio4a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio4a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
7:6	RW	0x2	gpio4a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio4a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio4a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio4a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO4B_P

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio4b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio4b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio4b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio4b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio4b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
5:4	RW	0x2	gpio4b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio4b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio4b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO4C_P

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio4c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio4c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio4c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio4c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio4c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio4c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio4c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio4c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO4D_P

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x0	gpio4c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x0	gpio4c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio4c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio4c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x1	gpio4c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio4c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio4c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GRF_GPIO1A_IE

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio1a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio1a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio1a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio1a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio1a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio1a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio1a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO1B_IE

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio1b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio1b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio1b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio1b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio1b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio1b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio1b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO1C_IE

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio1c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio1c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio1c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio1c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio1c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio1c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio1c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO1D_IE

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1d7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio1d6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio1d5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio1d4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio1d3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio1d2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio1d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio1d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO2A_IE

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio2a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio2a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio2a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio2a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio2a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio2a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio2a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO2B_IE

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio2b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio2b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio2b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio2b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio2b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio2b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio2b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO2C_IE

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio2c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio2c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio2c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio2c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio2c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio2c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio2c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO2D_IE

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio2d7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio2a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio2a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio2d4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio2d3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio2d2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio2d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio2d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO3A_IE

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio3a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio3a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio3a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio3a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio3a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio3a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio3a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO3B_IE

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio3b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio3b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio3b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio3b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio3b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio3b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio3b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO3C_IE

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio3c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio3c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio3c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio3c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio3c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio3c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio3c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO3D_IE

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3d7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio3d6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio3d5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio3d4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio3d3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio3d2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio3d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio3d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO4A_IE

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio4a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio4a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio4a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio4a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio4a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio4a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio4a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO4B_IE

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio4b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio4b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio4b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio4b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio4b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio4b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio4b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO4C_IE

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio4c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio4c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio4c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio4c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio4c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio4c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio4c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO4D_IE

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x0	gpio3a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x0	gpio3a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x0	gpio3a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x0	gpio3a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x0	gpio3a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x0	gpio3a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x0	gpio3a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GRF_GPIO1A_OPD

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1B_OPD

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1b6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio1b5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1b4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1b3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1b2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1b1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1b0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1C_OPD

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1c6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1c5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1c4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1c3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio1c2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1c1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1c0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1D_OPD

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2A_OPD

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2B_OPD

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2b7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	gpio2b6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2b5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2b4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2b3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2b2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2b1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2b0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2C_OPD

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2c7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2c6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2c5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2c4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	gpio2c3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2c2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2c1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2c0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2D_OPD

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2d7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2d6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2d5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2d4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2d3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2d2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2d1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio2d0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3A_OPD

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3B_OPD

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3b6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3b5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3b4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3b3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3b2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3b1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3b0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3C_OPD

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3c7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3c6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3c5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	gpio3c4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3c3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3c2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3c1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3c0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3D_OPD

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3d7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3d6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3d5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3d4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3d3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3d2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	gpio3d1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3d0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4A_OPD

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4a6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4a5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4a4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4a3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4a2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4a1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4a0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4B_OPD

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4b7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4b6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4b5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4b4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4b3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4b2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4b1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4b0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4C_OPD

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4c7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4c6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio4c5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4c4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4c3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4c2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4c1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4c0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4D_OPD

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4d7_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4d6_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4d5_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4d4_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4d3_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio4d2_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4d1_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4d0_opd GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1A_SUS

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1B_SUS

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1C_SUS

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	gpio1c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1D_SUS

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1d4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	gpio1d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1d2_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1d1_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1d0_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2A_SUS

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio2a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2B_SUS

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2C_SUS

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	gpio2c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio2c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio2c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO2D_SUS

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio2d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio2d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio2d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
4	RW	0x0	gpio2d4_sus GPIO PAD weak Pull Keeper enable 1'b1: Enable
3	RW	0x0	gpio2d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio2d2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio2d1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2d0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3A_SUS

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3a4_sus GPIO PADweak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	gpio3a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3B_SUS

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3C_SUS

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO3D_SUS

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio3d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3d4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3d2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3d1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3d0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4A_SUS

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_sus GPIO PAD weak Pull Keeper enablee 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	gpio4a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4B_SUS

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4b6_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4C_SUS

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO4D_SUS

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	gpio4d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4d4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4d2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4d1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4d0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GRF_GPIO1A_SL

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio1a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio1a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio1a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio1a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio1a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio1a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio1a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO1B_SL

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio1b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio1b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio1b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio1b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio1b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio1b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio1b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO1C_SL

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio1c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio1c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio1c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio1c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio1c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio1c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO1D_SL

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio1d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio1d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio1d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio1d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio1d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio1d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio1d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio1d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO2A_SL

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio2a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio2a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio2a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio2a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio2a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio2a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio2a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO2B_SL

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio2b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio2b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio2b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio2b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio2b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio2b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio2b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO2C_SL

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio2c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio2c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio2c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio2c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio2c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio2c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio2c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO2D_SL

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio2d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio2d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio2d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio2d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio2d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio2d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio2d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio2d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO3A_SL

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio3a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio3a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio3a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio3a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio3a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio3a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio3a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO3B_SL

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio3b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio3b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio3b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio3b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio3b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio3b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio3b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO3C_SL

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio3c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio3c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio3c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio3c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio3c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio3c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio3c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO3D_SL

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio3d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio3d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio3d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio3d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio3d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio3d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio3d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO4A_SL

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio4a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio4a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio4a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio4a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio4a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio4a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio4a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO4B_SL

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
15:14	RW	0x0	gpio4b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio4b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio4b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio4b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio4b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio4b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio4b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio4b0_sl 2'b00: slowest .. .. 2'b11: faset Always set to 2'b11 in normal operation.

GRF_GPIO4C_SL

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio4c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio4c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio4c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio4c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio4c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio4c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio4c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO4D_SL

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio4d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x0	gpio4d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x0	gpio4d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x0	gpio4d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x0	gpio4d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x0	gpio4d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x0	gpio4d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x0	gpio4d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GRF_GPIO1A_DS_0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio1a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio1a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1A_DS_1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio1a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio1a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1A_DS_2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio1a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio1a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1A_DS_3

Address: Operational Base + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio1a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio1a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1B_DS_0

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio1b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio1b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1B_DS_1

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio1b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio1b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1B_DS_2

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio1b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1B_DS_3

Address: Operational Base + offset (0x021C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1C_DS_0

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio1c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1C_DS_1

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1C_DS_2

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1C_DS_3

Address: Operational Base + offset (0x022C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	gpio1c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	gpio1c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1D_DS_0

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio1d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1D_DS_1

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x01	gpio1d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1D_DS_2

Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio1d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO1D_DS_3

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio1d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2A_DS_0

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio2a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2A_DS_1

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2A_DS_2

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Copwrite_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio2a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2A_DS_3

Address: Operational Base + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2B_DS_0

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2B_DS_1

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio2b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2B_DS_2

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2B_DS_3

Address: Operational Base + offset (0x025C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio2b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2C_DS_0

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2C_DS_1

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2C_DS_2

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio2c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2C_DS_3

Address: Operational Base + offset (0x026C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2D_DS_0

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio2d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2D_DS_1

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2D_DS_2

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio2d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2D_DS_3

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio2d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio2d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A_DS_0

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A_DS_1

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio3a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A_DS_2

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A_DS_3

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3B_DS_0

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio3b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3B_DS_1

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3B_DS_2

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio3b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3B_DS_3

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3C_DS_0

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	gpio3c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3C_DS_1

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio3c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3C_DS_2

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3C_DS_3

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio3c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3D_DS_0

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3D_DS_1

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3D_DS_2

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio3d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3D_DS_3

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio3d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio3d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4A_DS_0

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio4a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4A_DS_1

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4A_DS_2

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4A_DS_3

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio4a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4B_DS_0

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4B_DS_1

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio4b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4B_DS_2

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4B_DS_3

Address: Operational Base + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4C_DS_0

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x03	gpio4c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4C_DS_1

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x03	gpio4c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4C_DS_2

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x03	gpio4c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4C_DS_3

Address: Operational Base + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio4c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x03	gpio4c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4D_DS_0

Address: Operational Base + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio4d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio4d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4D_DS_1

Address: Operational Base + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio4d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	gpio4d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4D_DS_2

Address: Operational Base + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x01	gpio4d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio4d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4D_DS_3

Address: Operational Base + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x01	gpio4d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x01	gpio4d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_IOFUNC_SEL0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	i2c2_iomux_sel I2C2 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
13:11	RO	0x0	reserved
10	RW	0x0	hdmitx_iomux_sel HDMITX IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
9	RO	0x0	reserved
8	RW	0x0	gmac1_iomux_sel GMAC1 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
7	RO	0x0	reserved
6	RW	0x0	edp_hpd_iomux_sel EDP_HPD IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	can2_iomux_sel CAN2 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
3	RO	0x0	reserved
2	RW	0x0	can1_iomux_sel CAN1 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
1	RO	0x0	reserved
0	RW	0x0	can0_iomux_sel CAN0 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

GRF_IOFUNC_SEL1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pwm8_iomux_sel PWM8 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
13:5	RO	0x000	reserved
4	RW	0x0	i2c5_iomux_sel I2C5 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
3	RO	0x0	reserved
2	RW	0x0	i2c4_iomux_sel I2C4 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
1	RO	0x0	reserved
0	RW	0x0	i2c3_iomux_sel I2C3 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

GRF_IOFUNC_SEL2

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	sdmmc2_iomux_sel SDMMC2 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

Bit	Attr	Reset Value	Description
13	RO	0x0	reserved
12	RW	0x0	pwm15_iomux_sel PWM15 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
11	RO	0x0	reserved
10	RW	0x0	pwm14_iomux_sel PWM14 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
9	RO	0x0	reserved
8	RW	0x0	pwm13_iomux_sel PWM13 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
7	RO	0x0	reserved
6	RW	0x0	pwm12_iomux_sel PWM12 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
5	RO	0x0	reserved
4	RW	0x0	pwm11_iomux_sel PWM11 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
3	RO	0x0	reserved
2	RW	0x0	pwm10_iomux_sel PWM10 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
1	RO	0x0	reserved
0	RW	0x0	pwm9_iomux_sel PWM9 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

GRF_IOFUNC_SEL3

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	uart4_iomux_sel UART4 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
13	RO	0x0	reserved
12	RW	0x0	uart3_iomux_sel UART3 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

Bit	Attr	Reset Value	Description
11:10	RW	0x0	uart2_iomux_sel UART2 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10: USB3_OTG uart mux 2'b11: USB2_Host uart mux
9	RO	0x0	reserved
8	RW	0x0	uart1_iomux_sel UART1 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
7	RO	0x0	reserved
6	RW	0x0	spi3_iomux_sel SPI3 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
5	RO	0x0	reserved
4	RW	0x0	spi2_iomux_sel SPI2 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
3	RO	0x0	reserved
2	RW	0x0	spi1_iomux_sel SPI1 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
1	RO	0x0	reserved
0	RW	0x0	spi0_iomux_sel SPI0 IO mux selection 'b0:M0 mux solution 1'b1:M1 mux solution

GRF_IOFUNC_SEL4

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	i2s3_iomux_sel I2S3 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
13	RO	0x0	reserved
12	RW	0x0	i2s2_iomux_sel I2S2 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
11:10	RW	0x0	i2s1_iomux_sel I2S1 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x0	uart9_iomux_sel UART9 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved
7	RO	0x0	reserved
6	RW	0x0	uart8_iomux_sel UART8 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
5:4	RW	0x0	uart7_iomux_sel UART7 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved
3	RO	0x0	reserved
2	RW	0x0	uart6_iomux_sel UART6 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution
1	RO	0x0	reserved
0	RW	0x0	uart5_iomux_sel UART5 IO mux selection 1'b0:M0 mux solution 1'b1:M1 mux solution

GRF_IOFUNC_SEL5

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sata2_cp_del_sel sata2_cp_det select 1'b0: the value of sata2_cp_det is 1'b0 1'b1: the value of sata2_cp_det is from IO
14	RW	0x0	sata1_cp_del_sel sata1_cp_det select 1'b0: the value of sata1_cp_det is 1'b0 1'b1: the value of sata1_cp_det is from IO
13	RW	0x0	sata0_cp_del_sel sata0_cp_det select 1'b0: the value of sata0_cp_det is 1'b0 1'b1: the value of sata0_cp_det is from IO
12	RW	0x0	sata2_mp_switch_sel sata2_mp_switch select 1'b0: the value of sata2_mp_switch is 1'b0 1'b1: the value of sata2_mp_switch is from IO
11	RW	0x0	sata1_mp_switch_sel sata1_mp_switch select 1'b0: the value of sata1_mp_switch is 1'b0 1'b1: the value of sata1_mp_switch is from IO

Bit	Attr	Reset Value	Description
10	RW	0x0	sata0_mp_switch_sel sata0_mp_switch select 1'b0: the value of sata0_mp_switch is 1'b0 1'b1: the value of sata0_mp_switch is from IO
9:8	RW	0x0	sata_cp_pod_sel sata_cp_pod source select 2'b00: From sata0 2'b01: From sata1 2'b10: From sata2 2'b11: Reserved
7:6	RW	0x0	pcie30x2_iomux_sel PCIe30X2 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved
5:4	RW	0x0	pcie30x1_iomux_sel PCIe30X1 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved
3:2	RW	0x0	pcie20_iomux_sel PCIe20 IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved
1:0	RW	0x0	pdm_iomux_sel PDM IO mux selection 2'b00:M0 mux solution 2'b01:M1 mux solution 2'b10:M2 mux solution 2'b11: Reserved

GRF_VI_CON0

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	dvp_clk_inv_sel 1'b1: Clock is inverted for dvp clock 1'b0: Clock is not inverted for dvp clock
11	RW	0x0	csiphy_clk1_inv_selection 1'b0: Disable clock inverter for clock lane1 1'b1: Enable clock inverter for clock lane1
10	RW	0x0	csiphy_clklane1_en 1'b0: Disable clock1 lane 1'b1: Enable clock1 lane
9	RW	0x0	csiphy_clk0_inv_selection 1'b0: Disable clock inverter for clock lane0 1'b1: Enable clock inverter for clock lane0

Bit	Attr	Reset Value	Description
8	RW	0x0	csiphy_clklane0_en 1'b0: Disable clock0 lane 1'b1: Enable clock0 lane
7	RW	0x0	csiphy_datalane_en_3 1'b1: Enable csiphy lane3 1'b0: Disable csiphy_lane3
6	RW	0x0	csiphy_datalane_en_2 1'b1: Enable csiphy lane2 1'b0: Disable csiphy_lane2
5	RW	0x0	csiphy_datalane_en_1 1'b1: Enable csiphy lane1 1'b0: Disable csiphy_lane1
4	RW	0x0	csiphy_datalane_en_0 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
3	RW	0x0	csiphy_forcerxmode_3 1'b1: Force to rx mode of lane3; 1'b0: Disable force control
2	RW	0x0	csiphy_forcerxmode_2 1'b1: Force to rx mode of lane2; 1'b0: Disable force control
1	RW	0x0	csiphy_forcerxmode_1 1'b1: Force to rx mode of lane1; 1'b0: Disable force control
0	RW	0x0	csiphy_forcerxmode_0 1'b1: Force to rx mode od lane0; 1'b0: Disable force control

GRF_VI_CON1

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	isp_width ISP interface isp_width control
13	RW	0x0	isp_shutter_trig ISP interface shutter_trig control
12	RW	0x0	isp_csiphy_sel isp data lane select when dphy split mode 1'b0: lane0/lane1 1'b1: lane2/lane3
11	RW	0x0	vicap_csiphy_sel vicap data lane select when dphy split mode 1'b0: lane0/lane1 1'b1: lane2/lane3
10	RO	0x0	reserved
9	RW	0x0	cif_datapath pixel input data path selection for cif controller: 1'b0: Single-edge sampling for DVP signals 1'b1: Dual-edge sampling for DVP signals.
8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	csiphy_mode_sel 1'b0: Full mode(one dphy with 4 lanes) ; 1'b1: Split mode(two dphy each with 2 lanes).
6:0	RW	0x00	cif_clk_delaynum The delay value of dvp path clock.This register is valid only when cif_datapath(SYS_GRF_VI_CON1[9]) is set to high

GRF_VI_STATUS0

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	csiphy_errcontentionlp1_0 LP1 Contention error status
9	RW	0x0	csiphy_errcontentionlp0_0 LP0 Contention error status
8	RW	0x0	csiphy_rxskewcalhs_3 Lane3 high-speed receive skew calibration status
7	RW	0x0	csiphy_rxskewcalhs_2 Lane2 high-speed receive skew calibration status
6	RW	0x0	csiphy_rxskewcalhs_1 Lane1 high-speed receive skew calibration status
5	RW	0x0	csiphy_rxskewcalhs_0 Lane0 high-speed receive skew calibration status
4	RW	0x0	csiphy_direction Transmit/Receive direction. 1'b0: transmit mode 1'b1: receive mode
3	RW	0x0	csiphy_ulpsactivenot_3 Lane3 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
2	RW	0x0	csiphy_ulpsactivenot_2 Lane2 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
1	RW	0x0	csiphy_ulpsactivenot_1 Lane1 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
0	RW	0x0	csiphy_ulpsactivenot_0 Lane0 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state

GRF_VO_CON0

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x1	hdmiphy_i2c_jtagz hdmiphy configuration port select 1'b0: JTAG 1'b1: I2C
14:11	RO	0x0	reserved
10	RW	0x0	dsi1_dpiupdatecfg DSI1 controller dpiupdatecfg control
9	RW	0x0	dsi1_dpicolorm DSI1 controller dpicolorm configuration 1'b0: normal color modle 1'b1: reduced color mode
8	RW	0x0	dsi1_dpishutdn DSI1 Controller dpishutdn configuration 1'b0: enable display 1'b1: shutdown the disaplay
7:6	RO	0x0	reserved
5:4	RW	0x0	lvdsformat_lvds0_select 2'b00: VESA 24bit 2'b01: JEIDA 24bit 2'b10: JEIDA 18bit 2'b11: VESA 18bit
3	RW	0x0	lvdsformat_lvds0_msbsel 1'b0: LSB 1'b1:MSB
2	RW	0x0	dsi0_dpiupdatecfg DSI0 controller dpiupdatecfg control
1	RW	0x0	dsi0_dpicolorm DSI0 Controller dpicolorm configuration 1'b0: normal color modle 1'b1: reduced color mode
0	RW	0x0	dsi0_dpishutdn DSI0 Controller dpishutdn configuration 1'b0: enable display 1'b1: shutdown the disaplay

GRF_VO_CON1

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hdmi_sdain_msk HDMI sdain mask control 1'b1: Signal function enable 1'b0: Signal function disable
14	RW	0x0	hdmi_sclin_msk HDMI sclin mask control 1'b1: Signal function enable 1'b0: Signal function disable
13	RW	0x0	hdmi_cecin_msk HDMI cecin mask control 1'b1: Signal function disable 1'b0: Signal function enable

Bit	Attr	Reset Value	Description
12:7	RO	0x00	reserved
6	RW	0x0	rgb_bypass 1'b1: Bypass data sync 1'b0: Use data sync
5	RW	0x0	bt1120_bypass 1'b0: Use data sync 1'b1: Bypass data sync
4	RW	0x0	bt656_bypass 1'b0: Use data sync 1'b1: Bypass data sync
3	RW	0x0	RGB_dclk_inv_sel 1'b0: Normal clock. 1'b1: rbg_dclk is inverted
2	RW	0x0	bt1120_clk_inv_sel 1'b0: Normal clock. 1'b1: bt1120 Clock is inverted
1	RW	0x0	bt656_clk_inv_sel 1'b0: Normal clock. 1'b1: bt656 Clock is inverted
0	RW	0x0	ebc_clk_inv_sel 1'b0: Normal clock. 1'b1: ebc clock is inverted

GRF_VO_CON2

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dsiphy0_txskewcalhs_3 Request to transmit skew calibration on lane3. 1'b1: Request; 1'b0: Idle
14	RW	0x0	dsiphy0_txskewcalhs_2 Request to transmit skew calibration on lane2. 1'b1: Request; 1'b0: Idle
13	RW	0x0	dsiphy0_txskewcalhs_1 Request to transmit skew calibration on lane1. 1'b1: Request; 1'b0: Idle
12	RW	0x0	dsiphy0_txskewcalhs_0 Request to transmit skew calibration on lane0. 1'b1: Request; 1'b0: Idle
11	RW	0x0	dsiphy0_txskewcalhs_ck Request to transmit skew calibration on clock lane. 1'b1: Request; 1'b4: Idle
10	RO	0x0	reserved
9	RW	0x0	lvds0_dclk_inv_sel 1'b0: Normal clock 1'b1: Inverted clock

Bit	Attr	Reset Value	Description
8	RW	0x0	lvds0_dclk_div2_sel lvdsdclk divided by 2 selection 1'b0: clock bypass 1'b1: clock divided by 2
7	RW	0x0	dsiphy0_lane3_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsiphy0_lane2_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
5	RW	0x0	dsiphy0_lane1_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsiphy0_lane0_frctxstpm Force DSI TX PHY lane0 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	dsiphy0_lane0_turndisable Disable Turn-around. This signal is used to prevent Lane from going into transmit mode, even if it observes a turn-around request on the Lane interconnect
1	RW	0x0	dsiphy0_lvds_mode DSI/LVDS combo PHY0 mode control 1'b0: dsi mode 1'b1: lvds mode
0	RW	0x0	dsiphy0_forcerxmode Force DSI TX PHY0 lane module into Receive mode, wait for stop state 1'b0: Disable 1'b1: Enable

GRF_MAC0_CON0

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	gmac0_clk_rx_dl_cfg gmac0_clk_rx clock delay line control
7:0	RW	0x00	gmac0_clk_tx_dl_cfg gmac0_clk_tx clock delay line control

GRF_MAC0_CON1

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gmac0_qsgmii_mode gmac0_qsgmii_mode 1'b0: RMII and RGMII mode select 1'b1: SGMII and QSGMII mode select
6:4	RW	0x0	gmac0_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
3	RW	0x0	gmac0_flowctrl GMAC0 transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frame in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
2	RW	0x0	gmac0_mac_speed MAC speed 1'b1:100-Mbps 1'b0:10-Mbps
1	RW	0x0	gmac0_rxclk_dly_ena RGMII RX clock delayline enable 1'b1: Enable 1'b0: Disable
0	RW	0x0	gmac0_txclk_dly_ena RGMII TX clock delayline enable 1'b1: Enable 1'b0: Disable

GRF_MAC1_CON0

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	gmac1_clk_rx_dl_cfg RGMII RX clock delayline enable 1'b1: Enable 1'b0: Disable
7:0	RW	0x00	gmac1_clk_tx_dl_cfg RGMII TX clock delayline enable 1'b1: Enable 1'b0: Disable

GRF_MAC1_CON1

Address: Operational Base + offset (0x038C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gmac1_qsgmii_mode gmac1_qsgmii_mode 1'b0: RMII and RGMII mode select 1'b1: SGMII and QSGMII mode select
6:4	RW	0x0	gmac1_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
3	RW	0x0	gmac1_flowctrl GMAC1 transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frame in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
2	RW	0x0	gmac1_mac_speed MAC speed 1'b1:100-Mbps 1'b0:10-Mbps
1	RW	0x0	gmac1_rxclk_dly_ena RGMII RX clock delayline enable 1'b1: Enable 1'b0: Disable
0	RW	0x0	gmac1_txclk_dly_ena RGMII TX clock delayline enable 1'b1: Enable 1'b0: Disable

GRF_BIU_CON0

Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	top_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
14	RW	0x0	top_fwd_ddrc_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
13	RW	0x0	sf_req_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

Bit	Attr	Reset Value	Description
12	RW	0x0	rga_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
11	RW	0x0	pipe_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
10	RW	0x0	php_req_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
9	RW	0x0	peri_fwd_sf_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
8	RW	0x0	peri_fwd_php_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
7	RW	0x0	peri_req_ga_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
6	RW	0x0	peri_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
5	RW	0x0	npu_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
4	RW	0x0	gpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
3	RW	0x0	gic_fwd_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
2	RW	0x0	cpu_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
1	RW	0x0	cpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
0	RW	0x0	bus_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

GRF_BIU_CON1

Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	top_fwd_pipe_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
14	RW	0x0	top_fwd_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
13	RW	0x0	top_fwd_npu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
12	RW	0x0	top_fwd_bus_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
11	RW	0x0	top_fwd_venc_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
10	RW	0x0	top_fwd_vdec_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
9	RW	0x0	top_fwd_gpu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
8	RW	0x0	top_fwd_vo_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
7	RW	0x0	top_fwd_vi_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
6	RW	0x0	top_fwd_usb_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
5	RW	0x0	topal_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
4	RW	0x0	topahvo_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

Bit	Attr	Reset Value	Description
3	RW	0x0	topahpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
2	RW	0x0	top_fwd_vpu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
1	RW	0x0	top_fwd_rga_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
0	RW	0x0	top_fwd_pmu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

GRF_BIU_CON2

Address: Operational Base + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	vpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
5	RW	0x0	vo_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
4	RW	0x0	vi_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
3	RW	0x0	venc_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
2	RW	0x0	vdec_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
1	RW	0x0	vdec_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
0	RW	0x0	usb_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

GRF_GIC_CON0

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xfd40	gicd_page_offset gicd page offset address control

GRF_GIC_CON1

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xfd45	its_transr_page_offset used to set the page address of the GITS_TRANSLATER register of GIC

GRF_GIC_CON2

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	gic2core_pwrq_permit_deny_sar GIC gic2core_pwrq_permit_deny_sar bit control
4	RW	0x0	sample_req This 4-phase handshake provides a hardware mechanism to snapshot the PMU counters and has the same effect as writing to the GICP_CAPR register
3:0	RW	0xf	cpu_active cpu_active port control of GIC

GRF_GPU_CON0

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:2	RW	0x0	stripping_granule Controls memory striping in level two cache. Memory accesses are striped across the cache slices. For each memory transaction, its Physical Address(PA) is used to select the Level 2 Cache (L2C) slice and the external ACE port 3'b000: 4KB 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1KB 3'b101: 2KB

Bit	Attr	Reset Value	Description
1	RW	0x0	niden gpuniden port control 1'b0: Noninvasive debug disable 1'b1: Noninvasive debug enable
0	RW	0x0	dbgen gpudbgen port control 1'b0: Debug disable 1'b1: Debug enable

GRF_GPU_CON1

Address: Operational Base + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	gpu_texfmtenable Compressed texture format support control

GRF_CPU_CON0

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	adb400_pwrq_permit_deny This input determines whether the ADB-400 can enter the Q_DENIED state insate of Q_STOPPED sate
12	RO	0x0	reserved
11	RW	0x0	evenctireq Event input for processor wake-up from WFE state. This pin must be asserted for at least one CLKIN clock cycles. When this signal is asserted, it acts as WFE wake-up event to all the cores in the cluster
10	RW	0x0	eventoack Set this bit to clear the evento rising edge state
9	RW	0x1	dbgconnected A debugger is connected and so the DebugBlock can be accessed on boot
8	RW	0x1	pmusnapshotreq Request for a snapshot of the PMU counters. Once asserted, this signal must remain HIGH until PMUSNAPSHOTACK is asserted. It must not be reasserted until PMUSNAPSHOTACK is deasserted
7:4	RW	0x0	cfgte Enable T32 exception. It sets the initial value of the TE bit in the SCTLR and HSCTLR register. Each bit is defined below. 1'b0: TE bit is low 1'b1: TE bit is high These bits are sampled only during reset of the core. Tie low for the ARM instruction set for exception handling. Tie high for the Thumb instruction set for exception handling. Only change it when the core is in the reset state

Bit	Attr	Reset Value	Description
3:0	RW	0x0	cfgend Endianness configuration at reset. It sets the initial value of the EE bits in the SCTLR, HSCTLR, SCTLR_EL1, SCTLR_EL2, and SCTLR_EL3 registers. Each bit is defined below. 1'b0: EE bit is low 1'b1: EE bit is high These bits are sampled only during reset of the core. Tie high for big-endian data during exception handling. Tie it low for little-endian data during exception handling. Only change it when the cores are in the state

GRF_CPU_STATUS0

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	dormantstate Active-HIGH status to indicate that none of the protocol engines are selected and that the DP is in dormant state
21:18	RW	0x0	jtagstate JTAG State. Shows the current JTAG TAP state machine state
17:14	RW	0x0	jtagir JTAG Instruction Registe
13	RW	0x0	jtagactive JTAG Active. Output is driven HIGH when the Debug Port is operating using the JTAG protocol
12	RW	0x0	swactive Serial Wire Active. Output is driven HIGH when the Debug Port is operating using the Serial Wire protocol
11	RW	0x0	eventoreq Event output request for wake-up, triggered by SEV instruction
10	RW	0x0	eventiack Event input request acknowledge
9	RO	0x0	reserved
8	RW	0x0	pmusnapshotack Acknowledge a snapshot request
7:4	RW	0x0	coreinstrret Indicates that a core has retired at least one instruction recently
3:0	RW	0x0	coreinstrun Indicates that a core is in a running state (powered up and not in WFI or WFE low-power states)

GRF_SOC_CON0

Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart8_rts_inv uart8_rts polarity selection 1'b0: Low asserted 1'b1: High asserted

Bit	Attr	Reset Value	Description
14	RW	0x0	uart8_cts_inv uart8_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
13	RW	0x0	uart7_rts_inv uart7_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
12	RW	0x0	uart7_cts_inv uart7_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
11	RW	0x0	uart6_rts_inv uart6_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
10	RW	0x0	uart6_cts_inv uart6_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
9	RW	0x0	uart5_rts_inv uart5_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
8	RW	0x0	uart5_cts_inv uart5_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
7	RW	0x0	uart4_rts_inv uart4_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
6	RW	0x0	uart4_cts_inv uart4_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
5	RW	0x0	uart3_rts_inv uart3_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
4	RW	0x0	uart3_cts_inv uart3_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
3	RW	0x0	uart2_rts_inv uart2_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
2	RW	0x0	uart2_cts_inv uart2_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

Bit	Attr	Reset Value	Description
1	RW	0x0	uart1_rts_inv uart1_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
0	RW	0x0	uart1_cts_inv uart1_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

GRF_SOC_CON1

Address: Operational Base + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	optcns_lock otpc-non-secure lock signal
12	RW	0x0	otpcs_lock otpc-secure lock signal
11	RW	0x0	sdmmc2_buffer_en sdmmc2_buffer enable 1'b0: select sdmmc2 as sdmmc2 io 1'b1: select sdmmc2_buffer as sdmmc2 io
10	RW	0x0	sdmmc1_buffer_en sdmmc1_buffer enable 1'b0: select sdmmc1 as sdmmc1 io 1'b1: select sdmmc1_buffer as sdmmc1 io
9	RW	0x0	sdmmc0_buffer_en sdmmc0_buffer enable 1'b0: select sdmmc0 as sdmmc0 io 1'b1: select sdmmc0_buffer as sdmmc0 io
8	RW	0x1	pcie_addr_extend pcie slave address extend control 1'b0: address of 0xF0000000~0xFC000000 is config address 1'b1: address of 0xF0000000~0xFC000000 is DDR address
7	RW	0x1	i2s3_sclk_sel i2s3 sclk to GPIO source slection 1'b0: i2s3_sclk_rx 1'b1: i2s3_sclk_tx
6	RW	0x0	i2s3_lrck_sel i2s3 lrck to GPIO source slection 1'b0: i2s3_lrck_rx 1'b1: i2s3_lrck_tx
5	RW	0x0	i2s1_mclk_sel i2s1 mclk to GPIO source slection 1'b0: i2s1_mclk_rx 1'b1: i2s1_mclk_tx
4	RW	0x0	wdt_ns_pause_en Non-Secure wdt pause enable
3	RW	0x1	emmc_clkstable EMMC clkstable bit control

Bit	Attr	Reset Value	Description
2	RW	0x0	emmc_clkbypass EMMC clkbypass control 1'b0: Disable 1'b1: Enable
1	RW	0x0	uart9_rts_inv uart9_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
0	RW	0x0	uart9_cts_inv uart9_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

GRF_SOC_CON2

Address: Operational Base + offset (0x0508)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	i2s3_mclk_sel i2s3 mclk source selection 1'b0: i2s3_mclkout_rx 1'b1: i2s3_mclkout_tx
14	RW	0x0	acdcdig_i2c_tran_req acdcdig using i2c request
13	RW	0x0	acdcdig_i2s_active i2s3 usage selection 1'b0: Used as IO with external I2S bus device 1'b1: Used to comunucatied with acdcdig IP
12	RO	0x0	reserved
11	RW	0x0	bus_pwr_idle_req bus biu idle request
10	RW	0x0	pmu_pwr_idle_req pmubiu idle request
9:6	RO	0x0	reserved
5	RW	0x1	scr_det_inv_sel Smart card detect port invert enable 1'b0: Not inverted 1'b1: Inverted
4	RW	0x0	wdtns_glb_reset_en non-secure watch dog reset enable 1'b0: Disable reset system 1'b1: Enable reset system
3	RW	0x0	i2s3_mclk_oe i2s2 mclk source selection 1'b0: from external chip 1'b1: from cru
2	RW	0x0	i2s2_mclk_oe i2s2 mclk source selection 1'b0: from external chip 1'b1: from cru

Bit	Attr	Reset Value	Description
1	RW	0x0	i2s1_mclk_tx_oe i2s1 mclk_tx source selection 1'b0: from external chip 1'b1: from cru
0	RW	0x0	i2s1_mclk_rx_oe i2s1 mclk_rx source selection 1'b0: from external chip 1'b1: from cru

GRF_SOC_CON3

Address: Operational Base + offset (0x050C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mcu_ahb2axi_d_buf_flush MCU ahb2axi d_buf flush control
14	RW	0x0	mcu_ahb2axi_i_buf_flush MCU ahb2axi i_buf flush control
13	RW	0x0	mcu_sel_axi Both AHB and AXI bus are provided for MCU to access system register and memory 1'b0: MCU use AHB bus 1'b1: MCU use AXI bus
12	RW	0x0	mcu_soft_irq MCU soft interrupt request
11:9	RO	0x0	reserved
8	RW	0x0	hdcp_uart_en hdcpuart interface enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	sdmmc_buf_clk_inv_sel sdmmc_buffer clock inv select 1'b0: Disable 1'b1: Enable
6	RW	0x0	sdmmc_buffer_en sdmmc_buffer enable 1'b0: Disable 1'b1: Enable
5	RO	0x0	reserved
4:0	RW	0x00	sdmmc_buffer_wr_thresh SDMMC_BUFFER block write data threshhold control, when the valide data entry is more than this value, SDMMC_BUFFER will send data to GPIO.

GRF_SOC_CON4

Address: Operational Base + offset (0x0510)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mcu_boot_addr MCU boot address

GRF_SOC_CON5

Address: Operational Base + offset (0x0514)

Bit	Attr	Reset Value	Description
31:0	RW	0x0003a980	sdcard_dectn_dly Delay counter setting after sdcard plug out. Count by 24M clock

GRF_SOC_CON6

Address: Operational Base + offset (0x0518)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	gmac1_txclkm1_inv_en GMAC1 tx_clk_m1 inveter select 1'b0: Without clock inverter 1'b1: With clock inverter
14	RW	0x0	gmac1_txclkm0_inv_en GMAC1 tx_clk_m0 inveter select 1'b0: Without clock inverter 1'b1: With clock inverter
13	RW	0x0	gmac0_txclk_inv_en GMAC0 tx_clkinveter select 1'b0: Without clock inverter 1'b1: With clock inverter
12	RW	0x0	ppll_clk_sel PPLL clock mux select 1'b0: with level shifter 1'b1: without level shifter
11	RW	0x0	hpll_clk_sel HPLL clock mux select 1'b0: with level shifter 1'b1: without level shifter
10	RW	0x0	pcie30phy_prb_io_en pcie30 phy probe io enable register 1'b0 acdcdig_d2a_Dac_data to GPIO1A7 and GPIO1B0 1'b1: pcie30phy_dtb_out to GPIO1A7 and GPIO1B0
9	RW	0x0	ahb2axi_d_rd_clean ahb2axi D-bus read clean control register
8	RW	0x0	ahb2axi_i_rd_clean ahb2axi I-bus read clean control register
7:0	RW	0xff	ahb2axi_d_timeout ahb2axi D-Bus write time out control register, when time out, the data in write buffer will be flushed.

GRF_SOC_STATUS0

Address: Operational Base + offset (0x0580)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	wfi_halted wfi_halted status from MCU

Bit	Attr	Reset Value	Description
26	RW	0x0	otp_s_user_busy otpc-secuure USER busy
25	RW	0x0	otp_s_sbpi_busy otpc-secuure SBPI busy
24	RW	0x0	otpcns_user_busy otpc-non-secuure USER busy
23	RW	0x0	otpcns_sbpi_busy otpc-non-secuure SBPI busy
22	RW	0x0	pmu_pwr_idle_ack PMU NIU idle acknowledge status
21	RW	0x0	pmu_pwr_idle PMU NIU idle status
20	RW	0x0	buf_flush_ack_d buf_flush_ack_i
19	RW	0x0	buf_flush_ack_i buf_flush_ack_i
18	RW	0x0	scramble_shift_ready ddr_scramble seed shift ready status
17	RW	0x0	vop_dma_finish voprawb_dma_finish status
16	RW	0x0	timer_en_status5 timer5_en status
15	RW	0x0	timer_en_status4 timer4_en status
14	RW	0x0	timer_en_status3 timer3_en status
13	RW	0x0	timer_en_status2 timer2_en status
12	RW	0x0	timer_en_status1 timer1_en status
11	RW	0x0	timer_en_status0 timer0_en status
10	RW	0x0	ddr_cmd_pll_lock DDR CMDPLL lock status
9	RW	0x0	acdcdig_i2c_tran_ack acknowledge status signal to acdcdig IP use i2c request
8	RW	0x0	mpll_lock MPLL lock status
7	RW	0x0	hpll_lock HPLL lock status
6	RW	0x0	vpll_lock VPLL lock status
5	RW	0x0	npll_lock NPLL lock status
4	RW	0x0	ppll_lock PPLL lock status
3	RW	0x0	gpll_lock GPLL lock status
2	RW	0x0	cpll_lock CPLL lock status
1	RW	0x0	dpll_lock DPLL lock status
0	RW	0x0	apll_lock APLL lock status

GRF_RAM_CON

Address: Operational Base + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	rom_trb ROM memory timing adjustment setting for debug purpose
13:12	RW	0x1	rom_rtsel ROM memory timing adjustment setting for debug purpose
11:10	RW	0x1	rom_ptsel ROM memory timing adjustment setting for debug purpose
9:8	RW	0x0	dpra_wtsel DPRA memory timing adjustment setting for debug purpose 2'b00:Recommended setting with the optimized write margin 2'b01:Relaxed write margin setting, used for debugging purpose. 2'b10:More relaxed write margin setting, used for debugging purpose. 2'b11:Most relaxed write margin setting, used for debugging purpose.
7:6	RW	0x0	dpra_rtsel DPRA memory timing adjustment setting for debug purpose 2'b00: Recommended setting with the optimized read margin 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
5:4	RW	0x0	dpra_ptsel DPRA memory timing adjustment setting for debug purpose 2'b00: Recommended setting for internal clock skew of port A/B with the optimized design margin and timing 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose 2'b10: More relaxed setting for internal clock skew of port A/B used for debugging purpose 2'b11: Most relaxed setting for internal clock skew of port A/B used for debugging purpose
3:2	RW	0x0	spra_wtsel SPRA memory timing adjustment setting for debug purpose
1:0	RW	0x1	spra_rtsel SPRA memory timing adjustment setting for debug purpose

GRF_CORE_RAM_CON

Address: Operational Base + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	spra_slp SPRA memory sleep control 1'b0: sleep disable 1'b1: sleep enable
14:8	RO	0x00	reserved
7:6	RW	0x1	rtsel_cpu_dsu CPU DSU SPRA memory timing adjustment setting for debug purpose
5:4	RW	0x0	wtsel_cpu_dsu CPU DSU SPRA memory timing adjustment setting for debug purpose
3:2	RW	0x1	rtsel_cpu CPU SPRA memory timing adjustment setting for debug purpose
1:0	RW	0x0	wtsel_cpu CPU SPRA memory timing adjustment setting for debug purpose

GRF_TSADC_CON

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	tsadc_tsen x'bxxx(bits < 4), x'hxxxx(bits >= 4)
7	RO	0x0	reserved
6	RW	0x0	tsadc_ana_reg6 External voltage buffer control 0: disable voltage buffer 1: enable voltage buffer
5	RW	0x0	tsadc_ana_reg5 Temperature-related voltage filter bypass control 0: select filter 1: bypass filter
4	RW	0x0	tsadc_ana_reg4 Temperature-related voltage buffer control 0: disable voltage buffer 1: enable voltage buffer
3	RW	0x0	tsadc_ana_reg3 Temperature-related voltage control 0: select voltage 1 1: select voltage 2
2	RW	0x0	tsadc_ana_reg2 Bandgap voltage filter bypass control 0: select filter 1: bypass filter
1	RW	0x0	tsadc_ana_reg1 Bandgap voltage buffer control 0: disable voltage buffer and select AVDD as reference 1: enable voltage buffer and select bandgap voltage as reference
0	RW	0x0	tsadc_ana_reg0 Bandgap chopper enable control 0: disable chopper 1: enable chopper

GRF_SARADC_CON

Address: Operational Base + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0007	saradc_ana_reg Reserved

GRF_GPUPVTPLL_CON0

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:11	RW	0x0	gpu_pvtpll_clk_div_cnt gpupvtpll clock out divided nuber
10:8	RW	0x0	gpu_pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RW	0x00	gpu_pvtpll_ring_length_sel gpupvtpll delay cell element number control 3'b000: 10 3'b001: 20 3'b010: 30 3'b011: 40 3'b100: 50 3'b101: 60 3'b110: 70 3'b111: 80
2	RW	0x0	gpupvtpll_out_polar PVTPLL output polarity
1	RW	0x0	gpupvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	gpupvtpll_start Set high to start PVTPLL

GRF_GPUPVTPLL_CON1

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt pvtpll calculation counter

GRF_GPUPVTPLL_CON2

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gpu_pvtpll_threshold Threshold control for voltage adjustment

GRF_GPUPVTPLL_CON3

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gpu_pvtpll_ref_cnt pvtpll reference counter

GRF_NPUPVTPLL_CON0

Address: Operational Base + offset (0x0740)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:11	RW	0x0	gpu_pvtpll_clk_div_cnt gpupvtpll clock out divided nuber
10:8	RW	0x0	gpu_pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RW	0x00	gpu_pvtpll_ring_length_sel gpupvtpll delay cell element number control 3'b000: 10 3'b001: 20 3'b010: 30 3'b011: 40 3'b100: 50 3'b101: 60 3'b110: 70 3'b111: 80
2	RW	0x0	gpupvtpll_out_polar PVTPLL output polarity
1	RW	0x0	gpupvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	gpupvtpll_start Set high to start PVTPLL

GRF_NPUPVTPLL_CON1

Address: Operational Base + offset (0x0744)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt pvtpll calculation counter

GRF_NPUPVTPLL_CON2

Address: Operational Base + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gpu_pvtpll_threshold threshold control for voltage adjustment

GRF_NPUPVTPLL_CON3

Address: Operational Base + offset (0x074C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gpu_pvtpll_ref_cnt reference counter

GRF_CHIP_ID

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00003566	chip_id 32'h3566

GRF_GPIO1C5_DS

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x01	gpio1c5_ds GPIO1C5 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2A2_DS

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x01	gpio2a2_ds GPIO2A2 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO2B0_DS

Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x01	gpio2b0_ds GPIO2B0 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A0_DS

Address: Operational Base + offset (0x084C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x01	gpio3a0_ds GPIO3A0 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO3A6_DS

Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x01	gpio3a6_ds GPIO3A6 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_GPIO4A0_DS

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x01	gpio4a0_ds GPIO4A0 double bonding PAD Strength control,DS[11:6] 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GRF_DMAC0_CON0

Address: Operational Base + offset (0x0900)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma0_irq_boot_nonsec 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC0_CON1

Address: Operational Base + offset (0x0904)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma0_peri_ch_nonsec_15_0 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC0_CON2

Address: Operational Base + offset (0x0908)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma0_peri_ch_nonsec_31_16 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC0_CON3

Address: Operational Base + offset (0x090C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	dma0_manager_boot_nonsec 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC0_CON4

Address: Operational Base + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_uart_3_rx DMAC type of acknowledgement or request for UART_3 rx signals
13:12	RW	0x1	grf_type_uart_3_tx DMAC type of acknowledgement or request for UART_3 tx signals
11:10	RW	0x1	grf_type_uart_2_rx DMAC type of acknowledgement or request for UART_2 rx signals
9:8	RW	0x1	grf_type_uart_2_tx DMAC type of acknowledgement or request for UART_2 tx signals
7:6	RW	0x1	grf_type_uart_1_rx DMAC type of acknowledgement or request for UART_1 rx signals
5:4	RW	0x1	grf_type_uart_1_tx DMAC type of acknowledgement or request for UART_1 tx signals
3:2	RW	0x1	grf_type_uart_0_rx DMAC type of acknowledgement or request for UART_0 rx signals
1:0	RW	0x1	grf_type_uart_0_tx DMAC type of acknowledgement or request for UART_0 tx signals

GRF_DMAC0_CON5

Address: Operational Base + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_uart_7_rx DMAC type of acknowledgement or request for UART_7 rx signals
13:12	RW	0x1	grf_type_uart_7_tx DMAC type of acknowledgement or request for UART_7 tx signals
11:10	RW	0x1	grf_type_uart_6_rx DMAC type of acknowledgement or request for UART_6 rx signals
9:8	RW	0x1	grf_type_uart_6_tx DMAC type of acknowledgement or request for UART_6 tx signals
7:6	RW	0x1	grf_type_uart_5_rx DMAC type of acknowledgement or request for UART_5 rx signals
5:4	RW	0x1	grf_type_uart_5_tx DMAC type of acknowledgement or request for UART_5 tx signals
3:2	RW	0x1	grf_type_uart_4_rx DMAC type of acknowledgement or request for UART_4 rx signals

Bit	Attr	Reset Value	Description
1:0	RW	0x1	grf_type_uart_4_tx DMAC type of acknowledgement or request for UART_4 tx signals

GRF_DMAC0_CON6

Address: Operational Base + offset (0x0918)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_spi1_rx DMAC type of acknowledgement or request for SPI2 rx signals
13:12	RW	0x1	grf_type_spi1_tx DMAC type of acknowledgement or request for SPI2 tx signals
11:10	RW	0x1	grf_type_spi0_rx DMAC type of acknowledgement or request for SPI0 rx signals
9:8	RW	0x1	grf_type_spi0_tx DMAC type of acknowledgement or request for SPI0 tx signals
7:6	RW	0x1	grf_type_uart_9_rx DMAC type of acknowledgement or request for UART_9 rx signals
5:4	RW	0x1	grf_type_uart_9_tx DMAC type of acknowledgement or request for UART_9 tx signals
3:2	RW	0x1	grf_type_uart_8_rx DMAC type of acknowledgement or request for UART_8 rx signals
1:0	RW	0x1	grf_type_uart_8_tx DMAC type of acknowledgement or request for UART_8 tx signals

GRF_DMAC0_CON7

Address: Operational Base + offset (0x091C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_pwm3_tx DMAC type of acknowledgement or request for PWM3 tx signals
13:12	RW	0x1	grf_type_pwm2_tx DMAC type of acknowledgement or request for PWM2 tx signals
11:10	RW	0x1	grf_type_pwm1_tx DMAC type of acknowledgement or request for PWM1 tx signals
9:8	RW	0x1	grf_type_pwm0_tx DMAC type of acknowledgement or request for PWM0 tx signals
7:6	RW	0x1	grf_type_spi3_rx DMAC type of acknowledgement or request for UART_9 rx signals
5:4	RW	0x1	grf_type_spi3_tx DMAC type of acknowledgement or request for UART_9 tx signals
3:2	RW	0x1	grf_type_spi2_rx DMAC type of acknowledgement or request for UART_8 rx signals
1:0	RW	0x1	grf_type_spi2_tx DMAC type of acknowledgement or request for UART_8 tx signals

GRF_DMAC0_CON8

Address: Operational Base + offset (0x0920)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0x0000	grf_dma0_req_modify_dis dma0 peri channel request mode. bit0-15 correspond to ch0-15 1'b0 : Request valid only when last ack is finish 1'b1 : Request directly from peri device

GRF_DMAC0_CON9

Address: Operational Base + offset (0x0924)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0x0000	grf_dma0_req_modify_dis dma0 peri channel request mode. bit0-15 correspond to ch16-31 1'b0 : Request valid only when last ack is finish 1'b1 : Request directly from peri device

GRF_DMAC1_CON0

Address: Operational Base + offset (0x0940)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma1_irq_boot_nonsec 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC1_CON1

Address: Operational Base + offset (0x0944)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma1_peri_ch_nonsec_15_0 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC1_CON2

Address: Operational Base + offset (0x0948)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0xffff	dma1_peri_ch_nonsec_31_16 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC1_CON3

Address: Operational Base + offset (0x094C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	dma1_manager_boot_nonsec 1'b0 : Secure 1'b1 : Non-sercure

GRF_DMAC1_CON4

Address: Operational Base + offset (0x0950)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_i2s3_rx DMAC type of acknowledgement or request for CAN2 tx signals
13:12	RW	0x1	grf_type_i2s3_tx DMAC type of acknowledgement or request for CAN1 rx signals
11:10	RW	0x1	grf_type_i2s2_rx DMAC type of acknowledgement or request for CAN1 tx signals
9:8	RW	0x1	grf_type_i2s2_tx DMAC type of acknowledgement or request for CAN0 rx signals
7:6	RW	0x1	grf_type_i2s1_rx DMAC type of acknowledgement or request for CAN0 tx signals
5:4	RW	0x1	grf_type_i2s1_tx DMAC type of acknowledgement or request for SDMMC_BUFFER signals
3:2	RW	0x1	grf_type_spdif DMAC type of acknowledgement or request for PDM signals
1:0	RW	0x1	grf_type_i2s0_rx DMAC type of acknowledgement or request for AUPWN signals

GRF_DMAC1_CON5

Address: Operational Base + offset (0x0954)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x1	grf_type_can1_rx DMAC type of acknowledgement or request for CAN2 rx signals

GRF_DMAC1_CON6

Address: Operational Base + offset (0x0958)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:14	RW	0x1	grf_type_can2_tx DMAC type of acknowledgement or request for SPI2 rx signals

Bit	Attr	Reset Value	Description
13:12	RW	0x1	grf_type_can1_rx DMAC type of acknowledgement or request for SPI2 tx signals
11:10	RW	0x1	grf_type_can1_tx DMAC type of acknowledgement or request for SPI0 rx signals
9:8	RW	0x1	grf_type_can0_rx DMAC type of acknowledgement or request for SPI0 tx signals
7:6	RW	0x1	grf_type_can0_tx DMAC type of acknowledgement or request for UART_9 rx signals
5:4	RW	0x1	grf_type_sdmmc_buffer DMAC type of acknowledgement or request for UART_9 tx signals
3:2	RW	0x1	grf_type_pdm DMAC type of acknowledgement or request for UART_8 rx signals
1:0	RW	0x1	grf_type_audpwm DMAC type of acknowledgement or request for UART_8 tx signals

GRF_DMAC1_CON7

Address: Operational Base + offset (0x095C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x1	grf_type_can2_rx DMAC type of acknowledgement or request for UART_8 tx signals

GRF_DMAC1_CON8

Address: Operational Base + offset (0x0960)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0x0000	grf_dma1_req_modify_dis dma1 peri channel request mode. bit0-15 correspond to ch0-15 1'b0 : Request valid only when last ack is finish 1'b1 : Request directly from peri device

GRF_DMAC1_CON9

Address: Operational Base + offset (0x0964)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0 :Write access disable 1'b1 : Write access enable
15:0	RW	0x0000	grf_dma1_req_modify_dis dma1 peri channel request mode. bit0-15 correspond to ch16-31 1'b0 : Request valid only when last ack is finish 1'b1 : Request directly from peri device

3.8 PIPE_PHY Register Description

3.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PIPE_PHY_GRF_PIPE_CON0	0x0000	W	0x00000110	PCIe_USB3 PHY configuration register0
PIPE_PHY_GRF_PIPE_CON1	0x0004	W	0x00000000	PCIe_USB3 PHY configuration register1
PIPE_PHY_GRF_PIPE_CON2	0x0008	W	0x00009401	PCIe_USB3 PHY configuration register2
PIPE_PHY_GRF_PIPE_CON3	0x000C	W	0x00000402	PCIe_USB3 PHY configuration register3
PIPE_PHY_GRF_PIPE_STATUS1	0x0034	W	0x00000000	PCIe_USB3 PHY status register1
PIPE_PHY_GRF_LFPS_DET_CON	0x0080	W	0x00000009	
PIPE_PHY_GRF_PHY_INT_EN	0x00A0	W	0x00000000	
PIPE_PHY_GRF_PHY_INT_STATUS	0x00A4	W	0x00000000	

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.8.2 Detail Registers Description

PIPE_PHY_GRF_PIPE_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pipe_rxstandby SATA Mode: Controls whether the PHY RX is active when the PHY is in any power state with PCLK on. RX_STANDBY is ignored when the PHY is in any power state where the high speed receiver is always off. 0 : Active 1 : Standby PCIE Mode: Controls whether the PHY RX is active when the PHY is in P0 or P0s. RX_STANDBY is ignored when the PHY is in P1 or P2 0 : Active 1 : Standby Only used in SATA and PCIE mode. USB3.0 mode should be tied to 1'b0
13	RW	0x0	pipe_rxelecidle_disable Indicates receiver detection of an electrical idle. When deasserted with the PHY in P2 (PCIE Mode), indicates a detection of beacon, while indicate exit from electrical idle in other power states in PCIE mode In USB3.0 mode, it indicates the detection of LFPS. In SATA mode, it indicates if there is no data/OOB received

Bit	Attr	Reset Value	Description
12	RW	0x0	pipe_rxterm Control presence of receiver terminations: 0 : Termination removed 1 : Termination present Only used in USB3.0 mode , PCIE and USB mode should be tied to 1'b1
11	RW	0x0	pipe_bypass_codec PCIE Mode, USB Mode, and SATA Mode: Controls whether the PHY performs 8b/10b encode and decode. 0 : 8b/10b encode/decode performed normally by the PHY. 1 : 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2'b01 It should be tie to 1'b1 in QSGMII mode
10	RW	0x0	pipe_ebuffmode RX Elasticity Buffer operating mode selection 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode In SATA and USB3.0 mode, when RX elastic buffer is operating at nominal empty buffer mode, RX_DATA_VALID is de-asserted when elastic buffer is empty and no data isavailable. In PCIE mode, only nominal half-full EBUF mode is supported
9	RW	0x0	pipe_l1sub_entreq PCIE Mode: L1 sub-state entry request signal in PCIE mode. When set to high, it instructs PHY to do power transition to L1 sub-state SATA Mode: When set to high, it will be power down PLL. This signal could connected to the L1 sub-state enable/request signal from controller Only used in PCIE and SATA mode, USB mode should be tied to 1'b0
8	RW	0x1	pipe_mac_pclkreq_n PCIE common clock request signal in PCIE mode. The signal shall be high and CKREF_SRC[1:0] is set to 2'b10 when CKREFP/N and PCI_100M_CLK output from PHY is used for PCIE system with common clock Note: Details refer to CKREFP/N and PCI_100M_CLK. Only used in PCIE Mode , USB and SATA Mode should be tied to 1'b0
7:6	RW	0x0	pipe_powerdown Power up or power down status control of Transceiver

Bit	Attr	Reset Value	Description
5:4	RW	0x1	pipe_rate phy bit rate: PCIe Mode 2'b00: 2.5Gbps 2'b01: 5.0Gbps 2'b10: Reserved 2'b11: Reserved USB3.0 Mode 2'b00: 5Gbps 2'b01, 2'b10, 2'b11: Reserved SATA Mode 2'b00: 1.5Gbps 2'b01: 3.0Gbps 2'b10: 6.0Gbps QSGMII/SGMII Mode 2'b00: 1.25Gbps 2'b01: Reserved 2'b10: 5.0Gbps 2'b11: Reserved
3:2	RW	0x0	pipe_phymode phy mode: 2'b00: PCIe mode 2'b01: USB3 mode 2'b10: SATA mode 2'b11: QSGMII/SGMII mode
1:0	RW	0x0	pipe_databuswidth phy pipe data bus width: 2'b00: 32-bit, PCIe and USB3 only support 32-bit. 2'b01: 16-bit, SATA only support 16-bit 2'b10: Reserved 2'b11:Reserved

PIPE_PHY_GRF_PIPE_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	phy_clk_sel PHY reference clock frequency selection 2'b00: 24M 2'b01: 25M 2'b10: 100M 2'b11: Reserved

Bit	Attr	Reset Value	Description
12:11	RW	0x0	pipe_txpattern_sata Used in SATA mode only Controls which pattern the PHY sends at the Gen 1 rate when sending OOB or initialization signaling. The PHY transmits this pattern at the Gen 1 rate regardless of what rate the PHY is configured at. 2'b00 C ALIGN 2'b01 C D24.3 2'b10 C D10.2 2'b11 C Reserved
10:8	RW	0x0	pipe_txmargin Transmit margin control 3'b000: Normal operation range 3'b001: 800-1200mV for full swing or 400-700mV for half swing 3'b001: 200-400mV for full swing or 100-200mV for half swing Ohter: Reserved
7:6	RW	0x0	pipe_txdeemph De-emphasis control 2'b00: -6dB 2'b01: -3.5dB 2'b10: No de-emphasis 2'b11: Reserved
5	RW	0x0	pipe_txswing controls transmitter voltage swing level, for lane 0 1'b0: Full swing 1'b1: Low swing
4	RW	0x0	pipe_txcompliance pipe_txcompliance_i
3	RW	0x0	pipe_txcommonmode_disable pipe_txcommonmode_disable Note: Need set 0 when USB3 mode
2	RW	0x0	pipe_l0_txoneszeros pipe_l0_txoneszeros Note: Need set 0 when PCIe mode
1	RW	0x0	pipe_txelecidle pipe_txelecidle
0	RW	0x0	pipe_txdectrx_loopback pipe_l0_txdectrx_loopback

PIPE_PHY_GRF_PIPE_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x1	sel_pipe_txcompliance_i pipe_txcompliance_i_selection. 1'b0: From controller 1'b1: From grf
14	RW	0x0	sel_pipe_txcommonmode_disable pipe_txcommonmode_disable_selection. 1'b0: From controller 1'b1: From grf

Bit	Attr	Reset Value	Description
13	RW	0x0	sel_pipe_txoneszeros pipe_l0_txoneszeros selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf note: PCIe does not use this pipe signal, output 0, same to lane1
12	RW	0x1	sel_pipe_txelecidle pipe_l0_txelecidle selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf
11	RW	0x0	sel_pipe_txdectrx_loopback pipe_l0_txdectrx_loopback selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf
10	RW	0x1	sel_pipe_rxstandby sel_pipe_rxstandby_selection. 1'b0: From controller 1'b1: From grf
9	RW	0x0	sel_pipe_rxelecidle_disable pipe_rxelecidle_disable_selection. 1'b0: From controller 1'b1: From grf
8	RW	0x0	sel_pipe_rxterm pipe_rxterm_selection. 1'b0: From controller 1'b1: From grf
7	RW	0x0	sel_pipe_bypass_codec pipe_bypass_codec_selection. 1'b0: From controller 1'b1: From grf
6	RW	0x0	sel_pipe_ebuf pipe_ebufmode_selection. 1'b0: From controller 1'b1: From grf
5	RW	0x0	sel_pipe_l1sub_entreq_i pipe_txcompliance_selection. 1'b0: From controller 1'b1: From grf
4	RW	0x0	sel_pipe_powerdown pipe_l0_powerdown selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf
3	RW	0x0	sel_pipe_mac_pclkreq_n pipe_mac_pclkreq_n selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf
2	RW	0x0	sel_pipe_rate pipe_rate selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf
1	RW	0x0	sel_pipe_phymode pipe_phymode selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf

Bit	Attr	Reset Value	Description
0	RW	0x1	sel_pipe_databuswidth pipe_databuswidth selection. 1'b0: From PCIe, USB3 or SATA controller 1'b1: From grf

PIPE_PHY_GRF_PIPE_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15	RW	0x0	qsgm_mode qsgmii mode enabe 1'b0: other mode 1'b1: qsgmii/sgmii mode
14:13	RW	0x0	pipe_sel For pipephy0 2'b01: connect to USB3 Controller0 2'b10: connect to SATA port 0 For pipephy1 2'b01: connect to USB3 Controller 1 2'b10: connect to SATA port 1 2'b11: connect to QSGMII Controller For pipephy2 2'b00: connect to PCIe2.0 Controller 2'b10: connect to SATA port 2 2'b11: connect to QSGMII Controller
12	RO	0x0	reserved
11	RW	0x0	from_pcie_io pcie_clkreq source selection 1'b0: From Controller 1'b1: From pcie IO
10	RW	0x1	rxelecidle_sel rxelecidle_o source selection 1'b0: From Controller 1'b1: fixed b'b1
9:8	RW	0x0	phy_clk_ref_src_i PHY Reference clock source selection 2'b00: Use PLL_CKREF_INNER as reference clock source, CKREFP/N is not active, the PAD can be floating 2'b01: Use CKREFP/N as input reference clock source 2'b10: Use PLL_CKREF_INNER as reference clock source, Use CKREFP/N as output clock to provide a differential 100M reference clock in PCIE mode while CLKREQ=1. 2'b11: Not allowed
7:4	RO	0x0	reserved
3	RW	0x0	sel_pipe_txpattern_sata_i PHY control source selection 1'b0: From Controller 1'b1: From PIPE_CON3 register

Bit	Attr	Reset Value	Description
2	RW	0x0	sel_pipe_txmargin_i PHY control source selection 1'b0: From Controller 1'b1: From PIPE_CON3 register
1	RW	0x1	sel_pipe_txdeemph_i PHY control source selection 1'b0: From Controller 1'b1: From PIPE_CON3 register
0	RW	0x0	sel_pipe_txswing_i PHY control source selection 1'b0: From Controller 1'b1: From PIPE_CON3 register

PIPE_PHY_GRF_PIPE_STATUS1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:10	RO	0x00000	reserved
9	RW	0x0	pipe_clkreq_n Indicates that the PHY is in corresponding state to L1-sub-state in PCIE mode, during which PHY reference clock could be turned off.
8	RW	0x0	pipe_power_presetn PIPE Power Present This PIPE output indicates the presence of VBUS. If V BUS is connected to the PHY, this PIPE interface signal is generated by an internal VBUS comparator. This is an asynchronous signal
7	RW	0x0	pipe_rxelecidle_o PIPE Receiver Electrical Idle. Indicates receiver detection of an electrical idle. Signal desertion while the PHY is in a P0, P1, P2, or P3 state indicates the detection of Low Frequency Periodic Signaling (LFPS)
6	RW	0x0	pipe_phystatus_o PIPE PHY Status, Communicates completion of several PHY functions including power management state transitions, rate change, and receiver detection. When this signal transitions during entry and exit from P3 states and PCLK is not running, the signaling is asynchronous. In error situations (where the PHY fails to assert PhyStatus), the MAC can take MAC-specific error recovery actions
5:3	RW	0x0	pipe_rxstatus_o PIPE Receiver Status. Lane 0 Encodes receiver status and error codes for the received data stream when receiving data. 3'b000: received data OK 3'b001: one SKP Ordered set added 3'b010: one SKP Ordered set removed 3'b011: receiver detection 3'b100: 8B/10B decode error 3'b101: elastic buffer overflow 3'b110: elastic buffer underflow 3'b111: receive disparity error, overwritten by decode error
2:0	RO	0x0	reserved

PIPE_PHY_GRF_LFPS_DET_CON

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x09	lfps_detect_con lfps_detect_con

PIPE_PHY_GRF_PHY_INT_EN

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rxelecidle_l1_fall_irq_en rxelecidle_l1_fall irq enable 1'b0: irq disable 1'b1: irq enable
1:0	RW	0x0	rxelecidle_l0_fall_irq_en rxelecidle_l0_fall irq enable 1'b0: irq disable 1'b1: irq enable

PIPE_PHY_GRF_PHY_INT_STATUS

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxelecidle_l1_fall_irq_st rxelecidle_l1_fall irq status
0	RW	0x0	rxelecidle_l0_fall_irq_st rxelecidle_l0_fall irq status

3.9 USBPHY_U3_GRF_Register Description

3.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USBPHY_U3_GRF_CON0	0x0000	W	0x00000C52	USB PHY control register0
USBPHY_U3_GRF_CON1	0x0004	W	0x000001D2	USB PHY control register1
USBPHY_U3_GRF_CON2	0x0008	W	0x00000000	USB PHY control register2
USBPHY_U3_GRF_CON3	0x000C	W	0x00000019	USB PHY control register3
USBPHY_U3_GRF_CON4	0x0010	W	0x00000000	USB PHY control register3
USBPHY_U3_GRF_LS_CON	0x0040	W	0x00030100	USB PHY linestate control register
USBPHY_U3_GRF_DIS_CON	0x0044	W	0x00030100	USB PHY disconnect control register
USBPHY_U3_GRF_BVALID_CON	0x0048	W	0x00030100	USB PHY bvalid control register
USBPHY_U3_GRF_ID_CON	0x004C	W	0x00030100	USB PHY id control register
USBPHY_U3_GRF_INT_MASK	0x0080	W	0x00000000	USB PHY interrupt mask register
USBPHY_U3_GRF_INT_STATUS	0x0084	W	0x00000000	USB PHY interrupt status register
USBPHY_U3_GRF_INT_STATUS_CLR	0x0088	W	0x00000000	USB PHY interrupt status clear register
USBPHY_U3_GRF_STATUS	0x00C0	W	0x00000000	USB PHY status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.9.2 Detail Registers Description

USBPHY_U3_GRF_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	usbotg_utmi_dischrgvbus usbotg_utmi_dischrgvbus
12	RW	0x0	usbotg_utmi_chrgvbus usbotg_utmi_chrgvbus
11	RW	0x1	usbotg_utmi_idpullup usbotg_utmi_idpullup
10	RW	0x1	usbotg_utmi_iddig GRF USB OTG Plug iddig Indicator
9	RW	0x0	usbotg_utmi_iddig_sel USB OTG plug indicator output selection 1'b0:Select phyiddig status to controller 1'b1:Select GRF plug iddig indicator to controller
8	RW	0x0	usbotg_utmi_dmpulldown GRF OTG DM pulldown resistor
7	RW	0x0	usbotg_utmi_dppulldown GRF OTG DP pulldown resistor
6	RW	0x1	usbotg_utmi_termselect GRF OTG termination select between FS/LS/HS speed
5:4	RW	0x1	usbotg_utmi_xcvrselect GRF OTG transceiver select between FS/LS/HS speed
3:2	RW	0x0	usbotg_utmi_opmode GRF OTG operational mode selection
1	RW	0x1	usbotg_utmi_suspend_n GRF OTG suspend mode 1'b0:Suspend 1'b1:Normal
0	RW	0x0	usbotg_utmi_sel 1'b0:Select OTG controller utmi interface to phy 1'b1:Select GRF utmi interface to phy

USBPHY_U3_GRF_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	usbhost_utmi_dmpulldown GRF HOST DM pulldown resistor
7	RW	0x1	usbhost_utmi_dppulldown GRF HOST DP pulldown resistor
6	RW	0x1	usbhost_utmi_termselect GRF HOST termination select between FS/LS/HS speed
5:4	RW	0x1	usbhost_utmi_xcvrselect GRF HOST transceiver select between FS/LS/HS speed
3:2	RW	0x0	usbhost_utmi_opmode GRF HOST operational mode selection

Bit	Attr	Reset Value	Description
1	RW	0x1	usbhost_utmi_suspend_n GRF HOST suspend mode 1'b0:Suspend 1'b1:Normal
0	RW	0x0	usbhost_utmi_sel 1'b0:Select HOST controller utmi interface to phy 1'b1:Select GRF utmi interface to phy

USBPHY_U3_GRF_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	bvalid_vbusvalid_sel 1'b0: Select bvalid and vbusvalid of usbphy as bvalid and vbusvalid of usb controller 1'b1: Select value of bvalid_vbusvalid_grf (bit14) as bvalid and vbusvalid of usb controller
14	RW	0x0	bvalid_vbusvalid_grf bvalid_vbusvalid value to usb controller
15:13	RO	0x0	reserved
12	RW	0x0	vdm_src_en_usbotg open dm voltage source
11	RW	0x0	vdp_src_en_usbotg open dp voltage source
10	RW	0x0	rdm_pdwn_en_usbotg open dm pull down resistor
9	RW	0x0	idp_src_en_usbotg open dm source current
8	RW	0x0	idm_sink_en_usbotg open dm sink current
7	RW	0x0	idp_sink_en_usbotg open dp sink current
6:5	RO	0x0	reserved
4	RW	0x0	usbphy_commononn configure PLL clock output in suspend mode 1'b0:480MHz clock always on 1'b1:480MHz clock will turn off when both ports suspend asserted. If the supsend of any port deassert, it will wait 1ms to make 480MHz clock stable
3	RW	0x0	bypasssel_usbotg bypass select
2	RW	0x0	bypassdmen_usbotg bypass dm enable
1	RW	0x0	usbotg_disable_1 bypass OTG function
0	RW	0x0	usbotg_disable_0 bypass OTG function

USBPHY_U3_GRF_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	usbphy_hostport_wakeup_irq_en 1'b0:Disable wakeup irq 1'b1:Enable wakeup irq
14	RO	0x0	reserved
13	RW	0x0	usbotg_utmi_chrgvbus USB OTG GRF charge vbus
12	RO	0x0	reserved
11	RW	0x0	usbotg_utmi_drvvbus USB OTG GRF utmi_drvvbus
10	RW	0x0	usbotg_utmi_drvvbus_sel USB OTG utmi_drvvbus_sel bit control 1'b0:Select OTG controller drvvbus to phy 1'b1:Select OTG GRF utmidrvvbus to phy
9	RW	0x0	usbotg_utmi_fs_se0 USB OTG utmi_fs_se0 bit control
8	RW	0x0	usbotg_utmi_fs_data USB OTG utmi_fs_data bit control
7	RW	0x0	usbotg_utmi_fs_oe USB OTG utmi_fs_oe bit control
6	RW	0x0	usbotg_utmi_fs_xver_own USB OTG utmi_fs_xver_own bit control
5	RW	0x0	usbhost_utmi_idpullup USB HOST utmi_idpullup bit control
4	RW	0x1	usbhost_utmi_dmpulldown Enable DMINUS Pull Down resistor
3	RW	0x1	usbhost_utmi_dppulldown Enable DPLUS Pull Down resistor
2	RW	0x0	usbhost_utmi_dischrgvbus USB HOST utmi_dischrgvbus bit control
1	RW	0x0	usbhost_utmi_chrgvbus USB HOST utmi_chrgvbus bit control
0	RW	0x1	usbhost_utmi_drvvbus USB HOST utmi_drvvbus bit control

USBPHY_U3_GRF_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	usbotg_utmi_suspend_n usbotg_utmi_suspend_n GRF value
5	RW	0x0	usbotg_utmi_suspend_sel1 1'b0:grf_usbphy_con4[6] 1'b1:Usbotg_utmi_suspend_n & usbotg_utmi_l1_suspend_n
4	RW	0x0	usbotg_utmi_suspend_sel0 1'b0:~usbotg_utmi_suspend_com_n& ~usbotg_utmi_l1_suspend_com_n 1'b1:grf_usbphy_con4[5]?(usbotg_utmi_suspend_n& sbotg_utmi_l1_suspend_n) :grf_usbphy_con4[6];
3:0	RO	0x0	reserved

USBPHY_U3_GRF_LS_CON

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con host/otg port linestate filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U3_GRF_DIS_CON

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con host/otg port hostdisconnect filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U3_GRF_BVALID_CON

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_filter_con otg port bvalid filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U3_GRF_ID_CON

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	id_filter_con otg ID port filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U3_GRF_INT_MASK

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	host0_disconnect_irq_en host0_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
7:6	RW	0x0	otg0_disconnect_irq_en otg0_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
5:4	RW	0x0	otg0_id_irq_en otg0_id edge status enable 2'bx1:Id rising edge irq status enable 2'b1x:Id falling edge irq status enable
3:2	RW	0x0	otg0_bvalid_irq_en otg0_bvalid edge status irq enable 2'bx1:Bvalid rising edge irq status enable 2'b1x:Bvalid falling edge irq status enable
1	RW	0x0	host0_linestate_irq_en host0_linestate change status irq enable

Bit	Attr	Reset Value	Description
0	RW	0x0	otg0_linestate_irq_en otg0_linestate change status irq enable

USBPHY_U3_GRF_INT_STATUS

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	host0_disconnect_irq host0_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
7:6	RO	0x0	otg0_disconnect_irq otg0_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
5:4	RW	0x0	otg0_id_irq otg0_id edge irq status 2'bx1:Id rising edge irq status 2'b1x:Id falling edge irq status
3:2	RO	0x0	otg0_bvalid_irq otg0_bvalid edge irq status 2'bx1:Bvalid rising edge irq status 2'b1x:Bvalid falling edge irq status
1	RO	0x0	host0_linestate_irq host0_linestate change irq status
0	RO	0x0	otg0_linestate_irq otg0_linestate change irq status

USBPHY_U3_GRF_INT_STATUS_CLR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	host0_disconnect_irq_clr host0_disconnect_irq_clrirq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear
7:6	WO	0x0	otg0_disconnect_irq_clr otg0_disconnect_irq_clrirq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear
5:4	WO	0x0	otg0_id_irq_clr otg0_id edge irq status clear 2'b01:Id rising edge irq status clear 2'b10:Id falling edge irq status clear
3:2	WO	0x0	otg0_bvalid_irq_clr otg0_bvalid edge irq status clear 2'b01:Bvalid rising edge irq status clear 2'b10:Bvalid falling edge irq status clear
1	WO	0x0	host0_linestate_irq_clr host0_linestate change irq status clear, write 1 to clear irq status
0	WO	0x0	otg0_linestate_irq_clr otg0_linestate change irq status clear, write 1 to clear irq status

USBPHY_U3_GRF_STATUS

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	usbphy_dp_detected usbphy_dp_detected bit status
24	RO	0x0	usbphy_cp_detected usbphy_cp_detected bit status
23	RW	0x0	usbphy_dcp_detected usbphy_dcp_detected bit status
22	RO	0x0	usbhost_phy_ls_fs_rcv host_phy_ls_fs_rcv status
21	RO	0x0	usbhost_utmi_avalid host_utmi_avalid status
20	RO	0x0	usbhost_utmi_bvalid host_utmi_bvalid status
19	RO	0x0	usbhost_utmi_hostdisconnect host_utmi_hostdisconnect status
18	RO	0x0	usbhost_utmi_iddig_o host_utmi_iddig status
17:16	RO	0x0	usbhost_utmi_linestate host_utmi_linestate status
15	RO	0x0	usbhost_utmi_sessend host_utmi_sessend status
14	RO	0x0	usbhost_utmi_vbusvalid host_utmi_vbusvalid status
13	RO	0x0	usbhost_utmi_vmi host_utmi_vmi status
12	RO	0x0	usbhost_utmi_vpi host_utmi_vpi status
11	RO	0x0	usbotg_phy_ls_fs_rcv utmi_phy_ls_fs_rcv_out status
10	RO	0x0	usbotg_utmi_avalid otg_utmiavalid bit status
9	RO	0x0	usbotg_utmi_bvalid otg_utmibvalid bit status
8	RO	0x0	usbotg_utmi_fs_xver_own OTG utmi_fs_xver_own status
7	RO	0x0	usbotg_utmi_hostdisconnect otg_utmi_hostdisconnect status
6	RO	0x0	usbotg_utmi_iddig usbotg_utmi_iddig status
5:4	RO	0x0	usbotg_utmi_linestate otg_utmi_linestate status
3	RO	0x0	usbotg_utmi_sessend otg_utmi_sessend bit status
2	RO	0x0	usbotg_utmi_vbusvalid otg_utmi_vbusvalid bit status
1	RO	0x0	usbotg_utmi_vmi otg_utmi_vmi bit status
0	RO	0x0	usbotg_utmi_vpi otg_utmi_vpi bit status

3.10 USB2PHY_U2_GRF_Register Description

3.10.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USBPHY_U2_GRF_CON0	0x0000	W	0x00000C52	USB PHY control register0
USBPHY_U2_GRF_CON1	0x0004	W	0x000001D2	USB PHY control register1
USBPHY_U2_GRF_CON2	0x0008	W	0x00000000	USB PHY control register2
USBPHY_U2_GRF_CON3	0x000C	W	0x00000019	USB PHY control register3
USBPHY_U2_GRF_LS_CON	0x0040	W	0x00030100	USB PHY linestate control register
USBPHY_U2_GRF_DIS_CON	0x0044	W	0x00030100	USB PHY disconnect control register
USBPHY_U2_GRF_BVALID_CON	0x0048	W	0x00030100	USB PHY bvalid control register
USBPHY_U2_GRF_ID_CON	0x004C	W	0x00030100	USB PHY id control register
USBPHY_U2_GRF_INT_MASK	0x0080	W	0x00000000	USB PHY interrupt mask register
USBPHY_U2_GRF_INT_STATUS	0x0084	W	0x00000000	USB PHY interrupt status register
USBPHY_U2_GRF_INT_STATUS_CLR	0x0088	W	0x00000000	USB PHY interrupt status clear register
USBPHY_U2_GRF_STATUS	0x00C0	W	0x00000000	USB PHY status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.10.2 Detail Registers Description

USBPHY_U2_GRF_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x00	reserved
11	RW	0x1	usb2host0_utmi_idpullup GRF HOST0 ID pullup resistor
10	RW	0x1	usb2host0_utmi_iddig GRF HOST0 Plug Indicator
9	RW	0x0	usb2host0_utmi_iddig_sel 1'b0: USB Plug Indicator from usb2phy 1'b1: USB Plug Indicator from grf bit 10
8	RW	0x0	usb2host0_utmi_dmpulldown GRF HOST0 DM pulldown resistor
7	RW	0x0	usb2ho0_utmi_dppulldown GRF HOST st0 DP pulldown resistor
6	RW	0x1	usb2host0_utmi_termselect GRF HOST0 termination select between FS/LS/HS speed
5:4	RW	0x1	usb2host0_utmi_xcvrselect GRF HOST0 transceiver select between FS/LS/HS speed
3:2	RW	0x0	usb2host0_utmi_opmode GRF HOST0 operational mode selection

Bit	Attr	Reset Value	Description
1	RW	0x1	usb2host0_utmi_suspend_n GRF HOST0 suspend mode 1'b0:Suspend 1'b1:Normal
0	RW	0x0	usb2host0_utmi_sel 1'b0:Select HOST0 controller utmi interface to phy 1'b1:Select GRF utmi interface to phy

USBPHY_U2_GRF_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	usb2host1_utmi_dmpulldown GRF HOST1 DM pulldown resistor
7	RW	0x1	usb2host1_utmi_dppulldown GRF HOST1 DP pulldown resistor
6	RW	0x1	usb2host1_utmi_termselect GRF HOST1 termination select between FS/LS/HS speed
5:4	RW	0x1	usb2host1_utmi_xcvrselect GRF HOST1 transceiver select between FS/LS/HS speed
3:2	RW	0x0	usb2host1_utmi_opmode GRF HOST1 operational mode selection
1	RW	0x1	usb2host1_utmi_suspend_n GRF HOST1 suspend mode 1'b0:Suspend 1'b1:Normal
0	RW	0x0	usb2host1_utmi_sel 1'b0:Select HOST1 controller utmi interface to phy 1'b1:Select GRF utmi interface to phy

USBPHY_U2_GRF_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	vdm_src_en_usb2host0 open dm voltage source
11	RW	0x0	vdp_src_en_usb2host0 open dp voltage source
10	RW	0x0	rdm_pdwn_en_usb2host0 open dm pull down resistor
9	RW	0x0	idp_src_en_usb2host0 open dm source current
8	RW	0x0	idm_sink_en_usb2host0 open dm sink current
7	RW	0x0	idp_sink_en_usb2host0 open dp sink current
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	usbphy_commononn configure PLL clock output in suspend mode 1'b0:480MHz clock always on 1'b1:480MHz clock will turn off when both ports suspend asserted. If the supsend of any port deassert, it will wait 1ms to make 480MHz clock stable
3	RW	0x0	bypasssel_usb2host0 bypass select
2	RW	0x0	bypassdmen_usb2host0 bypass dm enable
1	RW	0x0	usb2host0_disable_1 bypass HOST0 function
0	RW	0x0	usb2host0_disable_0 bypass HOST0 function

USBPHY_U2_GRF_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	usbphy_hostport_wakeup_irq_en 1'b0:Disable wakeup irq 1'b1:Enable wakeup irq
14	RO	0x0	reserved
13	RW	0x0	usb2host0_utmi_chrgvbus USB HOST0 GRF charge vbus
12	RO	0x0	reserved
11	RW	0x0	usb2host0_utmi_drvvbus USB HOST0 GRF utmi_drvvbus
10	RW	0x0	usb2host0_utmi_drvvbus_sel USB HOST0 utmi_drvvbus_sel bit control 1'b0:Select HOST0 controller drvvbus to phy 1'b1:Select HOST0 GRF utmidrvvbus to phy
9	RW	0x0	usb2host0_utmi_fs_se0 USB HOST0 utmi_fs_se0 bit control
8	RW	0x0	usb2host0_utmi_fs_data USB HOST0 utmi_fs_data bit control
7	RW	0x0	usb2host0_utmi_fs_oe USB HOST0 utmi_fs_oe bit control
6	RW	0x0	usb2host0_utmi_fs_xver_own USB HOST0 utmi_fs_xver_own bit control
5	RW	0x0	usb2host1_utmi_idpullup USB HOST1 utmi_idpullup bit control
4	RW	0x1	usb2host1_utmi_dmpulldown Enable DMINUS Pull Down resistor
3	RW	0x1	usb2host1_utmi_dppulldown Enable DPLUS Pull Down resistor
2	RW	0x0	usb2host1_utmi_dischrgvbus USB HOST1 utmi_dischrgvbus bit control
1	RW	0x0	usb2host1_utmi_chrgvbus USB HOST1 utmi_chrgvbus bit control
0	RW	0x1	usb2host1_utmi_drvvbus USB HOST1 utmi_drvvbus bit control

USBPHY_U2_GRF_LS_CON

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con HOST1/HOST0 port linestate filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U2_GRF_DIS_CON

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con HOST1/HOST0 port HOST1disconnect filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U2_GRF_BVALID_CON

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_filter_con HOST0 port bvalid filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U2_GRF_ID_CON

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	id_filter_con HOST0 ID port filter time control register. Unit:Pclk(up to 100MHz)

USBPHY_U2_GRF_INT_MASK

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	usb2host1_disconnect_irq_en usb2HOST11_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
7:6	RW	0x0	usb2host0_disconnect_irq_en usb2HOST10_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
5:4	RW	0x0	usb2host0_id_irq_en usb2HOST10_id edge status enable 2'bx1:Id rising edge irq status enable 2'b1x:Id falling edge irq status enable

Bit	Attr	Reset Value	Description
3:2	RW	0x0	usb2host0_bvalid_irq_en usb2HOST10_bvalid edge status irq enable 2'bx1:Bvalid rising edge irq status enable 2'b1x:Bvalid falling edge irq status enable
1	RW	0x0	usb2host1_linestate_irq_en usb2HOST11_linestate change status irq enable
0	RW	0x0	usb2host0_linestate_irq_en usb2HOST10_linestate change status irq enable

USBPHY_U2_GRF_INT_STATUS

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	usb2host1_disconnect_irq usb2HOST11_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
7:6	RW	0x0	usb2host0_disconnect_irq usb2HOST10_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
5:4	RW	0x0	usb2host0_id_irq usb2HOST10_id edge irq status 2'bx1:Id rising edge irq status 2'b1x:Id falling edge irq status
3:2	RW	0x0	usb2host0_bvalid_irq usb2HOST10_bvalid edge irq status 2'bx1:Bvalid rising edge irq status 2'b1x:Bvalid falling edge irq status
1	RW	0x0	usb2host1_linestate_irq usb2HOST11_linestate change irq status
0	RW	0x0	usb2host0_linestate_irq usb2HOST10_linestate change irq status

USBPHY_U2_GRF_INT_STATUS_CLR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	usb2host1_disconnect_irq_clr usb2HOST11_disconnect_irq_clr irq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear
7:6	RW	0x0	usb2host0_disconnect_irq_clr usb2HOST10_disconnect_irq_clr irq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear
5:4	RW	0x0	usb2host0_id_irq_clr usb2HOST10_id edge irq status clear 2'b01:Id rising edge irq status clear 2'b10:Id falling edge irq status clear
3:2	RW	0x0	usb2host0_bvalid_irq_clr usb2HOST10_bvalid edge irq status clear 2'b01:Bvalid rising edge irq status clear 2'b10:Bvalid falling edge irq status clear

Bit	Attr	Reset Value	Description
1	RW	0x0	usb2host1_linestate_irq_clr usb2HOST11_linestate change irq status clear, write 1 to clear irq status
0	RW	0x0	usb2host0_linestate_irq_clr usb2HOST10_linestate change irq status clear, write 1 to clear irq status

USBPHY_U2_GRF_STATUS

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	usbphy_dp_detected usbphy_dp_detected bit status
24	RW	0x0	usbphy_cp_detected usbphy_cp_detected bit status
23	RW	0x0	usbphy_dcp_detected usbphy_dcp_detected bit status
22	RW	0x0	usb2host1_phy_ls_fs_rcv HOST1_phy_ls_fs_rcv status
21	RW	0x0	usb2host1_utmi_avalid HOST1_utmi_avalid status
20	RW	0x0	usb2host1_utmi_bvalid HOST1_utmi_bvalid status
19	RW	0x0	usb2host1_utmi_hostdisconnect HOST1_utmi_HOST1disconnect status
18	RW	0x0	usb2host1_utmi_iddig_o HOST1_utmi_iddig status
17:16	RW	0x0	usb2host1_utmi_linestate HOST1_utmi_linestate status
15	RW	0x0	usb2host1_utmi_sessend HOST1_utmi_sessend status
14	RW	0x0	usb2host1_utmi_vbusvalid HOST1_utmi_vbusvalid status
13	RW	0x0	usb2host1_utmi_vmi HOST1_utmi_vmi status
12	RW	0x0	usb2host1_utmi_vpi HOST1_utmi_vpi status
11	RW	0x0	usb2host0_phy_ls_fs_rcv utmi_phy_ls_fs_rcv_out status
10	RW	0x0	usb2host0_utmi_avalid HOST0_utmi avalid bit status
9	RW	0x0	usb2host0_utmi_bvalid HOST0_utmi bvalid bit status
8	RW	0x0	usb2host0_utmi_fs_xver_own HOST0 utmi_fs_xver_own status
7	RW	0x0	usb2host0_utmi_hostdisconnect HOST0_utmi_HOST1disconnect status
6	RW	0x0	usb2host0_utmi_iddig usb2HOST10_utmi_iddig status
5:4	RW	0x0	usb2host0_utmi_linestate HOST0_utmi_linestate status
3	RW	0x0	usb2host0_utmi_sessend HOST0_utmi_sessend bit status

Bit	Attr	Reset Value	Description
2	RW	0x0	usb2host0_utmi_vbusvalid HOST0_utmi_vbusvalid bit status
1	RW	0x0	usb2host0_utmi_vmi HOST0_utmi_vmi bit status
0	RW	0x0	usb2host0_utmi_vpi HOST0_utmi_vpi bit status

3.11 EDP_PHY Register Description

3.11.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EDP_PHY_GRF_CON0	0x0000	W	0x00000000	EDP PHY control register0
EDP_PHY_GRF_CON1	0x0004	W	0x00003840	EDP PHY control register1
EDP_PHY_GRF_CON2	0x0008	W	0x00000100	EDP PHY control register2
EDP_PHY_GRF_CON3	0x000C	W	0x00004444	EDP PHY control register3
EDP_PHY_GRF_CON4	0x0010	W	0x00003333	EDP PHY control register4
EDP_PHY_GRF_CON5	0x0014	W	0x00000055	EDP PHY control register5
EDP_PHY_GRF_CON6	0x0018	W	0x0000A97D	EDP PHY control register6
EDP_PHY_GRF_CON7	0x001C	W	0x00000000	EDP PHY control register7
EDP_PHY_GRF_CON8	0x0020	W	0x00000800	EDP PHY control register8
EDP_PHY_GRF_CON9	0x0024	W	0x00000000	EDP PHY control register9
EDP_PHY_GRF_CON10	0x0028	W	0x00000000	EDP PHY control register10
EDP_PHY_GRF_CON11	0x002C	W	0x00004501	EDP PHY control register11
EDP_PHY_GRF_STATUS0	0x0030	W	0x00000000	EDP PHY status register0
EDP_PHY_GRF_STATUS1	0x0034	W	0x00000000	EDP PHY status register1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.11.2 Detail Registers Description

EDP_PHY_GRF_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	edp_video_bist_en edp_video_bist_en
14	RW	0x0	edp_mem_ctrl_sel edp_mem_ctrl_sel
13	RW	0x0	edp_stmode edp_stmode
12	RW	0x0	edp_hdcp_protect hdcp protect enable
11:8	RW	0x0	edp_phy_tx_idle Force the high speed differential signal to common mode, for initialization of the serdes or special signaling 1'b1: force TXPN /TXMN to common mode 1'b0: normal operation

Bit	Attr	Reset Value	Description
7:4	RW	0x0	edp_phy_tx_pd Power down control signal of channel N (N = 0~3) 1'b1: power down channel 1'b0: normal operation
3:2	RO	0x0	reserved
1	RW	0x0	edp_phy_iddq_en IDDQ test enable 1'b0: normal operation 1'b1: do IDDQ TEST
0	RW	0x0	edp_phy_pd_pll Shared PLL block power down 1'b0: normal operation 1'b1: power down shared PLL, all the channels are not working

EDP_PHY_GRF_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14:0	RW	0x3840	edp_phy_pll_div The initial divider control for PLL. 1'b1000 0000 0000 000 (default)

EDP_PHY_GRF_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x1	edp_phy_tx_rterm TX termination resistance adjustment
7:6	RO	0x0	reserved
5:4	RW	0x0	edp_phy_rate Rate control for TX
3:0	RW	0x0	edp_phy_ref_div Reference clock divider control.

EDP_PHY_GRF_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RW	0x4	edp_phy_tx3_emp The adjustment for the emphasis level of the driver
11:8	RW	0x4	edp_phy_tx2_emp The adjustment for the emphasis level of the driver
7:4	RW	0x4	edp_phy_tx1_emp The adjustment for the emphasis level of the driver

Bit	Attr	Reset Value	Description
3:0	RW	0x4	edp_phy_tx0_emp The adjustment for the emphasis level of the driver

EDP_PHY_GRF_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14:12	RW	0x3	edp_phy_tx3_amp The adjustment for the amplitude level (signal-end amplitude) of the driver
11	RO	0x0	reserved
10:8	RW	0x3	edp_phy_tx2_amp The adjustment for the amplitude level (signal-end amplitude) of the driver
7	RO	0x0	reserved
6:4	RW	0x3	edp_phy_tx1_amp The adjustment for the amplitude level (signal-end amplitude) of the driver
3	RO	0x0	reserved
2:0	RW	0x3	edp_phy_tx0_amp The adjustment for the amplitude level (signal-end amplitude) of the driver

EDP_PHY_GRF_CON5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	edp_phy_tx_mode Control the TX driver mode. 2'b00: mode1, the termination resistor connects to AVDH. 2'b01: mode2, the termination resistor connects to AVDL. 2'b10: mode3, common mode voltage sets to meet LVDS. 2'b11: mode4, open drain mode.
7:6	RW	0x1	edp_phy_tx3_amp_scale The amplitude scale factor control 2'b00: scale down the output amplitude to 75%. 2'b01/10: keep the output amplitude 2'b11: scale up the output amplitude to 125%
5:4	RW	0x1	edp_phy_tx2_amp_scale The amplitude scale factor control 2'b00: scale down the output amplitude to 75%. 2'b01/10: keep the output amplitude 2'b11: scale up the output amplitude to 125%

Bit	Attr	Reset Value	Description
3:2	RW	0x1	edp_phy_tx1_amp_scale The amplitude scale factor control 2'b00: scale down the output amplitude to 75%. 2'b01/10: keep the output amplitude 2'b11: scale up the output amplitude to 125%
1:0	RW	0x1	edp_phy_tx0_amp_scale The amplitude scale factor control 2'b00: scale down the output amplitude to 75%. 2'b01/10: keep the output amplitude 2'b11: scale up the output amplitude to 125%

EDP_PHY_GRF_CON6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RW	0xa	edp_phy_ssc_depth SSC depth control signal
11	RW	0x1	edp_phy_ssc_en SSC function enable signal 1'b0: SSC function is disable 1'b1: SSC function is enable
10	RO	0x0	reserved
9:0	RW	0x17d	edp_phy_ssc_cnt SSC frequency control

EDP_PHY_GRF_CON7

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:0	RO	0x0000	reserved

EDP_PHY_GRF_CON8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:0	RW	0x0800	edp_phy_pll_ctl_h pll_ctl[31:16] Register Signal for PLL pll_ctl[28:27]: 2'b00 center spread ssc control pll_ctl[28:27]: 2'b01 down spread ssc control pll_ctl[28:27]: 2'b1x up spread ssc control pll_ctl[31]: the frequency control signal for clk_phy 1'b0: 1/20 of the data rate 1'b1: 1/10 of the data rate

EDP_PHY_GRF_CON9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:0	RW	0x0000	edp_phy_tx_ctl Reserved Register Signal for TX. tx_ctl[2:0]: when driver is set to LVDS mode, tx_ctl[2:0] is used for common mode voltage control. tx_ctl[3]:reserved tx_ctl[5:4]: 2'b00, txN_data[19:0] is clock-in by rising edge of txN_rpck tx_ctl[5:4]: 2'b11, txN_data[19:0] is clock-in by rising edge of clk_phy tx_ctl[5:4]:2'b01, forbidden. tx_ctl[5:4]:2'b10, txN_data[19:0] is clock-in by rising edge oftxN_pck. tx_ctl[6]: bit error control singal: 0, prbs7 pattern; 1, prbs7 pattern with bit error. tx_ctl[7]:reserved tx_ctl[9:8]: 2'b00/01/10, TXPN and TXMN will be pull to 0, when tx_pd[N]=1, tx_ctl[9:8]: 2'b11, TXPN and TXMN will be stay in Hz status, when tx_pd[N]=1 tx_ctl[10]: when tx_ctl[5:4] is set to 2'b11 1'b1: use positive terminal of high speed clock to sample low speed clock 1'b0: which terminal of high speed to use decide by the phase relation between high speed clock and low speed clock; Tx_ctl[11]: when tx_ctl[5:4] is set to 2'b00 1'b1: the internal sampler clock of parallel data originates from pll; 1'b0: the internal sampler clock of parallel data originates from txN_rpck; tx_ctl[12]: bus width 1'b1: 10bit mode, txN_data[9:0] is used 1'b0: 20bit mode, txN_data[19:0] is used tx_ctl[15:13]:reserved

EDP_PHY_GRF_CON10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	edp_phy_aux_rcv_pd_sel AUX channel receiver select 1'b0: edp_aux[3] 1'b1: edp_phy_aux_rcv_pd
4	RW	0x0	edp_phy_aux_drv_pd_sel AUX channel driver select 1'b0: ~edp_aux[3] 1'b1: edp_phy_aux_drv_pd

Bit	Attr	Reset Value	Description
3	RO	0x0	reserved
2	RW	0x0	edp_phy_aux_idle Force the AUX channel differential signal to common mode 1'b1: force AUXP /AUXN to common mode 1'b0: normal operation
1	RW	0x0	edp_phy_aux_rcv_pd AUX channel receiver enable control 1'b0: enable 1'b1: disable
0	RW	0x0	edp_phy_aux_drv_pd AUX channel driver enable control 1'b0: enable 1'b1: disable

EDP_PHY_GRF_CON11

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14:12	RW	0x4	edp_phy_aux_rcv_vcm common mode voltage control, when AUX channel operates as receiver
11:10	RW	0x1	edp_phy_aux_mode Control the TX driver mode. 2'b00: mode1, the termination resistor connects to AVDH. 2'b01: mode2, the termination resistor connects to AVDL.(default) 2'b10: mode3, common mode voltage sets to meet LVDS. 2'b11: mode4, open drain mode.
9:8	RW	0x1	edp_phy_aux_amp_scale
7	RO	0x0	reserved
6:4	RW	0x0	edp_phy_aux_amp The adjustment for the amplitude level (signal-end amplitude) of the driver 3'b000:150mV 3'b001:200mV 3'b010:250mV 3'b011:300mV Other: reserved
3	RO	0x0	reserved
2:0	RW	0x1	edp_phy_aux_rterm TX termination resistance adjustment setp: 100ohm

EDP_PHY_GRF_STATUS0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	edp_phy_pll_ctl_o Reserved Register Signal (output) for PLL bit0: pll_rdy bit1: por output test signal bit2: reference clock test signal bit3: pd_pll

EDP_PHY_GRF_STATUS1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	edp_phy_tx3_ctl_o Reserved Register Signal (output) for TX bit[0]: pd_tx; bit[7:1]: 0000000
23:16	RO	0x00	edp_phy_tx2_ctl_o Reserved Register Signal (output) for TX bit[0]: pd_tx; bit[7:1]: 0000000
15:8	RO	0x00	edp_phy_tx1_ctl_o Reserved Register Signal (output) for TX bit[0]: pd_tx; bit[7:1]: 0000000
7:0	RO	0x00	edp_phy_tx0_ctl_o Reserved Register Signal (output) for TX bit[0]: pd_tx; bit[7:1]: 0000000

3.12 PCIEPHY_GRF Register Description

3.12.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_PCIE30PHY_CON0	0x0000	W	0x00000001	PCIE30 PHY control register0
GRF_PCIE30PHY_CON1	0x0004	W	0x00000000	PCIE30 PHY control register1
GRF_PCIE30PHY_CON2	0x0008	W	0x00000000	PCIE30 PHY control register2
GRF_PCIE30PHY_CON3	0x000C	W	0x00009860	PCIE30 PHY control register3
GRF_PCIE30PHY_CON4	0x0010	W	0x0000E637	PCIE30 PHY control register
GRF_PCIE30PHY_CON5	0x0014	W	0x00002A90	PCIE30 PHY control register
GRF_PCIE30PHY_CON6	0x0018	W	0x00002A90	PCIE30 PHY control register
GRF_PCIE30PHY_CON7	0x001C	W	0x00000000	PCIE30 PHY control register
GRF_PCIE30PHY_CON8	0x0020	W	0x0000002A	PCIE30 PHY control register
GRF_PCIE30PHY_CON9	0x0024	W	0x00000033	PCIE30 PHY control register
GRF_PCIE30PHY_STATUS0	0x0080	W	0x00000000	PCIE30 PHY control register
GRF_PCIE30PHY_STATUS1	0x0084	W	0x00000000	PCIE30 PHY control register
GRF_PCIE30PHY_STATUS2	0x0088	W	0x00000000	PCIE30 PHY control register
GRF_PCIE30PHY_PRT0_CON0	0x0100	W	0x00000000	PCIE30 PHY PRT0 control register0
GRF_PCIE30PHY_PRT0_CON1	0x0104	W	0x00000000	PCIE30 PHY PRT0 control register1
GRF_PCIE30PHY_PRT0_CON2	0x0108	W	0x00000000	PCIE30 PHY PRT0 control register2

Name	Offset	Size	Reset Value	Description
GRF_PCIE30PHY_PRT0_CON3	0x010C	W	0x00000000	PCIE30 PHY PRT0 control register3
GRF_PCIE30PHY_PRT0_CON4	0x0110	W	0x00000000	PCIE30 PHY PRT0 control register4
GRF_PCIE30PHY_PRT0_CON5	0x0114	W	0x00000800	PCIE30 PHY PRT0 control register1
GRF_PCIE30PHY_PRT0_CON6	0x0118	W	0x00000800	PCIE30 PHY PRT0 control register6
GRF_PCIE30PHY_PRT0_CON7	0x011C	W	0x00000000	PCIE30 PHY PRT0 control register7
GRF_PCIE30PHY_PRT0_CON8	0x0120	W	0x00000000	PCIE30 PHY PRT0 control register8
GRF_PCIE30PHY_PRT0_CON9	0x0124	W	0x00000000	PCIE30 PHY PRT0 control register9
GRF_PCIE30PHY_PRT0_CON10	0x0128	W	0x00000000	PCIE30 PHY PRT0 control register10
GRF_PCIE30PHY_PRT0_CON11	0x012C	W	0x00000000	PCIE30 PHY PRT0 control register11
GRF_PCIE30PHY_PRT0_CON12	0x0130	W	0x00000000	PCIE30 PHY PRT0 control register12
GRF_PCIE30PHY_PRT0_CON13	0x0134	W	0x00000000	PCIE30 PHY PRT0 control register13
GRF_PCIE30PHY_PRT0_CON14	0x0138	W	0x00000000	PCIE30 PHY PRT0 control register14
GRF_PCIE30PHY_PRT0_CON15	0x013C	W	0x00000000	PCIE30 PHY PRT0 control register15
GRF_PCIE30PHY_PRT0_CON16	0x0140	W	0x00000000	PCIE30 PHY PRT0 control register16
GRF_PCIE30PHY_PRT0_CON17	0x0144	W	0x00000000	PCIE30 PHY PRT0 control register17
GRF_PCIE30PHY_PRT0_CON18	0x0148	W	0x00000000	PCIE30 PHY PRT0 control register18
GRF_PCIE30PHY_PRT0_CON19	0x014C	W	0x00000000	PCIE30 PHY PRT0 control register19
GRF_PCIE30PHY_PRT0_CON20	0x0150	W	0x00000000	PCIE30 PHY PRT0 control register20
GRF_PCIE30PHY_PRT0_CON21	0x0154	W	0x00000000	PCIE30 PHY PRT0 control register13
GRF_PCIE30PHY_PRT0_CON22	0x0158	W	0x00000000	PCIE30 PHY PRT0 control register22
GRF_PCIE30PHY_PRT0_CON23	0x015C	W	0x00000000	PCIE30 PHY PRT0 control register23
GRF_PCIE30PHY_PRT0_CON24	0x0160	W	0x00000000	PCIE30 PHY PRT0 control register24
GRF_PCIE30PHY_PRT0_CON25	0x0164	W	0x00000000	PCIE30 PHY PRT0 control register25
GRF_PCIE30PHY_PRT0_CON26	0x0168	W	0x00000000	PCIE30 PHY PRT0 control register13
GRF_PCIE30PHY_PRT0_CON27	0x016C	W	0x00000000	PCIE30 PHY PRT0 control register27
GRF_PCIE30PHY_PRT0_CON28	0x0170	W	0x00000000	PCIE30 PHY PRT0 control register13

Name	Offset	Size	Reset Value	Description
GRF_PCIE30PHY_PRT0_CON29	0x0174	W	0x00000000	PCIE30 PHY PRT0 control register29
GRF_PCIE30PHY_PRT0_CON30	0x0178	W	0x00000000	PCIE30 PHY PRT0 control register30
GRF_PCIE30PHY_PRT0_CON31	0x017C	W	0x00000000	PCIE30 PHY PRT0 control register31
GRF_PCIE30PHY_PRT0_CON32	0x0180	W	0x00000000	PCIE30 PHY PRT0 control register32
GRF_PCIE30PHY_PRT0_CON33	0x0184	W	0x00000000	PCIE30 PHY PRT0 control register33
GRF_PCIE30PHY_PRT0_CON34	0x0188	W	0x00000000	PCIE30 PHY PRT0 control register34
GRF_PCIE30PHY_PRT0_CON35	0x018C	W	0x00000000	PCIE30 PHY PRT0 control register35
GRF_PCIE30PHY_PRT0_CON36	0x0190	W	0x00000000	PCIE30 PHY PRT0 control register36
GRF_PCIE30PHY_PRT0_CON37	0x0194	W	0x00000000	PCIE30 PHY PRT0 control register37
GRF_PCIE30PHY_PRT0_CON38	0x0198	W	0x00000000	PCIE30 PHY PRT0 control register38
GRF_PCIE30PHY_PRT0_CON39	0x019C	W	0x00000000	PCIE30 PHY PRT0 control register33

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.12.2 Detail Registers Description

GRF_PCIE30PHY_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:0	RW	0x0001	ups_pipe_config upcs_pipe_config bit control

GRF_PCIE30PHY_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:9	RO	0x00	reserved
8:0	RW	0x000	phy0_txdn_term_offset Offset for TX Down Termination Specifies an additional fixed offset to calibrated TX down termination value. This is a signed input with 2's complement encoding. Voltage Range: 0-vpdig

GRF_PCIE30PHY_CON2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pcie30phy_test_burn PHY test_burn bit control
8:0	RW	0x000	phy0_txup_term_offset Offset for TX Up Termination Specifies an additional fixed offset to calibrated TX up termination value. This is a signed input with 2's complement encoding. Voltage Range: 0-vpdig

GRF_PCIE30PHY_CON3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x1	phy0_ref_use_pad Select reference clock connected to ref_pad_clk_p/ref_pad_clk_m Selects the external ref_pad_clk_p and ref_pad_clk_m inputs as the reference clock source when asserted. When de-asserted, ref_alt_clk_p and ref_alt_clk_m are the sources of the reference clock. Any change in this input must be followed by phy_reset assertion.
14	RW	0x0	phy0_ref_repeat_clk_en Repeat reference clock enable Enables the CML output clocks ref_repeat_clk_[p,m]. This pair of clocks can be used as reference clocks for other on-chip PHYs.
13	RW	0x0	phy0_ref_clkdet_en Enable Reference Clock Detection Enables detection of the reference clock on the pads input
12	RW	0x1	phy0_pma_pwr_stable Power stable for PMA Status signal indicating that the power for the PMA is stable. The pma_pwr_stable signal should only be asserted if the supply is 90% of nominal or higher.
11	RW	0x1	phy0_pcs_pwr_stable Power stable for Raw PCS Status signal indicating that the power for the Raw PCS is stable. The pcs_pwr_stable signal should only be asserted if the supply is 90% of nominal or higher.
10	RW	0x0	phy0_mpllb_ssc_en Spread spectrum enable (mpllb_ssc_en) Enables spread-spectrum clock (SSC) generation on the mpll(a,b)_div_clk output. If the reference clock already has spread spectrum applied, mpll(a,b)_ssc_en must be de-asserted.
9	RW	0x0	phy0_mpllb_force_en MPLLB force enable When asserted, the corresponding MPLL is forced to be powered up,irrespective of the txX_mpll_en input.

Bit	Attr	Reset Value	Description
8	RW	0x0	phy0_mplla_ssc_en Spread spectrum enable (mplla_ssc_en) Enables spread-spectrum clock (SSC) generation on thempll(a,b)_div_clk output. If the reference clock already has spread spectrum applied, mpll(a,b)_ssc_en must be de-asserted. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted.
7	RW	0x0	phy0_mplla_force_en MPLLA force enable When asserted, the corresponding MPLL is forced to be powered up, irrespective of the txX_mpll_en input.
6:5	RW	0x3	phy0_nominal_vph_sel VPH nominal selection Indicates the VPH voltage level supplied: 2'b00: Reserved 2'b01: 1.2 V 2'b10: 1.5 V 2'b11: 1.8 V This input can only be changed with phy_reset is asserted.
4:0	RW	0x00	phy0_rx_term_offset Offset for RX Termination Specifies an additional fixed offset to calibrated RX termination value. This is a signed input with 2's complement encoding. Voltage Range: 0-vpdig

GRF_PCIE30PHY_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x1	cr_para_sel Control Register (CR) parallel interface select Controls selection between JTAG and CR interfaces: 1'b0: JTAG 1'b1: Control Register (CR) This input can only be changed when the cr_para_clk and jtag_tck clock inputs are disabled.
14	RW	0x1	sram_ext_ld_done SRAM external load done Signal asserted by user after any updates to the SRAM have been loaded.
13	RW	0x1	sram_bypass SRAM bypass Control signal when asserted, bypasses the SRAM interface.
12	RW	0x0	pg_mode_en Power gating support enable Control input to enable the power gating support. When de-asserted, the control inputs related to power gating are ignored

Bit	Attr	Reset Value	Description
11	RW	0x0	ext_pclk_req External PCLK request When asserted, the MPLL clock sources in the PHY are powered up and pcs_laneX_pclk outputs stay active, regardless of the pcs_laneX_powerdown[3:0] inputs
10	RW	0x1	phy_rx1_term_acdc Receiver termination control
9	RW	0x1	phy_rx0_term_acdc Receiver termination control
8	RW	0x0	phy_rtune_req Resistor tune request Assertion triggers a resistor tune request (if one is not already in progress)
7	RW	0x0	phy_lane1_rx2tx_par_lb_en Parallel (RX to TX) loopback enable When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer.
6	RW	0x0	phy_lane0_rx2tx_par_lb_en Parallel (RX to TX) loopback enable When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer.
5	RW	0x1	phy_lane1_pwr_present phy_lane1_pwr_present VBUS power present Signal from external VBUS detection circuit
4	RW	0x1	phy_lane0_pwr_present phy_lane0_pwr_present VBUS power present Signal from external VBUS detection circuit
3	RW	0x0	ext_ctrl_sel ext_ctrl_sel phy_ext_ctrl_sel is PHY configuration setting per-protocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the DesignWare Cores PHY databook, "PHY Usage and Configuration" chapter). The PCS internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolX signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.
2	RW	0x1	phy0_sram_ext_ld_done SRAM external load done Signal asserted by user after any updates to the SRAM have been loaded.
1	RW	0x1	phy0_sram_bypass SRAM bypass Control signal when asserted, bypasses the SRAM interface.
0	RW	0x1	upcs_pwr_stable Power stable for upcs Status signal indicating that the power for the upcs is stable. The

GRF_PCIE30PHY_CON5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	rx0_eb_empty_mode_sel rx0_eb_empty_mode controll selection 1'b0: from PCIe controller 1'b1: from GRF
14	RW	0x0	tx0_disable TX disable control for lane X
13	RW	0x1	tx0_disable_sel tx_disable control selection 1'b0: from PCIe controller 1'b1: from GRF
12	RW	0x0	rx0_disable RX disable control for lane X This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.
11	RW	0x1	rx0_disable_sel rx_disable control selection 1'b0: from PCIe controller 1'b1: from GRF
10	RW	0x0	rx0_eb_empty_mode Elastic buffer mode for lane X Selects Elasticity Buffer operating mode. 1'b0: Nominal Half-Full Buffer mode 1'b1: Hybrid Pipe Buffer Mode
9	RW	0x1	rx0_cmn_refclk_mode RX common reference clock mode for lane X This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.
8	RW	0x0	rx0_sris_mode_en RX SRIS ECM mode enable for lane X When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data. Note: Any change to this input must be followed by phy_reset assertion.
7	RW	0x1	rx0_termination Receiver termination control
6	RW	0x0	lane0_clkreq_n Clock request for lane 0
5	RW	0x0	lane0_tx2rx_loopbk TX-to-RX loopback enable for lane X When asserted, this input turns on the TX-to-RX serial loopback within the PHY.

Bit	Attr	Reset Value	Description
4	RW	0x1	lane0_mpll_mode Sets MPLL bandwidth and lock time. Set this signal based on the chosen PCIe refclk architecture in the system (common clock versus separate clock). 1'b0: Normal MPLL bandwidth and lock time (use for PCIe separate refclk architecture) 1'b1: Higher MPLL bandwidth and shorter lock time (use for PCIe common refclk architecture)
3:0	RW	0x0	lane0_link_num Link number for lane X Link number of lane X used for bifurcation. Each lane can be assigned to any link using this input. The TX lane-to-lane skew within the PCS for lanes that are part of the same link is zero UI (0 UI).

GRF_PCIE30PHY_CON6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RW	0x0	rx1_eb_empty_mode_sel rx0_eb_empty_mode controll selection 1'b0: from PCIe controller 1'b1: from GRF
14	RW	0x0	tx1_disable TX disable control for lane X
13	RW	0x1	tx1_disable_sel tx_disable control selection 1'b0: from PCIe controller 1'b1: from GRF
12	RW	0x0	rx1_disable RX disable control for lane X This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.
11	RW	0x1	rx1_disable_sel rx_disable control selection 1'b0: from PCIe controller 1'b1: from GRF
10	RW	0x0	rx1_eb_empty_mode Elastic buffer mode for lane X Selects Elasticity Buffer operating mode. 1'b0: Nominal Half-Full Buffer mode 1'b1: Hybrid Pipe Buffer Mode
9	RW	0x1	rx1_cmn_refclk_mode RX common reference clock mode for lane X This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.

Bit	Attr	Reset Value	Description
8	RW	0x0	rx1_sris_mode_en RX SRIS ECM mode enable for lane X When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data.
7	RW	0x1	rx1_termination Receiver termination control
6	RW	0x0	lane1_clkreq_n Clock request for lane 0
5	RW	0x0	lane1_tx2rx_loopbk TX-to-RX loopback enable for lane X When asserted, this input turns on the TX-to-RX serial loopback within the PHY.
4	RW	0x1	lane1_mpll_mode Sets MPLL bandwidth and lock time. Set this signal based on the chosen PCIe refclk architecture in the system (common clock versus separate clock). 1'b0: Normal MPLL bandwidth and lock time (use for PCIe separate refclk architecture) 1'b1: Higher MPLL bandwidth and shorter lock time (use for PCIe common refclk architecture)
3:0	RW	0x0	lane1_link_num Link number for lane X Link number of lane X used for bifurcation. Each lane can be assigned to any link using this input. The TX lane-to-lane skew within the PCS for lanes that are part of the same link is zero UI (0 UI).

GRF_PCIE30PHY_CON7

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11:6	RW	0x00	rx1_idle_los_cnt_g1 RX IDLE Loss-of-Signal Counter for Gen1 Determines the number of PHY RX LOS samples of 1 (loss of signal samples) to consider the RX as electrical idle. When pcs_rxX_idle_los_cnt_g1[5:0] is 0, this feature is disabled and only EIOS detection is used to determine RX electrical idle condition. When pcs_rxX_idle_los_cnt_g1[5:0] is non-zero (for example, N: if phy_rxX_los = 1 for N number of pcs_laneX_clk clock cycles consecutively), the subsequent data is considered invalid data and pipe_rxX_valid is deasserted.

Bit	Attr	Reset Value	Description
5:0	RW	0x00	rx0_idle_los_cnt_g1 RX IDLE Loss-of-Signal Counter for Gen1 Determines the number of PHY RX LOS samples of 1 (loss of signal samples) to consider the RX as electrical idle. When pcs_rxX_idle_los_cnt_g1[5:0] is 0, this feature is disabled and only EIOS detection is used to determine RX electrical idle condition. When pcs_rxX_idle_los_cnt_g1[5:0] is non-zero (for example, N: if phy_rxX_los = 1 for N number of pcs_laneX_clk clock cycles consecutively), the subsequent data is considered invalid data and pipe_rxX_valid is deasserted.

GRF_PCIE30PHY_CON8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	pipe_lane0_powerdown control select pipe_lane0_powerdown control select 1'b0: from pcie30x2_mac2phy_powerdown 1'b1: from grf_pcie30phy_con9[3:0]
5	RW	0x1	pipe_rx0_standby grf control pipe_rx0_standby
4	RW	0x0	pipe_rx0_standby control select rxstandby_to_phy control selection 1'b0: from pcie3_l0_mac2phy_rxstandby_to_phy 1'b1: from grf_pcie30phy_con8[5]
3	RW	0x1	pipe_tx0_compliance grf control pipe_tx0_compliance
2	RW	0x0	pipe_tx0_compliance control select tx0_compliance control selection 1'b0: from pcie30_l0_mac2phy_txcompliance 1'b1: from grf_pcie30phy_con8[3]
1	RW	0x1	pipe_tx0_txelecidle grf control pipe_tx0_txelecidle
0	RW	0x0	pipe_tx0_elecidle control select tx0_elecidle control selection 1'b0: from pcie30_l0_mac2phy_txelecidle 1'b1: from grf_pcie30phy_con8[1]

GRF_PCIE30PHY_CON9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x3	pipe_lane1_powerdown grf control lane1_powerdown
3:0	RW	0x3	pipe_lane0_powerdown grf control pipe_lane0_powerdown

GRF_PCIE30PHY_STATUS0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	phy0_mpllb_state MPLLB state indicator

Bit	Attr	Reset Value	Description
29	RW	0x0	phy0_ref_clkdet_result Reference Clock Detection result
28	RW	0x0	phy0_mplla_force_ack MPLLA Force Acknowledge
27	RW	0x0	phy0_mplla_state MPLLA state indicator
26	RW	0x0	phy0_pma_pwr_en Power enable for PMA power switch Enable signal for PMA power switch (internal or external) to supply power to the PMA.
25	RW	0x0	phy0_pcs_pwr_en Power enable for PCS power switch(es) Enable signal for external switch(es) to supply power to the power-gated logic in the PCS. For information about power gating
24	RW	0x0	pipe_rx1_align_detect RX ALIGN symbol detected for lane 1
23:22	RW	0x0	pipe_lane1_databuswidth Bus width configuration for lane 1
21	RW	0x0	pipe_lane1_clkack_n Clock acknowledge for lane 0
20	RW	0x0	pipe_rx0_align_detect RX ALIGN symbol detected for lane 0
19:18	RW	0x0	pipe_lane0_databuswidth Bus width configuration for lane0
17	RW	0x0	pipe_lane0_clkack_n Clock acknowledge for lane 0
16	RW	0x0	upcs_pwr_en Power enable for PCS power switch(es) Enable signal for external switch(es) to supply power to the power-gated logic in the PCS. For information about power gating
15	RW	0x0	phy_rtune_ack Resistor tune acknowledge Indicates that a resistor tune has completed
14	RW	0x0	sram_init_done SRAM Initialization done Signal indicating that the SRAM has been initialized by the boot
13	RW	0x0	phy_rx1_ppm_drift_vld RX CDR PPM Drift Valid Indicates when the rxX_ppm_drift[5:0] output is valid and can be sampled.
12:7	RW	0x00	phy_rx1_ppm_drift RX CDR PPM Drift This value represents the amount of ppm on the rxX_clk with respect to the ideal desired frequency.
6	RW	0x0	phy_rx0_ppm_drift_vld RX CDR PPM Drift Valid Indicates when the rxX_ppm_drift[5:0] output is valid and can be sampled.
5:0	RW	0x00	phy_rx0_ppm_drift RX CDR PPM Drift This value represents the amount of ppm on the rxX_clk with respect to the ideal desired frequency.

GRF_PCIE30PHY_STATUS1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	pipe_rx1_ebuff_location Entries in elastic buffer for lane 1
8:0	RW	0x000	pipe_rx0_ebuff_location Entries in elastic buffer for lane 0

GRF_PCIE30PHY_STATUS2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	pipe_lane1_max_pclk
23	RW	0x0	pipe_lane0_max_pclk
22	RW	0x0	phy0_ref_repeat_clk_p
21	RW	0x0	phy0_ref_repeat_clk_m
20	RW	0x0	phy0_mplla_dword_clk
19	RW	0x0	phy0_mplla_div_clk
18	RW	0x0	phy0_mplla_div66_clk
17	RW	0x0	phy0_mplla_div33_clk
16	RW	0x0	phy0_ref_dig_fr_clk
15	RW	0x0	phy0_ref_dig_clk
14	RW	0x0	phy0_mpllb_word_fr_clk
13	RW	0x0	phy0_mpllb_word_clk
12	RO	0x0	reserved
11	RW	0x0	phy0_mpllb_qword_clk
10	RW	0x0	phy0_mpllb_oword_clk
9	RW	0x0	phy0_mpllb_force_ack
8	RW	0x0	phy0_mpllb_dword_clk
7	RW	0x0	phy0_mpllb_div_fr_clk
6	RW	0x0	phy0_mpllb_div_clk
5	RW	0x0	phy0_mplla_word_rf_clk
4	RW	0x0	phy0_mplla_word_clk
3	RO	0x0	reserved
2	RW	0x0	phy0_mplla_qword_clk
1	RW	0x0	phy0_mplla_oword_clk
0	RW	0x0	phy0_mplla_div_fr_clk Free-running MPLLA divide clock This clock is intended to be used for scan on-chip clocking mode.Whenscan_pma_occ_en is asserted, this clock stays running during scan_mode.

GRF_PCIE30PHY_PRT0_CON0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	protocol0_ext_mplla_bandwidth MPLLA bandwidth control.

GRF_PCIE30PHY_PRT0_CON1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5	RO	0x0	reserved
4:0	RO	0x00	reserved

GRF_PCIE30PHY_PRT0_CON2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	protocol0_ext_mplla_div_clk_en MPLLA divide clock enable When asserted, the frequency of the mpll(a,b)_div_clk output clock is the MPLL(A,B) frequency divided by mpll(a,b)_div_multiplier[6:0].Fractional division and/or SSC is additionally applied to mpll(a,b)_div_clk depending on the settings of mpll(a,b)_ssc_en and mpll(a,b)_fracn_ctrl[8:0]. These inputs can only be changed when the respective mpll(a,b)_ssc_en and txX_mpll_en inputs are de-asserted.
9	RW	0x0	protocol0_ext_mplla_div8_clk_en MPLLA divide by 8 enable When asserted, the frequency of the mpll(a,b)_word_clk output clock is the MPLL(A,B) frequency divided by 8. If mpll(a,b)_div10_clk_en is also asserted, then divide by 10 takes priority. These inputs can only be changed when the txX_mpll_en input is deasserted.
8	RW	0x0	protocol0_ext_mplla_div16p5_clk_en MPLLA divide by 16.5 enable
7	RW	0x0	protocol0_ext_mplla_div10_clk_en MPLLA divide by 10 enable When asserted, the frequency of the mpll(a,b)_word_clk output clock is the MPLL(A,B) frequency divided by 10. This divide by 10 takes priority over mpll(a,b)_div8_clk_en. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted
6:0	RW	0x00	protocol0_ext_mplla_div_multiplier MPLLA output frequency multiplier control Frequency multiplication factor used to generate MPLL clock output from the reference clock input as seen by the MPLL (after ref_clk_div2_en and ref_clk_mplla_div2_en/ref_clk_mpllb_div2_en dividers). This input can only be changed when the txX_mpll_en inputs for all lanes are de-asserted.

GRF_PCIE30PHY_PRT0_CON3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:11	RO	0x00	reserved
10:0	RW	0x000	protocol0_ext_mplla_fracn_ctrl MPLLA fractional control MPLL(A,B) fractional control input to be set as per the tables in the"Support Configuration Settings" appendix and the "Lane Configuration Settings" appendix.

GRF_PCIE30PHY_PRT0_CON4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	protocol0_ext_mplla_ssc_clk_sel MPLLA spread spectrum clock select MPLL(A,B) clock select for generating spread spectrum.
8	RW	0x0	protocol0_ext_mplla_short_lock_en MPLLA short lock enable Enables short lock mode for MPLLA.
7:0	RW	0x00	protocol0_ext_mplla_multiplier MPLLA frequency multiplier control Multiplies the reference clock to a frequency suitable for intended operating speed.

GRF_PCIE30PHY_PRT0_CON5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x800	protocol0_ext_mplla_ssc_freq_cnt_init MPLLA SSC Frequency Counter Initialization

GRF_PCIE30PHY_PRT0_CON6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11	RW	0x1	protocol0_ext_mplla_ssc_up_spread MPLLA SSC Up Spread Enable When asserted, the SSC is applied in upwards direction (positive ppm) and when deasserted the SSC is applied downwards (negative ppm).

Bit	Attr	Reset Value	Description
10:8	RW	0x0	protocol0_ext_mplla_tx_clk_div MPLLA TX Clock Divider Sets the divide ratio on the MPLL clock sent to the TX as follows: 2'b00 : div1 2'b01 : div2 2'b10 : div4 2'b11 : div1 (duplicate state)
7:0	RW	0x00	protocol0_ext_mplla_ssc_freq_cnt_peak MPLLA SSC Frequency Counter Peak Sets the peak value for the SSC frequency counter.

GRF_PCIE30PHY_PRT0_CON7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:0	RW	0x0000	protocol0_ext_mpllb_bandwidth MPLLB bandwidth control

GRF_PCIE30PHY_PRT0_CON8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	protocol0_ext_mpllb_div_clk_en MPLLB divide clock enable When asserted, the frequency of the mpll(a,b)_div_clk output clock is the MPLL(A,B) frequency divided by mpll(a,b)_div_multiplier[6:0]. Fractional division and/or SSC is additionally applied to mpll(a,b)_div_clk depending on the settings of mpll(a,b)_ssc_en and mpll(a,b)_fracn_ctrl[8:0].
8	RW	0x0	protocol0_ext_mpllb_div8_clk_en MPLLB divide by 8 enable When asserted, the frequency of the mpll(a,b)_word_clk output clock is the MPLL(A,B) frequency divided by 8. If mpl(a,b)_div10_clk_en is also asserted, then divide by 10 takes priority. These inputs can only be changed when the txX_mpll_en input is deasserted.
7	RW	0x0	protocol0_ext_mpllb_div10_clk_en MPLLB divide by 10 enable When asserted, the frequency of the mpll(a,b)_word_clk output clock is the MPLL(A,B) frequency divided by 10. This divide by 10 takes priority over mpll(a,b)_div8_clk_en. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted.

Bit	Attr	Reset Value	Description
6:0	RW	0x00	protocol0_ext_mpllb_div_multiplier MPLLB output frequency multiplier control Frequency multiplication factor used to generate MPLL clock output from the reference clock input as seen by the MPLL (after ref_clk_div2_en and ref_clk_mplla_div2_en/ref_clk_mpllb_div2_en dividers). This input can only be changed when the txX_mpll_en inputs for all lanes are de-asserted.

GRF_PCIE30PHY_PRT0_CON9

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:11	RO	0x00	reserved
10:0	RW	0x000	protocol0_ext_mpllb_fracn_ctrl MPLLB fractional control

GRF_PCIE30PHY_PRT0_CON10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	protocol0_ext_mpllb_ssc_clk_sel MPLLB spread spectrum clock select.
8	RW	0x0	protocol0_ext_mpllb_short_lock_en MPLLB short lock enable.
7:0	RW	0x00	protocol0_ext_mpllb_multiplier x'bxxx(bits < 4), x'hxxxx(bits >= 4)

GRF_PCIE30PHY_PRT0_CON11

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x000	protocol0_ext_mpllb_ssc_freq_cnt_init MPLLB SSC Frequency Counter Initialization.

GRF_PCIE30PHY_PRT0_CON12

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	protocol0_ext_mpllb_ssc_up_spread MPLLB SSC Up Spread Enable When asserted, the SSC is applied in upwards direction (positive ppm) and when deasserted the SSC is applied downwards (negative ppm).
10:8	RW	0x0	protocol0_ext_mpllb_tx_clk_div MPLLB TX Clock Divider Sets the divide ratio on the MPLL clock sent to the TX as follows: 2'b00 : div1 2'b01 : div2 2'b10 : div4 2'b11 : div1 (duplicate state)
7:0	RW	0x00	protocol0_ext_mpllb_ssc_freq_cnt_peak MPLLB SSC Frequency Counter Peak Sets the peak value for the SSC frequency counter.

GRF_PCIE30PHY_PRT0_CON13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	protocol0_ext_ref_clk_mpllb_div2_en MPLLB reference clock divider control The reference clock used for MPLLB calibration and locking can be divided by 2. This division is applied after ref_clk_div2_en. Hence the total division ratio (from the input reference clock) can be 1, 2 or 4.
4	RW	0x0	protocol0_ext_ref_clk_mplla_div2_en MPLLA reference clock divider control The reference clock used for MPLLA calibration and locking can be divided by 2. This division is applied after ref_clk_div2_en. Hence the division ratio (from the input reference clock) can be 1, 2 or 4.
3	RW	0x0	protocol0_ext_ref_clk_div2_en Input reference clock divider control The reference clock is divided by 2 when asserted. Any change in this input must be followed by phy_reset assertion.
2:0	RW	0x0	protocol0_ext_ref_range Input reference clock frequency range Specifies the frequency range of the input reference clock (post ref_clk_div2_en division if any). The code mapping of ref_range is as follows: 3'b000: 20 - 26 MHz 3'b001: 26.1 - 52 MHz 3'b010: 52.1 - 78 MHz 3'b011: 78.1 - 104 MHz 3'b100: 104.1 - 130 MHz 3'b101: 130.1 - 156 MHz 3'b110: 156.1 - 182 MHz 3'b111: 182.1 - 200 MHz Any change in this input must be followed by phy_reset assertion.

GRF_PCIE30PHY_PRT0_CON14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	protocol0_ext_rx_adapt_dfe_en_g3 RX adaptation enable Enables the RX adaptation circuitry
4	RW	0x0	protocol0_ext_rx_adapt_dfe_en_g2 RX adaptation enable Enables the RX adaptation circuitry
3	RW	0x0	protocol0_ext_rx_adapt_dfe_en_g1 RX adaptation enable Enables the RX adaptation circuitry
2	RW	0x0	protocol0_ext_rx_adapt_afe_en_g3 RX adaptation enable Enables the RX adaptation circuitry
1	RW	0x0	protocol0_ext_rx_adapt_afe_en_g2 RX adaptation enable Enables the RX adaptation circuitry
0	RW	0x0	protocol0_ext_rx_adapt_afe_en_g1 RX adaptation enable Enables the RX adaptation circuitry

GRF_PCIE30PHY_PRT0_CON15

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	protocol0_ext_rx_cdr_ppm_max_g3 Maximum Allowed PPM on the RX CDR Clock This input specifies the maximum PPM drift to be allowed on the RX clock (relative to ideal desired frequency) before the CDR recovery circuit is engaged.
9:5	RW	0x00	protocol0_ext_rx_cdr_ppm_max_g2 Maximum Allowed PPM on the RX CDR Clock This input specifies the maximum PPM drift to be allowed on the RX clock (relative to ideal desired frequency) before the CDR recovery circuit is engaged.
4:0	RW	0x00	protocol0_ext_rx_cdr_ppm_max_g1 Maximum Allowed PPM on the RX CDR Clock This input specifies the maximum PPM drift to be allowed on the RX clock (relative to ideal desired frequency) before the CDR recovery circuit is engaged.

GRF_PCIE30PHY_PRT0_CON16

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	protocol0_ext_rx_cdr_vco_freqband_g3 RX CDR VCO Frequency Band Controls coarse-DAC step-size based on data rate and VPH level.
3:2	RW	0x0	protocol0_ext_rx_cdr_vco_freqband_g2 RX CDR VCO Frequency Band Controls coarse-DAC step-size based on data rate and VPH level.
1:0	RW	0x0	protocol0_ext_rx_cdr_vco_freqband_g1 RX CDR VCO Frequency Band Controls coarse-DAC step-size based on data rate and VPH level.

GRF_PCIE30PHY_PRT0_CON17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	protocol0_ext_rx_delta_iq_g3 IQ offset value Indicates the amount of additional offset to apply to the Inphase/Quadrature (IQ) separation. This is an unsigned offset value and covers a range of 0UI to 0.2UI.
7:4	RW	0x0	protocol0_ext_rx_delta_iq_g2 IQ offset value Indicates the amount of additional offset to apply to the Inphase/Quadrature (IQ) separation. This is an unsigned offset value and covers a range of 0UI to 0.2UI.
3:0	RW	0x0	protocol0_ext_rx_delta_iq_g1 IQ offset value Indicates the amount of additional offset to apply to the Inphase/Quadrature (IQ) separation. This is an unsigned offset value and covers a range of 0UI to 0.2UI.

GRF_PCIE30PHY_PRT0_CON18

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x0	protocol0_ext_rx_eq_att_lvl_g3 RX equalization attenuation level Controls the AFE attenuation level from -2dB when set to 3'b000, to -6dB when set to 3'b111; binary encoded.

Bit	Attr	Reset Value	Description
5:3	RW	0x0	protocol0_ext_rx_eq_att_lvl_g2 RX equalization attenuation level Controls the AFE attenuation level from -2dB when set to 3'b000, to -6dB when set to 3'b111; binary encoded.
2:0	RW	0x0	protocol0_ext_rx_eq_att_lvl_g1 RX equalization attenuation level Controls the AFE attenuation level from -2dB when set to 3'b000, to -6dB when set to 3'b111; binary encoded.

GRF_PCIE30PHY_PRT0_CON19

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	protocol0_ext_rx_eq_ctle_boost_g3 RX equalization CTLE boost Controls the CTLE boost level; binary encoded.
9:5	RW	0x00	protocol0_ext_rx_eq_ctle_boost_g2 RX equalization CTLE boost Controls the CTLE boost level; binary encoded.
4:0	RW	0x00	protocol0_ext_rx_eq_ctle_boost_g1 RX equalization CTLE boost Controls the CTLE boost level; binary encoded.

GRF_PCIE30PHY_PRT0_CON20

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x0	protocol0_ext_rx_eq_ctle_pole_g3 RX equalization CTLE pole Controls the continuous time linear equalizer (CTLE) boost pole location; binary encoded.
5:3	RW	0x0	protocol0_ext_rx_eq_ctle_pole_g2 RX equalization CTLE pole Controls the continuous time linear equalizer (CTLE) boost pole location; binary encoded.
2:0	RW	0x0	protocol0_ext_rx_eq_ctle_pole_g1 RX equalization CTLE pole Controls the continuous time linear equalizer (CTLE) boost pole location; binary encoded.

GRF_PCIE30PHY_PRT0_CON21

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable

Bit	Attr	Reset Value	Description
15:8	RW	0x00	protocol0_ext_rx_eq_dfe_tap1_g2 RX equalization DFE Tap1 Controls the value of DFE data Tap1. This is a signed input; two's complement encoded.
7:0	RW	0x00	protocol0_ext_rx_eq_dfe_tap1_g1 RX equalization DFE Tap1 Controls the value of DFE data Tap1. This is a signed input; two's complement encoded.

GRF_PCIE30PHY_PRT0_CON22

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RW	0x0	protocol0_ext_rx_eq_vga1_gain_g2 RX equalization VGA gain 1 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.
11:8	RW	0x0	protocol0_ext_rx_eq_vga1_gain_g1 RX equalization VGA gain 1 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.
7:0	RW	0x00	protocol0_ext_rx_eq_dfe_tap1_g3 RX equalization DFE Tap1 Controls the value of DFE data Tap1. This is a signed input; two's complement encoded.

GRF_PCIE30PHY_PRT0_CON23

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RW	0x0	protocol0_ext_rx_eq_vga2_gain_g3 RX equalization VGA gain 2 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.
11:8	RW	0x0	protocol0_ext_rx_eq_vga2_gain_g2 RX equalization VGA gain 2 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.
7:4	RW	0x0	protocol0_ext_rx_eq_vga2_gain_g1 RX equalization VGA gain 2 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.
3:0	RW	0x0	protocol0_ext_rx_eq_vga1_gain_g3 RX equalization VGA gain 1 Controls the AFE first stage Variable Gain Amplifier gain; binary encoded.

GRF_PCIE30PHY_PRT0_CON24

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	protocol0_ext_rx_los_lfps_en Receiver LOS LFPS enable
1:0	RW	0x0	protocol0_ext_rx_los_threshold Receiver LOS threshold Sets the LOS threshold level trip point. It is recommended to set this input to 3'b001 for PCIe and 3'b010 for SATA. 3'b000, LOS threshold=Reserved 3'b001, LOS threshold=90 mVpp 3'b010, LOS threshold=120 mVpp 3'b011, LOS threshold=150 mVpp 3'b100, LOS threshold=180 mVpp 3'b101, LOS threshold=210 mVpp 3'b110, LOS threshold=240 mVpp 3'b111, LOS threshold=270 mVpp Voltage Range: 0-vpdig

GRF_PCIE30PHY_PRT0_CON25

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:8	RW	0x00	protocol0_ext_rx_misc_g2 RX Miscellaneous Controls This input controls miscellaneous settings in the RX.
7:0	RW	0x00	protocol0_ext_rx_misc_g1 RX Miscellaneous Controls This input controls miscellaneous settings in the RX.

GRF_PCIE30PHY_PRT0_CON26

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x00	protocol0_ext_rx_misc_g3 RX Miscellaneous Controls This input controls miscellaneous settings in the RX.

GRF_PCIE30PHY_PRT0_CON27

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:6	RW	0x00	protocol0_ext_rx_ref_ld_val_g2 RX VCO calibration reference load value This input is used to load internal calibration registers used to perform RX VCO calibration.
5:0	RW	0x00	protocol0_ext_rx_ref_ld_val_g1 RX VCO calibration reference load value This input is used to load internal calibration registers used to perform RX VCO calibration.

GRF_PCIE30PHY_PRT0_CON28

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x00	protocol0_ext_rx_ref_ld_val_g3 RX VCO calibration reference load value This input is used to load internal calibration registers used to perform RX VCO calibration.

GRF_PCIE30PHY_PRT0_CON29

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:13	RO	0x0	reserved
12:0	RW	0x0000	protocol0_ext_rx_vco_ld_val_g1 RX VCO calibration load value This input is used to load internal calibration registers used to perform RX VCO calibration.

GRF_PCIE30PHY_PRT0_CON30

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:13	RO	0x0	reserved
12:0	RW	0x0000	protocol0_ext_rx_vco_ld_val_g2 RX VCO calibration load value This input is used to load internal calibration registers used to perform RX VCO calibration.

GRF_PCIE30PHY_PRT0_CON31

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0000	protocol0_ext_rx_vco_ld_val_g3 RX VCO calibration load value This input is used to load internal calibration registers used to perform RX VCO calibration.

GRF_PCIE30PHY_PRT0_CON32

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	protocol0_ext_rx_vref_ctrl RX biasing current control Sets the RX biasing current for RX analog front end. The recommended default setting for this input is 5'b01111. Voltage Range: 0-vpdig
7:0	RW	0x00	protocol0_ext_sup_misc Support Miscellaneous Controls This input controls miscellaneous settings in the Support block.

GRF_PCIE30PHY_PRT0_CON33

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:10	RO	0x00	reserved
9:5	RW	0x00	protocol0_ext_tx_eq_main_g2 Transmitter amplitude adjustment control Control for setting the transmitter driver output amplitude (main coefficient) tx_eq_main[5:0]: Integer value (0 to 40)
4:0	RW	0x00	protocol0_ext_tx_eq_main_g1 Transmitter amplitude adjustment control Control for setting the transmitter driver output amplitude (main coefficient) tx_eq_main[5:0]: Integer value (0 to 40)

GRF_PCIE30PHY_PRT0_CON34

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x00	protocol0_ext_tx_eq_main_g3 Transmitter amplitude adjustment control Control for setting the transmitter driver output amplitude (main coefficient) tx_eq_main[5:0]: Integer value (0 to 40)

GRF_PCIE30PHY_PRT0_CON35

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15	RO	0x0	reserved
14	RW	0x0	protocol0_ext_tx_eq_ovrd_g3 Gen3 tx eq Override
13	RW	0x0	protocol0_ext_tx_eq_ovrd_g2 Gen2 tx eq Override
12	RW	0x0	protocol0_ext_tx_eq_ovrd_g1 Gen1 tx eq Override
11:6	RW	0x00	protocol0_ext_tx_eq_post_g2 Transmitter Post-Emphasis level adjustment control Control for setting the transmitter driver output post- emphasis (post coefficient) tx_eq_post[5:2]: Integer value (0 to 15) tx_eq_post[1:0]: Fraction value (0, 0.25, 0.5, 0.75)
5:0	RW	0x00	protocol0_ext_tx_eq_post_g1 Transmitter Post-Emphasis level adjustment control Control for setting the transmitter driver output post- emphasis (post coefficient) tx_eq_post[5:2]: Integer value (0 to 15) tx_eq_post[1:0]: Fraction value (0, 0.25, 0.5, 0.75)

GRF_PCIE30PHY_PRT0_CON36

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:12	RO	0x0	reserved
11:6	RW	0x00	protocol0_ext_tx_eq_pre_g1 Transmitter Pre-Emphasis level adjustment control Control for setting the transmitter driver output pre-emphasis(preshoot coefficient) tx_eq_pre[5:2]: Integer value (0 to10) tx_eq_pre[1:0]: Fraction value (0, 0.25, 0.5, 0.75)
5:0	RW	0x00	protocol0_ext_tx_eq_post_g3 Transmitter Post-Emphasis level adjustment control Control for setting the transmitter driver output post- emphasis (post coefficient) tx_eq_post[5:2]: Integer value (0 to 15) tx_eq_post[1:0]: Fraction value (0, 0.25, 0.5, 0.75)

GRF_PCIE30PHY_PRT0_CON37

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x0	protocol0_ext_tx_iboost_lvl Typical TX Launch Amplitude Vswing (mVppd) 4'b0000: 912 4'b0001: 925 4'b0010: 939 4'b0011: 950 4'b0100: 962 4'b0101: 975 4'b0110: 987 4'b0111: 1000 4'b1000: 1012 4'b1001: 1025 4'b1010: 1037 4'b1011: 1050 4'b1100: 1062 4'b1101: 1075 4'b1110: 1087 4'b1111: 1100
11:6	RW	0x00	protocol0_ext_tx_eq_pre_g3 Transmitter Pre-Emphasis level adjustment control Control for setting the transmitter driver output pre-emphasis(preshoot coefficient) tx_eq_pre[5:2]: Integer value (0 to10) tx_eq_pre[1:0]: Fraction value (0, 0.25, 0.5, 0.75)
5:0	RW	0x00	protocol0_ext_tx_eq_pre_g2 Transmitter Pre-Emphasis level adjustment control Control for setting the transmitter driver output pre-emphasis(preshoot coefficient) tx_eq_pre[5:2]: Integer value (0 to10) tx_eq_pre[1:0]: Fraction value (0, 0.25, 0.5, 0.75)

GRF_PCIE30PHY_PRT0_CON38

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable
15:8	RW	0x00	protocol0_ext_tx_misc_g2 TX Miscellaneous Controls This input controls miscellaneous settings in the TX analog block.
7:0	RW	0x00	protocol0_ext_tx_misc_g1 TX Miscellaneous Controls This input controls miscellaneous settings in the TX analog block.

GRF_PCIE30PHY_PRT0_CON39

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1:Write access enable

Bit	Attr	Reset Value	Description
15:8	RW	0x00	protocol0_ext_tx_vboost_lvl TX voltage boost maximum level Sets the maximum achievable TX swing. The recommended default setting for this input is 3'b100 (tx_vboost_vref= 0.252 V). Note: This signal does not set the actual TX swing, it only
7:0	RW	0x00	protocol0_ext_tx_misc_g3 TX Miscellaneous Controls This input controls miscellaneous settings in the TX analog block.

3.13 USB_GRF Register Description

3.13.1 Registers Summary

Name	Offset	Size	Reset Value	Description
USB_GRF_HOST0_CON0	0x0700	W	0x00000820	USB host control register0
USB_GRF_HOST0_CON1	0x0704	W	0x000004BC	USB host control register1
USB_GRF_HOST1_CON0	0x0708	W	0x00000820	USB host1 control register0
USB_GRF_HOST1_CON1	0x070C	W	0x000004BC	USB host1 control register1
USB_GRF_HOST0_STATUS	0x0890	W	0x00000000	USB host status register
USB_GRF_HOST1_STATUS	0x0894	W	0x00000000	USB host1 status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.13.2 Detail Registers Description

USB_GRF_HOST0_CON0

Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:6	RW	0x20	host0_fladj_val_common USB HOST0 fladj_val_common bit control
5:0	RW	0x20	host0_fladj_val USB HOST0 fladj bit control

USB_GRF_HOST0_CON1

Address: Operational Base + offset (0x0704)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	host0_arb_pause host0 ehci/ohci arbiter pause control
12	RW	0x0	host0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
11	RW	0x0	host0_ohci_cntsel USB HOST0 ohci_cntsel bit control
10	RW	0x1	host0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit control

Bit	Attr	Reset Value	Description
9	RW	0x0	host0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
8	RW	0x0	host0_autoppd_on_overcur_en USB HOST0 autoppd_on_overcur_en bit control
7	RW	0x1	host0_word_if USB HOST0 word_if bit control
6	RW	0x0	host0_sim_mode USB HOST0 sim_mode bit control 1'b0: Disable 1'b1: Enable
5	RW	0x1	host0_incrx_en USB HOST0 incrx_en bit control 1'b0: Disable 1'b1: Enable
4	RW	0x1	host0_incr8_en USB HOST0 incr8_en bit control 1'b0: Disable 1'b1: Enable
3	RW	0x1	host0_incr4_en USB HOST0 incr4_en bit control 1'b0: Disable 1'b1: Enable
2	RW	0x1	host0_incr16_en USB HOST0 incr16_en bit control 1'b0: Disable 1'b1: Enable
1	RW	0x0	host0_hubsetup_min USB HOST0 bubsetup_min bit control
0	RW	0x0	host0_app_start_clk USB HOST0 app_start_clk bit control

USB_GRF_HOST1_CON0

Address: Operational Base + offset (0x0708)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:6	RW	0x20	host1_fladj_val_common USB HOST1 fladj_val_common bit control
5:0	RW	0x20	host1_fladj_val USB HOST1 fladj bit control

USB_GRF_HOST1_CON1

Address: Operational Base + offset (0x070C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	host1_arb_pause host1 ehci/ohci arbiter pause control

Bit	Attr	Reset Value	Description
12	RW	0x0	host1_ohci_susp_lgcy USB HOST1 ohci_susp_lgcy bit control
11	RW	0x0	host1_ohci_cntsel USB HOST1 ohci_cntsel bit control
10	RW	0x1	host1_ohci_clkcktrst USB HOST1 ohci_clkcktrst bit control
9	RW	0x0	host1_app_prt_ovrcur USB HOST1 app_prt_ovrcur bit control
8	RW	0x0	host1_autoppd_on_overcur_en USB HOST1 autoppd_on_overcur_en bit control
7	RW	0x1	host1_word_if USB HOST1 word_if bit control
6	RW	0x0	host1_sim_mode USB HOST1 sim_mode bit control 1'b0: Disable 1'b1: Enable
5	RW	0x1	host1_incrx_en USB HOST1 incrx_en bit control 1'b0: Disable 1'b1: Enable
4	RW	0x1	host1_incr8_en USB HOST1 incr8_en bit control 1'b0: Disable 1'b1: Enable
3	RW	0x1	host1_incr4_en USB HOST1 incr4_en bit control 1'b0: Disable 1'b1: Enable
2	RW	0x1	host1_incr16_en USB HOST1 incr16_en bit control 1'b0: Disable 1'b1: Enable
1	RW	0x0	hos1_hubsetup_min USB HOST1 bubsetup_min bit control
0	RW	0x0	host1_app_start_clk USB HOST1 app_start_clk bit control

USB_GRF_HOST0_STATUS

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	host0_ehci_power_state_ack host0_ehci_power_state_ack bit status
29	RO	0x0	host0_ehci_pme_status host0_ehci_pme_status bit status
28	RO	0x0	host0_ehci_bufacc host0_ehci_bufacc bit status
27	RO	0x0	host0_ehci_xfer_prdc host0_ehci_xfer_prdc bit status
26	RO	0x0	host0_ohci_ccs host0_ohci_ccs bit status
25	RO	0x0	host0_ohci_rwe host0_ohci_rwe bit status
24	RO	0x0	host0_ohci_drwe host0_ohci_drwe bit status

Bit	Attr	Reset Value	Description
23	RO	0x0	host0_ohci_globalsuspend host0_ohci_globalsuspend bit status
22	RO	0x0	host0_ohci_bufacc host0_ohci_bufacc bit status
21	RO	0x0	host0_ohci_rmtwkp host0_ohci_rmtwkp bit status
20:17	RO	0x0	host0_ehci_lpsmc_state host0_ehci_lpsmc_state bit status
16:11	RO	0x00	host0_ehci_usbsts host0_ehci_usbsts bit status
10:0	RW	0x000	host0_ehci_xfer_cnt host0_ehci_xfer_cnt bit status

USB_GRF_HOST1_STATUS

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	host1_ehci_power_state_ack host1_ehci_power_state_ack bit status
29	RO	0x0	host1_ehci_pme_status host1_ehci_pme_status bit status
28	RO	0x0	host1_ehci_bufacc host1_ehci_bufacc bit status
27	RO	0x0	host1_ehci_xfer_prdc host1_ehci_xfer_prdc bit status
26	RO	0x0	host1_ohci_ccs host1_ohci_ccs bit status
25	RO	0x0	host1_ohci_rwe host1_ohci_rwe bit status
24	RO	0x0	host1_ohci_drwe host1_ohci_drwe bit status
23	RO	0x0	host1_ohci_globalsuspend host1_ohci_globalsuspend bit status
22	RO	0x0	host1_ohci_bufacc host1_ohci_bufacc bit status
21	RO	0x0	host1_ohci_rmtwkp host1_ohci_rmtwkp bit status
20:17	RO	0x0	host1_ehci_lpsmc_state host1_ehci_lpsmc_state bit status
16:11	RO	0x00	host1_ehci_usbsts host1_ehci_usbsts bit status
10:0	RW	0x000	host1_ehci_xfer_cnt host1_ehci_xfer_cnt bit status

Chapter 4 Cortex-A55

4.1 Overview

The RK3568 has a quad-core Cortex-A55 cluster with 512K L3 memory. Cortex-A55 processor, which is a mid-range, low-power processor that implements the ARMv8-A architecture.

The Cortex-A55 processor includes following features:

- Full implementation of the Armv8.2-A A64, A32, and T32 instruction sets
- Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3)
- In-order pipeline with direct and indirect branch prediction
- Separate L1 data and instruction side memory systems with a Memory Management Unit(MMU)
- Support for Arm TrustZone technology
- Support data engine that implements the Advanced SIMD and floating-point architecture support
- Support Cryptographic Extension
- ARMv8 debug logic
- Support Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor
- Generic Timers supporting 64-bit count input from an external system counter

The configuration details are shown in following tables

Table 4-1CPU Configuration

Number of CPU	4
L1 I cache size	32K
L1 D cache size	32K
L2 cache size	0
L3 cache size	512K
L3 data RAM output latency	2 cycles
L3 data RAM input latency	2 cycles
CPU cache protection	Yes
DSU L3 cache protection	Yes
BUS master interface	AXI4
NEON and floating point support	Yes
Cryptography extension	Yes

4.2 Block Diagram

The Cortex-A55 subsystem is shown in Figure 1-1. As illustrated, quad-core Cortex-A55 connects to system bus through DSU-L3 which can handle with CDC(clock domain crossing) issue.

The Cortex-A55 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

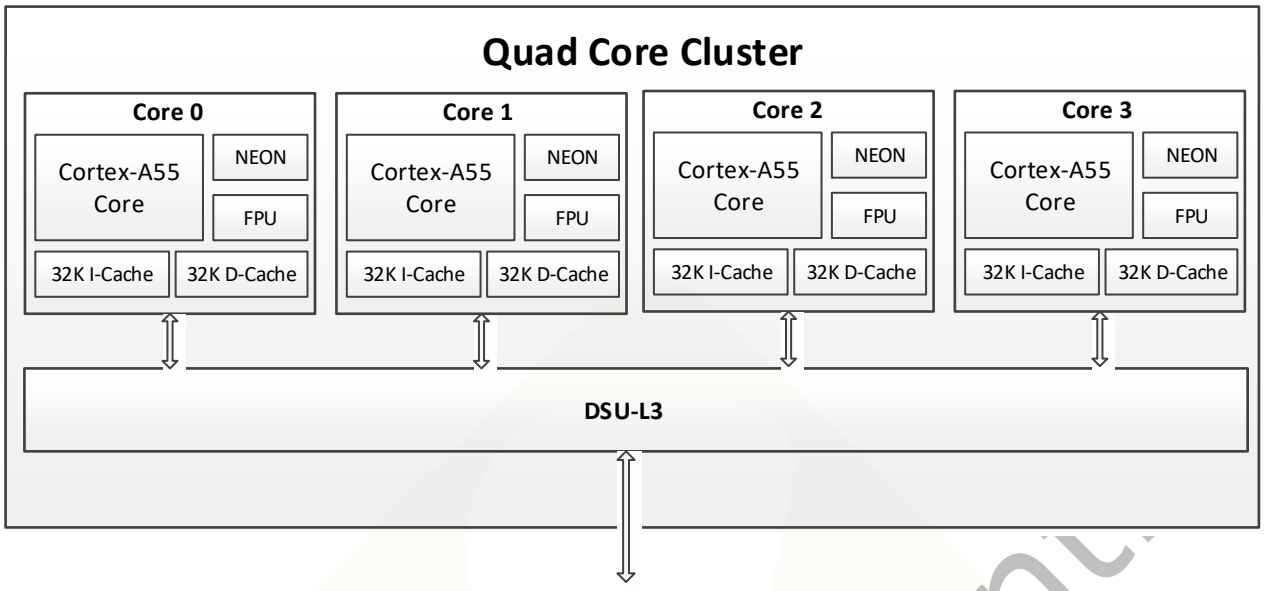


Fig. 4-1 Block Diagram

4.3 Function Description

Please refer to the document cortex_a55_r2p0_trm.pdf for the detail function description.

Chapter 5 Embedded SRAM

5.1 Overview

There are two embedded SRAMs, SYSTEM_SRAM and PMU_SRAM.

5.1.1 Features supported

- SYSTEM_SRAM
  - Provide 64KB access space
  - Support security and non-security access
  - Secure or non-secure space is software programmable
- PMU_SRAM
  - Provide 8KB access space
  - Support secure access only

5.2 Block Diagram

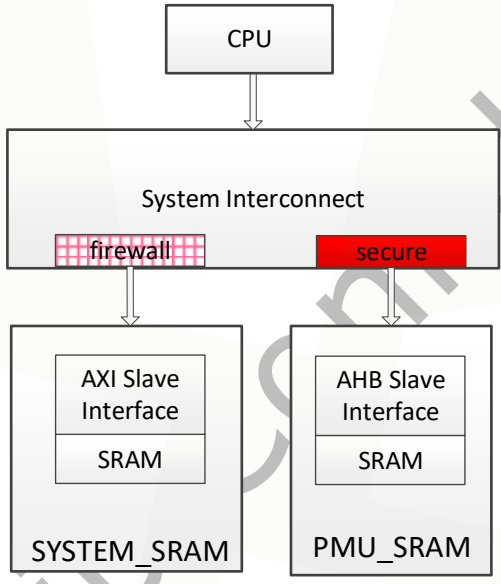


Fig. 5-1 Embedded SRAM block diagram

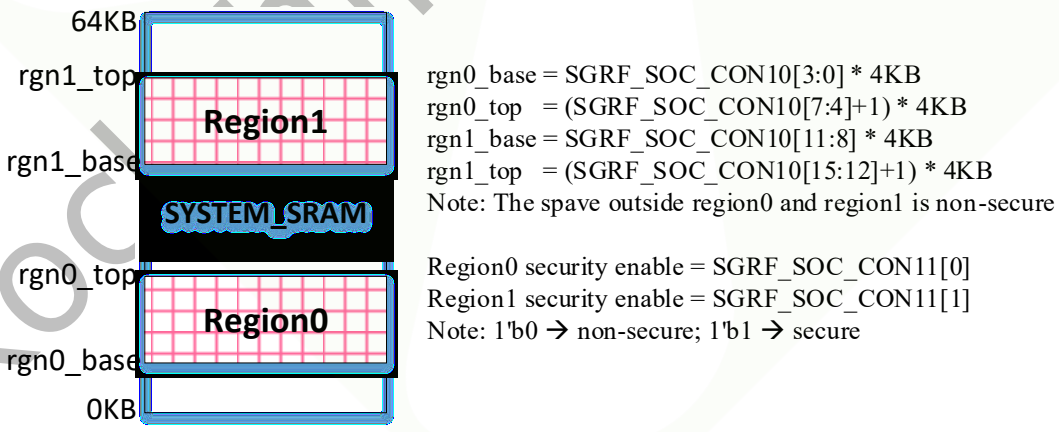


Fig. 5-2 SYSTEM_SRAM Security Configuration

5.3 Function Description

5.3.1 AXI slave interface of SYSTEM_SRAM

The AXI slave interface is bridge which translates AXI bus access to SRAM interface of SYSTEM_SRAM.

5.3.2 AHB slave interface of PMU_SRAM

The AHB slave interface is bridge which translates AHB bus access to SRAM interface of PMU_SRAM.

5.3.3 Embedded SRAM access path

The SYSTEM_SRAM can only be accessed by Cortex-A55, MCU, CRYPTO, DCF and DMAC. The PMU_SRAM can only be accessed by Cortex-A55, MCU, CRYPTO, DCF and DMAC.

Chapter 6 GPU(Graphics Process Unit)

6.1 Overview

The Mali-Gondul GPU is a graphics acceleration platform that is based on open standards. It supports 2D graphics, 3D graphics, and General Purpose computing on GPU (GPGPU).
The GPU hardware and software support compute standards and graphics API standards.
The GPU supports these compute API standards:

- OpenCL 2.0 Full Profile.

The GPU supports these graphics API standards:

- OpenGLES 1.1, 2.0, and 3.2.
- Vulkan 1.0 and 1.1.

The Arm Mali-Gondul GPU has significant features and properties.

- Compressed texture formats.
- Arm Frame Buffer Compression (AFBC) 1.2
- 8-bit, 10-bit and 16-bit YUV input and output formats
- L2 cache:128KB
- Support one Shader core and two execution engines

6.2 Block Diagram

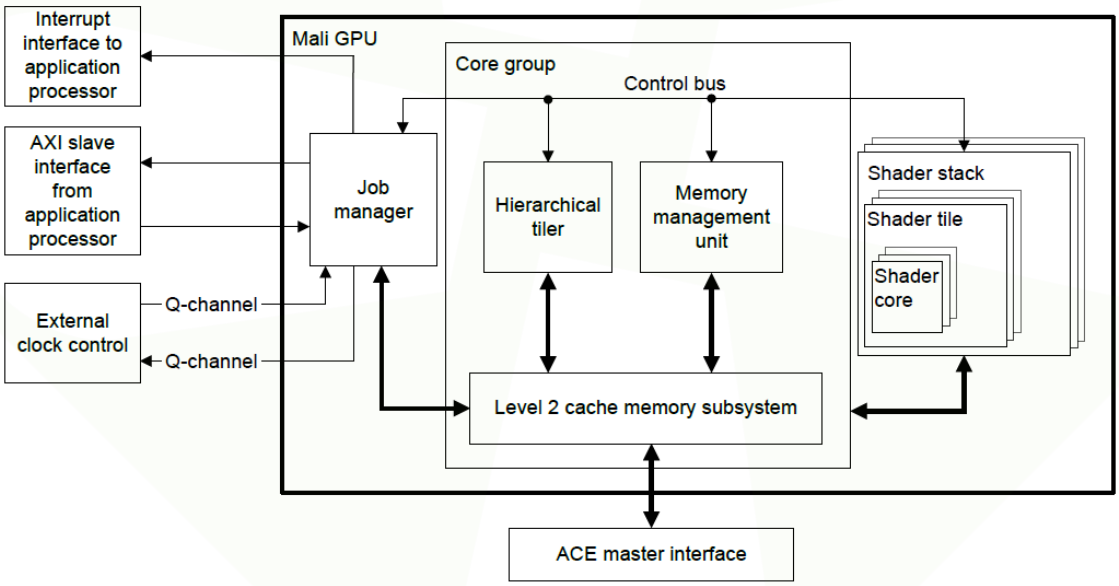


Fig. 6-1 GPU Architecture

6.3 Function Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

6.4 Register Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

Chapter 7 Power Management Unit (PMU)

7.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in RK3568. The RK3568 PMU is dedicated for managing the power of the whole chip.
PMU supports the following features:

- Support multi voltage domains: VD_CORE, VD_LOGIC, VD_PMU，VD_GPU,VD_NPU
- Support multi power domains in VD_CORE:PD_CPU_0, PD_CPU_1, PD_CPU_2, PD_CPU_3
- Support multi power domains in VD_LOGIC: PD_VPU, PD_RGA, PD_CENTER, PD_VI, PD_VO, PD_RKVDEC, PD_RKVENC, PD_PIPE
- Support PD_NPU act as power domain or voltage domain
- SupportBIU idle operations: BIU_MSCH, BIU_GPU, BIU_NPU, BIU_VI, BIU_VO, BIU_RGA, BIU_VPU, BIU_RKVDEC,BIU_RKVENC, BIU_GIC_AUDIO, BIU_SECURE_FLASH,BIU_PHP,BIU_PERIMID,BIU_PIPE,BIU_USB, BIU_PMU, BIU_BUS, BIU_TOP1, BIU_TOP2
- Support CPU auto power down and DSU auto power down
- Support CPU auto retention and DSU auto retention
- Support CPU auto emulation off and CPU auto debug recovery
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support to send idle request to BIU
- Support global interrupt disablein low power mode
- Support low frequency clock source from PVTM
- Support PMUclock switch to low frequencyclock in low power mode
- Support PLLspower down/up by hardware in low power mode
- Support OSC enable/disable request in low power mode
- Supportto clamp all VD_PMU input before power off VD_LOGIC in low power mode
- Support wakeup reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR controller clock auto gating in low power mode
- Support varies configurable wakeup source for low power mode

7.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB Interface and Register:Provide AMBA APB interface for registerread and write
- System Power State Control:Provide power management for various low power modes
- Power Gating Control:Provide power gating control for power domains

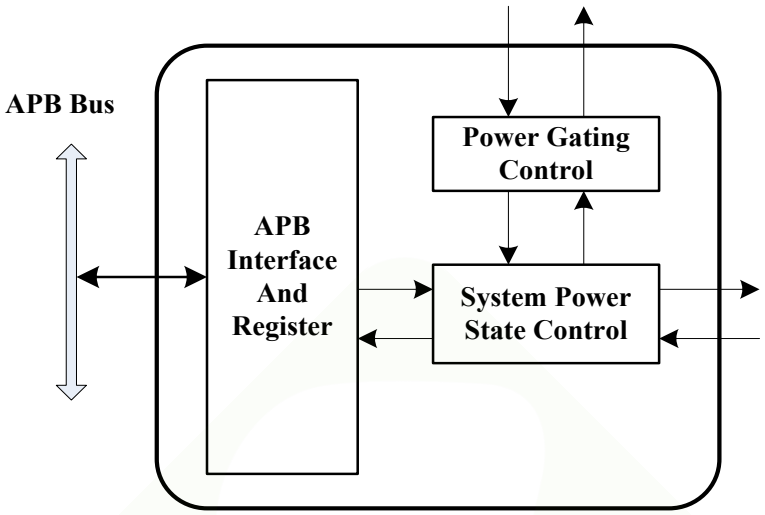


Fig.7-1PMU Bock Diagram

7.3 Function Description

7.3.1 DomainPartition

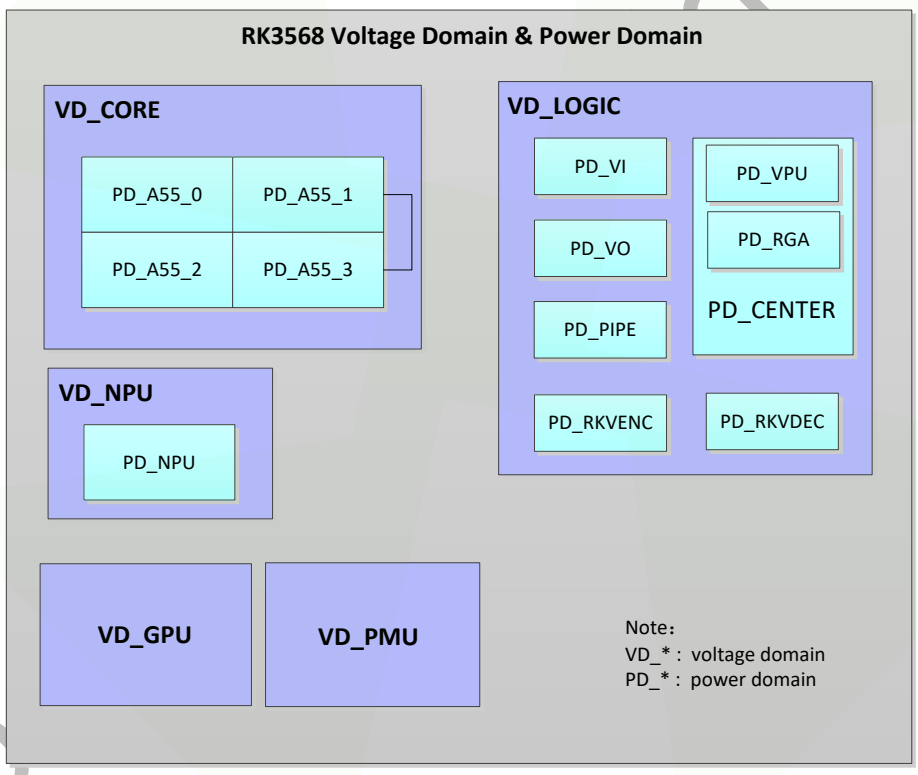


Fig.7-2RK3568Voltage Domain and Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table listsIPs in every power domain.

Table 7-1RK3568 Voltage Domain and Power Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE	PD_CPU_0	CPU CORE 0
	PD_CPU_1	CPU CORE 1
	PD_CPU_2	CPU CORE 2
	PD_CPU_3	CPU CORE 3
	ALIVE	BIU_CPU DSU,L3,DAP

Voltage Domain	Power Domain	Description
		PVTM,PVTPLL
VP_PMU	PD_PMU	BIU_PMU HPLL,PPLL PMU_SRAM SGRF PMU PMUCRU PMUGRF I2C0 GPIO0 PVTM UART0 PWM0
VD_NPU	PD_NPU	BIU_NPU RKNN PVTM,PVTPLL
VD_GPU	PD_GPU	BIU_GPU G52 PVTM,PVTPLL
VD_LOGIC	PD_VI	BIU_VI ISP VICAP CSIHOST
	PD_VO	BIU_VO VOP HDMI,HDCP DSIHOST EDP
	PD_RGA	BIU_RGA RGA IEP JPEG_DEC,JPEG_ENC EBC
	PD_VPU	BIU_VPU VPU
	PD_CENTER	BIU_MSCH DDR_UMCTL2 DDR_DFICTL DDR_MONITOR DDR_SCRAMBLE AXI_SPLIT DDR_GRF MSCH
	PD_RKVDEC	BIU_RKVDEC RKVDEC
	PD_RKVENC	BIU_RKVENC RKVENC
	PD_PIPE	BIU_PIPE USB3OTG PCIE20 PCIE30 SATA XPCS

Voltage Domain	Power Domain	Description
	ALIVE	BIU_SECURE_FLASH CRYPTO,OTPC SYSTEM_SRAM,BOOTROM DCF, STIMER_2CH WDT_S EMMC NANDC SFC
		BIU_GIC_AUDIO GIC600 SPINLOCK I2S0~3 SPDIF PDM audioPWM ACDC_DIG
		BIU_PHP GMAC0 SDMMC0~1
		BIU_USB GMAC1 SDMMC2 USBHOST0~1
		BIU_BUS MCU DMAC GRF, SGRF I2C1/2/3/4/5 TIMER_6CH WDT GPIO1/2/3/4 SPI1/2/3 UART1~9 PWM1/2/3 CAN0~2 TSADC,SARADC
		DDRPHY
		DSIPHY, CSIPHY, HDMIPHY
		USB_SATA_PCIE20_COMBO_PHY
		PCIE30PHY
		SARADC PHY, TSADC_PHY
		OTPPHY
		APLL, CPLL, DPLL, GPLL, MPLL,NPLL,VPLL
		BIU_TOP
		CRU

7.3.2 Operation Mode

First of all, we define two operation modes of PMU, normal mode and low power mode.
When operating at normal mode, that means software can manage power sources directly by accessing PMU registers. For example, CPU can write PMU_PWR_GATE_CON register to determine that power off/on which power domain independently.
When operating at low power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power

resources, but these setting will not be executed immediately after configuration. They will be delayed to execute after FSM running in particular phase.
To enter low power mode, after setting some power configurations, the PMU_PWR_CON[0] bit must be set 1 to enable PMU FSM. Then CPU needs to execute a WFI command to perform ready signal. After PMU detects all CPUs in WFI status, the FSM will be fetched. And the specific power sources will be controlled during specific status in FSM. So the low power mode is a "delay affect" way to handle power sources inside the RK3568 chip.

7.4 Register Description

7.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_VERSION	0x0000	W	0x03003566	Version
PMU_PWR_CON	0x0004	W	0x00000E0C	Main power control
PMU_MAIN_PWR_STATE	0x0008	W	0x00000000	Main power state
PMU_INT_MASK_CON	0x000C	W	0x00000000	Interrrupt mask control
PMU_WAKEUP_INT_CON	0x0010	W	0x00000000	Wakeup interrupt control
PMU_WAKEUP_INT_ST	0x0014	W	0x00000000	Wakeup interrupt state
PMU_WAKEUP_EDGE_CON	0x0018	W	0x00000000	Wakeup edge control
PMU_WAKEUP_EDGE_ST	0x001C	W	0x00000000	Wakeup edge state
PMU_BUS_IDLE_CON0	0x0040	W	0x00000000	Bus idle control register 0
PMU_BUS_IDLE_CON1	0x0044	W	0x00000000	Bus idle control register 1
PMU_BUS_IDLE_SFTCON0	0x0050	W	0x00000000	Bus idle software control register 0
PMU_BUS_IDLE_SFTCON1	0x0054	W	0x00000000	Bus idle software control register 1
PMU_BUS_IDLE_ACK	0x0060	W	0x00000000	Bus idle acknowledge
PMU_BUS_IDLE_ST	0x0068	W	0x00000000	Bus idle state
PMU_NOC_AUTO_CON0	0x0070	W	0x00000000	NOC auto mask control register 0
PMU_NOC_AUTO_CON1	0x0074	W	0x00000000	NOC auto mask control register 1
PMU_DDR_PWR_CON	0x0080	W	0x00000000	DDR power control
PMU_DDR_PWR_SFTCON	0x0084	W	0x00000000	DDR power software control
PMU_DDR_PWR_STATE	0x0088	W	0x00000000	DDR power fsm
PMU_DDR_PWR_ST	0x008C	W	0x00000002	DDR power state
PMU_PWR_GATE_CON	0x0090	W	0x00000000	Power gate control
PMU_PWR_GATE_STATE	0x0094	W	0x00000000	Power gate fsm
PMU_PWR_DWN_ST	0x0098	W	0x00000000	Power down state
PMU_PWR_GATE_SFTCON	0x00A0	W	0x00000000	Power gate software control
PMU_VOL_GATE_SFTCON	0x00A8	W	0x00000003	Voltage domain gate control
PMU_CRU_PWR_CON	0x00B0	W	0x00000000	CRU power control
PMU_CRU_PWR_SFTCON	0x00B4	W	0x00000000	CRU power software control
PMU_CRU_PWR_STATE	0x00B8	W	0x00000000	CRU power fsm
PMU_PLLPD_CON	0x00C0	W	0x00000000	PLL power down control
PMU_PLLPD_SFTCON	0x00C4	W	0x00000000	PLL power down software control
PMU_INFO_TX_CON	0x00D0	W	0x00000000	Debug control
PMU_DSU_STABLE_CNT	0x0100	W	0x000FFFFF	DSU stable counter
PMU_PMIC_STABLE_CNT	0x0104	W	0x000FFFFF	PMIC stable counter
PMU_OSC_STABLE_CNT	0x0108	W	0x000FFFFF	OSC stable counter
PMU_WAKEUP_RSTCLR_CNT	0x010C	W	0x000FFFFF	Wakeup stable counter
PMU_PLL_LOCK_CNT	0x0110	W	0x000FFFFF	PLL lock counter
PMU_DSU_PWRUP_CNT	0x0118	W	0x00005DC0	DSU powerup stable counter
PMU_DSU_PWRDN_CNT	0x011C	W	0x00005DC0	DSU power down stable counter

Name	Offset	Size	Reset Value	Description
PMU_GPU_VOLUP_CNT	0x0120	W	0x0000001F	GPU powerup stable counter
PMU_GPU_VOLDN_CNT	0x0124	W	0x0000001F	GPU power down stable counter
PMU_WAKEUP_TIMEOUT_CNT	0x0128	W	0x00005DC0	Wakeup timeout counter
PMU_PWM_SWITCH_CNT	0x012C	W	0x000FFFFF	PWM switch counter
PMU_DBG_RST_CNT	0x0130	W	0x000FFFFF	Debug reset counter
PMU_SYS_REG0	0x0180	W	0x00000000	System register 0
PMU_SYS_REG1	0x0184	W	0x00000000	System register 1
PMU_SYS_REG2	0x0188	W	0x00000000	System register 2
PMU_SYS_REG3	0x018C	W	0x00000000	System register 3
PMU_SYS_REG4	0x0190	W	0x00000000	System register 4
PMU_SYS_REG5	0x0194	W	0x00000000	System register 5
PMU_SYS_REG6	0x0198	W	0x00000000	System register 6
PMU_SYS_REG7	0x019C	W	0x00000000	System register 7
PMU_DSU_PWR_CON	0x0300	W	0x00000000	DSU power control
PMU_DSU_PWR_SFTCON	0x0304	W	0x00000000	DSU power software control
PMU_DSU_AUTO_CON	0x0308	W	0x00000000	DSU auto power control
PMU_DSU_PWR_STATE	0x030C	W	0x00000000	DSU power fsm
PMU_CPU_AUTO_PWR_CON0	0x0310	W	0x00000000	CPU auto power control register 0
PMU_CPU_AUTO_PWR_CON1	0x0314	W	0x00000000	CPU auto power control register 1
PMU_CPU_PWR_SFTCON	0x0318	W	0x00000000	CPU power software control
PMU_CLUSTER_PWR_ST	0x031C	W	0x00000000	Cluster power state
PMU_CLUSTER_IDLE_CON	0x0320	W	0x00000000	Cluster idle control
PMU_CLUSTER_IDLE_SFTCON	0x0324	W	0x00000000	Cluster idle software control
PMU_CLUSTER_IDLE_ACK	0x0328	W	0x00000000	Cluster idle acknowledge
PMU_CLUSTER_IDLE_ST	0x032C	W	0x00000000	Cluster idle state
PMU_DBG_PWR_CON	0x0330	W	0x00000000	CPU Debug wakeup control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

7.4.2 Detail Registers Description

PMU_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x03003566	version PMU version number

PMU_PWR_CON

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pmu_sleep_pol pmu_sleep polarity selection. 1'b0: High active 1'b1: Low active
14:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0xe	cpu_bypass Bypass CPU in low power procedure. Each bit represents a cpu core. 1'b0: Disable 1'b1: Enable
7	RW	0x0	cru_bypass Bypass CRU in low power procedure. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwrdn_bypass Bypass power domain in low power procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr_bypass Bypass DDR in low power procedure. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bus_bypass Bypass bus idle in low power procedure. 1'b0: Disable 1'b1: Enable
3:2	RO	0x3	reserved
1	RW	0x0	dsu_bypass Bypass DSU in low power procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode_en Low power mode enable. When controller enters low power flow, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU_MAIN_PWR_STATE

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	pmu_power_state PMU main power state. 4'h0: Normal state 4'h1: DSU low power state 4'h3: Bus low power state 4'h4: DDR low power state 4'h5: Power gating low power state 4'h6: Clock and reset low power state 4'h7: sleep state 4'h8: Clock and reset active state 4'h9: Power gating active state 4'ha: DDR active state 4'hb: Bus active state 4'hd: DSU active state 4'de: CORE active state Others: Reserved

PMU_INT_MASK_CON

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	wakeup_mcu_sft Write 1 to this bit to wakeup pmu when WAKEUP_INT_CON[15] is set
14:1	RO	0x0000	reserved
0	RW	0x0	glb_int_disable Global interrupt disable. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_CON

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	wakeup_mcu_sft_en Enable mcusft source as wakeup source. 1'b0: Disable 1'b1: Enable
14	RW	0x0	wakeup_timeout_en Enable PMU timeout interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
13	RW	0x0	wakeup_pwm0_en Enable PWM0 detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wakeup_timer_en Enable TIMER detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
11	RW	0x0	wakeup_vad_en Enable VAD detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
10	RW	0x0	wakeup_pcie_en Enable PCIE detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
9	RW	0x0	wakeup_usb_en Enable USB detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
8	RW	0x0	wakeup_sdmmc2_en Enable SDMMC2 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
7	RW	0x0	wakeup_sdmmc1_en Enable SDMMC1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
6	RW	0x0	wakeup_sdmmc0_en Enable SDMMC0 detect interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
5	RW	0x0	wakeup_uart0_en Enable UART0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wakeup_gpio0_int_en Enable GPIO0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wakeup_cpu3_int_en Enable CPU3 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_cpu2_int_en Enable CPU2 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wakeup_cpu1_int_en Enable CPU1 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wakeup_cpu0_int_en Enable CPU0 interrupt as wakeup source. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_INT_ST

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	wakeup_sys_int_st MCU sft as wakeup source status. 1'b0: Inactive 1'b1: Active
14	RO	0x0	wakeup_timeout_int_st PMU timeout interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
13	RO	0x0	wakeup_pwm0_int_st PWM0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	wakeup_timer_int_st TIMER interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
11	RO	0x0	wakeup_vad_int_st VAD interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

Bit	Attr	Reset Value	Description
10	RO	0x0	wakeup_pcie_int_st PCIE interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
9	RO	0x0	wakeup_usb_int_st USB detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	wakeup_sdmmc2_int_st SDMMC2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	wakeup_sdmmc1_int_st SDMMC1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	wakeup_sdmmc0_int_st SDMMC0 detect interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	wakeup_uart0_int_st UART0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	wakeup_gpio0_int_st GPIO0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	wakeup_cpu3_int_st CPU3 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	wakeup_cpu2_int_st CPU2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	wakeup_cpu1_int_st CPU1 interrupt wakeup status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	wakeup_cpu0_int_st CPU0 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active

PMU_WAKEUP_EDGE_CON

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	edge_wakeup_en Enable both posedge and negedge of GPIO0 pins as wakeup source. Each pin has independent control bit. 1'b0: Disable 1'b1: Enable

PMU_WAKEUP_EDGE_ST

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	edge_status Edge interrupt wakeup status. Each pin has independent control bit. 1'b0: Inactive 1'b1: Active

PMU_BUS_IDLE_CON0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	idle_req_bus Enable sending bus idle request to BIU_BUS by hardware. 1'b0: Disable 1'b1: Enable
14	RW	0x0	idle_req_usb Enable sending bus idle request to BIU_USB by hardware. 1'b0: Disable 1'b1: Enable
13	RW	0x0	idle_req_perimid Enable sending bus idle request to BIU_PERIMID by hardware. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_secure_flash Enable sending bus idle request to BIU_SECURE_FLASH by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_pipe Enable sending bus idle request to BIU_PIPE by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_php Enable sending bus idle request to BIU_PHP by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_gic_audio Enable sending bus idle request to BIU_GIC_AUDIO by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_rkvdec Enable sending bus idle request to BIU_RKVDEC by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_rkvenc Enable sending bus idle request to BIU_RKVENC by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vpu Enable sending bus idle request to BIU_VPU by hardware. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	idle_req_rga Enable sending bus idle request to BIU_RGA by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vo Enable sending bus idle request to BIU_VO by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vi Enable sending bus idle request to BIU_VI by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_npu Enable sending idle request to BIU_NPU by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_gpu Enable sending bus idle request to BIU_GPU by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_msch Enable sending bus idle request to BIU_MSCH by hardware. 1'b0: Disable 1'b1: Enable

PMU_BUS_IDLE_CON1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	idle_req_pmu Enable sending bus idle request to BIU_PMU by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_top2 Enable sending bus idle request to BIU_TOP2 by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_top1 Enable sending bus idle request to BIU_TOP1 by hardware. 1'b0: Disable 1'b1: Enable

PMU_BUS_IDLE_SFTCON0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	idle_req_bus Enable sending bus idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable
14	RW	0x0	idle_req_usb Enable sending bus idle request to BIU_USB by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	idle_req_perimid Enable sending bus idle request to BIU_PERIMID by software. 1'b0: Disable 1'b1: Enable
12	RW	0x0	idle_req_secure_flash Enable sending bus idle request to BIU_SECURE_FLASH by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_pipe Enable sending bus idle request to BIU_PIPE by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_php Enable sending bus idle request to BIU_PHP by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_gic_audio Enable sending bus idle request to BIU_GIC_AUDIO by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_rkvdec Enable sending bus idle request to BIU_RKVDEC by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_rkvenc Enable sending bus idle request to BIU_RKVENC by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vpu Enable sending bus idle request to BIU_VPU by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_rga Enable sending bus idle request to BIU_RGA by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vo Enable sending bus idle request to BIU_VO by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vi Enable sending bus idle request to BIU_VI by software. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	idle_req_npu Enable sending idle request to BIU_NPU by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_gpu Enable sending bus idle request to BIU_GPU by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_msch Enable sending bus idle request to BIU_MSCH by software. 1'b0: Disable 1'b1: Enable

PMU_BUS_IDLE_SFTCON1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	idle_req_pmu Enable sending bus idle request to BIU_PMU by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_top2 Enable sending bus idle request to BIU_TOP2 by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_top1 Enable sending bus idle request to BIU_TOP1 by software. 1'b0: Disable 1'b1: Enable

PMU_BUS_IDLE_ACK

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	idle_ack_pmu BIU_PMU bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
17	RO	0x0	idle_ack_top2 BIU_TOP2 bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
16	RO	0x0	idle_ack_top1 BIU_TOP1 bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
15	RO	0x0	idle_ack_bus BIU_BUS bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

Bit	Attr	Reset Value	Description
14	RO	0x0	idle_ack_usb BIU_USB bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
13	RO	0x0	idle_ack_perimid BIU_PERIMID bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
12	RO	0x0	idle_ack_secure_flash BIU_SECURE_FLASH bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
11	RO	0x0	idle_ack_pipe BIU_PIPE bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
10	RO	0x0	idle_ack_php BIU_PHP bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
9	RO	0x0	idle_ack_gic_audio BIU_GIC_AUDIO bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
8	RO	0x0	idle_ack_rkvdec BIU_RKVDEC bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
7	RO	0x0	idle_ack_rkvenc BIU_RKVENC bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
6	RO	0x0	idle_ack_vpu BIU_VPU bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
5	RO	0x0	idle_ack_rga BIU_RGA bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
4	RO	0x0	idle_ack_vo BIU_VO bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
3	RO	0x0	idle_ack_vi BIU_VI bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
2	RO	0x0	idle_ack_npu BIU_NPU bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

Bit	Attr	Reset Value	Description
1	RO	0x0	idle_ack_gpu BIU_GPU bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_ack_msch BIU_MSCH bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU_BUS_IDLE_ST

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	idle_pmu BIU_PMU idle state. 1'b0: Not idle 1'b1: Idle
17	RO	0x0	idle_top2 BIU_TOP2 idle state. 1'b0: Not idle 1'b1: Idle
16	RO	0x0	idle_top1 BIU_TOP1 idle state. 1'b0: Not idle 1'b1: Idle
15	RO	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle
14	RO	0x0	idle_usb BIU_USB idle state. 1'b0: Not idle 1'b1: Idle
13	RO	0x0	idle_perimid BIU_PERIMID idle state. 1'b0: Not idle 1'b1: Idle
12	RO	0x0	idle_secure_flash BIU_SECURE_FLASH idle state. 1'b0: Not idle 1'b1: Idle
11	RO	0x0	idle_pipe BIU_PIPE idle state. 1'b0: Not idle 1'b1: Idle
10	RO	0x0	idle_php BIU_PHP idle state. 1'b0: Not idle 1'b1: Idle
9	RO	0x0	idle_gic_audio BIU_GIC_AUDIO idle state. 1'b0: Not idle 1'b1: Idle

Bit	Attr	Reset Value	Description
8	RO	0x0	idle_rkvdec BIU_RKVDEC idle state. 1'b0: Not idle 1'b1: Idle
7	RO	0x0	idle_rkvenc BIU_RKVENC idle state. 1'b0: Not idle 1'b1: Idle
6	RO	0x0	idle_vpu BIU_VPU idle state. 1'b0: Not idle 1'b1: Idle
5	RO	0x0	idle_rga BIU_RGA idle state. 1'b0: Not idle 1'b1: Idle
4	RO	0x0	idle_vo BIU_VO idle state. 1'b0: Not idle 1'b1: Idle
3	RO	0x0	idle_vi BIU_VI idle state. 1'b0: Not idle 1'b1: Idle
2	RO	0x0	idle_npu BIU_NPU idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_gpu BIU_GPU idle state. 1'b0: Not idle 1'b1: Idle
0	RO	0x0	idle_msch BIU_MSCH idle state. 1'b0: Not idle 1'b1: Idle

PMU_NOC_AUTO_CON0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	auto_idle_bus When perform idle operation, BIU_BUS corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
14	RW	0x0	auto_idle_usb When perform idle operation, BIU_USB corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
13	RW	0x0	auto_idle_perimid When perform idle operation, BIU_PERIMID corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
12	RW	0x0	auto_idle_secure_flash When perform idle operation, BIU_SECURE_FLASH corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
11	RW	0x0	auto_idle_pipe When perform idle operation, BIU_PIPE corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
10	RW	0x0	auto_idle_php When perform idle operation, BIU_PHP corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
9	RW	0x0	auto_idle_gic_audio When perform idle operation, BIU_GIC_AUDIO corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
8	RW	0x0	auto_idle_rkvdec When perform idle operation, BIU_RKVDEC corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
7	RW	0x0	auto_idle_rkvenc When perform idle operation, BIU_RKVENC corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
6	RW	0x0	auto_idle_vpu When perform idle operation, BIU_VPU corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
5	RW	0x0	auto_idle_rga When perform idle operation, BIU_RGA corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
4	RW	0x0	auto_idle_vo When perform idle operation, BIU_VO corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
3	RW	0x0	auto_idle_vi When perform idle operation, BIU_VI corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	auto_idle_npu When perform idle operation, BIU_NPU corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
1	RW	0x0	auto_idle_gpu When perform idle operation, BIU_GPU corresponding clock can be opened or gated automatically. 3'b111: Enable Others: Disable
0	RW	0x0	auto_idle_msch When perform idle operation, BIU_MSCH corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable

PMU_NOC_AUTO_CON1

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	auto_idle_cpu When perform idle operation, BIU_CPU corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
2	RW	0x0	auto_idle_pmu When perform idle operation, BIU_PMU corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
1	RW	0x0	auto_idle_top2 When perform idle operation, BIU_TOP2 corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
0	RW	0x0	auto_idle_top1 When perform idle operation, BIU_TOP1 corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_CON

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	ddrphy_auto_gating_ena Enable DDR phy auto clock gating function performed by PMU, when DDR enter self-refresh state. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	ddrio_ret_ ena Enable DDR IO retention asserted performed by PMU. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_ena Enable DDR self-refresh by PMU. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_SFTCON

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	ddrctl_active_wait DDR controller waits for c_active high after c_sysack high. 1'b0: Disable 1'b1: Enable
2	RW	0x0	sw_ddrio_ret_exit DDR IO retention exit request by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	sw_ddrio_ret_req DDR IO retention enter request by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	sw_ddr_sref_req DDR self-refresh request by software. 1'b0: Disable 1'b1: Enable

PMU_DDR_PWR_STATE

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	ddr_power_state DDR power state. 3'h0: Normal state 3'h1: Self-refresh enter state 3'h2: IO retention state 3'h3: Sleep state 3'h4: IO retention exit state 3'h5: Self-refresh exit state Others: Reserved

PMU_DDR_PWR_ST

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	ddrio_ret DDR IO retention state. 1'b0: Inactive 1'b1: Active
1	RO	0x1	ddrctl_c_active ddrctlc_active state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddrctl_c_sysack ddrctlc_sysack state. 1'b0: Inactive 1'b1: Active

PMU_PWR_GATE_CON

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pd_center_dwn_ena Enable power down PD_CENTER by PMU automatically. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_pipe_dwn_ena Enable power down PD_PIPE by PMU automatically. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_vo_dwn_ena Enable power down PD_VO by PMU automatically. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_vi_dwn_ena Enable power down PD_VI by PMU automatically. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_rga_dwn_ena Enable power down PD_RGA by PMU automatically. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_rkvdec_dwn_ena Enable power down PD_RKVDEC by PMU automatically. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_rkvenc_dwn_ena Enable power down PD_RKVENC by PMU automatically. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vpu_dwn_ena Enable power down PD_VPU by PMU automatically. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	pd_npu_dwn_ena Enable power down PD_NPU by PMU automatically. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_gpu_dwn_ena Enable power down PD_GPU by PMU automatically. 1'b0: Disable 1'b1: Enable

PMU_PWR_GATE_STATE

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	power_gate_state Power domain state machine status. 3'h0: Normal state 3'h1: Power down start 3'h2: Power down selected domain 3'h3: Wait state 3'h4: Power up start 3'h5: Power up running selected domain Others: Reserved

PMU_PWR_DWN_ST

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	pd_center_dwn_stat The power status of PD_CENTER. 1'b0: Power up 1'b1: Power down
8	RO	0x0	pd_pipe_dwn_stat The power status of PD_PIPE. 1'b0: Power up 1'b1: Power down
7	RO	0x0	pd_vo_dwn_stat The power status of PD_VO. 1'b0: Power up 1'b1: Power down
6	RO	0x0	pd_vi_dwn_stat The power status of PD_VI. 1'b0: Power up 1'b1: Power down
5	RO	0x0	pd_rga_dwn_stat The power status of PD_RGA. 1'b0: Power up 1'b1: Power down
4	RO	0x0	pd_rkvdec_dwn_stat The power status of PD_RKVDEC. 1'b0: Power up 1'b1: Power down
3	RO	0x0	pd_rkvenc_dwn_stat The power status of PD_RKVENC. 1'b0: Power up 1'b1: Power down

Bit	Attr	Reset Value	Description
2	RO	0x0	pd_vpu_dwn_stat The power status of PD_VPU. 1'b0: Power up 1'b1: Power down
1	RO	0x0	pd_npu_dwn_stat The power status of PD_NPU. 1'b0: Power up 1'b1: Power down
0	RO	0x0	pd_gpu_dwn_stat The power status of PD_GPU. 1'b0: Power up 1'b1: Power down

PMU_PWR_GATE_SFTCON

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pd_center_dwn_ena Enable power down PD_CENTER by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_pipe_dwn_ena Enable power down PD_PIPE by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_vo_dwn_ena Enable power down PD_VO by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_vi_dwn_ena Enable power down PD_VI by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_rga_dwn_ena Enable power down PD_RGA by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_rkvdec_dwn_ena Enable power down PD_RKVDEC by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_rkvenc_dwn_ena Enable power down PD_RKVENC by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vpu_dwn_ena Enable power down PD_VPU by software. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
1	RW	0x0	pd_npu_dwn_ena Enable power down PD_NPU by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_gpu_dwn_ena Enable power down PD_GPU by software. 1'b0: Disable 1'b1: Enable

PMU_VOL_GATE_SFTCON

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	vd_npu_ena Enable PD_NPU as a voltage domain. 1'b0: Disable 1'b1: Enable
0	RW	0x1	vd_gpu_ena Enable PD_GPU as a voltage domain. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_CON

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	pmumem_clk_src_gate_ena Gating PMUMEM's bus clock source. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pd_pmu_clk_src_gate_ena Gating PD_PMU's bus clock source, waked up by special GPIOs. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_peri_clk_src_gate_ena Gating BIU_PERI's bus clock source. 1'b0: Disable 1'b1: Enable
9	RW	0x0	pd_bus_clk_src_gate_ena Gating BIU_BUS's bus clock source. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pwm_switch_iout PWM output value when pmu_cru_pwr_con[7]=0 1'b0: output low 1'b1: output high

Bit	Attr	Reset Value	Description
7	RW	0x0	pwm_gpio_ioe_ena PWM output enable. 1'b0: output mode 1'b1: input mode
6	RW	0x0	pwm_switch_ena PWM switch. 1'b0: Disable 1'b1: Enable
5	RW	0x0	power_off_ena Chip power off enable by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_ena pclk_pmu switch oscillator enable. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_ena VD_PMU input clamp enable by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Wakeup reset enable. If asserted, the whole chip except IPs supporting reset hold function will be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Disable oscillator by hardware. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_ena Enable pclk_pmu and clk_pmu switch to 32KHz clock by hardware. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_SFTCON

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	power_off_ena Power off chip by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_ena pclk_pmu switch oscillator enable by software. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	input_clamp_ena VD_PMU input clamp enable by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Wakeup reset enable by software. Reset the whole chip, except IPs supporting reset hold function. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Disable oscillator by software. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_ena Enable pclk_pmu and clk_pmu switch to 32KHz clock by software. 1'b0: Disable 1'b1: Enable

PMU_CRU_PWR_STATE

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	cru_power_state CRU power machine state. 4'h0: Normal state 4'h1: Clock low frequency state 4'h2: PLL power down state 4'h3: Input clamp state 4'h4: Oscillator disable state 4'h5: CRU sleep state 4'h6: CRU wakeup state 4'h7: Oscillator enable state 4'h8: Input clamp release state 4'h9: Clock high frequency state 4'ha: Wakeup reset clear state 4'hb: GPIO switch state 4'hc: PLL power up state 4'hd: PWM switch state Others: Reserved

PMU_PLLPD_CON

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	vpll_pd_ena VPLL power down by PMU. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
7	RW	0x0	ppll_pd_ena PPLL power down by PMU. 1'b0: Disable 1'b1: Enable
6	RW	0x0	hpll_pd_ena HPLL power down by PMU. 1'b0: Disable 1'b1: Enable
5	RW	0x0	npll_pd_ena NPLL power down by PMU. 1'b0: Disable 1'b1: Enable
4	RW	0x0	mpll_pd_ena MPLL power down by PMU. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpll_pd_ena GPLL power down by PMU. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_ena CPLL power down by PMU. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_ena DPLL power down by PMU. 1'b0: Disable 1'b1: Enable
0	RW	0x0	apll_pd_ena APLL power down by PMU. 1'b0: Disable 1'b1: Enable

PMU_PLLPD_SFTCON

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	vpll_pd_ena VPLL power down by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	ppll_pd_ena PPLL power down by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	hpll_pd_ena HPLL power down by software. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5	RW	0x0	npll_pd_ena NPLL power down by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	mpll_pd_ena MPLL power down by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpll_pd_ena GPLL power down by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_ena CPLL power down by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_ena DPLL power down by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	apll_pd_ena APLL power down by software. 1'b0: Disable 1'b1: Enable

PMU_INFO_TX_CON

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	info_tx_intv_time The interval time from 1 byte sends over to a new byte sends start. The value is the cycle number counted in clk_pmu
7:4	RW	0x0	info_tx_con Power state output selection. 4'h0: PMU_MAIN_PWR_STATE 4'h1: PMU_DSU_PWR_STATE 4'h4: PMU_DDR_PWR_STATE 4'h5: PMU_PWR_GATE_STATE 4'h6: PMU_CRU_PWR_STATE 4'h8: PMU_CPU0_PWR_STATE 4'h9: PMU_CPU1_PWR_STATE 4'h10: PMU_CPU2_PWR_STATE 4'h11: PMU_CPU3_PWR_STATE Others: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	info_tx_en Debug information transmit enable. 1'b0: Disable 1'b1: Enable

PMU_DSU_STABLE_CNT

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt DSU power stable counter for DSU from power off to wakeup

PMU_PMIC_STABLE_CNT

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt PMIC power stable counter for CRU from power off to wakeup

PMU_OSC_STABLE_CNT

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt OSC stable counter for OSC from power off to wakeup

PMU_WAKEUP_RSTCLR_CNT

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rstclr_cnt Stable counter for CRU wakeup reset clear

PMU_PLL_LOCK_CNT

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pll_lock_cnt Lock counter for PLL from powerup to lock

PMU_DSU_PWRUP_CNT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt DSU power up stable counter, reflect on the falling time of pd_dsu_dwn_ack.

PMU_DSU_PWRDN_CNT

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt DSU power down stable counter, reflect on the rising time of pd_dsu_dwn_ack.

PMU_GPU_VOLUP_CNT

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x0001f	stable_cnt GPU voltage up stable counter, reflect on the falling time of pd_gpu_dwn_ack.

PMU_GPU_VOLDN_CNT

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x0001f	stable_cnt GPU voltage up stable counter, reflect on the rising time of pd_gpu_dwn_ack.

PMU_WAKEUP_TIMEOUT_CNT

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	wakeup_timeout_cnt WAKEUP timeout counter

PMU_PWM_SWITCH_CNT

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x000fffff	stable_cnt PWM switch stable counter

PMU_DBG_RST_CNT

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x000fffff	dbg_rst_cnt CPU reset duration cycle (mesured by clk_pmu) when entering debug recovery

PMU_SYS_REG0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG3

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG4

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG5

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG6

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_SYS_REG7

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg PMU system register

PMU_DSU_PWR_CON

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	cluster_clk_src_gate_ena Cluster clock gate enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsu_ret_ena DSU retention enable. 1'b0: Disable 1'b1: Enable
5:4	RO	0x0	reserved
3	RW	0x0	dsu_pwroff_ena DSU hardware power off enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dsu_pwrdn_ena DSU hardware power down enable. 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

PMU_DSU_PWR_SFTCON

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	cluster_clk_src_gate_cfg Cluster clock gate software enable. 1'b0: Disable 1'b1: Enable
6:5	RO	0x00	reserved
4	R/WSC	0x0	dsu_sft_preq_ret DSU software p-channel reqest for RET enable. 1'b0: Disable 1'b1: Enable
3	R/WSC	0x0	dsu_sft_preq_on DSU software p-channel reqest for ON enable. 1'b0: Disable 1'b1: Enable
2	R/WSC	0x0	dsu_sft_preq_off DSU software p-channel reqest for OFF enable. 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	dsu_pwrdn_ena DSU software power down enable. 1'b0: Disable 1'b1: Enable

PMU_DSU_AUTO_CON

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	dsu_auto_ret_ena DSU auto retention enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	dsu_sft_wakeup_cluster_ena DSU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dsu_int_mask_ena DSU interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dsu_int_wakeup_cluster_ena DSU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	dsu_lp_ena DSU low power enable. 1'b0: Disable 1'b1: Enable

PMU_DSU_PWR_STATE

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RO	0x0	dsu_power_state DSU power state. 3'h0: DSU power on state 3'h1: Cluster transfer idle state 3'h2: DSU power down state 3'h3: DSU OFF state 3'h4: DSU wakeup state 3'h5: DSU power up state 3'h6: Cluster transfer resume state 3'h7: DSU function retention state Others: Reserved
15	RO	0x0	reserved
14:12	RO	0x0	cpu3_power_state CPU3 power state. 3'h0: CPU power on state 3'h1: CPU power off state 3'h2: CPU emulation off state 3'h3: CPU retention state 3'h4: CPU debug recovery state Others: Reserved
11	RO	0x0	reserved
10:8	RO	0x0	cpu2_power_state CPU2 power state. 3'h0: CPU power on state 3'h1: CPU power off state 3'h2: CPU emulation off state 3'h3: CPU retention state 3'h4: CPU debug recovery state Others: Reserved
7	RO	0x0	reserved
6:4	RO	0x0	cpu1_power_state CPU1 power state. 3'h0: CPU power on state 3'h1: CPU power off state 3'h2: CPU emulation off state 3'h3: CPU retention state 3'h4: CPU debug recovery state Others: Reserved
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x0	cpu0_power_state CPU0 power state. 3'h0: CPU power on state 3'h1: CPU power off state 3'h2: CPU emulation off state 3'h3: CPU retention state 3'h4: CPU debug recovery state Others: Reserved

PMU_CPU_AUTO_PWR_CON0

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cpu1_dbg_recov_rstsrc CPU1 reset source when entering debug recovery. 1'b0: corereset 1'b1: coreporeset
14	RW	0x0	cpu1_dbg_recov_ena CPU1 enter debug recovery enable. 1'b0: Disable 1'b1: Enable
13	RW	0x0	cpu1_sft_wakeup_ret_ena CPU1 software wakeup from retention enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	cpu1_auto_ret_ena CPU1 auto retention enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	cpu1_sft_wakeup_pwrdn_ena CPU1 software wakeup from power down enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	cpu1_int_mask_ena CPU1 interrupt mask enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	cpu1_int_wakeup_ena CPU1 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpu1_auto_pwrdn_ena CPU1 auto power down enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	cpu0_dbg_recov_rstsrc CPU0 reset source when entering debug recovery. 1'b0: corereset 1'b1: coreporeset

Bit	Attr	Reset Value	Description
6	RW	0x0	cpu0_dbg_recov_ena CPU0 enter debug recovery enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cpu0_sft_wakeup_ret_ena CPU0 software wakeup from retention enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cpu0_auto_ret_ena CPU0 auto retention enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu0_sft_wakeup_pwrdn_ena CPU0 software wakeup from power down enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu0_int_mask_ena CPU0 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu0_int_wakeup_ena CPU0 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_auto_pwrdn_ena CPU0 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU_AUTO_PWR_CON1

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cpu3_dbg_recov_rstsrc CPU3 reset source when entering debug recovery. 1'b0: corereset 1'b1: coreporeset
14	RW	0x0	cpu3_dbg_recov_ena CPU3 enter debug recovery enable. 1'b0: Disable 1'b1: Enable
13	RW	0x0	cpu3_sft_wakeup_ret_ena CPU3 software wakeup from retention enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	cpu3_auto_ret_ena CPU3 auto retention enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
11	RW	0x0	cpu3_sft_wakeup_pwrdn_ena CPU3 software wakeup from power down enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	cpu3_int_mask_ena CPU3 interrupt mask enable. 1'b0: Disable 1'b1: Enable
9	RW	0x0	cpu3_int_wakeup_ena CPU3 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpu3_auto_pwrdn_ena CPU3 auto power down enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	cpu2_dbg_recov_rstsrc CPU2 reset source when entering debug recovery. 1'b0: corereset 1'b1: coreporeset
6	RW	0x0	cpu2_dbg_recov_ena CPU2 enter debug recovery enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cpu2_sft_wakeup_ret_ena CPU2 software wakeup from retention enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cpu2_auto_ret_ena CPU2 auto retention enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu2_sft_wakeup_pwrdn_ena CPU2 software wakeup from power down enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu2_int_mask_ena CPU2 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu2_int_wakeup_ena CPU2 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu2_auto_pwrdn_ena CPU2 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU_CPU_PWR_SFTCON

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	R/W SC	0x0	cpu3_sft_preq_ret CPU3 software p-channel reqest for RET enable. 1'b0: Disable 1'b1: Enable
14	R/W SC	0x0	cpu3_sft_preq_on CPU3 software p-channel reqest for ON enable. 1'b0: Disable 1'b1: Enable
13	R/W SC	0x0	cpu3_sft_preq_off CPU3 software p-channel reqest for OFF enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	cpu3_sft_pwrdn_ena CPU3 software power down enable. 1'b0: Disable 1'b1: Enable
11	R/W SC	0x0	cpu2_sft_preq_ret CPU2 software p-channel reqest for RET enable. 1'b0: Disable 1'b1: Enable
10	R/W SC	0x0	cpu2_sft_preq_on CPU2 software p-channel reqest for ON enable. 1'b0: Disable 1'b1: Enable
9	R/W SC	0x0	cpu2_sft_preq_off CPU2 software p-channel reqest for OFF enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpu2_sft_pwrdn_ena CPU2 software power down enable. 1'b0: Disable 1'b1: Enable
7	R/W SC	0x0	cpu1_sft_preq_ret CPU1 software p-channel reqest for RET enable. 1'b0: Disable 1'b1: Enable
6	R/W SC	0x0	cpu1_sft_preq_on CPU1 software p-channel reqest for ON enable. 1'b0: Disable 1'b1: Enable
5	R/W SC	0x0	cpu1_sft_preq_off CPU1 software p-channel reqest for OFF enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cpu1_sft_pwrdn_ena CPU1 software power down enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	R/W SC	0x0	cpu0_sft_preq_ret CPU0 software p-channel reqest for RET enable. 1'b0: Disable 1'b1: Enable
2	R/W SC	0x0	cpu0_sft_preq_on CPU0 software p-channel reqest for ON enable. 1'b0: Disable 1'b1: Enable
1	R/W SC	0x0	cpu0_sft_preq_off CPU0 software p-channel reqest for OFF enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_sft_pwrdn_ena CPU0 software power down enable. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER_PWR_ST

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31	RO	0x0	cpu3_bit_on CPU3 pactive[8], indicating CPU should enter POWER ON.
30	RO	0x0	cpu3_bit_funcret CPU3 pactive[7] state, indicating CPU can enter FUNCTION RETENTION
29	RO	0x0	cpu3_bit_fullret CPU3 pactive[5] state, indicating CPU can enter FULL RETENTION
28	RO	0x0	cpu3_bit_emuoff CPU3 pactive[1] state, indicating CPU can enter EMULATION OFF
27	RO	0x0	cpu2_bit_on CPU2 pactive[8], indicating CPU should enter POWER ON.
26	RO	0x0	cpu2_bit_funcret CPU2 pactive[7] state, indicating CPU can enter FUNCTION RETENTION
25	RO	0x0	cpu2_bit_fullret CPU2 pactive[5] state, indicating CPU can enter FULL RETENTION
24	RO	0x0	cpu2_bit_emuoff CPU2 pactive[1] state, indicating CPU can enter EMULATION OFF
23	RO	0x0	cpu1_bit_on CPU1 pactive[8], indicating CPU should enter POWER ON.
22	RO	0x0	cpu1_bit_funcret CPU1 pactive[7] state, indicating CPU can enter FUNCTION RETENTION
21	RO	0x0	cpu1_bit_fullret CPU1 pactive[5] state, indicating CPU can enter FULL RETENTION
20	RO	0x0	cpu1_bit_emuoff CPU1 pactive[1] state, indicating CPU can enter EMULATION OFF
19	RO	0x0	cpu0_bit_on CPU0 pactive[8], indicating CPU should enter POWER ON.
18	RO	0x0	cpu0_bit_funcret CPU0 pactive[7] state, indicating CPU can enter FUNCTION RETENTION
17	RO	0x0	cpu0_bit_fullret CPU0 pactive[5] state, indicating CPU can enter FULL RETENTION

Bit	Attr	Reset Value	Description
16	RO	0x0	cpu0_bit_emuoff CPU0 pactive[1] state, indicating CPU can enter EMULATION OFF
15	RO	0x0	cpu3_preq_acceped PMU p-channel request sent and accepted by CPU3.
14	RO	0x0	cpu2_preq_acceped PMU p-channel request sent and accepted by CPU2.
13	RO	0x0	cpu1_preq_acceped PMU p-channel request sent and accepted by CPU1.
12	RO	0x0	cpu0_preq_acceped PMU p-channel request sent and accepted by CPU0.
11	RO	0x0	clusterpactive_bit_full Cluster pactive[19], indicating cluster L3 ways for full operation.
10	RO	0x0	clusterpactive_bit_on Cluster pactive[8], indicating cluster should enter POWER ON.
9	RO	0x0	clusterpactive_bit_funcret Cluster pactive[7] state, indicating cluster can enter FUNCTION RETENTION
8	RO	0x0	clusterpactive_bit_memret Cluster pactive[2] state, indicating cluster can enter MEMORRY RETENTION
7	RO	0x0	cluster_preq_acceped PMU p-channel request sent and accepted by DSU.
6:5	RO	0x0	reserved
4	RO	0x0	dsu_dwn_state Cluster power down state. 1'b0: Inactive 1'b1: Active
3	RO	0x0	cpu3_dwn_state CPU3 power down state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cpu2_dwn_state CPU2 power down state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cpu1_dwn_state CPU1 power down state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cpu0_dwn_state CPU0 power down state. 1'b0: Inactive 1'b1: Active

PMU_CLUSTER_IDLE_CON

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	gic2core_pwrq_req Enable sending gic2core power q-channel request to CPU by PMU. 1'b0: Disable 1'b1: Enable
2	RW	0x0	core2gic_pwrq_req Enable sending core2gic power q-channel request to CPU by PMU. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dbg_pwrq_req Enable sending debug power q-channel request to CPU by PMU. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by PMU. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER_IDLE_SFTCON

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gic2core_pwrq_req Enable sending gic2core power q-channel request to CPU by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	core2gic_pwrq_req Enable sending core2gic power q-channel request to CPU by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dbg_pwrq_req Enable sending debug power q-channel request to CPU by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by software. 1'b0: Disable 1'b1: Enable

PMU_CLUSTER_IDLE_ACK

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	gic2core_pwrq_accept CPU gic2core q-channel accept state. 1'b0: Not Accepted 1'b1: Accepted

Bit	Attr	Reset Value	Description
2	RO	0x0	core2gic_pwrq_accept CPU core2gic q-channel accept state. 1'b0: Not Accepted 1'b1: Accepted
1	RO	0x0	dbg_pwrq_accept CPU debug q-channel accept state. 1'b0: Not Accepted 1'b1: Accepted
0	RO	0x0	idle_ack_cpu BIU_CPU bus idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU_CLUSTER_IDLE_ST

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	gic2core_pwrq_active CPU gic2core q-channel active state. 1'b0: Low-power Not availablel 1'b1: Low-power availablel
2	RO	0x0	core2gic_pwrq_active CPU core2gic q-channel active state. 1'b0: Low-power Not availablel 1'b1: Low-power availablel
1	RO	0x0	dbg_pwrq_active CPU debug q-channel active state. 1'b0: Low-power Not availablel 1'b1: Low-power availablel
0	RO	0x0	idle_cpu BIU_CPU idle state. 1'b0: Not idle 1'b1: Idle

PMU_DBG_PWR_CON

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	cluster_dbg_pwrup_req_ena cluster debug power up request enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu3_dbg_pwrup_req_ena cpu3 debug power up request enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu2_dbg_pwrup_req_ena cpu2 debug power up request enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu1_dbg_pwrup_req_ena cpu1 debug power up request enable. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	cpu0_dbg_pwrup_req_ena cpu0 debug power up request enable. 1'b0: Disable 1'b1: Enable

7.5 Timing Diagram

7.5.1 Each Domain Power Switch Timing

The following figure showsthe timing for each domain power down and power up.

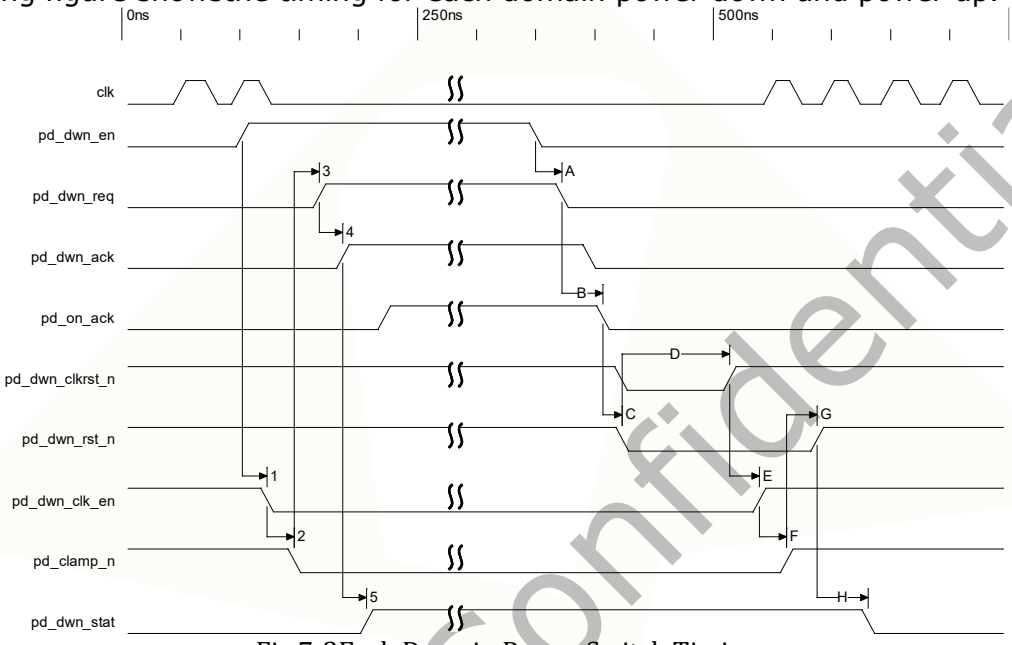


Fig.7-3Each Domain Power Switch Timing

7.5.2 External Wakeup PAD Timing

The PMU supports a lot of external wakeup sources, such as SDMMC, USBDEV, SDIO, GPIO0 wakeup source and so on. All these external wakeup sources must meet the timing requirement (at least 200us) when the wakeup event is asserted. The following figure gives the timing information.

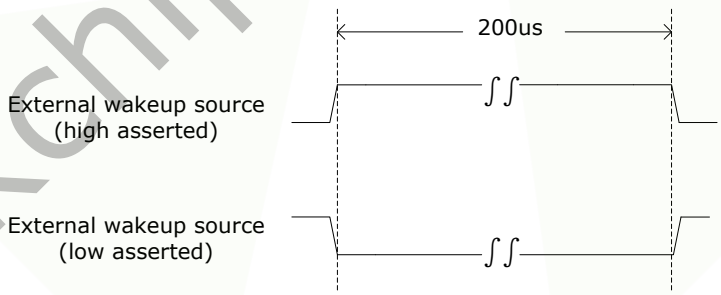


Fig.7-4External Wakeup Source PAD Timing

7.6 Application Notes

7.6.1 Low Power Mode

PMU can work in the Low power mode by setting bit[0] of PMU_PWR_CON register. After setting this bit and all CPUs enter standby states, PMU low power FSM will start to run. In the low power mode, PMU will manage power resources by hardware or software, such as power on/off the specified power domain, send idle request to specified power domain, shut down/up PLL and so on. All of above are configurable by setting corresponding registers.

7.6.2 Debug IO

ALL FSM power states could be monitored through IO. RK3568 provide PMU Debug IO for FSM observation in UARTsignal mode.

Table 7-2 Debug IO for PMU FSM state

Module Pin	Direction	Pin Name	IOMUX Setting
pmu_debug 0	O	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	PMU_GRF_GPIO0A_IOMUX_H [7:4]=4'h4
pmu_debug 1	O	GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	PMU_GRF_GPIO0A_IOMUX_H [11:8]=4'h3
pmu_debug 2	O	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	PMU_GRF_GPIO0C_IOMUX_H [3:0] =4'h4
pmu_debug 3	O	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	PMU_GRF_GPIO0C_IOMUX_H [7:4] =4'h4
pmu_debug _tx	O	HDMITX_CEC_M1/PWM0_M1/UART0_CTSn/GPIO0_C7_d	PMU_GRF_GPIO0C_IOMUX_H [15:12] =4'h4

7.6.3 System Register

PMU support 8 system registers: PMU_SYS_REG0~ PMU_SYS_REG7. These registers are always on no matter what low power mode. So software can use these registers to retain some information which is useful after wakeup from any mode.

7.6.4 Configuration Constraint

In order to shut down the power domains which are managed by software correctly, the software must obey the rules bellow:

- Send BIU request to the BIU in power domain that you want to shut down by configure PMU_BUS_IDLE_SFTCON0 or PMU_BUS_IDLE_SFTCON1 register.
- Querying PMU_ BUS_IDLE_ST register to get the information until the pacific BIU is in idle state.
- Send power request to the power domain through PMU_PWR_GATE_CON register.
- Querying PMU_PWR_DWN_ST register to make sure the pacific power domain is power down.

Chapter 8 MCU

8.1 Overview

The MCU core is load-store architecture, where only load and store instructions access memory and arithmetic instructions only operate on integer registers. The core provides a 32-bit user address space that is byte-addressed and little-endian. And it only implements machine levels, one of four privilege levels.
The key features of the MCU core include:

- Harvard architecture (separate instruction and data buses)
- Machine privilege level
- 32 32-bit general purpose integer registers
- Instruction set is RV32I with M and C extensions
- High-performance or area-optimized multiply/divide unit
- 3 stage pipeline implementation
- 32-bit AHB-Lite external memory interface
- Integrated Programmable Interrupt Controller(IPIC),up to 256 IRQ lines with 256 to 4 INTMUX
- Debug Controller with JTAG interface
- Hardware Break-point Module
- 3 embedded 64bit performance counters
- Real time clock
- Cycle counter
- Instructions-retired counter

8.2 Block Diagram

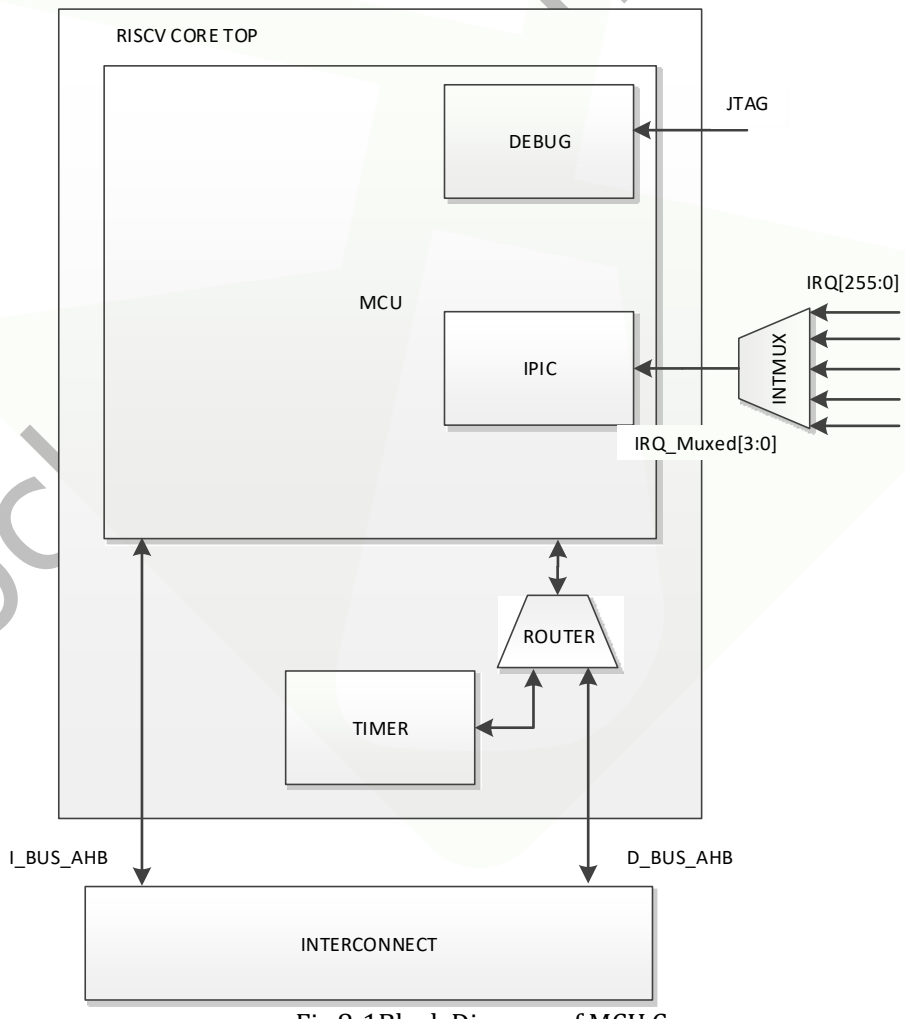


Fig.8-1Block Diagram of MCU Core

8.3 Function Description

8.3.1 Interrupt Multiplexer(INTMUX)

The Interrupt Multiplexer will select 4 interrupts from 256 interrupts using round robin algorithm. You can configure corresponding mask bit for each interrupt. It's a 2-step operation to obtain the interrupt in service. First you should read the INT_FLAG_LEVEL2 to obtain the correct INT_FLAG_GROUP, then read the corresponding INT_FLAG_GROUP to obtain the interrupt in service.

8.3.2 Integrated Programmable Interrupt Controller(IPIC)

MCU core include Integrated Programmable Interrupt Controller (IPIC) with low latency IRQ response. IPIC can be configured using IPIC Control Status Registers.

The term Interrupt Line has the meaning of corresponding IPIC external pin where suitable source of external interrupt may be connected to.

The term Interrupt Vector has the meaning of external interrupt number which will be generated by IPIC in response to external interrupt.

IPIC supports maximum 16 Interrupt vectors [0..15] and 16 Interrupt lines [0..15], each line is statically mapped to the corresponding vector.

Interrupt Vectors are given fixed priorities. The lowest Interrupt Vector number has the highest priority. IPIC supports nested interrupts. Only one interrupt can be serviced at a time. "Void interrupt vector" is defined as a non-existent vector number 0x10. This value is used to indicate absence of a valid interrupt vector.

NOTE: Write access to the IPIC control status registers is implemented only through the use of the CSRRW(I) instructions, the CSRRS(I) and CSRRC(I) instructions are not supported.

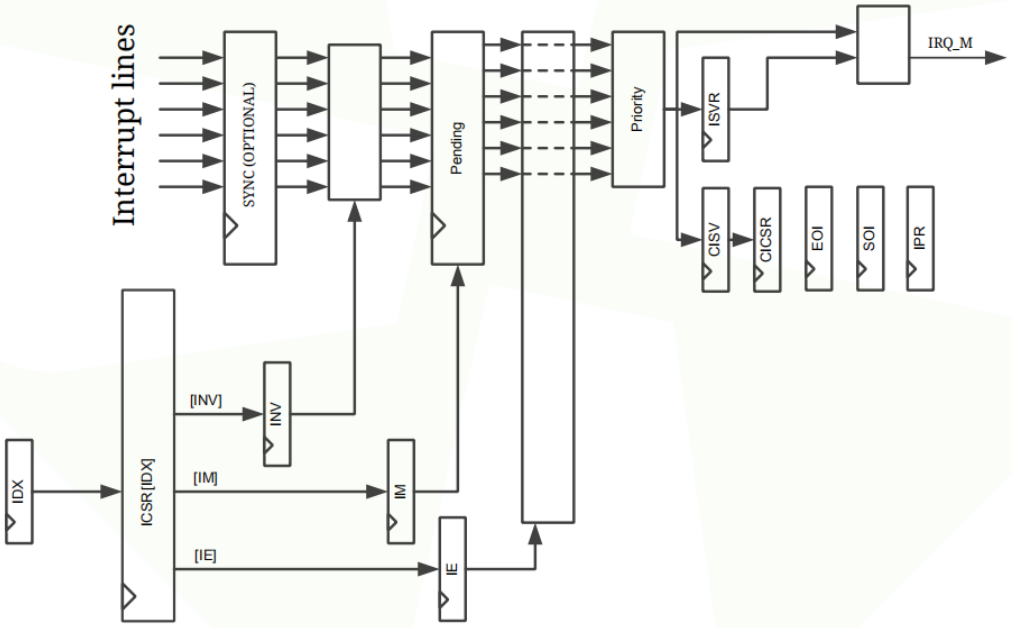


Fig.8-2Block Diagram of IPIC

Depending on the IM (interrupt mode), INV (line inversion) values for each vector, one of four conditions for IP (interrupt pending) bit activation is selected: high level, low level, rising edge, falling edge. Of all vectors with IP and IE (interrupt enable) bits active, the lowest numbered vector has the highest priority. Software is responsible for writing the SOI and EOI registers, thus notifying IPIC of the start and end of interrupt processing, respectively.

8.3.3 Debug

The core's debug sub-system is implemented in compliance with the MCU External Debug Support specification [3]. Its block diagram is shown in Fig.1-3.

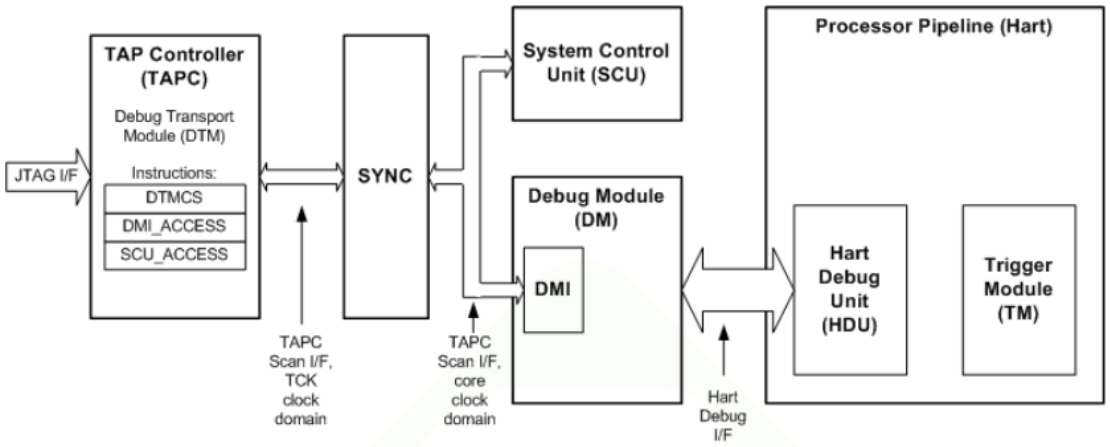


Fig.8-3Block Diagram of Debug Sub-system

An external debugger communicates with the core's debug sub-system via JTAG interface and TAP Controller (TAPC), playing a role of the Debug Transport Module (DTM) in terms of the MCU Debug Specification [3]. The TAPC implements several private TAP instructions allowing debugger to interact with internal debug units:

- DTMCS provides general control over DTM
- DMI_ACCESS provides access to the Debug Module (DM)
- SCU_ACCESS provides access to the System Control Unit (SCU)

Internal connection between TAPC and DM, DM and SCU, is a form of serial scan interface. Source and destination of the TAPC scan interface are in different clock domains: TAPC is fully running in JTAG's TCK clock domain, whereas DM and SCU are in the core clock domain. Therefore, the TAPC scan interface passes through the clock synchronization unit (SYNC).
The System Control Unit (SCU) provides control over implementation-specific reset circuitry, and allows to monitor states of main reset signals.
Using the Debug Module Interface (DMI), the Debug Module (DM) exposes a standard register interface to the core's debug features:

- run control of the core's single hart
- access to its internal registers (GPRs, CSRs)
- access to its memory space
- capability to execute arbitrary instructions from the Program Buffer

The register interface is compliant with the MCU Debug Specification [3].
Implementation of this debug functionality within the hart is distributed betweenseveral units, and from external prospective the most important among them are:

- Hart Debug Unit (HDU) - provides the hart's Debug Interface, connecting the hart with the DM, and contains Debug CSRs
- Trigger Module (TM) - provides a capability of hardware breakpoints, and contains Trigger CSRs

8.4 Register Description

8.4.1 General-purpose Integer Registers

General-purpose Integer Register is the user-visible registers of the core. There are 31 general-purpose registers x1-x31, which are designed to hold integer values. Register x0 is hardwired to the constant 0 and can be used as a source of constant zero or as a don'tcare destination register.
Don't care destination x0 is used to ignore the result of instruction execution provided that destination register is mandatory for instruction structure.
All general-purpose registers in the core are 32-bits wide.
The core implements 32-bit pc register, which is used as program counter, meaning that it holds the address of the current instruction.

8.4.2 Control and Status Register

Control/status registers (CSR) of the core are accessed atomically using instructions specifically designed for CSR access. CSR access instructions are listed in Instruction set summary section of this specification.

According to the MCU specification [2], the core uses 12-bit encoding space to address up to 4096 control/status registers (CSR) in the instructions which atomically read and modify CSRs. The core implements subset of CSRs according to the mapping shown in the next paragraphs. The core follows MCU convention, where the upper 4 bits of the CSR address [11:8] are used to encode the read and write accessibility of the CSRs according to the privilege level. The top two bits [11:10] indicate whether the register is read/write (00, 01, or 10) or read-only (11). The next two bits [9:8] indicate the lowest privilege level that can access the CSR.
The core implements the following rules for CSR access:
1. Attempts to access a non-existent CSR raise an illegal instruction exception.
2. Attempts to write a read-only CSR also raise illegal instruction exception.
3. If a read/write register contains some bits that are read-only, then writes to the read-only bits are ignored.

8.4.3 MCU Registers Summary

Name	Offset	Size	Reset Value	Description
MCU_TIMER_CTRL	0x0000	W	0x00000001	Timer Control Register
MCU_TIMER_DIV	0x0004	W	0x00000000	Timer Divider Register
MCU_MTIME	0x0008	W	0x00000000	Machine Timer Register Low 32bit
MCU_MTIMEH	0x000C	W	0x00000000	Machine Timer Register High 32bit
MCU_MTIMECMP	0x0010	W	0x00000000	Machine Timer Compare Register Low 32bit
MCU_MTIMECMPH	0x0014	W	0x00000000	Machine Timer Compare Register High 32bit
MCU_CSR_MVENDORID	0x0F11	W	0x00000000	Machine Vendor ID Register
MCU_CSR_MARCHID	0x0F12	W	0x00000000	Machine Architecture ID Register
MCU_CSR_MIMPID	0x0F13	W	0x011432A4	Machine Implementation ID Register
MCU_CSR_MHARTID	0x0F14	W	0x00000000	Machine Hart ID Register
MCU_CSR_MSTATUS	0x0300	W	0x00001880	Machine Status Register
MCU_CSR_MISA	0x0301	W	0x40001104	Machine Base ISA Control Register
MCU_CSR_MIE	0x0304	W	0x00000000	Machine Interrupt Enable Register
MCU_CSR_MTVEC	0x0305	W	0x002001C0	Machine Trap-Vector Base-Address Register
MCU_CSR_MSCRATCH	0x0340	W	0x00000000	Machine Scratch Register
MCU_CSR_MEPC	0x0341	W	0x00000000	Machine Exception Program Counter Register
MCU_CSR_MCAUSE	0x0342	W	0x00000000	Machine Cause Register
MCU_CSR_MTVAL	0x0343	W	0x00000000	Machine Trap Value Register
MCU_CSR_MIP	0x0344	W	0x00000000	Machine Interrupt Pending Register
MCU_CSR_MCYCLEL	0x0B00	W	0x00000000	Machine Cycle Counter Low Register
MCU_CSR_MCYCLEH	0x0B80	W	0x00000000	Machine Cycle Counter High Register
MCU_CSR_MINSTRETL	0x0B02	W	0x00000000	Machine Instructions Retired Low Register

Name	Offset	Size	Reset Value	Description
MCU_CSR_MINSTRETH	0x0B82	W	0x00000000	Machine Instructions Retired High Register
MCU_CSR_MCOUNTEN	0x07E0	W	0x00000005	Machine Counter Enable Register
MCU_CSR_DBG_SCRATCH	0x07C8	W	0x00000000	Debug Scratch Register
MCU_CSR_IPIC_CISV	0x0BF0	W	0x00000000	Current Interrupt Vector in Service
MCU_CSR_IPIC_CICSR	0x0BF1	W	0x00000000	Current Interrupt Control Status Register
MCU_CSR_IPIC_IPR	0x0BF2	W	0x00000000	Interrupt Pending Register
MCU_CSR_IPIC_ISVR	0x0BF3	W	0x00000000	Interrupt Serviced Register
MCU_CSR_IPIC_EOI	0x0BF4	W	0x00000000	End Of Interrupt
MCU_CSR_IPIC_SOI	0x0BF5	W	0x00000000	Start Of Interrupt
MCU_CSR_IPIC_IDX	0x0BF6	W	0x00000000	Index Register
MCU_CSR_IPIC_ICSR	0x0BF7	W	0x00000000	Interrupt Control Status register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.4 MCU Detail Registers Description

MCU_TIMER_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	CLKSRC timer clock source 1'b0: internal core clock(default) 1'b1: external real-time clock
0	RW	0x1	ENABLE timer enable bit 1'b0: timer disable 1'b1: timer enable

MCU_TIMER_DIV

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	DIV Timer divider Timer tick occurs every DIV+1 clock ticks

MCU_MTIME

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MTIMEL Low 32bit of wall-clock real time(number of timer ticks)

MCU_MTIMEH

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MTIMEH High 32bit of wall-clock real time(number of timer ticks)

MCU_MTIMECMP

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MTIMECMPL Machine-mode timer compare register low 32bit

MCU_MTIMECMPH

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MTIMECMPH Machine-mode timer compare register high 32bit

MCU_CSR_MVENDORID

Address: Operational Base + offset (0x0F11)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VENDOR ID The JEDEC manufacturer ID of the provider of the core

MCU_CSR_MARCHID

Address: Operational Base + offset (0x0F12)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ARCH ID Encoding the base micro-architecture of the hart

MCU_CSR_MIMPID

Address: Operational Base + offset (0x0F13)

Bit	Attr	Reset Value	Description
31:0	RO	0x011432a4	YEAR-MONTH-DAY-RELEASE Bit[31]-bit[24]: BCD-coded value of the year Bit[23]-bit[16]: BCD-coded value of the month Bit[16]-bit[8]: BCD-coded value of the day Bit[7]-bit[0]: 8-bit value of intraday release number

MCU_CSR_MHARTID

Address: Operational Base + offset (0x0F14)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HART ID Containing the integer ID of the hardware thread running the code.

MCU_CSR_MSTATUS

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:11	RO	0x3	MPP Previous privilege mode (hardwired to 11)
10:8	RO	0x0	reserved
7	RW	0x1	MPIE Previous global interrupt enable
6:4	RO	0x0	reserved
3	RW	0x0	MIE Global interrupt enable
2:0	RO	0x0	reserved

MCU_CSR_MISA

Address: Operational Base + offset (0x0301)

Bit	Attr	Reset Value	Description
31:30	RO	0x1	MXL Machine XLEN (hardwired to 01)
29:24	RO	0x00	reserved
23	RO	0x0	RVX Non-standard extensions
22:13	RO	0x000	reserved
12	RO	0x1	RVM Integer Multiply/Divide extension implemented
11:9	RO	0x0	reserved
8	RO	0x1	RVI RV32I base integer instruction set
7:5	RO	0x0	reserved
4	RO	0x0	RVE RV32E base integer instruction set
3	RO	0x0	reserved
2	RO	0x1	RVC Compressed instruction extension implemented
1:0	RO	0x0	reserved

MCU_CSR_MIE

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	MEIE Machine External Interrupt Enable
10:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	MTIE Machine Timer Interrupt Enable
6:4	RO	0x0	reserved
3	RW	0x0	MSIE Machine Software Interrupt Enable
2:0	RO	0x0	reserved

MCU_CSR_MTVEC

Address: Operational Base + offset (0x0305)

Bit	Attr	Reset Value	Description
31:6	RW	0x0008007	BASE Vector base address (upper 26 bits)
5:2	RO	0x0	reserved
1:0	RW	0x0	MODE Vector mode (0-direct mode, 1-vectored mode)

MCU_CSR_MSCRATCH

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MSCRATCH Hold a pointer to a machine-mode hart-local context space and swapped with a user register upon entry to an M-mode trap handler.

MCU_CSR_MEPC

Address: Operational Base + offset (0x0341)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	MEPC Hold the virtual address of the instruction that encountered the exception.
0	RO	0x0	reserved

MCU_CSR_MCAUSE

Address: Operational Base + offset (0x0342)

Bit	Attr	Reset Value	Description
31	RW	0x0	INT Interrupt
30:4	RO	0x0000000	reserved
3:0	RW	0x0	EC Exception Code

MCU_CSR_MTVAL

Address: Operational Base + offset (0x0343)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	MTVAL When a trap is taken into M-mode, mtval is written with exception-specific information to assist software in handling the trap.

MCU_CSR_MIP

Address: Operational Base + offset (0x0344)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	MEIP Machine External Interrupt Pending
10:8	RO	0x0	reserved
7	RO	0x0	MTIP Machine Timer Interrupt Pending
6:4	RO	0x0	reserved
3	RO	0x0	MSIP Machine Software Interrupt Pending
2:0	RO	0x0	reserved

MCU_CSR_MCYCLEL

Address: Operational Base + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MCYCLEL Represent the number of clock cycles(low 32bit) since some arbitrary point of time in the past.

MCU_CSR_MCYCLEH

Address: Operational Base + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MCYCLEH Represent the number of clock cycles(high 32bit) since some arbitrary point of time in the past.

MCU_CSR_MINSTRETL

Address: Operational Base + offset (0x0B02)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MINSTRETL Represent the number of instructions(low 32bit) retired by the core from some arbitrary time in the past.

MCU_CSR_MINSTRETH

Address: Operational Base + offset (0x0B82)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MINSTRETH Represent the number of instructions(low 32bit) retired by the core from some arbitrary time in the past.

MCU_CSR_MCOUNTEN

Address: Operational Base + offset (0x07E0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x1	IR Enable retired instructions counter
1	RO	0x0	reserved
0	RW	0x1	CY Enable cycle counter

MCU_CSR_DBG_SCRATCH

Address: Operational Base + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DSCRATCH Used to exchange data between the core and the debug controller.

MCU_CSR_IPIC_CISV

Address: Operational Base + offset (0x0BF0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RO	0x00	CISV Number of the interrupt vector currently in service

MCU_CSR_IPIC_CICSR

Address: Operational Base + offset (0x0BF1)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	IE Interrupt Enable Bit 1'b0: Interrupt disabled 1'b1: Interrupt enabled
0	W1C	0x0	IP Interrupt pending 1'b0: no interrupt 1'b1: Interrupt pending

MCU_CSR_IPIC_IPR

Address: Operational Base + offset (0x0BF2)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	PENDING Interrupt vector0 ~ vector15 pending status, each bit represents one vector.

MCU_CSR_IPIC_ISVR

Address: Operational Base + offset (0x0BF3)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	SERVICE When corresponding bit is set (1) - this interrupt vector is in service.

MCU_CSR_IPIC_EOI

Address: Operational Base + offset (0x0BF4)

Bit	Attr	Reset Value	Description
31:0	WS	0x00000000	END OF INTERRUPT Writing any value to EOI register ends the interrupt which is currently in service, read will return zero.

MCU_CSR_IPIC_SOI

Address: Operational Base + offset (0x0BF5)

Bit	Attr	Reset Value	Description
31:0	WS	0x00000000	START OF INTERRUPT Writing any value to SOI activates start of interrupt if one of the following conditions is true: 1. There is at least one pending interrupt with IE and ISR is zero (no interrupts in service) 2. There is at least one pending interrupt with IE and this interrupt has higher priority than the interrupts currently in service.

MCU_CSR_IPIC_IDX

Address: Operational Base + offset (0x0BF6)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	INDEX Interrupt vector index to access through IPIC_ICSR

MCU_CSR_IPIC_ICSR

Address: Operational Base + offset (0x0BF7)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
12	RO	0x0	LN External IRQ Line Number assigned to this interrupt vector. This value is always equal to IPIC_IDX, because of the static line to vector mapping.
11:9	RO	0x0	reserved
8	RO	0x0	PRV Privilege mode: hardwired to 11 (machine mode)
7:5	RO	0x0	reserved
4	RW	0x0	IS In Service
3	RW	0x0	INV Line Inversion 1'b0: no inversion 1'b1: line inversion
2	RW	0x0	IM Interrupt Mode 1'b0: Level interrupt 1'b1: Edge interrupt
1	RW	0x0	IE Interrupt Enable Bit 1'b0: Interrupt disabled 1'b1: Interrupt enabled
0	W1C	0x0	IP Interrupt pending 1'b0: no interrupt 1'b1: Interrupt pending

8.4.5 INTMUX Registers Summary

Name	Offset	Size	Reset Value	Description
INTMUX_INT_MASK_GROUP0	0x0000	W	0x00000000	Interrupt Group0 Enable Register
INTMUX_INT_MASK_GROUP1	0x0004	W	0x00000000	Interrupt Group1 Enable Register
INTMUX_INT_MASK_GROUP2	0x0008	W	0x00000000	Interrupt Group2 Enable Register
INTMUX_INT_MASK_GROUP3	0x000C	W	0x00000000	Interrupt Group3 Enable Register
INTMUX_INT_MASK_GROUP4	0x0010	W	0x00000000	Interrupt Group4 Enable Register
INTMUX_INT_MASK_GROUP5	0x0014	W	0x00000000	Interrupt Group5 Enable Register
INTMUX_INT_MASK_GROUP6	0x0018	W	0x00000000	Interrupt Group6 Enable Register

Name	Offset	Size	Reset Value	Description
INTMUX_INT_MASK_GROUP7	0x001C	W	0x00000000	Interrupt Group7 Enable Register
INTMUX_INT_MASK_GROUP8	0x0020	W	0x00000000	Interrupt Group8 Enable Register
INTMUX_INT_MASK_GROUP9	0x0024	W	0x00000000	Interrupt Group9 Enable Register
INTMUX_INT_MASK_GROUP10	0x0028	W	0x00000000	Interrupt Group10 Enable Register
INTMUX_INT_MASK_GROUP11	0x002C	W	0x00000000	Interrupt Group11 Enable Register
INTMUX_INT_MASK_GROUP12	0x0030	W	0x00000000	Interrupt Group12 Enable Register
INTMUX_INT_MASK_GROUP13	0x0034	W	0x00000000	Interrupt Group13 Enable Register
INTMUX_INT_MASK_GROUP14	0x0038	W	0x00000000	Interrupt Group14 Enable Register
INTMUX_INT_MASK_GROUP15	0x003C	W	0x00000000	Interrupt Group15 Enable Register
INTMUX_INT_MASK_GROUP16	0x0040	W	0x00000000	Interrupt Group16 Enable Register
INTMUX_INT_MASK_GROUP17	0x0044	W	0x00000000	Interrupt Group17 Enable Register
INTMUX_INT_MASK_GROUP18	0x0048	W	0x00000000	Interrupt Group18 Enable Register
INTMUX_INT_MASK_GROUP19	0x004C	W	0x00000000	Interrupt Group19 Enable Register
INTMUX_INT_MASK_GROUP20	0x0050	W	0x00000000	Interrupt Group20 Enable Register
INTMUX_INT_MASK_GROUP21	0x0054	W	0x00000000	Interrupt Group21 Enable Register
INTMUX_INT_MASK_GROUP22	0x0058	W	0x00000000	Interrupt Group22 Enable Register
INTMUX_INT_MASK_GROUP23	0x005C	W	0x00000000	Interrupt Group23 Enable Register
INTMUX_INT_MASK_GROUP24	0x0060	W	0x00000000	Interrupt Group24 Enable Register
INTMUX_INT_MASK_GROUP25	0x0064	W	0x00000000	Interrupt Group25 Enable Register
INTMUX_INT_MASK_GROUP26	0x0068	W	0x00000000	Interrupt Group26 Enable Register
INTMUX_INT_MASK_GROUP27	0x006C	W	0x00000000	Interrupt Group27 Enable Register

Name	Offset	Size	Reset Value	Description
INTMUX_INT_MASK_GROUP28	0x0070	W	0x00000000	Interrupt Group28 Enable Register
INTMUX_INT_MASK_GROUP29	0x0074	W	0x00000000	Interrupt Group29 Enable Register
INTMUX_INT_MASK_GROUP30	0x0078	W	0x00000000	Interrupt Group30 Enable Register
INTMUX_INT_MASK_GROUP31	0x007C	W	0x00000000	Interrupt Group31 Enable Register
INTMUX_INT_FLAG_GROUP0	0x0080	W	0x00000000	Interrupt Group0 Flag Register
INTMUX_INT_FLAG_GROUP1	0x0084	W	0x00000000	Interrupt Group1 Flag Register
INTMUX_INT_FLAG_GROUP2	0x0088	W	0x00000000	Interrupt Group2 Flag Register
INTMUX_INT_FLAG_GROUP3	0x008C	W	0x00000000	Interrupt Group3 Flag Register
INTMUX_INT_FLAG_GROUP4	0x0090	W	0x00000000	Interrupt Group4 Flag Register
INTMUX_INT_FLAG_GROUP5	0x0094	W	0x00000000	Interrupt Group5 Flag Register
INTMUX_INT_FLAG_GROUP6	0x0098	W	0x00000000	Interrupt Group6 Flag Register
INTMUX_INT_FLAG_GROUP7	0x009C	W	0x00000000	Interrupt Group7 Flag Register
INTMUX_INT_FLAG_GROUP8	0x00A0	W	0x00000000	Interrupt Group8 Flag Register
INTMUX_INT_FLAG_GROUP9	0x00A4	W	0x00000000	Interrupt Group9 Flag Register
INTMUX_INT_FLAG_GROUP10	0x00A8	W	0x00000000	Interrupt Group10 Flag Register
INTMUX_INT_FLAG_GROUP11	0x00AC	W	0x00000000	Interrupt Group11 Flag Register
INTMUX_INT_FLAG_GROUP12	0x00B0	W	0x00000000	Interrupt Group12 Flag Register
INTMUX_INT_FLAG_GROUP13	0x00B4	W	0x00000000	Interrupt Group13 Flag Register
INTMUX_INT_FLAG_GROUP14	0x00B8	W	0x00000000	Interrupt Group14 Flag Register
INTMUX_INT_FLAG_GROUP15	0x00BC	W	0x00000000	Interrupt Group15 Flag Register
INTMUX_INT_FLAG_GROUP16	0x00C0	W	0x00000000	Interrupt Group16 Flag Register

Name	Offset	Size	Reset Value	Description
INTMUX_INT_FLAG_GROUP17	0x00C4	W	0x00000000	Interrupt Group17 Flag Register
INTMUX_INT_FLAG_GROUP18	0x00C8	W	0x00000000	Interrupt Group18 Flag Register
INTMUX_INT_FLAG_GROUP20	0x00D0	W	0x00000000	Interrupt Group20 Flag Register
INTMUX_INT_FLAG_GROUP21	0x00D4	W	0x00000000	Interrupt Group21 Flag Register
INTMUX_INT_FLAG_GROUP22	0x00D8	W	0x00000000	Interrupt Group22 Flag Register
INTMUX_INT_FLAG_GROUP23	0x00DC	W	0x00000000	Interrupt Group23 Flag Register
INTMUX_INT_FLAG_GROUP24	0x00E0	W	0x00000000	Interrupt Group24 Flag Register
INTMUX_INT_FLAG_GROUP25	0x00E4	W	0x00000000	Interrupt Group25 Flag Register
INTMUX_INT_FLAG_GROUP26	0x00E8	W	0x00000000	Interrupt Group26 Flag Register
INTMUX_INT_FLAG_GROUP27	0x00EC	W	0x00000000	Interrupt Group27 Flag Register
INTMUX_INT_FLAG_GROUP28	0x00F0	W	0x00000000	Interrupt Group28 Flag Register
INTMUX_INT_FLAG_GROUP29	0x00F4	W	0x00000000	Interrupt Group29 Flag Register
INTMUX_INT_FLAG_GROUP30	0x00F8	W	0x00000000	Interrupt Group30 Flag Register
INTMUX_INT_FLAG_GROUP31	0x00FC	W	0x00000000	Interrupt Group31 Flag Register
INTMUX_INT_FLAG_LEVEL2	0x0100	W	0x00000000	Interrupt Flag LEVEL2Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

8.4.6 INTMUX Detail Registers Description

INTMUX_INT_MASK_GROUP0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP3

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP7

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP11

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP12

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP15

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP16

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP19

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP20

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP21

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP23

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP24

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP25

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP26

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP27

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP28

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP29

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP30

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_MASK_GROUP31

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MASK Each bit represents one interrupt mask bit. 1'b0: Interrupt enabled 1'b1: Interrupt disabled

INTMUX_INT_FLAG_GROUP0

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP2

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP3

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP4

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP5

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP6

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP7

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP8

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP9

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP10

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP11

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP12

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP13

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP14

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP15

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP16

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP17

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP18

Address: Operational Base + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP20

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP21

Address: Operational Base + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP22

Address: Operational Base + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP23

Address: Operational Base + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP24

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP25

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP26

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP27

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP28

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP29

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP30

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_GROUP31

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	FLAG Each bit represents one interrupt is in service. 1'b1: Interrupt in service 1'b0: Interrupt out of service

INTMUX_INT_FLAG_LEVEL2

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	INT_FLAG_32MUX4 Each bit correspoding to a INT_FLAG_GROUP 1'b1: INT_FLAG_GROUP in service 1'b0: INT_FLAG_GROUP out of service

8.5 Interface Description

Table 8-1 Serial Wire Debug Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
TCK	I	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	PMUGRF_GPIO0B_IOMUX_H[3:0]=4'b0100
TMS	I/O	PWM3_IR/EDP_DP_HPDIN_M1/PCIE30X1_WAKEn_M0/MCU_JTAG_TMS/GPIO0_C2_d	PMUGRF_GPIO0C_IOMUX_L[11:8]=4'b0100
TRSTN	I	PWM4/VOP_PWM_M0/PCIE30X1_PERSTn_M0/MCU_JTAG_TRSTn/GPIO0_C3_d	GRF_GPIO0C_IOMUX_L[15:12]=4'b0100
TDO	O	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B3_u	PMUGRF_GPIO0B_IOMUX_L[15:12]=4'b0100
TDI	I	PWM2_M0/NPUAVS/UART0_TX/MCU_JTAG_TDI/GPIO0_C1_d	PMUGRF_GPIO0C_IOMUX_L[7:4]=4'b0100

Notes: Unused Module Pin is tied to zero! I=input, O=output, I/O=input/output, bidirectional

8.6 Application Notes

- How to boot?
  Currently, the MCU core boot address is configurable, its default value is 32'h0000_0000, and the default value of trap vector base address is 32'h0000_01c0, you can configure SCR1_BOOT_ADDR of SGRF before de-assert its reset. if you change the boot address, don't forget to configure the MCU_CSR_MTVEC register by system instructions.
- Are 4 IRQ lines enough?
  Actually, there are 214 IRQ lines in full chip, and all of these IRQ lines are connected to MCU core, there is a 256to4 MUX for these IRQ lines before entering to IPIC of MCU core. Each 8 IRQ lines is regard as one group and connect to one IRQ line of MCU core. Not only We should configure IPIC, but also configure INTMUX before activates IRQ.

Chapter 9 GIC-600

9.1 Overview

The GIC-600 in RK3568 provides registers for managing interrupt sources, interrupt behavior, and interrupt routing to one or more cores.
The configuration of GIC-600 is shown below:

Table 9-1 GIC-600 configuration

Configuration item	Value
num_clusters	1
gic_num_rid_bits	10
num_spis	320
disable_security	false
gic_num_wid_bits	10
lpi_support	true
cpus_per_clsuter_0	4
are_option	false
lpi_ram_depth	128
did_width	16

The GIC-600 in RK3568 supports following feature:

- Support 1 cluster
- Support cluster 0 with 4 CPUs
- The following interrupt types:
  - Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the GIC-600.
  - 320 Shared Peripheral Interrupts (SPIs)
  - 16 Private Peripheral Interrupts (PPIs), that are independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts
  - 16 SGIs, that are generated either by using software to write to GICD_SGIR or through the GIC CPU interface of a core
- Interrupt Translation Service (ITS). This provides device isolation and ID translation for message-based interrupts, which allows virtual machines to program devices directly
- Memory-mapped access to all registers
- Interrupt masking and prioritization
- Programmable interrupt routing that is based on affinity
- Three different interrupt groups, which allow interrupts to target different Exception levels:
  - Group 0
  - Non-secure Group 1
  - Secure Group 1
- A global Disable Security (DS) bit. This allows support for systems with and without security
- 32 priority values, five bits for each interrupt

9.2 Block Diagram

The GIC-600 in the RK3568 is connected with CPU cluster through AXI Stream bus, as shown below:

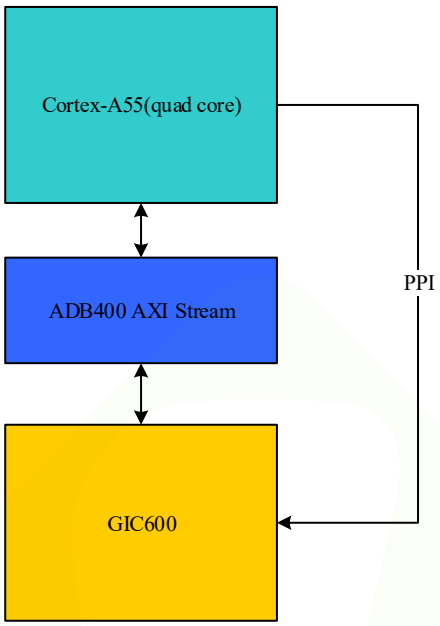


Fig. 9-1 Block Diagram

9.3 Function Description

Please refer to the document ARM_GIC-600_r1p6-00rel0_Technical_Reference_Manual.pdf for the detail function description.

Chapter 10 DMA Controller (DMAC)

10.1 Overview

This device supports 2 Direct Memory Access (DMA) Controller. DMAC0/1 support transfers between memory and memory, peripheral and memory. DMAC0/1 is under Non-secure state after reset, and the Secure state can be changed by configurable SGRF module.
DMAC supports the following features:

- DMAC0 Supports 32 peripheral requests
- DMAC1 Supports 17 peripheral requests
- Up to 64 bits data size
- 8 channel at the same time
- Up to burst 16
- 16 interrupts output and 1 abort output
- Supports 128 MFIFO depth

Following table shows the DMAC request mapping scheme.

Table 10-1 DMAC Request Mapping Table

DMAC0		
Req number	**Source**	**Polarity**
0	UART0_TX	High level
1	UART0_RX	High level
2	UART1_TX	High level
3	UART1_RX	High level
4	UART2_TX	High level
5	UART2_RX	High level
6	UART3_TX	High level
7	UART3_RX	High level
8	UART4_TX	High level
9	UART4_RX	High level
10	UART5_TX	High level
11	UART5_RX	High level
12	UART6_TX	High level
13	UART6_RX	High level
14	UART7_TX	High level
15	UART7_RX	High level
16	UART8_TX	High level
17	UART8_RX	High level
18	UART9_TX	High level
19	UART9_RX	High level
20	SPI0_TX	High level
21	SPI0_RX	High level
22	SPI1_TX	High level
23	SPI1_RX	High level
24	SPI2_TX	High level
25	SPI2_RX	High level
26	SPI3_TX	High level
27	SPI3_RX	High level
28	PWM0_TX	High level
29	PWM1_TX	High level
30	PWM2_TX	High level
31	PWM3_TX	High level
DMAC1		
Req number	**Source**	**Polarity**
0	I2S0_8CH_TX	High level
1	SPDIF	High level

2	I2S1_8CH_TX	High level
3	I2S1_8CH_RX	High level
4	I2S2_2CH_TX	High level
5	I2S2_2CH_RX	High level
6	I2S3_2CH_TX	High level
7	I2S3_2CH_RX	High level
8	AUDPWM	High level
9	PDM	High level
10	SDMMC_BUFFER	High level
11	CAN0_TX	High level
12	CAN0_RX	High level
13	CAN1_TX	High level
14	CAN1_RX	High level
15	CAN2_TX	High level
16	CAN2_RX	High level

DMAC supports incrementing-address burst and fixed-address burst. But in the case of access to SPI and UART at byte or halfword size, DMAC only supports fixed-address burst and the address must be aligned to word.

10.2 Block Diagram

Following figure shows the block diagram of DMAC.

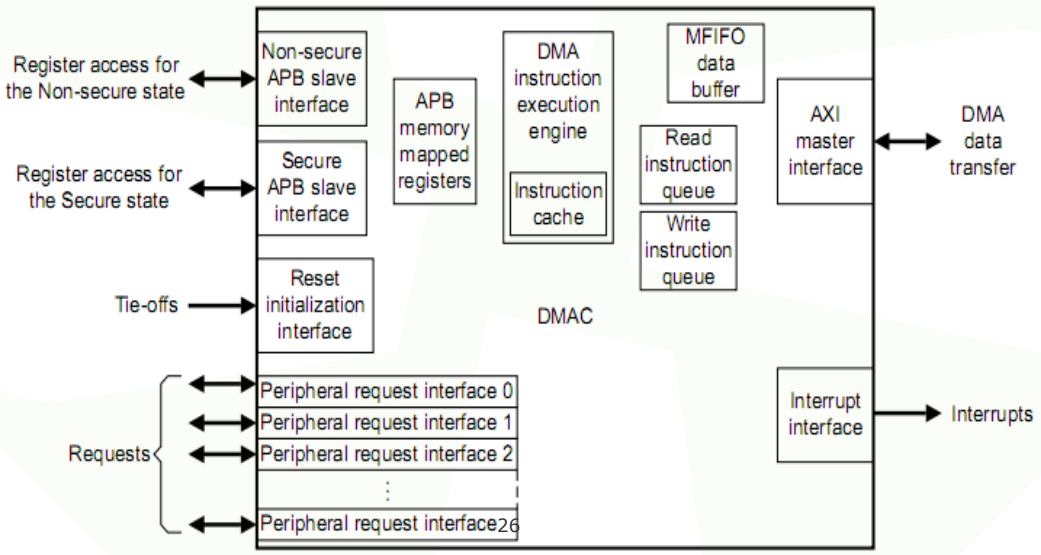


Fig. 10-1 Block Diagram of DMAC

As the DMAC supports TrustZone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the Secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is Non-secure APB interface.

10.3 Function Description

10.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache. It supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin

process when selecting the next active DMA channel thread to execute.
The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.
When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.
When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

10.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

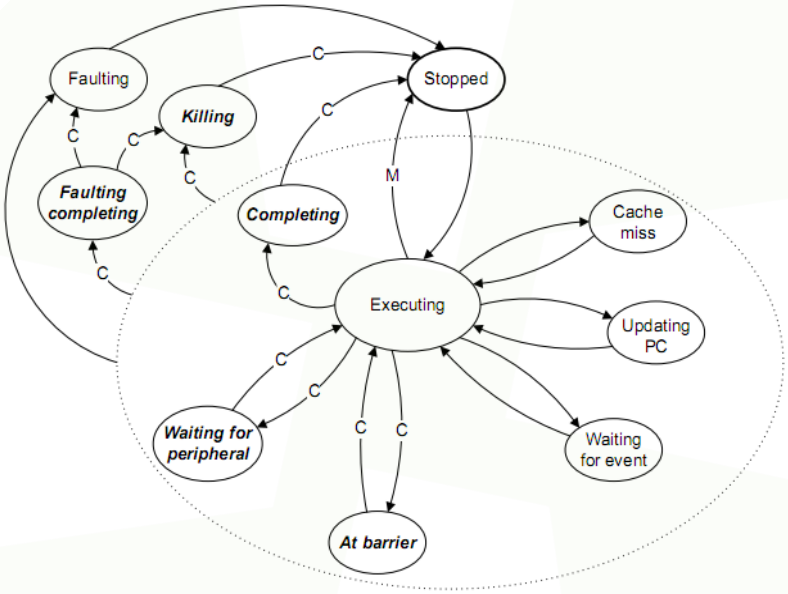


Fig. 10-2 DMAC Operation State

Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and DMA manager thread moves to the Stopped state.

10.4 Register Description

10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

10.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DMAC_DSR	0x0000	W	0x00000000	DMA Manager Status Register
DMAC_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMAC_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMAC_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMAC_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMAC_INTCLR	0x002c	W	0x00000000	Interrupt Clear Register
DMAC_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMAC_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMAC_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMAC_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel 0 Register
DMAC_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel 1 Register
DMAC_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel 2 Register
DMAC_FTR3	0x004c	W	0x00000000	Fault Type DMA Channel 3 Register
DMAC_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel 4 Register
DMAC_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel 5 Register
DMAC_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel 6 Register
DMAC_FTR7	0x005c	W	0x00000000	Fault Type DMA Channel 7 Register
DMAC_CSR0	0x0100	W	0x00000000	Channel 0 Status Register
DMAC_CPC0	0x0104	W	0x00000000	Channel 0 Program Counter Register
DMAC_CSR1	0x0108	W	0x00000000	Channel 1 Status Register
DMAC_CPC1	0x010c	W	0x00000000	Channel 1 Program Counter Register
DMAC_CSR2	0x0110	W	0x00000000	Channel 2 Status Register
DMAC_CPC2	0x0114	W	0x00000000	Channel 2 Program Counter Register
DMAC_CSR3	0x0118	W	0x00000000	Channel 3 Status Register
DMAC_CPC3	0x011c	W	0x00000000	Channel 3 Program Counter Register
DMAC_CSR4	0x0120	W	0x00000000	Channel 4 Status Register
DMAC_CPC4	0x0124	W	0x00000000	Channel 4 Program Counter Register
DMAC_CSR5	0x0128	W	0x00000000	Channel 5 Status Register
DMAC_CPC5	0x012c	W	0x00000000	Channel 5 Program Counter Register
DMAC_CSR6	0x0130	W	0x00000000	Channel 6 Status Register
DMAC_CPC6	0x0134	W	0x00000000	Channel 6 Program Counter Register
DMAC_CSR7	0x0138	W	0x00000000	Channel 7 Status Register
DMAC_CPC7	0x013c	W	0x00000000	Channel 7 Program Counter Register

DMAC_SAR0	0x0400	W	0x00000000	Channel 0 Source Address Register
DMAC_DAR0	0x0404	W	0x00000000	Channel 0 Destination Address Register
DMAC_CCR0	0x0408	W	0x00000000	Channel 0 Channel Control Register
DMAC_LC0_0	0x040c	W	0x00000000	Channel 0 Loop Counter 0 Register
DMAC_LC1_0	0x0410	W	0x00000000	Channel 0 Loop Counter 1 Register
DMAC_SAR1	0x0420	W	0x00000000	Channel 1 Source Address Register
DMAC_DAR1	0x0424	W	0x00000000	Channel 1 Destination Address Register
DMAC_CCR1	0x0428	W	0x00000000	Channel 1 Channel Control Register
DMAC_LC0_1	0x042c	W	0x00000000	Channel 1 Loop Counter 0 Register
DMAC_LC1_1	0x0430	W	0x00000000	Channel 1 Loop Counter 1 Register
DMAC_SAR2	0x0440	W	0x00000000	Channel 2 Source Address Register
DMAC_DAR2	0x0444	W	0x00000000	Channel 2 Destination Address Register
DMAC_CCR2	0x0448	W	0x00000000	Channel 2 Channel Control Register
DMAC_LC0_2	0x044c	W	0x00000000	Channel 2 Loop Counter 0 Register
DMAC_LC1_2	0x0450	W	0x00000000	Channel 2 Loop Counter 1 Register
DMAC_SAR3	0x0460	W	0x00000000	Channel 3 Source Address Register
DMAC_DAR3	0x0464	W	0x00000000	Channel 3 Destination Address Register
DMAC_CCR3	0x0468	W	0x00000000	Channel 3 Channel Control Register
DMAC_LC0_3	0x046c	W	0x00000000	Channel 3 Loop Counter 0 Register
DMAC_LC1_3	0x0470	W	0x00000000	Channel 3 Loop Counter 1 Register
DMAC_SAR4	0x0480	W	0x00000000	Channel 4 Address Register
DMAC_DAR4	0x0484	W	0x00000000	Channel 4 Destination Address Register
DMAC_CCR4	0x0488	W	0x00000000	Channel 4 Channel Control Register
DMAC_LC0_4	0x048c	W	0x00000000	Channel 4 Loop Counter 0 Register
DMAC_LC1_4	0x0490	W	0x00000000	Channel 4 Loop Counter 1 Register
DMAC_SAR5	0x04a0	W	0x00000000	Channel 5 Address Register
DMAC_DAR5	0x04a4	W	0x00000000	Channel 5 Destination Address Register
DMAC_CCR5	0x04a8	W	0x00000000	Channel 5 Channel Control Register

DMAC_LC0_5	0x04ac	W	0x00000000	Channel 5 Loop Counter 0 Register
DMAC_LC1_5	0x04b0	W	0x00000000	Channel 5 Loop Counter 1 Register
DMAC_SAR6	0x04c0	W	0x00000000	Channel 6 Source Address Register
DMAC_DAR6	0x04c4	W	0x00000000	Channel 6 Destination Address Register
DMAC_CCR6	0x04c8	W	0x00000000	Channel 6 Channel Control Register
DMAC_LC0_6	0x04cc	W	0x00000000	Channel 6 Loop Counter 0 Register
DMAC_LC1_6	0x04d0	W	0x00000000	Channel 6 Loop Counter 1 Register
DMAC_SAR7	0x04e0	W	0x00000000	Channel 7 Source Address Register
DMAC_DAR7	0x04e4	W	0x00000000	Channel 7 Destination Address Register
DMAC_CCR7	0x04e8	W	0x00000000	Channel 7 Channel Control Register
DMAC_LC0_7	0x04ec	W	0x00000000	Channel 7 Loop Counter 0 Register
DMAC_LC1_7	0x04f0	W	0x00000000	Channel 7 Loop Counter 1 Register
DMAC_DBGSTATUS	0x0d00	W	0x00000000	Debug Status Register
DMAC_DBGCMD	0x0d04	W	0x00000000	Debug Command Register
DMAC_DBGINST0	0x0d08	W	0x00000000	Debug Instruction-0 Register
DMAC_DBGINST1	0x0d0c	W	0x00000000	Debug Instruction-1 Register
DMAC_CR0	0x0e00	W	0x001f3075	Configuration Register 0
DMAC_CR1	0x0e04	W	0x000000b5	Configuration Register 1
DMAC_CR2	0x0e08	W	0x00000000	Configuration Register 2
DMAC_CR3	0x0e0c	W	0x0000ffff	Configuration Register 3
DMAC_CR4	0x0e10	W	0x000fffff	Configuration Register 4
DMAC_CRDn	0x0e14	W	0x07ff7f73	Configuration Register
DMAC_WD	0x0e80	W	0x00000000	DMA Watchdog Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.4.3 Detail Register Description

DMAC_DSR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RO	0x0	dns 1'b0: DMA manager operates in the Secure state 1'b1: DMA manager operates in the Non-secure state
8:4	RO	0x00	wakeup_event 5'h0: event[0] 5'h1: event[1] 5'h2: event[2] … 5'h1f: event[31]

Bit	Attr	Reset Value	Description
3:0	RO	0x0	dma_status 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'hf: Faulting Others: Reserved

DMAC_DPC

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_mgr Program counter for the DMA manager thread

DMAC_INTEN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	event_irq_select Bit [N] 1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request. 1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request.

DMAC_EVENT_RIS

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dmasev_active Bit [N] 1'b0: Event N is inactive or irq[N] is LOW 1'b1: Event N is active or irq[N] is HIGH

DMAC_INTMIS

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	irq_status Bit [N] 1'b0: Interrupt N is inactive and therefore irq[N] is LOW 1'b1: Interrupt N is active and therefore irq[N] is HIGH

DMAC_INTCLR

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	irq_clr Bit [N] 1'b0: The status of irq[N] does not change 1'b1: The DMAC sets irq[N] LOW if the DMAC_INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change.

DMAC_FSRD

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	fs_mgr 1'b0: The DMA manager thread is not in the Faulting state 1'b1: The DMA manager thread is in the Faulting state

DMAC_FSRC

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	fault_status Bit [N] 1'b0: No fault is present on DMA channel N 1'b1: DMA channel N is in the Faulting or Faulting completing state

DMAC_FTRD

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface
29:17	RO	0x0	reserved
16	RO	0x0	instr_fetch_err Performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response
15:6	RO	0x0	reserved
5	RO	0x0	mgr_evnt_err 1'b0: DMA manager has appropriate security to execute DMAWFE or DMASEV 1'b1: DMA manager thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt
4	RO	0x0	dmago_err 1'b0: DMA manager has appropriate security to execute DMAGO 1'b1: DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state
3:2	RO	0x0	reserved
1	RO	0x0	operand_invalid The configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand
0	RW	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction

DMAC_FTR0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR2

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR3

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR4

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR5

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

Bit	Attr	Reset Value	Description
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR6

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_FTR7

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr Memory or from the debug interface. 1'b0: Instruction that generated an abort was read from system memory 1'b1: Instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	data_read_err Thread performs a data read. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

Bit	Attr	Reset Value	Description
17	RO	0x0	data_write_err Thread performs a data write. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err Thread performs an instruction fetch. 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err To perform a secure read or secure write. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions. 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFP to wait for a secure peripheral b. DMALDP or DMASTP to notify a secure peripheral c. DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: A DMA channel thread in the Non-secure state attempted to execute either: a. DMAWFE to wait for a secure event b. DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	operand_invalid Valid for the configuration of the DMAC. 1'b0: Valid operand 1'b1: Invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: Defined instruction 1'b1: Undefined instruction This fault is a precise abort.

DMAC_CSR0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status Channel 0 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC0

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 0 thread

DMAC_CSR1

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status Channel 1 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC1

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 1 thread

DMAC_CSR2

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set

Bit	Attr	Reset Value	Description
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status Channel 2 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC2

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 2 thread

DMAC_CSR3

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status Channel 3 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC3

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 3 thread

DMAC_CSR4

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status Channel 4 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC4

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 4 thread

DMAC_CSR5

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status Channel 5 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC5

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 5 thread

DMAC_CSR6

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status Channel 6 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC6

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 6 thread

DMAC_CSR7

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	wakeup_number Indicate the event or peripheral number that the channel is waiting for. 5'h0: DMA channel is waiting for event, or peripheral, 0 5'h1: DMA channel is waiting for event, or peripheral, 1 5'h2: DMA channel is waiting for event, or peripheral, 2 … 5'h1f: DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status Channel 7 status. 4'h0: Stopped 4'h1: Executing 4'h2: Cache miss 4'h3: Updating PC 4'h4: Waiting for event 4'h5: At barrier 4'h7: Waiting for peripheral 4'h8: Killing 4'h9: Completing 4'he: Faulting completing 4'hf: Faulting Others: Reserved

DMAC_CPC7

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 7 thread

DMAC_SAR0

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 0

DMAC_DAR0

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 0

DMAC_CCR0

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_0

Address: Operational Base + offset (0x040c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_0

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR1

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 1

DMAC_DAR1

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 1

DMAC_CCR1

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_1

Address: Operational Base + offset (0x042c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_1

Address: Operational Base + offset (0x0430)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR2

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 2

DMAC_DAR2

Address: Operational Base + offset (0x0444)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 2

DMAC_CCR2

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_2

Address: Operational Base + offset (0x044c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_2

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR3

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 3

DMAC_DAR3

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 3

DMAC_CCR3

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

Bit	Attr	Reset Value	Description
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_3

Address: Operational Base + offset (0x046c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_3

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR4

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 4

DMAC_DAR4

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 4

DMAC_CCR4

Address: Operational Base + offset (0x0488)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH

Bit	Attr	Reset Value	Description
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

Bit	Attr	Reset Value	Description
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_4

Address: Operational Base + offset (0x048c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_4

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR5

Address: Operational Base + offset (0x04a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 5

DMAC_DAR5

Address: Operational Base + offset (0x04a4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 5

DMAC_CCR5

Address: Operational Base + offset (0x04a8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_5

Address: Operational Base + offset (0x04ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_5

Address: Operational Base + offset (0x04b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR6

Address: Operational Base + offset (0x04c0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 6

DMAC_DAR6

Address: Operational Base + offset (0x04c4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 6

DMAC_CCR6

Address: Operational Base + offset (0x04c8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_6

Address: Operational Base + offset (0x04cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_6

Address: Operational Base + offset (0x04d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_SAR7

Address: Operational Base + offset (0x04e0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 7

DMAC_DAR7

Address: Operational Base + offset (0x04e4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destination data for DMA channel 7

DMAC_CCR7

Address: Operational Base + offset (0x04e8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'h0: Writes 1 byte per beat 3'h1: Writes 2 bytes per beat 3'h2: Writes 4 bytes per beat 3'h3: Writes 8 bytes per beat 3'h4: Writes 16 bytes per beat Others: Reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'h0: 1 data transfer 4'h1: 2 data transfers 4'h2: 3 data transfers … 4'hf: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'h0: Reads 1 byte per beat 3'h1: Reads 2 bytes per beat 3'h2: Reads 4 bytes per beat 3'h3: Reads 8 bytes per beat 3'h4: Reads 16 bytes per beat Others: Reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMAC_LC0_7

Address: Operational Base + offset (0x04ec)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMAC_LC1_7

Address: Operational Base + offset (0x04f0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMAC_DBGSTATUS

Address: Operational Base + offset (0x0d00)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	dbgstatus 1'b0: Idle 1'b1: Busy

DMAC_DBGCMD

Address: Operational Base + offset (0x0d04)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	WO	0x0	dbgcmd 2'b00: Execute the instruction that the DMAC_DBGINST [1:0] Registers contain Others: Reserved

DMAC_DBGINST0

Address: Operational Base + offset (0x0d08)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte1 Instruction byte 1
23:16	WO	0x00	instruction_byte0 Instruction byte 0
15:11	RO	0x0	reserved
10:8	WO	0x0	channel_number 3'b000: DMA channel 0 3'b001: DMA channel 1 3'b010: DMA channel 2 … 3'b111: DMA channel 7
7:1	RO	0x0	reserved
0	WO	0x0	debug_thread 1'b0: DMA manager thread 1'b1: DMA channel

DMAC_DBGINST1

Address: Operational Base + offset (0x0d0c)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte5 Instruction byte 5
23:16	WO	0x00	instruction_byte4 Instruction byte 4
15:8	WO	0x00	instruction_byte3 Instruction byte 3
7:0	WO	0x00	instruction_byte2 Instruction byte 2

DMAC_CR0

Address: Operational Base + offset (0x0e00)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:17	RO	0x0f	num_events 5'h0: 1 interrupt output, irq[0] 5'h1: 2 interrupt outputs, irq[1:0] 5'h2: 3 interrupt outputs, irq[2:0] … 5'h1f: 32 interrupt outputs, irq[31:0]
16:12	RO	0x13	num_periph_req 5'h0: 1 peripheral request interface 5'h1: 2 peripheral request interfaces 5'h2: 3 peripheral request interfaces … 5'h1f: 32 peripheral request interfaces
11:7	RO	0x0	reserved
6:4	RO	0x7	num_chnls 3'b000: 1 DMA channel 3'b001: 2 DMA channels 3'b010: 3 DMA channels … 3'b111: 8 DMA channels
3	RO	0x0	reserved
2	RO	0x1	mgr_ns_at_rst 1'b0: boot_manager_ns was LOW 1'b1: boot_manager_ns was HIGH
1	RO	0x0	boot_en 1'b0: boot_from_pc was LOW 1'b1: boot_from_pc was HIGH
0	RO	0x1	periph_req 1'b0: The DMAC does not provide a peripheral request interface 1'b1: The DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies

DMAC_CR1

Address: Operational Base + offset (0x0e04)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0xb	num_i_cache_lines 4'b0000: 1 i-cache line 4'b0001: 2 i-cache lines 4'b0010: 3 i-cache lines … 4'b1111: 16 i-cache lines
3	RO	0x0	reserved
2:0	RO	0x5	i_cache_len 3'b010: 4 bytes 3'b011: 8 bytes 3'b100: 16 bytes 3'b101: 32 bytes Others: Reserved

DMAC_CR2

Address: Operational Base + offset (0x0e08)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	boot_addr Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMAC_CR3

Address: Operational Base + offset (0x0e0c)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	ins Bit [N] 1'b0: Assigns event<N> or irq[N] to the Secure state 1'b1: Assigns event<N> or irq[N] to the Non-secure state

DMAC_CR4

Address: Operational Base + offset (0x0e10)

Bit	Attr	Reset Value	Description
31:0	RO	0x000fffff	pns Bit [N] 1'b0: Assigns peripheral request interface N to the Secure state 1'b1: Assigns peripheral request interface N to the Non-secure state

DMAC_CRDn

Address: Operational Base + offset (0x0e14)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RO	0x07f	data_buffer_dep 10'b000000000: 1 line 10'b000000001: 2 lines … 10'b111111111: 1024 lines
19:16	RO	0xf	rd_q_dep 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
15	RO	0x0	reserved
14:12	RO	0x7	rd_cap 3'b000: 1 3'b001: 2 … 3'b111: 8
11:8	RO	0xf	wr_q_dep 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
7	RO	0x0	reserved
6:4	RO	0x7	wr_cap 3'b000: 1 3'b001: 2 … 3'b111: 8
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RO	0x3	data_width 3'b010: 32-bit 3'b011: 64-bit 3'b100: 128-bit Others:Reserved

DMAC_WD

Address: Operational Base + offset (0x0e80)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	wd_irq_only 1'b0: The DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1'b1: The DMAC sets irq_abort HIGH

10.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

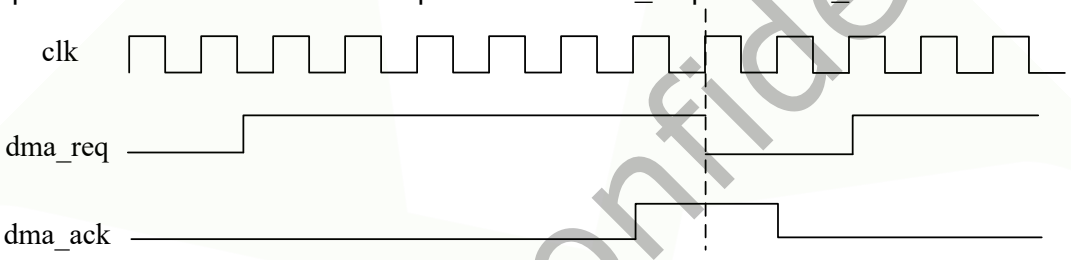


Fig. 10-3 DMAC Request and Acknowledge Timing

10.6 Interface Description

DMAC has the following tie-off signals. It can be configured by SGRF register. (Please refer to the SGRF chapter to find them)

Table 10-2 DMAC Boot Interface

DMAC0		
Interface	**Reset value**	**Control source**
boot_irq_ns	0xFFFF	sgrf_dmac0_con0[15:0]
boot_periph_ns	0xFFFFFFFF	{sgrf_dmac0_con2[15:0],sgrf_dmac0_con1[15:0]}
boot_manager_ns	0x1	sgrf_dmac0_con3[0]
grf_drtype_ch0	0x1	sgrf_dmac0_con4[1:0]
grf_drtype_ch1	0x1	sgrf_dmac0_con4[3:2]
grf_drtype_ch2	0x1	sgrf_dmac0_con4[5:4]
grf_drtype_ch3	0x1	sgrf_dmac0_con4[7:6]
grf_drtype_ch4	0x1	sgrf_dmac0_con4[9:8]
grf_drtype_ch5	0x1	sgrf_dmac0_con4[11:10]
grf_drtype_ch6	0x1	sgrf_dmac0_con4[13:12]
grf_drtype_ch7	0x1	sgrf_dmac0_con4[15:14]
grf_drtype_ch8	0x1	sgrf_dmac0_con5[1:0]
grf_drtype_ch9	0x1	sgrf_dmac0_con5[3:2]
grf_drtype_ch10	0x1	sgrf_dmac0_con5[5:4]
grf_drtype_ch11	0x1	sgrf_dmac0_con5[7:6]

grf_drtype_ch12	0x1	sgrf_dmac0_con5[9:8]
grf_drtype_ch13	0x1	sgrf_dmac0_con5[11:10]
grf_drtype_ch14	0x1	sgrf_dmac0_con5[13:12]
grf_drtype_ch15	0x1	sgrf_dmac0_con5[15:14]
grf_drtype_ch16	0x1	sgrf_dmac0_con6[1:0]
grf_drtype_ch17	0x1	sgrf_dmac0_con6[3:2]
grf_drtype_ch18	0x1	sgrf_dmac0_con6[5:4]
grf_drtype_ch19	0x1	sgrf_dmac0_con6[7:6]
grf_drtype_ch20	0x1	sgrf_dmac0_con6[9:8]
grf_drtype_ch21	0x1	sgrf_dmac0_con6[11:10]
grf_drtype_ch22	0x1	sgrf_dmac0_con6[13:12]
grf_drtype_ch23	0x1	sgrf_dmac0_con6[15:14]
grf_drtype_ch24	0x1	sgrf_dmac0_con7[1:0]
grf_drtype_ch25	0x1	sgrf_dmac0_con7[3:2]
grf_drtype_ch26	0x1	sgrf_dmac0_con7[5:4]
grf_drtype_ch27	0x1	sgrf_dmac0_con7[7:6]
grf_drtype_ch28	0x1	sgrf_dmac0_con7[9:8]
grf_drtype_ch29	0x1	sgrf_dmac0_con7[11:10]
grf_drtype_ch30	0x1	sgrf_dmac0_con7[13:12]
grf_drtype_ch31	0x1	sgrf_dmac0_con7[15:14]
grf_modify_dis_ch0	0x0	sgrf_dmac0_con8[0]
grf_modify_dis_ch1	0x0	sgrf_dmac0_con8[1]
grf_modify_dis_ch2	0x0	sgrf_dmac0_con8[2]
grf_modify_dis_ch3	0x0	sgrf_dmac0_con8[3]
grf_modify_dis_ch4	0x0	sgrf_dmac0_con8[4]
grf_modify_dis_ch5	0x0	sgrf_dmac0_con8[5]
grf_modify_dis_ch6	0x0	sgrf_dmac0_con8[6]
grf_modify_dis_ch7	0x0	sgrf_dmac0_con8[7]
grf_modify_dis_ch8	0x0	sgrf_dmac0_con8[8]
grf_modify_dis_ch9	0x0	sgrf_dmac0_con8[9]
grf_modify_dis_ch10	0x0	sgrf_dmac0_con8[10]
grf_modify_dis_ch11	0x0	sgrf_dmac0_con8[11]
grf_modify_dis_ch12	0x0	sgrf_dmac0_con8[12]
grf_modify_dis_ch13	0x0	sgrf_dmac0_con8[13]
grf_modify_dis_ch14	0x0	sgrf_dmac0_con8[14]
grf_modify_dis_ch15	0x0	sgrf_dmac0_con8[15]
grf_modify_dis_ch16	0x0	sgrf_dmac0_con9[0]
grf_modify_dis_ch17	0x0	sgrf_dmac0_con9[1]
grf_modify_dis_ch18	0x0	sgrf_dmac0_con9[2]
grf_modify_dis_ch19	0x0	sgrf_dmac0_con9[3]
grf_modify_dis_ch20	0x0	sgrf_dmac0_con9[4]
grf_modify_dis_ch21	0x0	sgrf_dmac0_con9[5]
grf_modify_dis_ch22	0x0	sgrf_dmac0_con9[6]
grf_modify_dis_ch23	0x0	sgrf_dmac0_con9[7]
grf_modify_dis_ch24	0x0	sgrf_dmac0_con9[8]

grf_modify_dis_ch25	0x0	sgrf_dmac0_con9[9]
grf_modify_dis_ch26	0x0	sgrf_dmac0_con9[10]
grf_modify_dis_ch27	0x0	sgrf_dmac0_con9[11]
grf_modify_dis_ch28	0x0	sgrf_dmac0_con9[12]
grf_modify_dis_ch29	0x0	sgrf_dmac0_con9[13]
grf_modify_dis_ch30	0x0	sgrf_dmac0_con9[14]
grf_modify_dis_ch31	0x0	sgrf_dmac0_con9[15]
DMAC1		
Interface	**Reset value**	**Control source**
boot_irq_ns	0xFFFF	sgrf_dmac1_con0[15:0]
boot_periph_ns	0xFFFFFFFF	{sgrf_dmac1_con2[15:0],sgrf_dmac1_con1[15:0]}
boot_manager_ns	0x1	sgrf_dmac1_con3[0]
grf_drtype_ch0	0x1	sgrf_dmac1_con4[1:0]
grf_drtype_ch1	0x1	sgrf_dmac1_con4[3:2]
grf_drtype_ch2	0x1	sgrf_dmac1_con4[5:4]
grf_drtype_ch3	0x1	sgrf_dmac1_con4[7:6]
grf_drtype_ch4	0x1	sgrf_dmac1_con4[9:8]
grf_drtype_ch5	0x1	sgrf_dmac1_con4[11:10]
grf_drtype_ch6	0x1	sgrf_dmac1_con4[13:12]
grf_drtype_ch7	0x1	sgrf_dmac1_con4[15:14]
grf_drtype_ch8	0x1	sgrf_dmac1_con5[1:0]
grf_drtype_ch9	0x1	sgrf_dmac1_con5[3:2]
grf_drtype_ch10	0x1	sgrf_dmac1_con5[5:4]
grf_drtype_ch11	0x1	sgrf_dmac1_con5[7:6]
grf_drtype_ch12	0x1	sgrf_dmac1_con5[9:8]
grf_drtype_ch13	0x1	sgrf_dmac1_con5[11:10]
grf_drtype_ch14	0x1	sgrf_dmac1_con5[13:12]
grf_drtype_ch15	0x1	sgrf_dmac1_con5[15:14]
grf_drtype_ch16	0x1	sgrf_dmac1_con6[1:0]
grf_drtype_ch17	0x1	sgrf_dmac1_con6[3:2]
grf_drtype_ch18	0x1	sgrf_dmac1_con6[5:4]
grf_drtype_ch19	0x1	sgrf_dmac1_con6[7:6]
grf_drtype_ch20	0x1	sgrf_dmac1_con6[9:8]
grf_drtype_ch21	0x1	sgrf_dmac1_con6[11:10]
grf_drtype_ch22	0x1	sgrf_dmac1_con6[13:12]
grf_drtype_ch23	0x1	sgrf_dmac1_con6[15:14]
grf_drtype_ch24	0x1	sgrf_dmac1_con7[1:0]
grf_drtype_ch25	0x1	sgrf_dmac1_con7[3:2]
grf_drtype_ch26	0x1	sgrf_dmac1_con7[5:4]
grf_drtype_ch27	0x1	sgrf_dmac1_con7[7:6]
grf_drtype_ch28	0x1	sgrf_dmac1_con7[9:8]
grf_drtype_ch29	0x1	sgrf_dmac1_con7[11:10]
grf_drtype_ch30	0x1	sgrf_dmac1_con7[13:12]
grf_drtype_ch31	0x1	sgrf_dmac1_con7[15:14]

grf_modify_dis_ch0	0x0	sgrf_dmac1_con8[0]
grf_modify_dis_ch1	0x0	sgrf_dmac1_con8[1]
grf_modify_dis_ch2	0x0	sgrf_dmac1_con8[2]
grf_modify_dis_ch3	0x0	sgrf_dmac1_con8[3]
grf_modify_dis_ch4	0x0	sgrf_dmac1_con8[4]
grf_modify_dis_ch5	0x0	sgrf_dmac1_con8[5]
grf_modify_dis_ch6	0x0	sgrf_dmac1_con8[6]
grf_modify_dis_ch7	0x0	sgrf_dmac1_con8[7]
grf_modify_dis_ch8	0x0	sgrf_dmac1_con8[8]
grf_modify_dis_ch9	0x0	sgrf_dmac1_con8[9]
grf_modify_dis_ch10	0x0	sgrf_dmac1_con8[10]
grf_modify_dis_ch11	0x0	sgrf_dmac1_con8[11]
grf_modify_dis_ch12	0x0	sgrf_dmac1_con8[12]
grf_modify_dis_ch13	0x0	sgrf_dmac1_con8[13]
grf_modify_dis_ch14	0x0	sgrf_dmac1_con8[14]
grf_modify_dis_ch15	0x0	sgrf_dmac1_con8[15]
grf_modify_dis_ch16	0x0	sgrf_dmac1_con9[0]
grf_modify_dis_ch17	0x0	sgrf_dmac1_con9[1]
grf_modify_dis_ch18	0x0	sgrf_dmac1_con9[2]
grf_modify_dis_ch19	0x0	sgrf_dmac1_con9[3]
grf_modify_dis_ch20	0x0	sgrf_dmac1_con9[4]
grf_modify_dis_ch21	0x0	sgrf_dmac1_con9[5]
grf_modify_dis_ch22	0x0	sgrf_dmac1_con9[6]
grf_modify_dis_ch23	0x0	sgrf_dmac1_con9[7]
grf_modify_dis_ch24	0x0	sgrf_dmac1_con9[8]
grf_modify_dis_ch25	0x0	sgrf_dmac1_con9[9]
grf_modify_dis_ch26	0x0	sgrf_dmac1_con9[10]
grf_modify_dis_ch27	0x0	sgrf_dmac1_con9[11]
grf_modify_dis_ch28	0x0	sgrf_dmac1_con9[12]
grf_modify_dis_ch29	0x0	sgrf_dmac1_con9[13]
grf_modify_dis_ch30	0x0	sgrf_dmac1_con9[14]
grf_modify_dis_ch31	0x0	sgrf_dmac1_con9[15]

boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.
boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.
boot_periph_ns
Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH

The DMAC assigns peripheral request interface x to the Non-secure state.

grf_drtype_<x>

The DMAC sets the state of the request_type flag:
grf_drtype_<x>[1:0]=b00: request_type<x> = Single.
grf_drtype_<x>[1:0]=b01: request_type<x> = Burst.

10.7 Application Notes

10.7.1 Using the APB Slave Interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-secure state.
The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DMAC_DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DMAC_DBGINST0 Register and enter the:

- Instruction byte 0 encoding for DMAGO.
- Instruction byte 1 encoding for DMAGO.
- Debug thread bit to 0. This selects the DMA manager thread.

5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program that was written to system memory in step 2.
6. Writing zero to the DMAC_DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

10.7.2 Security Usage

DMA manager thread is in the secure state

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:
ns = 0
The DMAC does not start a DMA channel thread and instead it:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

ns = 1
The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:
INS = 0
The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
INS = 1
The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:
INS = 0
The event-interrupt resource is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.
When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.
When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses.

DMA channel thread is in the Non-secure state

When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.

When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it waits for the peripheral to signal a request. If:

PNS = 0

The peripheral is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends an acknowledgement to the peripheral. If:

PNS = 0

The peripheral is in the secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

10.7.3 Programming Restrictions

Fixed unaligned bursts
The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
- src_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_SARn(n=0~7) Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write
- dst_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_DARn(n=0~7) Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions
If you program the endian_swap_size field in the DMAC_CCRn(n=0~7) Register, to enable a DMA channel to perform an endian swap then you must set the corresponding DMAC_SARn(n=0~7) Register and the corresponding DMAC_DARn(n=0~7) Register to contain an address that is aligned to the value that the endian_swap_size field contains.
Updating DMA channel control registers during a DMA cycle restrictions
Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the DMAC_CCRn(n=0~7) Register, DMAC_SARn(n=0~7) Register, and DMAC_DARn(n=0~7) Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.
Resource sharing between DMA channels
DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

10.7.4 Unaligned Transfers

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.
Data corruption might occur if all of the following are true:
1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across

two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below).

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be split across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.
Most applications of DMA do not split data in this way, so are NOT vulnerable to data corruption from this defect.
The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size.

Table 10-3 Source Size in DMAC_CCRn

Source size in DMAC_CCRn	Allowed offset between DMAC_SARn and DMAC_DARn
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

10.7.5 Interrupt Sharing between Channels

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.
There are 4 likely information sources that can be used to determine the progress made by a program:
- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.
The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:
1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

10.7.6 Instruction Sets

Table 10-4 DMAC Instruction Sets

Mnemonic	Instruction	Thread Usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C

DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

10.7.7 Assembler Directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. For the other instructions, please refer to pl330_trm.pdf.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the DMAC_SARn(n=0~7) Register or DMAC_DARn(n=0~7) Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 10-5 DMAC Instruction Encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

DMAC_SARn(n=0~7) Register and sets ra to 0.

DAR

DMAC_DARn(n=0~7) Register and sets ra to 1.

<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

Chapter 11 Timer

11.1 Overview

Timer is a programmable timer peripheral. This component is an APB slave device. There are 6 timers(Timer0~5) and 2 Secure timers(STimer0~1). CNTPCT_EL0 is provided by STimer1.

Timer5 and STimer0~1 count up from zero to a programmed value and generate an interrupt when the counter reaches the programmed value.

Timer0~4 count down from a programmed value to zero and generate an interrupt when the counter reaches zero.

Timer supports the following features:

- Timer0~5 is used for no-secure, STimer0~1 is used for secure.
- Two operation modes: free-running and user-defined count.
- Maskable for each individual interrupt.

11.2 Block Diagram

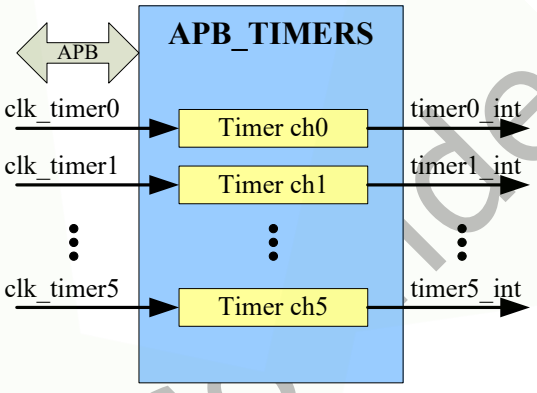


Fig. 11-1 Timer Block Diagram

The above figure shows the architecture of the APB timers (include six programmable timer channels). The Stimers that in the bus subsystem only include two programmable timer channels.

11.3 Function Description

11.3.1 Timer clock

TIMER0~ TIMER5 and STIMER0~1 are in the pd_bus subsystem. The clock source is 24MHz.

11.3.2 Programming sequence

1. Initialize the timer by the TIMERn_CONTROLREG (0≤n≤5) register:

- Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
- Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
- Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).

2. Load the timer count value into the TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMERn_LOAD_COUNT0 (0≤n≤5) register.

3. Enable the timer by writing a "1" to bit 0 of TIMERn_CONTROLREG (0≤n≤5).

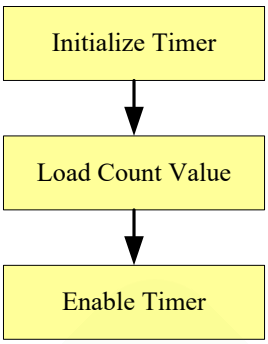


Fig. 11-2 Timer Usage Flow

11.3.3 Loading a timer count value

For the descending Timers(Timer0~4).The initial value for each timer—that is, the value from which it counts down—is loaded into the timer using the load count register (TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0). Two events can cause a timer to load the initial value from its load count register:

- Timer is enabled after reset or disabled.
- Timer counts down to 0, when timer is configured into free-running mode.

For the incremental Timers(Timer5 and STimer0~1).The initial value for each timer is zero. The count register will count up to the value loaded in the register TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0. Two events can cause a timer to load zero:

- Timer is enabled after reset or disabled.
- Timer counts up to the value stored in TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0, when timer is configured into free-running mode.

11.3.4 Timer mode selection

- User-defined count mode – Timer loads TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_ COUNT0 registers (for descending timers) or zero (for incremental timers) as initial value. When the timer counts down to 0 (for descending timers) or counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_ COUNT0 (for incremental timers),it will not automatically reload the count register. User need to disable timer firstly and follow the programming sequence to make timer work again.
- Free-running mode – Timer loads the TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0(for descending timers) or zero (for incremental timers)register as initial value. Timer will automatically reload the count register, when timer counts down to 0 (for descending timers) or counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0 (for incremental timers).

11.4 Register Description

11.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Timern Load Count Register 0
TIMER_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	Timern Load Count Register 1.Higher 32 bits Value to be loaded into Timer n. This is the value from which counting commences
TIMER_TIMERn_CURRENT_VALUE0	0x0008	W	0x00000000	Timern Current Value Register 0
TIMER_TIMERn_CURRENT_VALUE1	0x000c	W	0x00000000	Timern Current Value Register 1.High 32 bits of Current Value of Timer n
TIMER_TIMERn_CONTROLREG	0x0010	W	0x00000000	Timern Control Register
TIMER_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timern Interrupt Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.4.2 Detail Register Description

TIMER_TIMERn_LOAD_COUNT0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_0 Lower 32 bits Value to be loaded into Timer n. This is the value from which counting commences.

TIMER_TIMERn_LOAD_COUNT1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_1 Higher 32 bits Value to be loaded into Timer n. This is the value from which counting commences.

TIMER_TIMERn_CURRENT_VALUE0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timern_current_value0 Lower 32 bits of Current Value of Timer n

TIMER_TIMERn_CURRENT_VALUE1

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timern_current_value1 Higher 32 bits of Current Value of Timer n

TIMER_TIMERn_CONTROLREG

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	Reserved
2	RW	0x0	timer_int_en Timer interrupt enable. 1'b0: disable 1'b1: enable
1	RW	0x0	timer_mode Timer mode. 1'b0: Free-running mode 1'b1: User-defined count mode
0	RW	0x0	timer_en Timer enable. 1'b0: Disable 1'b1: Enable

TIMER_TIMERn_INTSTATUS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	Reserved
0	RO	0x0	timern_int This register contains the interrupt status for timern.

11.5 Application Notes

11.5.1 Register Base Address

Table 11-1 Register Base Address

Module	CNT	Base Addr
TIMER	TIMER0_BASE	0xFF700000
	TIMER1_BASE	0xFF700020
	TIMER2_BASE	0xFF700040
	TIMER3_BASE	0xFF700060

Module	CNT	Base Addr
	TIMER4_BASE	0xFF700080
	TIMER5_BASE	0xFF7000a0
STIMER	STIMER0_BASE	0xFF710000
	STIMER1_BASE	0xFF710020

11.5.2 Clock and Enable

In the chip, the timer_clk is from 24MHz XIN_OSC, asynchronous to the pclk. When user disables the timer enables bit (bit 0 of TIMERn_CONTROLREG (0≤n≤5)), the timer en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-config registers when timer_en is low.

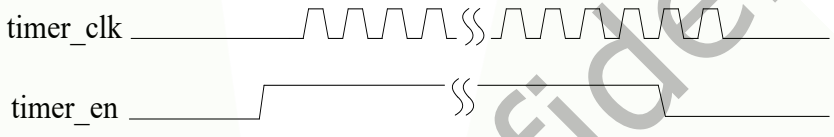


Fig. 11-3 Timing between timer_en and timer_clk

Please refer to function description section for the timer usage flow.

Chapter 12 Watchdog

12.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that may becaused by conflicting parts or programs in a SoC.The WDT would generate interrupt or reset signal when it's counter reaches zero, then a reset controller would reset the system. There is a Non-secure WDT(WDT_NS) and a Secure WDT(WDT_S); WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock is pclk
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period
- Supports speed up simulation through GRF

12.2 Block Diagram

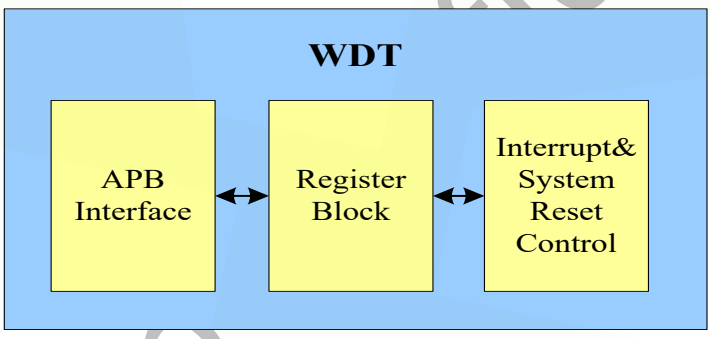


Fig. 12-1WDT block diagram

Block Descriptions:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & system reset control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

12.3 Function Description

12.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR). (After the counter counts down to 0, it will reload back to the initial value and restart counting.)

Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets

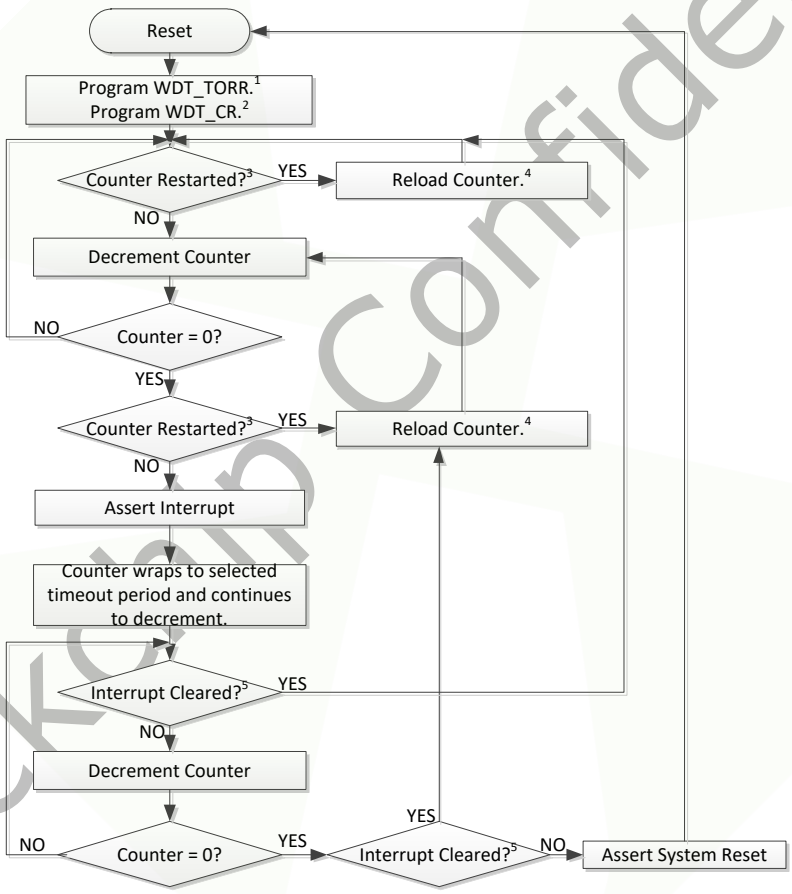
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

12.3.2 Programming sequence

Operation Flow Chart (Response mode=1)



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 12-2WDT Operation Flow

12.4 Register Description

This section describes the control/status registers of the design.

12.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x0000000A	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout Range Register
WDT_CCVR	0x0008	W	0x0000FFFF	Current Counter Value Register
WDT_CRR	0x000C	W	0x00000000	Counter Restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt Status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt Clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.2 Detail Registers Description

WDT_CR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x2	rst_pluse_length This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x1	resp_mode Selects the output response generated to a timeout. 1'b0: Generate a system reset. 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	wdt_en Writable when the configuration parameter WDT_ALWAYS_EN=0, otherwise,it is readable. This bit is used to enable and disable the DW_apb_wdt.When disabled, the counter dose not decrement .Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset. 1'b0: WDT disabled. 1'b1: WDT enabled.

WDT_TORR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	timeout_period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff 4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	cur_cnt This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read

WDT_CRR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	cnt_restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	wdt_status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity. 1'b0: Interrupt is inactive.

WDT_EOI

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	wdt_int_clr This can be used to clear the interrupt without restarting the watchdog counter.

Chapter 13 System Debug

13.1 Overview

The chip uses the DAP-LITE2 Technology to support real-time debug.

13.1.1 Features

- Invasive debug with core halted
- SW-DP

13.1.2 Debug components address map

The following table shows the debug components address in memory map:

Module	Base Address
DAP_ROM	0xfd900000

13.2 Block Diagram

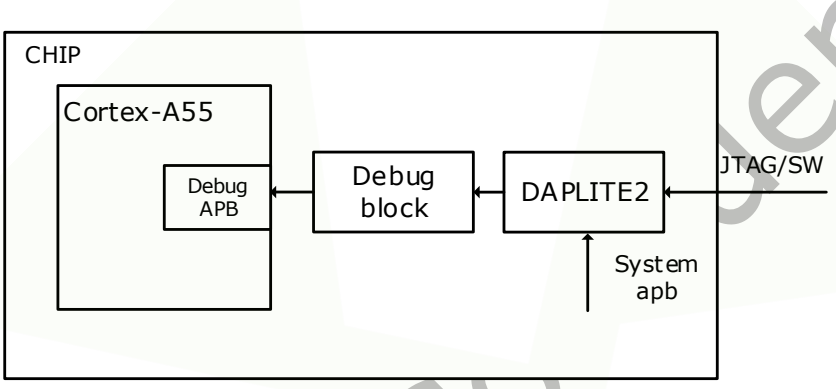


Fig. 13-1Debug system structure

13.3 Function Description

13.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port(SWJ-DP)
- APB Access Port(APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lite2. This interface controls any access ports provided within the DAP-Lite2. The DAP-Lite2 supports a combined debug port which includes both JTAG and Serial Wire Debug(SWD), with a mechanism that supports switching between them.

The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.

The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit[31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.

More information please refer to the document CoreSight_DAPLite2_TRM_r0p0.pdf for the debug detail description.

13.4 Register Description

Please refer to the document CoreSight_DAPLite2_TRM_r0p0.pdf for the debug detail description.

13.5 Interface Description

13.5.1 DAP SWJ-DP Interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug(SWJ) to JTAG probe to a target.

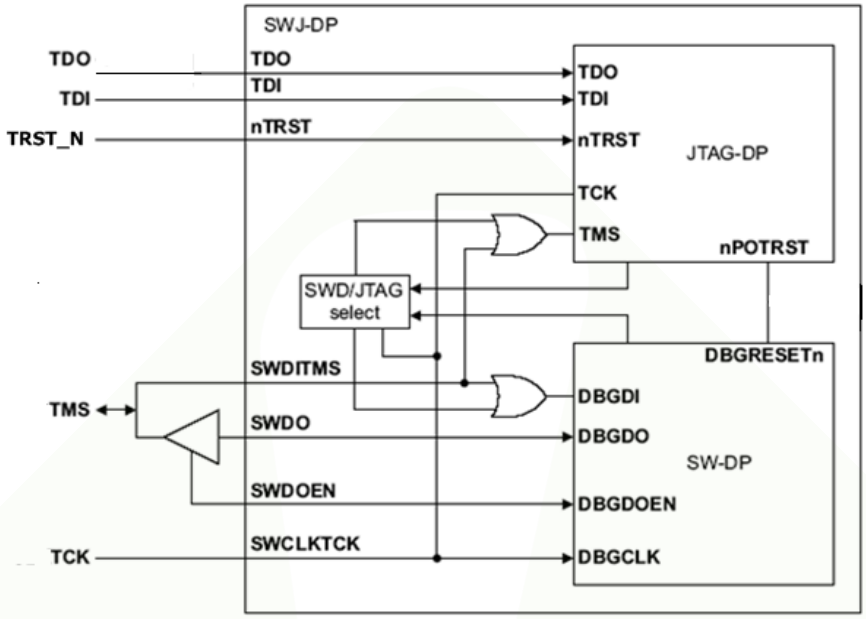


Fig. 13-2 DAP SWJ Interface

13.5.2 DAP SW-DP Interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.

The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

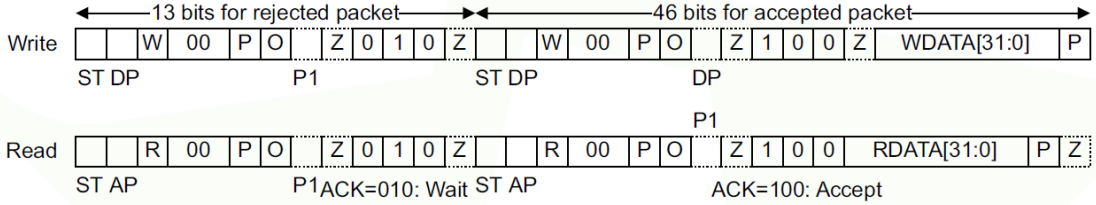


Fig. 13-3 SW-DP Acknowledgement Timing

Table 13-1 SW-DP Interface Description

Module pin	Dir.	Pad name	IOMUX
jtag_tck	I	SDMMC0_D2/JTAG_TCK/UART5_CTSn_M0/ GPIO1_D7_u	GRF_GPIO1D_IOMUX_H[14:12]=3'b010
jtag_tms	I/O	SDMMC0_D3/JTAG_TMS/UART5_RTSn_M0/ GPIO2_A0_u	GRF_GPIO2A_IOMUX_L[2:0]=3'b010

Notes: I=input, O=output, I/O=input/output, bidirectional.

Chapter 14 Mailbox

14.1 Overview

The Mailbox module is a simple APB peripheral that allows Cortex-A7, MCU core to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.
The Mailbox has the following main features:

- Support APB interface
- Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to Cortex-A7, and MCU core
- Provide 32 lock registers for software to use to indicate whether mailbox is occupied

14.2 Block Diagram

The figure below shows Mailbox block diagram:

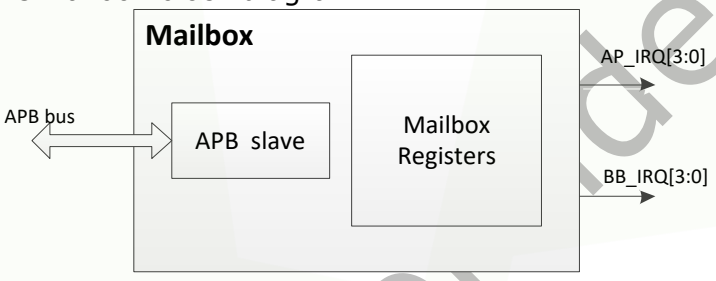


Fig. 14-1 Mailbox Block Diagram

14.3 Function Description

14.3.1 Mailbox

- Regard Cortex-A7 as the "AP" side of the Mailbox. The four elements combined interrupt (|mailbox_irq_ap[3:0]) to Cortex-A7 is:
  - Enabled when IRQs[111] is enabled in the GIC and MAILBOX_B2A_INTEN[i] is set to 1. (i=0~3)
  - Generated when there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS[i].
- Regard MCU core as the "BB" side of the Mailbox. The four elements combined interrupt (|mailbox_irq_bb[3:0]) to MCU core is:
  - Enabled when IRQs[112]/IRQs[13] is enabled in the INTC/IPIC of MCU core and MAILBOX_A2B_INTEN[i] is set to 1. (i=0~3)
  - Generated when there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS[i].
- You can also regard Cortex-A7 as the "BB" side of the Mailbox and regard MCU core as the "AP" side of the Mailbox. The configuration flow is similar.

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x0000	W	0x00000000	AP to BB Interrupt Enable Register
MAILBOX_A2B_STATUS	0x0004	W	0x00000000	AP to BB Interrupt Status Register
MAILBOX_A2B_CMD_0	0x0008	W	0x00000000	AP to BB Command 0 Register
MAILBOX_A2B_DAT_0	0x000C	W	0x00000000	AP to BB Data 0 Register
MAILBOX_A2B_CMD_1	0x0010	W	0x00000000	AP to BB Command 1 Register
MAILBOX_A2B_DAT_1	0x0014	W	0x00000000	AP to BB Data 1 Register
MAILBOX_A2B_CMD_2	0x0018	W	0x00000000	AP to BB Command 2 Register
MAILBOX_A2B_DAT_2	0x001C	W	0x00000000	AP to BB Data 2 Register
MAILBOX_A2B_CMD_3	0x0020	W	0x00000000	AP to BB Command 3 Register
MAILBOX_A2B_DAT_3	0x0024	W	0x00000000	AP to BB Data 3 Register
MAILBOX_B2A_INTEN	0x0028	W	0x00000000	BB to AP Interrupt Enable Register
MAILBOX_B2A_STATUS	0x002C	W	0x00000000	BB to AP Interrupt Status Register
MAILBOX_B2A_CMD_0	0x0030	W	0x00000000	BB to AP Command 0 Register
MAILBOX_B2A_DAT_0	0x0034	W	0x00000000	BB to AP Data 0 Register
MAILBOX_B2A_CMD_1	0x0038	W	0x00000000	BB to AP Command 1 Register
MAILBOX_B2A_DAT_1	0x003C	W	0x00000000	BB to AP Data 1 Register
MAILBOX_B2A_CMD_2	0x0040	W	0x00000000	BB to AP Command 2 Register
MAILBOX_B2A_DAT_2	0x0044	W	0x00000000	BB to AP Data 2 Register
MAILBOX_B2A_CMD_3	0x0048	W	0x00000000	BB to AP Command 3 Register
MAILBOX_B2A_DAT_3	0x004C	W	0x00000000	BB to AP Data 3 Register
MAILBOX_ATOMIC_LOCK_00	0x0100	W	0x00000000	Atomic Lock 00 Register
MAILBOX_ATOMIC_LOCK_01	0x0104	W	0x00000000	Atomic Lock 01 Register
MAILBOX_ATOMIC_LOCK_02	0x0108	W	0x00000000	Atomic Lock 02 Register
MAILBOX_ATOMIC_LOCK_03	0x010C	W	0x00000000	Atomic Lock 03 Register
MAILBOX_ATOMIC_LOCK_04	0x0110	W	0x00000000	Atomic Lock 04 Register
MAILBOX_ATOMIC_LOCK_05	0x0114	W	0x00000000	Atomic Lock 05 Register
MAILBOX_ATOMIC_LOCK_06	0x0118	W	0x00000000	Atomic Lock 06 Register
MAILBOX_ATOMIC_LOCK_07	0x011C	W	0x00000000	Atomic Lock 07 Register
MAILBOX_ATOMIC_LOCK_08	0x0120	W	0x00000000	Atomic Lock 08 Register
MAILBOX_ATOMIC_LOCK_09	0x0124	W	0x00000000	Atomic Lock 09 Register
MAILBOX_ATOMIC_LOCK_10	0x0128	W	0x00000000	Atomic Lock 10 Register
MAILBOX_ATOMIC_LOCK_11	0x012C	W	0x00000000	Atomic Lock 11 Register
MAILBOX_ATOMIC_LOCK_12	0x0130	W	0x00000000	Atomic Lock 12 Register
MAILBOX_ATOMIC_LOCK_13	0x0134	W	0x00000000	Atomic Lock 13 Register
MAILBOX_ATOMIC_LOCK_14	0x0138	W	0x00000000	Atomic Lock 14 Register
MAILBOX_ATOMIC_LOCK_15	0x013C	W	0x00000000	Atomic Lock 15 Register

Name	Offset	Size	Reset Value	Description
MAILBOX_ATOMIC_LOCK_16	0x0140	W	0x00000000	Atomic Lock 16 Register
MAILBOX_ATOMIC_LOCK_17	0x0144	W	0x00000000	Atomic Lock 17 Register
MAILBOX_ATOMIC_LOCK_18	0x0148	W	0x00000000	Atomic Lock 18 Register
MAILBOX_ATOMIC_LOCK_19	0x014C	W	0x00000000	Atomic Lock 19 Register
MAILBOX_ATOMIC_LOCK_20	0x0150	W	0x00000000	Atomic Lock 20 Register
MAILBOX_ATOMIC_LOCK_21	0x0154	W	0x00000000	Atomic Lock 21 Register
MAILBOX_ATOMIC_LOCK_22	0x0158	W	0x00000000	Atomic Lock 22 Register
MAILBOX_ATOMIC_LOCK_23	0x015C	W	0x00000000	Atomic Lock 23 Register
MAILBOX_ATOMIC_LOCK_24	0x0160	W	0x00000000	Atomic Lock 24 Register
MAILBOX_ATOMIC_LOCK_25	0x0164	W	0x00000000	Atomic Lock 25 Register
MAILBOX_ATOMIC_LOCK_26	0x0168	W	0x00000000	Atomic Lock 26 Register
MAILBOX_ATOMIC_LOCK_27	0x016C	W	0x00000000	Atomic Lock 27 Register
MAILBOX_ATOMIC_LOCK_28	0x0170	W	0x00000000	Atomic Lock 28 Register
MAILBOX_ATOMIC_LOCK_29	0x0174	W	0x00000000	Atomic Lock 29 Register
MAILBOX_ATOMIC_LOCK_30	0x0178	W	0x00000000	Atomic Lock 30 Register
MAILBOX_ATOMIC_LOCK_31	0x017C	W	0x00000000	Atomic Lock 31 Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

MAILBOX_A2B_INTEN

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int3 Interrupt enable for int3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int2 Interrupt enable for int2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int1 Interrupt enable for int1. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
0	RW	0x0	int0 Interrupt enable for int0. 1'b0: Disable 1'b1: Enable

MAILBOX_A2B_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	int3 Interrupt status for int3. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
2	W1C	0x0	int2 Interrupt status for int2. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
1	W1C	0x0	int1 Interrupt status for int1. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	int0 Interrupt status for int0. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_A2B_CMD_0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_2

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_3

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_3

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_INTEN

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int3 Interrupt enable for int3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int2 Interrupt enable for int2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int1 Interrupt enable for int1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int0 Interrupt enable for int0. 1'b0: Disable 1'b1: Enable

MAILBOX_B2A_STATUS

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	int3 Interrupt status for int3. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

Bit	Attr	Reset Value	Description
2	W1C	0x0	int2 Interrupt status for int2. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
1	W1C	0x0	int1 Interrupt status for int1. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	int0 Interrupt status for int0. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_B2A_CMD_0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_0

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_1

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_1

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_2

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_2

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_3

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_3

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_ATOMIC_LOCK_00

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_01

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_02

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_03

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_04

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_05

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_06

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_07

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_08

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_09

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_11

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_12

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_15

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_16

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_18

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_19

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_20

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_21

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_22

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_23

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_24

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_25

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_26

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_27

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_28

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_29

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_30

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

MAILBOX_ATOMIC_LOCK_31

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	atomic_lock Atomic lock flag bit.

14.5 Application Notes

- It is recommended to read one ATOMIC_LOCK register first when using the Mailbox. The read value is 0 means it is available, and 1 means it has been automatically locked. Writing to the ATOMIC_LOCK register will clear this bit.
- Write to the CMD register before writing to the DAT register. If wrong order is used, then the interrupt cannot be generated successfully.
- If you want to clear the interrupt, you can read out the STATUS register and writing 1 to corresponding bit.

Chapter 15 Pulse Width Modulation (PWM)

15.1 Overview

The pulse-width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components.
The PWM module supports the following features:

- 4-built-in PWM channels
- Support capture mode
  - Measures the high/low polarity effective cycles of the input waveform
  - Generates a single interrupt at the transition of input waveform polarity
  - 32-bit high polarity capture register
  - 32-bit low polarity capture register
  - 32-bit current value register
  - The capture result can be stored in a FIFO, and the depth of FIFO is 8. The data of FIFO can be read by CPU or DMA
  - Channel 3 support 32-bits power key capture mode
  - Support switch channel IO between channel 3 and channel0/1/2
  - Support a input filter to remove glitch
- Support continuous mode or one-shot mode
  - 32-bit period counter
  - 32-bit duty register
  - 32-bit current value register
  - PWM output polarity in inactive state and duty cycle polarity can be configured
  - Period and duty cycle are shadow buffered. Change takes effect when the end of the effective period is reached or when the channel is disabled
  - Programmable center or left aligned outputs, and change takes effect when the end of the effective period is reached or when the channel is disabled
  - 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value, and generates a single interrupt at the end of operation
  - Continuous mode generates the waveform continuously, and does not generates any interrupts
- Support 2 main clock input, one is from crystal oscillator and the frequency is fixed, the other one is from PLL and the frequency can be configured. Each channel can select one of the clocks according to requirement.
- Support two-level frequency division.
- Available low-power mode to reduce power consumption when the channel is inactive.

15.2 Block Diagram

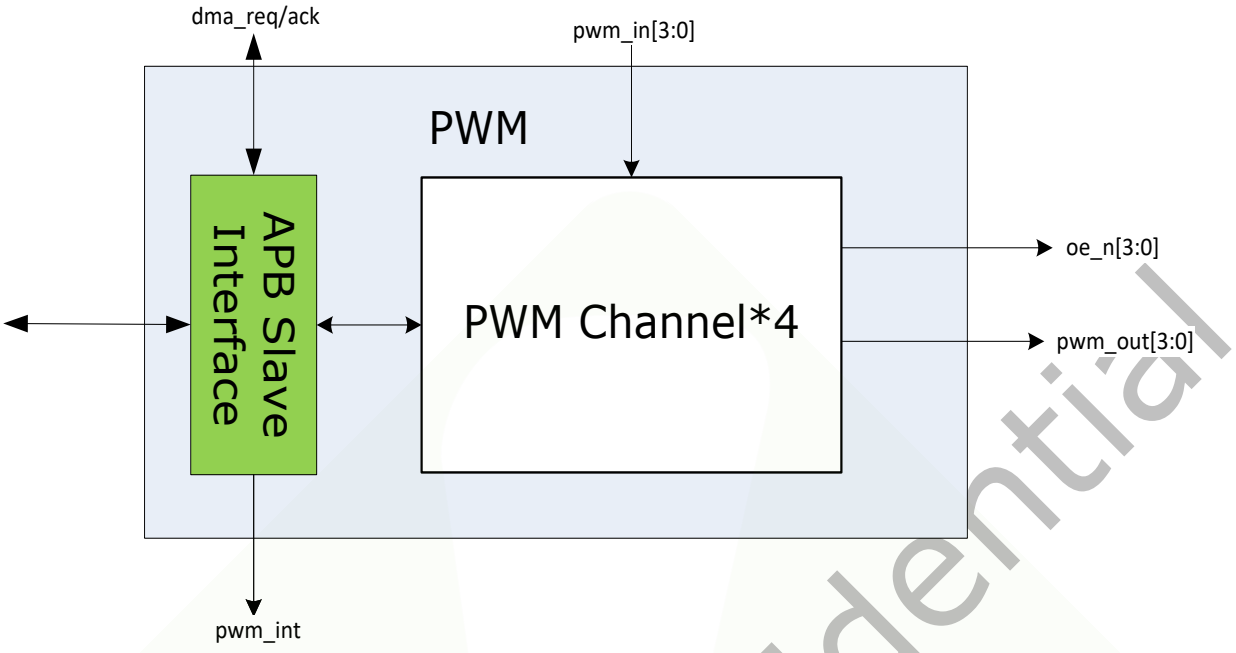


Fig. 15-1 PWM Block Diagram

The host processor gets access to PWM Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt. PWM only supports one interrupt output, please refer to interrupt register to know the raw interrupt status when an interrupt is asserted.

PWM Channel is the control logic of PWM module, and controls the operation of PWM module according to the configured working mode.

15.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

15.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock, and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWMx_PERIOD_HPC register, while the number of the low effective cycles is recorded in the PWMx_DUTY_LPC register.

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWMx_PERIOD_HPC and PWMx_DUTY_LPC.

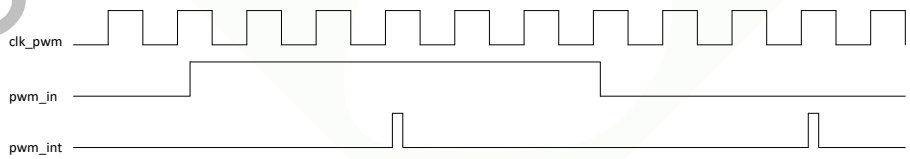


Fig. 15-2 PWM Capture Mode

The capture result can also be stored in a FIFO. The FIFO has an almost full indicator. The indicator can chose to use as an interrupt or DMA request. When it is used as an interrupt, the data in FIFO can be read by CPU. When it is used as a DMA request, the data in FIFO can be read through DMA. It also supports timeout interrupt when the data in FIFO has not been read in a time threshold.

The PWM (only channel 3) support 32-bits power key capture mode. User can configure 10 power key to match, user can poll the status to judge whether a power key access.

15.3.2 Continuous mode

The PWM channel generates a series of the pulses continuously as expected once the channel is enabled with continuous mode.

In the continuous mode, the PWM output waveforms can be in one form of the two output mode: left-aligned mode or center-aligned mode.

For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. After the period number (PWMx_PERIOD_HPC) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

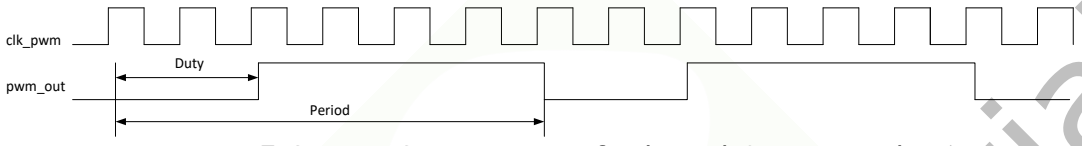


Fig. 15-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once one half of duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally after the period number (PWMx_PERIOD_HPC) is reached, the output starts another period of desired pulse.

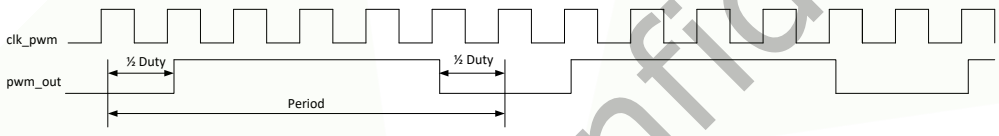


Fig. 15-4 PWM Continuous Center-aligned Output Mode

Once disable the PWM channel, the channel stops generating the output waveforms and output polarity is fixed as the configured inactive polarity (PWMx_CTRL.inactive_pol).

15.3.3 One-shot mode

Unlike the continuous mode, the PWM channel generates the output waveforms within the configured periods (PWM_CTRL.rpt + 1), and then stops. At the same times, an interrupt is asserted to inform that the operation has been finished.

There are also two output modes for the one-shot mode: the left-aligned mode and the center-aligned mode.

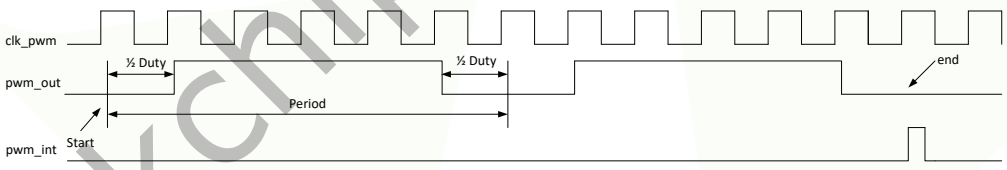


Fig. 15-5 PWM One-shot Center-aligned Output Mode

15.4 Register Description

15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_PWM0_CNT	0x0000	W	0x00000000	PWM Channel 0 Counter Register
PWM_PWM0_PERIOD_HPR	0x0004	W	0x00000000	PWM Channel 0 Period Register/High Polarity Capture Register
PWM_PWM0_DUTY_LPR	0x0008	W	0x00000000	PWM Channel 0 Duty Register/Low Polarity Capture Register
PWM_PWM0_CTRL	0x000C	W	0x00000000	PWM Channel 0 Control Register

Name	Offset	Size	Reset Value	Description
PWM_PWM1_CNT	0x0010	W	0x00000000	PWM Channel 1 Counter Register
PWM_PWM1_PERIOD_HPR	0x0014	W	0x00000000	PWM Channel 1 Period Register/High Polarity Capture Register
PWM_PWM1_DUTY_LPR	0x0018	W	0x00000000	PWM Channel 1 Duty Register/Low Polarity Capture Register
PWM_PWM1_CTRL	0x001C	W	0x00000000	PWM Channel 1 Control Register
PWM_PWM2_CNT	0x0020	W	0x00000000	PWM Channel 2 Counter Register
PWM_PWM2_PERIOD_HPR	0x0024	W	0x00000000	PWM Channel 2 Period Register/High Polarity Capture Register
PWM_PWM2_DUTY_LPR	0x0028	W	0x00000000	PWM Channel 2 Duty Register/Low Polarity Capture Register
PWM_PWM2_CTRL	0x002C	W	0x00000000	PWM Channel 2 Control Register
PWM_PWM3_CNT	0x0030	W	0x00000000	PWM Channel 3 Counter Register
PWM_PWM3_PERIOD_HPR	0x0034	W	0x00000000	PWM Channel 3 Period Register/High Polarity Capture Register
PWM_PWM3_DUTY_LPR	0x0038	W	0x00000000	PWM Channel 3 Duty Register/Low Polarity Capture Register
PWM_PWM3_CTRL	0x003C	W	0x00000000	PWM Channel 3 Control Register
PWM_INTSTS	0x0040	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0044	W	0x00000000	Interrupt Enable Register
PWM_FIFO_CTRL	0x0050	W	0x00000000	PWM Channel 3 FIFO Mode Control Register
PWM_FIFO_INTSTS	0x0054	W	0x00000010	FIFO Interrupts Status Register
PWM_FIFO_TOUTTHR	0x0058	W	0x00000000	FIFO Timeout Threshold Register
PWM_VERSION_ID	0x005C	W	0x02120B34	PWM Version ID Register
PWM_FIFO	0x0060	W	0x00000000	FIFO Register
PWM_PWRMATCH_CTRL	0x0080	W	0x00000000	Power Key Match Control Register
PWM_PWRMATCH_LPRE	0x0084	W	0x238C22C4	Power Key Match Of Low Preload Register
PWM_PWRMATCH_HPRE	0x0088	W	0x11F81130	Power Key Match Of High Preload Register
PWM_PWRMATCH_LD	0x008C	W	0x029401CC	Power Key Match Of Low Data Register
PWM_PWRMATCH_HD_ZERO	0x0090	W	0x029401CC	Power Key Match Of High Data For Zero Register
PWM_PWRMATCH_HD_ONE	0x0094	W	0x06FE0636	Power Key Match Of High Data For One Register

Name	Offset	Size	Reset Value	Description
PWM_PWRMATCH_VALUE0	0x0098	W	0x00000000	Power Key Match Value 0 Register
PWM_PWRMATCH_VALUE1	0x009C	W	0x00000000	Power Key Match Value 1 Register
PWM_PWRMATCH_VALUE2	0x00A0	W	0x00000000	Power Key Match Value 2 Register
PWM_PWRMATCH_VALUE3	0x00A4	W	0x00000000	Power Key Match Value 3 Register
PWM_PWRMATCH_VALUE4	0x00A8	W	0x00000000	Power Key Match Value 4 Register
PWM_PWRMATCH_VALUE5	0x00AC	W	0x00000000	Power Key Match Value 5 Register
PWM_PWRMATCH_VALUE6	0x00B0	W	0x00000000	Power Key Match Value 6 Register
PWM_PWRMATCH_VALUE7	0x00B4	W	0x00000000	Power Key Match Value 7 Register
PWM_PWRMATCH_VALUE8	0x00B8	W	0x00000000	Power Key Match Value 8 Register
PWM_PWRMATCH_VALUE9	0x00BC	W	0x00000000	Power Key Match Value 9 Register
PWM_PWM3_PWRCAPTURE_VALUE	0x00CC	W	0x00000000	Channel 3 Power Key Capture Value Register
PWM_CHANNEL_IO_CTRL	0x00D0	W	0x00000000	Channel IO Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.2 Detail Registers Description

PWM_PWM0_CNT

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cnt The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_PERIOD_HPR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	period_hpr If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_DUTY_LPR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	duty_lpr If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM0_CTRL

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.
8	RW	0x0	force_clk_en 1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption. 1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock PWM period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM0_CTRL.rpt. 2'b01: Continuous mode. PWM produces the waveform continuously. 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM1_CNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cnt The 32-bit indicates current value of PWM Channel 1 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_PERIOD_HPR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	period_hpr If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_DUTY_LPR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	duty_lpr If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM1_CTRL

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RO	0x0	reserved
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.
8	RW	0x0	force_clk_en 1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption. 1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock PWM period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive

Bit	Attr	Reset Value	Description
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM1_CTRL.rpt. 2'b01: Continuous mode. PWM produces the waveform continuously. 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM2_CNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cnt The 32-bit indicates current value of PWM Channel 2 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_PERIOD_HPR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	period_hpr If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_DUTY_LPR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	duty_lpr If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM2_CTRL

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RO	0x0	reserved
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.
8	RW	0x0	force_clk_en 1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption. 1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled.

Bit	Attr	Reset Value	Description
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock PWM period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM2_CTRL.rpt. 2'b01: Continuous mode. PWM produces the waveform continuously. 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWM3_CNT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cnt The 32-bit indicates current value of PWM Channel 3 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_PERIOD_HPR

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	period_hpr If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_DUTY_LPR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	duty_lpr If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_PWM3_CTRL

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	clk_src_sel 1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed.
9	RW	0x0	clk_sel 1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source. 1'b1: Scaled clock is selected as PWM clock source.
8	RW	0x0	force_clk_en 1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption. 1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled.
7	RW	0x0	ch_cnt_en 1'b0: Disabled 1'b1: Enabled
6	RW	0x0	conlock PWM period and duty lock to previous configuration 1'b0: Disable lock 1'b1: Enable lock
5	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM3_CTRL.rpt. 2'b01: Continuous mode. PWM produces the waveform continuously. 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	pwm_en 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_INTSTS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	CH3_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM3_PERIOD_HPR to know the effective high cycle of Channel 3 input waveform. Otherwise, please refer to PWM3_PERIOD_LPR to know the effective low cycle of Channel 3 input waveform. Write 1 to CH3_IntSts will clear this bit.
10	RO	0x0	CH2_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM2_PERIOD_HPR to know the effective high cycle of Channel 2 input waveform. Otherwise, please refer to PWM2_PERIOD_LPR to know the effective low cycle of Channel 2 input waveform. Write 1 to CH2_IntSts will clear this bit.
9	RO	0x0	CH1_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM1_PERIOD_HPR to know the effective high cycle of Channel 1 input waveform. Otherwise, please refer to PWM1_PERIOD_LPR to know the effective low cycle of Channel 1 input waveform. Write 1 to CH1_IntSts will clear this bit.
8	RO	0x0	CH0_Pol This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM0_PERIOD_HPR to know the effective high cycle of Channel 0 input waveform. Otherwise, please refer to PWM0_PERIOD_LPR to know the effective low cycle of Channel 0 input waveform. Write 1 to CH0_IntSts will clear this bit.
7	W1C	0x0	CH3_pwr_IntSts 1'b0: Channel 3 power key Interrupt not generated 1'b1: Channel 3 power key Interrupt generated
6:4	RO	0x0	reserved
3	W1C	0x0	CH3_IntSts 1'b0: Channel 3 Interrupt not generated 1'b1: Channel 3 Interrupt generated

Bit	Attr	Reset Value	Description
2	W1C	0x0	CH2_IntSts 1'b0: Channel 2 Interrupt not generated 1'b1: Channel 2 Interrupt generated
1	W1C	0x0	CH1_IntSts 1'b0: Channel 1 Interrupt not generated 1'b1: Channel 1 Interrupt generated
0	W1C	0x0	CH0_IntSts 1'b0: Channel 0 Interrupt not generated 1'b1: Channel 0 Interrupt generated

PWM_INT_EN

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	CH3_pwr_Int_en 1'b0: Channel 3 power key Interrupt disabled 1'b1: Channel 3 power key Interrupt enabled
6:4	RO	0x0	reserved
3	RW	0x0	CH3_Int_en 1'b0: Channel 3 Interrupt disabled 1'b1: Channel 3 Interrupt enabled
2	RW	0x0	CH2_Int_en 1'b0: Channel 2 Interrupt disabled 1'b1: Channel 2 Interrupt enabled
1	RW	0x0	CH1_Int_en 1'b0: Channel 1 Interrupt disabled 1'b1: Channel 1 Interrupt enabled
0	RW	0x0	CH0_Int_en 1'b0: Channel 0 Interrupt disabled 1'b1: Channel 0 Interrupt enabled

PWM_FIFO_CTRL

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	dma_ch_sel 2'b00: Select PWM0 2'b01: Select PWM1 2'b10: Select PWM2 2'b11: Select PWM3
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	dma_ch_sel_en 1'b0: Disabled. Select the channel PWM3 to FIFO mode and DMA mode. 1'b1: Enabled. Use dma_ch_sel to select the channel to FIFO mode and DMA mode.
9	RW	0x0	timeout_en FIFO timeout enable.
8	RW	0x0	dma_mode_en 1'b1: Enabled 1'b0: Disabled
7	RO	0x0	reserved
6:4	RW	0x0	almost_full_watermark Almost full Watermark level.
3	RW	0x0	watermark_int_en Watermark full interrupt.
2	RW	0x0	overflow_int_en When high, an interrupt asserts when the FIFO overflow.
1	RW	0x0	full_int_en When high, an interrupt asserts when the FIFO is full.
0	RW	0x0	fifo_mode_sel When high, PWM FIFO mode is activated.

PWM_FIFO_INTSTS

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x1	fifo_empty_status This bit indicates the FIFO is empty.
3	W1C	0x0	timieout_intsts Timeout interrupt.
2	W1C	0x0	fifo_watermark_full_intsts This bit indicates the FIFO is Watermark full.
1	W1C	0x0	fifo_overflow_intsts This bit indicates the FIFO is overflow.
0	W1C	0x0	fifo_full_intsts This bit indicates the FIFO is full.

PWM_FIFO_TOUTTHR

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	timeout_threshold FIFO timeout value (Unit: pwm clock).

PWM_VERSION_ID

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RW	0x02	main_version Main version 8'h0:Base version 8'h1:Support DMA mode 8'h2:Support DMA mode and Power key mode
23:16	RW	0x13	minor_version Minor version
15:0	RW	0x11B6	svn_version SVN version

PWM_FIFO

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	pol This bit indicates the polarity of the lower 31-bit counter. 1'b0: Low 1'b1: High
30:0	RO	0x00000000	cycle_cnt This 31-bit counter indicates the effective cycles of high/low waveform.

PWM_PWRMATCH_CTRL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	CH3_pwrkey_int_ctrl 1'b0: Assert interrupt after key capture with power key match 1'b1: Assert interrupt after key capture without power key match
14:12	RO	0x0	reserved
11	RW	0x0	CH3_pwrkey_capture_ctrl 1'b0: Capture the value after interrupt 1'b1: Capture the value directly
10:8	RO	0x0	reserved
7	RW	0x0	CH3_pwrkey_polarity 1'b0: PWM in polarity is positive 1'b1: PWM in polarity is negative
6:4	RO	0x0	reserved
3	RW	0x0	CH3_pwrkey_enable 1'b0: Disabled 1'b1: Enabled
2:0	RO	0x0	reserved

PWM_PWRMATCH_LPRE

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x238c	cnt_max The maximum counter value.
15:0	RW	0x22c4	cnt_min The minimum counter value.

PWM_PWRMATCH_HPRE

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x11f8	cnt_max The maximum counter value.
15:0	RW	0x1130	cnt_min The minimum counter value.

PWM_PWRMATCH_LD

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value.
15:0	RW	0x01cc	cnt_min The minimum counter value.

PWM_PWRMATCH_HD_ZERO

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value.
15:0	RW	0x01cc	cnt_min The minimum counter value.

PWM_PWRMATCH_HD_ONE

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x06fe	cnt_max The maximum counter value.
15:0	RW	0x0636	cnt_min The minimum counter value.

PWM_PWRMATCH_VALUE0

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 0.

PWM_PWRMATCH_VALUE1

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 1.

PWM_PWRMATCH_VALUE2

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 2.

PWM_PWRMATCH_VALUE3

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 3.

PWM_PWRMATCH_VALUE4

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 4.

PWM_PWRMATCH_VALUE5

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 5.

PWM_PWRMATCH_VALUE6

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 6.

PWM_PWRMATCH_VALUE7

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 7.

PWM_PWRMATCH_VALUE8

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 8.

PWM_PWRMATCH_VALUE9

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value Power key match value 9.

PWM_PWM3_PWRCAPTURE_VALUE

Address: Operational Base + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwrkey_capture_value Power key capture value.

PWM_CHANNEL_IO_CTRL

Address: Operational Base + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	CH2_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
17	RW	0x0	CH1_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
16	RW	0x0	CH0_and_CH3_switch_en 1'b0: Disabled 1'b1: Enabled
15:13	RO	0x0	reserved
12:4	RW	0x000	filter_number Filter window number.
3	RW	0x0	CH3_input_filter_enable 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	CH2_input_filter_enable 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	CH1_input_filter_enable 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	CH0_input_filter_enable 1'b0: Disabled 1'b1: Enabled

15.5 Interface Description

Table 15-1 PWM Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
PWM0CH0	I/O	PWM0_M0/CPUAVS/GPIO0_B7_d	PMUGRF_GPIO0B_IOMUX_H[14:12]=3'b001

Module Pin	Dir.	Pin Name	IOMUX Setting
		HDMITX_CEC_M1/PWM0_M1/UART0_CTSn/GPIO0_C7_d	PMUGRF_GPIO0C_IOMUX_H[14:12]=3'b010
PWM0CH1	I/O	PWM1_M0/GPUAVS/UART0_RX/GPIO0_C0_d	PMUGRF_GPIO0C_IOMUX_L[2:0]=3'b001
		I2C2_SCL_M0/SPI0_CLK_M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	PMUGRF_GPIO0B_IOMUX_H[6:4]=3'b100
PWM0CH2	I/O	PWM2_M0/NPUAVS/UART0_TX/MCU_JTAG_TDI/GPIO0_C1_d	PMUGRF_GPIO0C_IOMUX_L[6:4]=3'b001
		I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	PMUGRF_GPIO0B_IOMUX_H[10:8]=3'b100
PWM0CH3	I/O	PWM3_IR/EDP_DP_HPDIN_M1/PCIE30X1_WAKEn_M0/MCU_JTAG_TMS/GPIO0_C2_d	PMUGRF_GPIO0C_IOMUX_L[2:0]=3'b001
PWM1CH0	I/O	PWM4/VOP_PWM_M0/PCIE30X1_PERSTn_M0/MCU_JTAG_TRSTn/GPIO0_C3_d	PMUGRF_GPIO0C_IOMUX_L[14:12]=3'b001
PWM1CH1	I/O	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	PMUGRF_GPIO0C_IOMUX_H[2:0]=3'b001
PWM1CH2	I/O	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	PMUGRF_GPIO0C_IOMUX_H[6:4]=3'b001
PWM1CH3	I/O	PWM7_IR/SPI0_CS0_M0/PCIE30X2_PERSTn_M0/GPIO0_C6_d	PMUGRF_GPIO0C_IOMUX_H[10:8]=3'b001
PWM2CH0	I/O	LCDC_D16/VOP_BT1120_D7/GMAC1_RXD0_M0/UART4_RX_M1/PWM8_M0/GPIO3_B1_d	GRF_GPIO3B_IOMUX_L[6:4]=3'b101
		SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	GRF_GPIO1D_IOMUX_H[6:4]=3'b100
PWM2CH1	I/O	LCDC_D17/VOP_BT1120_D8/GMAC1_RXD1_M0/UART4_TX_M1/PWM9_M0/GPIO3_B2_d	GRF_GPIO3B_IOMUX_L[10:8]=3'b101
		SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	GRF_GPIO1D_IOMUX_H[10:8]=3'b100
PWM2CH2	I/O	LCDC_D20/VOP_BT1120_D11/GMAC1_TXD0_M0/I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d	GRF_GPIO3B_IOMUX_H[6:4]=3'b101
		SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	GRF_GPIO2A_IOMUX_L[6:4]=3'b010
PWM2CH3	I/O	LCDC_D21/VOP_BT1120_D12/GMAC1_TXD1_M0/I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d	GRF_GPIO3B_IOMUX_H[10:8]=3'b101
		CIF_CLKOUT/EBC_GDCLK/PWM11_IR_M1/GPIO4_C0_d	GRF_GPIO4C_IOMUX_L[2:0]=3'b011

Module Pin	Dir.	Pin Name	IOMUX Setting
PWM3CH0	I/O	LCDC_D22/PWM12_M0/GMAC1_TXEN_M0/UART3_TX_M1/PDM_SDI2_M2/GPIO3_B7_d	GRF_GPIO3B_IOMUX_H[14:12]=3'b010
		PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	GRF_GPIO4C_IOMUX_H[6:4]=3'b001
PWM3CH1	I/O	LCDC_D23/PWM13_M0/GMAC1_MCLKINOUT_M0/UART3_RX_M1/PDM_SDI3_M2/GPIO3_C0_d	GRF_GPIO3C_IOMUX_L[2:0]=3'b010
		PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	GRF_GPIO4C_IOMUX_H[10:8]=3'b001
PWM3CH2	I/O	PWM14_M0/VOP_PWM_M1/GMAC1_MDC_M0/UART7_TX_M1/PDM_CLK1_M2/GPIO3_C4_d	GRF_GPIO3C_IOMUX_H[2:0]=3'b001
		PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	GRF_GPIO4C_IOMUX_L[10:8]=3'b001
PWM3CH3	I/O	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	GRF_GPIO3C_IOMUX_H[6:4]=3'b101
		PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	GRF_GPIO4C_IOMUX_L[14:12]=3'b001

Notes: Unused Module Pin is tied to zero! I=input, O=output, I/O=input/output, bidirectional

15.6 Application Notes

15.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel and PWM_PWMx_CTRL.clk_src_sel.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation.
5. Set PWM_CHANNEL_IO_CTRL. filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CHx_input_filter_enable(Optional).
6. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
7. When an interrupt is asserted, refer to INTSTS register to know the raw interrupt status. If the corresponding polarity flag is set, turn to PWM_PWMx_PERIOD_HPC register to know the effective high cycles of input waveforms, otherwise turn to PWM_PWMx_DUTY_LPC register to know the effective low cycles.
8. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

15.6.2 PWM Capture DMA Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel and PWM_PWMx_CTRL.clk_src_sel.
3. Configure the channel 3 to work in the capture mode.
4. Configure the PWM_FIFO_CTRL.dma_mode_en and PWM_FIFO_CTRL.fifo_mode_sel to enable the DMA mode. Configure PWM_FIFO_CTRL.almost_full_watermark at appropriate value.
5. Configure DMAC_BUS to transfer data from PWM to DDR.
6. Set PWM_CHANNEL_IO_CTRL.filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CHx_input_filter_enable(Optional).
7. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
8. When a dma_req is asserted, DMAC_BUS transfer the data of effective high cycles and low cycles of input waveforms to DDR.
9. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

15.6.3 PWM Power key Capture Mode Standard Usage Flow

1. Set PWM_PWM3_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWM3_CTRL.prescale and PWM_PWM3_CTRL.scale, and select the clock needed by setting PWM_PWM3_CTRL.clk_sel. The clock should be 1 MHz after division.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.CH3_int_pwr to enable the interrupt generation.
5. Set the PWM_PWRMATCH_VALUE0~9 registers for the 10 power key match value.
6. Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers when the default value can meet the requirement.
7.Set PWM_PWRMATCH_CTRL.CH3_pwrkey_polarity for the polarity of power key signal, the default value is 0. Enable the PWM_PWRMATCH_CTRL.CH3_pwrkey_enable.
8. Set PWM_CHANNEL_IO_CTRL.filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CH3_input_filter_enable(Optional).
9. Enable the channel by writing '1' to PWM_PWM3_CTRL.pwm_en bit to start the channel.
10. Poll INTSTS. CH3_pwr_IntSts ==1, and refer to PWM_PWM3_PWRCAPTURE_VALUE to know the power key capture value.
11. Write '0' to PWM_PWM3_CTRL.pwm_en to disable the channel.

15.6.4 PWM One-shot Mode/Continuous Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for pclk by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
3. Choose the output mode by setting PWM_PWMx_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_PWMx_CTRL.duty_pol and PWM_PWMx_CTRL.inactive_pol.
4. Set the PWM_PWMx_CTRL.rpt if the channel is desired to work in the one-shot mode.
5. Configure the channel to work in the one-shot mode or the continuous mode.
6. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation if the channel is desired to work in the one-shot mode.
7. If the channel is working in the one-shot mode, an interrupt is asserted after the end of operation, and the PWM_PWMx_CTRL.pwm_en is automatically cleared. Whatever mode the channel is working in, write '0' to PWM_PWMx_CTRL.pwm_en bit to disable the PWM channel.

15.6.5 Low-power Usage Flow

The default value of PWM_PWMx_CTRL.force_clk_en is '0' which make the channel enter the low-power mode. In low-power mode, When the PWM channel is inactive, the clk_pwm to the clock prescale module is gated in order to reduce the power consumption. User can set PWM_PWMx_CTRL.force_clk_en to '1' which will make the channel quit the low-power mode. After the setting, the clk_pwm to the clock prescale module is always enable.

15.6.6 Other notes

When the channel is active to produce waveforms, it is free to program the PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC register. User can use PWM_PWMx_CTRL.conlock to take period and duty effect at the same time. The usage flow is as follow:

1. Set PWM_PWMx_CTRL.conlock to '1'.
2. Set PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC.
3. Set PWM_PWMx_CTRL.conlock to '0', others bits in PWM_PWMx_CTRL should be appropriate.

After above configuration, the change will not take effect immediately until the current period ends.

An active channel can be changed to another operation mode without disable the PWM channel. However, during the transition of the operation mode there may be some irregular output waveforms. So does changing the clock division factor when the channel is active.

Chapter 16 GPIO

16.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode

16.2 Block Diagram

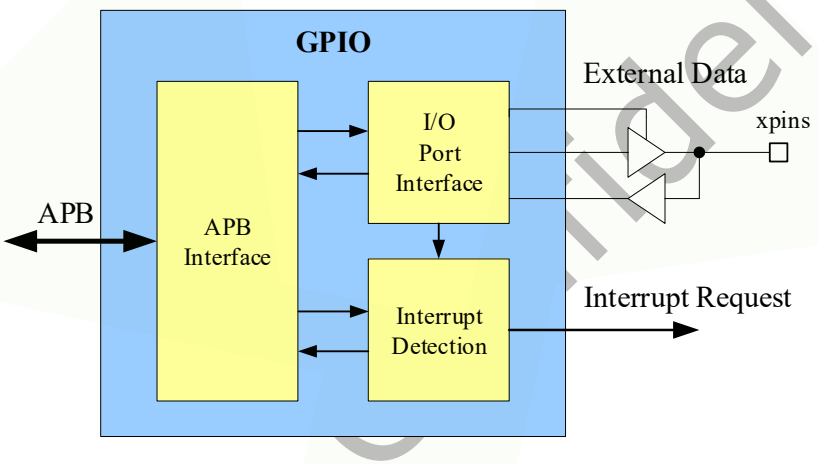


Fig. 16-1 GPIO Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection

Interrupt interface to or from interrupt controller.

16.3 Function Description

16.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H).
The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input.
The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.
External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

16.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

16.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of two cycles of the debounce clock to guarantee that it is registered. Any input pulse widths less than a debounce clock period are bounced. A pulse width between one and two debounce clock widths may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

16.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses. There are five GPIOs (GPIO0 in PD_PMU, GPIO1/GPIO2/GPIO3/GPIO4 in PD_BUS), and each of them has same register group. Therefore, five GPIOs' register groups have five different base addresses.

16.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DDR_H	0x000C	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable Register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001C	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002C	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003C	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_VER_ID	0x0078	W	0x0101157C	Version ID Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.4.2 Detail Registers Description

GPIO_SWPORT_DR_L

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_low Output data for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_high Output data for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_low Data direction for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port.

GPIO_SWPORT_DDR_H

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_high Data direction for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port.

GPIO_INT_EN_L

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_EN_H

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_MASK_L

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_MASK_H

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_TYPE_L

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_TYPE_H

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_POLARITY_L

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_POLARITY_H

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_BOTHEDGE_L

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers.

GPIO_INT_BOTHEDGE_H

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers.

GPIO_DEBOUNCE_L

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DEBOUNCE_H

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DBCLK_DIV_EN_L

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0.

GPIO_DBCLK_DIV_EN_H

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0.

GPIO_DBCLK_DIV_CON

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000001	dbclk_div_con dbclk_div = dbclk / (dbclk_div_con + 1)

GPIO_INT_STATUS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_status Interrupt status of I/O Port.

GPIO_INT_RAWSTATUS

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_rawstatus Interrupt raw status of I/O Port (premasking bits).

GPIO_PORT_EOI_L

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/W SC	0x0000	port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_PORT_EOI_H

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/W SC	0x0000	port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_EXT_PORT

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_VER_ID

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x0101157c	ver_id Version ID.

16.5 Interface Description

Table 16-1 GPIO Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
GPIO0 Interface			
gpio0_port[3:0]	I/O	GPIO0_A[3:0]	PMUGRF_GPIO0A_IOMUX_L[15:0]=16'h0
gpio0_port[7:4]	I/O	GPIO0_A[7:4]	PMUGRF_GPIO0A_IOMUX_H[15:0]=16'h0
gpio0_port[11:8]	I/O	GPIO0_B[3:0]	PMUGRF_GPIO0B_IOMUX_L[15:0]=16'h0
gpio0_port[15:12]	I/O	GPIO0_B[7:4]	PMUGRF_GPIO0B_IOMUX_H[15:0]=16'h0
gpio0_port[19:16]	I/O	GPIO0_C[3:0]	PMUGRF_GPIO0C_IOMUX_L[15:0]=16'h0
gpio0_port[23:20]	I/O	GPIO0_C[7:4]	PMUGRF_GPIO0C_IOMUX_H[15:0]=16'h0
gpio0_port[27:24]	I/O	GPIO0_D[3:0]	PMUGRF_GPIO0D_IOMUX_L[15:0]=16'h0
gpio0_port[31:28]	I/O	GPIO0_D[7:4]	PMUGRF_GPIO0D_IOMUX_H[15:0]=16'h0
GPIO1 Interface			
gpio1_port[3:0]	I/O	GPIO1_A[3:0]	GRF_GPIO1A_IOMUX_L[15:0]=16'h0
gpio1_port[7:4]	I/O	GPIO1_A[7:4]	GRF_GPIO1A_IOMUX_H[15:0]=16'h0
gpio1_port[11:8]	I/O	GPIO1_B[3:0]	GRF_GPIO1B_IOMUX_L[15:0]=16'h0
gpio1_port[15:12]	I/O	GPIO1_B[7:4]	GRF_GPIO1B_IOMUX_H[15:0]=16'h0
gpio1_port[19:16]	I/O	GPIO1_C[3:0]	GRF_GPIO1C_IOMUX_L[15:0]=16'h0
gpio1_port[23:20]	I/O	GPIO1_C[7:4]	GRF_GPIO1C_IOMUX_H[15:0]=16'h0
gpio1_port[27:24]	I/O	GPIO1_D[3:0]	GRF_GPIO1D_IOMUX_L[15:0]=16'h0
gpio1_port[31:28]	I/O	GPIO1_D[7:4]	GRF_GPIO1D_IOMUX_H[15:0]=16'h0
GPIO2 Interface			
gpio2_port[3:0]	I/O	GPIO2_A[3:0]	GRF_GPIO2A_IOMUX_L[15:0]=16'h0
gpio2_port[7:4]	I/O	GPIO2_A[7:4]	GRF_GPIO2A_IOMUX_H[15:0]=16'h0
gpio2_port[11:8]	I/O	GPIO2_B[3:0]	GRF_GPIO2B_IOMUX_L[15:0]=16'h0
gpio2_port[15:12]	I/O	GPIO2_B[7:4]	GRF_GPIO2B_IOMUX_H[15:0]=16'h0
gpio2_port[19:16]	I/O	GPIO2_C[3:0]	GRF_GPIO2C_IOMUX_L[15:0]=16'h0
gpio2_port[23:20]	I/O	GPIO2_C[7:4]	GRF_GPIO2C_IOMUX_H[15:0]=16'h0
gpio2_port[27:24]	I/O	GPIO2_D[3:0]	GRF_GPIO2D_IOMUX_L[15:0]=16'h0
gpio2_port[31:28]	I/O	GPIO2_D[7:4]	GRF_GPIO2D_IOMUX_H[15:0]=16'h0
GPIO3 Interface			
gpio3_port[3:0]	I/O	GPIO3_A[3:0]	GRF_GPIO3A_IOMUX_L[15:0]=16'h0
gpio3_port[7:4]	I/O	GPIO3_A[7:4]	GRF_GPIO3A_IOMUX_H[15:0]=16'h0
gpio3_port[11:8]	I/O	GPIO3_B[3:0]	GRF_GPIO3B_IOMUX_L[15:0]=16'h0
gpio3_port[15:12]	I/O	GPIO3_B[7:4]	GRF_GPIO3B_IOMUX_H[15:0]=16'h0
gpio3_port[19:16]	I/O	GPIO3_C[3:0]	GRF_GPIO3C_IOMUX_L[15:0]=16'h0
gpio3_port[23:20]	I/O	GPIO3_C[7:4]	GRF_GPIO3C_IOMUX_H[15:0]=16'h0
gpio3_port[27:24]	I/O	GPIO3_D[3:0]	GRF_GPIO3D_IOMUX_L[15:0]=16'h0
gpio3_port[31:28]	I/O	GPIO3_D[7:4]	GRF_GPIO3D_IOMUX_H[15:0]=16'h0
GPIO4 Interface			
gpio4_port[3:0]	I/O	GPIO4_A[3:0]	GRF_GPIO4A_IOMUX_L[15:0]=16'h0
gpio4_port[7:4]	I/O	GPIO4_A[7:4]	GRF_GPIO4A_IOMUX_H[15:0]=16'h0
gpio4_port[11:8]	I/O	GPIO4_B[3:0]	GRF_GPIO4B_IOMUX_L[15:0]=16'h0
gpio4_port[15:12]	I/O	GPIO4_B[7:4]	GRF_GPIO4B_IOMUX_H[15:0]=16'h0
gpio4_port[19:16]	I/O	GPIO4_C[3:0]	GRF_GPIO4C_IOMUX_L[15:0]=16'h0
gpio4_port[23:20]	I/O	GPIO4_C[7:4]	GRF_GPIO4C_IOMUX_H[15:0]=16'h0
gpio4_port[27:24]	I/O	GPIO4_D[3:0]	GRF_GPIO4D_IOMUX_L[15:0]=16'h0
gpio4_port[31:28]	I/O	GPIO4_D[7:4]	GRF_GPIO4D_IOMUX_H[15:0]=16'h0

Notes: Unused Module Pin is tied to zero! I=input, O=output, I/O=input/output, bidirectional

16.6 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

Chapter 17 SAR-ADC

17.1 Overview

The ADC is a 6-channel signal-ended 10-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as it reference which avoid use of any external reference. It converts the analog input signal into 10-bit binary digital codes at maximum conversion rate of 1MSPS with 12MHz A/D converter clock.

17.2 Block Diagram

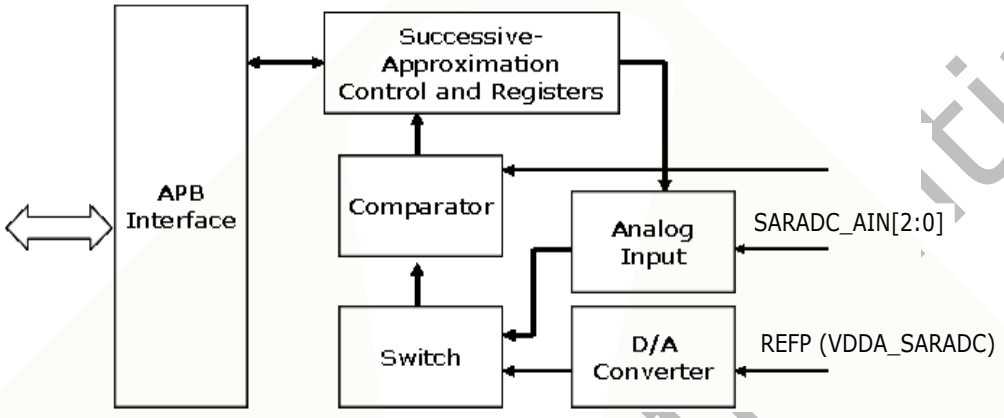


Fig. 17-1 SAR-ADC Block Diagram

Successive-Approximate Register and Control Logic Block
This block is exploited to realize binary search algorithm, storing the intermediate result and generate control signal for analog block.
Comparator Block
This block compares the analog input SARADC_AIN[2:0] with the voltage generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

17.3 Function Description

In RK3568, SAR-ADC works at single-sample operation mode.
This mode is useful to sample an analog input when there is a gap between two samples to be converted. In this mode START is asserted only on the rising edge of CLKIN where conversion is needed. At the end of every conversion EOC signal is made high and valid output data is available at the rising edge of EOC. The detailed timing diagram will be shown in the following.

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_DATA	0x0000	W	0x00000000	this register contains the data after A/D Conversion
SARADC_STAS	0x0004	W	0x00000000	the status register of A/D Converter
SARADC_CTRL	0x0008	W	0x00000000	the control register of A/D Converter

Name	Offset	Size	Reset Value	Description
SARADC_DLY_PU_SOC	0x000C	W	0x00000008	delay between power up and start command

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

SARADC_DATA

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	adc_data A/D value of the last conversion (DOUT[9:0]).

SARADC_STAS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	adc_status ADC status (EOC). 1'b0: ADC stop 1'b1: Conversion in progress

SARADC_CTRL

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	int_status Interrupt status. This bit will be set to 1 when end-of-conversion. Set 0 to clear the interrupt.
5	RW	0x0	int_en Interrupt enable. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3	RW	0x0	adc_power_ctrl ADC power down control bit. 1'b0: ADC power down 1'b1: ADC power up and reset Start signal will be asserted (DLY_PU_SOC + 2) sclk clock period later after power up.
2:0	RW	0x0	adc_input_src_sel ADC input source selection(CH_SEL[2:0]). 3'b000: Input source 0 (SARADC_AIN[0]) 3'b001: Input source 1 (SARADC_AIN[1]) 3'b010: Input source 2 (SARADC_AIN[2]) 3'b011: Input source 3 (SARADC_AIN[3]) 3'b100: Input source 4 (SARADC_AIN[4]) 3'b101: Input source 5 (SARADC_AIN[5]) Others : Reserved

SARADC_DLY_PU_SOC

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x08	dly_pu_soc Delay between power up and start command. The start signal will be asserted (dly_pu_soc + 2) sclk clock period later after power up.

17.5 Timing Diagram

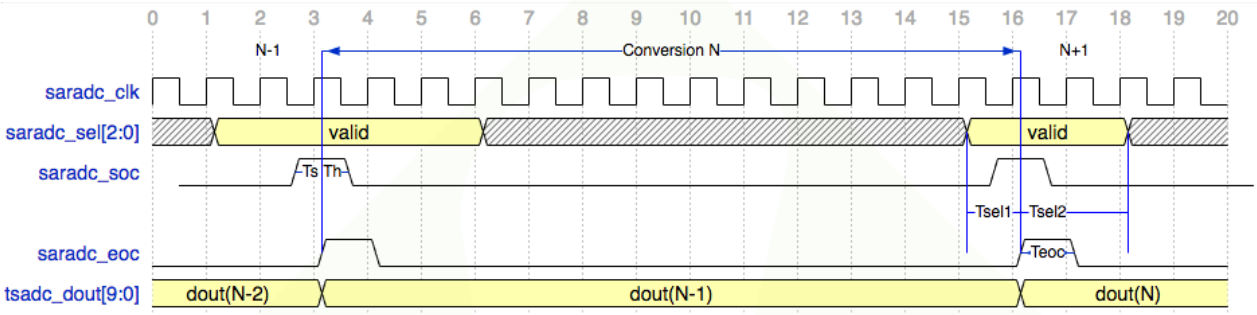


Fig. 17-2 SAR-ADC Timing Diagram in Single-sample Conversion Mode

The following table shows the detail value for timing parameters in the above diagram.

Table 17-1 SAR-ADC Timing Parameters List

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Timing Characteristic						
Clock Frequency	fCLK				26	MHz
Clock Period	tCLK		38			ns
Conversion Time			13			tCLK
Setup Time of soc signal	T_s		0.2		0.5	ns
Hold Time of soc signal	T_h		0.2		0.5	ns
High Level Time of eoc signal	T_{eoc}			1		tCLK
Time Interval between Transition of sel[2:0] and Rising Edge of 1st clock	t_{sel1}			1		tCLK
Time Interval between Transition of sel[2:0] and Rising Edge of 1st clock	t_{sel2}			2		tCLK

17.6 Application Notes

Steps of adc conversion:

- Write SARADC_CTRL[3] as 0 to power down ADC converter.
- Write SARADC_CTRL[2:0] as n to select ADC channel(n).
- Write SARADC_CTRL[5] as 1 to enable ADC interrupt.
- Write SARADC_CTRL[3] as 1 to power up ADC converter.
- Wait for ADC interrupt or poll SARADC_STAS register to assert whether the conversion is completed.
- Read the conversion result from SARADC_DATA[9:0].
- Note: The A/D converter was designed to operate at maximum 1MHz.

Chapter 18 Temperature-Sensor ADC (TS-ADC)

18.1 Overview

TS-ADC Controller module supports user-defined mode and automatic mode. User-defined mode refers, TSADC all the control signals entirely by software writing to register for direct control. Automatic mode refers to the module automatically poll TSADC output, and the results were checked. If you find that the temperature High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC.

TS-ADC Controller supports the following features:

- Support User-Defined Mode and Automatic Mode
- In User-Defined Mode, start-of-conversion can be controlled completely by software, and also can be generated by hardware
- In Automatic Mode, the temperature of alarm(high/low temperature) interrupt can be configurable
- In Automatic Mode, the temperature of system reset can be configurable
- Support to 2 channel TS-ADC(CPU and GPU), the temperature criteria of each channel can be configurable
- In Automatic Mode, the time interval of temperature detection can be configurable
- In Automatic Mode, when detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable
- -40~125°C temperature range and 5°C temperature resolution
- 12-bit SARADC up to 732 S/s sampling rate

18.2 Block Diagram

TS-ADC controller comprises with:

- APB Interface
- TS-ADC control logic

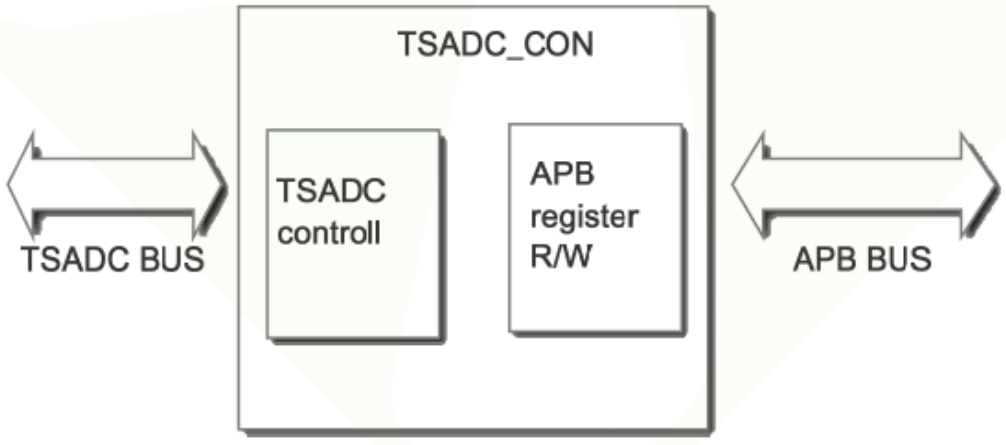


Fig.18-1 TS-ADC Controller Block Diagram

18.3 Function Description

18.3.1 AHB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

18.3.2 TS-ADC Controller

This block is exploited to realize binary search algorithm, storing the intermediate result and

generate control signal for analog block.This block compares the analog input with the voltage generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000200	the control register of A/D converter
TSADC_AUTO_CON	0x0004	W	0x00000000	TSADC auto mode control register
TSADC_INT_EN	0x0008	W	0x00000000	TSADC interrupts enable control
TSADC_INT_PD	0x000C	W	0x00000000	TSADC interrupts status
TSADC_DATA0	0x0020	W	0x00000000	this register contains the data from CH0 after A/D conversion
TSADC_DATA1	0x0024	W	0x00000000	this register contains the data from CH1 after A/D conversion
TSADC_COMP0_INT	0x0030	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_INT	0x0034	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP0_SHUT	0x0040	W	0x00000000	TSADC highshut temperature level for source 0
TSADC_COMP1_SHUT	0x0044	W	0x00000000	TSADC highshut temperature level for source 1
TSADC_HIGHT_INT_DEBOUNCE	0x0060	W	0x00000003	high temperature debounce
TSADC_HIGHT_TSHUT_DEBOUNCE	0x0064	W	0x00000003	shut temperature debounce
TSADC_AUTO_PERIOD	0x0068	W	0x00010000	TSADC auto access period
TSADC_AUTO_PERIOD_HT	0x006C	W	0x00010000	TSADC auto access period when temperature is high
TSADC_COMP0_LOW_INT	0x0080	W	0x00000000	TSADC low temperature level for source 0
TSADC_COMP1_LOW_INT	0x0084	W	0x00000000	TSADC low temperature level for source 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 Detail Registers Description

TSADC_USER_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adc_status 1'b0: ADC stop 1'b1: Conversion in progress
14:6	RW	0x008	inter_pd_soc Interleave between power down and start of conversion.

Bit	Attr	Reset Value	Description
5	RW	0x0	start When software write 1 to this bit , start_of_conversion will be assert. This bit will be cleared after TSADC access finishing. When TSADC_USER_CON[4] = 1'b1 take effect.
4	RW	0x0	start_mode Start mode. 1'b0: Tsadc controller will asert start_of_conversion after "inter_pd_soc" cycles 1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[5]
3	RW	0x0	adc_power_ctrl 1'b0: ADC power down 1'b1: ADC power up and reset
2:0	RW	0x0	adc_input_src_sel 3'b000: Input source 0 (SARADC_AIN[0]) 3'b001: Input source 1 (SARADC_AIN[1]) Others: Reserved

TSADC_AUTO_CON

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	last_tshut_2cru TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
24	RW	0x0	last_tshut_2gpio TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
23:18	RO	0x00	reserved
17	RW	0x0	sample_dly_sel 1'b0: AUTO_PERIOD is used 1'b1: AUTO_PERIOD_HT is used
16	RW	0x0	auto_status 1'b0: Auto mode stop 1'b1: Auto mode in progress
15:14	RO	0x0	reserved
13	RW	0x0	src1_lt_en 1'b0: Do not care low temperature of source 0 1'b1: Enable the low temperature monitor of source 0
12	RW	0x0	src0_lt_en 1'b0: Do not care low temperature of source 0 1'b1: Enable the low temperature monitor of source 0
11:9	RO	0x0	reserved
8	RW	0x0	tshut_prolarity 1'b0: Low active 1'b1: High active
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	src1_en 1'b0: Do not care the temperature of source 1 1'b1: If the temperature of source 0 is too high , TSHUT will be valid
4	RW	0x0	src0_en 1'b0: Do not care the temperature of source 0 1'b1: If the temperature of source 0 is too high , TSHUT will be valid
3:2	RO	0x0	reserved
1	RW	0x0	tsadc_q_sel 1'b0: Use tsadc_q as output(positive temperature coefficient) 1'b1: Use(4096- tsadc_q) as output (negative temperature coefficient) RK3399 is negative temprature coefficient, so please set this bit as 1'b1
0	RW	0x0	auto_en 1'b0: TSADC controller works at user-define mode 1'b1: TSADC controller works at auto mode

TSADC_INT_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	eoc_int_en Eoc_interrupt enable in user defined mode 1'b0: Disable 1'b1: Enable
15:14	RO	0x0	reserved
13	RW	0x0	lt_inten_src1 Low temperature interrupt enable for src1. 1'b0: Disable 1'b1: Enable
12	RW	0x0	lt_inten_src0 Low temperature interrupt enable for src0. 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	tshut_2cru_en_src1 1'b0: TSHUT output to cru disabled. TSHUT output will always keep low 1'b1: TSHUT output works
8	RW	0x0	tshut_2cru_en_src0 1'b0: TSHUT output to cru disabled. TSHUT output will always keep low 1'b1: TSHUT output works
7:6	RO	0x0	reserved
5	RW	0x0	tshut_2gpio_en_src1 1'b0: TSHUT output to gpio disabled. TSHUT output will always keep low 1'b1: TSHUT output works
4	RW	0x0	tshut_2gpio_en_src0 1'b0: TSHUT output to gpio disabled. TSHUT output will always keep low 1'b1: TSHUT output works
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	ht_inten_src1 High temperature interrupt enable for src1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ht_inten_src0 High temperature interrupt enable for src0. 1'b0: Disable 1'b1: Enable

TSADC_INT_PD

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	eoc_int_pd This bit will be set to 1 when end-of-conversion. Set 0 to clear the interrupt.
15:14	RO	0x0	reserved
13	RW	0x0	lt_irq_src1 When TSADC output is lower than COMP_INT_LOW, this bit will be valid, which means temperature is low, and the application should in charge of this. write 1 to it , this bit will be cleared.
12	RW	0x0	lt_irq_src0 When TSADC output is lower than COMP_INT_LOW, this bit will be valid, which means temperature is low, and the application should in charge of this. write 1 to it , this bit will be cleared.
11:6	RO	0x00	reserved
5	RW	0x0	tshut_o_src1 TSHUT output status When TSADC output is bigger than COMP_SHUT, this bit will be valid, which means temperature is VERY high, and the application should in charge of this. write 1 to it , this bit will be cleared.
4	RW	0x0	tshut_o_src0 TSHUT output status When TSADC output is bigger than COMP_SHUT, this bit will be valid, which means temperature is VERY high, and the application should in charge of this. write 1 to it , this bit will be cleared.
3:2	RO	0x0	reserved
1	RW	0x0	ht_irq_src1 When TSADC output is bigger than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
0	RW	0x0	ht_irq_src0 When TSADC output is bigger than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.

TSADC_DATA0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	adc_data Adc data. A/D value of the channel 0 last conversion (DOUT[11:0])

TSADC_DATA1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	adc_data Adc data. A/D value of the channel 1 last conversion (DOUT[11:0])

TSADC_COMP0_INT

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGHT_INT_DEBOUNCE

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times.

TSADC_HIGHT_TSHUT_DEBOUNCE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period When auto mode is enabled, this register controls the interleave between every two accessing of TSADC.

TSADC_AUTO_PERIOD_HT

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

TSADC_COMP0_LOW_INT

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP1_LOW_INT

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

18.5 Application Notes

18.5.1 Channel Select

The system has two Temperature Sensors, channel 0 is for CPU and channel 1 is for GPU.

18.5.2 Single-Sample Conversion

To start the temperature sensor, the bandgap circuit, the related voltage buffers and ADC should be enabled successively

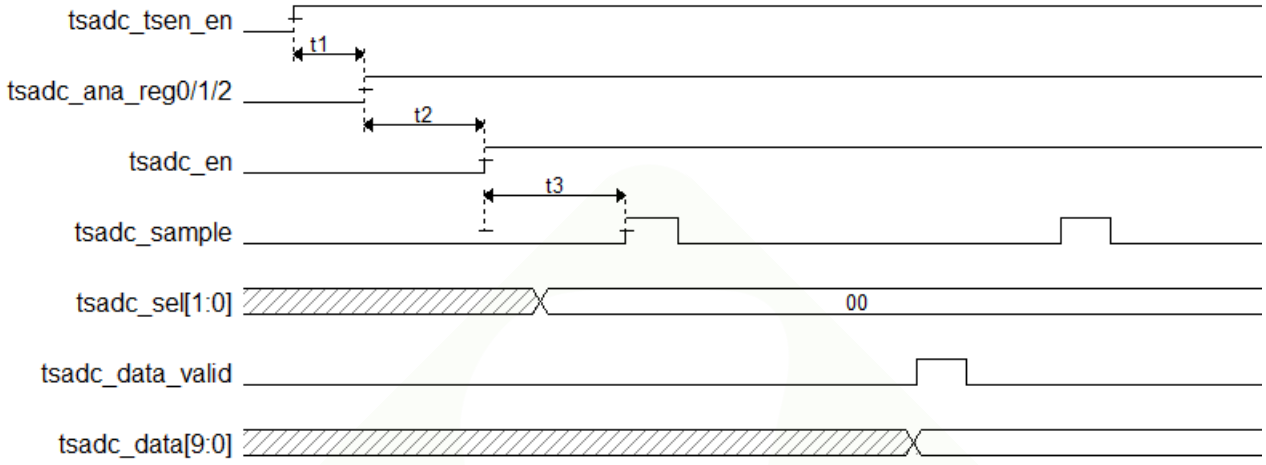


Fig. 18-2 Start Flow to Enable the Sensor and ADC

Table 1-1 gives requirement for start timing. t1 is the time interval between the rising edge of tsadc_tsen_en and the rising edge of tsadc_ana_reg_0/1/2, which should be no less than 10us. t2 is the time interval between the rising edge of tsadc_ana_reg_0/1/2 and the rising edge of tsadc_en. t3 is time interval between the rising edge of tsadc_en and the rising edge of tsadc_sample, which should be no less than 90us

Table 18-1 Start Timing Specification

Parameter	Min	Typ	Max
t1	10us		
t2	0us		
t3	90us		

18.5.3 Temperature-to-Code Mapping

Table 18-2 Temperature Code Mapping

Temperature (℃)	Temperature Sensor Output		
	Min	Typ	Max
-40	-	2512	-
-35	-	2476	-
-30	-	2444	-
-25	-	2408	-
-20	-	2376	-
-15	-	2340	-
-10	-	2308	-
-5	-	2272	-
0	-	2240	-
5	-	2204	-
10	-	2172	-
15	-	2140	-

Temperature (℃)	Temperature Sensor Output		
	Min	Typ	Max
20	-	2104	-
25	-	2072	-
30	-	2036	-
35	-	2004	-
40	-	1968	-
45	-	1936	-
50	-	1900	-
55	-	1868	-
60	-	1832	-
65	-	1796	-
70	-	1764	-
75	-	1728	-
80	-	1696	-
85	-	1660	-
90	-	1628	-
95	-	1596	-
100	-	1560	-
105	-	1524	-
110	-	1492	-
115	-	1460	-
120	-	1424	-
125	-	1392	-

18.5.4 User-Define Mode

- In user-define mode, the PD_DVDD and CHSEL_DVDD are generate by setting register TSADC_USER_CON, bit[3] and bit[2:0]. In order to ensure timing between PD_DVDD and CHSEL_DVDD, the CHSEL_DVDD must be set before the PD_DVDD.
- In user-define mode, you can choose the method to control the START_OF_CONVERSION by setting bit[4] of TSADC_USER_CON. If set to 0, the start_of_conversion will be assert after "inter_pd_soc" cycles, which could be set by bit[11:6] of TSADC_USER_CON. And if start_mode was set 1, the start_of_conversion will be controlled by bit[5] of TSADC_USER_CON.
- Software can get the four channel temperature from TSADC_DATAn (n=0,1,2,3).

18.5.5 Automatic Mode

You can use the automatic mode with the following step:

- Set TSADC_AUTO_PERIOD to configure the interleave between every two accessing of TSADC in normal operation.
- Set TSADC_AUTO_PERIOD_HT to configure the interleave between every two accessing

of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

- Set TSADC_COMPn_INT(n=0,1) to configure the high temperature level, if tsadc output is smaller than the value, means the temperature is high, tsadc_int will be asserted.
- Set TSADC_COMPn_SHUT(n=0,1) to configure the super high temperature level, if tsadc output is smaller than the value, means the temperature is too high, TSHUT will be asserted.
- Set TSADC_INT_EN to enable the high temperature interrupt for all channel; and you can also set TSHUT output to GPIO to reset the whole chip; and you can set TSHUT output to cru to reset the whole chip.
- Set TSADC_HIGHT_INT_DEBOUNCE and TSADC_HIGHT_TSHUT_DEBOUNCE, if the temperature is higher than COMP_INT or COMP_SHUT for "debounce" times, TSADC controller will generate interrupt or TSHUT.
    - Set TSADC_AUTO_CON to enable the TSADC controller.

Chapter 19 Pulse Density Modulation Interface Controller

19.1 Overview

The PDM interface controller and decoder support mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
PDM supports the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels. It can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16~24 bit sample resolution
- Support sample rate: 8kHz,16kHz,32kHz,64kHz,128kHz,11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz,12kHz,24kHz,48kHz,96kHz,192kHz
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support programmable left and right channel exchange

19.2 Block Diagram

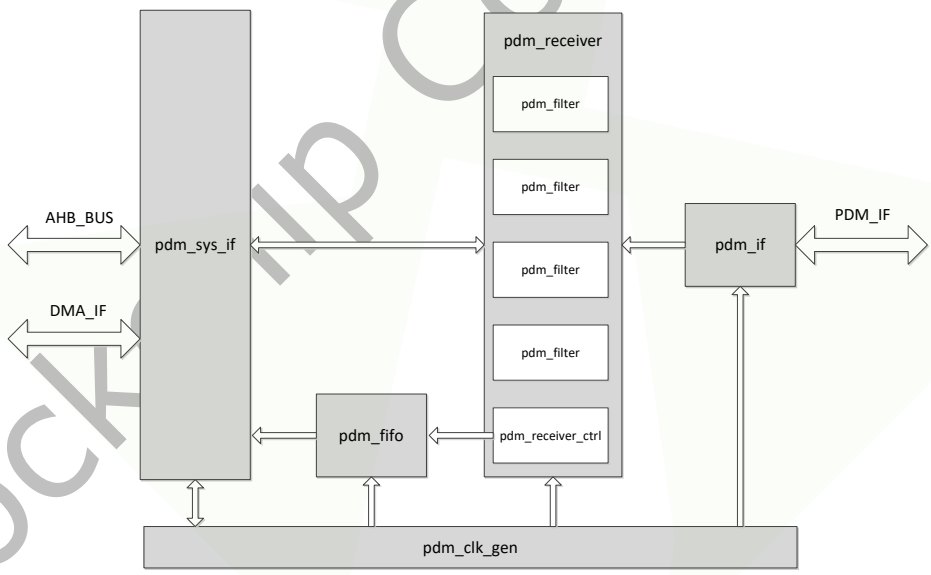


Fig.19-1 PDM Block Diagram

System Interface
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK, and by the divider of the module, the clock generator generates CLK_PDM to receiver.
Receiver
The receiver can act as a decimation filter of PDM. And export PCM format data.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x

128.

19.3 Function Description

19.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers.

19.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

Following shows two cases of usage of the PDM, but all configurations are possible with stereo and mono digital microphones.

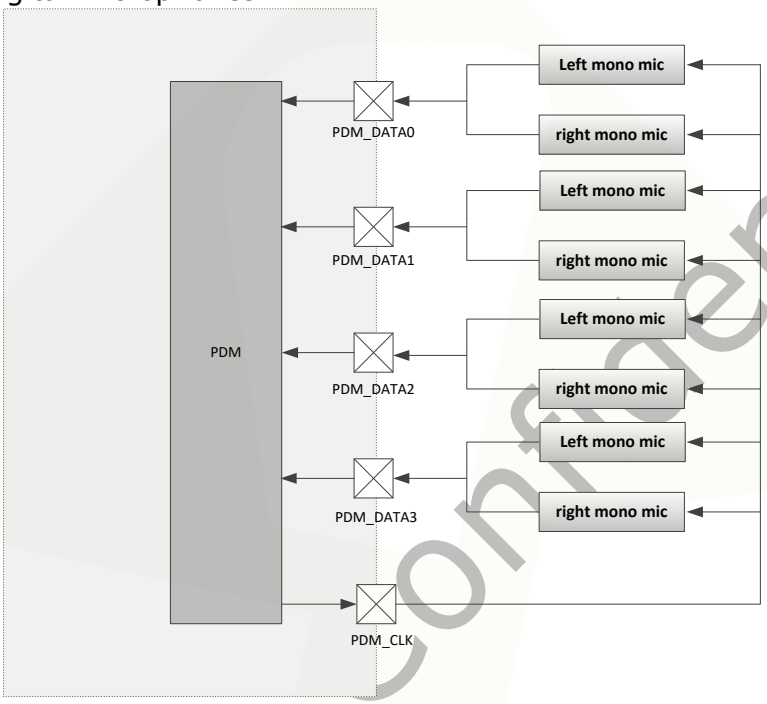


Fig.19-2 PDM with Eight Mono MIC

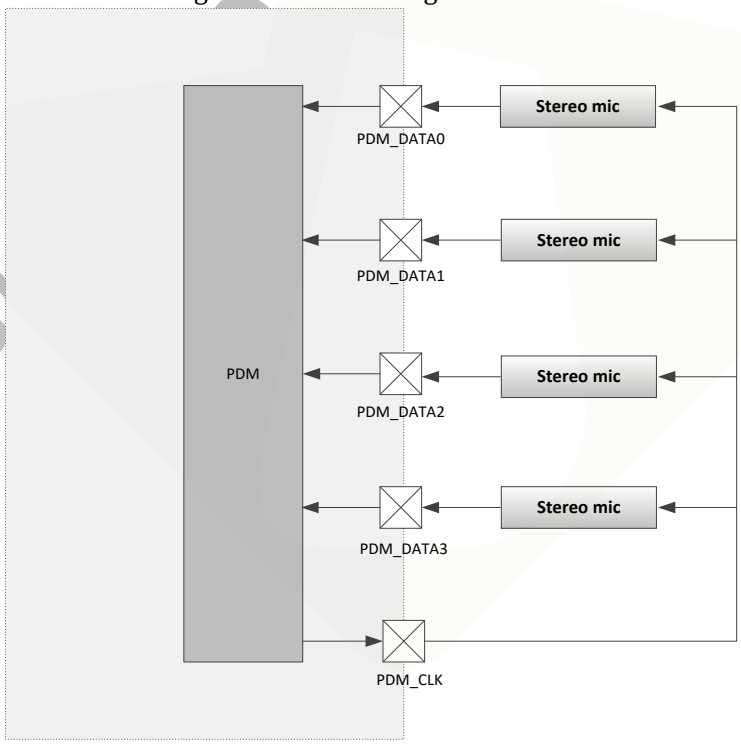


Fig.19-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital MICs, and both digital MICs'

data(left channel and right channel) outputs share a single signal line. To share a single line, the digital MICs tri-state their output during one phase of the clock(high or low part of cycle, depending on how they are configured via their L/R input).

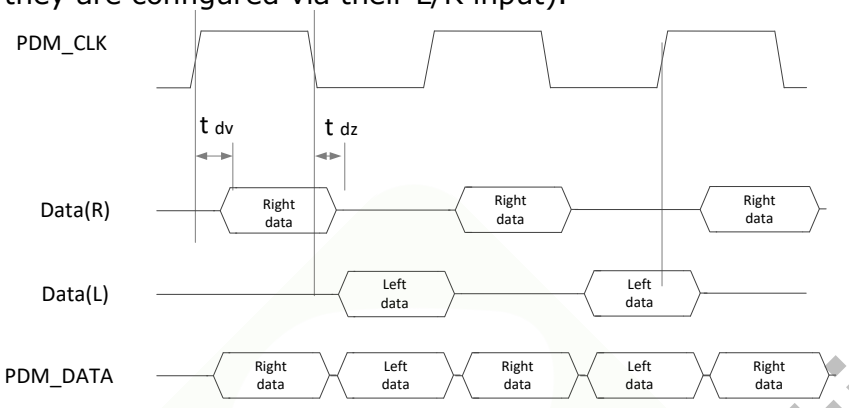


Fig.19-4 PDM interface diagram with external MIC

19.3.3 Digital Filter

The external PDM MIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO.
The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

19.3.4 Frequency Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the frequency of PDM_CLK when selecting the source clock (MCLK).

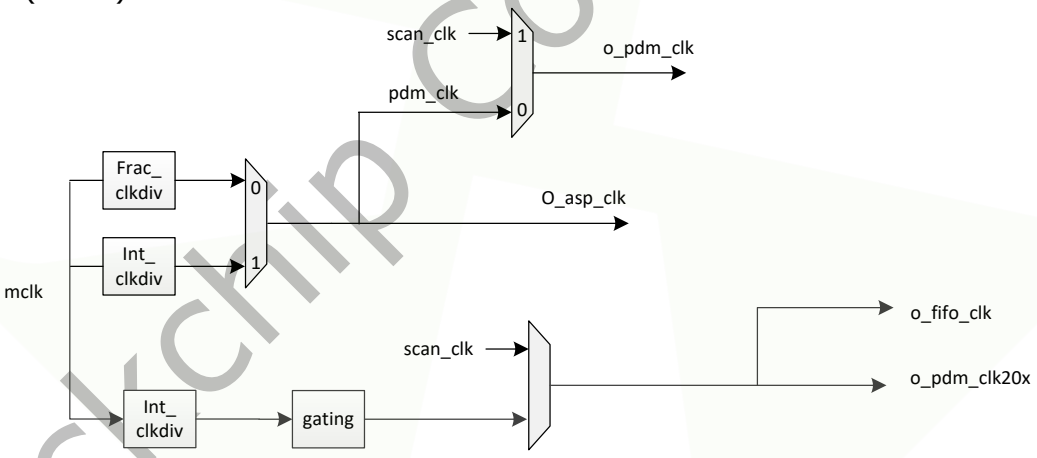


Fig.19-5 PDM Clock Structure

Table 19-1 Relation between PDM_CLK and Sample Rate

PDM_CLK	Sample Rate
3.072MHz	12kHz,24kHz,48kHz,96kHz,192kHz
2.8224MHz	11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz
2.048MHz	8kHz,16kHz,32kHz,64kHz,128kHz

19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PDM_SYSCONFIG	0x0000	W	0x00000000	PDM System Configure Register
PDM_CTRL0	0x0004	W	0x78000377	PDM Control Register 0
PDM_CTRL1	0x0008	W	0x0bb8ea60	PDM Control Register 1
PDM_CLK_CTRL	0x000c	W	0x0000e400	PDM Clock Control Register
PDM_HPF_CTRL	0x0010	W	0x00000000	PDM High-pass Filter Control Register
PDM_FIFO_CTRL	0x0014	W	0x00000000	PDM FIFO Control Register
PDM_DMA_CTRL	0x0018	W	0x0000001f	PDM DMA Control Register
PDM_INT_EN	0x001c	W	0x00000000	PDM Interrupt Enable Register
PDM_INT_CLR	0x0020	W	0x00000000	PDM Interrupt Clear Register
PDM_INT_ST	0x0024	W	0x00000000	PDM Interrupt Status Register
PDM_RXFIFO_DATA_REG	0x0030	W	0x00000000	PDM Receive FIFO Data Register
PDM_DATA0R_REG	0x0034	W	0x00000000	PDM Path0 Right Channel Data Register
PDM_DATA0L_REG	0x0038	W	0x00000000	PDM Path0 Left Channel Data Register
PDM_DATA1R_REG	0x003c	W	0x00000000	PDM Path1 Right Channel Data Register
PDM_DATA1L_REG	0x0040	W	0x00000000	PDM Path1 Left Channel Data Register
PDM_DATA2R_REG	0x0044	W	0x00000000	PDM Path2 Right Channel Data Register
PDM_DATA2L_REG	0x0048	W	0x00000000	PDM Path2 Left Channel Data Register
PDM_DATA3R_REG	0x004c	W	0x00000000	PDM Path3 Right Channel Data Register
PDM_DATA3L_REG	0x0050	W	0x00000000	PDM Path3 Left Channel Data Register
PDM_DATA_VALID	0x0054	W	0x00000000	PDM Path Data Valid Register
PDM_VERSION	0x0058	W	0x59313031	PDM Version Register
PDM_INCR_RXDR	0x0400	W	0x00000000	Increment Address Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

19.4.3 Detail Registers Description

PDM_SYSCONFIG

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rx_start RX transfer start bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
1	RO	0x0	reserved
0	RW	0x0	rx_clr PDM RX logic clear This is a self-cleared bit. High active. Write 1'b1: Clear RX logic Write 1'b0: No action Read 1'b1: Clear ongoing Read 1'b0: Clear done

PDM_CTRL0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	sjm_sel Store justified mode Can be written only when SYSCONFIG[2] is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
30	RW	0x1	path3_en Path 3 enable 1'b1: Enable 1'b0: Disable
29	RW	0x1	path2_en Path 2 enable 1'b1: Enable 1'b0: Disable
28	RW	0x1	path1_en Path 1 enable 1'b1: Enable 1'b0: Disable
27	RW	0x1	path0_en Path 0 enable 1'b1: Enable 1'b0: Disable
26	RW	0x0	hwt_en Halfword word transform Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid
25	RW	0x0	filter_gate_en Filter gate enable If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active.
24	RW	0x0	sig_scale_mode Signal scale mode select 1'b0: CIC outputs the normal latitude. 1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter.
23:16	RW	0x00	int_div_20x_con Integer divider for PDM filter operation.
15:8	RW	0x03	int_div_con Integer divider Can be written only when SYSCONFIG[2] is 0.

Bit	Attr	Reset Value	Description
7:5	RW	0x3	sample_rate_sel Selects which kind of sample rate. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz 3'b011: 48kHz/44.1kHz 3'b100: 96kHz/88.2kHz/64kHz 3'b101~3'b111: 192kHz/176.4kHz/128kHz
4:0	RW	0x17	data_vld_width Can be written only when SYSCONFIG[2] is 0. Valid Data width 0~14: Reserved 15: 16bit 16: 17bit 17: 18bit 18: 19bit ..... n: (n+1)bit 23: 24bit

PDM_CTRL1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0bb8	frac_div_numerator Fraction divider numerator Can be written only when SYSCONFIG[2] is 0.
15:0	RW	0xea60	frac_div_denomonator Fraction divider denominator Can be written only when SYSCONFIG[2] is 0.

PDM_CLK_CTRL

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x3	rx_path_select3 RX Path Select 2'b00: Path3 data from PDM data0 2'b01: Path3 data from PDM data1 2'b10: Path3 data from PDM data2 2'b11: Path3 data from PDM data3
13:12	RW	0x2	rx_path_select2 RX Path Select 2'b00: Path2 data from PDM data0 2'b01: Path2 data from PDM data1 2'b10: Path2 data from PDM data2 2'b11: Path2 data from PDM data3
11:10	RW	0x1	rx_path_select1 RX Path Select 2'b00: Path1 data from PDM data0 2'b01: Path1 data from PDM data1 2'b10: Path1 data from PDM data2 2'b11: Path1 data from PDM data3

Bit	Attr	Reset Value	Description
9:8	RW	0x0	rx_path_select0 RX Path Select 2'b00: Path0 data from PDM data0 2'b01: Path0 data from PDM data1 2'b10: Path0 data from PDM data2 2'b11: Path0 data from PDM data3
7:6	RO	0x0	reserved
5	RW	0x0	pdm_clk_en PDM clk enable, working at PDM mode. Can be written only when SYSCONFIG[2] is 0. 1'b0: PDM clk disable 1'b1: PDM clk enable
4	RW	0x0	div_type_sel Divider type select signal Can be written only when SYSCONFIG[2] is 0. 1'b0: Fraction divider 1'b1: Integer divider
3	RW	0x0	lr_ch_ex Left and right channel data exchange 1'b0: Not inverted 1'b1: Inverted
2	RW	0x0	fir_com_bps Fir compensate filter bypass 1'b0: Not bypass 1'b1: Bypass
1:0	RW	0x0	cic_ds_ratio CIC filter decimation ratio 2'b00: 16 times decimation 2'b01: 8 times decimation 2'b10: 4 times decimation other: 8 times decimation

PDM_HPF_CTRL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	hpfle High-pass filter enable for left channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
2	RW	0x0	hpfre High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
1:0	RW	0x0	hpf_cf High-pass filter configure 2'b00: 3.79Hz 2'b01: 60Hz 2'b10: 243Hz 2'b11: 493Hz

PDM_FIFO_CTRL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	rft Receive FIFO threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered.
7:0	RO	0x00	rfl Receive FIFO level Contains the number of valid data entries in the receive FIFO.

PDM_DMA_CTRL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
7	RO	0x0	reserved
6:0	RW	0x1f	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.

PDM_INT_EN

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxoie RX overflow interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	rxftie RX full threshold interrupt enable 1'b0: Disable 1'b1: Enable

PDM_INT_CLR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxoic RX overflow interrupt clear (high active and auto cleared).

PDM_INT_ST

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	rxoi RX overflow interrupt 1'b0: Inactive 1'b1: Active

Bit	Attr	Reset Value	Description
0	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active

PDM_RXFIFO_DATA_REG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdr Receive FIFO shadow register When the register is read, data in the receive FIFO is accessed.

PDM_DATA0R_REG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0r Data of the path 0 right channel

PDM_DATA0L_REG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0l Data of the path 0 left channel

PDM_DATA1R_REG

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1r Data of the path 1 right channel

PDM_DATA1L_REG

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1l Data of the path 1 left channel

PDM_DATA2R_REG

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2r Data of the path 2 right channel

PDM_DATA2L_REG

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2l Data of the path 2 left channel

PDM_DATA3R_REG

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3r Data of the path 3 right channel

PDM_DATA3L_REG

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3l Data of the path 3 left channel

PDM_DATA_VALID

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	WO	0x0	path0_vld 1'b0: DATA0R_REG, DATA0L_REG value is invalid. 1'b1: DATA0R_REG, DATA0L_REG value is valid.
2	WO	0x0	path1_vld 1'b0: DATA1R_REG, DATA1L_REG value is invalid. 1'b1: DAT1R_REG, DATA1L_REG value is valid.
1	WO	0x0	path2_vld 1'b0: DATA2R_REG, DATA2L_REG value is invalid. 1'b1: DATA2R_REG, DATA2L_REG value is valid.
0	WO	0x0	path3_vld 1'b0: DATA3R_REG, DATA3L_REG value is invalid. 1'b1: DATA3R_REG, DATA3L_REG value is valid.

PDM_VERSION

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x59313031	version PDM version

PDM_INCR_RXDR

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	receive_fifo_data FIFO data can be read from these registers. This register is used when the access address is increment.

19.5 Interface Description

There are three groups of PDM IO interfaces embedded in the chip. Following figure shows the group 0, group 1 and group 2 PDM IO interface respectively.

Table 19-2 Group 0 PDM IO Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
o_pdm_clk	O	IO_I2S1lrckrxm0_UART4txm0_PDMclk0m0_AUDIOPWMroutp_VCCIO1GPIO1a6	GRF_GPIO1A_IOMUX_H[10:8]=3'b011
o_pdm_clk	O	IO_I2S1sclkrxm0_UART4rxm0_PDMclk1m0_SPDIFtxm0_VCCIO1GPIO1a4	GRF_GPIO1A_IOMUX_H[2:0]=3'b011
i_pdm_data0	I	IO_I2S1sdi0m0_PDMsdi0m0_VCCIO1GPIO1b3	GRF_GPIO1B_IOMUX_L[14:12]=3'b010
i_pdm_data1	I	IO_I2S1sdo3m0_I2S1sdi1m0_PDMsdi1m0_PCIE20perstnm2_VCCIO1GPIO1b2	GRF_GPIO1B_IOMUX_L[10:8]=3'b011
i_pdm_data2	I	IO_I2S1sdo2m0_I2S1sdi2m0_PDMsdi2m0_PCIE20wakenm2_ACODECadc_sync_VCCIO1GPIO1b1	GRF_GPIO1B_IOMUX_L[6:4]=3'b011
i_pdm_data3	I	IO_I2S1sdo1m0_I2S1sdi3m0_PDMsdi3m0_PCIE20clkreqnm2_ACODECdac_datar_VCCIO1GPIO1b0	GRF_GPIO1B_IOMUX_L[2:0]=3'b011

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 19-3 Group 1 PDM IO Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
o_pdm_clk	O	IO_CIFd8_EBCsddo8_GMAC1txd2m1_UART1txm1_PDMclk0m1_VCCIO6GPIO3d6	GRF_GPIO3D_IOMUX_H[10:8]=3'b101
o_pdm_clk	O	IO_CIFd10_EBCsddo10_GMAC1txclkm1_PDMclk1m1_VCCIO6GPIO4a0	GRF_GPIO4A_IOMUX_L[2:0]=3'b100

i_pdm_data0	I	IO_CIFd9_EBCsddo9_GMAC1txd3m1_UART1rxm1_PDMsdi0m1_VCCIO6GPIO3d7	GRF_GPIO3D_IOMUX_H[14:12]=3'b101
i_pdm_data1	I	IO_CIFd11_EBCsddo11_GMAC1rxd2m1_PDMsdi1m1_VCCIO6GPIO4a1	GRF_GPIO4A_IOMUX_L[6:4]=3'b100
i_pdm_data2	I	IO_CIFd12_EBCsddo12_GMAC1rxd3m1_UART7txm2_PDMsdi2m1_VCCIO6GPIO4a2	GRF_GPIO4A_IOMUX_L[10:8]=3'b101
i_pdm_data3	I	IO_CIFd13_EBCsddo13_GMAC1rxclkm1_UART7rxm2_PDMsdi3m1_VCCIO6GPIO4a3	GRF_GPIO4A_IOMUX_L[14:12]=3'b101

Table 19-4 Group 2 PDM IO Interface Description

Module Pin	Dir.	Pin Name	IOMUX Setting
o_pdm_clk	O	IO_PWM14m0_VOPpwmm1_GMAC1mdcm0_UART7txm1_PDMclk1m2_VCCIO5GPIO3c4	GRF_GPIO3C_IOMUX_H[2:0]=3'b101
i_pdm_data0	I	IO_LCDCd18_BT1120d9_GMAC1rxdvcrsm0_I2C5sclm0_PDMsdi0m2_VCCIO5GPIO3b3	GRF_GPIO3B_IOMUX_L[14:12]=3'b101
i_pdm_data1	I	IO_LCDCd19_BT1120d10_GMAC1rxerm0_I2C5sdam0_PDMsdi1m2_VCCIO5GPIO3b4	GRF_GPIO3B_IOMUX_H[2:0]=3'b101
i_pdm_data2	I	IO_LCDCd22_PWM12m0_GMAC1txenm0_UART3txm1_PDMsdi2m2_VCCIO5GPIO3b7	GRF_GPIO3B_IOMUX_H[14:12]=3'b101
i_pdm_data3	I	IO_LCDCd23_PWM13m0_GMAC1mclkinoutm0_UART3rxm1_PDMsdi3m2_VCCIO5GPIO3c0	GRF_GPIO3C_IOMUX_L[2:0]=3'b101

19.6 Application Notes

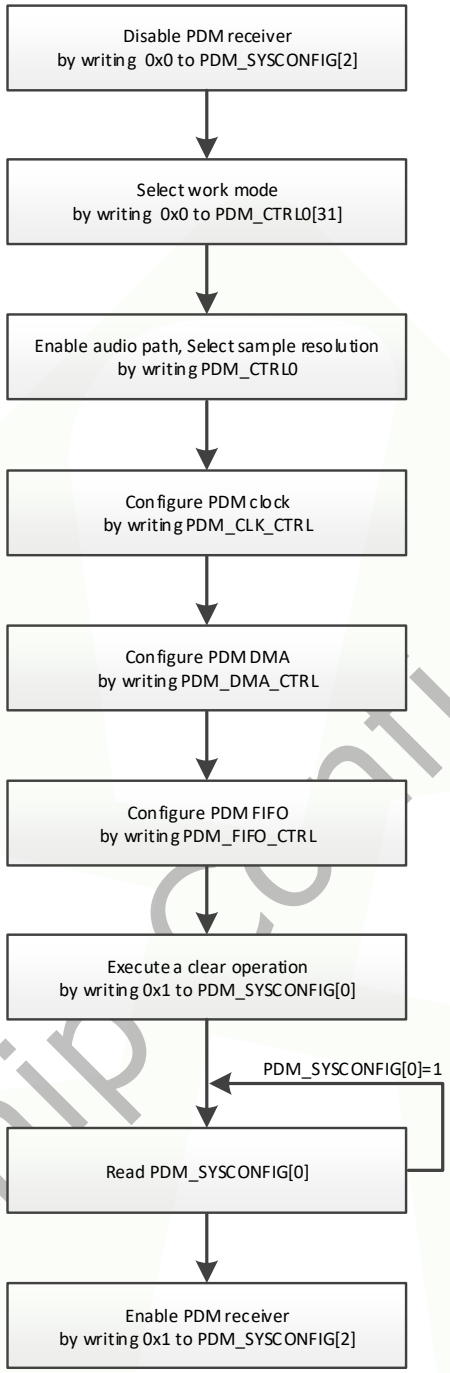


Fig.19-6 PDM Operation Flow

Chapter 20 SPDIF Transmitter

20.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme.
It supports following features:

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support 16, 20, 24 bits audio data transfer

20.2 Block Diagram

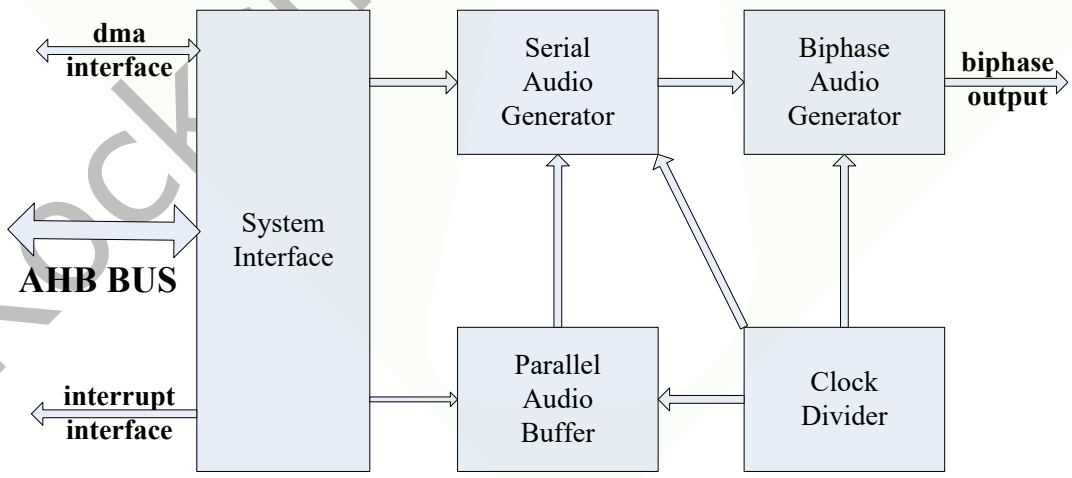


Fig.20-1 SPDIF transmitter Block Diagram

The SPDIF is composed by:

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

Parallel Audio Buffer

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

20.3 Function description

20.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

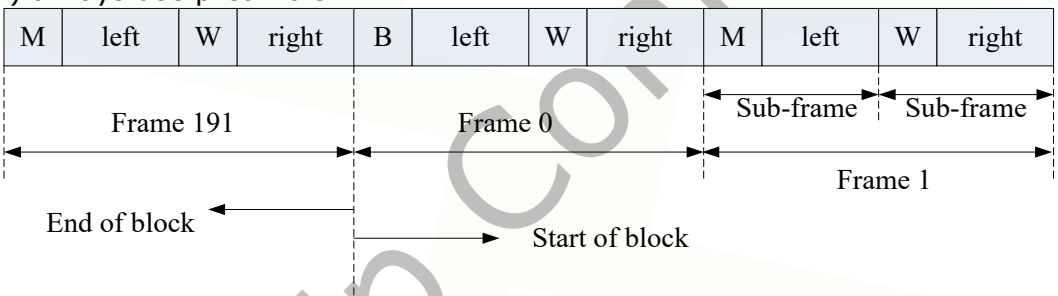


Fig.20-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

20.3.2 Sub-frame Format

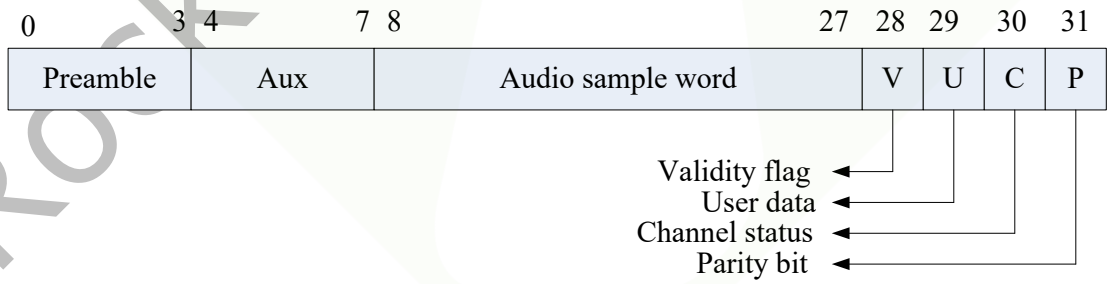


Fig.20-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8.Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20),the unused LSBs

are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

20.3.3 Channel Coding

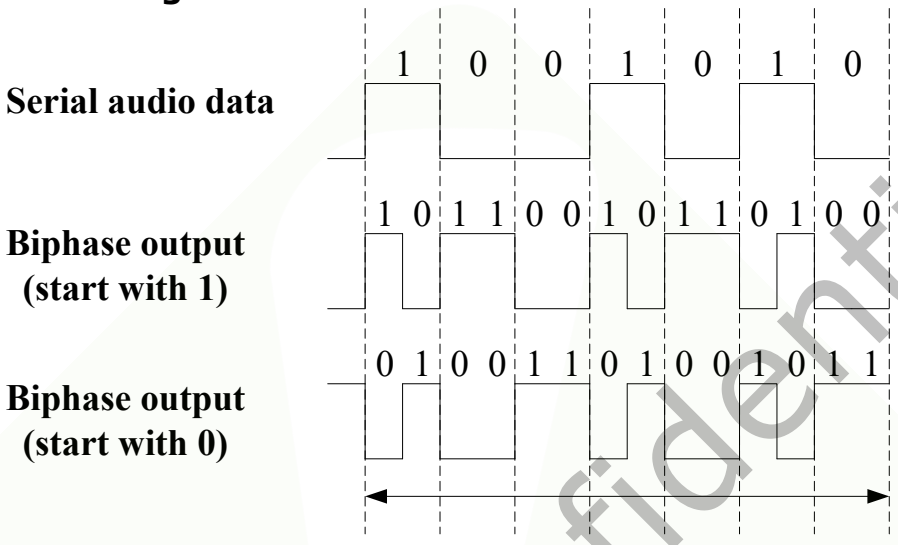


Fig.20-4 SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

20.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

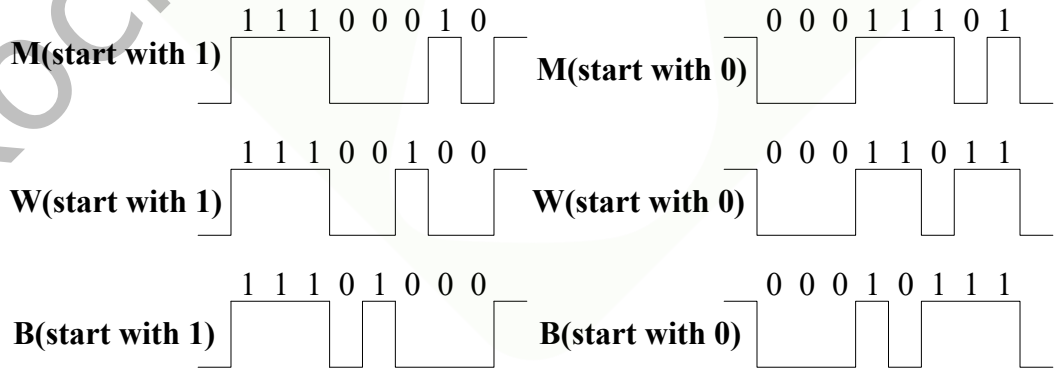


Fig.20-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

20.4 Register Description

20.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_CFGR	0x0000	W	0x00000000	Transfer Configuration Register
SPDIF_SDBLR	0x0004	W	0x00000000	Sample Date Buffer Level Register
SPDIF_DMACR	0x0008	W	0x00000000	DMA Control Register
SPDIF_INTCR	0x000C	W	0x00000000	Interrupt Control Register
SPDIF_INTSR	0x0010	W	0x00000000	Interrupt Status Register
SPDIF_XFER	0x0018	W	0x00000000	Transfer Start Register
SPDIF_SMPDR	0x0020	W	0x00000000	Sample Data Register
SPDIF_VLDFRn	0x0060	W	0x00000000	Validity Flag Register n
SPDIF_USRDRn	0x0090	W	0x00000000	User Data Register n
SPDIF_CHNSRn	0x00C0	W	0x00000000	Channel Status Register n
SPDIF_BURTSINFO	0x0100	W	0x00000000	Channel Burst Info Register
SPDIF_REPETTION	0x0104	W	0x00000000	Channel Repetition Register
SPDIF_BURTSINFO_SHD	0x0108	W	0x00000000	Shadow Channel Burst Info Register
SPDIF_REPETTION_SHD	0x010C	W	0x00000000	Shadow Channel Repetition Register
SPDIF_USRDR_SHDn	0x0190	W	0x00000000	Shadow User Data Register n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.4.2 Detail Registers Description

SPDIF_CFGR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	MCD Fmclk/Fsdo This parameter can be calculated by Fmclk/(Fs*128). Fs=the sample frequency be wanted
15:9	RO	0x00	reserved
8	RW	0x0	PCMTYPE 1'b0: linear PCM 1'b1: non-linear PCM
7	WO	0x0	CLR Write 1 to clear MCLK domain logic. Read return zero.
6	RW	0x0	CSE 1'b0: disable 1'b1: enable The bit should be set to 1 when the channel conveys non-linear PCM
5	RW	0x0	UDE 1'b0: disable 1'b1: enable
4	RW	0x0	VFE 1'b0: disable 1'b1: enable
3	RW	0x0	ADJ 1'b0: Right justified 1'b1: Left justified

Bit	Attr	Reset Value	Description
2	RW	0x0	HWT 1'b0: disable 1'b1: enable It is valid only when the valid data width is 16bit.
1:0	RW	0x0	VDW 2'b00: 16bit 2'b01: 20bit 2'b10: 24bit 2'b11: reserved The valid data width is 16bit only for non-linear PCM

SPDIF_SDBLR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	SDBLR Contains the number of valid data entries in the sample data buffer.

SPDIF_DMACR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	TDE 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
4:0	RW	0x00	TDL This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value

SPDIF_INTCR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	UDTIC Write 1'b1 to clear the user data interrupt.
16	W1C	0x0	BTTIC Write 1'b1 to clear the interrupt.
15:10	RO	0x00	reserved
9:5	RW	0x00	SDBT Sample Date Buffer Threshold for empty interrupt
4	RW	0x0	SDBEIE 1'b0: disable 1'b1: enable
3	RW	0x0	BTTIE When enabled, an interrupt will be asserted when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
2	RW	0x0	UDTIE 1'b0: disable 1'b1: enable If enabled, an interrupt will be asserted when the content of the user data register is fed into the corresponding shadow register
1:0	RO	0x0	reserved

SPDIF_INTSR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	SDBEIS 1'b0: inactive 1'b1: active
3	RW	0x0	BTTIS 1'b0: inactive 1'b1: active
2	RW	0x0	UDTIS 1'b0: inactive 1'b1: active
1:0	RO	0x0	reserved

SPDIF_XFER

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	XFER Transfer Start Register

SPDIF_SMPDR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SMPDR Sample Data Register

SPDIF_VLDFRn

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VLDFR_SUB_1 Validity Flag Register 0
15:0	RW	0x0000	VLDFR_SUB_0 Validity Flag For Subframe 0

SPDIF_USRDRn

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RW	0x0000	USR_SUB_0 User Data Bit for Subframe 0

SPDIF_CHNSRn

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel Status Bit for Subframe 1
15:0	RW	0x0000	CHNSR_SUB_0 Channel Status Bit for Subframe 0

SPDIF_BURTSINFO

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the bitstream number is 0.
12:8	RW	0x00	DATAINFO This field gives the data-type-dependent info
7	RW	0x0	ERRFLAG 1'b0: indicates a valid burst-payload 1'b1: indicates that the burst-payload may contain errors
6:0	RW	0x00	DATATYPE 7'b0000000: null data 7'b0000001: AC-3 data 7'b0000011: Pause data 7'b0000100: MPEG-1 layer 1 data 7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 7'b0000110: MPEG-2 data with extension 7'b0000111: MPEG-2 AAC 7'b0001000: MPEG-2, layer-1 low sampling frequency 7'b0001001: MPEG-2, layer-2 low sampling frequency 7'b0001010: MPEG-2, layer-3 low sampling frequency 7'b0001011: DTS type I 7'b0001100: DTS type II 7'b0001101: DTS type III 7'b0001110: ATRAC 7'b0001111: ATRAC 2/3 7'b0010000: ATRAC-X 7'b0010001: DTS type IV 7'b0010010: WMA professional type I 7'b0110010: WMA professional type II 7'b1010010: WMA professional type III 7'b1110010: WMA professional type IV 7'b0010011: MPEG-2 AAC low sampling frequency 7'b0110011: MPEG-2 AAC low sampling frequency 7'b1010011: MPEG-2 AAC low sampling frequency 7'b1110011: MPEG-2 AAC low sampling frequency 7'b0010100: MPEG-4 AAC 7'b0110100: MPEG-4 AAC 7'b1010100: MPEG-4 AAC 7'b1110100: MPEG-4 AAC 7'b0010101: Enhanced AC-3 7'b0010110: MAT others: reserved

SPDIF_REPETTION

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This define the repetition period when the channel conveys non-linear PCM

SPDIF_BURTSINFO_SHD

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM This field indicates the bitstream number. Usually the bitstream number is 0.
12:8	RO	0x00	DATAINFO This field gives the data-type-dependent info
7	RO	0x0	ERRFLAG 1'b0: indicates a valid burst-payload 1'b1: indicates that the burst-payload may contain errors
6:0	RO	0x00	DATATYPE 7'b0000000: null data 7'b0000001: AC-3 data 7'b0000011: Pause data 7'b0000100: MPEG-1 layer 1 data 7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 7'b0000110: MPEG-2 data with extension 7'b0000111: MPEG-2 AAC 7'b0001000: MPEG-2, layer-1 low sampling frequency 7'b0001001: MPEG-2, layer-2 low sampling frequency 7'b0001010: MPEG-2, layer-3 low sampling frequency 7'b0001011: DTS type I 7'b0001100: DTS type II 7'b0001101: DTS type III 7'b0001110: ATRAC 7'b0001111: ATRAC 2/3 7'b0010000: ATRAC-X 7'b0010001: DTS type IV 7'b0010010: WMA professional type I 7'b0110010: WMA professional type II 7'b1010010: WMA professional type III 7'b1110010: WMA professional type IV 7'b0010011: MPEG-2 AAC low sampling frequency 7'b0110011: MPEG-2 AAC low sampling frequency 7'b1010011: MPEG-2 AAC low sampling frequency 7'b1110011: MPEG-2 AAC low sampling frequency 7'b0010100: MPEG-4 AAC 7'b0110100: MPEG-4 AAC 7'b1010100: MPEG-4 AAC 7'b1110100: MPEG-4 AAC 7'b0010101: Enhanced AC-3 7'b0010110: MAT others: reserved

SPDIF_REPETTION_SHD

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	REPETTION This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it defines the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.

SPDIF_USRDR_SHDn

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User Data Bit for Subframe 1
15:0	RO	0x0000	USR_SUB_0 User Data Bit for Subframe 0

20.5 Interface Description

Table 20-1 spdif transmitter interface

Module Pin	Dir.	Pad Name	IOMUX Setting
spdif_txm0	O	I2S1_SCLK_RX_M0/UART4_RX_M0/PDM_CLK1_M0/SPDIF_TX_M0/GPIO1_A4_d	GRF_GPIO1A_IOMUX_H[2:0]=3'b100
spdif_txm1	O	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	GRF_GPIO3C_IOMUX_H[6:4]=3'b010
spdif_txm2	O	EDP_DP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	GRF_GPIO4C_IOMUX_H[2:0]=3'b010

The output of SPDIF module which signals as spdif_8ch_sdo is also connected to the audio interface of HDMI.

Table 20-2 Interface Between SPDIF And HDMI

Module Pin	Direction	Module Pin	Direction
mclk_spdif_8ch	O	ispdifclk	I
spdif_8ch_sdo	O	ispdifdata	I

Notes: I=input, O=output, I/O=input/output, bidirectional

20.6 Application Notes

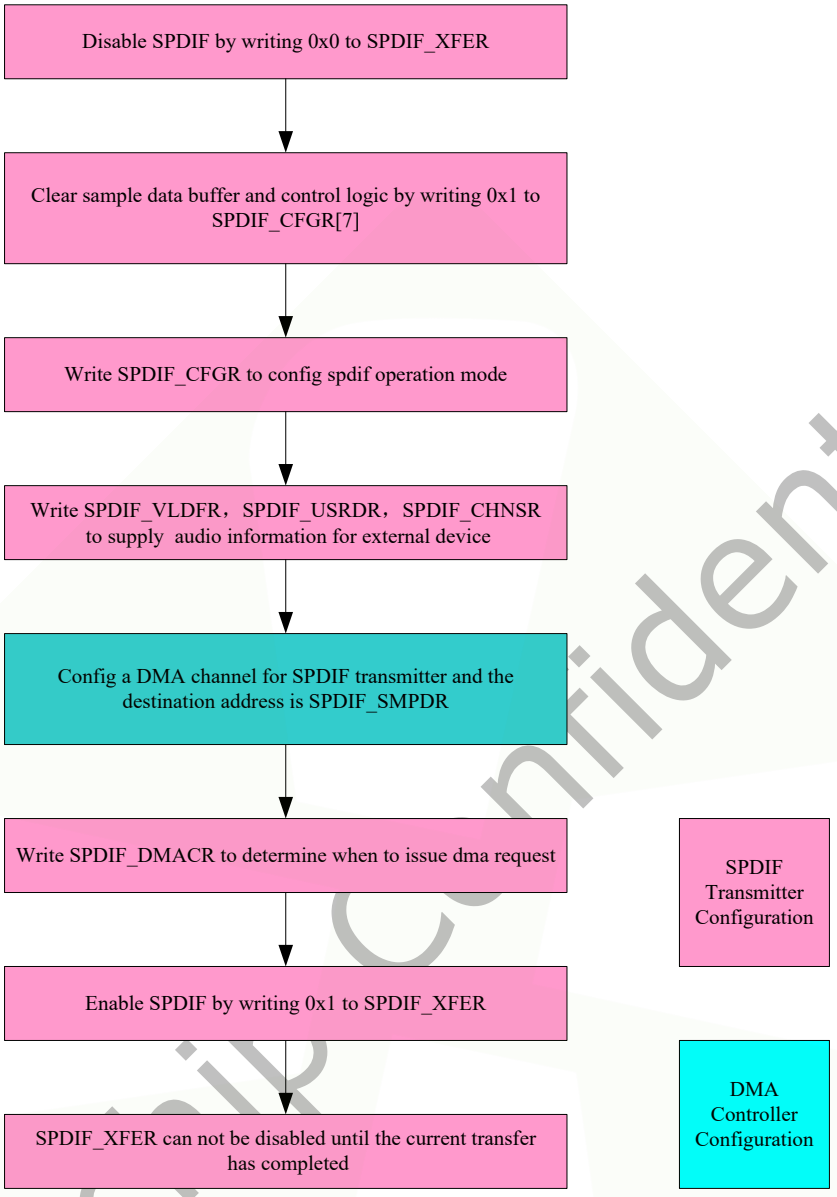


Fig.20-6 SPDIF transmitter operation flow chart

The above figure shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.

Chapter 21 I2S_TDM

21.1 Overview

The I2S/PCM/TDM controller is designed for interfacing between the AHB bus and the I2S bus.
The I2S bus (Inter-IC sound bus) is a serial link for digital audio data transfer between devices in the system and is invented by Philips Semiconductor. Now it is widely used by many semiconductor manufacturers.
I2S bus is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the I2S interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

21.1.1 Features

There is one I2S/PCM/TDM controller and two I2S/PCM controllers embed in the system. These four controllers are named as I2S0, I2S1 and I2S2/ I2S3. The I2S0 is connected hdmi.The I2S1 supports I2S, PCM and TDM mode while the I2S2 or I2S3 supports I2S and PCM mode stereo audio output and input. Unless stated separately, all of the following features apply to I2S0, I2S1 ,I2S2 and I2S3.

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and the others for receiving audio data for I2S1
- Support two internal 32-bit wide and 32-location deep FIFOs, one for transmitting and the other for receiving audio data for each I2S2 and I2S3
- Support AHB bus interface
- Support 16~32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support a total of 8 channels transmitting and receiving in I2S mode at the same time for I2S1
- Support 2-channel audio transmitting and receiving in PCM mode for I2S1
- Support 2-channel audio transmitting and receiving in I2S mode and 2 channel in PCM mode for I2S2
- Support 2-channel audio transmitting and receiving in I2S mode and 2-channel in PCM mode for I2S3
- Support up to 192kHz sample rate
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support TDM normal, 1/2 cycle left shift , 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer for I2S1
- Support MSB or LSB first serial audio data transfer
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 2 independent LRCK signals, one for receiving and the other for transmitting audio data. Single LRCK can be used for transmitting and receiving data if the sample rate are the same
- Support configurable SCLK and LRCK polarity
- Support a range of 16 to 32 programmable slot bit width in TDM mode for I2S1
- Support a range of 32 to 512 programmable frame width in TDM mode for I2S1
- Support programmable FSYNC width in TDM mode for I2S1

21.2 Controller Block Diagram

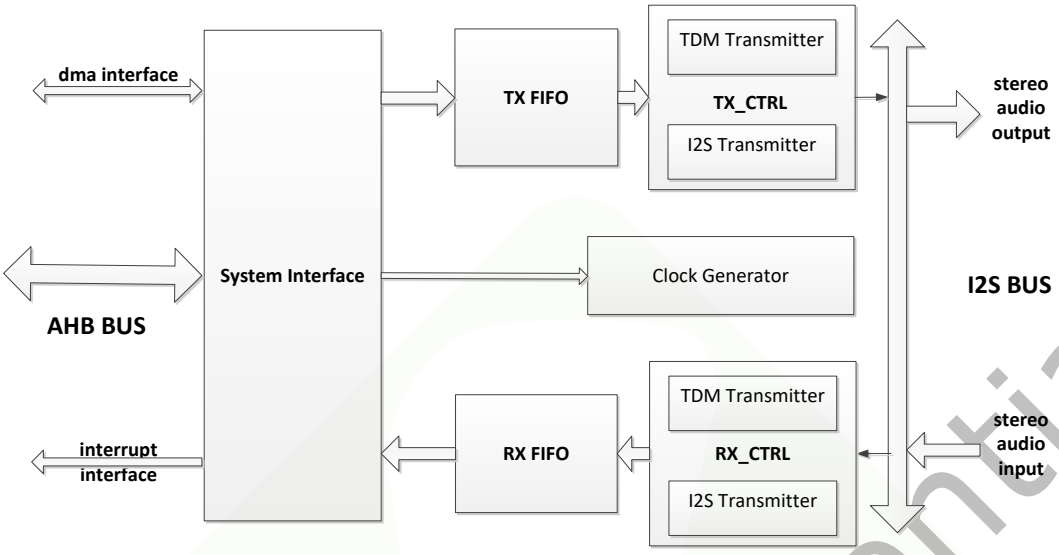


Fig.21-1 I2S/PCM/TDM Controller (8-channel) Block Diagram

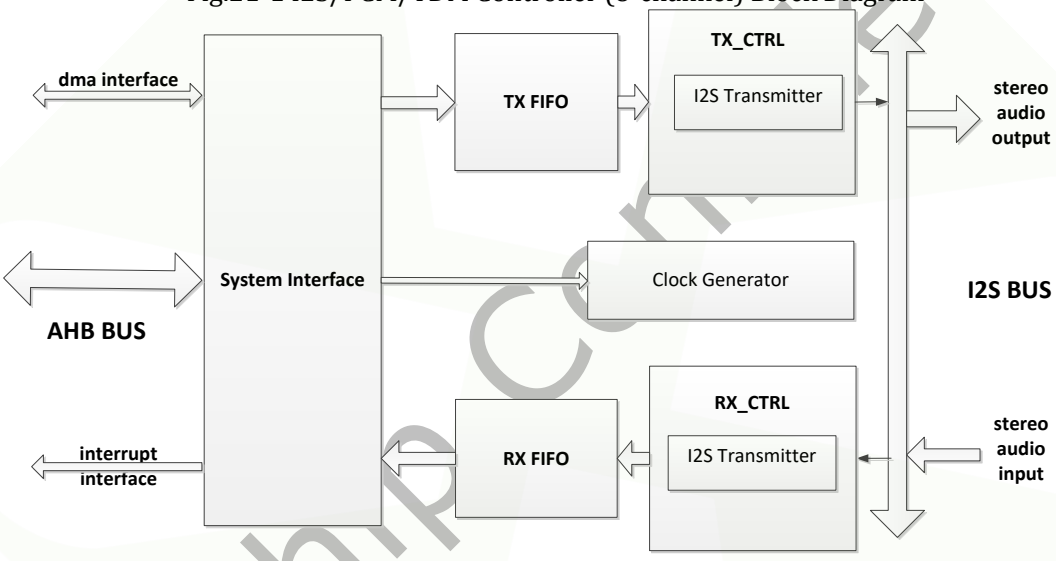


Fig.21-2 I2S/PCM Controller (2-channel) Block Diagram

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Generator

The Clock Generator implements clock generation function. By the divider of the module, the clock generator generates SCLK and LRCK to transmitter and receiver.

Transmitters

The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.

Receiver

The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.

Transmit FIFO

The Transmit FIFO is the buffer to store transmitted audio data. The size of one FIFO is 32bits x 32.

Receive FIFO

The Receive FIFO is the buffer to store received audio data. The size of one FIFO is 32bits x 32.

21.3 Function description

In the I2S/PCM/TDM or I2S/PCM controller, there are four types: transmitter-master & receiver-master; transmitter-master & receiver-slave; transmitter-slave & receiver-master; transmitter-slave & receiver-slave.
In broadcasting application, the I2S/PCM/TDM or I2S/PCM controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the I2S/PCM/TDM or I2S/PCM controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the I2S/PCM/TDM or I2S/PCM controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

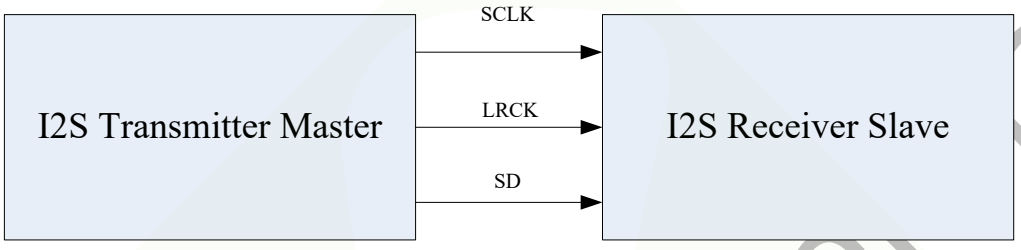


Fig.21-3 I2S Transmitter-Master & Receiver-Slave Condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and LRCK signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and LRCK signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.

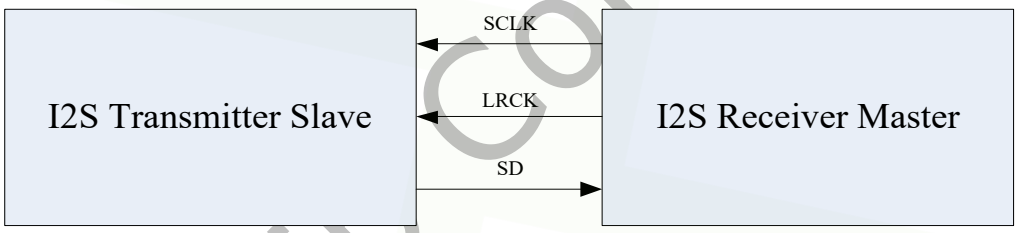


Fig.21-4 I2S Transmitter-Slave & Receiver-Master Condition

When the receiver acts as a master, it sends SCLK and LRCK signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.
Before transmitting or receiving data, CPU need do initial setting to the I2S register. These includes CPU settings, I2S interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.

21.3.1 I2S Normal Mode

This is the waveform of I2S normal mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes low to indicate left channel and high to right channel. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

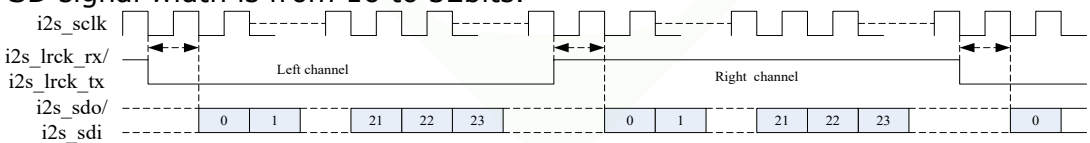


Fig.21-5 I2S Normal Mode Timing Format

21.3.2 I2S Left Justified Mode

This is the waveform of I2S left justified mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range

of SD signal width is from 16 to 32bits.

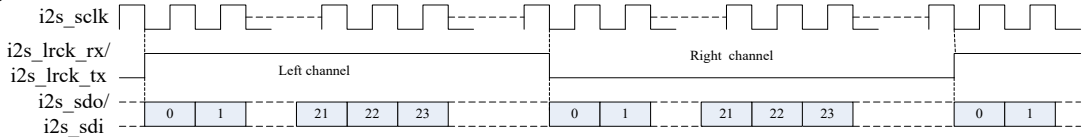


Fig.21-6 I2S Left Justified Mode Timing Format

21.3.3 I2S Right Justified Mode

This is the waveform of I2S right justified mode. For LRCK (i2s_lrck_rx/ i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo, i2s_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the LRCK signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 16 to 32bits.

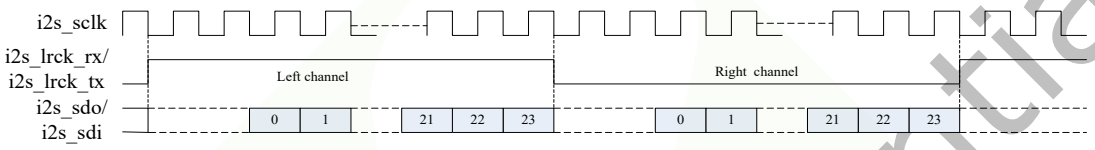


Fig.21-7 I2S Right Justified Mode Timing Format

21.3.4 PCM Early Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

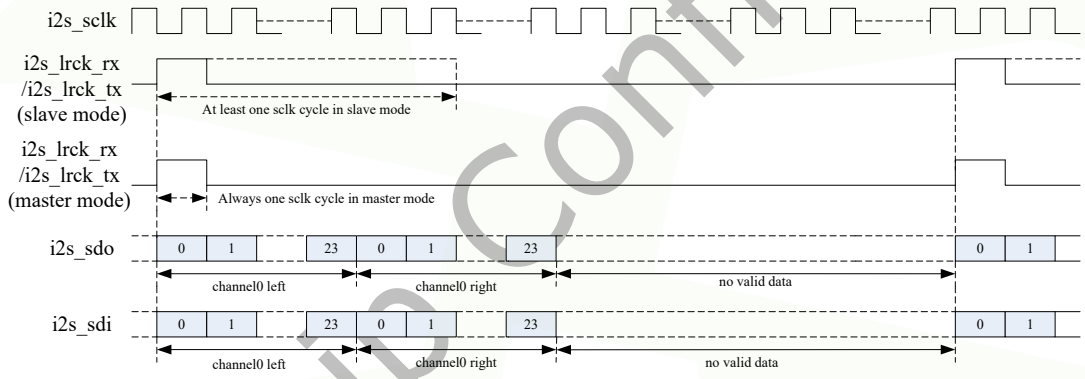


Fig.21-8 PCM Early Mode Timing Format

21.3.5 PCM Late1 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits.

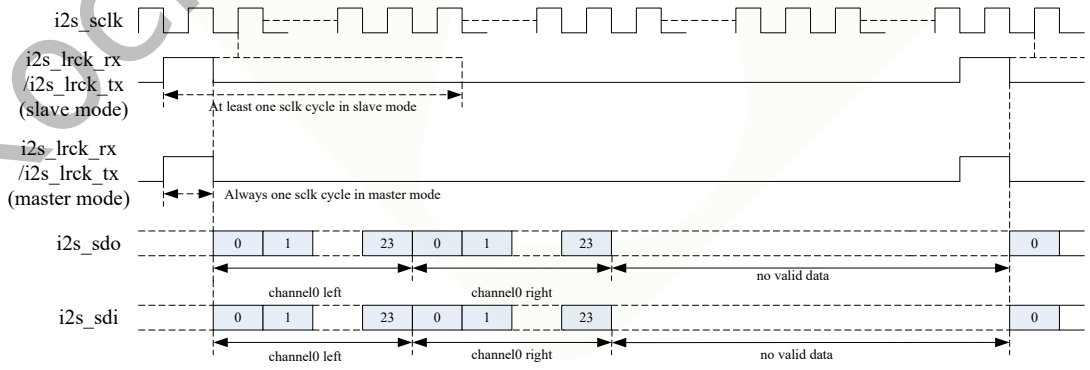


Fig.21-9 PCM Late1 Mode Timing Format

21.3.6 PCM Late2 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it

sends the first bit (MSB or LSB)two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

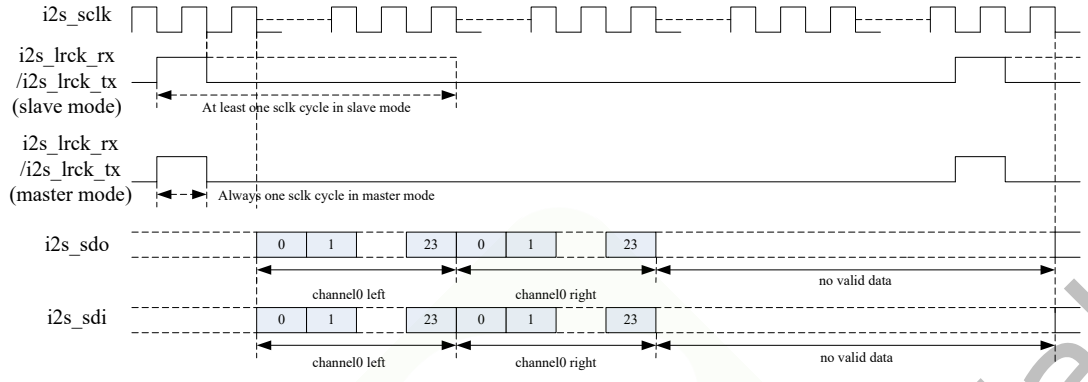


Fig.21-10 PCM Late2 Mode Timing Format

21.3.7 PCM Late3 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

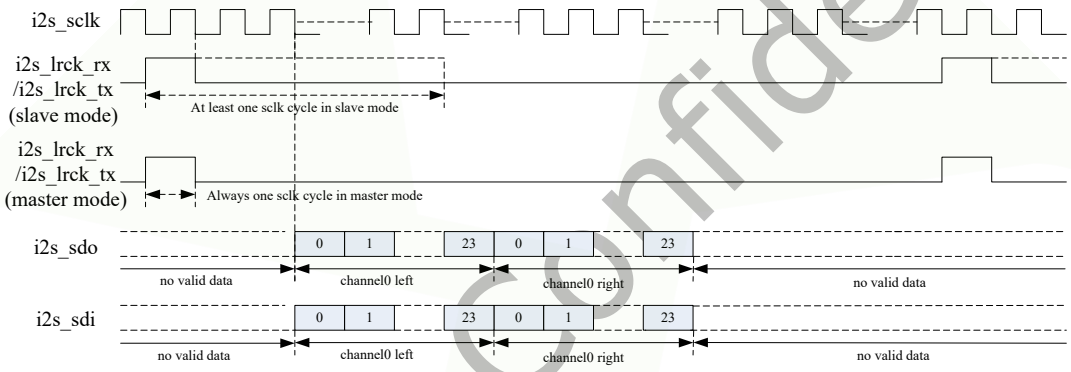


Fig.21-11 PCM Late3 Mode Timing Format

21.3.8 TDM Normal Mode (PCM Format)

This is the waveform of TDM normal mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the second falling edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

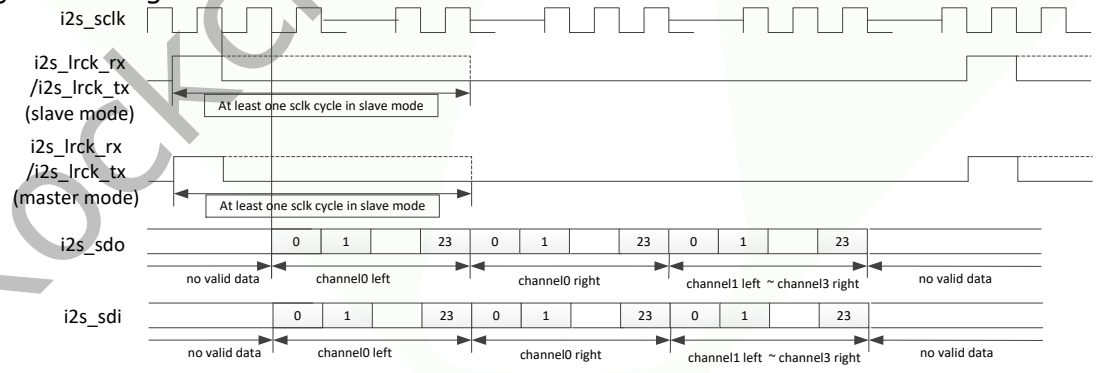


Fig.21-12 TDM Normal Mode Timing Format (PCM Format)

21.3.9 TDM Left Shift Mode0 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the second rising edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

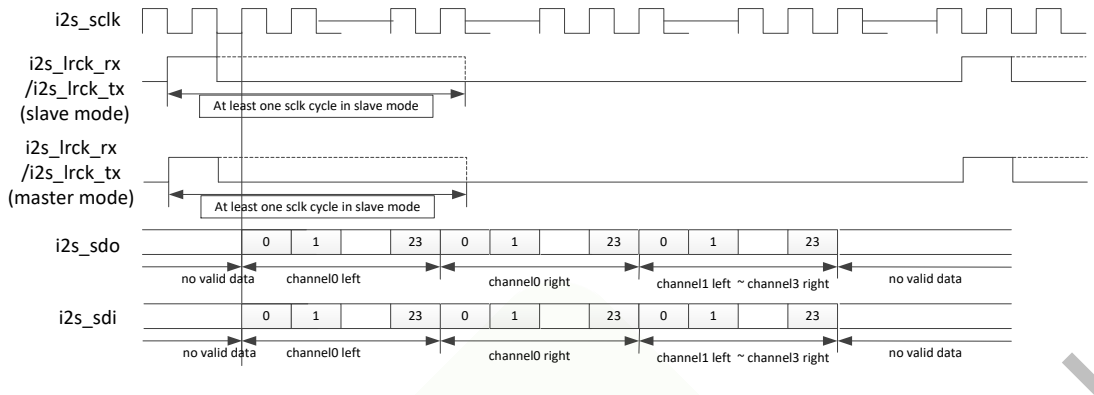


Fig.21-13 TDM Left Shift Mode 0 Timing Format (PCM Format)

21.3.10 TDM Left Shift Mode1 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the first falling edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

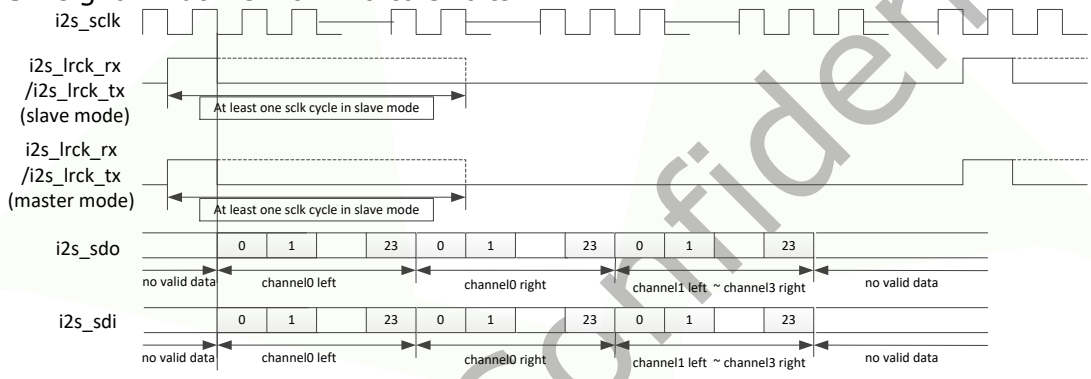


Fig.21-14 TDM Left Shift Mode 1 Timing Format (PCM Format)

21.3.11 TDM Left Shift Mode2 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the first rising edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

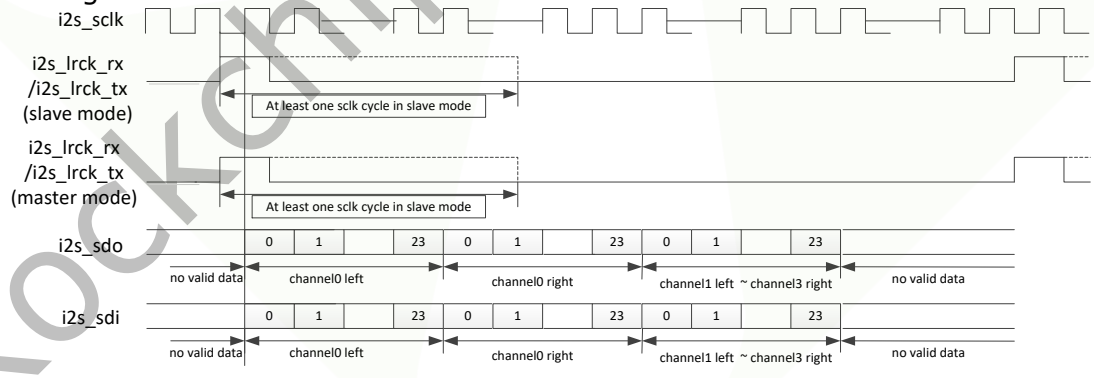


Fig.21-15 TDM Left Shift Mode 2 Timing Format (PCM Format)

21.3.12 TDM Left Shift Mode3 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s1_sdo, i2s1_sdi) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

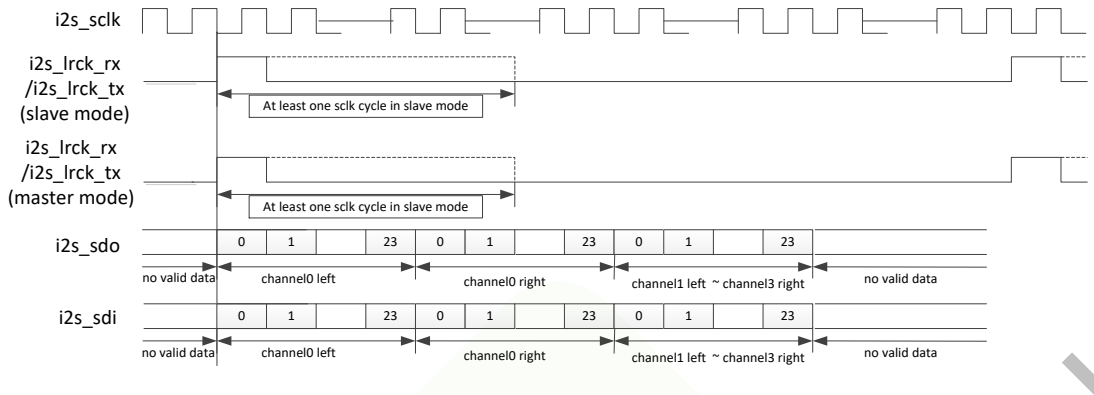
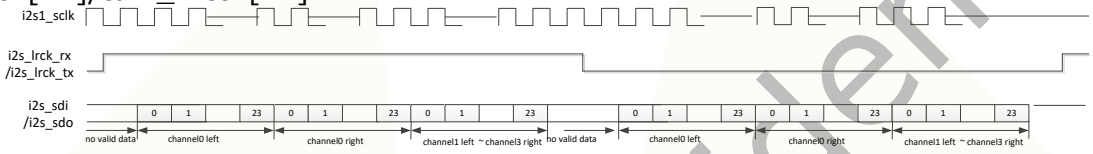


Fig.21-16 TDM Left Shift Mode 3 Timing Format (PCM Format)

21.3.13 TDM Normal Mode (I2S Format)

This is the waveform of I2S normal mode. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB)on the first falling edge of SCLK after LRCK changes. The range of SD signal width is from 16 to 32bits.

tdm_txctrl[17]/tdm_rxctrl[17]=1:



tdm_txctrl[17]/tdm_rxctrl[17]=0:

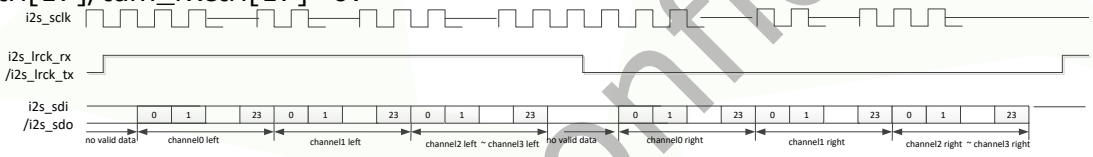
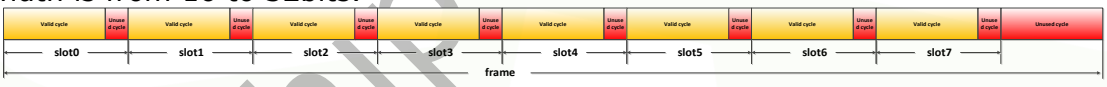


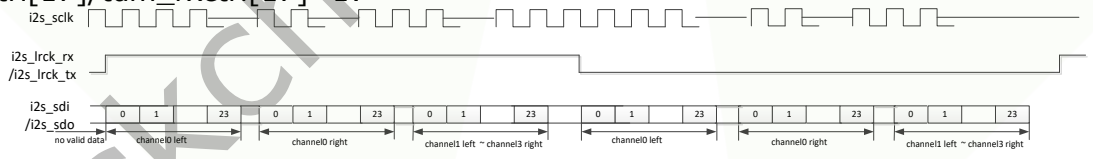
Fig.21-17 TDM Normal Mode Timing Format (I2S Format)

21.3.14 TDM Left Justified Mode (I2S Format)

This is the waveform of I2S left justified mode. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.



tdm_txctrl[17]/tdm_rxctrl[17]=1:



tdm_txctrl[17]/tdm_rxctrl[17]=0:

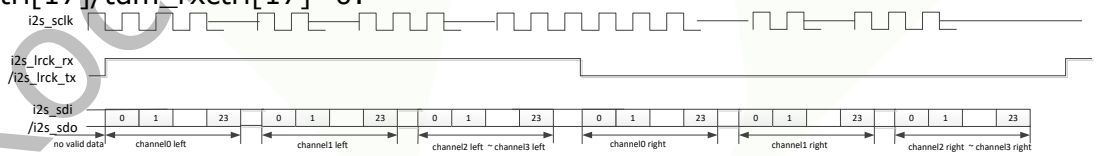
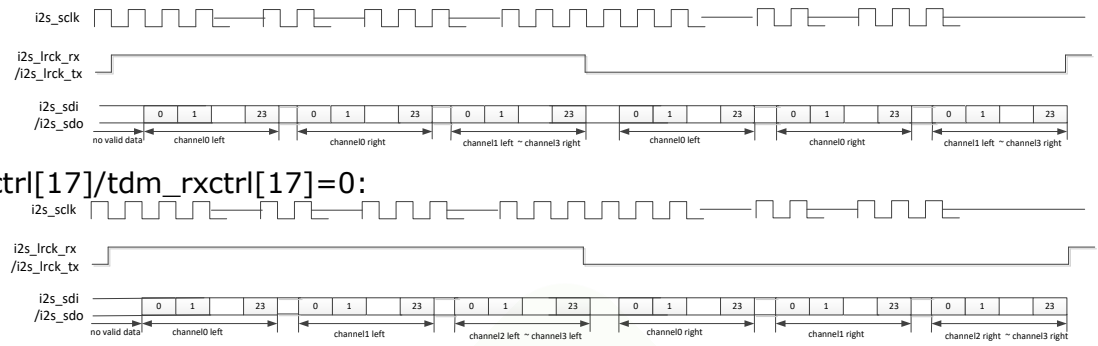


Fig.21-18 TDM Left Justified Mode Timing Format (I2S Format)

21.3.15 TDM Right Justified Mode (I2S Format)

This is the waveform of I2S right justified mode. For SD (i2s_sdo, i2s_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode. The range of SD signal width is from 16 to 32bits.

tdm_txctrl[17]/tdm_rxctrl[17]=1:



tdm_txctrl[17]/tdm_rxctrl[17]=0:

Fig.21-19 TDM Right Justified Mode Timing Format (I2S Format)

21.4 Register description

21.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

21.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
I2S_TDM_8CH_TXCR	0x0000	W	0x72000000	Transmit Operation Control Register
I2S_TDM_8CH_RXCR	0x0004	W	0x01C80000	Receive Operation Control Register
I2S_TDM_8CH_CKR	0x0008	W	0x00000000	Clock Generation Register
I2S_TDM_8CH_TXFIFOLR	0x000C	W	0x00000000	TX FIFO Level Register
I2S_TDM_8CH_DMACR	0x0010	W	0x00000000	DMA Control Register
I2S_TDM_8CH_INTCR	0x0014	W	0x01F00000	Interrupt Control Register
I2S_TDM_8CH_INTSR	0x0018	W	0x00000000	Interrupt Status Register
I2S_TDM_8CH_XFER	0x001C	W	0x00000000	Transfer Start Register
I2S_TDM_8CH_CLR	0x0020	W	0x00000000	Sclk Domain Logic Clear Register
I2S_TDM_8CH_TXDR	0x0024	W	0x00000000	Transmit FIFO Data Register
I2S_TDM_8CH_RXDR	0x0028	W	0x00000000	Receive FIFO Data Register
I2S_TDM_8CH_RXFIFOLR	0x002C	W	0x00000000	RX FIFO Level Register
I2S_TDM_8CH_TDM_TXCTRL	0x0030	W	0x00000000	TDM Mode Transmit Operation Control Register
I2S_TDM_8CH_TDM_RXCTRL	0x0034	W	0x00000000	TDM Mode Receive Operation Control Register
I2S_TDM_8CH_CLKDIV	0x0038	W	0x00000000	Clock Divider Register
I2S_TDM_8CH_VERSION	0x003C	W	0x013376F1	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.3 Detail Registers Description

I2S_TDM_8CH_TXCR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x3	TX_PATH_SEL3 TX Path Select 3 2'b00: Sdo3 output data from path0 2'b01: Sdo3 output data from path1 2'b10: Sdo3 output data from path2 2'b11: Sdo3 output data from path3 Note: When TDM mode, only path0 enable.

Bit	Attr	Reset Value	Description
28:27	RW	0x2	TX_PATH_SEL2 TX Path Select 2 2'b00: Sdo2 output data from path0 2'b01: Sdo2 output data from path1 2'b10: Sdo2 output data from path2 2'b11: Sdo2 output data from path3 Note: When TDM mode, only path0 enable.
26:25	RW	0x1	TX_PATH_SEL1 TX Path Select 1 2'b00: Sdo1 output data from path0 2'b01: Sdo1 output data from path1 2'b10: Sdo1 output data from path2 2'b11: Sdo1 output data from path3 Note: When TDM mode, only path0 enable.
24:23	RW	0x0	TX_PATH_SEL0 TX Path Select 0 2'b00: Sdo0 output data from path0 2'b01: Sdo0 output data from path1 2'b10: Sdo0 output data from path2 2'b11: Sdo0 output data from path3 Note: When TDM mode, only path0 enable.
22:17	RW	0x00	RCNT Can be written only when XFER[0] bit is 0. Only valid in I2S Right justified format and slave TX mode is selected. Start to transmit data RCNT sclk cycles after left channel valid. Note: Only function when TX TFS[1]=0.
16:15	RW	0x0	TCSR Transmit Channel Select Register 2'b00: Two channel 2'b01: Four channel 2'b10: Six channel 2'b11: Eight channel
14	RW	0x0	HWT Halfword Word Transform Can be written only when XFER[0] bit is 0. Only valid when VDW select 16bit data. 1'b0: 32 bit data valid from AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid from AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved
12	RW	0x0	SJM Store Justified Mode Can be written only when XFER[0] bit is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 0. Because if HWT is 1, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified

Bit	Attr	Reset Value	Description
11	RW	0x0	FBM First Bit Mode Can be written only when XFER[0] bit is 0. 1'b0: MSB 1'b1: LSB
10:9	RW	0x0	IBM I2S Bus Mode Can be written only when XFER[0] bit is 0. 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved
8:7	RW	0x0	PBM Can be written only when XFER[0] bit is 0. 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode Note: Function when TX TFS[1:0] is 1.
6:5	RW	0x0	TFS Can be written only when XFER[0] bit is 0. 2'b00: I2S format 2'b01: PCM format 2'b10: TDM format 0 (PCM mode) 2'b11: TDM format 1 (I2S mode)
4:0	RW	0x00	VDW Valid Data Width Can be written only when XFER[0] bit is 0. 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit …… 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

I2S_TDM_8CH_RXCR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:23	RW	0x3	RX_PATH_SEL3 Rx Path Select 3 2'b00: Path3 data from sdi0 2'b01: Path3 data from sdi1 2'b10: Path3 data from sdi2 2'b11: Path3 data from sdi3 Note: Inoperative at TDM mode.

Bit	Attr	Reset Value	Description
22:21	RW	0x2	RX_PATH_SEL2 Rx Path Select 2 2'b00: Path2 data from sdi0 2'b01: Path2 data from sdi1 2'b10: Path2 data from sdi2 2'b11: Path2 data from sdi3 Note: Inoperative at TDM mode.
20:19	RW	0x1	RX_PATH_SEL1 Rx Path Select 1 2'b00: Path1 data from sdi0 2'b01: Path1 data from sdi1 2'b10: Path1 data from sdi2 2'b11: Path1 data from sdi3 Note: Inoperative at TDM mode.
18:17	RW	0x0	RX_PATH_SEL0 Rx Path Select 0 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
16:15	RW	0x0	RCSR Receive Channel Select Register 2'b00: Two channel 2'b01: Four channel 2'b10: Six channel 2'b11: Eight channel
14	RW	0x0	HWT Halfword Word Transform Can be written only when XFER[1] bit is 0. Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved
12	RW	0x0	SJM Store Justified Mode Can be written only when XFER[1] bit is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 0. Because if HWT is 1, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
11	RW	0x0	FBM First Bit Mode Can be written only when XFER[1] bit is 0. 1'b0: MSB 1'b1: LSB

Bit	Attr	Reset Value	Description
10:9	RW	0x0	IBM I2S Bus Mode Can be written only when XFER[1] bit is 0. 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved
8:7	RW	0x0	PBM PCM Bus Mode Can be written only when XFER[1] bit is 0. 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
6:5	RW	0x0	TFS Transfer Format Select Can be written only when XFER[1] bit is 0. 2'b00: I2S format 2'b01: PCM format 2'b10: TDM format 0 (PCM mode) 2'b11: TDM format 1 (I2S mode)
4:0	RW	0x00	VDW Valid Data Width Can be written only when XFER[1] bit is 0. 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

I2S_TDM_8CH_CKR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	LRCK_COMMON TX and RX Common Use 2'b00/2'b11: Tx_lrck/rx_lrck are used as synchronous signal for TX /RX respectively. 2'b01: Only tx_lrck is used as synchronous signal for TX and RX. 2'b10: Only rx_lrck is used as synchronous signal for TX and RX.
27	RW	0x0	MSS Master/Slave Mode Select Can be written only when XFER[1] or XFER[0] bit is 0. 1'b0: Master mode (sclk output) 1'b1: Slave mode (sclk input)
26	RW	0x0	CKP Sclk Polarity Can be written only when XFER[1] or XFER[0] bit is 0. 1'b0: Sample data at posedge sclk and drive data at negedge sclk 1'b1: Sample data at negedge sclk and drive data at posedge sclk

Bit	Attr	Reset Value	Description
25	RW	0x0	RLP Receive Lrck Polarity Can be written only when XFER[1] or XFER[0] bit is 0. 1'b0: Normal polarity (I2S normal: Low for left channel, high for right channel I2S left/right just: High for left channel, low for right channel PCM start signal: High valid) 1'b1: Opposite polarity (I2S normal: High for left channel, low for right channel I2S left/right just: Low for left channel, high for right channel PCM start signal: Low valid)
24	RW	0x0	TLP Transmit Lrck Polarity Can be written only when XFER[1] or XFER[0] bit is 0. 1'b0: Normal polarity (I2S normal: Low for left channel, high for right channel I2S left/right just: High for left channel, low for right channel PCM start signal: High valid) 1'b1: Opposite polarity (I2S normal: High for left channel, low for right channel I2S left/right just: Low for left channel, high for right channel PCM start signal: Low valid)
23:16	RO	0x00	reserved
15:8	RW	0x00	RSD Receive Sclk Divider Can be written only when XFER[1] or XFER[0] bit is 0. 8'h00~8'h1e: Reserved 8'h1f~8'hff: Frequency of sclk = (receive sclk divider/2)*2*frequency of rx_lrck Note: Function when RX TFS[1:0] is 2'b00 or 2'b01.
7:0	RW	0x00	TSD Transmit Sclk Divider Can be written only when XFER[1] or XFER[0] bit is 0. 8'h00~8'h1e: Reserved 8'h1f~8'hff: Frequency of sclk = (Transmit sclk divider/2)*2*frequency of tx_lrck Note: Function when TX TFS[1:0] is 2'b00 or 2'b01.

I2S_TDM_8CH_TXFIFOLR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	TFL3 Transmit FIFO3 Level Contains the number of valid data entries in the transmit FIFO3.
17:12	RO	0x00	TFL2 Transmit FIFO2 Level Contains the number of valid data entries in the transmit FIFO2.
11:6	RO	0x00	TFL1 Transmit FIFO1 Level Contains the number of valid data entries in the transmit FIFO1.
5:0	RO	0x00	TFL0 Transmit FIFO0 Level Contains the number of valid data entries in the transmit FIFO0.

I2S_TDM_8CH_DMACR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	RDE Receive DMA Enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x00	RDL Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x00	reserved
8	RW	0x0	TDE Transmit DMA Enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=00;TX FIFO1 if CSR=01,TX FIFO2 if CSR=10,TX FIFO3 if CSR=11)is equal to or below this field value.

I2S_TDM_8CH_INTCR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x1f	RFT Receive FIFO Threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	RXOIC RX Overrun Interrupt Clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	RXOIE RX Overrun Interrupt Enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	RXFIE RX Full Interrupt Enable 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8:4	RW	0x00	TFT Transmit FIFO Threshold When the number of transmit FIFO entries is less than or equal to this threshold, the transmit FIFO empty interrupt is triggered.
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	TXUIC TX Underrun Interrupt Clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	TXUIE TX Underrun Interrupt Enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	TXEIE TX empty Interrupt Enable 1'b0: Disable 1'b1: Enable

I2S_TDM_8CH_INTSR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	RXOI RX Overrun Interrupt 1'b0: Inactive 1'b1: Active
16	RO	0x0	RXFI RX Full Interrupt 1'b0: Inactive 1'b1: Active
15:2	RO	0x0000	reserved
1	RO	0x0	TXUI TX Underrun Interrupt 1'b0: Inactive 1'b1: Active
0	RO	0x0	TXEI TX Empty Interrupt 1'b0: Inactive 1'b1: Active

I2S_TDM_8CH_XFER

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RXS RX Start Bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RW	0x0	TXS TX Transfer Start Bit 1'b0: Stop TX transfer 1'b1: Start TX transfer

I2S_TDM_8CH_CLR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	RXC RX Logic Clear This is a self-cleared bit. Write 1 to clear all receive logic.

Bit	Attr	Reset Value	Description
0	RW	0x0	TXC TX Logic Clear This is a self-cleared bit. Write 1 to clear all transmit logic.

I2S_TDM_8CH_TXDR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	TXDR Transmit FIFO Data Register When it is written, data are moved into the transmit FIFO.

I2S_TDM_8CH_RXDR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXDR Receive FIFO Data Register When the register is read, data in the receive FIFO is accessed.

I2S_TDM_8CH_RXFIFOLR

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	RFL3 Receive FIFO3 Level Contains the number of valid data entries in the receive FIFO3.
17:12	RO	0x00	RFL2 Receive FIFO2 Level Contains the number of valid data entries in the receive FIFO2.
11:6	RO	0x00	RFL1 Receive FIFO1 Level Contains the number of valid data entries in the receive FIFO1.
5:0	RO	0x00	RFL0 Receive FIFO0 Level Contains the number of valid data entries in the receive FIFO0.

I2S_TDM_8CH_TDM_TXCTRL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:18	RW	0x0	TX_TDM_FSYNC_WIDTH_SEL1 TDM Transfer Fsync Width Sel1 Can be written only when XFER[0] is 0. 3'b000: Single period of the sclk_tx 3'b001: 2 period of the sclk_tx n: n+1 period of the sclk_tx 3'b110: 7 period of the sclk_tx 3'b111: The width is equivalent to a channel block. Note: Function when TX TFS[1:0] is 2 or 3.
17	RW	0x0	TX_TDM_FSYNC_WIDTH_SEL0 TDM Transfer Fsync Width Sel0 Can be written only when XFER[0] is 0. 1'b0: 1/2 frame width. It should be set to an even number. 1'b1: Frame width.

Bit	Attr	Reset Value	Description
16:14	RW	0x0	TDM_TX_SHIFT_CTRL TDM Transfer Shift Ctrl Can be written only when XFER[0] is 0. 3'b000: PCM format 0: Normal mode, drive data on the second negedge of sclk_tx after rising edge of TX LRCK. I2S format 0: Normal mode 3'b001: PCM format 1: 1/2 cycle shift left, drive data on second posedge of sclk_tx after rising edge of TX LRCK. I2S format 1: Left justified mode 3'b010: PCM format 2: 1 cycle shift left, drive data on first negedge of sclk_tx after rising edge of TX LRCK. I2S format 2: Right justified mode 3'b011: PCM format 3: 3/2 cycle shift left, drive data on first posedge of sclk_tx after rising edge of TX LRCK. I2S format: Not supported 3'b100: PCM format 4: 2 cycle shift left, drive data aligned to the posedge of TX LRCK. I2S format: Not supported 3'b101~3'b111: Not supported Note: Function when TX TFS[1:0] is 2 or 3.
13:9	RW	0x00	TDM_TX_SLOT_BIT_WIDTH TDM Transfer Slot Bits Can be written only when XFER[0] is 0. 5'h00~5'h0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1f: 32bit Note: Function when TX TFS[1:0] is 2 or 3.
8:0	RW	0x000	TDM_TX_FRAME_WIDTH TDM Transfer Frame Width Can be written only when XFER[0] is 0. 9'h000~9'h01e: Reserved 9'h01f: 32bit 9'h020: 33bit 9'h021: 34bit 9'h022: 35bit ..... 9'h1ff: 512bit Note: Functional when TX TFS[1:0] is 2 or 3.

I2S_TDM_8CH_TDM_RXCTRL

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

Bit	Attr	Reset Value	Description
20:18	RW	0x0	RX_TDM_FSYNC_WIDTH_SEL1 TDM Receive Fsync Width Sel1 Can be written only when XFER[1] is 0. 3'b000: Single period of the sclk_rx 3'b001: 2 period of the sclk_rx n: n+1 period of the sclk_rx 3'b110: 7 period of the sclk_rx 3'b111: The width is equivalent to a channel block Note: Function when RX TFS[1:0] is 2 or 3.
17	RW	0x0	RX_TDM_FSYNC_WIDTH_SEL0 TDM Receive Fsync Width Sel0 Can be written only when XFER[1] is 0. 1'b0: 1/2 frame width. It should be set to an even number. 1'b1: Frame width
16:14	RW	0x0	TDM_RX_SHIFT_CTRL TDM Receive Shift Ctrl Can be written only when XFER[1] is 0. 3'b000: PCM format 0: Normal mode, sample data on the third posedge of sclk_rx after rising edge of RX LRCK. I2S format 0: Normal mode 3'b001: PCM format 1: 1/2 cycle shift left, sample data on second negedge of sclk_rx after rising edge of RX LRCK. I2S format 1: left justified mode 3'b010: PCM format 2: 1 cycle shift left, sample data on second posedge of sclk_rx after rising edge of RX LRCK. I2S format 2: Right justified mode 3'b011: PCM format 3: 3/2 cycle shift left, sample data on first negedge of sclk_rx after rising edge of RX LRCK. I2S format: Not supported 3'b100: PCM format 4: 2 cycle shift left, sample data on the first posedge of sclk_rx after rising edge of RX LRCK. I2S format: Not supported 3'b101~3'b111: Not supported Note: Function when RX TFS[1:0] is 2 or 3.
13:9	RW	0x00	TDM_RX_SLOT_BIT_WIDTH TDM Receive Slot Bits Can be written only when XFER[1] is 0. 5'h00~5'h0e: Reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ..... 5'h1f: 32bit Note: Function when RX TFS[1:0] is 2 or 3.

Bit	Attr	Reset Value	Description
8:0	RW	0x000	TDM_RX_FRAME_WIDTH TDM Receive Frame Width Can be written only when XFER[1] is 0. 9'h000~9'h01e: Reserved 9'h01f: 32bit 9'h020: 33bit 9'h021: 34bit 9'h022: 35bit ..... 9'h1ff: 512bit Note: Functional when RX TFS[1:0] is 2 or 3.

I2S_TDM_8CH_CLKDIV

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	RX_MDIV RX Mclk Divider Can be written only when XFER[1] bit is 0. mclk_rx divider = (mclk_rx/sclk_rx)-1. For example, if mclk_rx divider is 5, then the frequency of sclk_rx is mclk_rx/6.
7:0	RW	0x00	TX_MDIV TX Mclk Divider Can be written only when XFER[0] bit is 0. mclk_tx divider = (mclk_tx/sclk_tx)-1. For example, if mclk_tx divider is 5, then the frequency of sclk_tx is mclk_tx/6.

I2S_TDM_8CH_VERSION

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x013376f1	VER I2S Version

21.5 Interface Description

Three I2S controllers embed in the chip are I2S1, I2S2 and I2S3. The I2S1 is connected to three groups of IO interfaces. The I2S2/3 is connected to two groups of IO interfaces. The following table shows the I2S1 group 0 interface description.

Table 21-1 I2S1 Group 0 Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s1_mclkm0	I/O	I2S1_MCLK_M0/UART3_RTSn_M0/SCR_CLK/PCIE30X1_PERSTn_M2/GPIO1_A2_d	GRF_GPIO1A_IOMUX_L[10:8]=3'b001
i2s1_sclktxm0	I/O	I2S1_SCLK_TX_M0/UART3_CTSn_M0/SCR_IO/PCIE30X1_WAKEn_M2/ACODEC_DAC_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_L[14:12]=3'b001
i2s1_sclkrxm0	I/O	I2S1_SCLK_RX_M0/UART4_RX_M0/PDM_CLK1_M0/SPDIF_TX_M0/GPIO1_A4_d	GRF_GPIO1A_IOMUX_H[2:0]=3'b001
i2s1_lrcktxm0	I/O	I2S1_LRCK_TX_M0/UART4_RTSn_M0/SCR_RST/PCIE30X1_CLKREQn_M2/ACODEC_DAC_SYNC/GPIO1_A5_d	GRF_GPIO1A_IOMUX_H[6:4]=3'b001
i2s1_lrckrxm0	I/O	I2S1_LRCK_RX_M0/UART4_TX_M0/PDM_CLK0_M0/AUDIOPWM_ROUT_P/GPIO1_A6_d	GRF_GPIO1A_IOMUX_H[10:8]=3'b001
i2s1_sdo0m0	I	I2S1_SDO0_M0/UART4_CTSn_M0/SCR_DET/AUDIOPWM_ROUT_N/ACODEC_DAC_DATAL/GPIO1_A7_d	GRF_GPIO1A_IOMUX_H[14:12]=3'b001
i2s1_sdo1m0	O	I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0/PCIE20	GRF_GPIO1B_IOMUX_L[2:0]=3'b001

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s1_sdi3m0	I	_CLKREQn_M2/ACODEC_DAC_DATAR/GPIO1_B0_d	GRF_GPIO1B_IOMUX_L[2:0]=3'b010
i2s1_sdo2m0	O	I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEn_M2/ACODEC_ADC_SYNC/GPIO1_B1_d	GRF_GPIO1B_IOMUX_L[6:4]=3'b001
i2s1_sdi2m0	I		GRF_GPIO1B_IOMUX_L[6:4]=3'b010
i2s1_sdo3m0	O	I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTn_M2/GPIO1_B2_d	GRF_GPIO1B_IOMUX_L[10:8]=3'b001
i2s1_sdi1m0	I		GRF_GPIO1B_IOMUX_L[10:8]=3'b010
i2s1_sdi0m0	I	I2S1_SDI0_M0/PDM_SDI0_M0/GPIO1_B3_d	GRF_GPIO1B_IOMUX_L[14:12]=3'b001

The following table shows the I2S1 group 1 interface description.

Table 21-2 I2S1 Group 1 Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s1_mclkm1	I/O	CIF_D0/EBC_SDDO0/SDMMC2_D0_M0/I2S1_MCLK_M1/VOP_BT656_D0_M1/GPIO3_C6_d	GRF_GPIO3C_IOMUX_H[10:8]=3'b100
i2s1_sclktxm1	I/O	CIF_D1/EBC_SDDO1/SDMMC2_D1_M0/I2S1_SCLK_TX_M1/VOP_BT656_D1_M1/GPIO3_C7_d	GRF_GPIO3C_IOMUX_H[14:12]=3'b100
i2s1_lrcktxm1	I/O	CIF_D2/EBC_SDDO2/SDMMC2_D2_M0/I2S1_LRCK_TX_M1/VOP_BT656_D2_M1/GPIO3_D0_d	GRF_GPIO3D_IOMUX_L[2:0]=3'b011
i2s1_sdo0m1	I/O	CIF_D3/EBC_SDDO3/SDMMC2_D3_M0/I2S1_SDO0_M1/VOP_BT656_D3_M1/GPIO3_D1_d	GRF_GPIO3D_IOMUX_L[6:4]=3'b100
i2s1_sdi0m1	I/O	CIF_D4/EBC_SDDO4/SDMMC2_CMD_M0/I2S1_SDI0_M1/VOP_BT656_D4_M1/GPIO3_D2_d	GRF_GPIO3D_IOMUX_L[10:8]=3'b100
i2s1_sdi1m1	I	CIF_D5/EBC_SDDO5/SDMMC2_CLK_M0/I2S1_SDI1_M1/VOP_BT656_D5_M1/GPIO3_D3_d	GRF_GPIO3D_IOMUX_L[14:12]=3'b100
i2s1_sdi2m1	O	CIF_D6/EBC_SDDO6/SDMMC2_DET_M0/I2S1_SDI2_M1/VOP_BT656_D6_M1/GPIO3_D4_d	GRF_GPIO3D_IOMUX_H[2:0]=3'b011
i2s1_sdi3m1	I/O	CIF_D7/EBC_SDDO7/SDMMC2_PWREN_M0/I2S1_SDI3_M1/VOP_BT656_D7_M1/GPIO3_D5_d	GRF_GPIO3D_IOMUX_H[6:4]=3'b011
i2s1_sclkrxm1	I/O	ISP_FLASHTRIGOUT/EBC_SDCE0/GMAC1_TXEN_M1/SPI3_CS0_M0/I2S1_SCLK_RX_M1/GPIO4_A6_d	GRF_GPIO4A_IOMUX_H[10:8]=3'b101
i2s1_lrckrxm1	I/O	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1/SPI3_CS1_M0/I2S1_LRCK_RX_M1/GPIO4_A7_d	GRF_GPIO4A_IOMUX_H[14:12]=3'b101
i2s1_sdo1m1		CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1/SPI3_MISO_M0/I2S1_SDO1_M1/GPIO4_B0_d	GRF_GPIO4B_IOMUX_L[2:0]=3'b101
i2s1_sdo2m1		ISP_PRELIGHT_TRIG/EBC_SDCE3/GMAC1_RXDV_CRS_M1/I2S1_SDO2_M1/GPIO4_B1_d	GRF_GPIO4B_IOMUX_L[6:4]=3'b100
i2s1_sdo3m1		I2C2_SCL_M1/EBC_SDSHR/CAN2_TX_M0/I2S1_SDO3_M1/GPIO4_B5_d	GRF_GPIO4B_IOMUX_H[6:4]=3'b100

Table 21-3 I2S1 Group 2 Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s1_mclkm2	I/O	LCDC_D0/VOP_BT656_D0_M0/SPI0_MISO_M1/PCIE20_CLKREQn_M1/I2S1_MCLK_M2/GPIO2_D0_d	GRF_GPIO2D_IOMUX_L[2:0]=3'b101
i2s1_sclktxm2	I/O	LCDC_D1/VOP_BT656_D1_M0/SPI0_MOSI_M1/PCIE20_WAKEn_M1/I2S1_SCLK_TX_M2/GPIO2_D1_d	GRF_GPIO2D_IOMUX_L[6:4]=3'b101
i2s1_lrcktxm2	I/O	LCDC_D2/VOP_BT656_D2_M0/SPI0_CS0_M1/PCIE30X1_CLKREQn_M1/I2S1_LRCK_TX_M2/GPIO2_D2_d	GRF_GPIO2D_IOMUX_L[10:8]=3'b101
i2s1_sdi0m2	I	LCDC_D3/VOP_BT656_D3_M0/SPI0_CLK_M1/PCIE30X1_WAKEn_M1/I2S1_SDI0_M2/GPIO2_D3_d	GRF_GPIO2D_IOMUX_L[14:12]=3'b101
i2s1_sdi1m2	I	LCDC_D4/VOP_BT656_D4_M0/SPI2_CS1_M1/PCIE30X2_CLKREQn_M1/I2S1_SDI1_M2/GPIO2_D4_d	GRF_GPIO2D_IOMUX_H[2:0]=3'b101
i2s1_sdi2m2	I	LCDC_D5/VOP_BT656_D5_M0/SPI2_CS0_M1/PCIE30X2_WAKEn_M1/I2S1_SDI2_M2/GPIO2_D5_d	GRF_GPIO2D_IOMUX_H[6:4]=3'b101
i2s1_sdi3m2	I	LCDC_D6/VOP_BT656_D6_M0/SPI2_MOSI_M1/PCIE30X2_PERSTn_M1/I2S1_SDI3_M2/GPIO2_D6_d	GRF_GPIO2D_IOMUX_H[10:8]=3'b101
i2s1_sdo0m2	O	LCDC_D7/VOP_BT656_D7_M0/SPI2_MISO_M1/UART8_TX_M1/I2S1_SDO0_M2/GPIO2_D7_d	GRF_GPIO2D_IOMUX_H[14:12]=3'b101
i2s1_sdo1m2	O	LCDC_CLK/VOP_BT656_CLK_M0/SPI2_CLK_M1/UART8_RX_M1/I2S1_SDO1_M2/GPIO3_A0_d	GRF_GPIO3A_IOMUX_L[2:0]=3'b101
i2s1_sdo2m2	O	LCDC_HSYNC/VOP_BT1120_D13/SPI1_MOSI_M1/PCIE20_PERSTn_M1/I2S1_SDO2_M2/GPIO3_C1_d	GRF_GPIO3C_IOMUX_L[6:4]=3'b101
i2s1_sdo3m2	O	LCDC_VSYNC/VOP_BT1120_D14/SPI1_MISO_M1/UART5_TX_M1/I2S1_SDO3_M2/GPIO3_C2_d	GRF_GPIO3C_IOMUX_L[10:8]=3'b101
i2s1_sclkrxm2	I/O	LCDC_DEN/VOP_BT1120_D15/SPI1_CLK_M1/UART5_RX_M1/I2S1_SCLK_RX_M2/GPIO3_C3_d	GRF_GPIO3C_IOMUX_L[14:12]=3'b101
i2s1_lrckrxm2	I/O	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	GRF_GPIO3C_IOMUX_L[6:4]=3'b101

The I2S2 is connected to two groups of IO interfaces. The following table shows the I2S2 group 0 interface description.

Table 21-3 I2S2 Group 0 Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s2_sclkrxm0	I/O	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	GRF_GPIO2B_IOMUX_H[14:12]=3'b001
i2s2_lrckrxm0	I/O	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	GRF_GPIO2C_IOMUX_L[2:0]=3'b001
i2s2_mclkm0	I/O	I2S2_MCLK_M0/ETH0_REFCLKO_25M/UART7_RTSn_M0/SPI2_CLK_M0/GPIO2_C1_d	GRF_GPIO2C_IOMUX_L[6:4]=3'b001
i2s2_sclktxm0	I/I	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	GRF_GPIO2C_IOMUX_L[10:8]=3'b001
i2s2_lrcktxm0	I/O	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	GRF_GPIO2C_IOMUX_L[14:12]=3'b001
i2s2_sdom0	O	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	GRF_GPIO2C_IOMUX_H[2:0]=3'b001
i2s2_sdim0	I	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	GRF_GPIO2C_IOMUX_H[6:4]=3'b001

Table 21-4 I2S2 Group 1 Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s2_lrcktxm1	I/O	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	GRF_GPIO4A_IOMUX_H[2:0]=3'b101
i2s2_lrckrxm1	I/O	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	GRF_GPIO4A_IOMUX_H[6:4]=3'b101
i2s2_sdim1	I	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1/SPI3_MOSI_M0/I2S2_SDI_M1/GPIO4_B2_d	GRF_GPIO4B_IOMUX_L[10:8]=3'b101
i2s2_sdom1	O	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1/SPI3_CLK_M0/I2S2_SDO_M1/GPIO4_B3_d	GRF_GPIO4B_IOMUX_L[14:12]=3'b101
i2s2_mclkm1	I/O	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTSn_M1/I2S2_MCLK_M1/GPIO4_B6_d	GRF_GPIO4B_IOMUX_H[10:8]=3'b101
i2s2_sclkrxm1	I/O	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1/UART1_CTSn_M1/I2S2_SCLK_RX_M1/GPIO4_C1_d	GRF_GPIO4C_IOMUX_L[6:4]=3'b101
i2s2_sclktxm1	I/O	CIF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1/I2S2_SCLK_TX_M1/GPIO4_B7_d	GRF_GPIO4B_IOMUX_H[14:12]=3'b100

The I2S3 is connected to two groups of IO interfaces. The following table shows the I2S3 group 0 interface description.

Table 21-5 I2S3 Group 0Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s3_mclkm0	I/O	LCDC_D9/VOP_BT1120_D1/GMAC1_TXD2_M0/I2S3_MCLK_M0/SDMMC2_D1_M1/GPIO3_A2_d	GRF_GPIO2A_IOMUX_L[2:0]=3'b001
i2s3_sclkm0	I/O	LCDC_D10/VOP_BT1120_D2/GMAC1_TXD3_M0/I2S3_SCLK_M0/SDMMC2_D2_M1/GPIO3_A3_d	GRF_GPIO3A_IOMUX_L[10:8]=3'b001
i2s3_lrckm0	I/O	LCDC_D11/VOP_BT1120_D3/GMAC1_RXD2_M0/I2S3_LRCK_M0/SDMMC2_D3_M1/GPIO3_A4_d	GRF_GPIO3A_IOMUX_H[14:12]=3'b001
i2s3_sdom0	O	LCDC_D12/VOP_BT1120_D4/GMAC1_RXD3_M0/I2S3_SDO_M0/SDMMC2_CMD_M1/GPIO3_A5_d	GRF_GPIO3A_IOMUX_H[6:4]=3'b001
i2s3_sdim0	I	LCDC_D13/VOP_BT1120_CLK/GMAC1_TXCLK_M0/I2S3_SDI_M0/SDMMC2_CLK_M1/GPIO3_A6_d	GRF_GPIO3A_IOMUX_H[2:0]=3'b001

Table 21-6 I2S3 Group 1Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
i2s3_mclkm1	I/O	PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	GRF_GPIO4C_IOMUX_L[10:8]=3'b101
i2s3_sclkm1	I/O	PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	GRF_GPIO4C_IOMUX_L[14:12]=3'b101
i2s3_lrckm1	I/O	EDP_DP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	GRF_GPIO4C_IOMUX_H[2:0]=3'b101
i2s3_sdom1	O	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	GRF_GPIO4C_IOMUX_H[6:4]=3'b101
i2s3_sdim1	I	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	GRF_GPIO4C_IOMUX_H[10:8]=3'b101

21.6 Application Notes

21.6.1 Software Application Notes

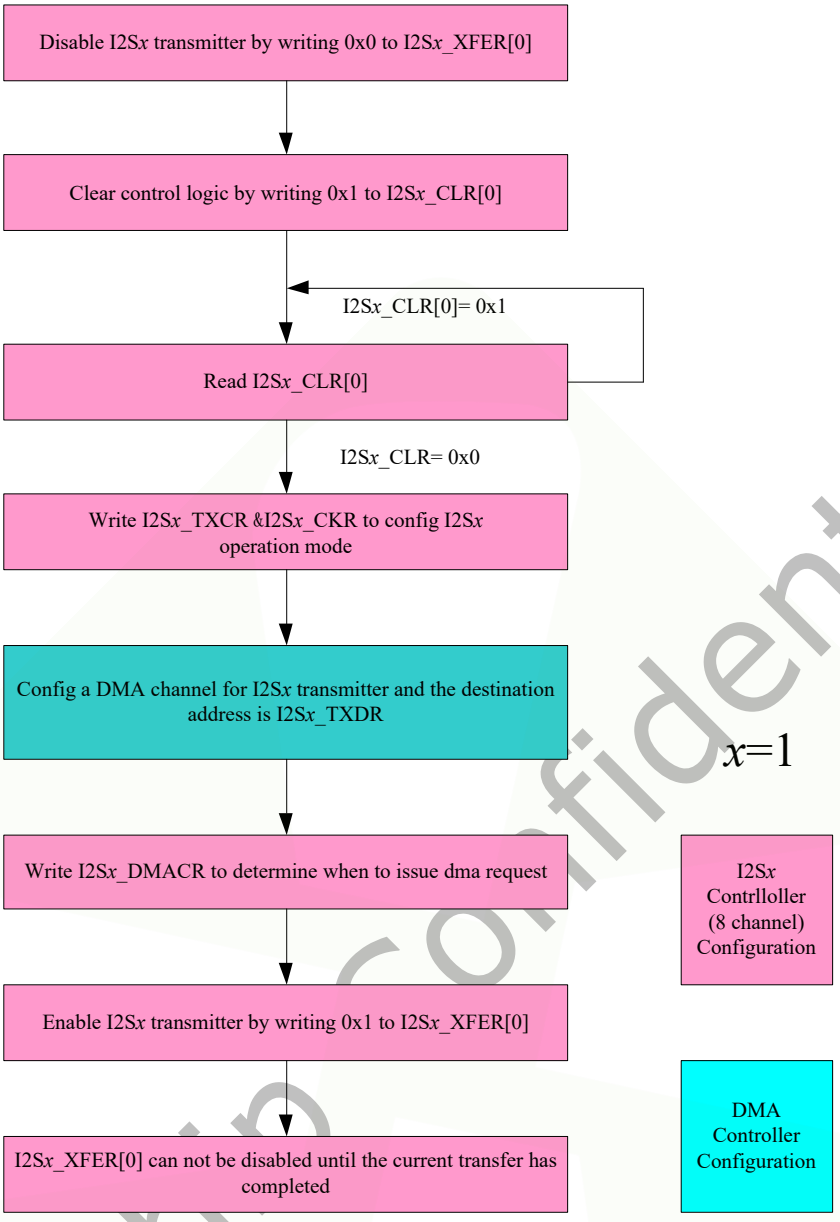


Fig.21-20 I2S/PCM/TDM Controller Transmit Operation Flow Chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

Chapter 22 I2C Interface

22.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 6 independent I2C: I2C0, I2C1, I2C2, I2C3,I2C4,I2C5
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Supports master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Supports 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

22.2 Block Diagram

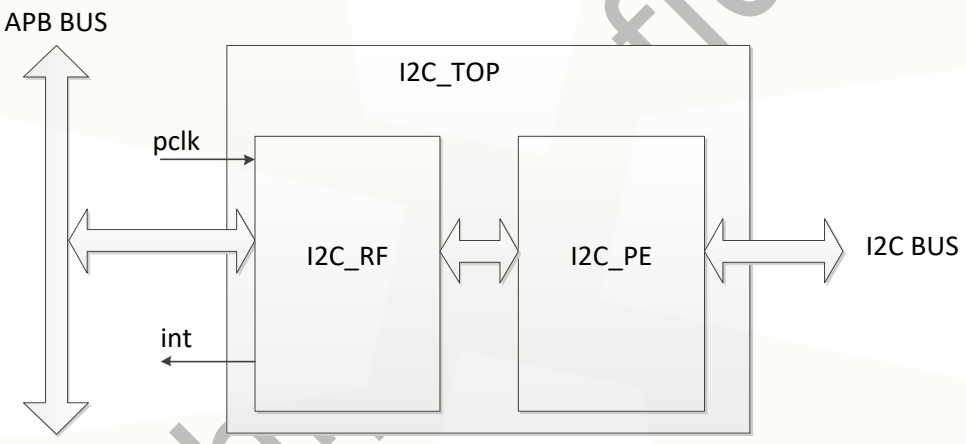


Fig.22-1 I2C architecture

22.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The CSR component operates synchronously with the pclk clock.

22.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the pclk.

22.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

22.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.

The I2C controller supports only Masterfunction. Itsupports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.

The operations of I2C controller is divided to 2 parts and described separately: initialization

and master mode programming.

22.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock as the working clock so the APB clock will determine the I2C bus clock. The correct register setting is subject to the system requirement.

22.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1)
  SCL = PCLK/ SCLK Divisor

- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data， CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command

- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01,the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.
  - When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
  - When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR . After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.

- Read/Write Command
  - When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.

- In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
- In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

- Master Interrupt Condition

There are 7 interrupt bits in I2C_ISR register related to master mode.

- Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
- Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
- MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
- MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
- Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
- Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
- NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.

- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity

The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

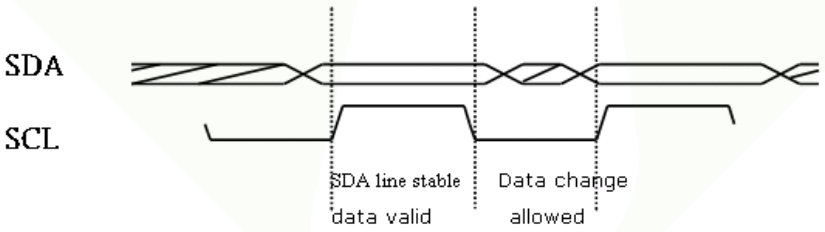


Fig.22-2I2C DATA Validity

    - START and STOP conditions

START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

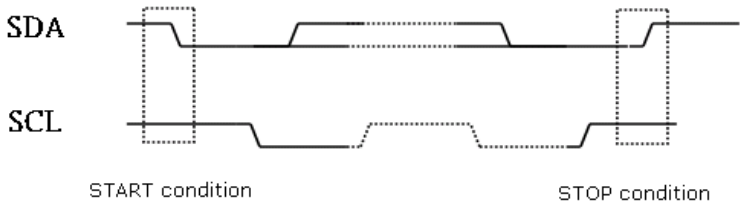


Fig.22-3 I2C Start and stop conditions

- Data transfer
  - Acknowledge

After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means “ACK”, on the contrary, it’s “NOT ACK”.

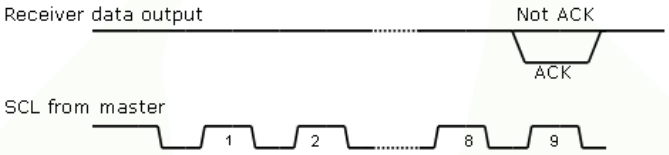


Fig.22-4 I2C Acknowledge

  - Byte transfer

The master own I2C bus might initiate multi byte to transfer to a slave.The transfer starts from a “START” command and ends in a “STOP”command. After every byte transfer, the receiver must reply an ACK to transmitter.

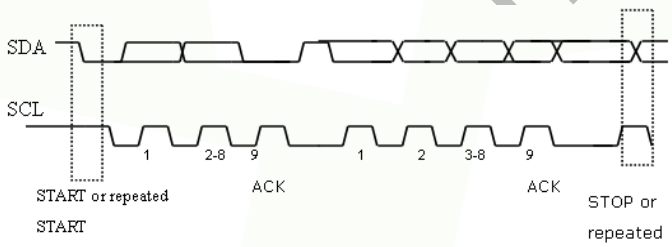


Fig.22-5 I2C byte transfer

22.4 Register Description

22.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI2C_CON	0x0000	W	0x00030000	control register
RKI2C_CLKDIV	0x0004	W	0x00000001	clock divider register，I2C CLK = PCLK / (16*CLKDIV)
RKI2C_MRXADDR	0x0008	W	0x00000000	the slave address accessed for master rx mode
RKI2C_MRXRADDR	0x000c	W	0x00000000	the slave register address accessed for master rx mode
RKI2C_MTXCNT	0x0010	W	0x00000000	master transmit count.specify the total bytes to be transmit (0~32)
RKI2C_MRXCNT	0x0014	W	0x00000000	master rx count.specify the total bytes to be recieved(0~32)
RKI2C_IEN	0x0018	W	0x00000000	interrupt enable register
RKI2C_IPD	0x001c	W	0x00000000	interrupt pending register
RKI2C_FCNT	0x0020	W	0x00000000	finished count: the count of data which has been transmitted or receivedfor debug purpose
RKI2C_SCL_OE_DB	0x0024	W	0x00000020	slave hold debounce configure register
RKI2C_TXDATA0	0x0100	W	0x00000000	I2C tx data register 0
RKI2C_TXDATA1	0x0104	W	0x00000000	I2C tx data register 1
RKI2C_TXDATA2	0x0108	W	0x00000000	I2C tx data register 2
RKI2C_TXDATA3	0x010c	W	0x00000000	I2C tx data register 3
RKI2C_TXDATA4	0x0110	W	0x00000000	I2C tx data register 4
RKI2C_TXDATA5	0x0114	W	0x00000000	I2C tx data register 5
RKI2C_TXDATA6	0x0118	W	0x00000000	I2C tx data register 6
RKI2C_TXDATA7	0x011c	W	0x00000000	I2C tx data register 7
RKI2C_RXDATA0	0x0200	W	0x00000000	I2C rx data register 0
RKI2C_RXDATA1	0x0204	W	0x00000000	I2C rx data register 1
RKI2C_RXDATA2	0x0208	W	0x00000000	I2C rx data register 2
RKI2C_RXDATA3	0x020c	W	0x00000000	I2C rx data register 3
RKI2C_RXDATA4	0x0210	W	0x00000000	I2C rx data register 4
RKI2C_RXDATA5	0x0214	W	0x00000000	I2C rx data register 5
RKI2C_RXDATA6	0x0218	W	0x00000000	I2C rx data register 6
RKI2C_RXDATA7	0x021c	W	0x00000000	I2C rx data register 7
RKI2C_ST	0x0220	W	0x00000000	status debug register
RKI2C_DBGCTRL	0x0224	W	0x00000000	Debug config register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

22.4.2 Detail Register Description

RKI2C_CON

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0003	version rki2c version information
15:14	RW	0x0	stop_setup stop setup config: TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c
13:12	RW	0x0	start_setup start setup config: TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c
11	RO	0x0	reserved
10:8	RW	0x0	data_upd_st SDA update point config: Used to config sda change state when scl is low, used to adjust setup/hold time 4'bn: Thold = (n + 1) * Tclk_i2c Note: 0 <= n <= 5
7	RO	0x0	reserved
6	RW	0x0	act2nak operation when NAK handshake is received: 1'b0: ignored 1'b1: stop transaction
5	RW	0x0	ack last byte acknowledge control in master receive mode: 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop stop enable, when this bit is written to 1, I2C will generate stop signal.
3	RW	0x0	start start enable, when this bit is written to 1, I2C will generate start signal.
2:1	RW	0x0	i2c_mode i2c mode select: 2'b00: transmit only 2'b01: transmit address (device + register address) --> restart --> transmit address -> receive only 2'b10: receive only 2'b11: transmit address (device + register address, write/read bit is 1) --> restart --> transmit address (device address) --> receive data

Bit	Attr	Reset Value	Description
0	RW	0x0	i2c_en i2c module enable: 1'b0: not enable 1'b1: enable

RKI2C_CLKDIV

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH scl high level clock count: T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8
15:0	RW	0x0001	CLKDIVL scl low level clock count: T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8

RKI2C_MRXADDR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	addhvld address high byte valid: 1'b0: invalid 1'b1: valid
25	RW	0x0	addmvld address middle byte valid: 1'b0: invalid 1'b1: valid
24	RW	0x0	addlvld address low byte valid: 1'b0: invalid 1'b1: valid
23:0	RW	0x000000	saddr master address register. the lowest bit indicate write or read 24 bits address register

RKI2C_MRXRADDR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	sraddhvld address high byte valid: 1'b0: invalid 1'b1: valid

Bit	Attr	Reset Value	Description
25	RW	0x0	sraddmvld address middle byte valid: 1'b0: invalid 1'b1: valid
24	RW	0x0	sraddlvld address low byte valid: 1'b0: invalid 1'b1: valid
23:0	RW	0x000000	sraddr slave register address accessed. 24 bits register address

RKI2C_MTXCNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	mtxcnt master transmit count. 6 bits counter

RKI2C_MRXCNT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	mrxcnt master rx count. 6 bits counter

RKI2C_IEN

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	slavehdsclen slave hold scl interrupt enable: 1'b0: disable 1'b1: enable
6	RW	0x0	nakrcvien NAK handshake received interrupt enable: 1'b0: disable 1'b1: enable
5	RW	0x0	stopien stop operation finished interrupt enable: 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
4	RW	0x0	startien start operation finished interrupt enable: 1'b0: disable 1'b1: enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable: 1'b0: disable 1'b1: enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable: 1'b0: disable 1'b1: enable
1	RW	0x0	brfien byte rx finished interrupt enable: 1'b0: disable 1'b1: enable
0	RW	0x0	btfien byte tx finished interrupt enable: 1'b0: disable 1'b1: enable

RKI2C_IPD

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	slavehdsclipd slave hold scl interrupt pending bit: 1'b0: no interrupt available 1'b1: slave hold scl interrupt appear, write 1 to clear
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit: 1'b0: no interrupt available 1'b1: NAK handshake received interrupt appear, write 1 to clear
5	W1C	0x0	stopipd stop operation finished interrupt pending bit: 1'b0: no interrupt available 1'b1: stop operation finished interrupt appear, write 1 to clear
4	W1C	0x0	startipd start operation finished interrupt pending bit: 1'b0: no interrupt available 1'b1: start operation finished interrupt appear, write 1 to clear

Bit	Attr	Reset Value	Description
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit: 1'b0: no interrupt available 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit: 1'b0: no interrupt available 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear
1	W1C	0x0	brfipd byte rx finished interrupt pending bit: 1'b0: no interrupt available 1'b1: byte rx finished interrupt appear, write 1 to clear
0	W1C	0x0	btfipd byte tx finished interrupt pending bit: 1'b0: no interrupt available 1'b1: byte tx finished interrupt appear, write 1 to clear

RKI2C_FCNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	fcnt the count of data which has been transmitted or received for debug purpose

RKI2C_SCL_OE_DB

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x20	scl_oe_db slave hold scl debounce. cycles for debounce (unit: Tclk_i2c)

RKI2C_TXDATA0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 data0 to be transmitted. 32 bits data

RKI2C_TXDATA1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 data1 to be transmitted. 32 bits data

RKI2C_TXDATA2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 data2 to be transmitted. 32 bits data

RKI2C_TXDATA3

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 data3 to be transmitted. 32 bits data

RKI2C_TXDATA4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 data4 to be transmitted. 32 bits data

RKI2C_TXDATA5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 data5 to be transmitted. 32 bits data

RKI2C_TXDATA6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 data6 to be transmitted. 32 bits data

RKI2C_TXDATA7

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 data7 to be transmitted. 32 bits data

RKI2C_RXDATA0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 data0 received. 32 bits data

RKI2C_RXDATA1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 data1 received. 32 bits data

RKI2C_RXDATA2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 data2 received. 32 bits data

RKI2C_RXDATA3

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 data3 received. 32 bits data

RKI2C_RXDATA4

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 data4 received. 32 bits data

RKI2C_RXDATA5

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 data5 received. 32 bits data

RKI2C_RXDATA6

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 data6 received. 32 bits data

RKI2C_RXDATA7

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 data7 received. 32 bits data

RKI2C_ST

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	scl_st scl status: 1'b0: scl status low 1'b0: scl status high
0	RO	0x0	sda_st sda status: 1'b0: sda status low 1'b0: sda status high

RKI2C_DBGCTRL

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7).
13	RW	0x0	nak_release_scl 1'b0: Hold scl as low when recieved nack 1'b1: Release scl as high when recieved nack

Bit	Attr	Reset Value	Description
12	RW	0x0	flt_en SCL edage glitch filter enable 1'b0: disable 1'b1: enable
11:8	RW	0x0	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c

22.5 Interface Description

Table 22-1I2C Interface Description

Module pin	Dir.	Pin name	IOMUX
I2C0 Interface			
i2c0_sda	I/O	I2C0_SDA/GPIO0_B2_u	PMU_GRF_GPIO0B_IOMUX_L[10:8]=3'h1
i2c0_scl	I/O	I2C0_SCL/GPIO0_B1_u	PMU_GRF_GPIO0B_IOMUX_L[6:4]=3'h1
I2C1 Interface			
i2c1_sda	I/O	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	PMU_GRF_GPIO0B_IOMUX_H[2:0]=3'h1
i2c1_scl	I/O	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B3_u	PMU_GRF_GPIO0B_IOMUX_L[14:12]=3'h1
I2C2 M0 Interface			
i2c2m0_sda	I/O	I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	PMU_GRF_GPIO0B_IOMUX_H[10:8]=3'h1
i2c2m0_scl	I/O	I2C2_SCL_M0/SPI0_CLK_M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	PMU_GRF_GPIO0B_IOMUX_H[6:4]=3'h1
I2C2 M1 Interface			
i2c2m1_sda	I/O	I2C2_SDA_M1/EBC_GDSP/CAN2_RX_M0/ISP_FLASH_TRIGIN/VOP_BT656_CLK_M1/GPIO4_B4_d	GRF_GPIO4B_IOMUX_H[2:0]=3'h1
i2c2m1_scl	I/O	I2C2_SCL_M1/EBC_SDSHR/CAN2_TX_M0/I2S1_SDO3_M1/GPIO4_B5_d	GRF_GPIO4B_IOMUX_H[6:4]=3'h1
I2C3 M0 Interface			
i2c3m0_sda	I/O	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	GRF_GPIO1A_IOMUX_L[2:0]=3'h1
i2c3m0_scl	I/O	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	GRF_GPIO1A_IOMUX_L[6:4]=3'h1
I2C3 M1 Interface			
i2c3m1_sda	I/O	LCDC_D21/VOP_BT1120_D12/GMAC1_TXD1_M0/I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d	GRF_GPIO3B_IOMUX_H[10:8]=3'h4

i2c3m1_scl	I/O	LCDC_D20/VOP_BT1120_D11/GMAC1_TXD0_M0/I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d	GRF_GPIO3B_IOMUX_H[6:4]=3'h4
I2C4 M0 Interface			
i2c4m0_sda	I/O	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1/SPI3_MOSI_M0/I2S2_SDI_M1/GPIO4_B2_d	GRF_GPIO4B_IOMUX_L[10:8]=3'h1
i2c4m0_scl	I/O	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1/SPI3_CLK_M0/I2S2_SDO_M1/GPIO4_B3_d	GRF_GPIO4B_IOMUX_L[14:12]=3'h1
I2C4 M1 Interface			
i2c4m1_sda	I/O	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	GRF_GPIO2B_IOMUX_L[6:4]=3'h2
i2c4m1_scl	I/O	SDMMC1_DET/I2C4_SCL_M1/UART8_CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	GRF_GPIO2B_IOMUX_L[10:8]=3'h2
I2C5 M0 Interface			
i2c5m0_sda	I/O	LCDC_D19/VOP_BT1120_D10/GMAC1_RXER_M0/I2C5_SDA_M0/PDM_SDI1_M2/GPIO3_B4_d	GRF_GPIO3B_IOMUX_H[2:0]=3'h4
i2c5m0_scl	I/O	LCDC_D18/VOP_BT1120_D9/GMAC1_RXDV_CRS_M0/I2C5_SCL_M0/PDM_SDI0_M2/GPIO3_B3_d	GRF_GPIO3B_IOMUX_L[14:12]=3'h4
I2C5 M1 Interface			
i2c5m1_sda	I/O	HDMITX_SDA/I2C5_SDA_M1/GPIO4_D0_u	GRF_GPIO4D_IOMUX_L[2:0]=3'h2
i2c5m1_scl	I/O	HDMITX_SCL/I2C5_SCL_M1/GPIO4_C7_u	GRF_GPIO4C_IOMUX_H[14:12]=3'h2

The I/O interface of I2C3 can be chosen by setting GRF_SOC_CON5[4] bit, if this bit is set to 1, I2C3 uses the I2C3m1 I/O interface, if those bit is set to 0, I2C3 uses the I2C3m0 I/O interface.

22.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow

- Transmit only mode (I2C_CON[1:0]=2’b00)

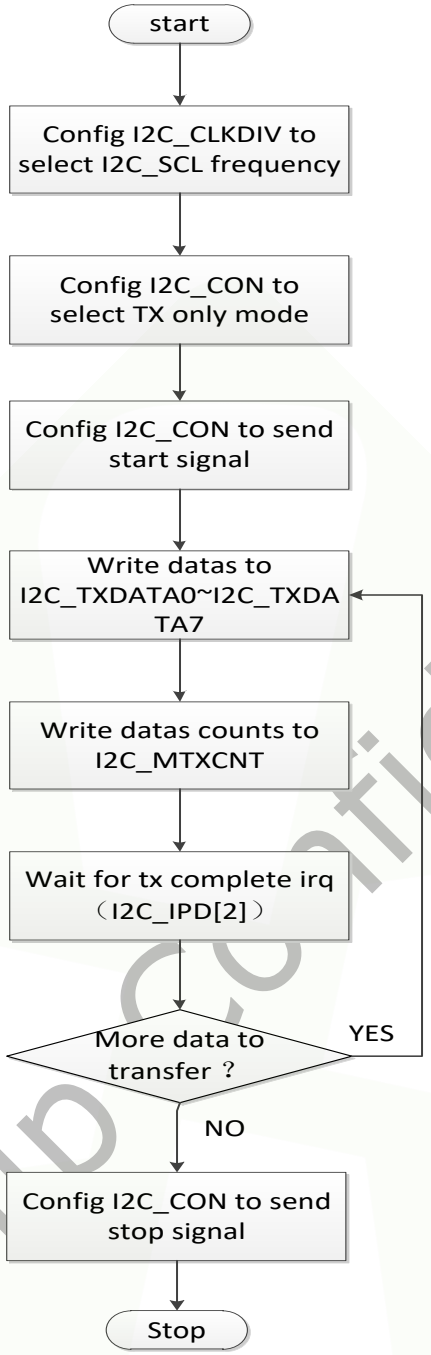


Fig.22-6 I2C Flow chat for transmit only mode

- Receive only mode (I2C_CON[1:0]=2'b10)

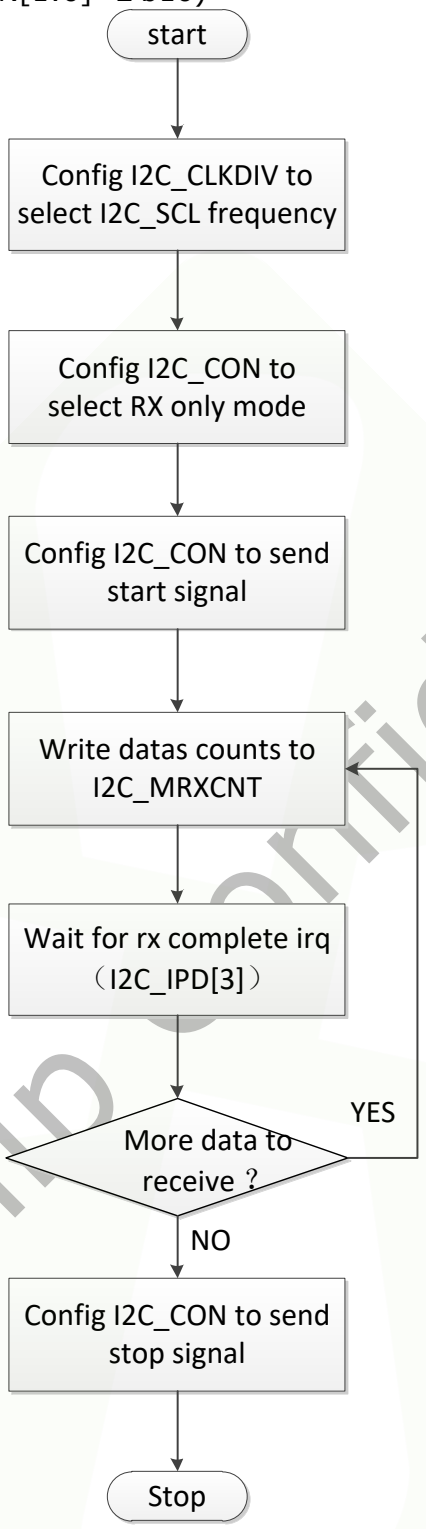


Fig.22-7 I2C Flow chat for receive only mode

- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

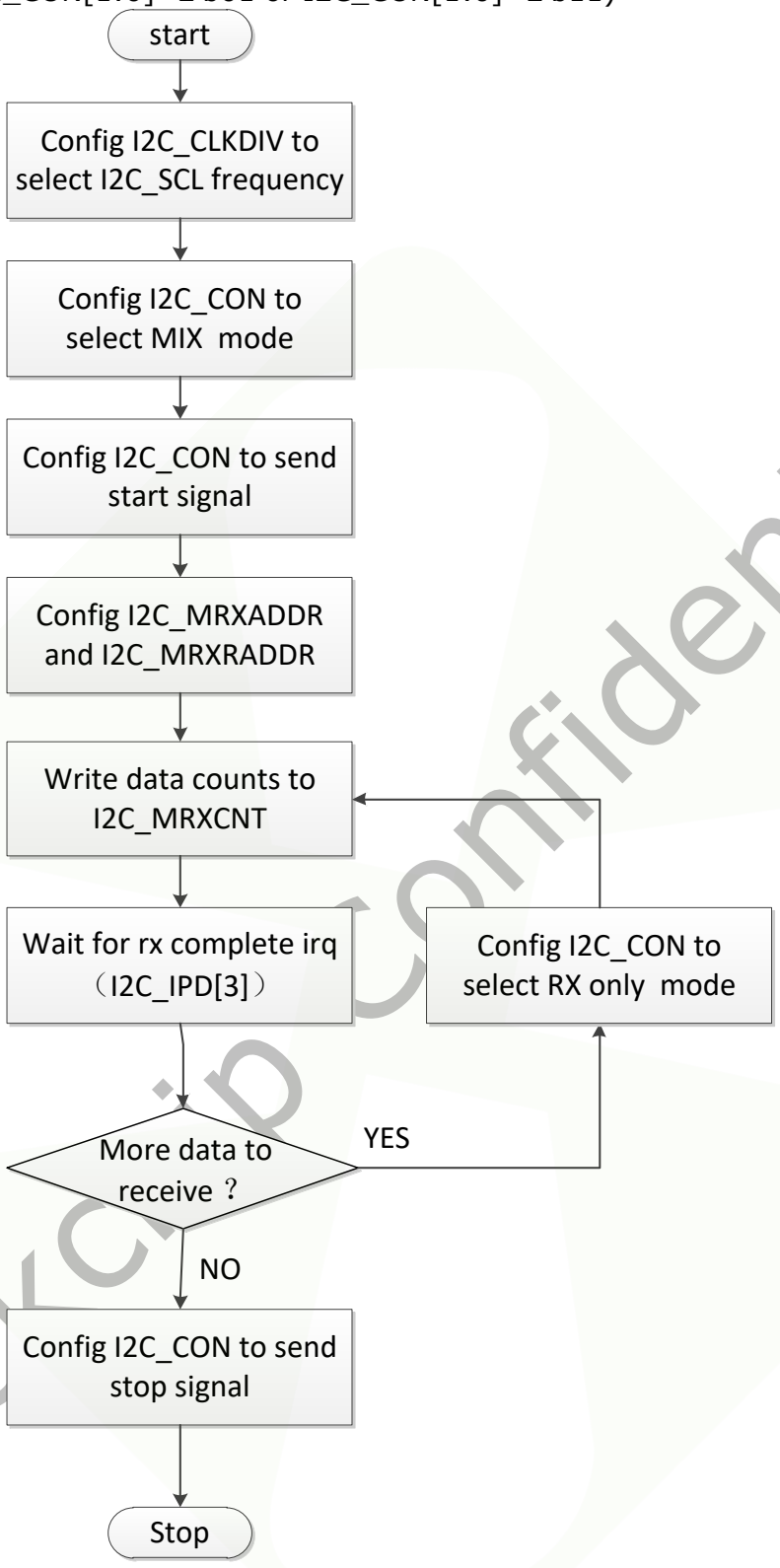


Fig.22-8 I2C Flow chat for mix mode

Chapter 23 Digital Audio Codec

23.1 Overview

Digital Audio Codec is a 24-bit digital audio encoder/decoder which supports multiple sample rates. It is mainly composed of digital ADC and digital DAC. The function of digital ADC is to convert pulse density modulation format data into PCM format audio data through a series of filters and volume control. Decoding result of digital ADC is sent out through I2S/PCM interface. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation. Finally the modulated result is sent to Analog Codec.

The Digital Audio Codec supports the following features.

- Support 8-bit APB bus slave interface
- Support 3-channel digital ADC
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 4-channel audio transmitting in I2S mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio transmitting or receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16~24 bit sample resolution for both digital ADC and digital DAC
- Support programmable left and right channel exchangeable in I2S mode and PCM mode for both digital ADC and digital DAC
- Support three modes of mixing for every digital DAC channel
- Both digital ADC and digital DAC support three groups of sample rates. Group 0 are 8kHz/16kHz/32kHz/64kHz/128kHz, group 1 are 11.025kHz/22.05kHz/44.1kHz/88.2kHz/176.4kHz and group 2 are 12kHz/24kHz/48kHz/96kHz/192kHz
- Support asynchronous mode and synchronous mode
- In asynchronous mode, there are no constraints on the sample rate of digital ADC and digital DAC. They are completely independent
- In synchronous mode, support digital ADC or digital DAC operating individually. The sample rate of digital ADC and digital DAC can be within any groups and any kind within one group
- In synchronous mode, support digital ADC and digital DAC operating at the same time within same sample rate group. Sample rates of digital ADC and digital DAC are within the same group
- In synchronous mode, support digital ADC and digital DAC operating at the same time within different sample rate group. Sample rate of digital ADC is within group 0 and digital DAC is within group 2 or digital ADC is within group 2 and digital DAC is within group 0, group 1 not supported
- The pass-band of digital ADC filters is 0.45625*fs
- Support digital ADC pass-band ripple within +/-0.1dB
- The stop-band of digital ADC filters is 0.5*fs
- Support digital ADC stop-band attenuation at least 60dB
- Support volume control for both digital ADC and digital DAC
- Support Automatic Level Control(ALC)and noise gate for digital ADC
- Support programmable negative and positive volume gain for both digital ADC and digital DAC
- Support communication with Analog Codec through I2C bus

23.2 Block Diagram

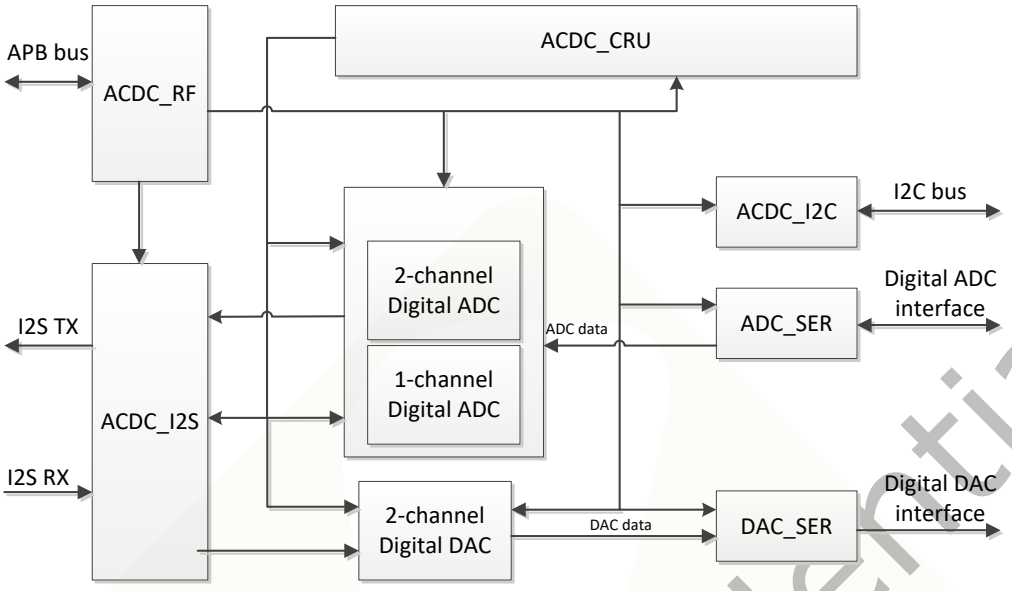


Fig.23-1 Digital Audio Codec Block Diagram

ACDC_RF

The ACDC_RF implements the 8-bit APB slave operation through APB bus. It is responsible for configuring the operation registers of other modules.

ACDC_CRU

The ACDC_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital ADC/DAC operation clock and I2S operation clock.

Digital ADC

There are 3 digital ADC channels in total inside Digital Audio Codec. The 2-channel digital ADC is composed of left channel and right channel while the 1-channel digital ADC contains only one channel. The digital ADC receives three channels data from ADC_SER module. It includes CIC filters, compensation filters, low-pass decimation filters, high-pass filters and other audio signal processing related modules. The output of digital ADC is sent to the I2S module.

ADC_SER

This module receives serial data from analog ADC. It extracts three channels from input serial data and distributes them to the corresponding digital ADC channel.

Digital DAC

There are 2 digital DAC channels inside the Audio Codec. The digital DAC receives audio data from I2S RX. It includes one CIC filter, one high-pass filter, several low-pass decimation filters, modulator and other audio signal processing related modules. The output of digital DAC is sent to DAC_SER module and serialized before transmitting to analog DAC.

DAC_SER

This module receives parallel data from digital DAC. It then serializes the parallel data and sends it to analog DAC.

ACDC_I2S

The I2S/PCM audio interface can be configured to master mode or slave mode. In Master Mode, SCLK and LRCK are configured as output. In Slave Mode, SCLK and LRCK are configured as input. The ACDC_I2S module can operate in TX or RX mode. When in TX mode, it receives audio data from digital ADC and sends it out through I2S TX interface. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

ACDC_I2C

The ACDC_I2C module is used to communicate with analog ADC/DAC. It is responsible for sending 4-bit PGA gain codes for each channel to analog ADC/DAC every interval of time.

23.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S0 controller. Please

refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

23.3.1 Filters of Digital ADC

Digital Audio Codec receives 3 channels data such as DATA0, DATA1 and DATA2 from Analog Codec. DATA0 is connected to the left channel of 2-channel digital ADC, DATA1 is connected to the right channel of 2-channel digital ADC and DATA2 is connected to the 1-channel digital ADC.

In order to achieve PCM format audio data from DATA0, DATA1 and DATA2, a total of 8 filters for 2-channel digital ADC and 8 filters for 1-channel digital ADC are embedded. It includes a CIC decimation filter, a compensation filter, 4 half-band filters, a low-pass filter and a high-pass filter in 2-channel digital ADC or 1-channel digital ADC.

The CIC decimation filter achieves maximum 16-times decimation when in normal mode. It also can be programmed to 8-times in low power mode 1 or 4-times decimation in low power mode 2. When operates in low power mode 1 or 2, the operating clock of digital ADC can be reduced to half or quarter of the normal mode. The problem is that signal indicators will become worse and some sample rates not support in low power mode 1 or 2. So make sure that the CIC decimation filter works in 16-times decimation unless you don't care about signal indicators.

Compensation filter is connected in series following CIC filter. Its function is to reduce the ripple of CIC filter output. It can be software enabled or disabled.

The 4 half-band filters and a low-pass filter each perform 2-times decimation. That means a maximum of 32-times decimation can be achieved. Not all of these 5 decimation filters are working all the time. How many of them are needed to work depends on the sample rate. For example, in order to output a 192K sample rate signal, only one filter works, the rest of filters are idle.

The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the volume control.

The equivalent parameters of digital ADC filters are as follows.

Table 23-1 Equivalent Parameters of Digital ADC Filters

Parameter	Test condition	Min	Typ	Max	Unit
Pass-band	+/- 0.1dB	20	N/A	0.45625fs	Hz
Pass-band ripple	N/A	N/A	N/A	+/- 0.1	dB
Stop-band	N/A	0.5fs	N/A	N/A	Hz
Stop-band attenuation	f>0.5fs	60	N/A	N/A	dB

23.3.2 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

Audio processing of digital DAC is similar to that of digital ADC, which is almost the inverse process of digital ADC. The 2-channel digital DAC includes a high-pass filter and 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control, each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a third-order Sigma-Delta modulator.

23.3.3 Volume Control

PCM format data output from 3-channel digital ADC high-pass filters are fed into volume control module. The volume control module inside digital ADC contains several sub-modules such as noise gate, peak detect, frequency cross zero detect, ALC and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is

attenuated or amplified can be software programmed. The volume of each channel can be controlled separately. Each channel has an 8-bit register for volume control. For negative gain, 0xff corresponds to digital mute while 0x00 corresponds to 0dB. For positive gain, 0xff corresponds to maximum gain while 0x00 corresponds to 0dB.
As for digital DAC, output of high-pass filter is fed into volume control module. Similar to digital ADC, The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It also can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

23.3.4 I2C Interface

The role of I2C inside the Digital Audio Codec is to send 4-bit PGA gain codes for each digital ADC channel to Analog Codec every interval of time. The interval of time is software programmable and the unit is the sample rate of digital ADC. There are 12 bits PGA gain codes in total for 3-channeldigital ADC, requiring the I2C inside Digital Audio Codec to initiate a request to transmit two bytes when interval of time reaches. The I2C inside Digital Audio Codec can be enabled or disabled by software. Its output bus will multiplex with RKI2C2 controller.

23.4 Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
ACDCDIG_SYSCTRL0	0x0000	W	0x00000000	System Control Register
ACDCDIG_ADCVUCTL	0x0040	W	0x00000001	ADC Volume Control Register
ACDCDIG_ADCVUCTIME	0x0044	W	0x00000000	ADC Volume Control Time Limit Register
ACDCDIG_ADCDIGEN	0x0048	W	0x00000000	ADC Digital Enable Register
ACDCDIG_ADCCLKCTRL	0x004c	W	0x00000000	ADC Clock Control Register
ACDCDIG_ADCINT_DIV	0x0054	W	0x00000000	ADC Integer Clock Divider Register
ACDCDIG_ADCSCLKTXINT_DIV	0x006c	W	0x00000000	I2S SCLK TX Integer Divider Register
ACDCDIG_ADCCFG1	0x0084	W	0x00000000	ADC Configure Register 1
ACDCDIG_ADCVOLL0	0x0088	W	0x00000000	Volume of ADC Left Channel 0 Register
ACDCDIG_ADCVOLL1	0x008c	W	0x00000000	Volume of ADC Left Channel 2 Register
ACDCDIG_ADCVOLR0	0x0098	W	0x00000000	Volume of ADC right Channel 1 Register
ACDCDIG_ADCVOGP	0x00a8	W	0x00000000	ADC Volume Gain Polarity Register
ACDCDIG_ADCRVOLL0	0x00ac	W	0x000000ff	Internal Volume of ADC Left Channel 0 Register
ACDCDIG_ADCRVOLL1	0x00b0	W	0x00000000	Internal Volume of ADC Left Channel 2 Register

Name	Offset	Size	Reset Value	Description
ACDCDIG_ADCRVOLR0	0x00bc	W	0x000000ff	Internal Volume of ADC right Channel 1 Register
ACDCDIG_ADCALC0	0x00cc	W	0x00000000	Automatic Level Control Register 0
ACDCDIG_ADCALC1	0x00d0	W	0x00000000	Automatic Level Control Register 1
ACDCDIG_ADCALC2	0x00d4	W	0x00000000	Automatic Level Control Register 2
ACDCDIG_ADCNG	0x00d8	W	0x00000000	ADC Noise Gate Control Register
ACDCDIG_ADCNGST	0x00dc	W	0x00000000	ADC Noise Gate Status Register
ACDCDIG_ADCHPFEN	0x00e0	W	0x00000000	ADC High-pass Filter Enable Register
ACDCDIG_ADCHPFCF	0x00e4	W	0x00000000	ADC High-pass Control Register
ACDCDIG_ADCPGL0	0x00ec	W	0x00000000	PGA Gain of Left Channel 0
ACDCDIG_ADCPGL1	0x00f0	W	0x00000000	PGA Gain of Left Channel 2
ACDCDIG_ADCPGR0	0x00fc	W	0x00000000	PGA Gain of right Channel 1
ACDCDIG_ADCLILMT1	0x010c	W	0x00000000	PGA Gain Limiter Register 1
ACDCDIG_ADCLILMT2	0x0110	W	0x00000000	PGA Gain Limiter Register 2
ACDCDIG_ADCDMICNG1	0x0114	W	0x00000000	Limiter Noise Gate Register 1
ACDCDIG_ADCDMICNG2	0x0118	W	0x00000000	Limiter Noise Gate Register 2
ACDCDIG_DACVUCTL	0x0140	W	0x00000001	DAC Volume Control Register
ACDCDIG_DACVUCTIME	0x0144	W	0x00000000	DAC Volume Control Time Limit Register
ACDCDIG_DACDIGEN	0x0148	W	0x00000000	DAC Digital Enable Register
ACDCDIG_DACCLKCTRL	0x014c	W	0x00000000	DAC Clock Control Register
ACDCDIG_DACINT_DIV	0x0154	W	0x00000007	DAC Integer Clock Divider Register
ACDCDIG_DACSCLKRXINT_DIV	0x0160	W	0x0000001f	I2S SCLK RX Integer Divider Register
ACDCDIG_DACPWM_DIV	0x0164	W	0x00000003	PWM Mode Integer Divider Register
ACDCDIG_DACPWM_CTRL	0x0168	W	0x00000000	PWM Mode Control Register
ACDCDIG_DACCFG1	0x0184	W	0x00000000	DAC Configure Register 1
ACDCDIG_DACMUTE	0x0188	W	0x00000000	DAC Mute Control Register
ACDCDIG_DACMUTEST	0x018c	W	0x00000000	DAC Mute Status Register
ACDCDIG_DACVOLL0	0x0190	W	0x00000000	Volume of DAC Left Channel 0 Register
ACDCDIG_DACVOLR0	0x01a0	W	0x00000000	Volume of DAC right Channel 1 Register
ACDCDIG_DACVOGP	0x01b0	W	0x00000000	ADC Volume Gain Polarity Register
ACDCDIG_DACRVOLL0	0x01b4	W	0x000000ff	Internal Volume of DAC Left Channel 0 Register
ACDCDIG_DACRVOLR0	0x01c4	W	0x000000ff	Internal Volume of DAC right Channel 1 Register
ACDCDIG_DACLMT0	0x01d4	W	0x00000000	DAC Limiter Register 0
ACDCDIG_DACLMT1	0x01d8	W	0x00000000	DAC Limiter Register 1

Name	Offset	Size	Reset Value	Description
ACDCDIG_DACLMT2	0x01dc	W	0x00000000	DAC Limiter Register 2
ACDCDIG_DACMIXCTRLL	0x01e0	W	0x00000000	DAC Mixing Control Register Of Left Channels
ACDCDIG_DACMIXCTRLR	0x01e4	W	0x00000000	DAC Mixing Control Register Of right Channels
ACDCDIG_DACHPF	0x01e8	W	0x00000000	DAC High-pass Filter Control Register
ACDCDIG_I2C_FLT_CON0	0x0280	W	0x00000000	I2C Filter Control Register 0
ACDCDIG_I2C_FLT_CON1	0x0284	W	0x0000000f	I2C Filter Control Register 1
ACDCDIG_I2C_CON0	0x0288	W	0x00000000	I2C Control Register 0
ACDCDIG_I2C_CON1	0x028c	W	0x00000003	I2C Control Register 1
ACDCDIG_I2C_CLKDIVL0	0x0290	W	0x00000006	I2C Scl Low Level Divider Register 0
ACDCDIG_I2C_CLKDIVL1	0x0294	W	0x00000000	I2C Scl Low Level Divider Register 1
ACDCDIG_I2C_CLKDIVH0	0x0298	W	0x00000006	I2C Scl High Level Divider Register 0
ACDCDIG_I2C_CLKDIVH1	0x029c	W	0x00000000	I2C Scl High Level Divider Register 1
ACDCDIG_I2C_MAXCNT	0x02a0	W	0x00000080	I2C Master Transmit Count Register.
ACDCDIG_I2C_SCLOE_DB0	0x02a4	W	0x00000020	Slave Hold Debounce Configure Register 0
ACDCDIG_I2C_SCLOE_DB1	0x02a8	W	0x00000000	Slave Hold Debounce Configure Register 1
ACDCDIG_I2C_SCLOE_DB2	0x02ac	W	0x00000020	Slave Hold Debounce Configure Register 2
ACDCDIG_I2C_SCLOE_DB3	0x02b0	W	0x00000020	Slave Hold Debounce Configure Register 3
ACDCDIG_I2C_TMOUTL	0x02b4	W	0x0000001f	I2C Transmit Request Time Out Register 0
ACDCDIG_I2C_TMOUTH	0x02b8	W	0x00000000	I2C Transmit Request Time Out Register 1
ACDCDIG_I2C_DEV_ADDR	0x02bc	W	0x00000048	I2C Slave Device Address Register
ACDCDIG_I2C_REG_ADDR	0x02c0	W	0x00000028	Register Address of I2C Slave
ACDCDIG_I2C_STATUS	0x02c4	W	0x00000000	I2C Status Register
ACDCDIG_I2S_TXCR0	0x0300	W	0x0000000f	Transmit Operation Control Register 0
ACDCDIG_I2S_TXCR1	0x0304	W	0x00000000	Transmit Operation Control Register 1
ACDCDIG_I2S_TXCR2	0x0308	W	0x00000000	Transmit Operation Control Register 2
ACDCDIG_I2S_RXCR0	0x030c	W	0x00000001	Receive Operation Control Register 0
ACDCDIG_I2S_RXCR1	0x0310	W	0x00000000	Receive Operation Control Register 1
ACDCDIG_I2S_CKR0	0x0314	W	0x00000000	Clock Generation Register 0
ACDCDIG_I2S_CKR1	0x0318	W	0x00000000	Clock Generation Register 1
ACDCDIG_I2S_XFER	0x031c	W	0x00000000	Transfer Start Register
ACDCDIG_I2S_CLR	0x0320	W	0x00000000	SCLK Domain Logic Clear Register

Name	Offset	Size	Reset Value	Description
ACDCDIG_VERSION	0x0380	W	0x00000002	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.4.3 Detail Registers Description

ACDCDIG_SYSCTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sync_mode 1'b0: Asynchronous mode. Input operation clocks of Digital ADC and Digital ADC are asynchronous to each other. 1'b1: Synchronous mode. Digital ADC and Digital ADC internally share one common clock.
4	RW	0x0	clk_com_sel Selects the operation clock of Digital ADC or Digital DAC as common clock when Digital ADC and Digital DAC work in synchronous mode. Keep the default value when Digital ADC and Digital DAC work in asynchronous mode. 1'b0: Selects operation clock of Digital ADC 1'b1: Selects operation clock of Digital DAC
3	RW	0x0	glbcke Global enable for synchronization signal of both Digital ADC and DAC. It works well when Digital ADC and DAC operate in synchronous mode where the Digital ADC and DAC share the same d2a_adc_clk and d2a_adc_sync to communicate with Analog ADC/DAC. If Digital ADC and DAC operate in asynchronous mode meaning that they are independent, glbcke is ineffective. 1'b0: Disable 1'b1: Enable
2	RO	0x0	reserved
1	RW	0x0	sync_sel Selects the synchronization signal generated by Digital ADC or by Digital DAC that is connected to d2a_adc_sync to communicate with Analogy ADC/DAC. Make sure that sync_sel is set to 1'b0 when in synchronous mode. If in asynchronous mode, sync_sel should be set according to the following illustration. 1'b0: Synchronization signal generated by Digital ADC is connected to d2a_adc_sync. 1'b1: Synchronization signal generated by Digital DAC is connected to d2a_adc_sync.

ACDCDIG_ADCVUCTL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	adc_byps Digital ADC volume control bypass. 1'b0: ADC volume control enable 1'b1: ADC volume control bypass
1	RW	0x0	adcfade Digital ADC volume adjust mode. 1'b0: update to new volume immediately 1'b1: update volume as adczdt field describes

Bit	Attr	Reset Value	Description
0	RW	0x1	adczdt Digital ADC volume cross zero detect enable. It works when adc_byps is 1'b0 and adcfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

ACDCDIG_ADCVUCTIME

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	adcvuct Volume control time limit, valid only in fade cross zero mode. Time limit = adcvuct*(1/sample rate) Unit: sample rate

ACDCDIG_ADCDIGEN

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	adcglben Global enable of all Digital ADC channels. Only when adcglben and the enable signal corresponding to each Digital ADC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	adcen_l2 Digital ADC left channel 2 enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adcen_l0r1 Digital ADC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

ACDCDIG_ADCCLKCTRL

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	cic_ds_ratio CIC filter decimation ratio. 2'b00: 16 times decimation 2'b01: 8 times decimation other: 4 times decimation
5	RW	0x0	adc_cke Digital ADC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2stx_cke Clock enable of internal I2S TX channel. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
3	RW	0x0	cke_bclktx Clock enable of sclk_out_tx. 1'b0: Disable 1'b1: Enable
2	RW	0x0	filter_gate_en Filter gate enable. There are some filters in Digital ADC, they work depends on the sample rate. If any filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active. 1'b0: Don't gate filters' clock 1'b1: Gate filters' clock
1	RW	0x0	adc_sync_ena Enable of the synchronization signal generated by Digital ADC. Note that only when both glbcke and adc_sync_ena are equal to 1'b1, the synchronization signal of Digital ADC can be generated. 1'b0: Disable 1'b1: Enable
0	RW	0x0	adc_sync_status There is a counter to generate synchronization signal of Digital ADC. In order to ensure the integrity of synchronization signal, it is necessary to read back adc_sync_status to judge whether the counter stops working when adc_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital ADC is complete.

ACDCDIG_ADCINT_DIV

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	int_div_con Interger clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

ACDCDIG_ADCSCLKTXINT_DIV

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	scktxdiv Integer clock divider to generate sclk_out_tx when I2S TX works in master mode. It is ignored when in slave mode.

ACDCDIG_ADCCFG1

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:2	RW	0x0	adcsrt Sample rates of Digital ADC. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz 3'b011: 48kHz/44.1kHz 3'b100: 96kHz/88.2kHz/64kHz 3'b101~3'b111: 192kHz/176.4kHz/128kHz
1	RW	0x0	sig_scale_mode Signal scale mode select. 1'b0: CIC output the normal latitude. 1'b1: Scale the CIC output to half of the normal latitude and scale 2 times after high-pass filter.
0	RW	0x0	fir_com_bps FIR compensate filter bypass control. 1'b0: Not bypass 1'b1: Bypass

ACDCDIG_ADCVOLL0

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	adclv0 Volume of Digital ADC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_ADCVOLL1

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	adclv1 Volume of Digital ADC left channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_ADCVOLR0

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	adcrv0 Volume of Digital ADC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_ADCVOGP

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	volgpl2 Gain polarity for the volume of Digital ADC left channel 2. 1'b0: Negative gain 1'b1: Positive gain
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital ADC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital ADC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

ACDCDIG_ADCRVOLL0

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital ADC left channel 0.

ACDCDIG_ADCRVOLL1

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rvoll1 Internal real-time volume of Digital ADC left channel 2.

ACDCDIG_ADCRVOLR0

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital ADC right channel 1.

ACDCDIG_ADCALC0

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	alcl2 Automatic level control enable for Digital ADC left channel 2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	alcr1 Automatic level control enable for Digital ADC right channel 1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	alcl0 Automatic level control enable for Digital ADC left channel 0. 1'b0: Disable 1'b1: Enable

ACDCDIG_ADCALC1

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	alcarate ALC attack rate=sample rate/(8*power(2,alcarate)).
3:0	RW	0x0	alcrrate ALC release rate=sample rate/(8*power(2,alcrrate)).

ACDCDIG_ADCALC2

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	alcmax The highest threshold of ALC. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	alcmin The lowest threshold of ALC. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

ACDCDIG_ADCNG

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ngchl Noise gate channel. 1'b0: Individual channel(or) 1'b1: Both channel(and)
6	RW	0x0	ngen Noise gate enable. 1'b0: Noise gate disable 1'b1: Noise gate enable
5	RW	0x0	ngboost Noise gate boost. 1'b0: Normal noise gate 1'b1: Boost noise gate

Bit	Attr	Reset Value	Description
4:2	RW	0x0	nggate Noise gate threshold. If ngboost is 1'b0: 3'b000~3'b111: -63db~-84db, 3db/step If ngboost is 1'b1: 3'b000~3'b111: -33db~-54db, 3db/step
1:0	RW	0x0	ngdly Noise gate delay. The delay time before the noise gate attacks. 2'b00: 2048 samples 2'b01: 4096 samples 2'b10: 8192 samples 2'b11: 16384 samples

ACDCDIG_ADCNGST

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	ngstl2 Noise gates valid status of left channel 2. 1'b0: Not in NG status 1'b1: Now in NG status
0	RO	0x0	ngstl0r1 Noise gates valid status of left channel 0 and right channel 1. 1'b0: Not in NG status 1'b1: Now in NG status

ACDCDIG_ADCHPFEN

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	hpfen_l2 High-pass filter enable for left channel 2. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.
1	RW	0x0	hpfen_r1 High-pass filter enable for right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.
0	RW	0x0	hpfen_l0 High-pass filter enable for left channel 0. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

ACDCDIG_ADCHPFCF

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	hpfcf High-pass filter control. 2'b00: 3.79Hz 2'b01: 60Hz 2'b10: 243Hz 2'b11: 493Hz

ACDCDIG_ADCPGL0

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	pga_l0 PGA gain of left channel 0 for analogy ADC. Minimal gain: -18dB, maximum gain: 27dB, step: 3dB. The minimal gain corresponds to 4'b0000 and the maximum gain corresponds to 4'b1111.

ACDCDIG_ADCPGL1

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	pga_l1 PGA gain of left channel 2 for analogy ADC. Minimal gain: -18dB, maximum gain: 27dB, step: 3dB. The minimal gain corresponds to 4'b0000 and the maximum gain corresponds to 4'b1111.

ACDCDIG_ADCPGR0

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	pga_r0 PGA gain of right channel 1 for analogy ADC. Minimal gain: -18dB, maximum gain: 27dB, step: 3dB. The minimal gain corresponds to 4'b0000 and the maximum gain corresponds to 4'b1111.

ACDCDIG_ADCLILMT1

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	lmt_en PGA gain LIMITER enable. 1'b0: Disable 1'b1: Enable
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

ACDCDIG_ADCLILMT2

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

ACDCDIG_ADCDMICNG1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ngchl_li Noise gate channel. 1'b0: Individual channel(or) 1'b1: Both channel(and)
6	RW	0x0	ngen_li Noise gate enable. 1'b0: Noise gate disable 1'b1: Noise gate enable
5	RW	0x0	ngboost_li Noise gate boost. 1'b0: Normal noise gate 1'b1: Boost noise gate
4:2	RW	0x0	nggate_li Noise gate threshold. If ngboost is 1'b0: 3'b000~3'b111: -63db~-84db, 3db/step If ngboost is 1'b1: 3'b000~3'b111: -33db~-54db, 3db/step
1:0	RW	0x0	ngdly_li Noise gate delay. The delay time before the noise gate attacks. 2'b00: 2048 samples 2'b01: 4096 samples 2'b10: 8192 samples 2'b11: 16384 samples

ACDCDIG_ADCDMICNG2

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	ngvalid_li_l2 Noise gates valid status of Limiter for left channel 2. 1'b0: Not in NG status 1'b1: Now in NG status
0	RO	0x0	ngvalid_li_l0r1 Noise gates valid status of Limiter for left channel 0 and right channel 1. 1'b0: Not in NG status 1'b1: Now in NG status

ACDCDIG_DACVUCTL

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dac_byps Digital DAC volume control bypass. 1'b0: Digital DAC volume control enable 1'b1: Digital DAC volume control bypass

Bit	Attr	Reset Value	Description
1	RW	0x0	dacfade Digital DAC volume adjust mode. 1'b0: Update to new volume immediately. 1'b1: Update volume as daczdt field describes.
0	RW	0x1	daczdt Digital DAC volume cross zero detect enable. It works when adc_byps is 1'b0 and adcfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

ACDCDIG_DACVUCTIME

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacvuct Volume control time limit, valid only in fade cross zero mode. Time limit = dacvuct*(1/sample rate) Unit: sample rate

ACDCDIG_DACDIGEN

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	adcglben Global enable of all Digital DAC channels. Only when adcglben and the enable signal corresponding to each Digital DAC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	dacen_l0r1 Digital DAC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

ACDCDIG_DACCLKCTRL

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dac_cke Digital DAC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2srx_cke Clock enable of internal I2S RX channel. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cke_bclkrx Clock enable of sclk_out_rx. 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	dac_sync_ena Enable of the synchronization signal generated by Digital DAC. Note that only when both glbcke and dac_sync_ena are equal to 1'b1, the synchronization signal of Digital DAC can be generated. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dac_sync_status There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete.
0	RW	0x0	dac_mod_attenu_en When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB. 1'b0: Disable 1'b1: Enable

ACDCDIG_DACINT_DIV

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x07	int_div_con Interger clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

ACDCDIG_DACSCLKRXINT_DIV

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	sckrxdiv Interger clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode.

ACDCDIG_DACPWM_DIV

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	audio_pwm_div PWM mode division of Digital DAC's operation clock.

ACDCDIG_DACPWM_CTRL

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	pwm_mode_cke Clock enable of 1-bit PWM modulator 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
5:4	RW	0x0	pwm_mode Audio PWM mode or Audio DAC mode selection 2'b00: Audio DAC mode 2'b01: Audio PWM mode 0. The input of 1-bit PWM modulator is from the last filter of Audio DAC. 2'b01: Audio PWM mode 1. The input of 1-bit PWM modulator is directly from output of I2S RX inside the ACDCDIG.
3	RW	0x0	pwm_en 1-bit PWM modulator enable 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	dith_sel Dith mode selection of 1-bit PWM modulator

ACDCDIG_DACCFG1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x0	dacsrt Sample rates of Digital DAC. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz/48kHz/44.1kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100: 192kHz/176.4kHz/128kHz 3'b101~3'b111: Reserved

ACDCDIG_DACMUTE

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dacunmt 1'b0: DAC normal mode 1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*.
0	RW	0x0	dacmt 1'b0: DAC normal mode 1'b1: DAC mute mode

ACDCDIG_DACMUTEST

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	unmutest_l0r1 Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*. 1'b0: Unmute not done 1'b1: Unmute done
3:1	RO	0x0	reserved
0	RO	0x0	mutest_l0r1 Mute status for Digital DAC left channel 0 and right channel 1. 1'b0: Not mute 1'b1: Mute

ACDCDIG_DACVOLL0

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv0 Volume of Digital DAC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DACVOLR0

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacrv0 Volume of Digital DAC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

ACDCDIG_DACVOGP

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital DAC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital DAC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

ACDCDIG_DACRVOLL0

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital DAC left channel 0.

ACDCDIG_DACRVOLR0

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital DAC right channel 1.

ACDCDIG_DACLMT0

Address: Operational Base + offset (0x01d4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	limen LIMITER enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	limdct Limiter detect mode. 1'b0: (Left channel + right channel)/2 1'b0: Left channel or right channel independently

ACDCDIG_DACLMT1

Address: Operational Base + offset (0x01d8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

ACDCDIG_DACLMT2

Address: Operational Base + offset (0x01dc)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

ACDCDIG_DACMIXCTRLL

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_l0 Digital DAC left channel 0 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

ACDCDIG_DACMIXCTRLR

Address: Operational Base + offset (0x01e4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	mixmode_r0 Digital DAC right channel 1 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

ACDCDIG_DACHPF

Address: Operational Base + offset (0x01e8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	hpfcf High-pass filter control. 2'b00: 80Hz 2'b01: 100Hz 2'b10: 120Hz 2'b11: 140Hz
3:1	RO	0x0	reserved
0	RW	0x0	hpfen_l0r1 High-pass filter enable for left channel 0 and right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

ACDCDIG_I2C_FLT_CON0

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c.
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c.

ACDCDIG_I2C_FLT_CON1

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH.(SCL_HIGH including h0~h7)
5	RW	0x0	nak_release_scl 1'b0: Hold scl as low when received nack. 1'b1: Release scl as high when received nack.
4	RW	0x0	flt_en SCL edge glitch filter enable. 1'b0: Disable 1'b1: Enable
3:0	RW	0xf	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c.

ACDCDIG_I2C_CON0

Address: Operational Base + offset (0x0288)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	act2nak Operation when NAK handshake is received. 1'b0: Ignored 1'b1: Stop transaction
5:3	RO	0x0	reserved
2:1	RW	0x0	i2c_mode I2C mode select. 2'b00: Transmit only 2'b01~2'b11: Reserved
0	RW	0x0	i2c_en I2C enable. 1'b0: Not enable 1'b1: Enable

ACDCDIG_I2C_CON1

Address: Operational Base + offset (0x028c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	stop_setup Stop setup configure. TSU: sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c
5:4	RW	0x0	start_setup Start setup configure. TSU: sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c THD: sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c
3:0	RW	0x3	data_upd_st SDA update point configure. Used to configure sda change state when scl is low, used to adjust setup/hold time. 4'bn: Thold = (n + 1) * Tclk_i2c Note: 0 <= n <= 5

ACDCDIG_I2C_CLKDIVL0

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x06	clkdivl0 Low 8 bits of scl low level clock divider. The value of 16 bits scl low level clock divider updates only when clkdivl1 is programmed. So ensure to program clkdivl0 firstly, followed by clkdivl1.

ACDCDIG_I2C_CLKDIVL1

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clkdivl1 High 8 bits of scl low level clock divider. The value of 16 bits scl low level clock divider updates only when clkdivl1 is programmed. So ensure to program clkdivl0 firstly, followed by clkdivl1. T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8, where the CLKDIVL is equal to clkdivl0+clkdivl1*256.

ACDCDIG_I2C_CLKDIVH0

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x06	clkdivh0 Low 8 bits of scl high level clock divider. The value of 16 bits scl high level clock divider updates only when clkdivh1 is programmed. So ensure to program clkdivh0 firstly, followed by clkdivh1.

ACDCDIG_I2C_CLKDIVH1

Address: Operational Base + offset (0x029c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clkdivh1 High 8 bits of scl high level clock divider. The value of 16 bits scl high level clock divider updates only when clkdivh1 is programmed. So ensure to program clkdivh0 firstly, followed by clkdivh1. T(SCL_LOW) = Tclk_i2c * (CLKDIVH + 1) * 8, where the CLKDIVH is equal to clkdivh0+clkdivh1*256.

ACDCDIG_I2C_MAXCNT

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x1	idle 1'b0: I2C module is busy. 1'b1: I2C module is idle.
6	RO	0x0	reserved
5:0	RW	0x00	mtxcnt Master transmit number. Specify the total bytes to be transmitted (0~32).

ACDCDIG_I2C_SCLOE_DB0

Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scloedb0 Bit7~bit0 of slave hold scl debounce register. Cycles for debounce (unit: Tclk_i2c).

ACDCDIG_I2C_SCLOE_DB1

Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	scloedb1 Bit15~bit8 of slave hold scl debounce register. Cycles for debounce (unit: Tclk_i2c).

ACDCDIG_I2C_SCLOE_DB2

Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scloedb2 Bit23~bit16 of slave hold scl debounce register. Cycles for debounce (unit: Tclk_i2c).

ACDCDIG_I2C_SCLOE_DB3

Address: Operational Base + offset (0x02b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	scloedb3 Bit31~bit24 of slave hold scl debounce register. Cycles for debounce (unit: Tclk_i2c).

ACDCDIG_I2C_TMOUTL

Address: Operational Base + offset (0x02b4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	tmoutl Low 8 bits of 16 bits I2C transmit request time out register. The value of 16 bits I2C transmit request time out register updates only when tmouth is programmed. So ensure to program tmoutl firstly, followed by tmouth.

ACDCDIG_I2C_TMOUTH

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	tmouth High 8 bits of 16 bits I2C transmit request time out register. The value of 16 bits I2C transmit request time out register updates only when tmouth is programmed. So ensure to program tmoutl firstly, followed by tmouth.

ACDCDIG_I2C_DEV_ADDR

Address: Operational Base + offset (0x02bc)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x48	dev_addr I2C slave device address.

ACDCDIG_I2C_REG_ADDR

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x28	regaddr I2C slave register address to be accessed.

ACDCDIG_I2C_STATUS

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	slavehdsclst Slave hold scl status bit. 1'b0: Slave not hold scl. 1'b1: Slave hold scl, write 1'b1 to clear.
6	RO	0x0	nakrcvst NAK handshake received status bit. 1'b0: No NAK handshake received. 1'b1: NAK handshake received, write 1'b1 to clear.

Bit	Attr	Reset Value	Description
5	RO	0x0	stopst Stop operation finished status bit. 1'b0: No finished. 1'b1: Stop operation finished, write 1'b1 to clear.
4	RO	0x0	startst Start operation finished status bit. 1'b0: Not finished. 1'b1: Start operation finished, write 1'b1 to clear.
3	RO	0x0	reserved
2	RO	0x0	mbtfst I2C_MTXCNT data transfer finished status bit. 1'b0: Not finished. 1'b1: I2C_MTXCNT data transfer finished, write 1'b1 to clear.
1	RO	0x0	reserved
0	RO	0x0	btfst Byte tx finished status bit. 1'b0: Byte tx not finish. 1'b1: Byte tx finished, write 1'b1 to clear.

ACDCDIG_I2S_TXCR0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pbm 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x0f	vdw 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

ACDCDIG_I2S_TXCR1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	tcsr 2'b00: Two channel 2'b01: Four channel Others: Reserved
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	cex Exchange left channel and right channel in the every transmit line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm 1'b0: MSB 1'b1: LSB
1:0	RW	0x0	ibm 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

ACDCDIG_I2S_TXCR2

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rcnt Only valid in I2S Right justified format and slave tx mode is selected. Start to transmit data rcnt sclk cycles after left channel valid.

ACDCDIG_I2S_RXCR0

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	pbm 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x01	vdw 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

ACDCDIG_I2S_RXCR1

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rcsr 2'b00: Two channel Others: Reserved

Bit	Attr	Reset Value	Description
5	RO	0x0	reserved
4	RW	0x0	cex Exchange left channel and right channel in the every receive line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm 1'b0: MSB 1'b1: LSB
1:0	RW	0x0	ibm 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

ACDCDIG_I2S_CKR0

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	rsd I2S rx sclk divider for rx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256
1:0	RW	0x0	tsd I2S tx sclk divider for tx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256

ACDCDIG_I2S_CKR1

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	mss 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
2	RW	0x0	ckp 1'b0: Sample data at posedge sclk and drive data at negedge sclk. 1'b1: Sample data at negedge sclk and drive data at posedge sclk.
1	RW	0x0	rlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)

Bit	Attr	Reset Value	Description
0	RW	0x0	tlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)

ACDCDIG_I2S_XFER

Address: Operational Base + offset (0x031c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RW	0x0	txs 1'b0: Stop TX transfer 1'b1: Start TX transfer

ACDCDIG_I2S_CLR

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxc This is a self-cleared bit. Write 1 to clear all receive logic.
0	RW	0x0	txc This is a self-cleared bit. Write 1 to clear all transmit logic.

ACDCDIG_VERSION

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	ver Version of ACDCDIG.

23.4.4 Interface Description

Digital Audio Codec supports audio DAC mode and audio PWM mode. The following table shows the Digital Audio Codec interface description for audio DAC mode.

Table 23-2 Digital Audio Codec Interface Description for Audio DAC Mode

Module Pin	Dir.	Pad Name	IOMUX Setting
D2A_ADC_CLK	O	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	GRF_GPIO1A_IOMUX_L[6:4]=3'b101
D2A_ADC_SYNC	O	I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEn_M2/ACODEC_ADC_SYNC/GPIO1_B1_d	GRF_GPIO1B_IOMUX_L[6:4]=3'b101
A2D_ADC_DATA	I	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	GRF_GPIO1A_IOMUX_L[2:0]=3'b101
D2A_DAC_CLK	O	I2S1_SCLK_TX_M0/UART3_CTSn_M0/SCR_IO/PCIE30X1_WAKEn_M2/ACODEC_DAC_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_L[14:12]=3'b101
D2A_DAC_SYNC	O	I2S1_LRCK_TX_M0/UART4_RTSn_M0/SCR_RST/PCIE30X1_CLKREQn_M2/ACODEC_DAC_SYNC/GPIO1_A5_d	GRF_GPIO1A_IOMUX_H[6:4]=3'b101

Module Pin	Dir.	Pad Name	IOMUX Setting
D2A_DAC_DATA_L	O	I2S1_SDO0_M0/UART4_CTSn_M0/SCR_DET/AUDIOPWM_ROUT_N/ACODEC_DAC_DATAL/GPIO1_A7_d	GRF_GPIO1A_IOMUX_H[14:12]=3'b101
D2A_DAC_DATA_R	O	I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0/PCIE20_CLKREQn_M2/ACODEC_DAC_DATAR/GPIO1_B0_d	GRF_GPIO1B_IOMUX_L[2:0]=3'b101

When operating in audio PWM mode, Digital Audio Codec outputs two pairs of differential signals encoded in PWM format. The following table shows the Digital Audio Codec interface description for audio PWM mode.

Table 23-3 Digital Audio Codec Interface Description for Audio PWM Mode

Module Pin	Dir.	Pad Name	IOMUX Setting
AUDIO_PWM_L_P	O	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	GRF_GPIO1A_IOMUX_L[2:0]=3'b110
AUDIO_PWM_L_N	O	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	GRF_GPIO1A_IOMUX_L[6:4]=3'b110
AUDIO_PWM_R_P	O	I2S1_LRCK_RX_M0/UART4_TX_M0/PDM_CLK0_M0/AUDIOPWM_ROUT_P/GPIO1_A6_d	GRF_GPIO1A_IOMUX_H[10:8]=3'b100
AUDIO_PWM_R_N	O	I2S1_SDO0_M0/UART4_CTSn_M0/SCR_DET/AUDIOPWM_ROUT_N/ACODEC_DAC_DATAL/GPIO1_A7_d	GRF_GPIO1A_IOMUX_H[14:12]=3'b100

23.5 Application Notes

23.5.1 Frequency Configuration

ACDC_ADC_CLK and ACDC_DAC_CLK are input clocks of Digital Audio Codec. Operation clock of digital ADC and I2S master TX mode are generated from ACDC_ADC_CLK, while operation clock of digital DAC and I2S master RX mode are generated from ACDC_DAC_CLK. ACDC_ADC_CLK and ACDC_DAC_CLK are asynchronous to each other. ACDC_ADC_CLK must be homologous to the MCLK_TX of I2S which is connected to Digital Audio Codec when the I2S TX module inside Digital Audio Codec acts as a slave. It is similar that ACDC_DAC_CLK must be homologous to the MCLK_RX of I2S which is connected to Digital Audio Codec when the I2S RX module inside Digital Audio Codec acts as a slave.

Clocks named D2A_ADC_CLK and D2A_DAC_CLK acting as interface clock generated from ACDC_ADC_CLK and ACDC_DAC_CLK respectively are sent out to Analog Codec. In order to transfer audio data between digital Codec and Analog Codec, in addition to the audio data lines of digital ADC and DAC, two periodic synchronous signal named D2A_ADC_SYNC and D2A_DAC_SYNC are needed to indicate the start of every sample data.

The Digital ADC supports three application scenarios that are normal mode, low power mode 1 and low power mode 2. Different application mode requires different frequency of ACDC_ADC_CLK. If ACDCDIG_ADCCLKCTRL.cic_ds_ratio is programmed to 16, 8 and 4, the Digital ADC operates in normal mode, low power mode 1 and low power mode 2 respectively.

The relationship of ACDC_ADC_CLK, D2A_ADC_CLK, D2A_ADC_SYNC and sample rates is as follows where the D2A_ADC_CLK is 8 times of D2A_ADC_SYNC.

Table 23-4 Relationship of ACDC_ADC_CLK, D2A_ADC_CLK, D2A_ADC_SYNC and Sample Rates in Normal Mode

ACDC_ADC_CLK	D2A_ADC_CLK	D2A_ADC_SYNC	Sample rates supported
49.152MHz	49.152MHz	6.144MHz	12/24/48/96/192kHz
45.154MHz	45.154MHz	5.644MHz	11.024/22.05/44.1/88.2/176.4 kHz
32.768MHz	32.768MHz	4.096MHz	8/16/32/64/128kHz

Table 23-5 Relationship of ACDC_ADC_CLK, D2A_ADC_CLK, D2A_ADC_SYNC and Sample Rates in Low Power Mode 1

ACDC_ADC_CLK	D2A_ADC_CLK	D2A_ADC_SYNC	Sample rates supported
24.576MHz	24.576MHz	3.072MHz	12/24/48/96kHz
22.577MHz	22.577MHz	2.822MHz	11.024/22.05/44.1/88.2kHz

16.384MHz	16.384MHz	2.048MHz	8/16/32/64kHz

Table 23-6 Relationship of ACDC_ADC_CLK, D2A_ADC_CLK, D2A_ADC_SYNC and Sample Rates in Low Power Mode 2

ACDC_CLK	D2A_ADC_CLK	D2A_ADC_SYNC	Sample rates supported
12.288MHz	1.536MHz	1.536MHz	12/24/48kHz
11.288MHz	1.411MHz	1.411MHz	11.024/22.05/44.1kHz
8.192MHz	1.024MHz	1.024MHz	8/16kHz

For Digital DAC, the relationship of ACDC_DAC_CLK, D2A_DAC_CLK, D2A_DAC_SYNC and sample rates is as follows where the D2A_DAC_CLK is 8 times of D2A_DAC_SYNC.

Table 23-7 Relationship of ACDC_DAC_CLK, D2A_DAC_CLK, D2A_DAC_SYNC and Sample Rates

ACDC_DAC_CLK	D2A_DAC_CLK	D2A_DAC_SYNC	Sample rates supported
49.152MHz	49.152MHz	6.144MHz	12/24/48/96/192kHz
45.154MHz	45.154MHz	5.644MHz	11.024/22.05/44.1/88.2/176.4 kHz
32.768MHz	32.768MHz	4.096MHz	8/16/32/64/128kHz

23.5.2 Operation Mode

The Digital Audio Codec supports two operation modes, asynchronous mode and synchronous mode by programming ACDCDIG_SYSCTRL0.sync_mode.
The asynchronous mode refers to that ACDC_ADC_CLK and ACDC_DAC_CLK are asynchronous to each other. The interface of Digital ADC is consists of D2A_ADC_CLK, D2A_ADC_SYNC and A2D_ADC_DATA, independently to the interface of Digital DAC which is consists of D2A_DAC_CLK, D2A_DAC_SYNC, D2A_DAC_DATA_L and D2A_DAC_DATA_R. There are no relationship between interface of Digital ADC and Digital DAC.
The synchronous mode refers to that ACDC_ADC_CLK and ACDC_DAC_CLK are fed into a mux to generate a common operation clock(named as ACDC_COM_CLK) for both Digital ADC and DAC. The operation clock of Digital ADC and DAC are from the same source. In this situation, the Digital Audio Codec use
D2A_ADC_CLK, D2A_ADC_SYNC , A2D_ADC_DATA, D2A_DAC_DATA_L and D2A_DAC_DATA_R to communicate with Analogy Audio Codec. D2A_ADC_CLK and D2A_ADC_SYNC are shared by Digital ADC and DAC.
When operates in synchronous mode, some restrictions should be taken into account. There are 3 applications(application mode 0, application mode 1 and application mode 2) that should be considered separately.
For application mode 0 and application mode 1, there are no restrictions on ACDC_COM_CLK. Just configure the frequency of ACDC_COM_CLK according to sample rate and make sure that the frequency of D2A_ADC_CLK is at least 8 times of D2A_ADC_SYNC. In this situation, the divider ACDCDIG_ADCINT_DIV and ACDCDIG_DACINT_DIV must be equal to 0x07.
For application mode 2, there are some differences. For example, sample rate of digital ADC is 12kHz while sample rate of DAC is 128kHz. Configure ACDC_COM_CLK to the higher frequency such as 49.152MHz. The divider ACDCDIG_ADCINT_DIV must be set to 0x07 while ACDCDIG_DACINT_DIV must be set to 0x0b. On the contrary, if sample rate of digital ADC is 128kHz while sample rate of DAC is 12kHz. Configure ACDC_COM_CLK to the higher frequency such as 49.152MHz. The divider ACDCDIG_ADCINT_DIV must be set to 8'h0b while ACDCDIG_DACINT_DIV must be set to 0x07.

23.5.3 Software Application Notes

Steps to configure Digital ADC and DAC to start transfer at the same time are as follows.
1. Program CRU in the SOC system to achieve the frequency of ACDC_ADC_CLK and ACDC_DAC_CLK.
2. Program ACDCDIG_SYSCTRL0 to set sync_mode and clk_com_sel.
3. Program ACDCDIG_ADCINT_DIV to 0x07 or 0x0b according to application modes.
4. Program ACDCDIG_ADCCLKCTRL to 0x3e. It is preferred to set cic_ds_ratio=2'b00 to make Digital Audio Codec work in normal mode.
5. Program ACDCDIG_ADCSCLKTXINT_DIV.
6. Program ACDCDIG_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S TX related registers.

7. Program ACDCDIG_DACINT_DIV to 0x07 or 0x0b according to application modes.
8. Program ACDCDIG_DACCLKCTRL to 0x3c.
9. Program ACDCDIG_DACSCLKRXINT_DIV.
10. Program ACDCDIG_I2S_CKR0 to set I2S RX related registers.
11. Program ACDCDIG_SYSCTRL0. clk_com_sel to select ACDC_COM_CLK source if works in synchronous mode. Program ACDCDIG_SYSCTRL0.sync_sel to select D2A_ADC_SYNC source. Don't enable glbcke at this time.
12. Program I2C related registers to set properly device address, timeout value and so on. Then program ACDCDIG_I2C_CON0 to enable I2C at last.
13. Program ACDCDIG_I2S_CLR to clear I2S TX and RX logic.
14. Program ACDCDIG_I2S_TXCR0, ACDCDIG_I2S_TXCR1, ACDCDIG_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
15. Program I2S controller that is connected to Digital Audio Codec. Don't start I2S TX and RX at this time.
16. Program digital ADC related registers such as ACDCDIG_ADCHPFEN, ACDCDIG_ADCVUCTL, ACDCDIG_ADCCFG1 to achieve basic configuration.
17. Program DAC related registers such as ACDCDIG_DACHPF, ACDCDIG_DACVUCTL and ACDCDIG_DACCFG1 to achieve basic configuration.
18. Program ACDCDIG_I2S_XFER to start I2S TX and RX.
19. Program I2S controller outside Digital Audio Codec to start I2S TX and RX.
20. Program ACDCDIG_SYSCTRL0.glbcke to 1'b1 to enable output of D2A_ADC_SYNC if works in synchronous mode. Skip this step if ACDCDIG_SYSCTRL0.sync_mode is 1'b0.
21. Program ACDCDIG_ADCDIGEN and ACDCDIG_DACDIGEN to enable digital ADC channels and DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end transfer are as follows.

1. Program ACDCDIG_ADCDIGEN and ACDCDIG_DACDIGEN to disable digital ADC channels and DAC channels.
2. Program ACDCDIG_ADCCLKCTRL.adc_sync_ena and 1'b0 and ACDCDIG_DACCLKCTRL.dac_sync_ena to 1'b0 to disable the D2A_ADC_SYNC and D2A_ADC_SYNC respectively. Wait ACDCDIG_ADCCLKCTRL.adc_sync_status and ACDCDIG_DACCLKCTRL.dac_sync_status until both of them read back to be 1'b0.
3. Program ACDCDIG_SYSCTRL0.glbcke to 1'b0 if works in synchronous mode.

Chapter 24 Voice Activity Detect (VAD)

24.1 Overview

Voice Activity Detect (VAD) is used to detect the amplitude of voice which is received by Analog Mic, I2S Digital Mic or PDM digital Mic when SoC is in low power mode. If the amplitude of voice is over threshold, the VAD will assert interrupt to wake up SoC, then SoC will exit low power mode.

VAD supports the following features:

- Support AHB bus interface
- Support read voice data from I2S0, I2S1,PDM
  - Support to configure the voice source address
  - Support to configure increment or fixed for the direction of voice data address
  - Support DMA request and acknowledge
  - Support transfer 1~8 burst per DMA request
  - Support read 1~8 Mic voice data, and only support single Mic voice detection, user can select any Mic voice data to detect the amplitude of voice
  - Support 16/24 bits voice data
- Support voice amplitude detection
  - Support an Amplifier for the voice data
  - Support a IIR high pass filter for the voice frequency band, and the filter coefficient can be configured
  - Support a voice detect threshold that take the ambient noise to account
- Support Multi-Mic array data storing
  - Buffer memory is shared with Internal SRAM
  - The start and end address of storing can be configured
  - When current storing address is up to end address, it will loop to start address and overlap previous data, it will also assert a flag
  - Support 3 data storing mode: mode 0 start storing data after the voice detect event, mode 1 start storing after VAD is enabled and mode 2 do not storing data
  - Support storing data through bus or ram write interface
- Support a level combined interrupt
  - Support voice detect interrupt
  - Support time out interrupt
  - Support transfer error interrupt
  - Support data transfer interrupt

24.2 Block Diagram

VAD comprises with:

- ahb_master: AHB Master Interface
- ahb_sram_if: AHB Slave Interface
- vad_reg_bank : Register bank
- dmac_engine: DMA control engine
- vad_det : Voice detection

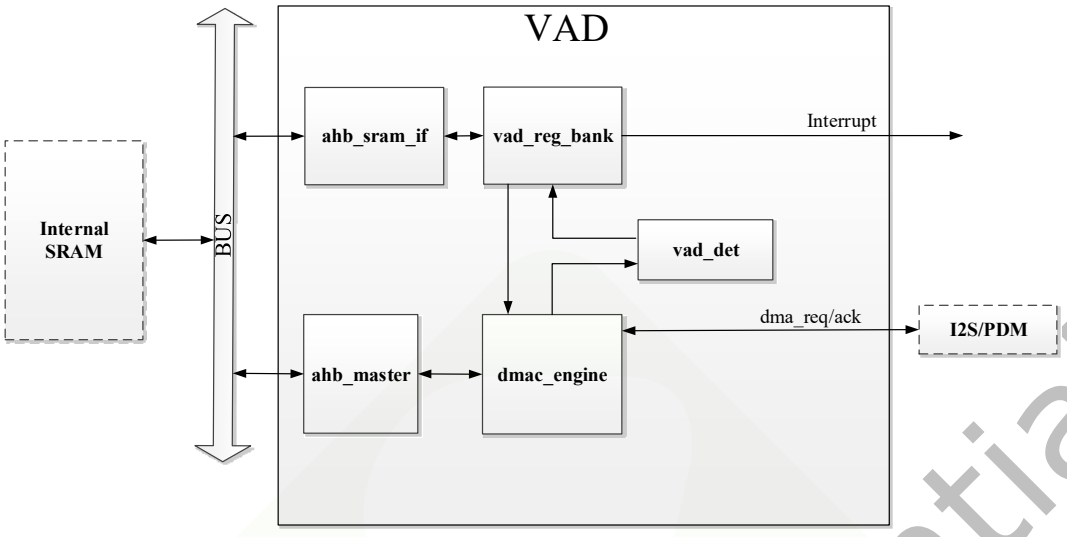


Fig. 24-1 VAD Block Diagram

24.3 Function Description

24.3.1 DMAC_ENGINE

dmac_engine is used to read voice data from one of I2S_8CH_0 or PDM, and it can store all channels data to Internal SRAM. If the bus can be access, user can configure to store through bus. Otherwise user should configure to store through ram write interface. When VAD is working, user can change the data storing mode dynamically. The storing address can be continuous transition or be spitted.

The voice data can be 16 or 24 bits:

- When it's 16 bits, it must be half word transfer mode that low 16 bits in a word for left channel and high 16 bits in a word for right channel.
- When it's 24bits, it must be word transfer mode that only 24 bits data is valid in a word, and it support left or right justified.

dmac_engine also select and send one channel data to vad_det for voice detection. vad_det only support 16 bits data to detect the amplitude of voice, so when the voice data is 24 bits, user can use the high or low 16 bits in 24 bits.

- When use high bits, the data value will be divided by 256.
- When use low bits, the data value will be saturation to 16 bits.

24.3.2 VAD_DET

vad_det is used to detect the amplitude of voice.

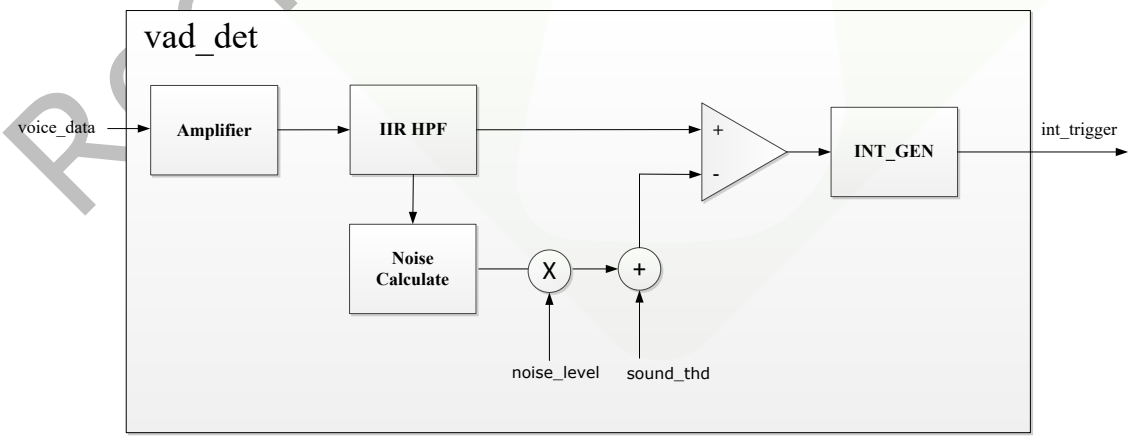


Fig. 24-2 vad_det Block Diagram

Amplifier

voice_amplitude_amplified=gain*voice_amplitude_original/8.

IIR HPF

There is a high pass filter for the human voice frequency band, the filter is a two order direct I type IIR. The following formula describes:

y(n)=-a1*y(n-1)-a2*y(n-2)+b0*x(n)+b1*x(n-1)+b2*x(n-2)

The coefficient a1, a2, b0, b1 and b2 are all quantified by multiplying 16384 and represented as 16 bits, the result is follow registers that can be configured: iir_anum_0, iir_anum_1, iir_anum_2, iir_aden_1 and iir_aden_2.

The output of HPF need some time to achieve convergence after VAD is enabled.

Noise Calculate

VAD support a voice detection threshold that take the ambient noise to account:

- VAD calculate the average amplitude of voice data within noise_sample_num samples, the result is regard as the noise value of one frame. The noise value of last 128 frames also can be configured directly.
- VAD find the minimum noise value within noise_frm_num frames, the result is regard as the noise_min(minimum noise value).User can configure min_noise_find_mode to change the mode to find the minimum noise.
- The noise_min will be smooth updated to noise_abs(current noise value), the formula is as follow: noise_abs= (noise_abs * noise_alpha + noise_min * (256-noise_alpha)/256. noise_abs will be updated once every frame. noise_abs also can be configured directly, and it is not clear until VAD is reset.

Voice Detect Threshold

The final threshold is sound_thd + noise_abs * noise_level.

INT_GEN

VAD support 3 modes to assert the voice detection interrupt.

- Normal mode: When equal or more than a number (vad_con_thd) of continuous samples over the threshold, the voice detection interrupt will be asserted. The vad_con_thd can be configured by register.
- Allow an exception mode: base on normal mode, it can be configured to allow exceptions during continuous sample judgment. The exception number can be configured by register. When the exceptions is more, the voice detect condition is less strict.
- Accumulating mode: A counter is used for accumulating, the counter will plus 1 when current sample is over threshold (it will not plus when it reach maximum value 256), the counter will minus 1 when current sample is not over threshold (it will not minus when it reach 0); When the counter is equal or more than a number (vad_con_thd), the voice detection interrupt will be asserted. Compare with normal mode, the voice detect condition is less strict when use the same value of vad_con_thd.

24.4 Register Description

24.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VAD_CONTROL	0x0000	W	0x03000000	Control register
VAD_VS_ADDR	0x0004	W	0x00000000	Voice source address register
VAD_TIMEOUT	0x004c	W	0x00000000	Timeout register
VAD_RAM_START_ADDR	0x0050	W	0x00000000	RAM start address register
VAD_RAM_END_ADDR	0x0054	W	0x00000000	RAM end address register
VAD_RAM_CUR_ADDR	0x0058	W	0x00000000	RAM current address register
VAD_DET_CON0	0x005c	W	0x01024008	Detect control register0
VAD_DET_CON1	0x0060	W	0x04ff0064	Detect control register1
VAD_DET_CON2	0x0064	W	0x3bf5e663	Detect control register2
VAD_DET_CON3	0x0068	W	0x3bf58817	Detect control register3
VAD_DET_CON4	0x006c	W	0x382b8858	Detect control register4
VAD_DET_CON5	0x0070	W	0x00000000	Detect control register5
VAD_INT	0x0074	W	0x00000000	VAD Interrupt register
VAD_AUX_CON0	0x0078	W	0x00000000	Auxiliary control register0
VAD_SAMPLE_CNT	0x007c	W	0x00000000	Sample counter register
VAD_RAM_START_ADDR_BUS	0x0080	W	0x00000000	RAM start address register for bus write mode
VAD_RAM_END_ADDR_BUS	0x0084	W	0x00000000	RAM end address register for bus write mode
VAD_RAM_CUR_ADDR_BUS	0x0088	W	0x00000000	RAM current address register for bus write mode
VAD_AUX_CON1	0x008c	W	0x00000000	Auxiliary control register1
VAD_NOISE_FIRST_DATA	0x0100	W	0x00000000	Noise first data register
VAD_NOISE_LAST_DATA	0x02fc	W	0x00000000	Noise last data register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

24.4.2 Detail Register Description

VAD_CONTROL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	vad_det_channel Index of the channal for voice detect, from channel 0 to channel 7
28	RW	0x0	voice_24bit_sat The mode of voice 24bit data change to 16bit 1'b0: Get the high 16bit data(divided by 256) 1'b1: Saturation from 24bit to 16bit
27	RW	0x0	voice_24bit_align_mode Align mode of channel 24bit width 1'b0: 8~31bits is valid 1'b1: 0~23bits is valid

Bit	Attr	Reset Value	Description
26	RW	0x0	voice_channel_bitwidth 1'b0: 16bits 1'b1: 24bits
25:23	RW	0x6	voice_channel_num Voice channel number, the value N means N+1 channel
22	RO	0x0	reserved
21:20	RW	0x0	vad_mode 2'h0: Begin to store the data after voice detect 2'h1: Begin to store the data after VAD is enable 2'h2: Don't store the data 2'h3: Reserved
19:15	RO	0x0	reserved
14	RW	0x0	source_fixaddr_en Direction of source address 1'b0: Increment 1'b1: Fixed
13:10	RW	0x0	incr_length INCR burst length, 0~15 is valid. It is valid when source_burst is set to 3'h1.
9:7	RW	0x0	source_burst_num Source burst number per dma_req, the value N means N+1 burst
6:4	RW	0x0	source_burst 3'h0: SINGLE 3'h1: INCR 3'h3: INCR4 3'h5: INCR8 3'h7: INCR16 Others: Reserved
3:1	RW	0x0	source_select Voice source select 3'h0: I2S0 3'h1: I2S1 3'h2: PDM Others: Reserved
0	RW	0x0	vad_en VAD enable 1'b0: Disable 1'b1: Enable

VAD_VS_ADDR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vs_addr Voice source address

VAD_TIMEOUT

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RW	0x0	work_timeout_en Work timeout enable 1'b0: Disable 1'b1: Enable
30	RW	0x0	idle_timeout_en Idle timeout enable 1'b0: Disable 1'b1: Enable
29:20	RW	0x000	work_timeout_thd work timeout threshold, the unit is one cycle of hclk
19:0	RW	0x00000	idle_timeout_thd Idle timeout threshold, the unit is one cycle of hclk

VAD_RAM_START_ADDR

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_start_addr RAM start address to store voice data, the address must be double word alignment

VAD_RAM_END_ADDR

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_end_addr RAM end address to store voice data, the address must be double word alignment

VAD_RAM_CUR_ADDR

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_cur_addr RAM current address to store voice data, The last valid double word data is at address ram_cur_addr-0x8. When the ram_loop_flag is valid, the valid voice data will be ram_cur_addr ~ ram_end_addr ~ loop to ram_begin_addr ~ ram_cur_addr-0x8. When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr ~ ram_cur_addr-0x8

VAD_DET_CON0

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	vad_thd_mode Threshold mode for vad_con_thd 2'b00: Normal mode 2'b01: Allow an exception mode 2'b10: Accumulating mode 2'b11: reserved
27:24	RW	0x1	dis_vad_con_thd In the determining of continuous sample number exceed threshold, allow some number of sample as an exception. It's valid only when vad_thd_mode=1. When this value is lower, the voice detect condition is more strict
23:16	RW	0x02	vad_con_thd When continuous sample number(>=vad_con_thd) exceed threshold, then assert the vad_det interrupt, the value N means N+1. When this value is higher, the voice detect condition is more strict
15	RO	0x0	reserved
14:12	RW	0x4	noise_level Noise level, valid value is 0x1~0x6 when this value is higher, the voice detect condition is more strict
11:0	RW	0x008	gain The gain control of voice data amplifier, the value of gain is unsigned and is valid from 0 to 4095. voice_amplitude_amplified=gain*voice_amplitude_original/8.

VAD_DET_CON1

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	min_noise_find_mode Minimal noise value find mode 1'b0: Always find the value at the range of noise_frm_num 1'b1: When receive N frame: if N is less than noise_frm_num, find the value at the range of N; if N is more than noise_frm_num, find the value at the range of noise_frm_num
29	RW	0x0	clean_noise_at_begin 1'b0: The noise will be clean only at the begin of the first time VAD is enable after reset 1'b1: The noise will be clean every time at the begin of VAD is enable

Bit	Attr	Reset Value	Description
28	RW	0x0	force_noise_clk_en Force noise calculate clk enable 1'b0: The clock will be auto gating for low power 1'b1: The clock will be always enable
27	RO	0x0	reserved
26	RW	0x1	clean_iir_en Clean IIR filter when VAD is disable 1'b0: Not clean 1'b1: Clean
25:16	RW	0x0ff	noise_sample_num The number of sample in one frame to calculate the noise, the value N means N+1 sample. When this value is higher, the voice detect condition is more strict
15:0	RW	0x0064	sound_thd Initial sound threshold when this value is higher, the voice detect condition is more strict

VAD_DET_CON2

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x3bf5	iir_anum_0 IIR numerator coefficient b0
15:8	RW	0xe6	noise_alpha The update smooth speed of noise When this value is lower, the voice detect condition is more strict
7	RO	0x0	reserved
6:0	RW	0x63	noise_frm_num The number of frame to calculate the noise, the value N means N+1 frame. When this value is lower, the voice detect condition is more strict

VAD_DET_CON3

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x3bf5	iir_anum_2 IIR numerator coefficient b2
15:0	RW	0x8817	iir_anum_1 IIR numerator coefficient b1

VAD_DET_CON4

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:16	RW	0x382b	iir_aden_2 IIR demoninator coefficient a2
15:0	RW	0x8858	iir_aden_1 IIR demoninator coefficient a1

VAD_DET_CON5

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	iir_result Voice real time data after IIR filter
15:0	RW	0x0000	noise_abs Noise abs value

VAD_INT

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	ramp_loop_flag_bus RAM adress loop flag for AHB bus interface write mode. Only valid when bus_write_addr_mode=1'b1. 1'b0: not loop 1'b1: loop
11	W1C	0x0	vad_data_trans_int VAD data transfer interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
10	RW	0x0	vad_data_trans_int_en VAD data transfer interrupt enable 1'b0: Disable 1'b1: Enable
9	RW	0x0	vad_idle VAD idle flag 1'b0: Not idle 1'b1: Idle
8	RO	0x0	ramp_loop_flag RAM address loop flag 1'b0: not loop 1'b1: loop
7	W1C	0x0	work_timeout_int Work timeout interrupt 1'b0: interrupt not generated 1'b1: interrupt generated

Bit	Attr	Reset Value	Description
6	W1C	0x0	idle_timeout_int Idle timeout interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
5	RW	0x0	error_int Error interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
4	W1C	0x0	vad_det_int VAD detect interrupt 1'b0: interrupt not generated 1'b1: interrupt generated
3	RW	0x0	work_timeout_int_en Wrok timeout interrupt enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_timeout_int_en Idle timeout interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	error_int_en Error interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	vad_det_int_en VAD detect interrupt enable 1'b0: Disable 1'b1: Enable

VAD_AUX_CON0

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sample_cnt_en Sample counter enable 1'b0: Disable 1'b1: Enable
28	RW	0x0	int_trig_ctrl_en The VAD detection interrupt trigger control enable. 1'b0: Disable, the VAD detection interrupt is always trigger 1'b1: Enable, the VAD detection interrupt trigger is controlled by int_trig_valid_thd

Bit	Attr	Reset Value	Description
27:16	RW	0x000	int_trig_valid_thd VAD detection interrupt trigger valid threshold. The VAD detection interrupt will be triggered valid after sample_cnt exceed int_trig_valid_thd. The value N means N+1,The unit is one voice sample point.
15	RO	0x0	reserved
14	RW	0x0	ram_write_rework_addr_mode The rework address for RAM interface write mode. 1'b0: Store the data from the current address 1'b1: Store the data from the start address
13	RW	0x0	bus_write_rework_addr_mode The rework address for bus write mode. 1'b0: Store the data from the current address 1'b1: Store the data from the start address
12	RW	0x0	bus_write_addr_mode The address selection when use AHB bus interface write mode. 1'b0: Use RAM_START_ADDR, RAM_END_ADDR, RAM_CUR_ADDR(same with RAM interface write mode). The internal address will continuous when dynamic change between bus write mode and RAM interface write mode. 1'b1: Use RAM_START_ADDR_BUS, RAM_END_ADDR_BUS and RAM_CUR_ADDR_BUS.
11:4	RW	0x00	data_trans_kbyte_thd Data transfer number threshold, the unit is KByte. The value N means N+1 KByte. The interrupt is generated per data_trans_kbyte_thd+1 KBytes.
3	RO	0x0	reserved
2	RW	0x0	data_trans_trig_int_en Trigger an interrupt for data transfer, It's valid only when bus_write_en=1'b1. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dis_ram_itf Disable write voice data to Internal SRAM through RAM interface 1'b0: Enable ram interface 1'b1: Disable ram interface
0	RW	0x0	bus_write_en Enable write voice data to Internal SRAM through AHB bus interface 1'b0: Disable 1'b1: Enable

VAD_SAMPLE_CNT

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sample_cnt sample counter

VAD_RAM_START_ADDR_BUS

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_start_addr_bus RAM start address to store voice data, the address must be double word alignment. Only used for bus write mode and when bus_write_addr_mode=1'b1.

VAD_RAM_END_ADDR_BUS

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_begin_addr_bus RAM start address to store voice data, the address must be double word alignment. Only used for bus write mode and when bus_write_addr_mode=1'b1.

VAD_RAM_CUR_ADDR_BUS

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ram_cur_addr_bus RAM current address to store voice data. Only used for bus write mode and when bus_write_addr_mode=1'b1. The last valid double word data is at address ram_cur_addr_bus-0x8. When the ram_loop_flag_bus is valid, the valid voice data will be ram_cur_addr_bus ~ ram_end_addr_bus ~ loop to ram_begin_addr_bus ~ ram_cur_addr_bus-0x8. When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr_bus ~ ram_cur_addr_bus-0x8

VAD_AUX_CON1

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	data_trans_int_mode_sel Data transfer number threshold selection for interrupt trigger 1'b0: data_trans_kbyte_thd 1'b1: data_trans_word_thd
15:0	RW	0x0000	data_trans_word_thd Data transfer number threshold, the unit is word. The value N means N+1 words. The interrupt is generated per trans_word_thd+1 words.

VAD_NOISE_FIRST_DATA

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	noise_first_data Noise first data

VAD_NOISE_LAST_DATA

Address: Operational Base + offset (0x02fc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	noise_last_data Noise last data

24.5 Application Notes

24.5.1 VAD usage flow

VAD usage flow is as following figure.

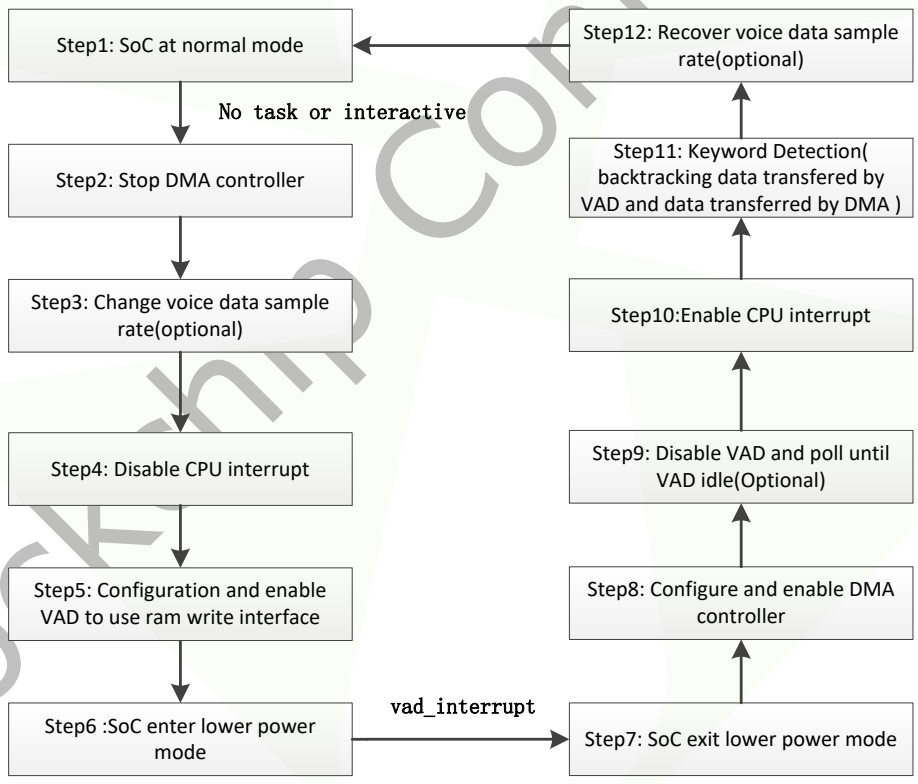


Fig. 24-3 VAD usage flow (only used ram write interface mode)

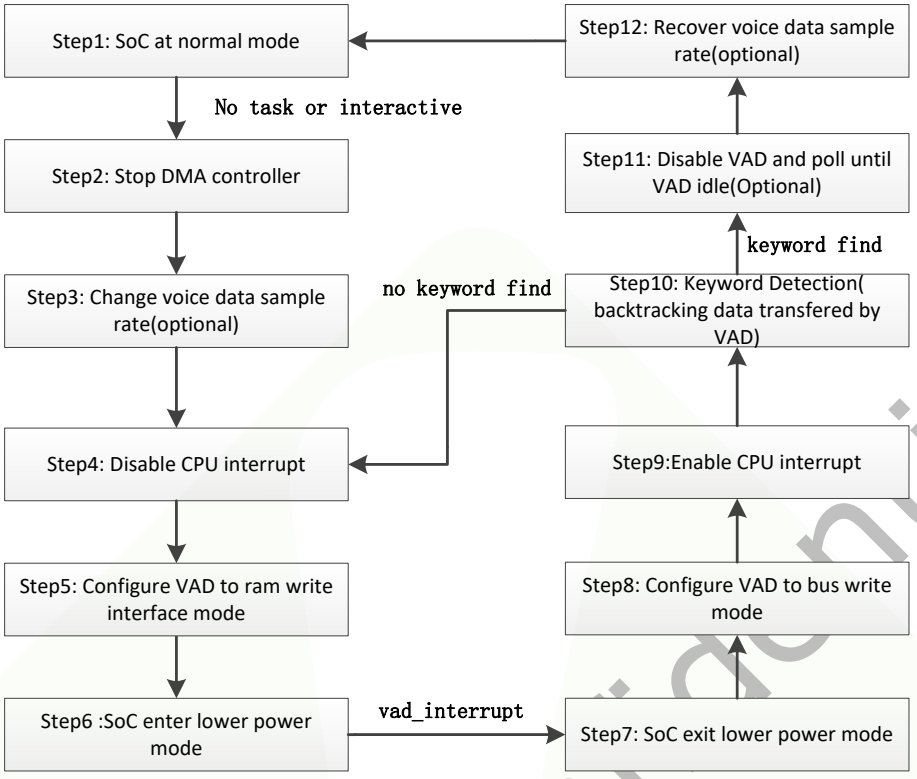


Fig. 24-4 VAD usage flow (use bus mode and ram write interface mode)

- Step3, step12 are optional, user should consider the power consumption and keyword detection accuracy for these steps.
- Disable VAD step is optional, user can keep VAD working, and use it as a DMA Controller.

24.5.2 VAD configuration usage flow

1. Set VAD_VS_ADDR.vs_addr=I2S_8CH_0 base address + I2S_8CH_INCR_RXDR.
2. Set VAD_RAM_BEGIN_ADDR.ram_begin_addr and VAD_RAM_END_ADDR.ram_end_addr, the address should match with the Internal SRAM sharing scheme.
3. Set to bus write mode or ram interface mode when enable VAD

Set VAD_AUX_CON0.bus_write_en=0, and VAD_AUX_CON0.dis_ram_itf =0 to enable VAD as ram interface write mode.

Set VAD_AUX_CON0.bus_write_en=1, and VAD_AUX_CON0.dis_ram_itf =1 to enable VAD as bus write mode.

4. Adjust the sensitivity of voice activity detect by setting follow registers:

VAD_DET_CON0.noise_level
VAD_DET_CON0.vad_con_thd
VAD_DET_CON0.dis_vad_con_thd
VAD_DET_CON0.vad_thd_mode
VAD_DET_CON1.noise_sample_num
VAD_DET_CON1.sound_thd
VAD_DET_CON2.noise_frm_num
VAD_DET_CON2.noise_alpha

5. Set the iir_anum_0~3 and iir_aden_1~2 to adjust the IIR HPF coefficient.

For 48Khz sample rate：
iir_anum_0: 0x382d
iir_anum_1: 0x8fa5
iir_anum_2: 0x382d
iir_aden_1: 0x909b
iir_aden_2: 0x3150

For 16Khz sample rate（default）：
iir_anum_0: 0x3bf5

iir_anum_1: 0x8817
iir_anum_2: 0x3bf5
iir_aden_1: 0x8858
iir_aden_2: 0x382b
For 8Khz sample rate：
iir_anum_0: 0x3e9f
iir_anum_1: 0x82c2
iir_anum_2:0x3e9f
iir_aden_1: 0x82c9
iir_aden_2: 0x3d46
6. Set DET_CON5.noise_abs to ambient noise which is calculated by software.
Set VAD_NOISE_DATA+offset to initial the noise data of all frames. The frame number is VAD_DET_CON2.noise_frm_num. The first frame noise data address is VAD_NOISE_DATA, the second frame noise data address is VAD_NOISE_DATA+0x4, and so on.
7. Set VAD_INT.vad_det_int_en=0x1 to enable the interrupt.
8. Set VAD_AUX_CONTROL to disable detection at the beginning after VAD is enabled.
Set sample_cnt_en=0x1
Set int_trig_ctrl_en=0x1
Set int_trig_valid_thd to appropriate value, it recommended configuration to 4ms.
For 48Khz sample rate：int_trig_valid_thd= 0xc0
For 16Khz sample rate：int_trig_valid_thd= 0x40
For 8Khz sample rate：int_trig_valid_thd= 0x20
9. Set VAD_CONTROL register:
Set source_select=0x1, select I2S_8CH_0
Set source_burst=0x3, select INCR4 burst type
Set source_burst_num=0x0, select 1 burst transfer per DMA request
Set vad_mode=0x0, select Mode 0
Set voice_channel_num=0x7, all voice channel number is 8
Set voice_channel_bitwidth=0x0, voice data width is 16 bits
Set vad_det_channel=0x0, use channel 0 to voice activity detect
Set vad_en=0x1, enable VAD
10. After above setting, VAD will start to work and system can enter low power mode.
When VAD is working, user can configure the VAD_AUX_CON0.bus_write_en and VAD_AUX_CON0.ram_itf_dis to change the data storing mode dynamically. The storing address can be continuous transition or be spitted. It’s controlled by following bits:
VAD_AUX_CON0.bus_write_addr_mode
VAD_AUX_CON0. bus_write_rework_addr_mode
VAD_AUX_CON0. ram_write_rework_addr_mode

24.5.3 Data Transfer Interrupt usage flow

When VAD is working at bus write mode. User can get data transfer interrupt by following additional configuration.
1. Set VAD_AUX_CONTROL.data_trans_trig_int_en=0x1
2. Set VAD_AUX_CONTROL.data_trans_kbyte_thd at appropriate value
3. Set VAD_INT.vad_data_trans_int_en=0x1

24.5.4 Timeout configuration usage flow

1. Set VAD_TIMEOUT.idle_timeout_thd=0xfffff, set VAD_TIMEOUT.idle_timeout_en=0x1, set VAD_INT.idle_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is idle, the counter will be clear to 0 once dmac_engine start to read voice data. An interrupt will be asserted when the counter up to idle_timeout_thd. This idle timeout is used for I2S/PDM work fail(Don’t assert DMA request for a long time).
2. Set VAD_TIMEOUT.work_timeout_thd=0x3ff, set VAD_TIMEOUT.work_timeout_en=0x1, set VAD_INT.work_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is busy, the counter will be clear to 0 once dmac_engine is idle. An interrupt will be asserted when the counter up to work_timeout_thd. This work timeout is used for bus transmission congestion (a burst transferring is not completed for a long time).

Chapter 25 UART

25.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.
UART Controller supports the following features:

- Support 6 independent UART controller: UART0-UART5
- All contain two 64Bytes FIFOs for data receive and transmit
- All support auto flow-control except
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer

25.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

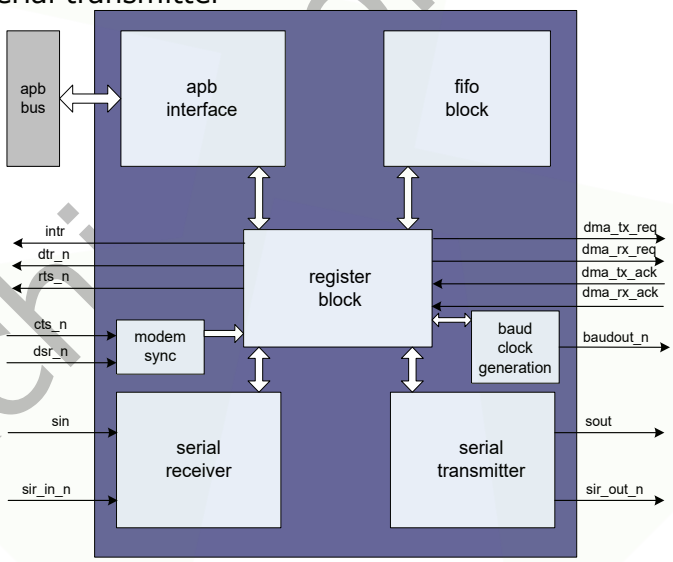


Fig. 25-1 UART Architecture

APB INTERFACE
The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.
Register block
Be responsible for the main UART functionality including control, status and interrupt generation.
Modem Synchronization block
Synchronizes the modem input signal.
FIFO block
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).
Baud Clock Generator
Generates the transmitter and receiver baud clock along with the output reference clock

signal (baudout_n).

Serial Transmitter

Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission. This makeup of serial data, referred to as a character can exit the block in two forms, either serial UART format or IrDA 1.0 SIR format.

Serial Receiver

Converts the serial data character (as specified by the control register) received in either the UART or IrDA 1.0 SIR format to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

25.3 Function Description

UART (RS232) Serial Protocol

Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in Figure.

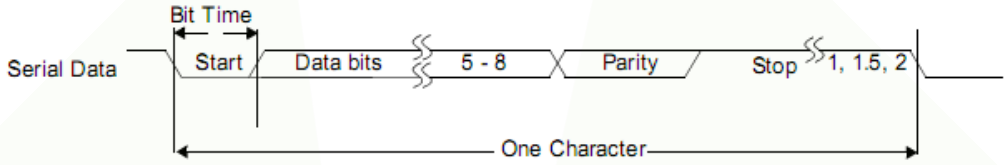


Fig. 25-2 UART Serial protocol

IrDA 1.0 SIR Protocol

The Infrared Data Association (IrDA) 1.0 Serial Infrared (SIR) mode supports bi-directional datacommunications with remote devices using infrared radiation as the transmission medium. IrDA 1.0 SIR mode specifies a maximum baud rate of 115.2 Kbaud.

Transmitting a single infrared pulse signals a logic zero, while a logic one is represented by not sending a pulse. The width of each pulse is 3/16ths of a normal serial bit time. Data transfers can only occur in half-duplex fashion when IrDA SIR mode is enabled.

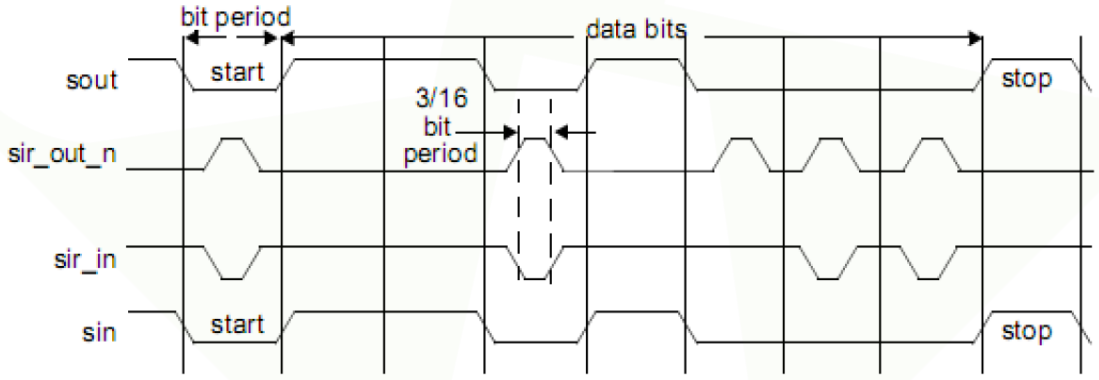


Fig. 25-3 IrDA 1.0

Baud Clock

The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

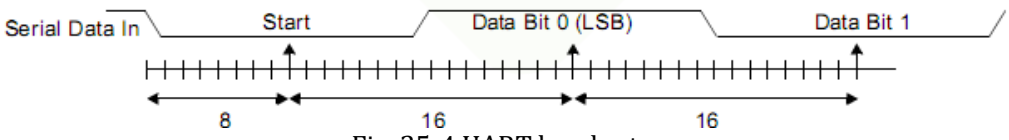


Fig. 25-4 UART baud rate

FIFO Support

1. NONE FIFO MODE

If FIFO support is not selected, then no FIFOs are implemented and only a single receive

data byte and transmit data byte can be stored at a time in the RBR and THR.

2. FIFO MODE

The FIFO depth of UART0/UART1/UART2is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

Interrupts

The following interrupt types can be enabled with the IER register.

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)
- Modem Status

DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

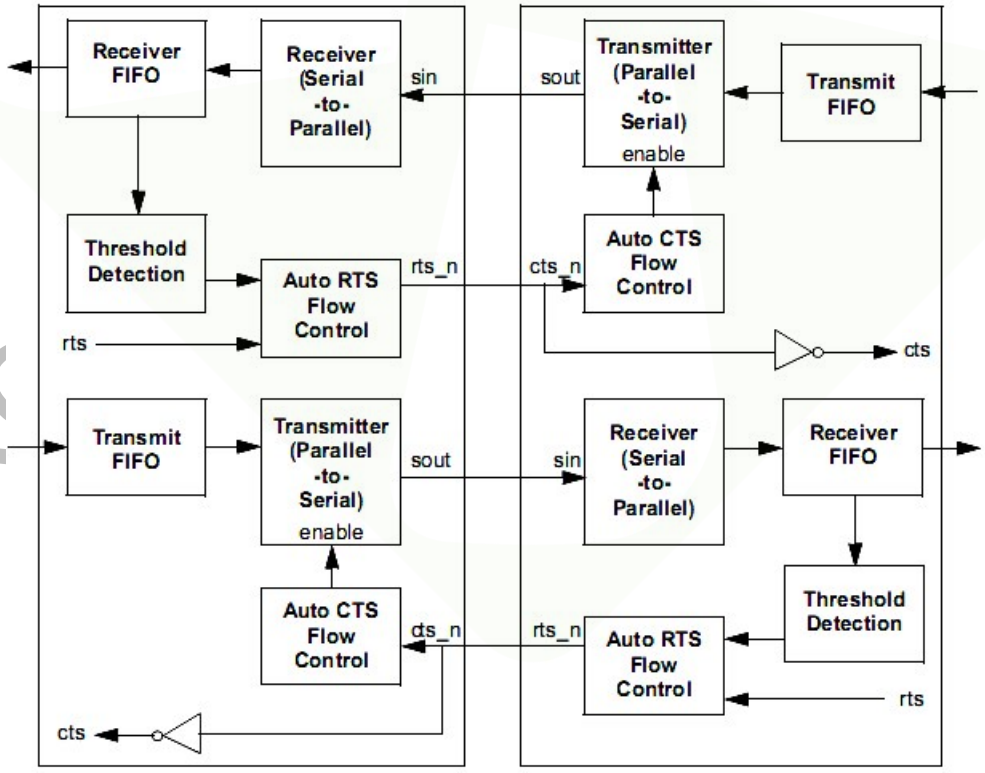


Fig. 25-5 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

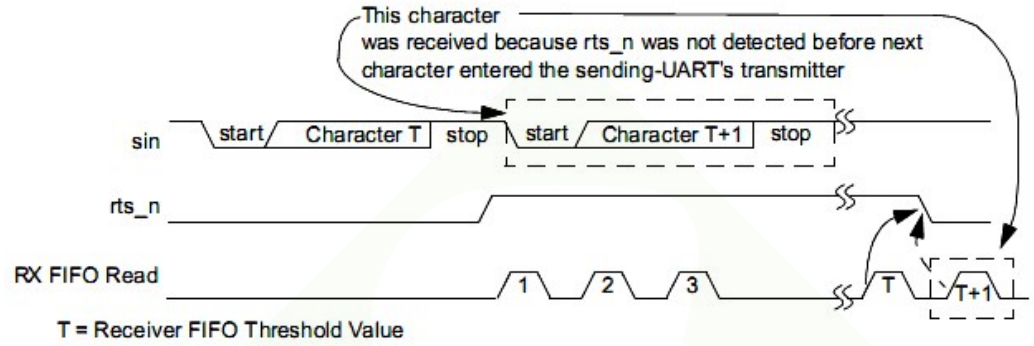


Fig. 25-6 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

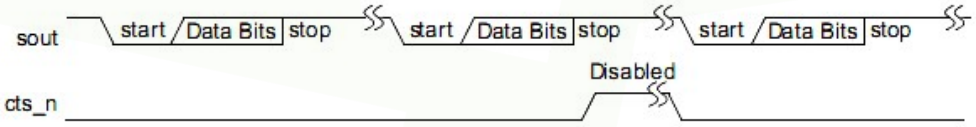


Fig. 25-7 UART AUTO CTS TIMING

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch Low
UART_THR	0x0000	W	0x00000000	Transmit Buffer Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch High
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_FCR	0x0008	W	0x00000000	FIFO Enable
UART_IIR	0x0008	W	0x00000001	Interrupt Identity Register
UART_LCR	0x000C	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000060	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register
UART_SCR	0x001C	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x0030	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read

Name	Offset	Size	Reset Value	Description
UART_RFW	0x0078	W	0x00000000	Receive FIFO write
UART_USR	0x007C	W	0x00000006	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO level
UART_RFL	0x0084	W	0x00000000	Receive FIFO level
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008C	W	0x00000000	Shadow Request to Send
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode
UART_SFE	0x0098	W	0x00000000	Shadow FIFO enable
UART_SRT	0x009C	W	0x00000000	Shadow RCVR Trigger
UART_STET	0x00A0	W	0x00000000	Shadow TX Empty Trigger
UART_HTX	0x00A4	W	0x00000000	Halt TX
UART_DMASA	0x00A8	W	0x00000000	DMA Software Acknowledge
UART_CPR	0x00F4	W	0x00043FF2	Component Parameter Register
UART_UCV	0x00F8	W	0x3330382A	UART Component Version
UART_CTR	0x00FC	W	0x44570110	Component Type Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

UART_RBR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_DLL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	baud_rate_divisor_l Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

UART_THR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full.. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_DLH

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_h Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest DW_apb_uart clock should be allowed to pass before transmitting or receiving data.

UART_IER

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	prog_thre_int_en Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. 1'b0: Disabled 1'b1: Enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	receive_line_status_int_en Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	trans_hold_empty_int_en Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
0	RW	0x0	receive_data_available_int_en Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: Disabled 1'b1: Enabled

UART_FCR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	WO	0x0	rcvr_trigger at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Suppor". The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

Bit	Attr	Reset Value	Description
5:4	WO	0x0	tx_empty_trigger TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to " DMA Suppor" . The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support. 1'b0: Mode 0 1'b1: Mode 1
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

UART_IIR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	fifos_en FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: Disabled 2'b11: Enabled
5:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x1	int_id Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: Modem status 4'b0001: No interrupt pending 4'b0010: THR empty 4'b0100: Received data available 4'b0110: Receiver line status 4'b0111: Busy detect 4'b1100: Character timeout The interrupt priorities are split into four levels that are detailed in Table X. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

UART_LCR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	div_lat_access Divisor Latch Access Bit.Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	RW	0x0	break_ctrl Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RO	0x0	reserved
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: Parity disabled 1'b1: Parity enabled

Bit	Attr	Reset Value	Description
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit.
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in "IrDA 1.0 SIR Protocol". 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.

Bit	Attr	Reset Value	Description
3	RW	0x0	out2 OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: Out2_n de-asserted (logic 1) 1'b1: Out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	RW	0x0	out1 OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 1'b0: Out1_n de-asserted (logic 1) 1'b1: Out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive

UART_LSR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: No error in RX FIFO 1'b1: Error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	RO	0x1	trans_empty Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	RO	0x1	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

Bit	Attr	Reset Value	Description
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No framing error 1'b1: Framing error Reading the LSR clears the FE bit.
2	RO	0x0	parity_eror Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No parity error 1'b1: Parity error Reading the LSR clears the PE bit.
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 1'b0: No overrun error 1'b1: Overrun error Reading the LSR clears the OE bit.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 1'b0: No data ready 1'b1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

UART_MSR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RO	0x0	data_carrior_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 1'b0: dcd_n input is de-asserted (logic 1) 1'b1: dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 1'b0: ri_n input is de-asserted (logic 1) 1'b1: ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. 1'b0: dsr_n input is de-asserted (logic 1) 1'b1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. 1'b0: cts_n input is de-asserted (logic 1) 1'b1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 1'b0: No change on dcd_n since last read of MSR 1'b1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.

Bit	Attr	Reset Value	Description
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 1'b0: No change on ri_n since last read of MSR 1'b1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 1'b0: No change on dsr_n since last read of MSR 1'b1: Change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 1'b0: No change on ctsdsr_n since last read of MSR 1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

UART_SCR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	temp_store_space Scratchpad register.This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart.

UART_SRBR

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	shadow_rbr This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	shadow_thr This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_FAR

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	fifo_access_test_en Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

UART_TFR

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.

UART_RFW

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

UART_USR

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	RO	0x1	trasn_fifo_empty Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	0x1	trans_fifo_not_full Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the DW_apb_uart is idle or inactive. 1'b0: DW_apb_uart is idle or inactive 1'b1: DW_apb_uart is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock.

UART_TFL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

UART_SBCR

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.

UART_SDMAM

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 1'b0: Mode 0 1'b1: Mode 1

UART_SFE

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

UART_SRT

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store thepreviously written value to the FCR in memory and having to mask thisvalue so that only the RCVR trigger bit gets updated.This is used to select the trigger level in the receiver FIFO at which theReceived Data Available Interrupt is generated. It also determines when thedma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

UART_STET

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full

UART_HTX

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation.

UART_DMASA

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

UART_CPR

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x04	fifo_mode 8'h0: 0 8'h0: 16 8'h0: 32 to 8'h80: 2048 8'h81-8'hff:reserved
15:14	RO	0x0	reserved
13	RO	0x1	dma_extra 1'b0: False 1'b1: Ture
12	RO	0x1	uart_add_encoded_params 1'b0: False 1'b1: Ture
11	RO	0x1	shadow 1'b0: False 1'b1: Ture
10	RO	0x1	fifo_stat 1'b0: False 1'b1: Ture
9	RO	0x1	fifo_access 1'b0: False 1'b1: Ture
8	RO	0x1	new_feat 1'b0: False 1'b1: Ture
7	RO	0x1	sir_lp_mode 1'b0: False 1'b1: Ture
6	RO	0x1	sir_mode 1'b0: False 1'b1: Ture
5	RO	0x1	thre_mode 1'b0: False 1'b1: Ture
4	RO	0x1	afce_mode 1'b0: False 1'b1: Ture
3:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RO	0x2	apb_data_width 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: reserved

UART_UCV

Address: Operational Base + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3330382a	ver ASCII value for each number in the version.

UART_CTR

Address: Operational Base + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

25.5 Interface Description

Table 25-1UART Interface Description

Module Pin	Dir.	Pad Name	IOMUX Setting
UART0mux0 Interface			
uart0_sin	I	PWM1_M0/GPUAVS/UART0_RX/GPIO0_C0_d	PMUGRF_GPIO0C_IOMUX_SEL_L[3:0]=4'h3
uart0_sout	O	PWM2_M0/NPUAVS/UART0_TX/MCU_JTAG_TDI/GPIO0_C1_d	PMUGRF_GPIO0C_IOMUX_SEL_L[7:4]=4'h3
uart0_cts_n	I	HDMITX_CEC_M1/PWM0_M1/UART0_CTSn/GPIO0_C7_d	PMUGRF_GPIO0C_IOMUX_SEL_H[15:12]=4'h3
uart0_rts_n	O	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	PMUGRF_GPIO0C_IOMUX_SEL_H[3:0]=4'h3
UART1mux0 Interface			
uart1_sin	I	GMAC0_TXD0/UART1_RX_M0/GPIO2_B3_u	GRF_GPIO2B_IOMUX_SEL_L[15:12]=4'h2
uart1_sout	O	GMAC0_TXD1/UART1_TX_M0/GPIO2_B4_u	GRF_GPIO2B_IOMUX_SEL_H[3:0]=4'h2
uart1_cts_n	I	GMAC0_RXD0/UART1_CTSn_M0/SPI1_MISO_M0/GPIO2_B6_u	GRF_GPIO2B_IOMUX_SEL_H[11:8]=4'h2
uart1_rts_n	O	GMAC0_TXEN/UART1_RTSn_M0/SPI1_CLK_M0/GPIO2_B5_u	GRF_GPIO2B_IOMUX_SEL_H[7:4]=4'h2
UART1mux1 Interface			
uart1_sin	I	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M1/UART1_RX_M1/PDM_SDI0_M1/GPIO3_D7_d	GRF_GPIO3D_IOMUX_SEL_H[15:12]=4'h4
uart1_sout	O	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1/UART1_TX_M1/PDM_CLK0_M1/GPIO3_D6_d	GRF_GPIO3D_IOMUX_SEL_H[11:8]=4'h4
uart1_cts_n	I	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1/UART1_CTSn_M1/I2S2_SCLK_RX_M1/GPIO4_C1_d	GRF_GPIO4C_IOMUX_SEL_L[7:4]=4'h4
uart1_rts_n	O	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTSn_M1/I2S2_MCLK_M1/GPIO4_B6_d	GRF_GPIO4B_IOMUX_SEL_H[11:8]=4'h4
UART2mux0 Interface			
uart2_sin	I	UART2_RX_M0/GPIO0_D0_u	PMUGRF_GPIO0D_IOMUX_SEL_L[3:0]=4'h1

uart2_sout	O	UART2_TX_M0/GPIO0_D1_u	GRF_GPIO0D_IOMUX_SEL_L[7:4]=4'h1
UART2mux1 Interface			
uart2_sin	I	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	GRF_GPIO1D_IOMUX_SEL_H[11:8]=4'h2
uart2_sout	O	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	GRF_GPIO1D_IOMUX_SEL_H[7:4]=4'h2
UART3mux0 Interface			
uart3_sin	I	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	GRF_GPIO1A_IOMUX_SEL_L[3:0]=4'h2
uart3_sout	O	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	GRF_GPIO1A_IOMUX_SEL_L[7:4]=4'h2
uart3_cts_n	I	I2S1_SCLK_TX_M0/UART3_CTSn_M0/SCR_IO/PCIE30X1_WAKEn_M2/ACODEC_DAC_CLK/GPIO1_A3_d	GRF_GPIO1A_IOMUX_SEL_L[15:12]=4'h2
uart3_rts_n	O	I2S1_MCLK_M0/UART3_RTSn_M0/SCR_CLK/PCIE30X1_PERSTn_M2/GPIO1_A2_d	GRF_GPIO1A_IOMUX_SEL_L[11:8]=4'h2
UART3mux1 Interface			
uart3_sin	I	LCDC_D23/PWM13_M0/GMAC1_MCLKINOUT_M0/UART3_RX_M1/PDM_SDI3_M2/GPIO3_C0_d	GRF_GPIO3C_IOMUX_SEL_L[3:0]=4'h4
uart3_sout	O	LCDC_D22/PWM12_M0/GMAC1_TXEN_M0/UART3_TX_M1/PDM_SDI2_M2/GPIO3_B7_d	GRF_GPIO3B_IOMUX_SEL_H[15:12]=4'h4
UART4mux0 Interface			
uart4_sin	I	I2S1_SCLK_RX_M0/UART4_RX_M0/PDM_CLK1_M0/SPDIF_TX_M0/GPIO1_A4_d	GRF_GPIO1A_IOMUX_SEL_H[3:0]=4'h2
uart4_sout	O	I2S1_LRCK_RX_M0/UART4_TX_M0/PDM_CLK0_M0/AUDIOPWM_ROUT_P/GPIO1_A6_d	GRF_GPIO1A_IOMUX_SEL_H[11:8]=4'h2
uart4_cts_n	I	I2S1_SDO0_M0/UART4_CTSn_M0/SCR_DET/AUDIOPWM_ROUT_N/ACODEC_DAC_DATAL/GPIO1_A7_d	GRF_GPIO1A_IOMUX_SEL_H[15:12]=4'h2
uart4_rts_n	O	I2S1_LRCK_TX_M0/UART4_RTSn_M0/SCR_RST/PCIE30X1_CLKREQn_M2/ACODEC_DAC_SYNC/GPIO1_A5_d	GRF_GPIO1A_IOMUX_SEL_H[7:4]=4'h2
UART4mux1 Interface			
uart4_sin	I	LCDC_D16/VOP_BT1120_D7/GMAC1_RXD0_M0/UART4_RX_M1/PWM8_M0/GPIO3_B1_d	GRF_GPIO3B_IOMUX_SEL_L[7:4]=4'h4
uart4_sout	O	LCDC_D17/VOP_BT1120_D8/GMAC1_RXD1_M0/UART4_TX_M1/PWM9_M0/GPIO3_B2_d	GRF_GPIO3B_IOMUX_SEL_L[11:8]=4'h4
UART5mux0 Interface			
uart5_sin	I	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	GRF_GPIO2A_IOMUX_SEL_L[7:4]=4'h3
uart5_sout	O	SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1/GPIO2_A2_d	GRF_GPIO2A_IOMUX_SEL_L[11:8]=4'h3
uart5_cts_n	I	SDMMC0_D2/JTAG_TCK/UART5_CTSn_M0/GPIO1_D7_u	GRF_GPIO1D_IOMUX_SEL_H[15:12]=4'h3
uart5_rts_n	O	SDMMC0_D3/JTAG_TMS/UART5_RTSn_M0/GPIO2_A0_u	GRF_GPIO2A_IOMUX_SEL_L[3:0]=4'h3
UART5mux1 Interface			
uart5_sin	I	LCDC_DEN/VOP_BT1120_D15/SPI1_CLK_M1/UART5	GRF_GPIO3C_IOMUX_SEL_L[15:12]=4'h4

		_RX_M1/I2S1_SCLK_RX_M2/GPIO3_C3_d	
uart5_sout	O	LCDC_VSYNC/VOP_BT1120_D14/SPI1_MISO_M1/UART5_TX_M1/I2S1_SDO3_M2/GPIO3_C2_d	GRF_GPIO3C_IOMUX_SEL_L[11:8]=4'h4
UART6mux0 Interface			
uart6_sin	I	SDMMC1_D0/GMAC0_RXD2/UART6_RX_M0/GPIO2_A3_u	GRF_GPIO2A_IOMUX_SEL_L[15:12]=4'h3
uart6_sout	O	SDMMC1_D1/GMAC0_RXD3/UART6_TX_M0/GPIO2_A4_u	GRF_GPIO2A_IOMUX_SEL_H[3:0]=4'h3
uart6_cts_n	I	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	GRF_GPIO2C_IOMUX_SEL_L[3:0]=4'h3
uart6_rts_n	O	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	GRF_GPIO2B_IOMUX_SEL_H[15:12]=4'h3
UART6mux1 Interface			
uart6_sin	I	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	GRF_GPIO1D_IOMUX_SEL_H[11:8]=4'h3
uart6_sout	O	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	GRF_GPIO1D_IOMUX_SEL_H[7:4]=4'h3
UART7mux0 Interface			
uart7_sin	I	SDMMC1_D2/GMAC0_RXCLK/UART7_RX_M0/GPIO2_A5_u	GRF_GPIO2A_IOMUX_SEL_H[7:4]=4'h3
uart7_sout	O	SDMMC1_D3/GMAC0_TXD2/UART7_TX_M0/GPIO2_A6_u	GRF_GPIO2A_IOMUX_SEL_H[11:8]=4'h3
uart7_cts_n	I	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	GRF_GPIO2C_IOMUX_SEL_L[11:8]=4'h3
uart7_rts_n	O	I2S2_MCLK_M0/ETH0_REFCLKO_25M/UART7_RTSn_M0/SPI2_CLK_M0/GPIO2_C1_d	GRF_GPIO2C_IOMUX_SEL_L[7:4]=4'h3
UART7mux1 Interface			
uart7_sin	I	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	GRF_GPIO3C_IOMUX_SEL_H[7:4]=4'h4
uart7_sout	O	PWM14_M0/VOP_PWM_M1/GMAC1_MDC_M0/UART7_TX_M1/PDM_CLK1_M2/GPIO3_C4_d	GRF_GPIO3C_IOMUX_SEL_H[3:0]=4'h4
UART7mux2 Interface			
uart7_sin	I	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1/UART7_RX_M2/PDM_SDI3_M1/GPIO4_A3_d	GRF_GPIO4A_IOMUX_SEL_L[15:12]=4'h4
uart7_sout	O	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1/UART7_TX_M2/PDM_SDI2_M1/GPIO4_A2_d	GRF_GPIO4A_IOMUX_SEL_L[11:8]=4'h4
UART8mux0 Interface			
uart8_sin	I	CLK32K_OUT1/UART8_RX_M0/SPI1_CS1_M0/GPIO2_C6_d	GRF_GPIO2C_IOMUX_SEL_H[11:8]=4'h2
uart8_sout	O	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	GRF_GPIO2C_IOMUX_SEL_H[7:4]=4'h3
uart8_cts_n	I	SDMMC1_DET/I2C4_SCL_M1/UART8_CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	GRF_GPIO2B_IOMUX_SEL_L[11:8]=4'h3
uart8_rts_n	O	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	GRF_GPIO2B_IOMUX_SEL_L[7:4]=4'h3
UART8mux1 Interface			

uart8_sin	I	LCDC_CLK/VOP_BT656_CLK_M0/SPI2_CLK_M1/UART8_RX_M1/I2S1_SDO1_M2/GPIO3_A0_d	GRF_GPIO3A_IOMUX_SEL_L[3:0]=4'h4
uart8_sout	O	LCDC_D7/VOP_BT656_D7_M0/SPI2_MISO_M1/UART8_TX_M1/I2S1_SDO0_M2/GPIO2_D7_d	GRF_GPIO2D_IOMUX_SEL_H[15:12]=4'h4
UART9mux0 Interface			
uart9_sin	I	SDMMC1_CMD/GMAC0_TXD3/UART9_RX_M0/GPIO2_A7_u	GRF_GPIO2A_IOMUX_SEL_H[15:12]=4'h3
uart9_sout	O	SDMMC1_CLK/GMAC0_TXCLK/UART9_TX_M0/GPIO2_B0_d	GRF_GPIO2B_IOMUX_SEL_L[3:0]=4'h3
uart9_cts_n	I	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	GRF_GPIO2C_IOMUX_SEL_H[3:0]=4'h3
uart9_rts_n	O	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	GRF_GPIO2C_IOMUX_SEL_L[15:12]=4'h3
UART9mux1 Interface			
uart9_sin	I	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	GRF_GPIO4C_IOMUX_SEL_H[11:8]=4'h4
uart9_sout	O	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	GRF_GPIO4C_IOMUX_SEL_H[7:4]=4'h4
UART9mux2 Interface			
uart9_sin	I	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	GRF_GPIO4A_IOMUX_SEL_H[7:4]=4'h4
uart9_sout	O	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	GRF_GPIO4A_IOMUX_SEL_H[3:0]=4'h4

25.6 Application Notes

25.6.1 None FIFO Mode Transfer Flow

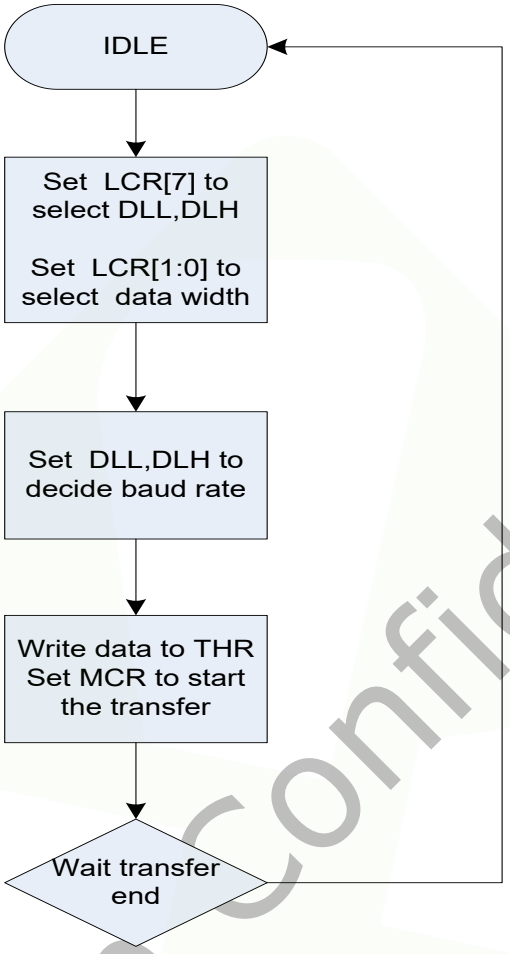


Fig. 25-8 UART none fifo mode

25.6.2 FIFO Mode Transfer Flow

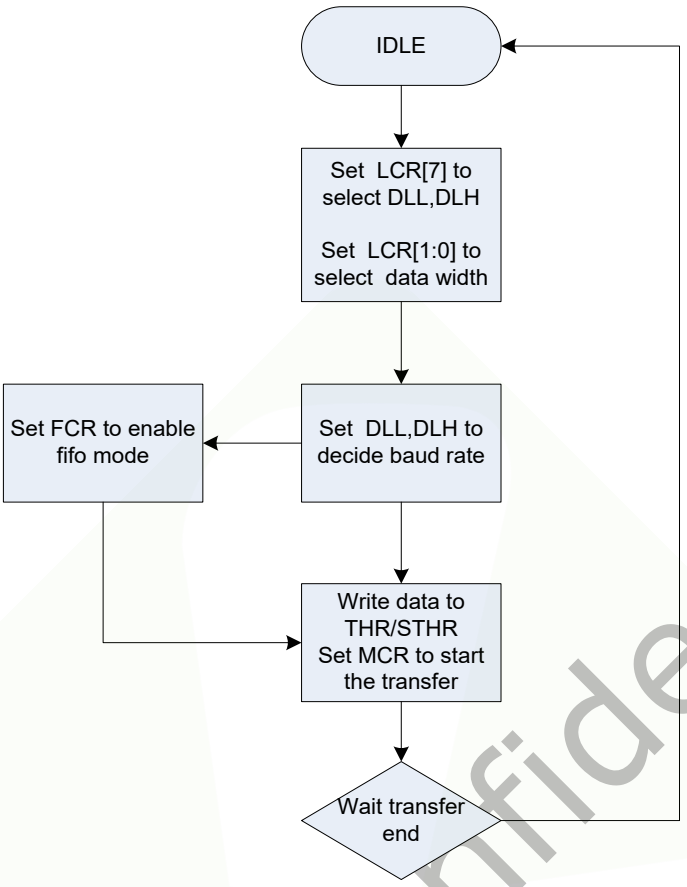


Fig. 25-9 UART fifo mode

The UART is an APB slave performing:
Serial-to-parallel conversion on data received from a peripheral device.
Parallel-to-serial conversion on data transmitted to the peripheral device.
The CPU reads and writes data and control/status information through the APB interface.
The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

25.6.3 Baud Rate Calculation

The following table provides some reference configuration for different UART baud rates.

Table 25-2 UART baud rate configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure PLL to get 1.2GHz clock output; Divide 1.2GHz clock by 16 to get 75MHz clock; Divide 75MHz clock by 72/46875 to get 115.2KHz clock;
460.8 Kbps	Configure PLL to get 1.2GHz clock output; Divide 1.2GHz clock by 16 to get 75MHz clock; Divide 75MHz clock by 288/46875 to get 460.8KHz clock;
921.6 Kbps	Configure PLL to get 1.2GHz clock output; Divide 1.2GHz clock by 16 to get 75MHz clock; Divide 75MHz clock by 576/46875 to get 921.6KHz clock;
1.5 Mbps	Choose PLL to get 1.2GHz clock output; Divide 1.2GMHz clock by 25 to get 48MHz clock; Divide 48MHz clock by 32 to get 1.5MHz clock;
3 Mbps	Choose PLL to get 1.2GHz clock output; Divide 1.2GMHz clock by 25 to get 48MHz clock; Divide 48MHz clock by 16 to get 3MHz clock;
4 Mbps	Choose PLL to get 1.2GHz clock output; Divide 1.2GMHz clock by 25 to get 48MHz clock; Divide 48MHz clock by 12 to get 4MHz clock;

Chapter 26 Serial Peripheral Interface (SPI)

26.1 Overview

The serial peripheral interface is an APB slave device. A four wire full duplex serial protocol from Motorola. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support Motorola SPI,TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combine interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one sixth of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample RXD 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode.
- Support BYPASS slave mode, in which RX and TX logic is drive by SCLK_IN directly instead of spi_clk.

26.2 Block Diagram

The SPI Controller comprises with:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

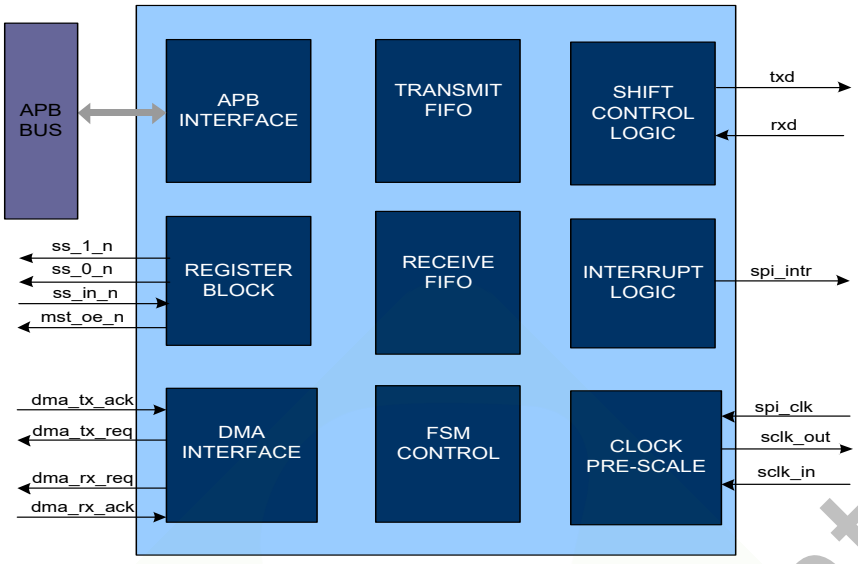


Fig. 26-1SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size(SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both FIFOs are 64x16bits.

FSM CONTROL

Control the state's transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit FIFO or to the receive FIFO. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the OR relationshipbetween all other SPI interrupts after masking.

26.3 Function Description

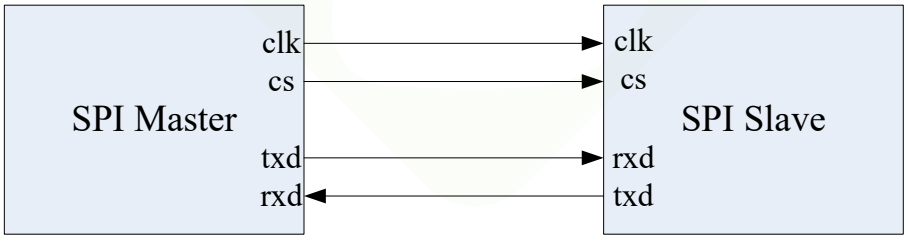


Fig. 26-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram show how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.

1). Transmit and Receive

When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.

2). Transmit Only

When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.

3). Receive Only

When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

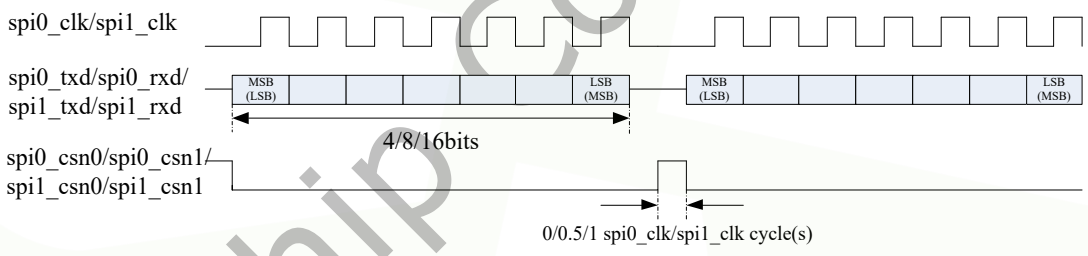


Fig. 26-3 SPI Format (SCPH=0 SCPOL=0)

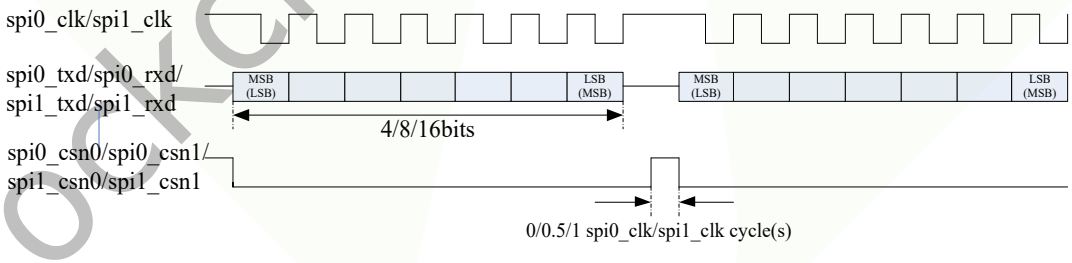


Fig. 26-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

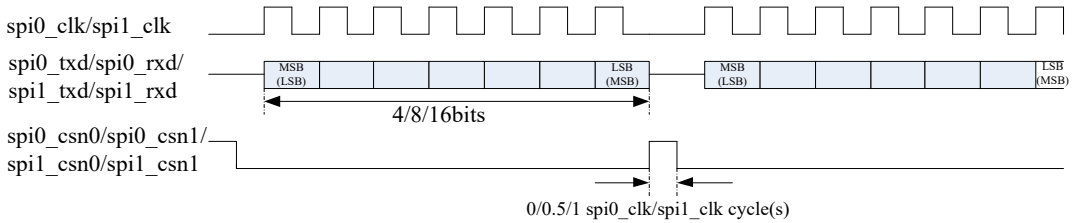


Fig. 26-5 SPI Format (SCPH=1 SCPOL=0)

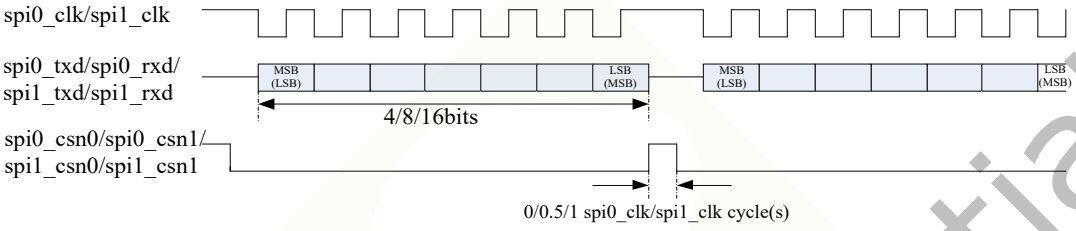


Fig. 26-6 SPI Format (SCPH=1 SCPOL=1)

26.4 Register Description

26.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00400002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable Register
SPI_SER	0x000c	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001c	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000004c	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002c	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003c	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_TIMEOUT	0x004c	W	0x00000000	Timeout control register
SPI_BYPASS	0x0050	W	0x00000000	BYPASS control register
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

26.4.2 Detail Register Description

SPI_CTRLR0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	lbk Loop back mode select. 1'b0: Normal mode. 1'b1: Loop back mode,rxd is connected to txd.
24:23	RW	0x0	soi SS_N output inverted. 1'b0: Corresponding bit of ss_in is not inverted. 1'b1: Corresponding bit of ss_in is inverted.
22	RW	0x0	sm SCLK_IN is masked by SS_N or not. 1'b0: SCLK_IN is masked 1'b1: SCLK_IN is not masked
21	RW	0x0	mtm Valid when frame format is set to National Semiconductors Microwire. 1'b0: Non-sequential transfer 1'b1: Sequential transfer
20	RW	0x0	opm Master and slave mode select. 1'b0: Master Mode 1'b1: Slave Mode
19:18	RW	0x0	xfm Transmit and receive mode select. 2'b00 : Transmit & Receive 2'b01 : Transmit Only 2'b10 : Receive Only 2'b11 : Reserved
17:16	RW	0x0	frf 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved
15:14	RW	0x0	rsd When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: Do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay

Bit	Attr	Reset Value	Description
13	RW	0x0	bht Valid when data frame size is 8bit. 1'b0: APB 16bit write/read, spi 8bit write/read. 1'b1: APB 8bit write/read, spi 8bit write/read.
12	RW	0x0	fbm 1'b0: First bit is MSB. 1'b1: First bit is LSB.
11	RW	0x0	em Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: Little endian 1'b1: Big endian
10	RW	0x0	ssd Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle.
9:8	RW	0x0	csm Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11: Reserved
7	RW	0x0	scpol Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low. 1'b1: Inactive state of serial clock is high.
6	RW	0x0	scph Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit. 1'b1: Serial clock toggles at start of first data bit.

Bit	Attr	Reset Value	Description
5:2	RW	0x0	cfs Selects the length of the control word for the Microwire frame format. 4'b0000~0010: Reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer 4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	dfs Selects the data frame length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: Reserved

SPI_CTRLR1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ndm When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer.

SPI_ENR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enr Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	ser Slave enable register.The register enable the individual slave select output lines, 2 slave-select output pins are available.This register is valid only when SPI is configured as a master device.

SPI_BAUDR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	baudr SPI Clock Divider. This register is valid only when the SPI is configured as a master device.The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/ SCKDV Where SCKDV is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	xftlr When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rxftlr When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
6:0	RO	0x00	txflr Contains the number of valid data entries in the transmit FIFO.

SPI_RXFLR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	rxflr Contains the number of valid data entries in the receive FIFO.

SPI_SR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	ssi 1'b0: ss_in_n is low. 1'b1: ss_in_n is high.
5	RO	0x0	stb 1'b0: Slave tx not busy. 1'b1: Slave tx busy.
4	RO	0x0	rff 1'b0: Receive FIFO is not full. 1'b1: Receive FIFO is full.
3	RO	0x1	rfe 1'b0: Receive FIFO is not empty. 1'b1: Receive FIFO is empty.
2	RO	0x1	tfe 1'b0: Transmit FIFO is not empty. 1'b1: Transmit FIFO is empty.
1	RO	0x0	tff 1'b0: Transmit FIFO is not full. 1'b1: Transmit FIFO is full.
0	RO	0x0	bsf When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled. 1'b1: SPI is actively transferring data.

SPI_IPR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	ipr Interrupt Polarity Register. 1'b0: Active Interrupt Polarity Level is HIGH. 1'b1: Active Interrupt Polarity Level is LOW.

SPI_IMR

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfim 1'b0: TX finish interrupt is masked. 1'b1: TX finish interrupt is not masked.
6	RW	0x0	sspim 1'b0: ss_in_n posedege interrupt is masked. 1'b1: ss_in_n posedege interrupt is not masked.
5	RW	0x0	toim 1'b0: spi timeout interrupt is masked. 1'b1: spi timeout interrupt is not masked.
4	RW	0x0	rffim 1'b0: spi_rxf_intr interrupt is masked. 1'b1: spi_rxf_intr interrupt is not masked.
3	RW	0x0	rfoim 1'b0: spi_rxo_intr interrupt is masked. 1'b1: spi_rxo_intr interrupt is not masked.
2	RW	0x0	rfuim 1'b0: spi_rxu_intr interrupt is masked. 1'b1: spi_rxu_intr interrupt is not masked.
1	RW	0x0	tfoim 1'b0: spi_txo_intr interrupt is masked. 1'b1: spi_txo_intr interrupt is not masked.
0	RW	0x0	tfeim 1'b0: spi_txe_intr interrupt is masked. 1'b1: spi_txe_intr interrupt is not masked.

SPI_ISR

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfis 1'b0: TX finish interrupt is not active after masking. 1'b1: TX finish interrupt is active after masking.
6	RW	0x0	sspis 1'b0: ss_in_n posedege interrupt is not active after masking. 1'b1: ss_in_n posedege interrupt is active after masking.

Bit	Attr	Reset Value	Description
5	RW	0x0	tois 1'b0: spi timeout interrupt is not active after masking. 1'b1: spi timeout interrupt is active after masking.
4	RO	0x0	rffis 1'b0: spi_rxf_intr interrupt is not active after masking. 1'b1: spi_rxf_intr interrupt is full after masking.
3	RO	0x0	rfois 1'b0: spi_rxo_intr interrupt is not active after masking. 1'b1: spi_rxo_intr interrupt is active after masking.
2	RO	0x0	rfuis 1'b0: spi_rxu_intr interrupt is not active after masking. 1'b1: spi_rxu_intr interrupt is active after masking.
1	RO	0x0	tfois 1'b0: spi_txo_intr interrupt is not active after masking. 1'b1: spi_txo_intr interrupt is active after masking.
0	RO	0x0	tfeis 1'b0: spi_txe_intr interrupt is not active after masking. 1'b1: spi_txe_intr interrupt is active after masking.

SPI_RISR

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfris 1'b0: TX finish interrupt is not active prior to masking. 1'b1: TX finish interrupt is active prior to masking.
6	RW	0x0	sspris 1'b0: ss_in_n posedege interrupt is not active prior to masking. 1'b1: ss_in_n posedege interrupt is active prior to masking.
5	RW	0x0	toris 1'b0: spi_timeout interrupt is not active prior to masking. 1'b1: spi_timeout interrupt is active prior to masking.
4	RO	0x0	rffris 1'b0: spi_rxf_intr interrupt is not active prior to masking. 1'b1: spi_rxf_intr interrupt is full prior to masking.
3	RO	0x0	rforis 1'b0: spi_rxo_intr interrupt is not active prior to masking. 1'b1: spi_rxo_intr interrupt is active prior to masking.
2	RO	0x0	rfuris 1'b0: spi_rxu_intr interrupt is not active prior to masking. 1'b1: spi_rxu_intr interrupt is active prior to masking.
1	RO	0x0	tforis 1'b0: spi_txo_intr interrupt is not active prior to masking. 1'b1: spi_txo_intr interrupt is active prior to masking.

Bit	Attr	Reset Value	Description
0	RO	0x1	tferis 1'b0: spi_txe_intr interrupt is not active prior to masking. 1'b1: spi_txe_intr interrupt is active prior to masking.

SPI_ICR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	ctxfi Write 1 to Clear tx finish Interrupt.
5	WO	0x0	csspi Write 1 to Clear ss_in_n posdege Interrupt.
4	WO	0x0	ctoi Write 1 to Clear Timeout Interrupt.
3	WO	0x0	ctfoi Write 1 to Clear Transmit FIFO Overflow Interrupt.
2	WO	0x0	crfoi Write 1 to Clear Receive FIFO Overflow Interrupt.
1	WO	0x0	crfui Write 1 to Clear Receive FIFO Underflow Interrupt.
0	WO	0x0	cci Write 1 to Clear Combined Interrupt.

SPI_DMACR

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	tde 1'b0: Transmit DMA disabled. 1'b1: Transmit DMA enabled.
0	RW	0x0	rde 1'b0: Receive DMA disabled. 1'b1: Receive DMA enabled.

SPI_DMATDLR

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	tdl This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1).

SPI_DMARDLR

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rdl This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled(DMACR[0]=1).

SPI_TIMEOUT

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	toe Timeout enable. 1'b0: Timeout counter is inactive. 1'b1: Timeout counter will be active after the first rising edge of sclk_in.
15:0	RW	0x0000	tov Timeout threshold value. If sclk_in keep inactive for a threshold time , timeout interrupt will be triggered .The timeout threshold time is TOV*pclk_perid*16.

SPI_BYPASS

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	txcp TX clock polarity.This bit is only valid in bypass mode. 1'b0: TX logic use raw SCLK. 1'b1: TX logic use inverted SCLK.
3	RW	0x0	rxcp RX clock polarity.This bit is only valid in bypass mode. 1'b0: RX logic use raw SCLK. 1'b1: RX logic use inverted SCLK.
2	RW	0x0	end Endian mode.This bit is only valid in bypass mode. 1'b0: Work in littel endian mode. 1'b1: Work in big endian mode.
1	RW	0x0	fbm First bit mode.This bit is only valid in bypass mode. 1'b0: First bit is LSB. 1'b1: First bit is MSB.

Bit	Attr	Reset Value	Description
0	RW	0x0	byen Bypass enable. 1'b0: Normal mode. 1'b1: Bypass mode, SPI serial/parallel convert logic is drive by SCLK.

SPI_TXDR

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	txdr When it is written to, data are moved into the transmit FIFO.

SPI_RXDR

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rxdr When the register is read, data in the receive FIFO is accessed.

26.5 Interface Description

Table 26-1SPI interface description

Module Pin	Dir	Pad Name	IOMUX Setting
SPI0mux0 Interface			
spi0_clk	I/O	I2C2_SCL_M0/SPI0_CLK_M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	PMU_GRF_GPIO0B_IOMUX_H[6:4] = 3'h2
spi0_mosi	I	I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	PMU_GRF_GPIO0B_IOMUX_H[10:8]=4'h2
spi0_miso	O	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	PMU_GRF_GPIO0C_IOMUX_H[6:4]=4'b2
spi0_csn0	I/O	PWM7_IR/SPI0_CS0_M0/PCIE30X2_PERSTn_M0/GPIO0_C6_d	PMU_GRF_GPIO0C_IOMUX_H[10:8]=3'h2
spi0_csn1	O	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	PMU_GRF_GPIO0C_IOMUX_H[2:0]=3'b2
SPI0mux1 Interface			
spi0_clk	I/O	LCDC_D3/VOP_BT656_D3_M0/SPI0_CLK_M1/PCIE30X1_WAKEn_M1/I2S1_SDI0_M2/GPIO2_D3_d	GRF_GPIO2D_IOMUX_L[14:12]=3'h3
spi0_csn0	I/O	LCDC_D2/VOP_BT656_D2_M0/SPI0_CS0_M1/PCIE30X1_CLKREQn_M1/I2S1_LRCK_TX_M2/GPIO2_D2_d	GRF_GPIO2D_IOMUX_L[10:8]=3'h3
spi0_mosi	I	LCDC_D1/VOP_BT656_D1_M0/SPI0_MOSI_M1/PCIE20_WAKEn_M1/I2S1_SCLK_TX_M2/GPIO2_D1_d	GRF_GPIO2D_IOMUX_L[6:4]=3'h3
spi0_miso	O	LCDC_D0/VOP_BT656_D0_M0/SPI0_MISO_M1/PCIE20_CLKREQn_M1/I2S1_MCLK_M2/GPIO2_D0_d	GRF_GPIO2D_IOMUX_L[2:0]=3'h3
SPI1mux0 Interface			
spi1_clk	I/O	GMAC0_TXEN/UART1_RTSn_M0/SPI1_CLK_M0/GPIO2_B5_u	GRF_GPIO2B_IOMUX_H[6:4]=3'h3
spi1_csn0	I/O	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	GRF_GPIO2B_IOMUX_H[2:0]=3'h4
spi1_csn1	O	CLK32K_OUT1/UART8_RX_M0/SPI1_CS1_M0/GPIO2_C6_d	GRF_GPIO2C_IOMUX_H[10:8]=3'h3
spi1_mosi	I	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	GRF_GPIO2B_IOMUX_H[14:12]=3'h4
spi1_miso	O	GMAC0_RXD0/UART1_CTSn_M0/SPI1_MISO_M0/GPIO2_B6_u	GRF_GPIO2B_IOMUX_H[10:8]=3'h3
SPI1mux1 Interface			
spi1_clk	I/O	LCDC_DEN/VOP_BT1120_D15/SPI1_CLK_M1/UART5_RX_M1/I2S1_SCLK_RX_M2/GPIO3_C3_d	GRF_GPIO3C_IOMUX_L[14:12]=2'h3
spi1_mosi	I	LCDC_HSYNC/VOP_BT1120_D13/SPI1_MOSI_M1/PCIE20_PERSTn_M1/I2S1_SDO2_M2/GPIO3_C1_d	GRF_GPIO3C_IOMUX_L[6:4]=2'h3
spi1_miso	O	LCDC_VSYNC/VOP_BT1120_D14/SPI1_MISO_M1/UART5_TX_M1/I2S1_SDO3_M2/GPIO3_C2_d	GRF_GPIO3C_IOMUX_L[10:8]=2'h3
spi1_csn0	I/O	LCDC_D8/VOP_BT1120_D0/SPI1_CS0_M1/PCIE30X1_PERST	GRF_GPIO3A_IOMUX_L[6:4]=3'h3

Module Pin	Dir。	Pad Name	IOMUX Setting
		n_M1/SDMMC2_D0_M1/GPIO3_A1_d	
SPI2mux0 Interface			
spi2_clk	I/O	I2S2_MCLK_M0/ETH0_REFCLKO_25M/UART7_RTSn_M0/SPI2_CLK_M0/GPIO2_C1_d	GRF_GPIO2C_IOMUX_L[6:4]=3'h4
spi2_mosi	I	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	GRF_GPIO2C_IOMUX_L[14:12]=3'h4
spi2_miso	O	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	GRF_GPIO2C_IOMUX_L[10:8]=3'h4
spi2_csn0	I/O	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	GRF_GPIO2C_IOMUX_H[2:0]=3'h4
spi2_csn1	O	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	GRF_GPIO2C_IOMUX_H[6:4]=3'h4
SPI2mux1 Interface			
spi2_clk	I/O	LCDC_CLK/VOP_BT656_CLK_M0/SPI2_CLK_M1/UART8_RX_M1/I2S1_SDO1_M2/GPIO3_A0_d	GRF_GPIO3A_IOMUX_L[2:0]=3'h3
spi2_mosi	I	LCDC_D6/VOP_BT656_D6_M0/SPI2_MOSI_M1/PCIE30X2_PERSTn_M1/I2S1_SDI3_M2/GPIO2_D6_d	GRF_GPIO2D_IOMUX_H[10:8]=3'h3
spi2_miso	O	LCDC_D7/VOP_BT656_D7_M0/SPI2_MISO_M1/UART8_TX_M1/I2S1_SDO0_M2/GPIO2_D7_d	GRF_GPIO2D_IOMUX_H[14:12]=3'h3
spi2_csn0	I/O	LCDC_D5/VOP_BT656_D5_M0/SPI2_CS0_M1/PCIE30X2_WAKEn_M1/I2S1_SDI2_M2/GPIO2_D5_d	GRF_GPIO2D_IOMUX_H[6:4]=3'h3
spi2_csn1	O	LCDC_D4/VOP_BT656_D4_M0/SPI2_CS1_M1/PCIE30X2_CLKREQn_M1/I2S1_SDI1_M2/GPIO2_D4_d	GRF_GPIO2D_IOMUX_H[2:0]=3'h3
SPI3mux0 Interface			
spi3_clk	I/O	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1/SPI3_CLK_M0/I2S2_SDO_M1/GPIO4_B3_d	GRF_GPIO4B_IOMUX_L[14:12]=3'h4
spi3_csn0	I/O	ISP_FLASHTRIGOUT/EBC_SDCE0/GMAC1_TXEN_M1/SPI3_CS0_M0/I2S1_SCLK_RX_M1/GPIO4_A6_d	GRF_GPIO4A_IOMUX_H[10:8]=3'h4
spi3_csn1	O	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1/SPI3_CS1_M0/I2S1_LRCK_RX_M1/GPIO4_A7_d	GRF_GPIO4A_IOMUX_H[14:12]=3'h4
spi3_mosi	I	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1/SPI3_MOSI_M0/I2S2_SDI_M1/GPIO4_B2_d	GRF_GPIO4B_IOMUX_L[10:8]=3'h4
spi3_miso	I/O	CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1/SPI3_MISO_M0/I2S1_SDO1_M1/GPIO4_B0_d	GRF_GPIO4B_IOMUX_L[2:0]=3'h4
SPI3mux1 Interface			
spi3_clk	I/O	PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	GRF_GPIO4C_IOMUX_L[10:8]=3'h2
spi3_csn0	I/O	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	GRF_GPIO4C_IOMUX_H[10:8]=3'h2
spi3_csn1	O	HDMITX_CEC_M0/SPI3_CS1_M1/GPIO4_D1_u	GRF_GPIO4D_IOMUX_L[6:4]=3'h2
spi3_mosi	I	PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	GRF_GPIO4C_IOMUX_L[14:12]=3'h2
spi3_miso	I/O	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	GRF_GPIO4C_IOMUX_H[6:4]=3'h2

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

26.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,
When SPI Controller works as master, the Fspi_clk>= 2 × (maximum Fsclk_out)
When SPI Controller works as slave, the Fspi_clk>= 6 × (maximum Fsclk_in)

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.
When the SPI serial slave is selected during configuration, it enables its txd data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

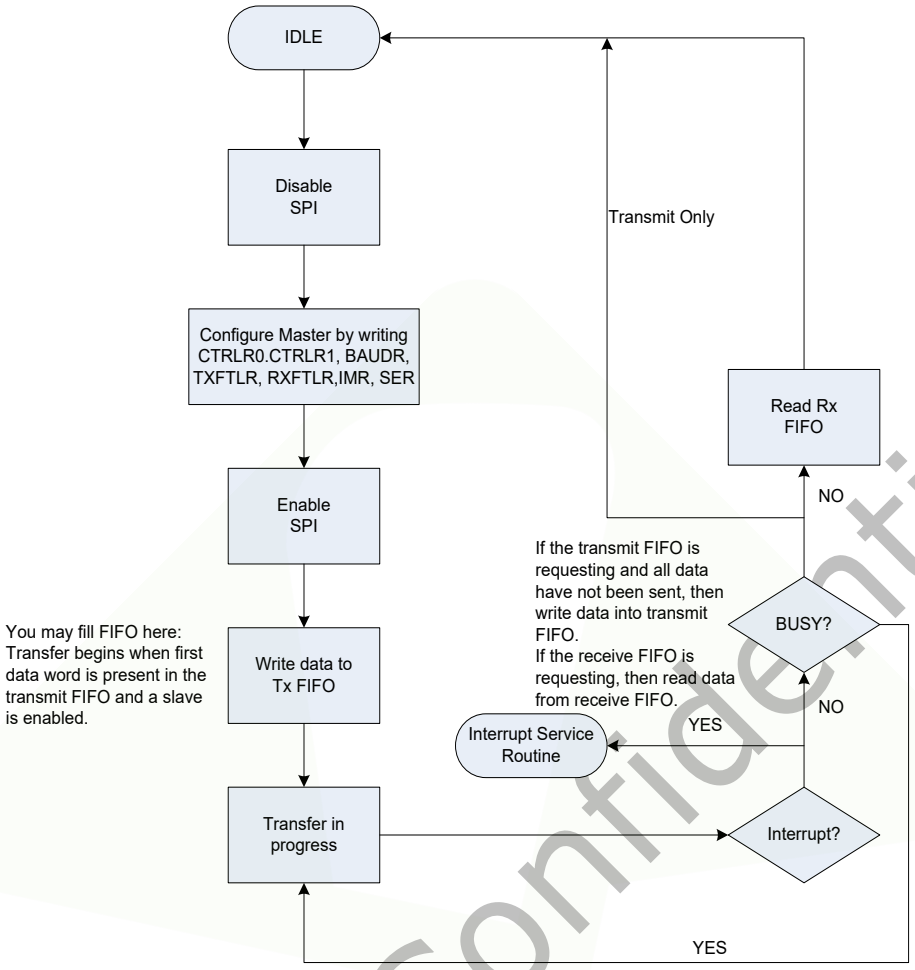


Fig. 26-7 SPI Master transfer flow diagram

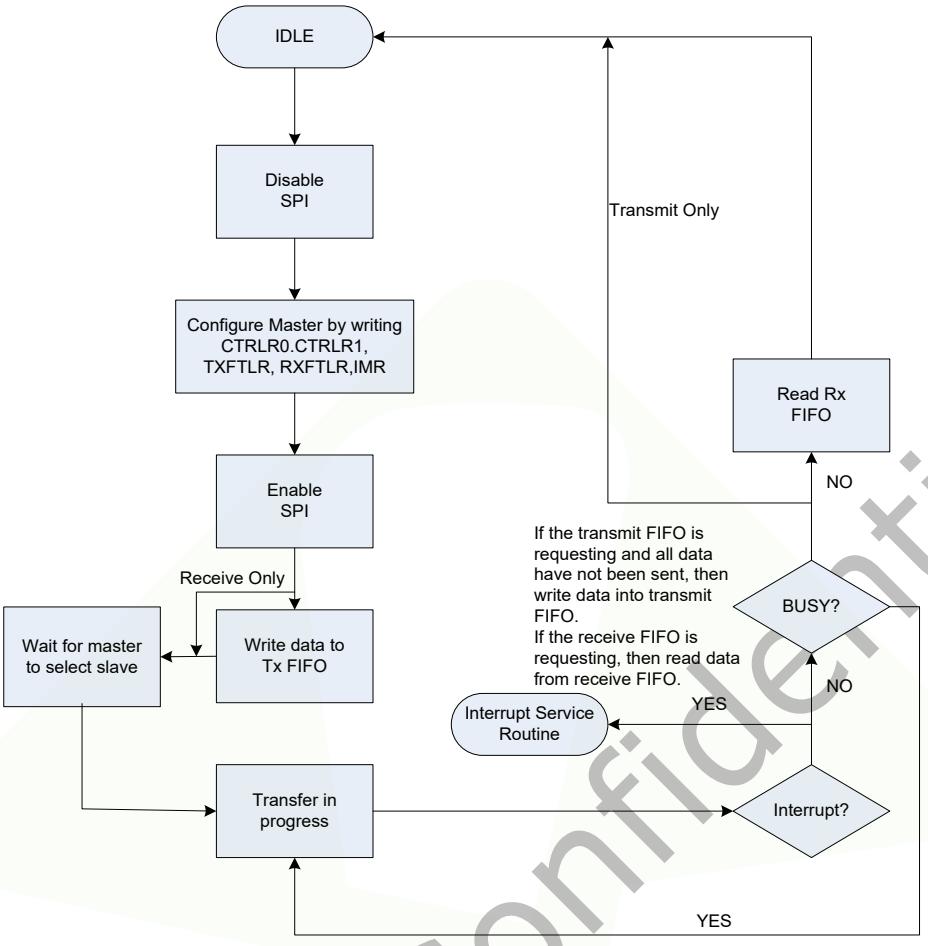


Fig. 26-8 SPI Slave transfer flow diagram

Chapter 27 Flexible Serial Peripheral Interface (FSPI)

27.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller SCLK
- Support maskable interrupt generation
- Support sampling clock with optionally configurable delay line
- Support 2 CS# operation

27.2 Block Diagram

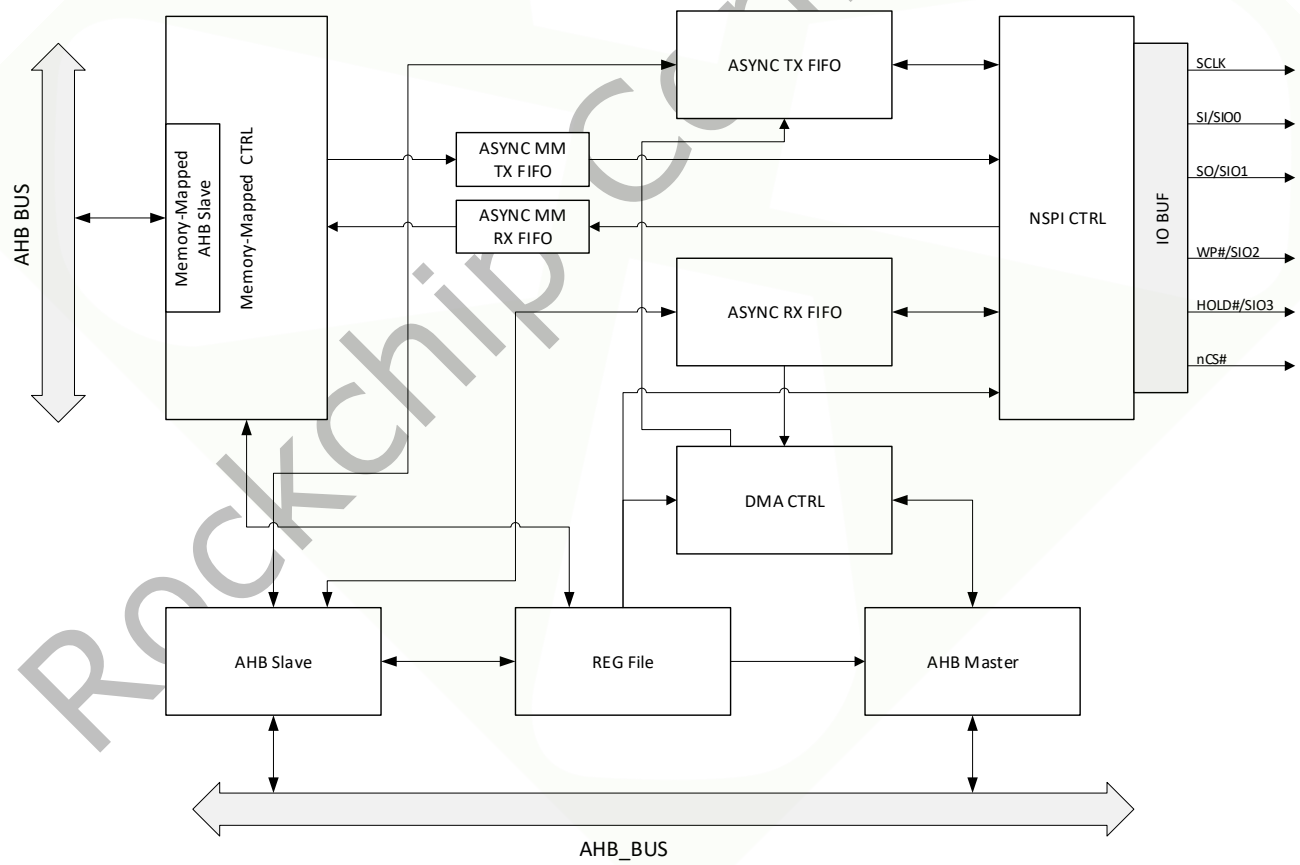


Fig. 27-1 FSPI Architecture

27.3 Function Description

27.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible

command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

27.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

27.3.3 Memory-Mapped AHB Slave

After the software initialize the controller based on the specialized memory device, CPU and other system bus masters can read data from external memory directly. If the external memory is SRAM or pSRAM, it also supports write data to it. The Memory-Mapped AHB Slave module can generate the relative CS# based on the access address from system address, example CS#0 and CS#1. Non-Supported in this chip.

27.3.4 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

27.3.5 DMA CTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

27.3.6 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

27.3.7 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

27.4 Register Description

27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 27-1 FSPI Address Mapping Table

Name	Address Base	Size
FSPI CFG	0xFE300000	64KB

27.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FSPI_CTRL0	0x0000	W	0x00000000	Control Register for CS0 Device
FSPI_IMR	0x0004	W	0x000001FF	Interrupt Mask Register
FSPI_ICLR	0x0008	W	0x00000000	Interrupt Clear Register
FSPI_FTLR	0x000C	W	0x00001010	FIFO Threshold Level Register
FSPI_RCVR	0x0010	W	0x00000000	FSPI Recover Register
FSPI_AX0	0x0014	W	0x00000000	FSPI Auxiliary Data Value for CS0 Device
FSPI_ABIT0	0x0018	W	0x00000000	Extend Address Bits for CS0 Device
FSPI_ISR	0x001C	W	0x00000000	Interrupt Status
FSPI_FSR	0x0020	W	0x00000001	FIFO Status Register
FSPI_SR	0x0024	W	0x00000000	FSPI Status Register
FSPI_RISR	0x0028	W	0x00000000	Raw Interrupt Status Register
FSPI_VER	0x002C	W	0x00000004	Version Register

Name	Offset	Size	Reset Value	Description
FSPI_QOP	0x0030	W	0x00000000	Quad Line Operation IO Level Pre-set Register
FSPI_EXT_CTRL	0x0034	W	0x00004023	Extend Control Register
FSPI_DLL_CTRL0	0x003C	W	0x00000001	Delay Line Control Register for CS0 Device
FSPI_EXT_AX	0x0044	W	0x0000F0FF	Extend Auxiliary Data Control Register
FSPI_SCLK_INATM_CNT	0x0048	W	0xFFFFFFFF	SCLK Inactive Timeout Counter
FSPI_XMMC_WCMD0	0x0050	W	0x00000000	Memory Mapped Control Write Command Register for CS0 Device
FSPI_XMMC_RCMD0	0x0054	W	0x00000000	Memory Mapped Control Read Command Register for CS0 Device
FSPI_XMMC_CTRL	0x0058	W	0x000072E0	Memory Mapped Control Register
FSPI_MODE	0x005C	W	0x00000000	Controller Working Mode Register
FSPI_DEVRGN	0x0060	W	0x00000017	Device Region Size Register
FSPI_DEVSIZE0	0x0064	W	0x00000012	Device Size Register for CS0 Device
FSPI_TME0	0x0068	W	0x00000000	Timeout Enable Control Register for CS0 Device
FSPI_XMMC_RX_WTMRK	0x0070	W	0x00000002	Memory Mapped Mode Receiver FIFO Water Mark Register
FSPI_DMATR	0x0080	W	0x00000000	DMA Trigger Register
FSPI_DMAADDR	0x0084	W	0x00000000	DMA Address Register
FSPI_LEN_CTRL	0x0088	W	0x00000000	Length Control Register
FSPI_LEN_EXT	0x008C	W	0x00000000	Length Extended Register
FSPI_XMMCSR	0x0094	W	0x00000000	Memory Mapped Status Register
FSPI_CMD	0x0100	W	0x00000000	Indirect Command Register
FSPI_ADDR	0x0104	W	0x00000000	Address Register
FSPI_DATA	0x0108	W	0x00000000	Data Register
FSPI_CTRL1	0x0200	W	0x00000000	Control Register for CS1 Device
FSPI_AX1	0x0214	W	0x00000000	FSPI Auxiliary Data Value for CS1 Device
FSPI_ABIT1	0x0218	W	0x00000000	Extend Address Bits for CS1 Device
FSPI_DLL_CTRL1	0x023C	W	0x00000001	Delay Line Control Register for CS1 Device
FSPI_XMMC_WCMD1	0x0250	W	0x00000000	Memory Mapped Control Write Command Register for CS1 Device
FSPI_XMMC_RCMD1	0x0254	W	0x00000000	Memory-Mapped Command Control Register for CS1 Device
FSPI_DEVSIZE1	0x0264	W	0x00000012	Device Size Register for CS1 Device
FSPI_TME1	0x0268	W	0x00000000	Timeout Enable Control Register for CS1 Device

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

27.4.3 Detail Registers Description

FSPI_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_IMR

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

Bit	Attr	Reset Value	Description
7	RW	0x1	DMAM DMA Finish Interrupt Mask 1'b0: DMA finish interrupt is not masked 1'b1: DMA finish interrupt is masked Only valid in indirect access mode.
6	RW	0x1	NSPIM NSPI Interrupt Mask 1'b0: NSPI interrupt is not masked 1'b1: NSPI interrupt is masked Valid in indirect access mode and memory mapped mode.
5	RW	0x1	AHBM AMBA AHB Error Interrupt Mask 1'b0: AMBA AHB Error interrupt is not masked 1'b1: AMBA AHB Error interrupt is masked Only valid in indirect access mode.
4	RW	0x1	TRANSM Transfer Finish Interrupt Mask 1'b0: Transfer finish interrupt is not masked 1'b1: Transfer finish interrupt is masked Only valid in indirect access mode.
3	RW	0x1	TXEM Transmit FIFO Empty Interrupt Mask 1'b0: Transmit FIFO empty interrupt is not masked 1'b1: Transmit FIFO empty interrupt is masked Only valid in indirect access mode.
2	RW	0x1	TXOM Transmit FIFO Overflow Interrupt Mask 1'b0: Transmit FIFO overflow interrupt is not masked 1'b1: Transmit FIFO overflow interrupt is masked Only valid in indirect access mode.
1	RW	0x1	RXUM Receive FIFO Underflow Interrupt Mask 1'b0: Receive FIFO underflow interrupt is not masked 1'b1: Receive FIFO underflow interrupt is masked Only valid in indirect access mode.
0	RW	0x1	RXFM Receive FIFO Full Interrupt Mask 1'b0: Receive FIFO full interrupt is not masked 1'b1: Receive FIFO full interrupt is masked Only valid in indirect access mode.

FSPI_ICLR

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	DMAC DMA Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMAS
6	W1C	0x0	NSPIC NSPI Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NSPIS.

Bit	Attr	Reset Value	Description
5	W1C	0x0	AHBC AMBA AHB Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the AHBS.
4	W1C	0x0	TRANSC Transfer Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TRANSS.
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXES.
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXOS.
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXUS.
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXFS.

FSPI_FTLR

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x10	RXFTLR Receive FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x10	TXFTLR Transmit FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

FSPI_RCVR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	RCVR FSPI Recover Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state.

FSPI_AX0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_ISR

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	NSPIS NSPI Transaction Decode Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

Bit	Attr	Reset Value	Description
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

FSPI_FSR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 5'h0: FIFO is empty 5'h1: 1 entry is taken ... 5'h10: 16 entry is taken, FIFO is full
15:13	RO	0x0	reserved
12:8	RO	0x00	TXWLVL TX FIFO Water Level 5'h0: FIFO is full 5'h1: 1 entry is left ... 5'h10: 16 entry is left, FIFO is empty
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 1'b0: RX FIFO is not full 1'b1: RX FIFO is full
2	RO	0x0	RXES Receive FIFO Empty Status 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 1'b0: TX FIFO is not empty 1'b1: TX FIFO is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 1'b0: TX FIFO is not full 1'b1: TX FIFO is full

FSPI_SR

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RO	0x0	SR Status Register 1'b0: NSPI Controller is idle 1'b1: NSPI Controller is busy When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device.

FSPI_RISR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
6	RO	0x0	NSPIS NSPI Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

Bit	Attr	Reset Value	Description
0	RO	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

FSPI_VER

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0005	VER The Version ID of FSPI

FSPI_QOP

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SO123BP SO123 Bypass Mode 1'b0: Disable bypass 1'b1: Enable bypass Default is enabled.
0	RW	0x0	SO123 D1/D2/D3 Data Value During Inactive When CS is Active 1'b0: Set to "0" 1'b1: Set to "1" The value of SO1, SO2 and SO3 during command and address bits input.

FSPI_EXT_CTRL

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	SR_GEN_MODE Status Register Generation Mode 1'b0: Compatible mode with old controller 1'b1: Robust generation to indicates the status of controller If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high.
13	RW	0x0	TRANS_INT_MODE Transmit Done Interrupt Generation Mode 1'b0: Trigger NSPI end in data done 1'b1: Trigger NSPI end in CS inactive Default Generation is compatible with old controller.
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	SWITCH_IO_O2I_CNT Switch IO Attribute Cycles in O2I Idle Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in O2I idle phase.
7:4	RW	0x2	SWITCH_IO_DUMM_CNT Switch IO Attribute Cycles in Dummy Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in Dummy data phase.
3:0	RW	0x3	CS_DESEL_CTRL CS Inactive Control 4'h0: 1 cycle 4'h1: 2 cycles 4'h2: 3 cycles 4'h3: 4 cycles ... 4'hf: 16 cycles The target cycles to hold CS inactive after de-assert the CS. Default value are 4 SCLK cycles that is enough for normal device.

FSPI_DLL_CTRL0

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_EXT_AX

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0xf0	AX_SETUP_PAT Auxiliary Setup Data Pattern The AX data pattern that setup the continuous/enhance/XIP read mode
7:0	RW	0xff	AX_CANCEL_PAT Auxiliary Cancel Data Pattern The AX data pattern that cancel the continuous/enhance/XIP read mode.

FSPI_SCLK_INATM_CNT

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	SCLK_INATM_CNT SCLK Inactive Timeout Counter When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed.

FSPI_XMMC_WCMD0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD0

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

Bit	Attr	Reset Value	Description
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_CTRL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	reserved
12	RO	0x0	reserved
11:8	RO	0x0	reserved
7	RO	0x0	reserved
6	RW	0x1	PFT_EN Prefetch Enable 1'b0: Disable 1'b1: Enable Should disable prefetch if controller communicate with pSRAM which need refresh.
5	RW	0x1	DEV_HWEN Device AMBA AHB HWRITE Enable 1'b0: Disable 1'b1: Enable
4:0	RO	0x00	reserved

FSPI_MODE

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	XMMC_MODE_EN Memory Mapped Mode Enable 1'b0: Disable, indirect access mode 1'b1: Enable, Memory-Mapped mode Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that.

FSPI_DEVRGN

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DEC_CTRL Decode Control 2'b00: 1 CS# 2'b01: 2 CS# 2'b10: 4 CS# 2'b11: Reserved Only valid in XMMC mode.
7:5	RO	0x0	reserved
4:0	RW	0x17	RSIZE Region Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS.

FSPI_DEVSIZE0

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G byte Device size is used to generate slop over status.

FSPI_TME0

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_XMMC_RX_WTMRK

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x02	RX_FULL_WTMRK Memory Mapped Mode Receiver FIFO Water Mark. Default is enough.

FSPI_DMATR

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	DMATR DMA Trigger Write "1" to start the DMA transfer.

FSPI_DMAADDR

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAADDR DMA Address The destination or source data address in current system.

FSPI_LEN_CTRL

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRB_SEL Total Transfer Bytes Selection 1'b0: TRB controlled by CMD[TRB] 1'b1: TRB controlled by LEN_EXT

FSPI_LEN_EXT

Address: Operational Base + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRB_EXT Total Transfer Bytes Extended 32'd0: No data 32'd1: 1 Byte 32'd2: 2 Bytes ... Total data bytes number that will write to /read from the device.

FSPI_XMMCSR

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

Bit	Attr	Reset Value	Description
1	R/W SC	0x0	SLOPOVER1 Slop Over Register for CS1 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.
0	R/W SC	0x0	SLOPOVER0 Slop Over Register for CS0 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.

FSPI_CMD

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	WO	0x0	CS Device Chip Select. 2'b00: Chip select 0 2'b01: Chip select 1 2'b10: Reserved 2'b11: Reserved
29:16	WO	0x0000	TRB Total Transfer Bytes 14'd0: No data 14'd1: 1 Byte 14'd2: 2 Bytes ... Total data bytes number that will write to or read from the device.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in indirect access mode. If there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	WO	0x0	WR Write or Read 1'b0: Read 1'b1: Write
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in indirect access mode.

Bit	Attr	Reset Value	Description
7:0	WO	0x00	CMD Command Command data in indirect access mode.

FSPI_ADDR

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ADDR Address Register Indirect access start address data for current command sequence.

FSPI_DATA

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DATA Data Register Device data read or write from/to device.

FSPI_CTRL1

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.

Bit	Attr	Reset Value	Description
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_AX1

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT1

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ABIT Address Bits Extend 5'h0: 1 bit 5'h1: 2 bits ... 5'h1f: 32 bits Only valid when ADDRB is set to 2'b11.

FSPI_DLL_CTRL1

Address: Operational Base + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	SCLK_SMP_SEL SCLK sampling selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved

Bit	Attr	Reset Value	Description
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_XMMC_WCMD1

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD1

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.

Bit	Attr	Reset Value	Description
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_DEVSIZE1

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes Device size is used to generate slop over status.

FSPI_TME1

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

27.5 Interface Description

Table 27-2 FSPI(SFC) interface description

Module Pin	Dir。	Pin Name	IOMUX Setting
sfc_clk	O	FSPI_CLK/FLASH_ALE/GPIO1_D0_d	GRF_GPIO1D_IOMUX_L[3:0]=4'h1
sfc_csn0	O	FSPI_CS0n/FLASH_CS0n/GPIO1_D3_u	GRF_GPIO1D_IOMUX_L[15:12]=4'h1
sfc_csn1	O	EMMC_DATA_STROBE/FSPI_CS1n/FLASH_CLE/GPIO1_C6_d	GRF_GPIO1C_IOMUX_H[11:8]=4'h2
sfc_sio0	I/O	FSPI_D0/FLASH_RDY/GPIO1_D1_u	GRF_GPIO1D_IOMUX_L[7:4]=4'h1

Module Pin	Dir。	Pin Name	IOMUX Setting
sfc_sio1	I/O	FSPI_D1/FLASH_RDn/GPIO1_D2_u	GRF_GPIO1D_IOMUX_L[11:8]=4'h1
sfc_sio2	I/O	EMMC_RSTn/FSPI_D2/FLASH_WPn/GPIO1_C7_d	GRF_GPIO1C_IOMUX_H[15:12]=4'h2
sfc_sio3	I/O	FSPI_D3/FLASH_CS1n/GPIO1_D4_u	GRF_GPIO1D_IOMUX_H[3:0]=4'h1

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

27.6 Application Notes

27.6.1 Typical Program Flow Without DMA

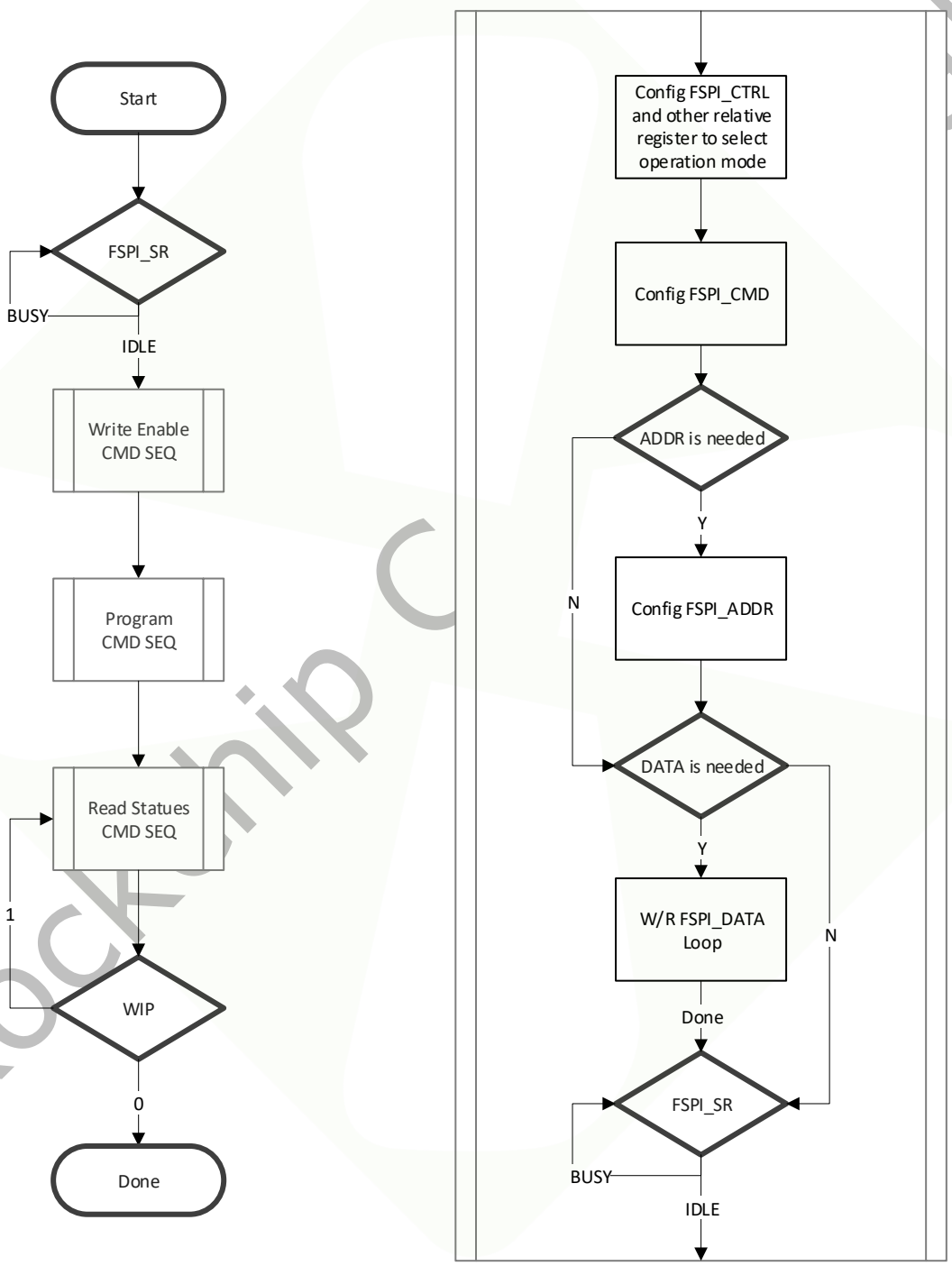


Fig.27-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

27.6.2 Typical READ Flow Without DMA

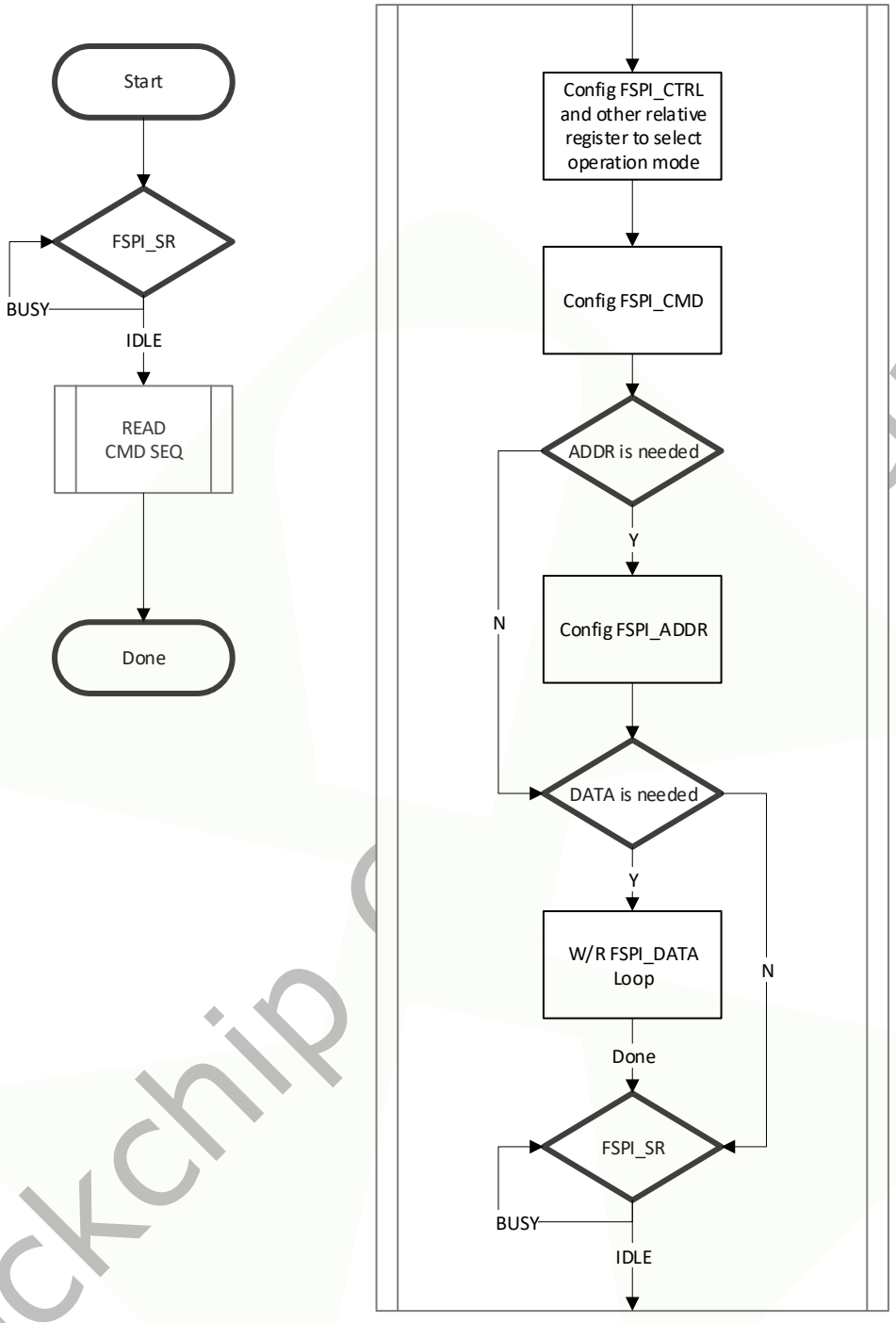


Fig.27-3 Read Flow

27.6.3 Command Flow with DMA

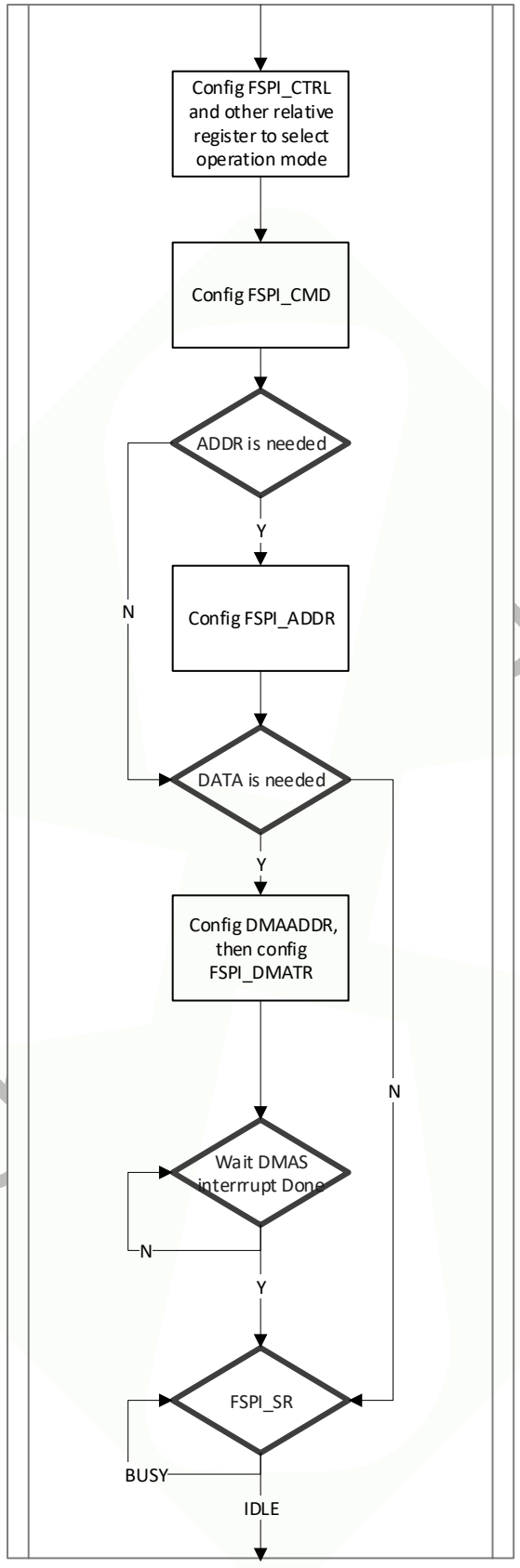


Fig.27-4 Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

27.6.4 SPI Mode and Shift Phase

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default value is 1, means SPI Mode 3.

The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of sclk_out. If SHIFTPHASE=1, it will sample the data at the negedge of sclk_out.

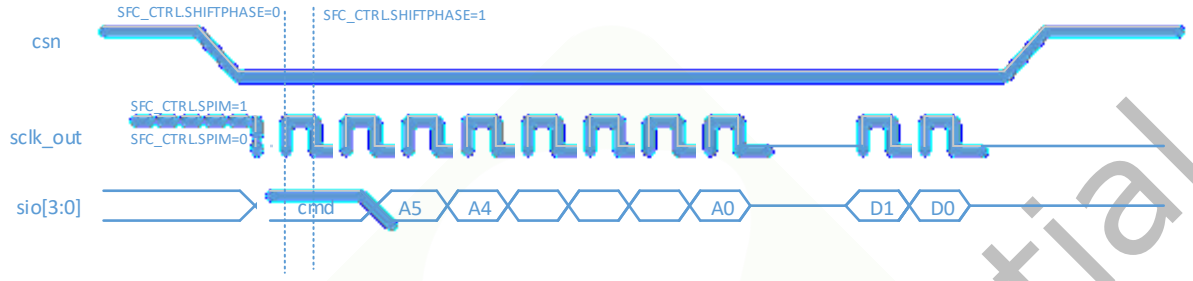


Fig.27-5 SPI mode

27.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (sclk) before reading the first bit of the read command.

Like the following picture shows: the red line of the sclk is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE =0, it means there will be not idle level cycles.

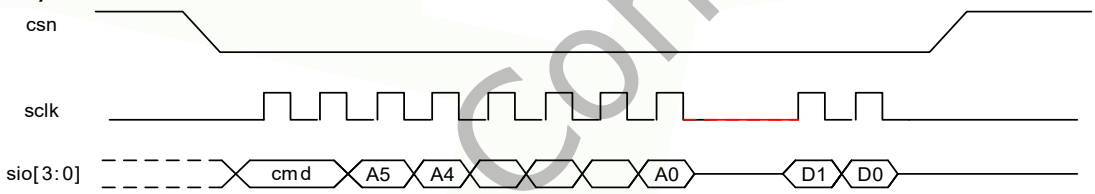


Fig.27-6 Idle cycles

27.6.6 Memory-Mapped Mode

After the Controller is configured as Memory-Mapped mode, the normal operation mode is not allowed which means indirect command transaction is forbidden unless software configures the FSPI_MODE back to indirect access mode.

Before switching into Memory-Mapped mode, the software should initiate some transactions to configure the external device, such as Quad IO enable and IO Drive Strength.

In Memory-Mapped mode, it supports read transaction from serial NOR Flash and serial pSRAM, and the write transaction is only support by serial pSRAM.