RK3566 RK3568 IO Domain Configuration Developer Guide

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Preface

Overview

The IO level of the controller's power domain must be matched with the IO level of the connected peripheral chip, and the voltage configuration of the software must be consistent with the voltage of the hardware. Otherwise, it may cause IO damage at worst.

There are 10 independent IO power domains in RK3566/RK3568, they are PMUIO[0:2] and VCCIO[1:7].

1. PMUIO0 and PMUIO1 are fixed-level power domains which cannot be configured;
2. PMUIO2 and VCCIO1,VCCIO[3:7]power domains require that their hardware power supply voltages must be consistent with the software configuration correspondingly:
   - When the hardware IO level is connected to 1.8V, the software voltage configuration should also be configured to 1.8V accordingly;
   - When the hardware IO level is connected to 3.3V, the software voltage configuration should also be configured to 3.3V accordingly
3. There is no need to configure VCCIO2 power domain by software, but its hardware power supply and FLASH_VOL_SEL status must be consistent:
   - When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high;
   - When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low;

Otherwise:

1. If the software configuration is 1.8V, but the hardware power supply is 3.3V, it will cause the low withstand voltage circuit working in overvoltage state, and the chipset will be damaged after long time working.
2. If the software configuration is 3.3V, but the hardware power supply is 1.8V, the circuit will work abnormally;

This document mainly introduce the ways to configure IO power domain of RK3566, RK3568 SDK platform, aiming to help developers to configure IO power domain correctly.

Product Version

Chipset	System Version	Kernel Version
RK3566、RK3568	Linux	Kernel 4.19
RK3566、RK3568	Android 11.0	Kernel 4.19

Intended Audience

This document (this guide) is mainly intended for:

- Technical support engineers
- Software development engineers
- Hardware development engineers

Revision History

Version	Author	Date	Change Description
V1.0.0	Caesar Wang	2021-05-15	Initial version
V1.0.1	Caesar Wang	2021-05-27	Update some description of IO power domain
V1.0.2	Caesar Wang	2021-06-02	Add Android and more detailed register introduction

Contents

1. Step 1: Obtain the Hardware Schematic Diagram and Check the Design of the Hardware Power Supply

It will take RK_EVB1_RK3568_DDR4P216SD6_V10_20200911 EVB board as an example to introduce in this document.

Hardware schematic diagram is: RK_EVB1_RK3568_DDR4P216SD6_V10_20200911.pdf

Power solution: checking from the hardware schematic, the power solution of the **EVB board RK_EVB1_RK3568_DDR4P216SD6_V10_20200911** is with a PMU (RK809-5).

2. Step 2: Find the Corresponding Kernel dts Configuration File

From the first step, it can be seen that the hardware power supply design of the EVB board is with a PMU , and the corresponding kernel dts configuration file is located in:

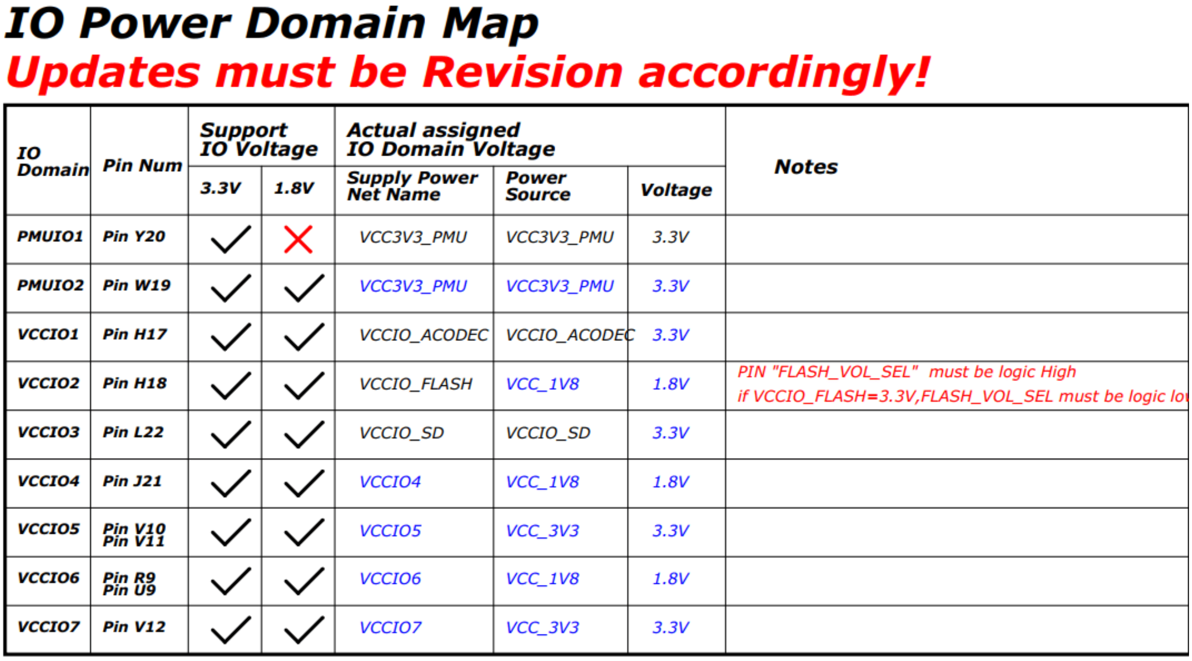
`<SDK>/kernel/arch/arm64/boot/dts/rockchip/rk3568-evb.dtsi` (The solution discussed in this document)

3. Step 3: Modify the Power Domain Configuration Node pmu_io_domains of the Kernel dts

The SDK default kernel dts power domain configuration file is as follows:

```
<SDK>/kernel/arch/arm64/boot/dts/rockchip/rk3568-evb.dtsi

&pmu_io_domains {
    status = "okay";
    pmuio2-supply = <&vcc_3v3>;
    vccio1-supply = <&vcc_3v3>;
    vccio3-supply = <&vcc_3v3>;
    vccio4-supply = <&vcc_3v3>;
    vccio5-supply = <&vcc_3v3>;
    vccio6-supply = <&vcc_3v3>;
    vccio7-supply = <&vcc_3v3>;
};
```

Next, we will take vccio1-supply as an example. Firstly, check the hardware schematic diagram to confirm that the configuration of vccio1 power domain (VCCIO1) as shown in the figure below:

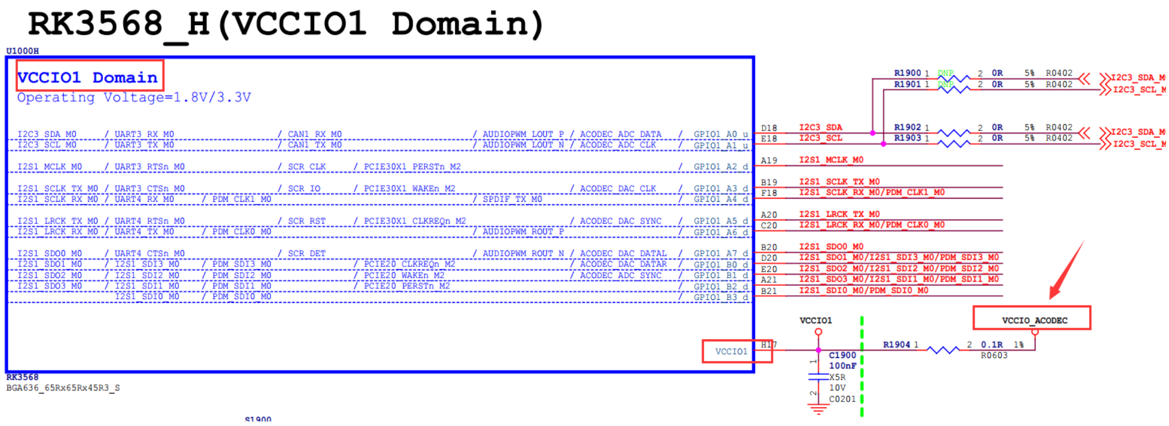


IO Power Domain Map

Updates must be Revision accordingly!

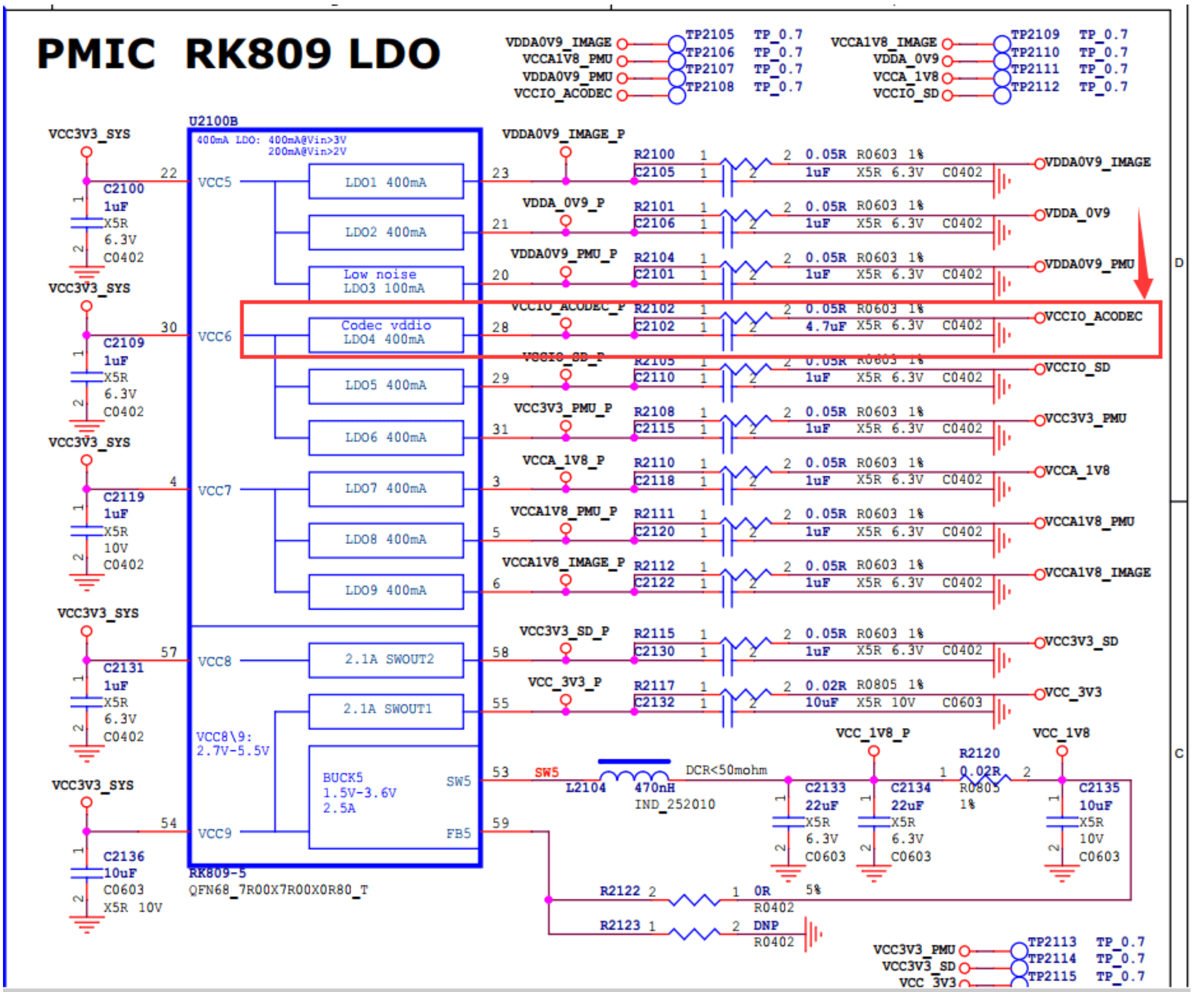
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic lo
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

Search for `VCCIO1` from the hardware schematic, as follows:



From the above figure, you will find that the power supply of `VCCIO1` is `vccio_acodec`.

Search for `vccio_acodec` from the schematic, as shown in the following figure.



From the above figure, you will find that `vccio_acodec` is powered by LDO4 of RK809.
Find the configuration information of LDO_REG4 (LDO4) from the dts file as follows:

```
vccio_acodec: LDO_REG4 {
        regulator-always-on;
        regulator-boot-on;
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
        regulator-name = "vccio_acodec";
        regulator-state-mem {
                regulator-off-in-suspend;
        };
};
```

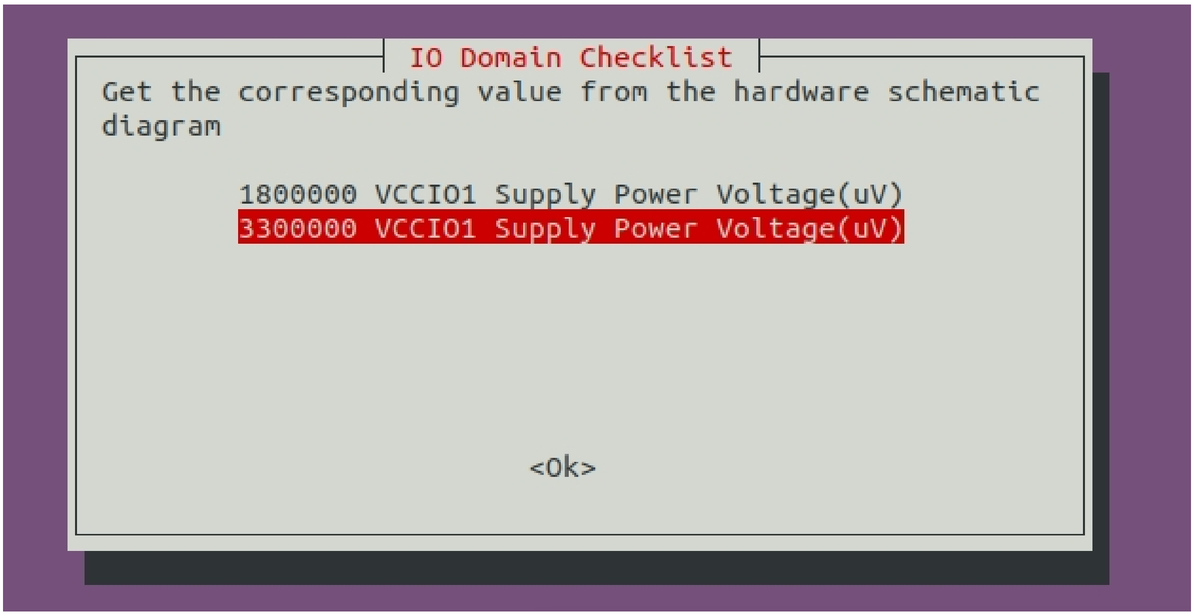
Change the "vccio1-supply = <&vcc_3v3>" to "vccio1-supply = <&vccio_acodec>" in the above pmu_io_domains node; you will complete the voltage configuration of vccio1:

```
&pmu_io_domains {
        status = "okay";
        pmuio2-supply = <&vcc_3v3>;
        vccio1-supply = <&vccio_acodec>;
        vccio3-supply = <&vcc_3v3>;
        vccio4-supply = <&vcc_3v3>;
        vccio5-supply = <&vcc_3v3>;
        vccio6-supply = <&vcc_3v3>;
        vccio7-supply = <&vcc_3v3>;
};
```

note:

- pmuio0 and pmuio1 are fixed-level power domains and they should not be configured by software;
- The vccio2 software does not need to be configured, but its hardware power supply voltage must be matched with the FLASH_VOL_SEL state: When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high; When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low;
- For other power domains (pmuio2 and VCCIO[3:7]), please refer to the configuration way of VCCIO1 above;

RK356X kernel compilation for the fist time will pop up IO-Domain confirmation dialog :



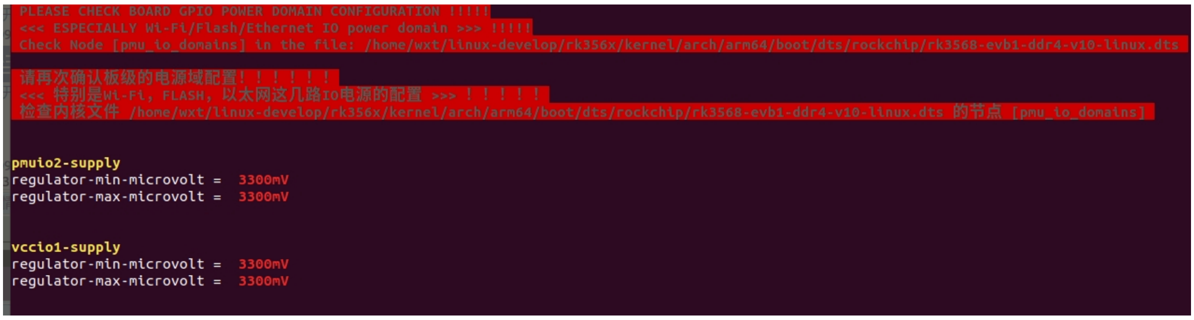
```
IO Domain Checklist
Get the corresponding value from the hardware schematic
diagram

        1800000 VCCIO1 Supply Power Voltage(uV)
        3300000 VCCIO1 Supply Power Voltage(uV)

                        <Ok>
```

The purpose of this dialog box is to check whether the actual hardware schematic diagram is matched with the IO voltage of the software or not. Customers need to choose according to the actual design voltage of the hardware schematic diagram of their projects(the value selected in the dialog will not be saved to the dts file which need to modify manually), if you are a software engineer, please check and confirm with your hardware engineers. **This is very important, please be sure to confirm!** If the IO voltage configuration is incorrect, it will cause the chip IO damage at worst.
When you confirm the IO voltage, this dialog will not pop up again (make sure the input values are the same as the dts configuration values). If the dts name or the io-domian in the dts changes, it will continue to pop up to confirm again.

4. Step 4: Check the Current Firmware IO Domain Configuration from SDK

After compiling Kernel, you can check the current power domain configuration from the Linux SDK, the way is as follows:

```
./build.sh info
```



```
 PLEASE CHECK BOARD GPIO POWER DOMAIN CONFIGURATION !!!!!
 <<< ESPECIALLY Wi-Fi/Flash/Ethernet IO power domain >>> !!!!!
 Check Node [pmu_io_domains] in the file: /home/wxt/linux-develop/rk356x/kernel/arch/arm64/boot/dts/rockchip/rk3568-evb1-ddr4-v10-linux.dts

 请再次确认板级的电源域配置！！！！！！
 <<< 特别是Wi-Fi，FLASH，以太网这几路IO电源的配置 >>> ！！！！！
 检查内核文件 /home/wxt/linux-develop/rk356x/kernel/arch/arm64/boot/dts/rockchip/rk3568-evb1-ddr4-v10-linux.dts 的节点 [pmu_io_domains]


pmuio2-supply
regulator-min-microvolt =  3300mV
regulator-max-microvolt =  3300mV


vccio1-supply
regulator-min-microvolt =  3300mV
regulator-max-microvolt =  3300mV
```

The way to check from the Android 11.0 SDK is as follows (this way is also suitable to the Linux SDK):

```
cat <SDK>/kernel/arch/arm64/boot/dts/rockchip/.rk3568-evb1-ddr4-v10-linux.dtb.dts.tmp.domain

PMUIO2 Supply Power Voltage1:3300000
VCCIO1 Supply Power Voltage1:3300000
VCCIO3 Supply Power Voltage1:3300000
VCCIO4 Supply Power Voltage1:3300000
VCCIO5 Supply Power Voltage1:3300000
VCCIO6 Supply Power Voltage1:3300000
VCCIO7 Supply Power Voltage1:3300000
```

5. Step 5: Confirm Whether the Register Value is Correct after Flashing the Firmware

Take **RK356X** chip as an example, get PMU_GRF_IO_VSEL0~PMU_GRF_IO_VSEL2 registers (base address are: 0xFDC20140~0xFDC20148)from the manual, they are shown as follows:

PMU_GRF_IO_VSEL0
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	poc_vccio7_sel25 VCCIO7 2.5V control 1'b0: Disable 1'b1: Enable
13	RW	0x0	poc_vccio6_sel25 VCCIO6 2.5V control 1'b0: Disable 1'b1: Enable
12	RW	0x0	poc_vccio5_sel25 VCCIO5 2.5V control 1'b0: Disable 1'b1: Enable
11	RW	0x0	poc_vccio4_sel25 VCCIO4 2.5V control 1'b0: Disable 1'b1: Enable
10	RW	0x0	poc_vccio3_sel25 VCCIO3 2.5V control 1'b0: Disable 1'b1: Enable
9	RW	0x0	poc_vccio2_sel25 VCCIO2 2.5V control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio1_sel25 VCCIO1 .25V control 1'b0: Disable 1'b1: Enable
7	RW	0x0	poc_vccio7_sel18 VCCIO7 1.8V control 1'b0: Disable 1'b1: Enable

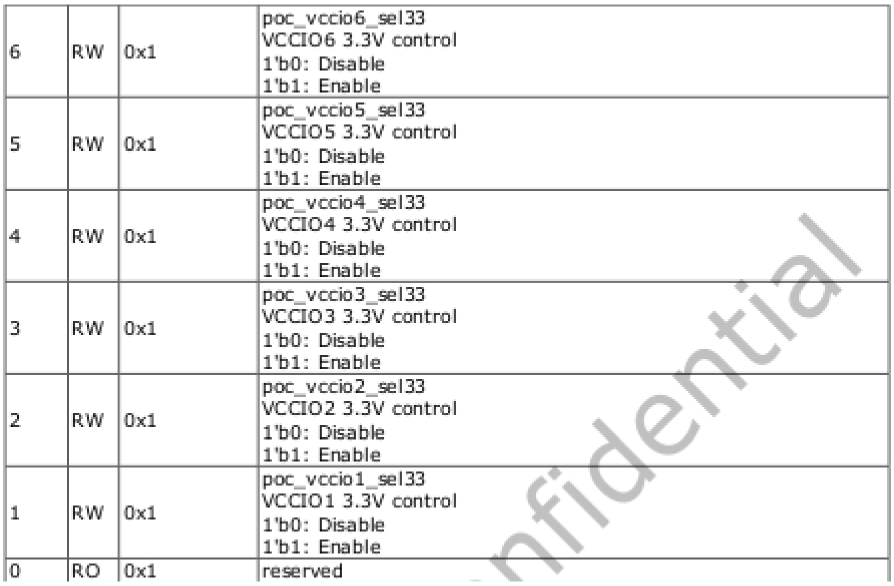
6	RW	0x0	poc_vccio6_sel18 VCCIO6 1.8V control 1'b0: Disable 1'b1: Enable
5	RW	0x0	poc_vccio5_sel18 VCCIO5 1.8V control 1'b0: Disable 1'b1: Enable
4	RW	0x0	poc_vccio4_sel18 VCCIO4 1.8V control 1'b0: Disable 1'b1: Enable
3	RW	0x0	poc_vccio3_sel18 VCCIO3 1.8V control 1'b0: Disable 1'b1: Enable

Bit	Attr	Reset Value	Description
2	RW	0x0	poc_vccio2_sel18 VCCIO2 1.8V control 1'b0: Disable 1'b1: Enable
1	RW	0x0	poc_vccio1_sel18 VCCIO1 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	vccio2 voltage control select VCCIO2 voltage control selection 1'b0: from GPIO_0A7 1'b1: from GRF

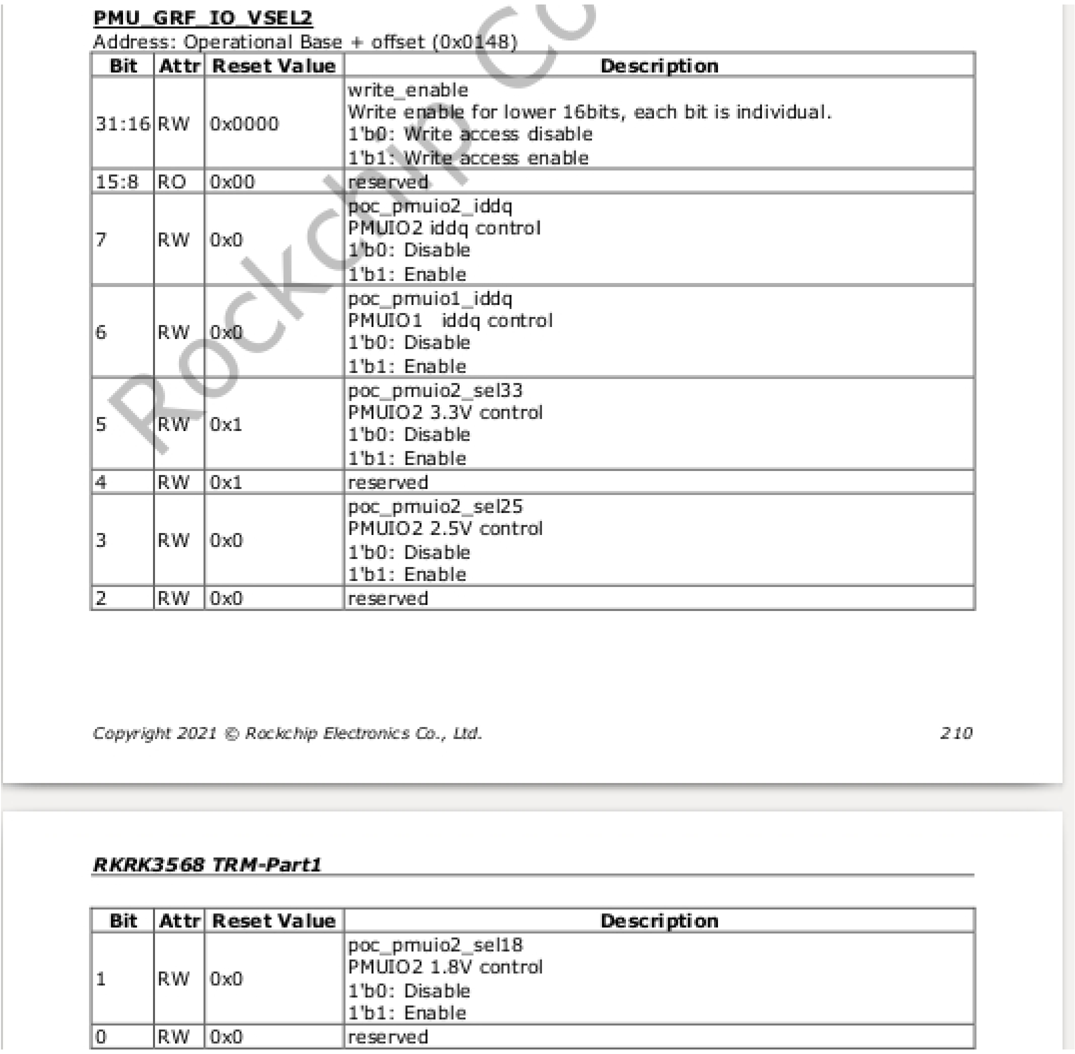
PMU_GRF_IO_VSEL1

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	poc_vccio7_iddq VCCIO7 iddq control 1'b0: Disable 1'b1: Enable
13	RW	0x0	poc_vccio6_iddq VCCIO6 iddq control 1'b0: Disable 1'b1: Enable
12	RW	0x0	poc_vccio5_iddq VCCIO5 iddq control 1'b0: Disable 1'b1: Enable
11	RW	0x0	poc_vccio4_iddq VCCIO4 iddq control 1'b0: Disable 1'b1: Enable
10	RW	0x0	poc_vccio3_iddq VCCIO3 iddq control 1'b0: Disable 1'b1: Enable
9	RW	0x0	poc_vccio2_iddq VCCIO2 iddq control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio1_iddq VCCIO1 iddq control 1'b0: Disable 1'b1: Enable
7	RW	0x1	poc_vccio7_sel33 VCCIO7 3.3V control 1'b0: Disable 1'b1: Enable



6	RW	0x1	poc_vccio6_sel33 VCCIO6 3.3V control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_vccio5_sel33 VCCIO5 3.3V control 1'b0: Disable 1'b1: Enable
4	RW	0x1	poc_vccio4_sel33 VCCIO4 3.3V control 1'b0: Disable 1'b1: Enable
3	RW	0x1	poc_vccio3_sel33 VCCIO3 3.3V control 1'b0: Disable 1'b1: Enable
2	RW	0x1	poc_vccio2_sel33 VCCIO2 3.3V control 1'b0: Disable 1'b1: Enable
1	RW	0x1	poc_vccio1_sel33 VCCIO1 3.3V control 1'b0: Disable 1'b1: Enable
0	RO	0x1	reserved



PMU_GRF_IO_VSEL2

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	poc_pmuio2_iddq PMUIO2 iddq control 1'b0: Disable 1'b1: Enable
6	RW	0x0	poc_pmuio1_iddq PMUIO1 iddq control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_pmuio2_sel33 PMUIO2 3.3V control 1'b0: Disable 1'b1: Enable
4	RW	0x1	reserved
3	RW	0x0	poc_pmuio2_sel25 PMUIO2 2.5V control 1'b0: Disable 1'b1: Enable
2	RW	0x0	reserved

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RKRK3568 TRM-Part1

Bit	Attr	Reset Value	Description
1	RW	0x0	poc_pmuio2_sel18 PMUIO2 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	reserved

In order to ensure that customers can use safely, the current IO Domain configuration of the SDK are all set to 3.3V, and the value of the register are shown in the following table, but some functions may be abnormal.

Register	Address	Read Command	Value
PMU_GRF_IO_VSEL0	0xFDC20140	io -4 -r 0xFDC20140	0x00000000
PMU_GRF_IO_VSEL1	0xFDC20144	io -4 -r 0xFDC20144	0x000000ff
PMU_GRF_IO_VSEL2	0xFDC20148	io -4 -r 0xFDC20148	0x00000030

If you need to restore the EVB function configuration, you need to revert the Kernel commit (git revert e18c51f465dd0dd0185f5). However, please note that the dts configuration of this EVB is only applicable to our EVB and cannot be used in customer's projects at will. Customers need to modify the corresponding dts configuration according to the actual hardware power supply voltage of their respective projects.

```
commit e18c51f465dd0dd0185f5f80a72699fca0a68adc
Author: Wu Liangqing <wlq@rock-chips.com>
Date: Mon May 24 09:31:10 2021 +0800
```