# RK3568 Hardware Design Guide

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# Preface

## Overview

This document presents the key points of hardware design and notices for RK3568 processors, aiming to help customers shorten developing period of product, improving product design stability and reducing fault rate. Please refer to the requirements of this guide for hardware design, and use the relevant core templates released by Rockchip. If you need to modify for special reasons, please strictly follow the design rule of high-speed-digital-circuit and Rockchip Schematic&PCB checklist requirements.

## Chipset Model

This document is suitable for the following chipset model: **RK3568**

## Intended Audience

This document (this guide) is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

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# Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

| Version No. | Author | Revision Date | Revision Description | Remark |
|---|---|---|---|---|
| V1.2 | Zhangdz | 2021-10-14 | 1:Update the description of ECC (Section 2.1.7.2) | |
| V1.1 | Zhangdz | 2021-06-08 | 1: Update the description of wake-up and standby of infrared receiver (Section 2.3.17)<br>2: Add IO Domain power supply and software configuration attentions (Section 2.1.11)<br>3: Update the DCDC power supply capacity requirements of VDD_NPU and VDD_LOGIC power supplies, which require 2A or more (Section 2.2.2.6 and 2.2.2.7)<br>4: VDD_LOGIC peak current is updated to 1.2A (Section 2.2.6)<br>5: Add a description of the module that does not supply power, and the corresponding node in DTS should be disabled (Section 2.2.2.1) | |
| V1.0 | Zhangdz | 2021-04-16 | The initial release version | |
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# Acronyms

Acronyms include the abbreviations of commonly used phrases in this document:

| | | |
|---|---|---|
| ARM | Advanced RISC Machine | 高级精简指令集计算机 |
| CAN | Controller Area Network | 控制器局域网络 |
| CEC | Consumer Electronics Control | 消费电子控制 |
| CIF | Camera Input Format | 相机并行接口 |
| CPU | Central processing unit | 中央处理器 |
| CSI | Camera Serial Interface | 相机串行接口 |
| DC/DC | Direct current-Direct current converter | 直流/直流变换器 |
| DDR | Double Data Rate | 双倍速率同步动态随机存储器 |
| DP | DisplayPort | 显示接口 |
| DSI | Display Serial Interface | 显示串行接口 |
| EBC | E-book controller | 电子书控制器 |
| eDP | Embedded DisplayPort | 嵌入式数码音视讯传输接口 |
| eMMC | Embedded Multi Media Card | 内嵌式多媒体存储卡 |
| ESD | Electro-Static discharge | 静电释放 |
| ESR | Equivalent Series Resistance | 等效电阻 |
| Flash_VOL_SEL | Flash voltage selection | eMMC/Nand Flash IO电压选择 |
| FSPI | Flexible Serial Peripheral Interface | 灵活串行外设接口 |
| GPU | Graphics Processing Unit | Figure形处理单元 |
| HDMI | High Definition Multimedia Interface | 高清晰度多媒体接口 |
| HPD | Hot Plug Detect | 热插拔检测 |
| I2C | Inter-Integrated Circuit | 内部整合电路(两线式串行通讯总线) |
| I2S | Inter-IC Sound | 集成电路内置音频总线 |
| ISP | Image Signal Processing | Figure像信号处理 |
| JTAG | Joint Test Action Group | 联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容） |
| LDO | Low Drop Out Linear Regulator | 低压差线性稳压器 |
| LCDC | LCD Controller | LCD 控制器并行接口 |
| LCM | LCD Module | LCD显示模组 |
| LVDS | Low-Voltage Differential Signaling | 低电压差分信号 |
| MAC | Media Access Control | 以太网媒体接入控制器 |
| MIPI | Mobile Industry Processor Interface | 移动产业处理器接口 |
| NPU | Neural network Processing Unit | 神经网络处理器 |
| PCB | Printed Circuit Board | 印制电路板 |

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| | | |
|---|---|---|
| PCIe | Peripheral Component Interconnect -express | 外设组件互联标准 |
| PCM | Pulse Code Modulation | 脉冲编码调制 |
| PDM | Pulse density modulation | 脉冲密度调制 |
| PLL | Phase-locked loop | 锁相环 |
| PMIC | Power Management IC | 电源管理芯片 |
| PMU | Power Management Unit | 电源管理单元 |
| PWM | Pulse width modulation | 脉冲宽度调制 |
| QSGMII | Quad Serial Gigabit Media Independent Interface | 四串行千兆媒体独立接口 |
| RGB | RGB color mode is a color standard in industry | RGB色彩模式，是工业界的一种颜色标准 |
| GMAC | Gigabit Media Access Controller | 千兆媒体访问控制器 |
| RGMII | Reduced Gigabit Media Independent Interface | 简化千兆媒体独立接口 |
| RMII | Reduced Media Independent Interface | 简化媒体独立接口 |
| RK | Rockchip Electronics Co.,Ltd. | 瑞芯微电子股份有限公司 |
| SARADC | successive approximation register Analog to digital converter | 逐次逼近寄存器型模数转换器 |
| SATA | Serial Advanced Technology Attachment | 串行高级技术附件 |
| SCR | Smart Card Reader | 智能卡读卡器 |
| SD Card | Secure Digital Memory Card | 安全数码卡 |
| SDIO | Secure Digital Input and Output Card | 安全数字输入输出卡 |
| SDMMC | Secure Digital Multi Media Card | 安全数字多媒体存储卡 |
| SGMII | Serial Gigabit Media Independent Interface | 串行千兆媒体独立接口 |
| SPDIF | Sony/Philips Digital Interface Format | SONY、PHILIPS数字音频接口 |
| SPI | Serial Peripheral Interface | 串行外设接口 |
| SubLVDS | Sub- Low-Voltage Differential Signaling | 低摆幅差分信号技术 |
| TF Card | Micro SD Card(Trans-flash Card) | 外置记忆卡 |
| TSADC | Temperature sensing A / D converter | 温度感应模数转换器 |
| UART | Universal Asynchronous Receiver / Transmitter | 通用异步收发传输器 |
| VOP | Video Output Processor | 视频输出处理器 |
| VPU | Video Processing Unit | 视频处理器 |
| USB2.0 | Universal Serial Bus 2.0 | 通用串行总线 |
| USB3.0 | Universal Serial Bus 3.0 | 通用串行总线 |

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# Contents



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# Figures



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# Tables



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# 1 System Introduction

## 1.1 Overview

RK3568 is a low-power and high-performance processor designed for personal mobile Internet devices and AIoT devices.

RK3568 provides many powerful embedded hardware engines to optimize the performance of advanced applications. RK3568 supports almost all formats of H.264 4k@60fps decoding, and supports H.265 4k@60fps decoding, H.264/ H.265 1080p@60fps encoding, and high-quality JPEG encoding/decoding.

RK3568 embedded 3D GPU is fully compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1; the special 2D hardware engine maximizes the display performance and provides a smooth operating experience also.

The built-in NPU supports INT8/INT16 mixed operation. Due to strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

There are high-performance external memory interfaces in RK3568 to ensure high-capacity and high-stability system operating memory bandwidth, and it supports multiple memory models such as DDR3, DDR3L, LPDDR3, DDR4, LPDDR4, LPDDR4X, etc.

## 1.2 Block Diagram

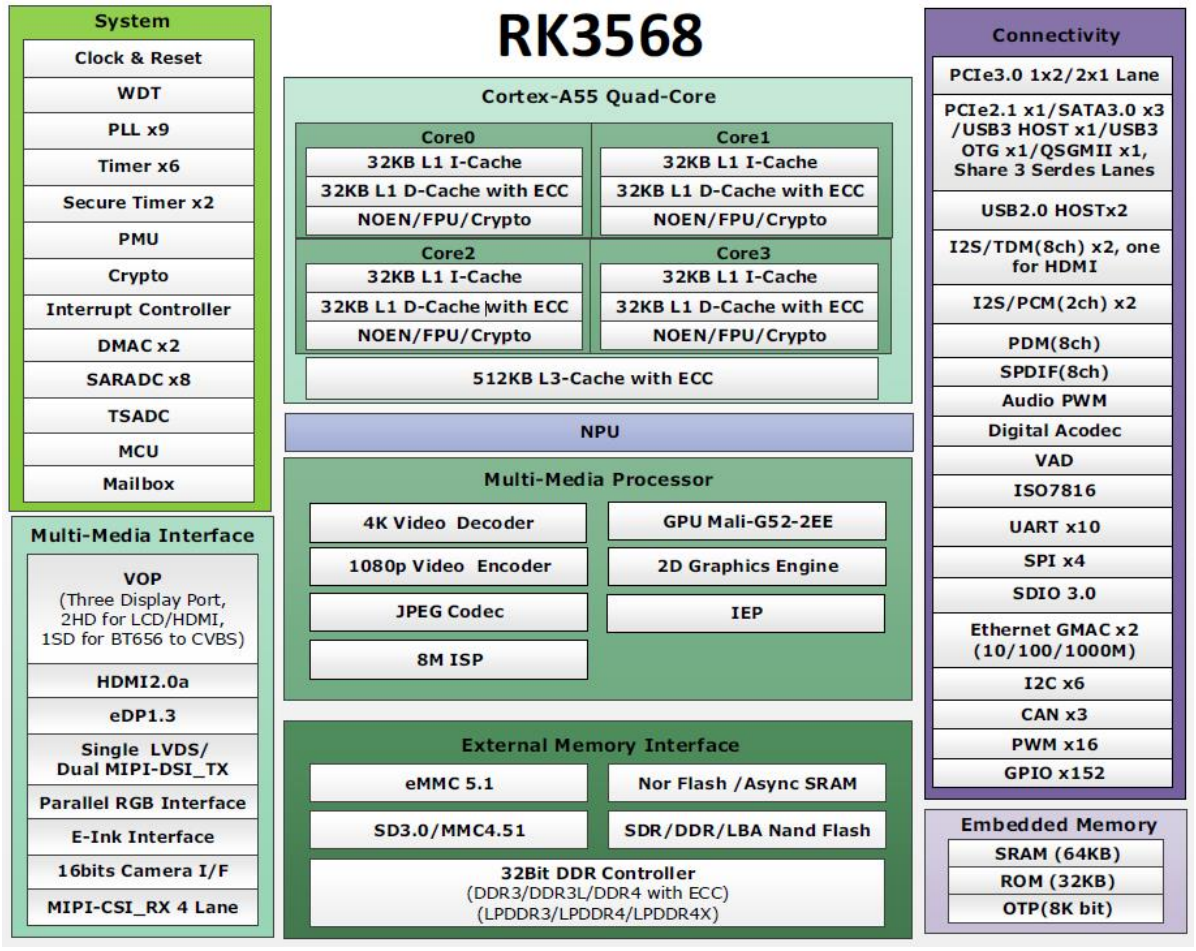


Figure 1-1 RK3568 block diagram

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## 1.3 Application Block Diagram

### 1.3.1 RK3568 EVB Application Block Diagram

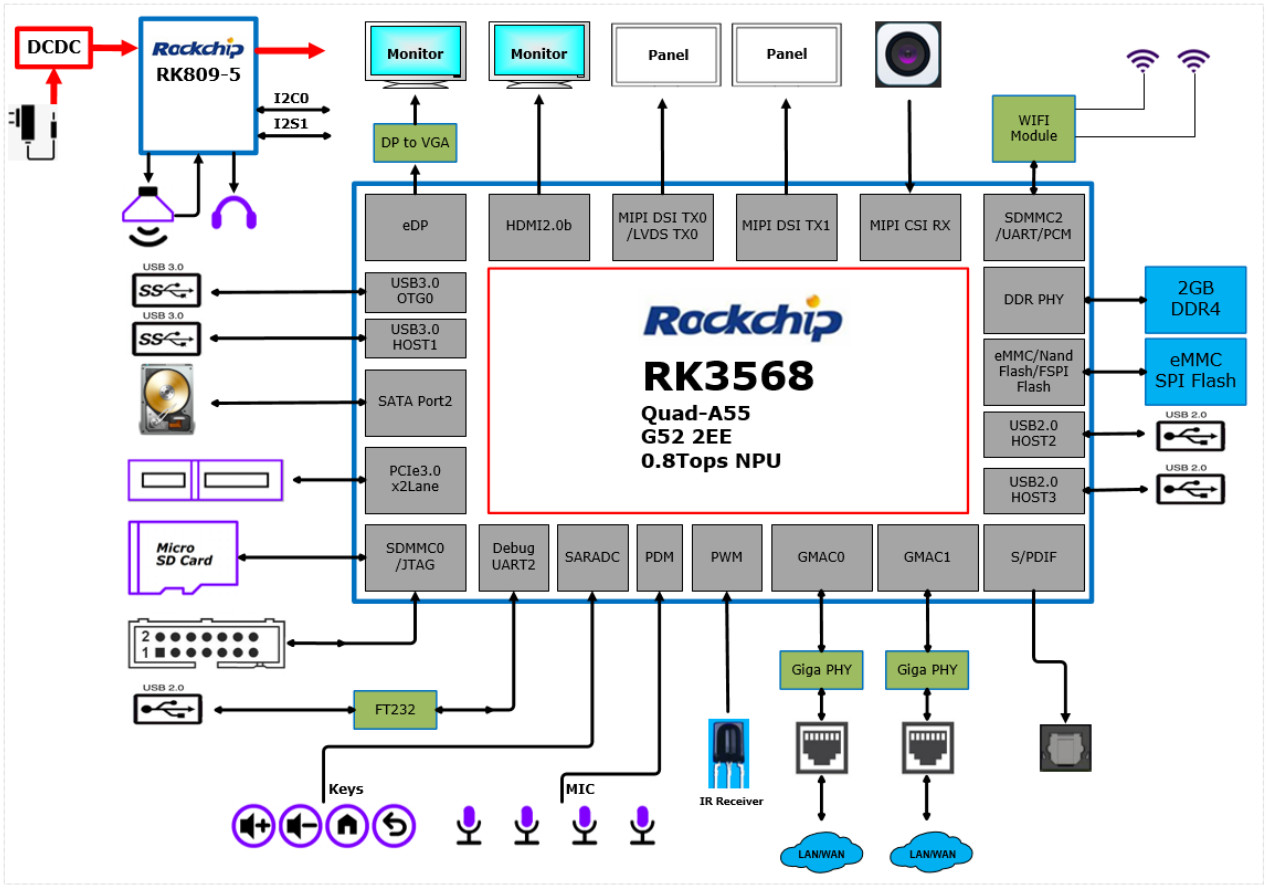


Figure 1-2 RK3568 EVB application block diagram

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### 1.3.2 RK3568 Smart NVR Application Block Diagram

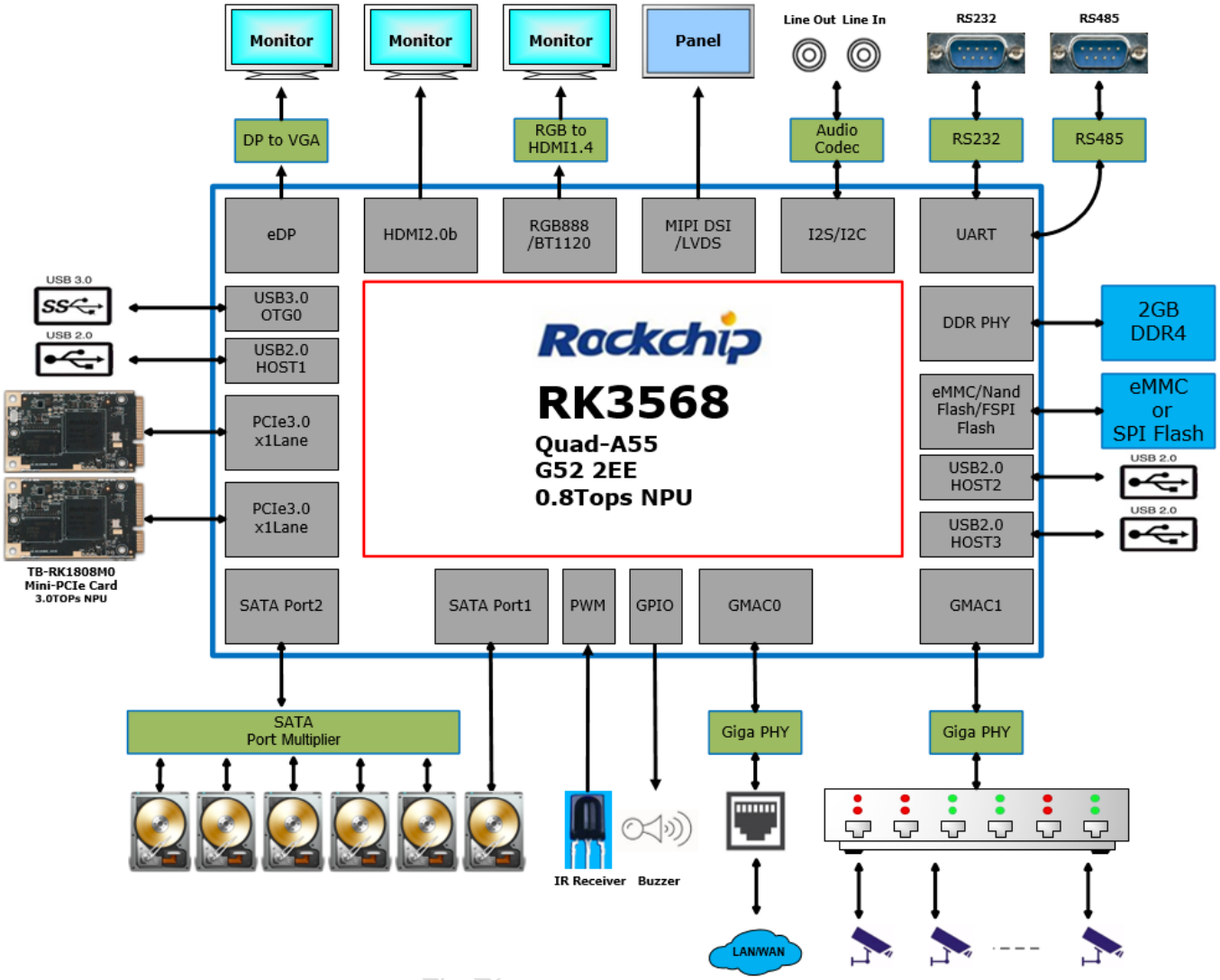


Figure 1-3 RK3568 Smart NVR application block diagram

The figures above are example application block diagrams of RK3568, please refer to the reference design schematic released by RK for more details.

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# 2 Schematic Design Recommendation

## 2.1 Minimum System Design

### 2.1.1 Clock Circuit

- The oscillator circuit inside RK3568 and the external 24MHz crystal form the system clock, as shown in Figure 2-1.
- The 22ohm resistor connected to the XOUT24M network in series must be added to limit current and prevent overdrive.
- The 1M ohm resistor between XOUT24M and XIN24M network cannot be modified at will.

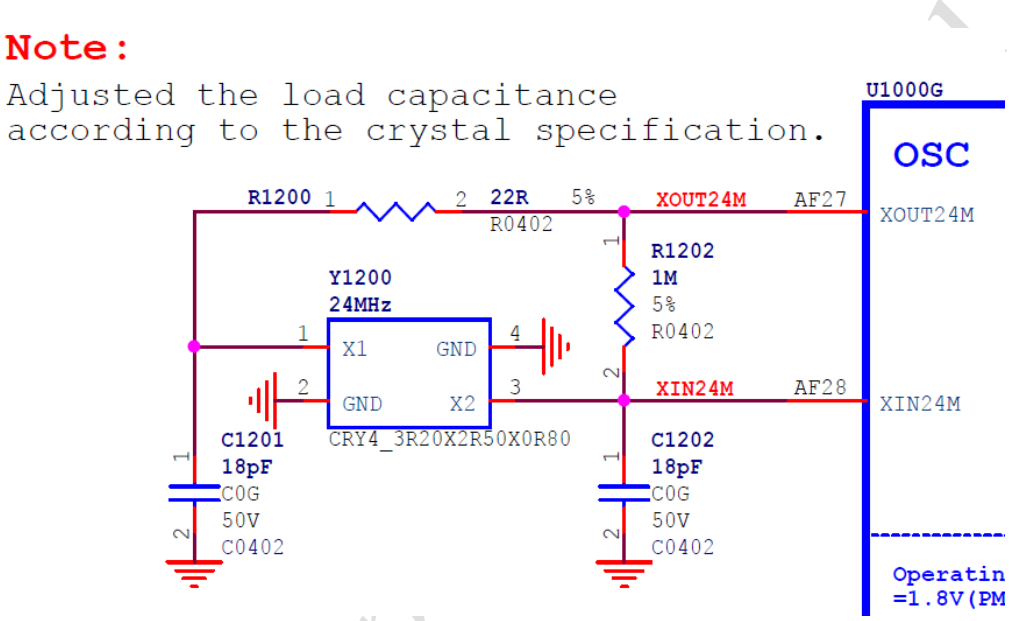


Figure 2-1 RK3568 Crystal circuit and components parameters

**Note**

*The load capacitances of crystal should be selected according to the CL capacitance value of the crystal actually used, and the frequency tolerance at room temperature should be controlled within 20ppm.*

*18pF is the capacitance value of the crystal selected by RK, not a general value, and COG or NPO material are recommended.*

*It is recommended to use 4Pin SMT crystal, with 2 GND pins fully connected with the ground of the PCB to enhance ESD anti-interference ability*

- The system clock can also be directly generated by an external active crystal circuit with a clock amplitude of 1.8V. When working, the clock is input through the XIN24M pin, and the XOUT24M pin can be floated. The clock parameters are shown in the following Table 2-1:

Table 2–1 RK3568 24MHz clock requirements

| Parameters | Spec | | | Description |
|---|---|---|---|---|
| | Min. | Max. | Unit | |
| Frequency | 24.000000 | | MHz | |
| Frequency tolerance | +/-20 | | ppm | |
| Clock amplitude | 1.8 | | V | Peak-to-peak |
| Operating temperature | -20 | 80 | ℃ | |
| ESR | / | 40 | Ohm | |

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- When RK3568 is in standby, you can choose to switch the working clock source to the clock provided by the PMU_PVTM module or an external 32.768KHz clock. Turn off the OSC oscillator circuit to get better standby power consumption. At this time, only the IO interrupt in the PMUIO1 and PMUIO2 power domain are supported to wake up. If the required wake-up source is related to the 24MHz clock, the 24MHz clock cannot be turned off.

- The clock oscillation loop integrated in PVTM (Process-Voltage-Temperature Monitor) module can generate a clock, its frequency is determined by the delay unit of the clock oscillation loop circuit. The generated clock can be used as a clock source for the chip in standby; the external clock 32.768KHz will reach optimal chip standby power consumption when RK3568 chip in sleeps, and the PVTM module can also be turned off at this time.

- The external 32.768KHz clock can be obtained from PMIC or external RTC clock source. The 32.768KHz clock input pin of RK3568 is shown in the figure below:

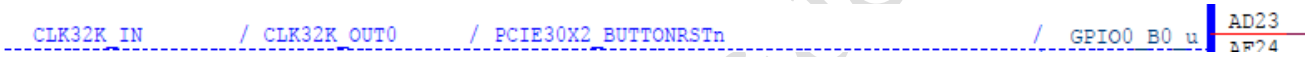


Figure 2-2 RK3568 the 32.768KHz clock input pin in standby

- The external 32.768kHz RTC clock parameters are shown in Table 2-2 below

Table 2–2 RK3568 32.768KHz clock requirements

| Parameters | Spec | | | Description |
|---|---|---|---|---|
| | Min. | Max. | Unit | |
| Frequency | 32.768000 | | kHz | |
| Frequency tolerance | +/-30 | | ppm | |
| Clock amplitude | 0.65*VDD | VDD+0.3V | V | VDD:PMUIO2 voltage |
| Operating temperature | -20 | 80 | ℃ | |
| Duty Ratio | 50 | | % | |

Note

*When using this function, the IOMUX pin must be set to CLK32K_IN function, and the input amplitude must meet the power supply requirements of PMUIO2 Domain.*

- RK3568 can provide working clocks to peripherals:
  - REFCLK_OUT: 24MHz clock output as default, which can be provided to Camera and other devices as working clock
  - CLK32K_OUT0: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock
  - CLK32K_OUT1: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock

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- ETH0_REFCLKO_25M: 25MHz clock output, which can be provided to Ethernet PHY and other devices as working clock
- ETH1_REFCLKO_25M_M0/ETH1_REFCLKO_25M_M1: 25MHz clock output, which can be provided to Ethernet PHY and other devices as working clock
- CIF_CLKOUT: 24MHz clock output by default, other frequency value can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock
- CAM_CLKOUT0: 24MHz clock output by default, other frequency points can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock
- CAM_CLKOUT1: 24MHz clock output by default, other frequency value can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock

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Note

*The IO Domains where the above clocks are located must match the IO level of connected peripherals. If they do not match, a level conversion circuit must be added.*

*Please evaluate whether they can meet the clock requirements of the peripheral device.*

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### 2.1.2 Reset/watchdog/TSADC Circuit

The hardware reset signal of RK3568 is input through Pin AH27 (NPOR_u), which must be controlled externally and is active at low level. In order to ensure the stability and normal operation of the chip, the minimum reset time required is 100 cycles of the 24MHz main clock, that is, at least 4us or more.

Pin AH27 (NPOR_u) has to add a 100nF capacitor to eliminate jitter of the reset signal, enhance anti-interference ability, and prevent abnormal system reset caused by false triggering.

The pull-up power of the RESETn network must be consistent with the IO domain (PMUIO1) where the nPOR pin is located.

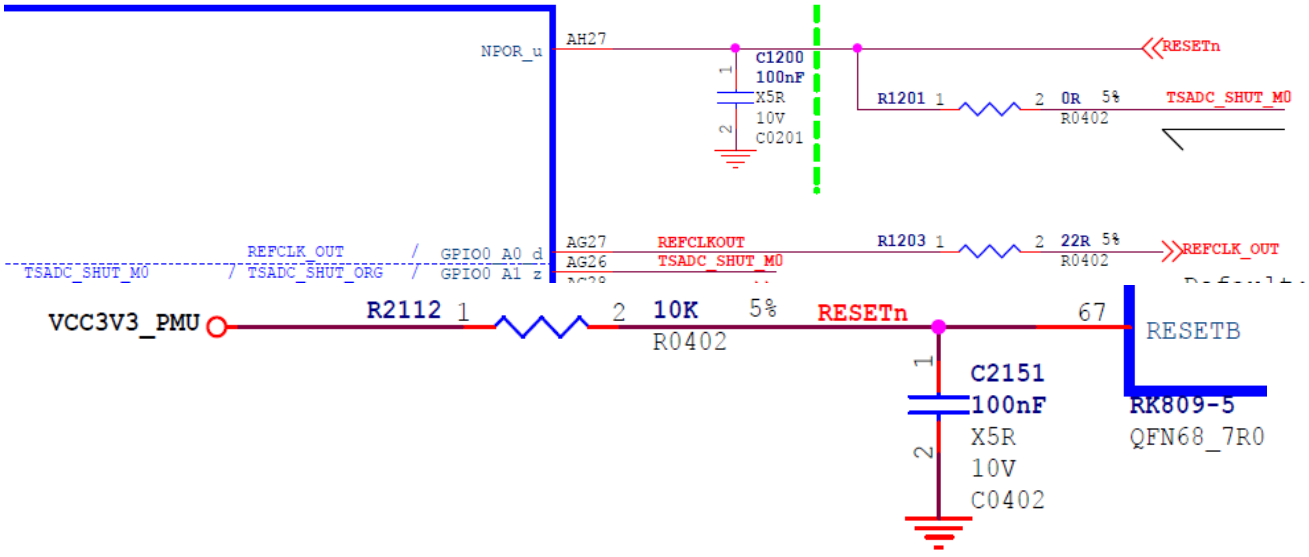


Figure 2-3 RK3568 reset input (RK809-5 solution)

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- When using a discrete power solution, the reset signal circuit diagram is as follows:

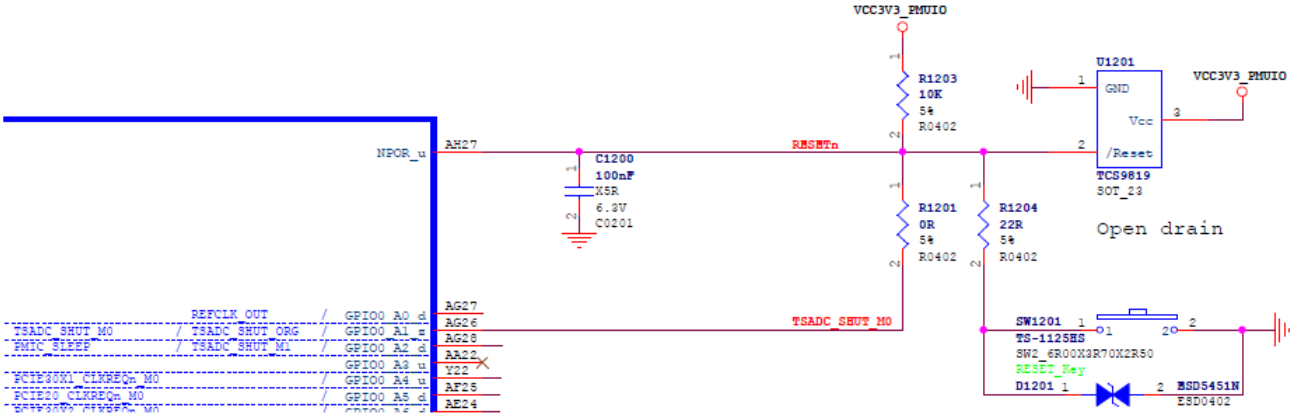


Figure 2-4 RK3568 reset input (discrete power solution)

Note: The reset IC must be with open-drain output, and low level active.

- The RK3568 chip integrates a Watchdog Timer. When a reset signal is generated, a low level will be output through TSADC_SHUT_M0 or TSADC_SHUT_M1 pin, and then resets RK3568 by hardware.
- The RK3568 chip integrates two TSADC (Temperature-Sensor ADC) modules. When the temperature inside the chip exceeds the threshold, the internal TSHUT signal can be passed to the CRU module and reset RK3568 chip, or it can output low level through TSADC_SHUT_M0 or TSADC_SHUT_M1 pin to reset RK3568 by hardware. As shown in the figure above, the TSADC_SHUT_M0 network is connected to the RESETn network.
- RK3568 reset signal path diagram is as follows:

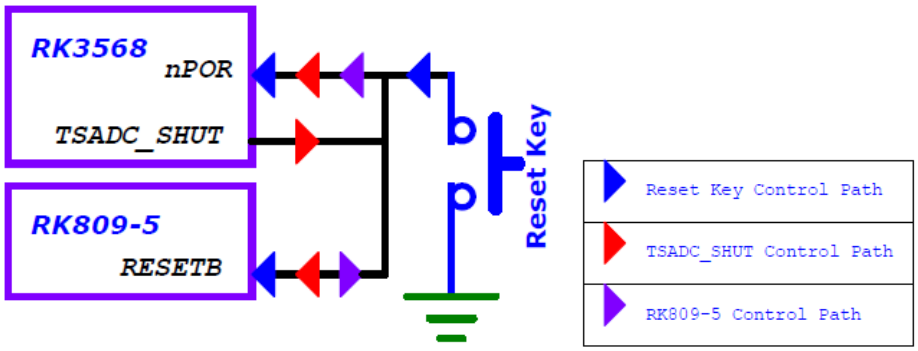


Figure 2-5 RK3568 the path of reset signal

- When the RESETB pin of RK809-5 is powered on for the first time, after all power supplies are powered on, RESETB will change from low level to high level (open drain output) after delaying the set time, to complete the power-on reset process; when RK809-5 is in working or sleep mode, if the RESETB pin is pulled low, RK809-5 will also be restarted. The restart power-on sequence is the same as the first time power-on.

### 2.1.3 PMU Circuit

In order to meet the requirement of low power consumption products, RK3568 has designed a power management unit (PMU) to control and manage the internal power supply of the chip.

This module supports registers inside chip or PMUIO power domain IO control peripheral power circuit,

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realize power on and power off to other functional modules, and also support IO interrupt wake-up, so as to realize the chip's standby and wake-up functions.

### 2.1.4 System Boot Sequence

The RK3568 chip supports multiple booting ways. After chip reset, the boot code integrated inside the chip will automatically boot in the following sequence:

- Serial Nor Flash (FSPI)
- Serial Nand Flash (FSPI)
- Nand Flash
- eMMC
- SDMMC0 Card

If there is no boot code in the above devices, you can download the system code to these devices through the USB3_OTG0_DP/USB3_OTG0_DM signal of the USB3.0 OTG0 interface.

### 2.1.5 System Initialization Configuration Signal

There are two important signals in RK3568 will affect the system boot configuration, which need to be configured and kept stable before power-on. They are:

- FLASH_VOL_SEL pin (Pin AG25): hardware configuration VCCIO2 power domain IO driver voltage
- SDMMC0_DET pin (Pin Y22): determine whether VCCIO3 power domain IO is SDMMC0 or JTAG function

After the system reset, the chip will configure the default power-on function of the corresponding module according to the input level of the two pins

- The IO drive voltage mode of RK3568 VCCIO2 power domain is configured by hardware by default. Because it belongs to FLASH power domain, it's used during system boots. Therefore, when the system is booting, the IO drive voltage mode must be set through the hardware configuration first instead of setting by register operation, as shown below:
  - When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high;
  - When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low;
  - If the IO power supply is changed, the FLASH_VOL_SEL pin must be changed synchronously, they cannot be mismatch, otherwise the function will be abnormal or the chip may even be damaged.

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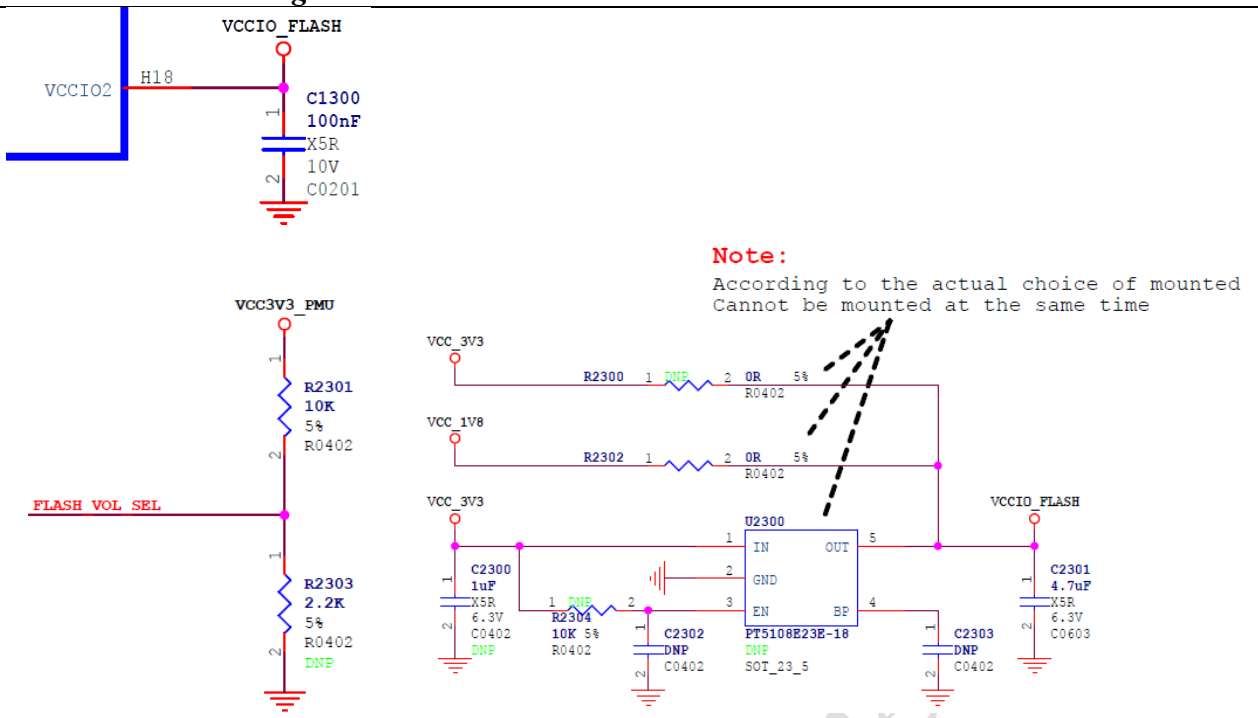


Figure 2-6 RK3568 VCIO2 power supply and FLASH_VOL_SEL

- The ARM JTAG function of RK3568 is reused with the SDMMC0 function, and the IOMUX function is switched through the SDMMC0_DET pin. Therefore, you have to finish configuration operate of this pin before power-on, otherwise the ARM JTAG function has no output that will affect the debugging during booting, no output from SDMMC0 will affect the boot function of SDMMC0.

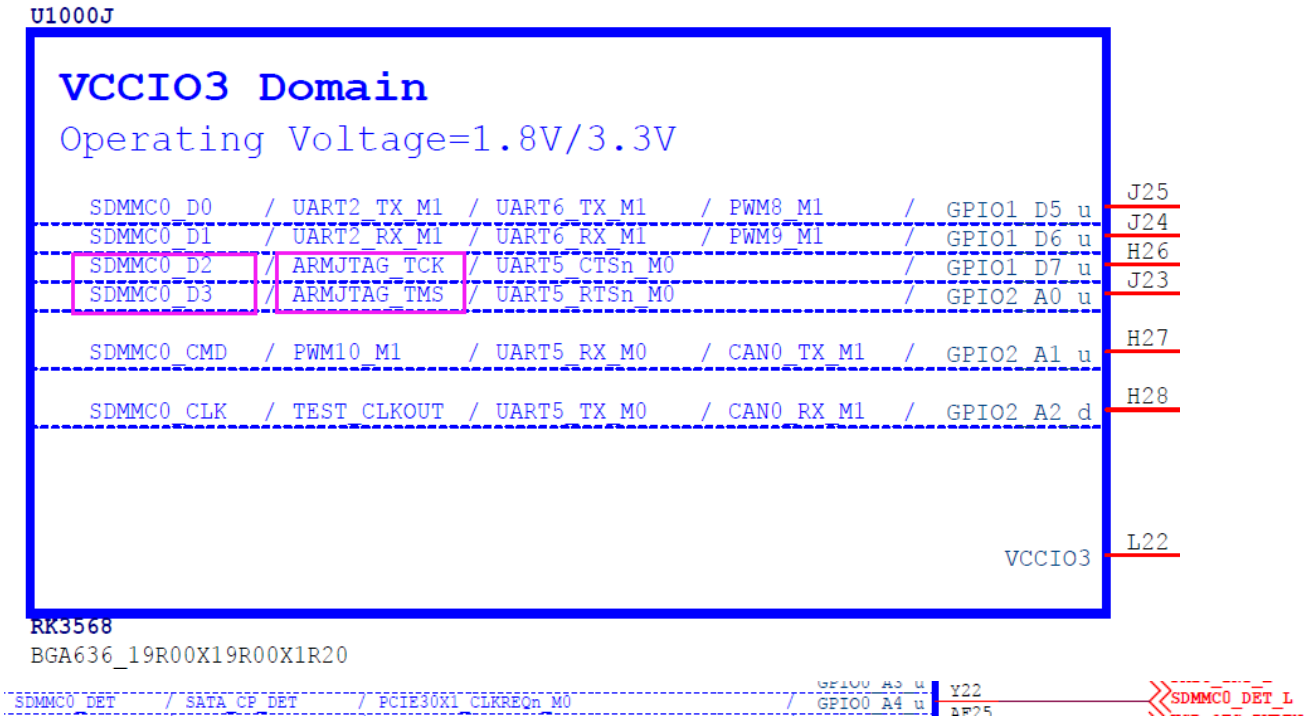


Figure 2-7 RK3568 SDMMC0/ARM JTAG multiplexed pins and SDMMC0 DET pin

If this pin is detected as high level, the corresponding IO will be switched to ARM JTAG function;

When it is detected as low level (If there is no special requirement, most SD card insertion will pull down this

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pin), the corresponding IO is switched to the SDMMC0 function.

After the system is up, it can be switched to register to control IOMUX, then the pin can be released.

In order to query easily, the configuration status and function of the two pins are shown as follows:

Table 2–3 RK3568 System initialization configuration signal description

| Signal name | Internal up and down | Description |
|---|---|---|
| FLASH_VOL_SEL | Pull up | IO drive voltage mode of FLASH VCCIO2 power domain:<br>0: IO level mode is 3.3V;<br>1: IO level mode is 1.8V |
| SDMMC0_DET | Pull up | SDMMC0/ARM JATG pin multiplexing selection control signal:<br>0: Recognized as SD card insertion, SDMMC0/ARM JATG pins are multiplexed as SDMMC0 function;<br>1: Not recognized as SD card insertion, SDMMC0/ARM JATG pins are multiplexed as ARM JTAG function (Default) |

### 2.1.6 JTAG and UART Debug Circuit

The ARM JTAG interface of RK3568 conforms to the IEEE1149.1 standard. The PC can be connected to the DSTREAM emulator through SWD mode (two-wire mode) to debug ARM Core inside the chip.

When connecting to emulator during booting, you need to ensure that the SDMMC0_DET pin is at a high level, otherwise the JTAG debugging mode cannot be entered. The management configuration is described in the previous sections.

After the system is up, it will switch to control IOMUX by register. The ARM JTAG interface introduction is shown in the following Table:

Table 2–4 RK3568 JTAG debug interface signal

| Signal name | Description |
|---|---|
| ARM_JTAG_TCK | Clock input in SWD mode |
| ARM_JTAG_TMS | Data input and output in SWD mode |

The connection way of JTAG and the definition of standard connector pins are shown in the figure below:

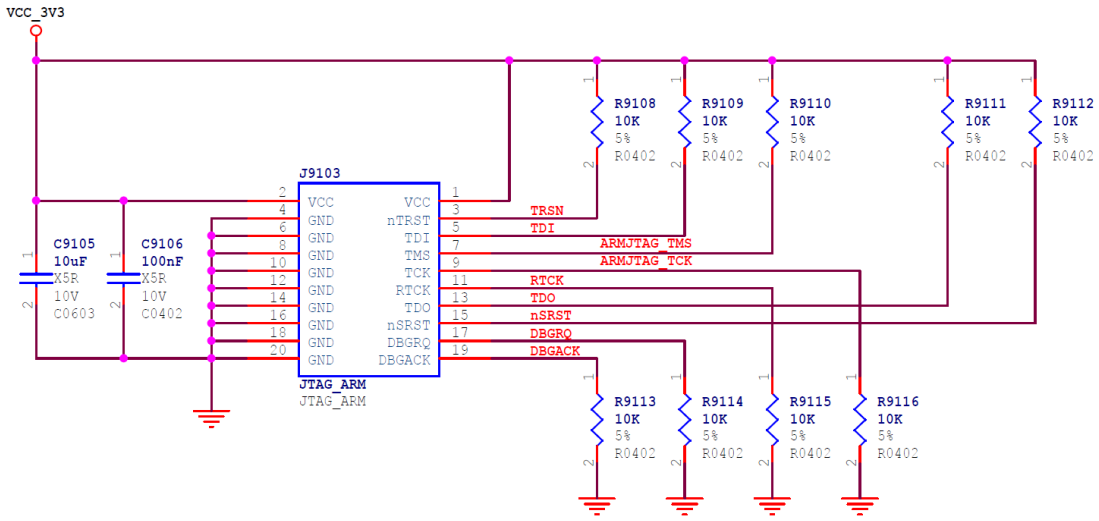


Figure 2-8 RK3568 JTAG connection schematic

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- If there is no SD Card function, it is recommended to reserve the ARM JTAG function to facilitate debug. The reserved circuit is as shown in the figure below:

Note that the VCCIO3 power supply must be powered, and the power supply voltage could be VCCIO_SD or VCC_3V3

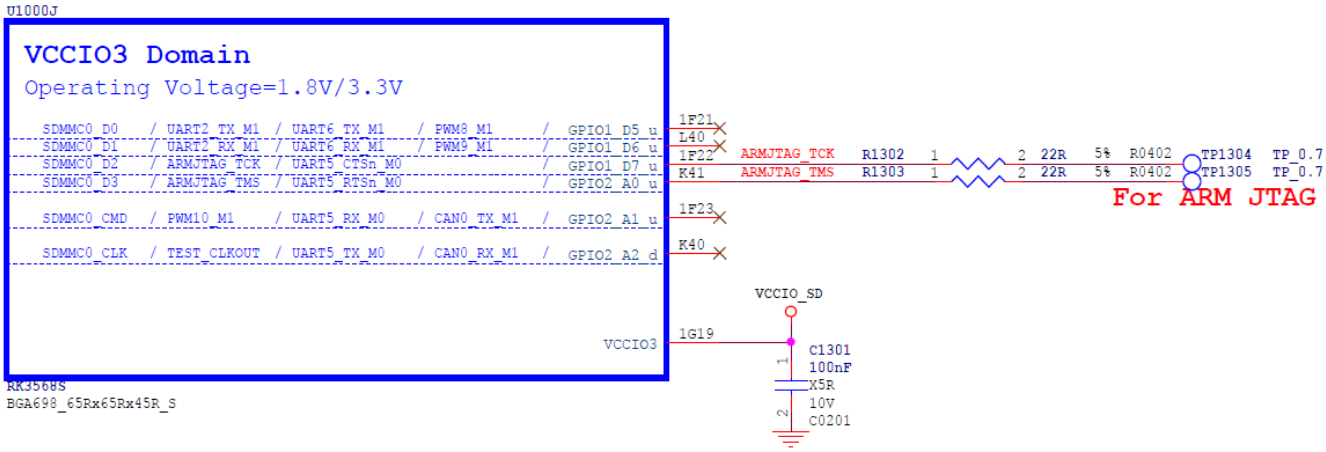


Figure 2-9 RK3568 ARM JTAG pin

- The MCU_JTAG module of RK3568 is temporarily not released, no special processing is required.
- The UART2_RX_M0/UART2_TX_M0 is used for RK3568 UART Debug by default, with default baud rate 1500000M.

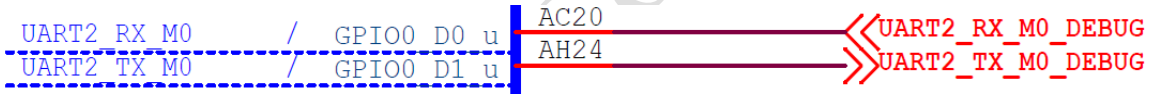


Figure 2-10 RK3568 UART2 M0 pin

The 100ohm resistor connected in series with UART2_RX_M0/UART2_TX_M0 shall not be deleted, and TVS tube shall be added to strengthen the anti-static surge capability and prevent the chip pins from being damaged during the development process. It is recommended to reserve 2.54 pins as much as possible. If conditions are not allowed, it is recommended to use test points above 0.7mm or larger to facilitate soldering.

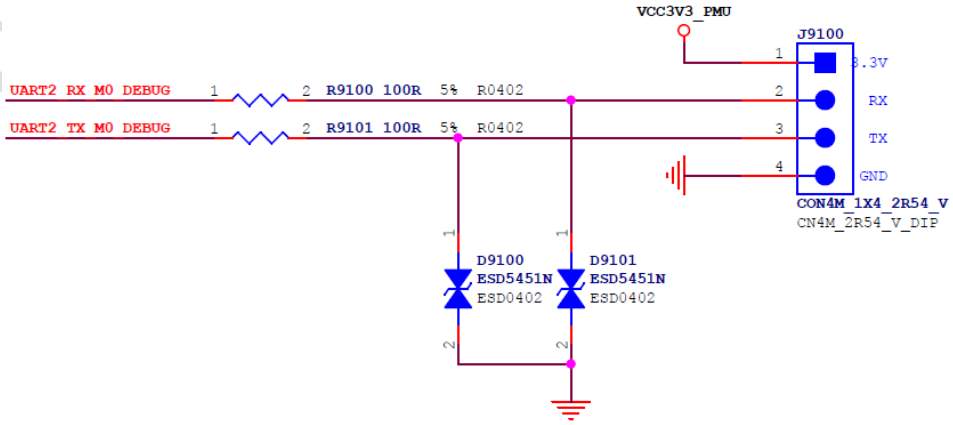


Figure 2-11 RK3568 Debug UART2 Connection diagram

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## 2.1.7 DDR Circuit

### 2.1.7.1 DDR Controller Introduction

The RK3568 DDR controller interface supports JEDEC SDRAM standard interface with following features:

- Support DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X, etc.
- Support 32-bits data bus width, 2 ranks (chip selects), totally 8GB (max) address;
- Support Power Down, Self-Refresh and other modes;
- Compensate the PCB delay through software;
- For DDR3/DDR3L/DDR4, support 8 bits ECC;
- Programmable output and ODT impedance with dynamic PVT compensation.

### 2.1.7.2 Circuit Design Suggestion

The schematic of RK3568 DDR PHY and each DRAM need to be consistent with the reference design diagram, including power supply decoupling capacitors.

RK3568 supports DDR3/DDR3L, LPDDR3, DDR4 or LPDDR4/LPDDR4X. These DRAM have different I/O signals. Choose the signal according to the DRAM type. The RK3568 DDR PHY I/O Map is as follows:

Table 2–5 RK3568 DDR PHY I/O map

| | DDR4 | LPDDR4/LPDDR4x | DDR3 | LPDDR3 |
|---|---|---|---|---|
| DDR_DQ0_A | DDR4_DQL0_A | LPDDR4_DQ0_A | DDR3_DQ0 | LPDDR3_D15 |
| DDR_DQ1_A | DDR4_DQL2_A | LPDDR4_DQ1_A | DDR3_DQ1 | LPDDR3_D14 |
| DDR_DQ2_A | DDR4_DQL4_A | LPDDR4_DQ2_A | DDR3_DQ2 | LPDDR3_D10 |
| DDR_DQ3_A | DDR4_DQL6_A | LPDDR4_DQ3_A | DDR3_DQ3 | LPDDR3_D9 |
| DDR_DQ4_A | DDR4_DQL7_A | LPDDR4_DQ4_A | DDR3_DQ4 | LPDDR3_D13 |
| DDR_DQ5_A | DDR4_DQL5_A | LPDDR4_DQ5_A | DDR3_DQ5 | LPDDR3_D12 |
| DDR_DQ6_A | DDR4_DQL3_A | LPDDR4_DQ6_A | DDR3_DQ6 | LPDDR3_D8 |
| DDR_DQ7_A | DDR4_DQL1_A | LPDDR4_DQ7_A | DDR3_DQ7 | LPDDR3_D11 |
| DDR_DM0_A | DDR4_DML_A | LPDDR4_DM0_A | DDR3_DM0 | LPDDR3_DM1 |
| DDR_DQS0P_A | DDR4_DQSL_P_A | LPDDR4_DQS0P_A | DDR3_DQS0P | LPDDR3_DQS1P |
| DDR_DQS0N_A | DDR4_DQSL_N_A | LPDDR4_DQS0N_A | DDR3_DQS0N | LPDDR3_DQS1N |
| DDR_DQ8_A | DDR4_DQU3_A | LPDDR4_DQ8_A | DDR3_DQ8 | LPDDR3_D25 |
| DDR_DQ9_A | DDR4_DQU1_A | LPDDR4_DQ9_A | DDR3_DQ9 | LPDDR3_D24 |
| DDR_DQ10_A | DDR4_DQU7_A | LPDDR4_DQ10_A | DDR3_DQ10 | LPDDR3_D28 |
| DDR_DQ11_A | DDR4_DQU5_A | LPDDR4_DQ11_A | DDR3_DQ11 | LPDDR3_D29 |
| DDR_DQ12_A | DDR4_DQU2_A | LPDDR4_DQ12_A | DDR3_DQ12 | LPDDR3_D26 |
| DDR_DQ13_A | DDR4_DQU4_A | LPDDR4_DQ13_A | DDR3_DQ13 | LPDDR3_D31 |
| DDR_DQ14_A | DDR4_DQU6_A | LPDDR4_DQ14_A | DDR3_DQ14 | LPDDR3_D30 |
| DDR_DQ15_A | DDR4_DQU0_A | LPDDR4_DQ15_A | DDR3_DQ15 | LPDDR3_D27 |
| DDR_DM1_A | DDR4_DMU_A | LPDDR4_DM1_A | DDR3_DM1 | LPDDR3_DM3 |
| DDR_DQS1P_A | DDR4_DQSU_P_A | LPDDR4_DQS1P_A | DDR3_DQS1P | LPDDR3_DQS3P |
| DDR_DQS1N_A | DDR4_DQSU_N_A | LPDDR4_DQS1N_A | DDR3_DQS1N | LPDDR3_DQS3N |
| DDR_DQ0_B | DDR4_DQU7_B | LPDDR4_DQ0_B | DDR3_DQ16 | LPDDR3_D1 |
| DDR_DQ1_B | DDR4_DQU5_B | LPDDR4_DQ1_B | DDR3_DQ17 | LPDDR3_D5 |
| DDR_DQ2_B | DDR4_DQU3_B | LPDDR4_DQ2_B | DDR3_DQ18 | LPDDR3_D6 |
| DDR_DQ3_B | DDR4_DQU1_B | LPDDR4_DQ3_B | DDR3_DQ19 | LPDDR3_D4 |
| DDR_DQ4_B | DDR4_DQU0_B | LPDDR4_DQ4_B | DDR3_DQ20 | LPDDR3_D2 |

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| | DDR4 | LPDDR4/LPDDR4x | DDR3 | LPDDR3 |
|---|---|---|---|---|
| DDR_DQ5_B | DDR4_DQU6_B | LPDDR4_DQ5_B | DDR3_DQ21 | LPDDR3_D3 |
| DDR_DQ6_B | DDR4_DQU4_B | LPDDR4_DQ6_B | DDR3_DQ22 | LPDDR3_D7 |
| DDR_DQ7_B | DDR4_DQU2_B | LPDDR4_DQ7_B | DDR3_DQ23 | LPDDR3_D0 |
| DDR_DM0_B | DDR4_DMU_B | LPDDR4_DM0_B | DDR3_DM2 | LPDDR3_DM0 |
| DDR_DQS0P_B | DDR4_DQSU_P_B | LPDDR4_DQS0P_B | DDR3_DQS2P | LPDDR3_DQS0P |
| DDR_DQS0N_B | DDR4_DQSU_N_B | LPDDR4_DQS0N_B | DDR3_DQS2N | LPDDR3_DQS0N |
| DDR_DQ8_B | DDR4_DQL0_B | LPDDR4_DQ8_B | DDR3_DQ24 | LPDDR3_D18 |
| DDR_DQ9_B | DDR4_DQL2_B | LPDDR4_DQ9_B | DDR3_DQ25 | LPDDR3_D19 |
| DDR_DQ10_B | DDR4_DQL4_B | LPDDR4_DQ10_B | DDR3_DQ26 | LPDDR3_D22 |
| DDR_DQ11_B | DDR4_DQL6_B | LPDDR4_DQ11_B | DDR3_DQ27 | LPDDR3_D23 |
| DDR_DQ12_B | DDR4_DQL7_B | LPDDR4_DQ12_B | DDR3_DQ28 | LPDDR3_D16 |
| DDR_DQ13_B | DDR4_DQL5_B | LPDDR4_DQ13_B | DDR3_DQ29 | LPDDR3_D17 |
| DDR_DQ14_B | DDR4_DQL1_B | LPDDR4_DQ14_B | DDR3_DQ30 | LPDDR3_D20 |
| DDR_DQ15_B | DDR4_DQL3_B | LPDDR4_DQ15_B | DDR3_DQ31 | LPDDR3_D21 |
| DDR_DM1_B | DDR4_DML_B | LPDDR4_DM1_B | DDR3_DM3 | LPDDR3_DM2 |
| DDR_DQS1P_B | DDR4_DQSL_P_B | LPDDR4_DQS1P_B | DDR3_DQS3P | LPDDR3_DQS2P |
| DDR_DQS1N_B | DDR4_DQSL_N_B | LPDDR4_DQS1N_B | DDR3_DQS3N | LPDDR3_DQS2N |
| DDR_ECC_DQ0 | DDR4_ECC_DQ7 | - | DDR3_ECC_DQ0 | - |
| DDR_ECC_DQ1 | DDR4_ECC_DQ0 | - | DDR3_ECC_DQ1 | - |
| DDR_ECC_DQ2 | DDR4_ECC_DQ2 | - | DDR3_ECC_DQ2 | - |
| DDR_ECC_DQ3 | DDR4_ECC_DQ1 | - | DDR3_ECC_DQ3 | - |
| DDR_ECC_DQ4 | DDR4_ECC_DQ6 | - | DDR3_ECC_DQ4 | - |
| DDR_ECC_DQ5 | DDR4_ECC_DQ4 | - | DDR3_ECC_DQ5 | - |
| DDR_ECC_DQ6 | DDR4_ECC_DQ3 | - | DDR3_ECC_DQ6 | - |
| DDR_ECC_DQ7 | DDR4_ECC_DQ5 | - | DDR3_ECC_DQ7 | - |
| DDR_ECC_DM | DDR4_ECC_DM | - | DDR3_ECC_DM | - |
| DDR_ECC_DQSP | DDR4_ECC_DQSP | - | DDR3_ECC_DQSP | - |
| DDR_ECC_DQSN | DDR4_ECC_DQSN | - | DDR3_ECC_DQSN | - |
| AC0 | DDR4_A0 | LPDDR4_CLKP_B | DDR3_A9 | - |
| AC1 | DDR4_A1 | - | DDR3_A2 | - |
| AC2 | DDR4_A2 | LPDDR4_A1_A | DDR3_A4 | LPDDR3_A6 |
| AC3 | DDR4_A3 | LPDDR4_CKE1_A | DDR3_A3 | - |
| AC4 | DDR4_A4 | LPDDR4_A3_B | DDR3_BA1 | LPDDR3_A3 |
| AC5 | DDR4_A5 | LPDDR4_A5_B | DDR3_A11 | LPDDR3_A2 |
| AC6 | DDR4_A6 | LPDDR4_A1_B | DDR3_A13 | LPDDR3_A1 |
| AC7 | DDR4_A7 | LPDDR4_ODT0_CA_B | DDR3_A8 | - |
| AC8 | DDR4_A8 | LPDDR4_ODT0_CA_A | DDR3_A6 | LPDDR3_A9 |
| AC9 | DDR4_A9 | LPDDR4_CLKN_B | DDR3_A5 | - |
| AC10 | DDR4_A10 | LPDDR4_CKE0_B | DDR3_A10 | - |
| AC11 | DDR4_A11 | LPDDR4_A0_A | DDR3_A7 | LPDDR3_A8 |
| AC12 | DDR4_A12 | LPDDR4_A3_A | DDR3_BA2 | - |
| AC13 | DDR4_A13 | LPDDR4_A0_B | DDR3_A14 | LPDDR3_A0 |
| AC14 | DDR4_A14_WEN | LPDDR4_A4_A | DDR3_A15 | LPDDR3_A5 |
| AC15 | DDR4_A15_CASN | LPDDR4_A2_A | DDR3_A0 | - |
| AC16 | DDR4_A16_RASN | LPDDR4_A5_A | DDR3_RASN | LPDDR3_A7 |
| AC17 | DDR4_ACTN | LPDDR4_CKE1_B | DDR3_CASN | - |
| AC18 | DDR4_BA0 | LPDDR4_A2_B | DDR3_A1 | - |
| AC19 | DDR4_BA1 | LPDDR4_A4_B | DDR3_A12 | LPDDR3_A4 |

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| | DDR4 | LPDDR4/LPDDR4x | DDR3 | LPDDR3 |
|---|---|---|---|---|
| AC20 | DDR4_BG0 | LPDDR4_ODT1_CA_B | DDR3_WEN | - |
| AC21 | DDR4_BG1 | LPDDR4_ODT1_CA_A | DDR3_BA0 | - |
| AC22 | DDR4_CKE | LPDDR4_CKE0_A | DDR3_CKE | LPDDR3_CKE |
| AC23 | DDR4_CLKP | LPDDR4_CLKP_A | DDR3_CLKP | LPDDR3_CLKP |
| AC24 | DDR4_CLKN | LPDDR4_CLKN_A | DDR3_CLKN | LPDDR3_CLKN |
| AC25 | DDR4_CS0N | LPDDR4_CS0N_A | DDR3_ODT1 | LPDDR3_ODT0 |
| AC26 | DDR4_CS1N | LPDDR4_CS1N_A | DDR3_CS1N | LPDDR3_ODT1 |
| AC27 | DDR4_ODT0 | LPDDR4_CS1N_B | DDR3_ODT0 | LPDDR3_CS1N |
| AC28 | DDR4_ODT1 | LPDDR4_CS0N_B | DDR3_CS0N | LPDDR3_CS0N |
| AC29 | DDR4_RESETN | LPDDR4_RESETN | DDR3_RESETN | - |

- For DDR3/DDR3L:

  Support the entire group swap between Byte; support DQ swap within Byte;

  The CA sequence cannot be swapped and must be allocated according to the schematic design ;

  If need to support the template with a total bit width of 16bit and a template with a total bit width compatible of 16bit/32bit, it's must use the template provided by RK, and no difference is allowed.

- For DDR3/DDR3L and ECC:

  ECC Byte is fixed, cannot swap with other Bytes; Support the entire group swap among other bytes; Support DQ swap within Byte;

  The CA sequence cannot be swapped and must be allocated according to the schematic design .

- For LPDDR3:

  It is necessary to maintain the one-to-one connection between LPDDR3 D0-D7 and LPDDR3_D0-D7 of controller, as well as the corresponding relationship between the associated DQS and DM, does not support adjustment. Other Bytes support the entire group swap;

  Support DQ swap within other Bytes;

  The CA sequence cannot be swapped and must be allocated according to the schematic design .

- For DDR4:

  Support the entire group swap between Byte; support DQ swap within Byte;

  The CA sequence cannot be swapped and must be allocated according to the schematic design ;

  If need to support the template with a total bit width of 16bit and a template with a total bit width compatible of 16bit/32bit, it's must use the template provided by RK, and no difference is allowed.

- For DDR4 and ECC:

  ECC Byte is fixed, cannot swap with other Bytes;

  The DQ sequence in the ECC Byte does not support swapping, and the DQ in other Bytes does not support swapping also, and must be allocated according to the reference diagram;

  The CA sequence cannot be swapped, must be allocated according to the schematic design .

- For LPDDR4/LPDDR4X:

  All DQ and CA sequences cannot be swapped, must be allocated according to the schematic design .

  8bits ECC function is supported in DDR3/DDR3L/DDR4 mode, requirements for the DDR with ECC function:

  Select the same model of 8bit or 16bit DDR, the row/bank/col must be the same as the main DDRs(the

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two DDRs you have already selected), and the rate must be greater than or equal to the main DDRs, it is recommended to use the same model as the main DDRs.

When using 16bit ECC DDR, since RK3568 only supports 8bits ECC, one of the Bytes of the 16bit ECC needs to be processed as shown below:

- DDR3/DDR3L 16bit ECC processing method: as shown below, DMU pin is connected to power, DQSU pin is connected to power, $\overline{\text{DQSU}}$ pin is grounded.

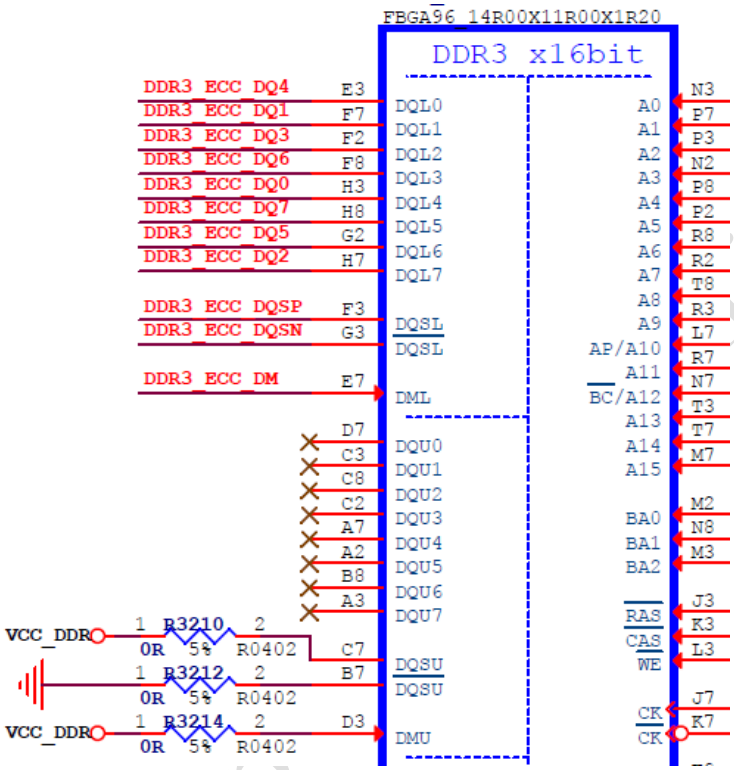


Figure 2-12 RK3568 16bit ECC DDR3/DDR3L processing method

- DDR4 16bit ECC process method: as shown below, DMU_n/DBIU_n pin is connected to power, DQSU_P pin is connected to power, DQSU_N pin is grounded.

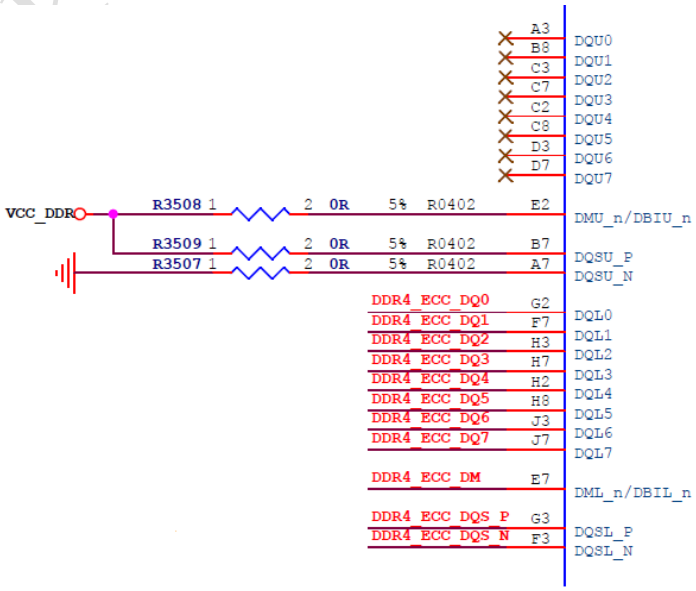


Figure 2-13 RK3568 16bit ECC DDR4 processing method

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RK3568 DDR PHY's DDR_RZQ (Pin H7) pin connection method:

- For DDR3/DDR3L/DDR4/LPDDR3, DDR_RZQ pin must be grounded with a 120ohm 1% resistor.
- For LPDDR4/LPDDR4X, a 120ohm 1% resistor is connected to DDRPHY_VDDQ power (VCC_DDR).

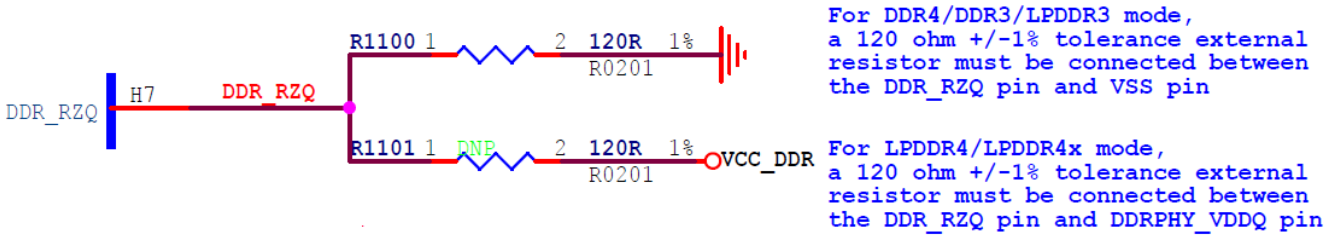


Figure 2-14 RK3568 DDR_RZQ pin

RK3568 DDR PHY can provide voltage to VREFDQ or VREFCA of DRAM, that is, DDR_VREFOUT pin (Pin P8) can output a voltage to DRAM as VREF voltage.

- For DDR3/DDR3L: the default voltage of VREFDQ (VREF_DDR_DQ network) provided for DDR3/DDR3L is 0.75V/0.675V, and the voltage can be adjusted through registers according to the actual needs. The VREFCA of DDR3/DDR3L still uses two 1Kohm 1% resistor for voltage-dividing.

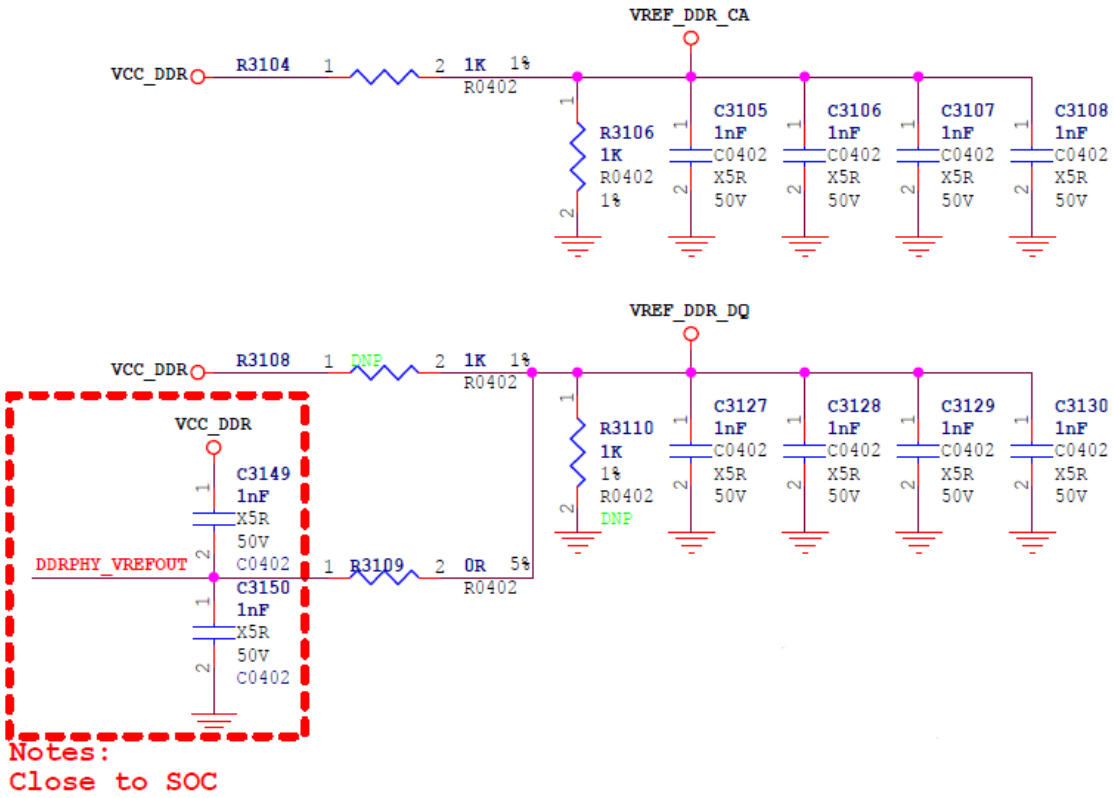


Figure 2-15 DDR3/DDR3L VREF circuit

- For LPDDR3: the voltage of VREFDQ provided for LPDDR3 is related to the configuration of ODT, and the voltage can be adjusted through registers according to the actual needs. The VREFCA of LPDDR3 still uses two 1Kohm 1% resistor for voltage-dividing.

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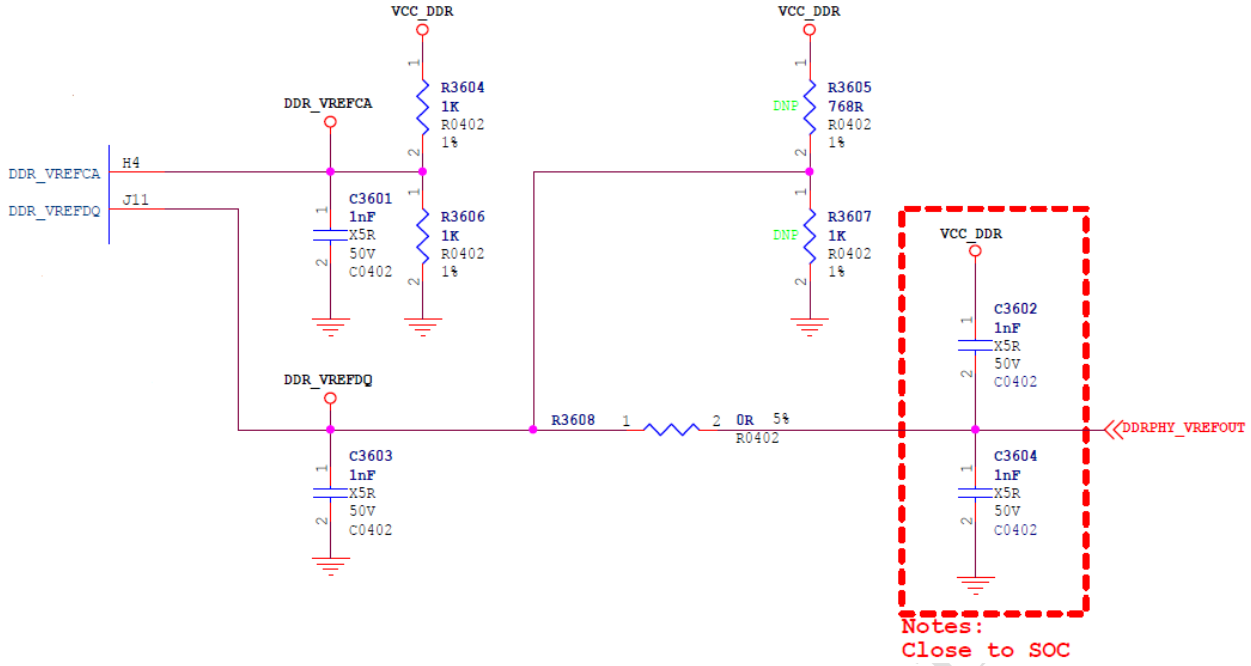


Figure 2-16 LPDDR3 VREF circuit

- For DDR4: the default voltage of VREFCA (VREF_DDR4_CA network) provided for DDR4 is 0.6V, and the voltage can be adjusted through registers according to the actual needs.

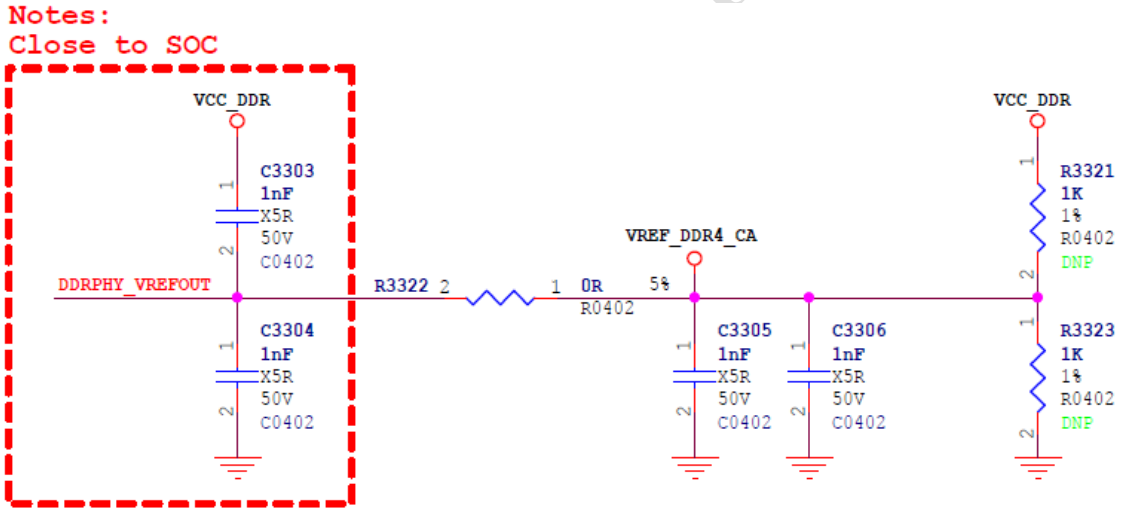


Figure 2-17 DDR4 VREF circuit

- For LPDDR4/LPDDR4X: when it is not used, leave floating.

Note: the 1nF capacitors connected to the ground and power of DDRPHY_VREFOUT network cannot be deleted or modified randomly; the VREF pins of DDR must be with a 1nF decoupling capacitor, and the capacity cannot be modified randomly.

### 2.1.7.3 DDR Peripheral Circuit Design

- The ZQ of DDR3/DDR3L/DDR4/LPDDR3 must connect a 240 ohm 1% resistor to ground;
- The ZQ of LPDDR4 must connect a 240 ohm 1% resistor to the VCC_DDR power;
- The ZQ of LPDDR4x must connect a 240 ohm 1% resistor to the VCC0V6_DDR power;
- It is recommended to reserve a 1nF capacitor for the DDR RESET pin to improve the anti-ESD interference capability

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- For 16bit DDR4 template, reserved to support DDP (Dual-Die Package), the default configuration parameter is SDP (Single-Die Package). When DDP is needed, the following parameters should be updated synchronously:
  1) DDR4 M9 pin connect to DDR_BG1 net of SOC
  2) DDR4 T7 pin connect to GND
  3) DDR4 E9 pin connect to GND by 240ohm 1% resistor

#### 2.1.7.4 DDR Topology and Matching Design

- For DDR3/DDR3L 4 16bit 2CS, DQ uses T topology (one drive two), CA uses double T topology (one drive four).

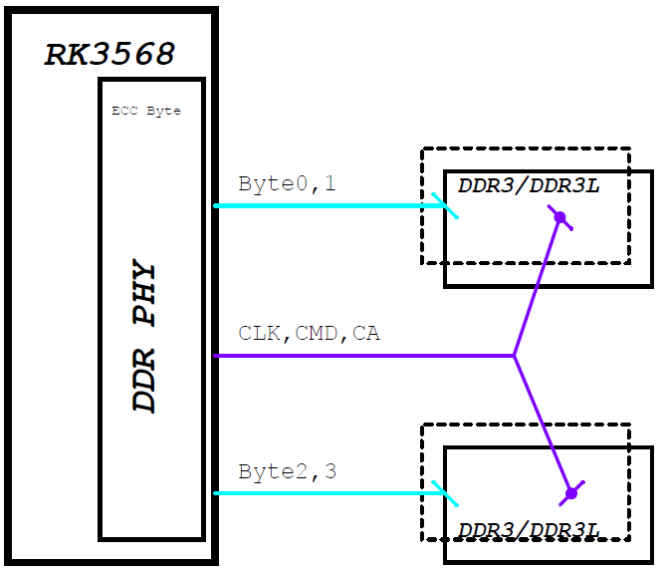


Figure 2-18 DDR3/DDR3L T topology

Clock matching mode: Place the RC circuit at the branch point as shown in the figure below, which can improve signal quality and reduce EMI.

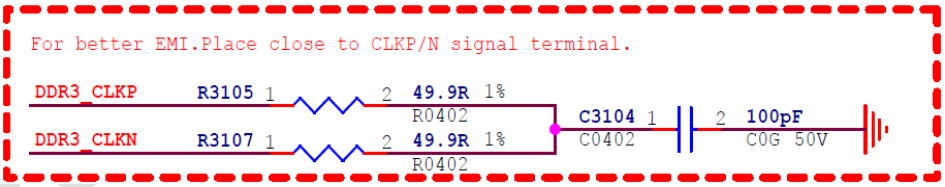


Figure 2-19 The CLKP/CLKN termination of DDR3/DDR3L T topology

- For DDR3/DDR3L+ ECC six 16bit 2CS, DQ uses T topology (one drive two), CA uses Fly-by topology (one drive six).

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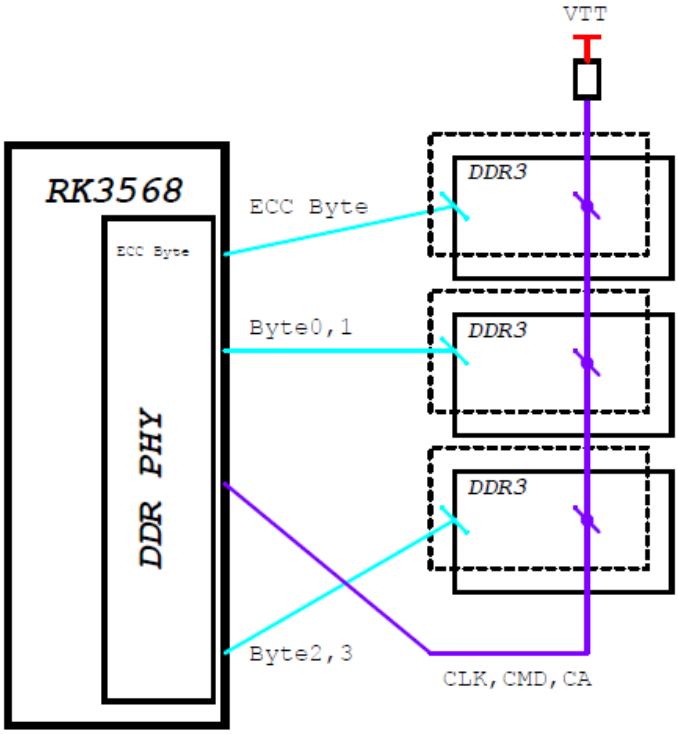


Figure 2-20 DDR3/DDR3L Fly-by topology

Clock, control, address line signal matching mode: add 39ohm resistor to the VTT power at the end, please refer circuit shown in the schematic design.

In addition, a 2pF capacitor is reserved for connecting between the clock P and the clock N near RK3568, whether to add the capacitor according to the actual debugging, and the signal quality can be improved.

- For DDR4 two 16bit 1CS, DQ uses point-to-point connection (one drive one), CA uses T topology (one drive two).

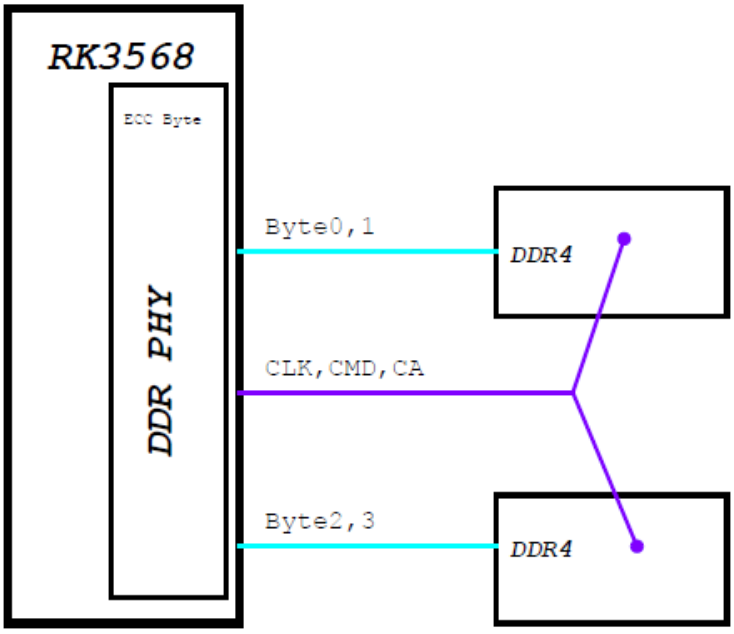


Figure 2-21 DDR4 T topology

Clock signal matching method: Place the RC circuit at the branch point, it is also necessary to connect resistors in series to DDR4 on the branch line, and the series resistor must be placed at the branch point to

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improve the quality of the clock signal.


Figure 2-22 The CLKP/CLKN termination of DDR4 T topology

- For DDR4 and ECC 3 16bit 1CS, DQ uses point-to-point connection (one drive one), CA uses Fly-by topology (one drive three).

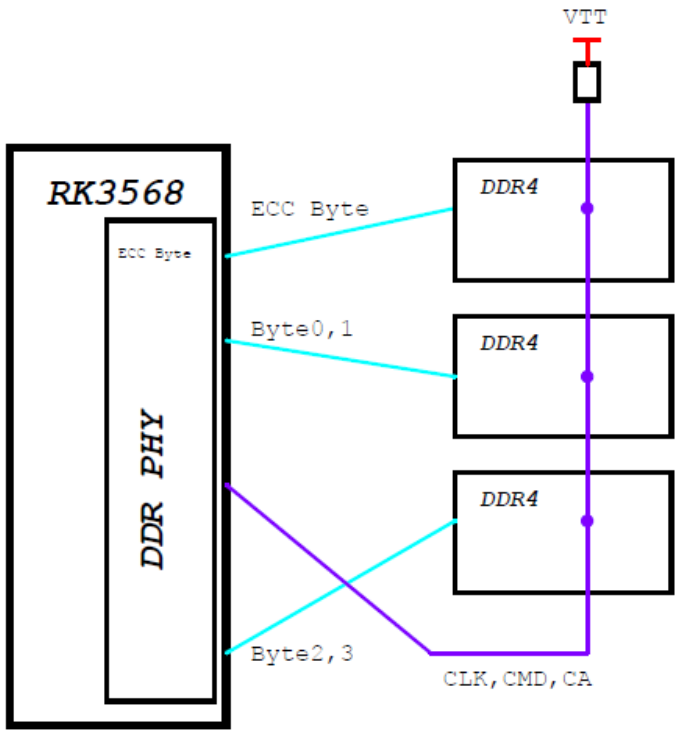


Figure 2-23 DDR4 Fly-by topology

Clock, control, address line signal matching mode: Add 39ohm resistor to the VTT power at the end, refer to the circuit shown in the reference diagram/ schematic design.

In addition, a 2pF capacitor is reserved for connecting between the clock P and the clock N near RK3568, and the signal quality can be improved.

Note: When chooses a VTT power chip, it needs to support DDR4.

- For LPDDR3 1 32bit, DQ and CA use point-to-point topology.

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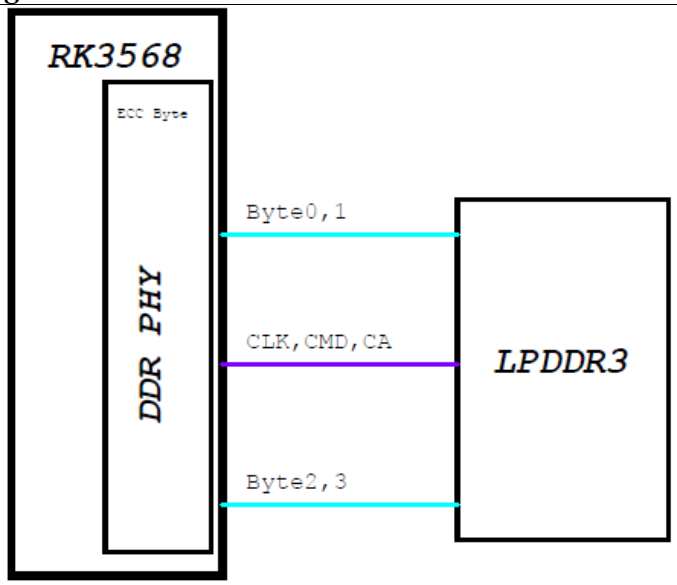


Figure 2-24 LPDDR3 point-to-point topology

Clock matching method: the RC circuit is placed at the end of the line, as shown in the figure below, which can improve signal quality and reduce EMI.

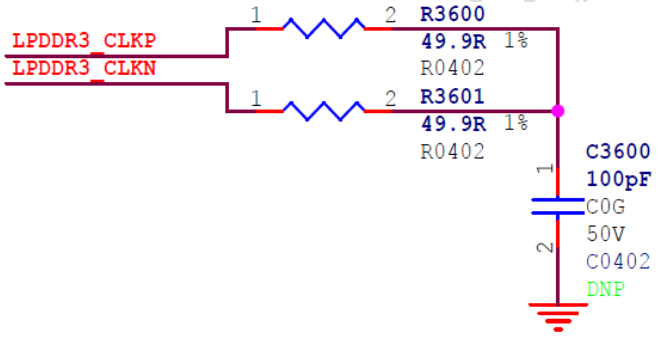


Figure 2-25 LPDDR3 CLKP/CLKN termination

- For one 32bit LPDDR4, DQ and CA use point-to-point topology.

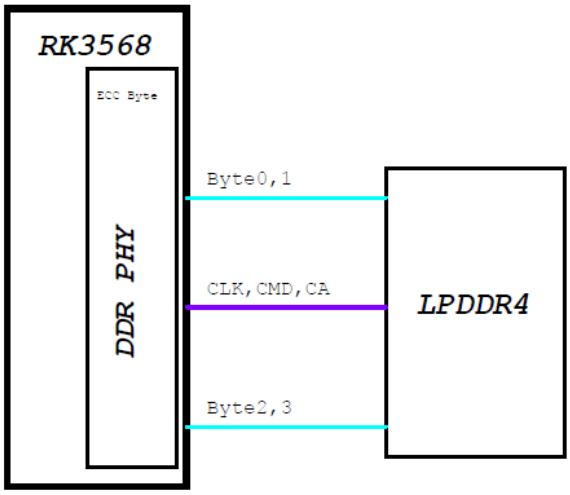


Figure 2-26 LPDDR4 point-to-point topology

Matching method: The DQ, CLK, CMD and CA of LPDDR4 all support ODT, all use point-to-point connection.

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- For one 32bit LPDDR4X, DQ and CA use point-to-point topology.

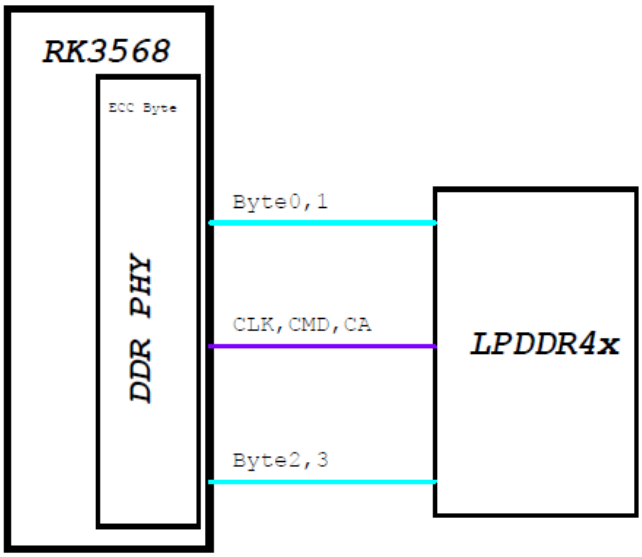


Figure 2-27 LPDDR4X point-to-point topology

Matching method: The DQ, CLK, CMD and CA of LPDDR4X all support ODT, all use point-to-point connection.

#### 2.1.7.5 DDR Power Design and Power up Sequence Requirement

RK3568 DDR PHY have two groups of power supplies, DDRPHY_VDDQ和DDRPHY_VDDQL.

- For DDR3: DDRPHY_VDDQ for 1.5V, DDRPHY_VDDQL for 1.5V
- For DDR3L: DDRPHY_VDDQ for 1.35V, DDRPHY_VDDQL for 1.35V
- For LPDDR3: DDRPHY_VDDQ for 1.2V, DDRPHY_VDDQL for 1.2V (Actually supply 1.25V for improved compatibility）
- For DDR4: DDRPHY_VDDQ for 1.2V, DDRPHY_VDDQL for 1.2V
- For LPDDR4: DDRPHY_VDDQ for 1.1V, DDRPHY_VDDQL for 1.1V
- For LPDDR4X: DDRPHY_VDDQ for 1.1V, DDRPHY_VDDQL for 0.6V

Notes of power supply circuit:

- When using the RK809-5 power solution, it is important to note that according to the actual use of DRAM particles, the voltage divider resistance value of RK809-5 FB3 (pin27) should be modified synchronously to make the VCC_DDR output voltage match the particle.

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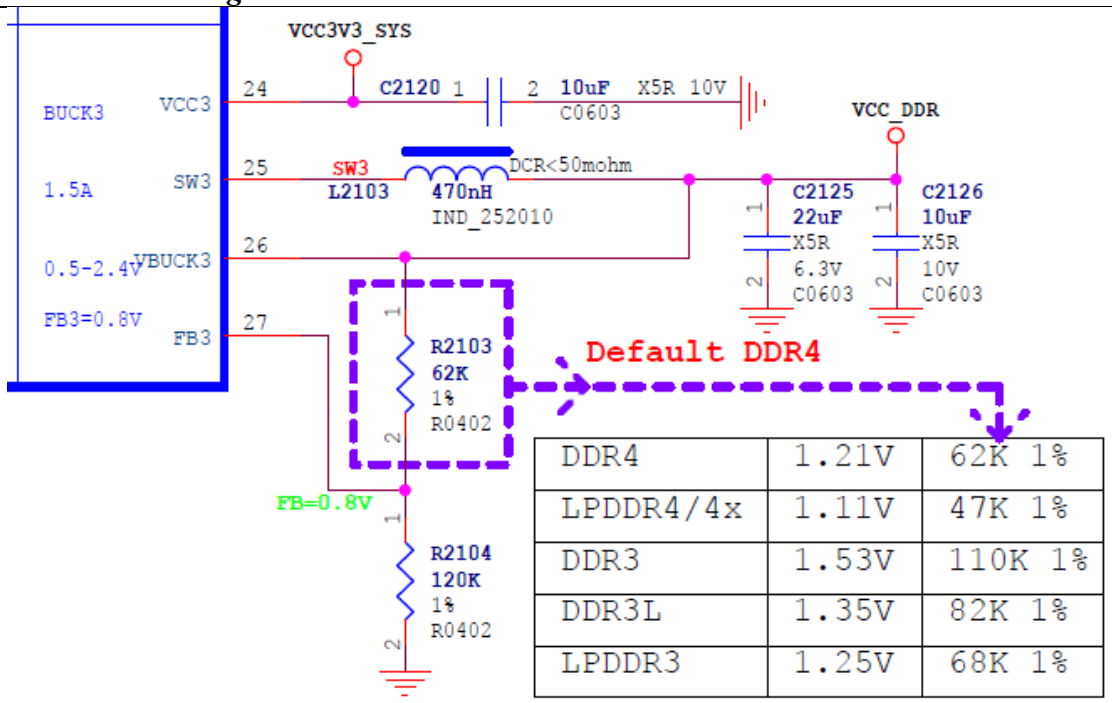


| | | |
|---|---|---|
| DDR4 | 1.21V | 62K 1% |
| LPDDR4/4x | 1.11V | 47K 1% |
| DDR3 | 1.53V | 110K 1% |
| DDR3L | 1.35V | 82K 1% |
| LPDDR3 | 1.25V | 68K 1% |

Figure 2-28 RK809-5 BUCK3 parameters regulation

- When using discrete power supply solution, the voltage-dividing resistance value of power supply BUCK should be modified synchronously to make the VCC_DDR output voltage match with the DRAM.
- RK3568 reference template provides LPDDR4 and LPDDR4X compatible design "RK3568_Template_LP4XD200P132SD6_43x28_1600MHz", it should be noted that the circuit must be selected according to the actual materials. When using LPDDR4, only need to connect the R3804 resistor as shown below, all component s in the green box below are not needed; when using LPDDR4X, R3804 is not connected, all components in the green box below are needed.

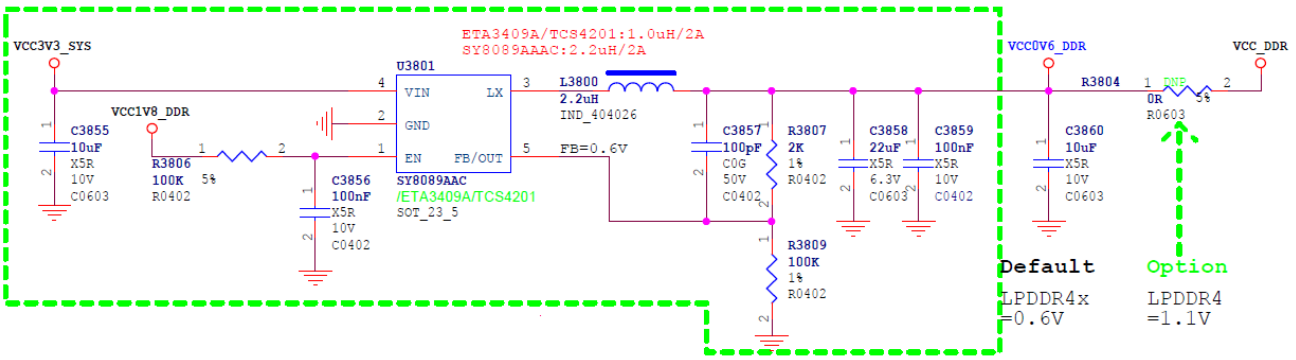


Figure 2-29 Power selection of LPDDR4/LPDDR4x compatible design

For all types of DRAM power-up sequence, please refer to JEDEC standards:

- The power-up sequence of DDR3/DDR3L SDRAM is shown in the figure below:

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1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2-30 DDR3 SDRAM power up sequence

■ The power-up sequence of LPDDR3 SDRAM is shown in the figure below:

| After... | Applicable Conditions |
|---|---|
| Ta is reached | $V_{DD1}$ must be greater than $V_{DD2}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$—200mV |
| | $V_{Ref}$ must always be less than all other supply voltages |

Figure 2-31 LPDDR3 SDRAM power up sequence

■ The power-up sequence of DDR4 SDRAM is shown in the figure below:

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to $V_{DD}$ min must be no greater than 200ms; and during the ramp, $V_{DD}$ ≥ $V_{DDQ}$ and ($V_{DD}$-$V_{DDQ}$) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
   - $V_{DD}$ and $V_{DDQ}$ are driven from a single power converter output, AND
   - The voltage levels on all pins other than $V_{DD}$,$V_{DDQ}$,$V_{SS}$,$V_{SSQ}$ must be less than or equal to $V_{DDQ}$ and $V_{DD}$ on one side and must be larger than or equal to $V_{SSQ}$ and $V_{SS}$ on the other side. In addition, $V_{TT}$ is limited to TBDV max once power ramp is finished, AND
   - VrefCA tracks TBD.

   or
   - Apply $V_{DD}$ without any slope reversal before or at the same time as $V_{DDQ}$
   - Apply $V_{DDQ}$ without any slope reversal before or at the same time as $V_{TT}$ & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than $V_{DD}$,$V_{DDQ}$,$V_{SS}$,$V_{SSQ}$ must be less than or equal to $V_{DDQ}$ and $V_{DD}$ on one side and must be larger than or equal to $V_{SSQ}$ and $V_{SS}$ on the other side.

Figure 2-32 DDR4 SDRAM power up sequence

■ The power-up sequence of LPDDR4/4x SDRAM is shown in the figure below:

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1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x $V_{DD2}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. $V_{DD1}$ must ramp at the same time or earlier than $V_{DD2}$. $V_{DD2}$ must ramp at the same time or earlier than $V_{DDQ}$.

**Table 5 — Voltage Ramp Conditions**

| After | Applicable Conditions |
|---|---|
| Ta is reached | $V_{DD1}$ must be greater than $V_{DD2}$ |
| | $V_{DD2}$ must be greater than $V_{DDQ}$ - 200 mV |

NOTE 1 Ta is the point when any power supply first reaches 300 mV.
NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.
NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
NOTE 5 The voltage difference between any of $V_{SS}$ and $V_{SSQ}$ pins must not excess 100 mV.

Figure 2-33 LPDDR4/4x SDRAM power up sequence

#### 2.1.7.6 DDR Support List

For the DDR support list, please refer to the document "Rockchip_Support_List_DDR", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 2.1.8 eMMC Circuit

#### 2.1.8.1 eMMC Controller Introduction

The features of RK3568 eMMC controller are as follows:

- Compatible with standard iNAND interface;
- Compatible with the 4.41,4.51,5.0, and 5.1 specifications;
- Support three data bus widths of 1-bit, 4-bit and 8-bit;
- Support HS200 mode;
- Support CMD Queue;

#### 2.1.8.2 eMMC Circuit Design Suggestion

RK3568 eMMC interface is multiplexed with Nand Flash and FSPI Flash interface, in the design of eMMC interface, please refer to the schematic for the eMMC signal connection method, including the decoupling capacitors of each power supply.

The boot code is placed in eMMC, when using eMMC, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the EMMC_D0 or EMMC_CLK network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the EMMC_D0 or EMMC_CLK short to ground, and power on, RK3568 will enter into the Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of EMMC_D0 or EMMC_CLK, otherwise the flashing will fail).

Normally, it is not recommended to update the firmware in this way, because improper operation may cause

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IO damage.

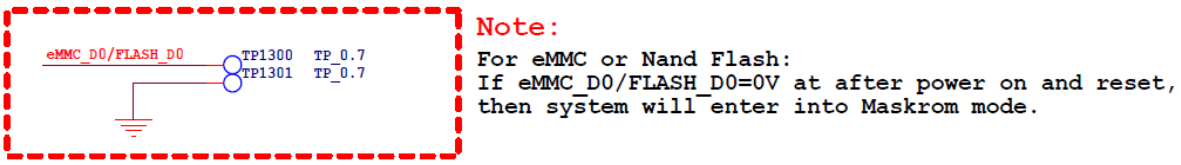


Figure 2-34 eMMC_D0 test point

### 2.1.8.3 eMMC Topology and Matching Method Design

- eMMC connection diagram:

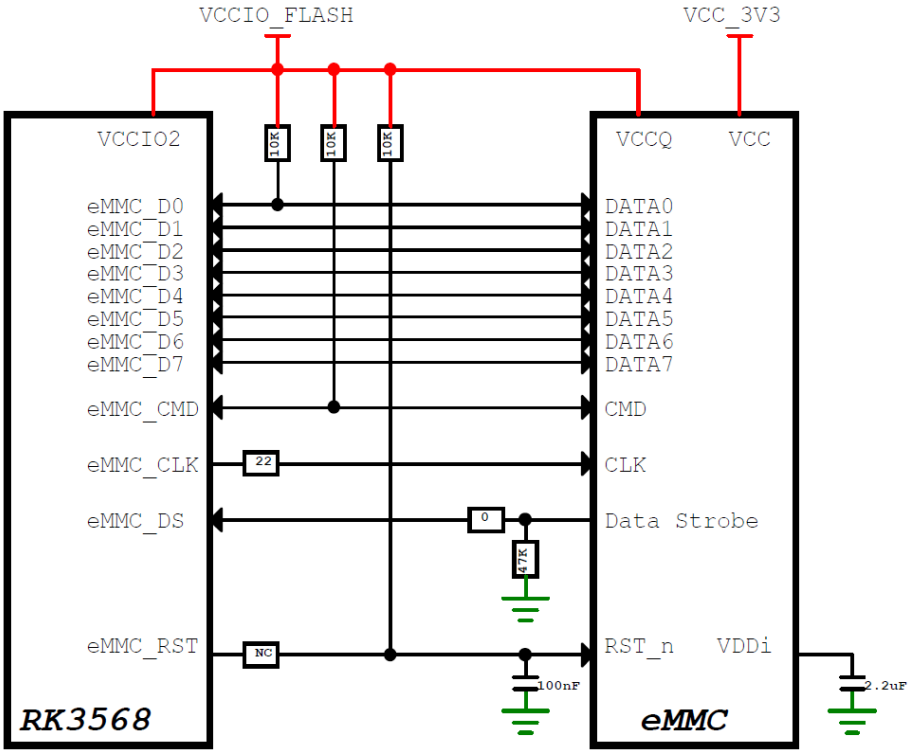


Figure 2-35 eMMC connection diagram

- eMMC interface pull up and down and matching design suggestions as shown in Table 2-6:

Table 2–6 RK3568 eMMC interface design

| Signal | Internal pull up/down | Connection mode | Description(chipset)） |
|---|---|---|---|
| eMMC_D[7:0] | pull up | direct connection, D0 external pull-up with a 10K ohm resistor, other data use the pull-up resistor inside the RK3568 chip | eMMC data send/receive |
| eMMC_CLK | pull down | connect 22ohm resistor in series with RK3568 | eMMC clock send |
| eMMC_CMD | pull up | direct connection, D0 external pull-up with a 10K ohm resistor | eMMC command send/receive |
| eMMC_DATA_ Strobe | pull down | connect a 0ohm resistor in series with the eMMC, and reserve a 47K ohm pull-down resistor | eMMC data and command receive refer to Strobe |

- Connection diagram of eMMC and Nand Flash in compatible design:

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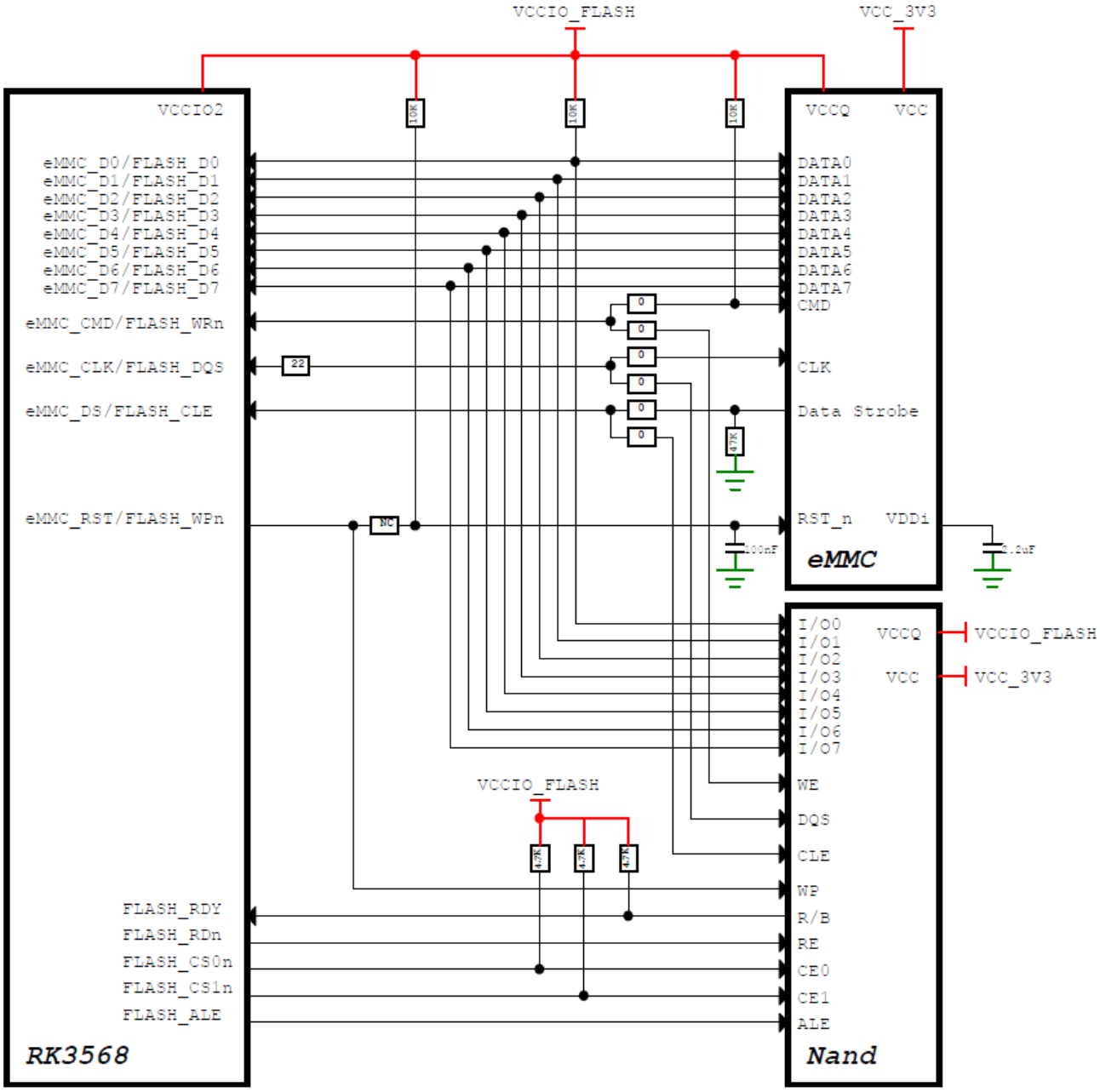


Figure 2-36 Connection diagram of eMMC and Nand Flash in compatible design

In compatible design, there will be branches in the multiplexed signal routing. To ensure that the impact of eMMC signal quality is minimized, the three signals eMMC_CMD/FLASH_WRn, eMMC_CLK/FLASH_DQS, eMMC_DS/FLASH_CLE should reserve series resistors at the branch points. For example: when using eMMC, the 0ohm resistors that branch to the eMMC are needed, and the 0ohm resistors that branch to the Nand Flash are not needed, which will minimize the branching impact in routing. D0-D7 can minimize the branching impact through PCB Layout (For Nand, the D0 pull-up resistor cannot be connected, please refer to the PCB Layout design below.

#### 2.1.8.4 eMMC Power up Sequence Requirement

The eMMC interface of RK3568 belongs to VCCIO2 power domain, only one power supply, so there is no sequence requirements.

The eMMC have two sets of power supplies, refer to JEDEC standard for power-on sequence:

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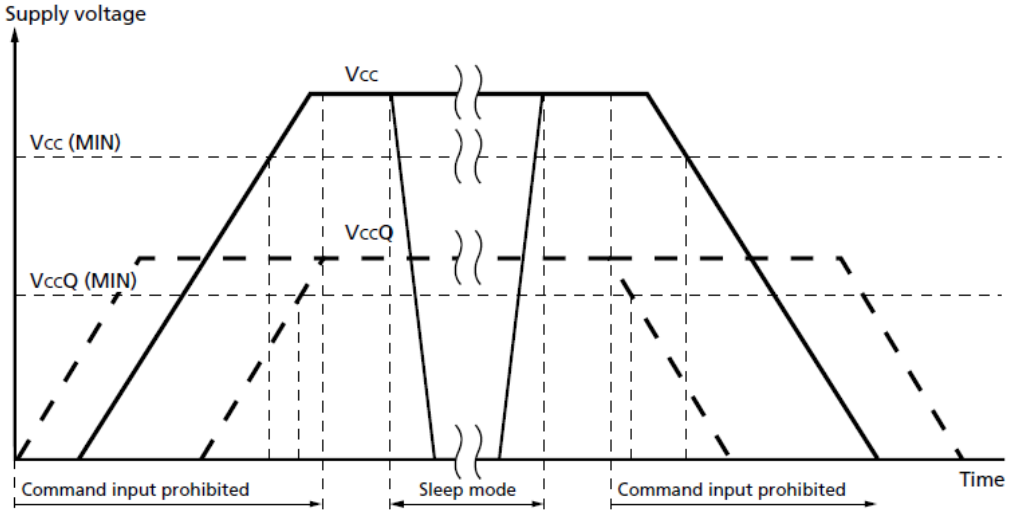


Figure 2-37 eMMC power up and power down sequence

#### 2.1.8.5 eMMC Support List

For RK3568 eMMC support list, please refer to the document "RKeMMCSupportList", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 2.1.9 FSPI Flash Circuit

#### 2.1.9.1 FSPI Flash（Boot is supported）Interface Introduction

FSPI is a flexible serial interface controller. There is a FSPI controller in RK3568 chip, which can be used to connect FSPI devices.

The features of RK3568 FSPI controller are as follows:

- Support serial NOR and NAND FLASH;
- Support SDR mode;
- Support single/dual/four-line mode;

#### 2.1.9.2 FSPI Flash Circuit Design Suggestion

FSPI Flash interface of RK3568 is multiplexed with Nand Flash and eMMC interface. In FSPI Flash interface design, please refer to the schematic for the FSPI Flash signal connection mode, including the decoupling capacitors for each power supply.

The boot code is placed in FSPI Flash, when using the FSPI Flash, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the FSPI_CLK network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the FSPI_CLK short to ground, and then power on, RK3568 will enter Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of FSPI_CLKK, and otherwise the flashing will fail).

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Normally, it is not recommended to update the firmware in this way, because improper operation may cause IO damage.

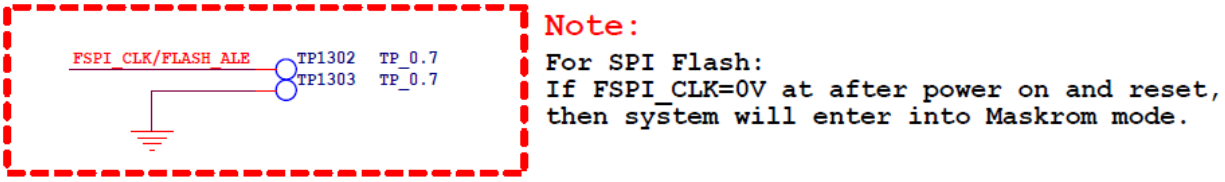


Figure 2-38 FSPI_CLK test point

### 2.1.9.3 FSPI Flash Topology and Matching Design

- FSPI Flash connection diagram:

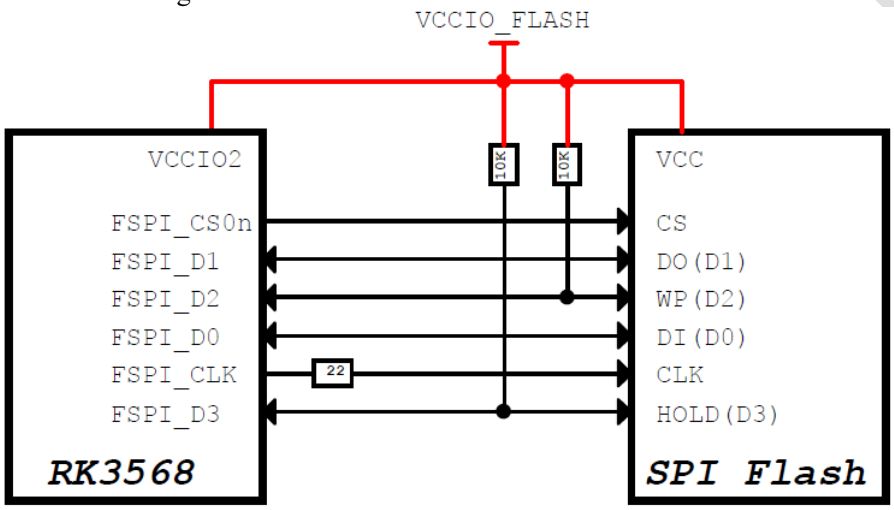


Figure 2-39 FSPI Flash connection diagram

- FSPI interface pull up and down and matching design suggestions as shown in Table 2-7:

Table 2–7 RK3568 FSPI interface design

| Signal | Internal pull up/down | Connection mode | Description(chipset) |
|---|---|---|---|
| FSPI_D[3:0] | D2 pull down<br>D0/D1/D3 pull up | direct connection, D2, D3 external pull-up with a 10K ohm resistor, | FSPI data send/receive |
| FSPI0_CLK | pull down | connect 22ohm resistor in series with RK3568 | FSPI clock send |
| FSPI0_CS0n | pull up | direct connection | FSPI chip select signal |

### 2.1.9.4 FSPI Power up Sequence Requirement

The FSPI Flash interface of RK3568 chip belongs to the VCCIO2 power domain, only one power supply, so there is no sequence requirements.

The SPI Flash have only one power supply, the power supply must be the same as the VCCIO2 power domain power supply.

### 2.1.9.5 SPI Flash Support List

For RK3568 SPI Flash support list, please refer to the document "RK SpiNor and SLC Nand SupportLis", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

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## 2.1.10 Nand Flash Circuit

### 2.1.10.1 Nand Flash Controller Introduction

RK3568 Nand Flash controller supports the following features:

- Support asynchronous Nand Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support ONFI synchronous Nand Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support Toggle Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support SLC, MLC, TLC Flash;
- Support ECC and so on;

### 2.1.10.2 Nand Flash Circuit Design Suggestion

The Nand Flash interface of RK3568 is multiplexed with FSPI Flash and eMMC interface. In Nand Flash interface design, please refer to the schematic for the Nand Flash signal connection mode, including the decoupling capacitors for each power supply.

The reference schematic is compatible with different types of Nand Flash. Please select the peripherals according to the model actually used. When using Nand Flash in DDR mode, Pin28 and 45 of Nand Flash should be connected to the VCCIO_FLASH power; and Pin38 of some SLC is for protection. If such Flash are used, Pin38 leave floating

The boot code is placed in Nand Flash, when using the Nand Flash, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the Flash_D0 network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the Flash_D0 short to the ground, and power on, RK3568 will enter the Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of Flash_D0, otherwise the flashing will fail)..

Normally, it is not recommended to update the firmware in this way, because improper operation may cause IO damage.

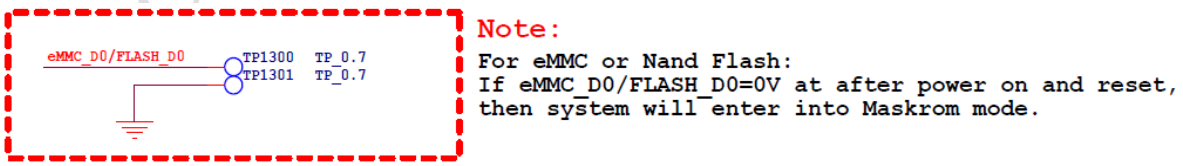


Figure 2-40 Flash_D0 test point

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### 2.1.10.3 Nand Flash Topology and Matching Design

- Nand Flash connection diagram:

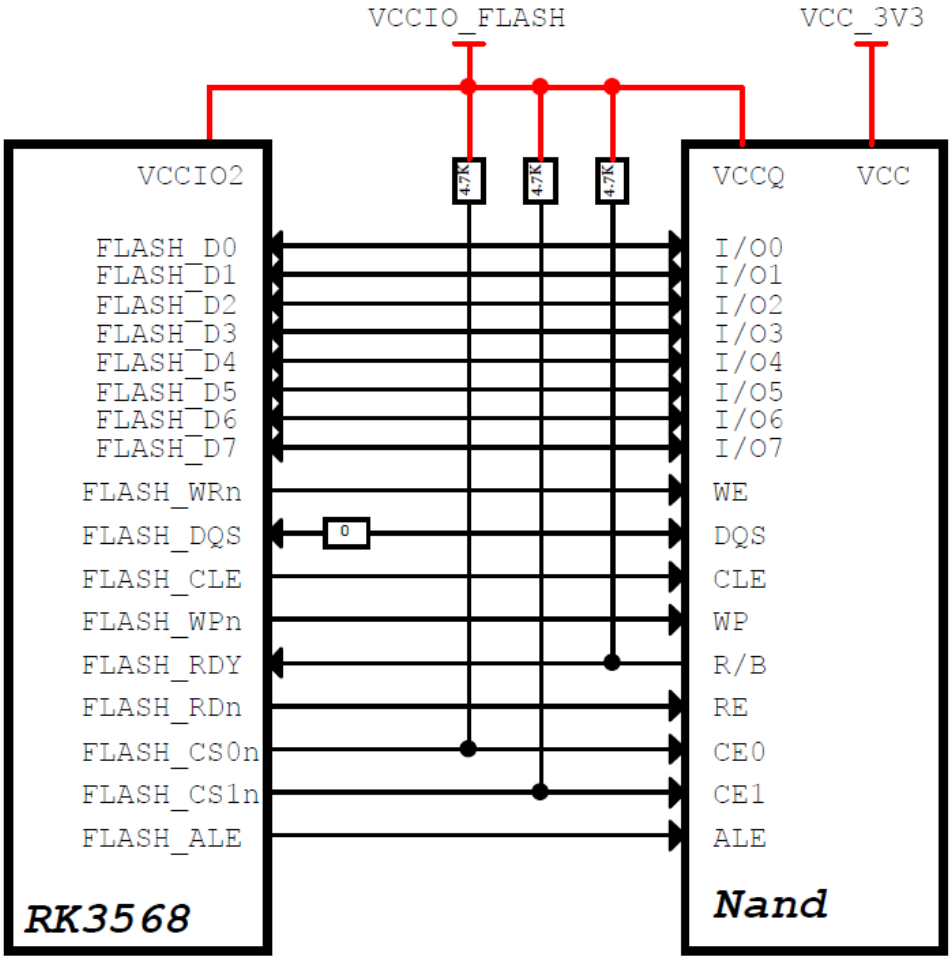


Figure 2-41 Nand Flash connection diagram

- Nand Flash interface pull up and down and matching design suggestions as shown in Table 2-8:

Table 2–8 RK3568 Nand Flash interface design

| Signal | Internal pull up/down | Connection mode | Description(chipset) |
|---|---|---|---|
| Flash_D[7:0] | pull up | direct connection | Nand Flash data send and receive |
| Flash_WRn | pull up | direct connection | Nand Flash write enable |
| Flash_DQS | pull down | connect 22ohm resistor in series with RK3568 | Nand Flash data strobe |
| Flash_CLE | pull down | direct connection | Nand Flash command latch enable |
| Flash_WPn | pull down | direct connection | Nand Flash write protected |
| Flash_RDY | pull up | direct connection, external pull-up with a 4.7K ohm resistor | Nand Flash ready/busy |
| Flash_RDn | pull up | direct connection | Nand Flash read enable |
| Flash_CS0n | pull up | direct connection, external pull-up with a 4.7K ohm resistor | Nand Flash chip select 0 |
| Flash_CS1n | pull up | direct connection, external pull-up with a 4.7K ohm resistor | Nand Flash chip select 1 |
| Flash_ALE | pull down | direct connection | Nand Flash address latch enable |

- When using eMMC and Nand Flash compatible design, please see eMMC circuit description.

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#### 2.1.10.4 Nand Flash Power up Sequence Requirement

The Nand Flash interface of RK3568 chip belongs to the VCCIO2 power domain, only one power supply, so there are no sequence requirements.

- The Nand Flash have only one power supply, the power supply must be the same as the VCCIO2 power domain power supply.
- The Nand Flash have two sets of power supplies, refer to JEDEC standard for power-on sequence:

*Some NAND Flash devices do not support $V_{CCQ}$. For these devices all references to $V_{CCQ}$ are replaced with $V_{CC}$.*

SpecTek NAND Flash devices are designed to prevent data corruption during power transitions. $V_{CC}$ is internally monitored. (The WP# signal supports additional hardware protection during power transitions. When ramping $V_{CC}$ and $V_{CCQ}$, use the following procedure to initialize the device:

1. Ramp $V_{CC}$.
2. Ramp $V_{CCQ}$ and $V_{CCQ}$ must not exceed $V_{CC}$.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 29). The R/B# signal becomes valid when 50µs has elapsed since the beginning the VCC ramp, and 10µs has elapsed since $V_{CCQ}$ reaches $V_{CCQ}$ (MIN) and $V_{CC}$ reaches $V_{CC}$ (MIN).
4. If not monitoring R/B#, the host must wait at least 100µs after $V_{CCQ}$ reaches $V_{CCQ}$ (MIN) and $V_{CC}$ reaches $V_{CC}$ (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
5. If $V_{CCQ}$ is in the 1.8V operational range, then the asynchronous interface is active by default for each target. Each LUN draws less than an average of $I_{ST}$ measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for $^{t}$POR after a RESET command is issued. LUN0 of each target is selected by default after power-on. The RESET busy time can be monitored by polling R/B# or by using the READ STATUS (70h) command. For multi-LUN configurations the READ STATUS ENHANCED (78h) command should be used to check initialization status of each LUN on the target. The host must not issue an additional RESET (FFh) command during $^{t}$POR.
7. The device is now initialized and ready for normal operation.

At power-down, $V_{CCQ}$ must go LOW, either before, or simultaneously with, $V_{CC}$ going LOW.

When $V_{CCQ}$ = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with $V_{CCQ}$ during power up but not exceed $V_{CCQ}$. When $V_{CCQ}$ = 0V, the host must keep DQ[7:0] signals LOW or they can be left High-Z. DQ[7:0] signals may be ramped with $V_{CCQ}$ during power up but not exceed $V_{CCQ}$.

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND $V_{CCQ}$ voltage is below $V_{CCQ,min}$. R/B# signals maybe ramped with $V_{CCQ}$ during power up but not exceed $V_{CCQ}$.

Figure 2-42 Nand Flash power up and down sequence

#### 2.1.10.5 Nand Flash Support List

For RK3568 Nand Flash support list, please refer to the document "RK Nand Flash SupportList", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 2.1.11 GPIO Circuit

In RK3568, there are three types of GPIO: only support 1.8V, only support 3.3V, and support configurable 1.8V/3.3V two voltages.

#### 2.1.11.1 GPIO Pins Description

For example, the function SDMMC1_D0, GMAC0_RXD2 and UART6_RX_M0 in the figure below are multiplexed on GPIO2_A3, and only one of the functions can be selected for use when assigning.

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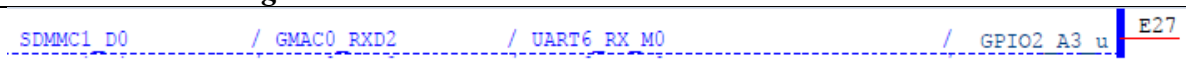


- Except for boot related GPIO, the rest of IOs are reset to input by defaults;
- GPIOx_xx_u where _u indicates that the default state of this IO reset is internal pull-up;
- GPIOx_xx_d where _d indicates that the default state of this IO reset is internal pull-down;
- GPIOx_xx_z where _z indicates that the default state of this IO reset is high impedance;
- **The name suffix of each function with _M0 or M1 or _M2 indicates that the same function is multiplexed on different IO, only one of them can be selected at the same time. For example, when selecting the UART2 function, the UART2_ TX_ M0 and UART2_ RX_ M0 combination must be selected. The combination of UART2_TX_M0 and UART2_RX_M1 is not supported. This is the constraint for all functions with different IOMUX.**

#### 2.1.11.2 GPIO Drive Capability

In RK3568, GPIO provides multiple levels of adjustable driving strength. Most are Level 0-5 and some GPIO can achieve Level 0-11 adjustment levels. For details, please refer to the "RK3568_PinOut" document. In addition, depending on the type of GPIO, the initial default driving strength is different. Please refer to the chip TRM for configuration modification, or refer to Table 5 "SupportDriveStrength" and "DefaultIO DriveStrength" columns in the "RK3568_PinOut" document.

#### 2.1.11.3 GPIO Power

The power pins of the GPIO power domain are described as follows:

Table 2–9 RK3568 GPIO power pins description

| Power domain | GPIO Type | Pin name | Description |
|---|---|---|---|
| PMUIO0 | 1.8V | PMUPLL_AVDD_1V8 | 1.8V Only IO supply for this GPIO domain (group). |
| PMUIO1 | 3.3V | PMUIO1 | 3.3V Only IO supply for this GPIO domain (group). |
| PMUIO2 | 1.8V/3.3V | PMUIO2 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO1 | 1.8V/3.3V | VCCIO1 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO2 | 1.8V/3.3V | VCCIO2 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO3 | 1.8V/3.3V | VCCIO3 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO4 | 1.8V/3.3V | VCCIO4 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO5 | 1.8V/3.3V | VCCIO5 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO6 | 1.8V/3.3V | VCCIO6 | 1.8V or 3.3V IO supply for this GPIO domain (group). |
| VCCIO7 | 1.8V/3.3V | VCCIO7 | 1.8V or 3.3V IO supply for this GPIO domain (group). |

PMUIO0 and PMUIO1 are fixed-level power domains which cannot be configured;

**PMUIO2 and VCCIO1, VCCIO [3:7] power domains require that their hardware power supply voltages must be consistent with the software configuration correspondingly:**

- **When the hardware IO is connected to 1.8V, the software voltage configuration should be set to 1.8V accordingly;**

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- **When the hardware IO is connected to 3.3V, the software voltage configuration should be set to 3.3V accordingly;**

**There is no need to configure VCCIO2 power domain by software, but its hardware power supply and FLASH_VOL_SEL status must be matched:**

- **When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high;**
- **When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low;**

**Otherwise:**

- **If the software configuration is 1.8V, but the hardware power supply is 3.3V, it will cause the low withstand voltage circuit working in overvoltage state, and the IO will be damaged after long time working;**
- **If the software configuration is 3.3V, but the hardware power supply is 1.8V, the circuit will work abnormally;**

For example, the default dts configuration is as follows:

```
&pmu_io_domains {
    status = "okay";
    pmuio1-supply = <&vcc_3v3>;
    pmuio2-supply = <&vcc_3v3>;
    vccio1-supply = <&vcc_3v3>;
    vccio3-supply = <&vcc_3v3>;
    vccio4-supply = <&vcc_1v8>;
    vccio5-supply = <&vcc_3v3>;
    vccio6-supply = <&vcc_1v8>;
    vccio7-supply = <&vcc_3v3>;
};
```

If the actual VCCIO4 power supply is 3.3V, then dts needs to be updated to:

```
&pmu_io_domains {
    status = "okay";
    pmuio1-supply = <&vcc_3v3>;
    pmuio2-supply = <&vcc_3v3>;
    vccio1-supply = <&vcc_3v3>;
    vccio3-supply = <&vcc_3v3>;
    vccio4-supply = <&vcc_3v3>;
    vccio5-supply = <&vcc_3v3>;
    vccio6-supply = <&vcc_1v8>;
    vccio7-supply = <&vcc_3v3>;
};
```

If other power domains have changed and they must be updated and matched accordingly.

**Various documents released by Rockchip have emphasized this notice, please review the voltage**

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**configuration and hardware power supply of your projects as soon as possible!**

Reference documents:

1) DTS configuration documentation: https://redmine.rock-chips.com/documents/106

2) Checklist: Rockchip_RK3568_IO Power Domain Description and Checklist_V1.0_CN.xlsx

Also, note that the IO level of the power domain should be consistent with the IO level of the peripheral chip/device.

At least one 100nF decoupling capacitor must be placed nearby the power supply pins of each power domain. See the reference schematic for the detailed design and they cannot be deleted at will.

If all IOs in a power domain are not used, then the power supply of this power domain does not need to supply power, and the pin leave floating.

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# 2.2 Power Supply Design

## 2.2.1 RK3568 Power Supply Introduction

### 2.2.1.1 Power Supply Requirements of RK3568

Table 2–10 RK3568 power supply requirements

| Module | Power Pin | Description |
|---|---|---|
| PMUPLL | PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8 | PMU PLL Power |
| SYSPLL | SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8 | System PLL Power |
| CPU | VDD_CPU | ARM Power |
| GPU | VDD_GPU | GPU Power |
| NPU | VDD_NPU | NPU Power |
| Logic | VDD_LOGIC | SOC Logic Power |
| PMU Logic | PMU_VDD_LOGIC_0V9 | PMU Logic Power |
| DDR | DDRPHY_VDDQ、<br>DDRPHY_VDDQL | DDR PHY Power |
| GPIO | PMUIO0, PMUIO1, PMUIO2, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7 | IO Domain Power |
| SARADC | SARADC_AVDD_1V8 | SAR ADC Power |
| OTP | OTP_VCC18 | OTP Power |
| USB2.0 PHY | USB3_AVDD_0V9 、 USB3_AVDD_1V8 、 USB3_AVDD_3V3 | USB2.0 PHY Power(Controller use USB3.0, it is combined with the SS signal of MULTI PHY0/1 to form a complete USB3.0 interface, so the name starts with USB3) |
| USB2.0 PHY | USB2_AVDD_0V9 、 USB2_AVDD_1V8 、 USB2_AVDD_3V3 | USB2.0 PHY Power |
| MULTI_PHY | MULTI_PHY_AVDD_0V9 、 MULTI_PHY_AVDD_1V8 | MULTI_PHY Power |
| PCIe3.0 PHY | PCIE30_AVDD_0V9、<br>PCIE30_AVDD_1V8 | PCIe3.0 PHY Power |
| MIPI CSI RX PHY | MIPI_CSI_RX_AVDD_0V9 、 MIPI_CSI_RX_AVDD_1V8 | MIPI CIS RX PHY Power |
| MIPI DSI TX0/LVDS TX Combo PHY | MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 、 MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 | MIPI DSI TX0/LVDS TX Combo PHY Power |
| MIPI DSI TX1 PHY | MIPI_DSI_TX1_AVDD_0V9 、 MIPI_DSI_TX1_AVDD_1V8 | MIPI DSI TX1 PHY Power |
| eDP TX PHY | eDP_TX_AVDD_0V9、<br>eDP_TX_AVDD_1V8 | eDP TX PHY Power |
| HDMI2.0 TX PHY | HDMI_TX_AVDD_0V9、<br>HDMI_TX_AVDD_1V8 | HDMI2.0 TX PHY Power |

### 2.2.1.2 Power-on Sequence Requirements of RK3568

Theoretically, follow the principle: for the same module, low voltage power on first, high voltage power on later; for the same module with the same voltage can power on together, and there is no timing requirement between different modules, after the last voltage is stable, RESETn can only be released after at least 10ms.

- The recommended power-on sequence of the digital power supply is as follows:

PMU_VDD_LOGIC_0V9 → VDD_LOGIC → VDD_CPU/VDD_GPU/VDD_NPU

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The recommended power-on sequence for SARADC is as follows:

VDD_LOGIC → SARADC_AVDD_1V8

- The recommended power-on sequence for OTP is as follows:

VDD_LOGIC → OTP_VCC18

- The recommended power-on sequence for USB PHY is as follows:

USB3_AVDD_0V9 → USB3_AVDD_1V8 → USB3_AVDD_3V3

USB2_AVDD_0V9 → USB2_AVDD_1V8 → USB2_AVDD_3V3

- The recommended power-on sequence for MIPI CSI RX PHY is as follows:

MIPI_CSI_RX_AVDD_0V9 → MIPI_CSI_RX_AVDD_1V8

- The recommended power-on sequence for MIPI DSI TX0/LVDS Combo PHY is as follows:

MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 → MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8

- There is no restriction on other modules power-on sequence.

According to the power network name assigned by the reference schematic, the overall recommended power-on sequence is as follows:

VDDA0V9_PMU、VDDA_0V9、VDD_LOGIC → VCCA1V8_PMU、VCCA_1V8、VDD_GPU、VCC3V3_PMU、VCC_1V8 → VDD_CPU、VCC2V5_DDR → VCC_DDR → VCC_3V3、VCCIO_SD、VCC3V3_SD → RESETn

Intervals>=0us

#### 2.2.1.3 Power-off Sequence Requirements of RK3568

During the power-off process, RESETn must be pulled down first, and then each power supply will be powered off.

### 2.2.2 Power Supply Design Suggestion

#### 2.2.2.1 Power-on and Standby Circuit Scheme

- The power supply status of each module of RK3568 is shown as the following Table when it is first powered on:

Table 2–11 RK3568 power supply requirement of each module for the first powered on

| Module | Power Pin | Power supply requirements in first power-on |
|---|---|---|
| PMUPLL | PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8 | **Must be powered** |
| SYSPLL | SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8 | **Must be powered** |
| CPU | VDD_CPU | **Must be powered** |
| GPU | VDD_GPU | Can be unpowered |
| NPU | VDD_NPU | Can be unpowered |
| Logic | VDD_LOGIC | **Must be powered** |
| PMU Logic | PMU_VDD_LOGIC_0V9 | **Must be powered** |

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| Module | Power Pin | Power supply requirements in first power-on |
|---|---|---|
| DDR | DDRPHY_VDDQ、DDRPHY_VDDQL | **Must be powered** |
| GPIO | PMUIO0、PMUIO1、PMUIO2 | **Must be powered** |
| GPIO | VCCIO2 | **Must be powered** |
| GPIO | VCCIO3 | **Must be powered** |
| GPIO | VCCIO1、VCCIO4、VCCIO5、VCCIO6、VCCIO7 | Can be unpowered |
| SARADC | SARADC_AVDD_1V8 | **Must be powered** |
| OTP | OTP_VCC18 | **Must be powered** |
| USB2.0 PHY | USB3_AVDD_0V9、USB3_AVDD_1V8、USB3_AVDD_3V3、 | **Must be powered** |
| USB2.0 PHY | USB2_AVDD_0V9、USB2_AVDD_1V8、USB2_AVDD_3V3 | Can be unpowered |
| MULTI_PHY | MULTI_PHY_AVDD_0V9、MULTI_PHY_AVDD_1V8 | Can be unpowered |
| PCIe3.0 PHY | PCIE30_AVDD_0V9、PCIE30_AVDD_1V8 | Can be unpowered |
| MIPI CSI RX PHY | MIPI_CSI_RX_AVDD_0V9、MIPI_CSI_RX_AVDD_1V8 | Can be unpowered |
| MIPI DSI TX0/LVDS Combo PHY | MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9、MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 | Can be unpowered |
| MIPI DSI TX1 PHY | MIPI_DSI_TX1_AVDD_0V9、MIPI_DSI_TX1_AVDD_1V8 | Can be unpowered |
| deep TX PHY | eDP_TX_AVDD_0V9、eDP_TX_AVDD_1V8 | Can be unpowered |
| HDMI2.0 TX PHY | HDMI_TX_AVDD_0V9、HDMI_TX_AVDD_1V8 | Can be unpowered |

**Note: If the unused module is not powered, the software is required to disable the configuration of the corresponding node in the DTS, otherwise it may cause the kernel initialization stuck.**

- The RK3568 chip can support a low-power standby solution. When entering the standby mode, the power supply and power-off conditions are as follows:

Table 2–12 RK3568 standby power supply requirements

| Module | Power Pin | Power supply requirements in Low power consumption standby |
|---|---|---|
| PMUPLL | PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8 | **Power must be supplied** |
| SYSPLL | SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8 | Can support power off |
| CPU | VDD_CPU | Can support power off |
| GPU | VDD_GPU | Can support power off |
| NPU | VDD_NPU | Can support power off |
| Logic | VDD_LOGIC | Can support power off |
| PMU Logic | PMU_VDD_LOGIC_0V9 | **Power must be supplied** |
| DDR | DDRPHY_VDDQ、DDRPHY_VDDQL | **Power must be supplied** |

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| Module | Power Pin | Power supply requirements in Low power consumption standby |
|---|---|---|
| GPIO | PMUIO0、PMUIO1、PMUIO2 | **Power must be supplied** |
| GPIO | VCCIO2 | Can support power off |
| GPIO | VCCIO3 | Can support power off |
| GPIO | VCCIO1、VCCIO4、VCCIO5、VCCIO6、VCCIO7 | Can support power off |
| SARADC | SARADC_AVDD_1V8 | Can support power off |
| OTP | OTP_VCC18 | Can support power off |
| USB2.0 PHY | USB3_AVDD_0V9、USB3_AVDD_1V8、USB3_AVDD_3V3、 | Can support power off |
| USB2.0 PHY | USB2_AVDD_0V9、USB2_AVDD_1V8、USB2_AVDD_3V3 | Can support power off |
| MULTI_PHY | MULTI_PHY_AVDD_0V9、MULTI_PHY_AVDD_1V8 | Can support power off |
| PCIe3.0 PHY | PCIE30_AVDD_0V9、<br>PCIE30_AVDD_1V8 | Can support power off |
| MIPI CSI RX PHY | MIPI_CSI_RX_AVDD_0V9、MIPI_CSI_RX_AVDD_1V8 | Can support power off |
| MIPI DSI TX0/LVDS Combo PHY | MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9<br>、<br>MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 | Can support power off |
| MIPI DSI TX1 PHY | MIPI_DSI_TX1_AVDD_0V9、MIPI_DSI_TX1_AVDD_1V8 | Can support power off |
| eDP TX PHY | eDP_TX_AVDD_0V9、<br>eDP_TX_AVDD_1V8 | Can support power off |
| HDMI2.0 TX PHY | HDMI_TX_AVDD_0V9、<br>HDMI_TX_AVDD_1V8 | Can support power off |

This standby solution can only support IO interrupt wake-up of PMUIO0, PMUIO1 and PMUIO2.

In the standby state, at least the following four groups of power supplies should be kept turning on (refer to the power supply network name in the schematic):

- VCC_DDR/VCC0V6_DDR: Provide power for DDR self-refresh (DDR4: 2.5V power supply also needs power supply, LPDDR3/LPDDR4/LPDDR4x: 1.8V power supply also needs power supply);
- VDDA0V9_PMU: Provide power for the logic of PMUIO0 & PMUIO1 & PMUIO2 power domain; It also provides power for PMUPLL and chip OSC work;
- VCCA1V8_PMU: Provide power for PMUPLL work; provide IO power for PMUIO0 power domain to maintain output status and interrupt response;
- VCC3V3_PMU: Provide IO power for PMUIO1 & PMUIO2 power domain to maintain output status and interrupt response;

In standby, if it need to supports USB HID device wake-up, the USB PHY power supply must remain powered; if it need to supports IO interrupt wake-up in VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7, VDD_LOGIC and VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7 power supply must be kept.

#### 2.2.2.2 PLL Power Supply

The PLL of RK3568 chip is distributed in two parts as follows:

Table 2–13 RK3568 internal PLL Introduction

| | Power | Standby Mode |
|---|---|---|
| Inside the PMU unit | PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8 | Can't turn off the power |
| Modules in the chip | SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8 | Can turn off the power |

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- PMUPLL_AVDD_0V9: Peak current 10mA
- PMUPLL_AVDD_1V8: Peak current 9mA
- SYSPLL_AVDD_0V9: Peak current 30mA
- SYSPLL_AVDD_1V8: Peak current 18mA

It is recommended to use LDO for power supply, PSRR@1KHz should be greater than 65dB, and the power supply capacity should be more than 200mA.

0.9V AC requirement: <20mV;

1.8V AC requirement: <50mV;

A stable PLL power supply will improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Refer to the schematic for the detailed number and capacity of the capacitors. Please do not change them at will.

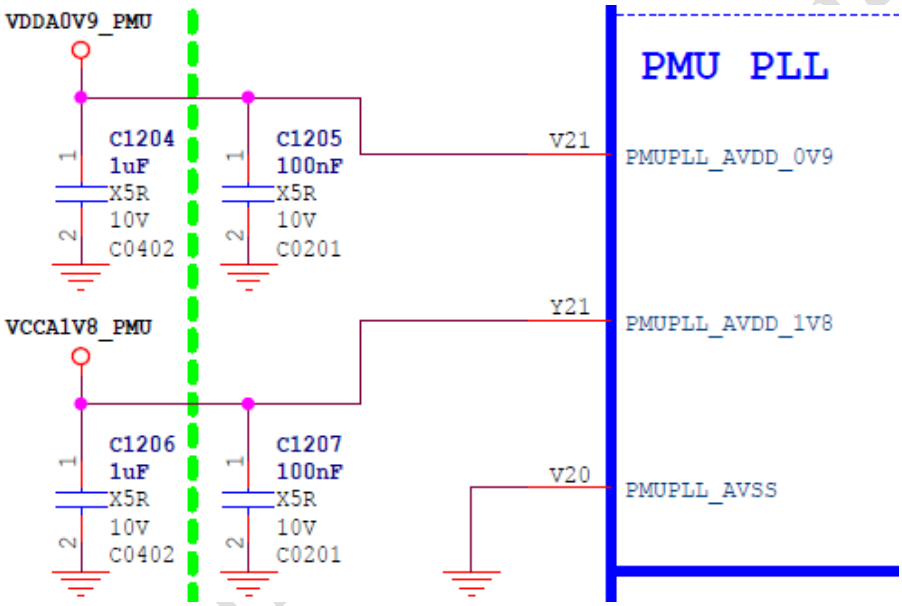


Figure 2-43 RK3568 PMU PLL power pin

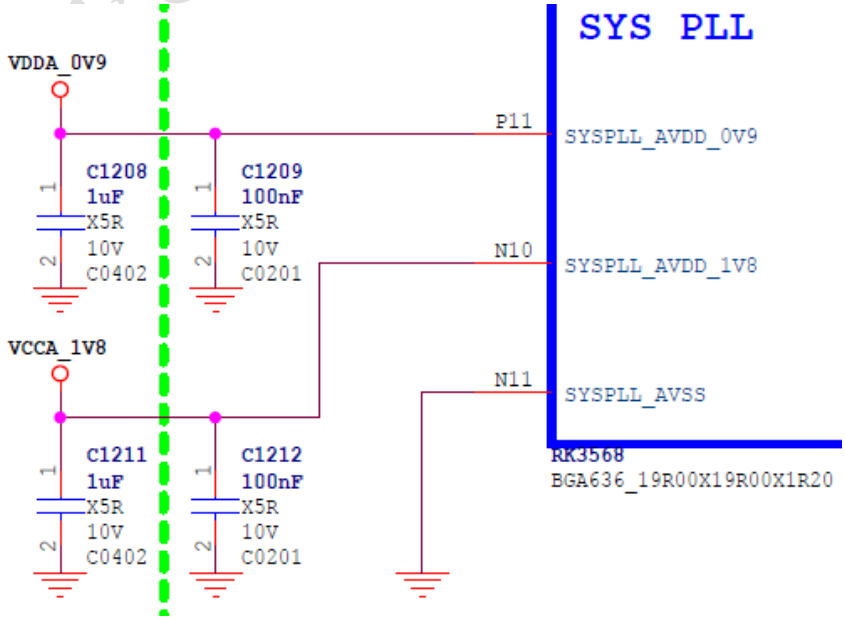


Figure 2-44 RK3568 SYS PLL power pin

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#### 2.2.2.3 PMU LOGIC Power Supply

The PMU_VDD_LOGIC_0V9 power supply of RK3568 supplies the LOGIC of the internal PMU unit with a peak current of 50mA. Please do not delete the decoupling capacitor in the RK3568 chip reference schematic.

DC/DC or LDO can be used for power supply. From the cost considerations, it can work with PMUPLL_AVDD_0V9 power supply together.

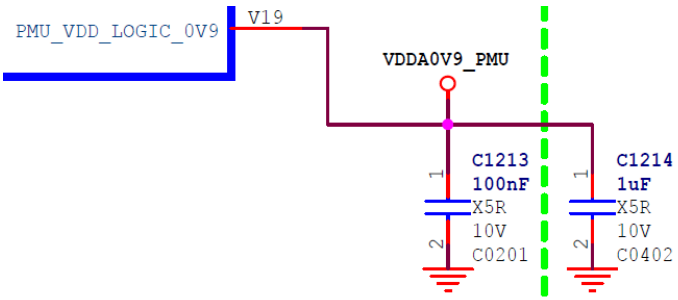


Figure 2-45 RK3568 PMU_VDD_LOGIC_0V9 power pin

#### 2.2.2.4 CPU Power Supply

The VDD_CPU power of RK3568 supplies power to the internal ARM Cortex-A55 core, which is independently powered by DC/DC power supply and supports dynamic frequency and voltage regulation function. The peak current can reach more than 3A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 4A;
- The output voltage accuracy is required at ±1.5%;
- BUCK transient response requirements: $I_{load}$=BUCK Max current*10%~BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1000, C1001, and C1004 capacitors in the figure below on the back of the RK3568 chip during layout. C1002 and C1003 should be as close as possible to RK3568. The total capacitance of the VDD_CPU power supply must be greater than 135μF (it is recommended to reserve one or two 22μF capacitors, which cannot be connected by default), in order to ensure that the power supply ripple is within 80mV, then avoid large power supply ripples under heavy load conditions.

The VDD_CPU_COM signal is the VDD_CPU power feedback pin, which needs to be connected to the FB of the DC/DC power supply, which can effectively improve the voltage drop caused by PCB routing and improve the timeliness of power dynamic adjustment.

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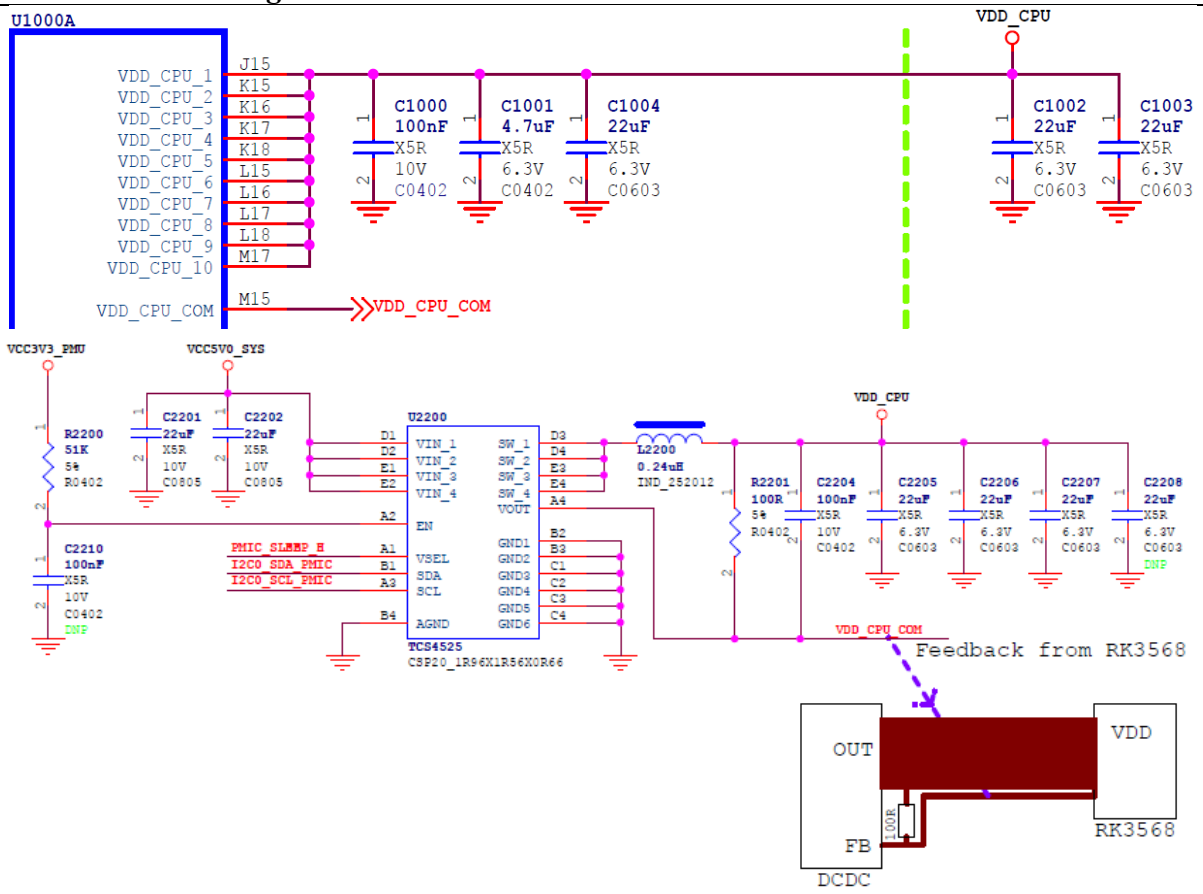


Figure 2-46 RK3568 VDD_CPU power pin and power supply DC/DC

### 2.2.2.5 GPU Power Supply

The VDD_GPU power of RK3568 supplies power to the internal GPU unit. It uses DC/DC power supply and supports dynamic frequency and voltage regulation. The peak current can reach 1.2A. Please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be ±1.5%;
- BUCK transient response requirements: $I_{load}$=BUCK Max current*10%~BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1012, C1013, and C1014 capacitors in the figure below on the back of the RK3568 chip during layout. C1015 and C1016 should be as close as possible to RK3568. The total capacitance of the VDD_CPU power supply need to be greater than 90μF, in order to ensure that the power supply ripple is within 60mV, and avoid large power supply ripples under heavy load conditions.

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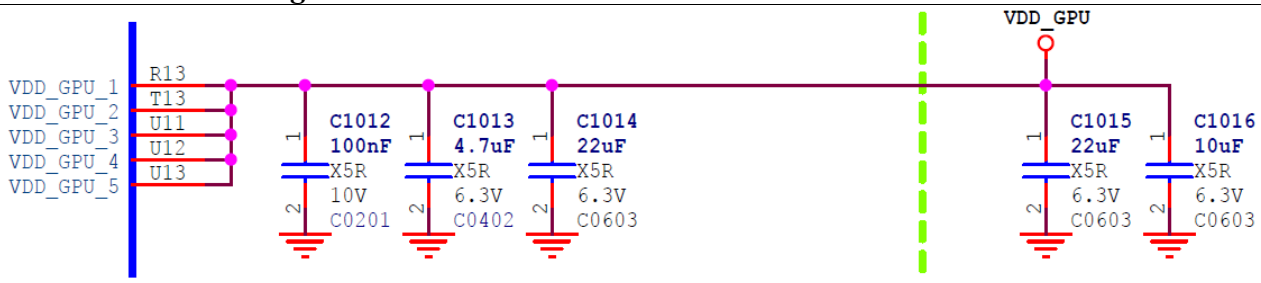


Figure 2-47 RK3568 VDD_GPU power pin

#### 2.2.2.6 NPU Power Supply

The VDD_NPU power of RK3568 supplies the internal NPU unit with DC/DC power supply and supports dynamic frequency and voltage regulation. The peak current can reach 1A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be ±1.5%;
- BUCK transient response requirements: $I_{load}$=BUCK Max current*10%~BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1017 and C1018 capacitors in the figure below on the back of the RK3568 chip during layout. C1019 and C1020 should be as close as possible to RK3568. The total capacitance of the VDD_CPU power supply need to be greater than 90μF, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.


Figure 2-48 RK3568 VDD_NPU power pin

#### 2.2.2.7 Logic Power Supply

The VDD_LOGIC power of RK3568 supplies power to the internal logic unit. It uses a DC/DC power supply for independent power supply, which can support dynamic frequency and voltage regulation, and the default fixed voltage for power supply. The peak current can reach 1A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be ±1.5%;
- BUCK transient response requirements: $I_{load}$=BUCK Max current*10%~BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

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Place the C1005, C1006, C1007 and C1008 capacitors in the figure below on the back of the RK3568 chip during layout. C1010 and C1011 should be as close as possible to RK3568. The total capacitance of the VDD_LOGIC power supply need to be greater than 90μF, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

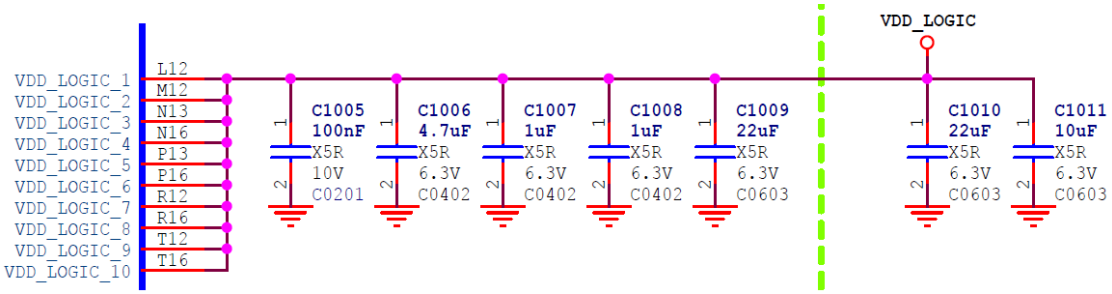


Figure 2-49 RK3568 VDD_LOGIC power pin

### 2.2.2.8 DDR Power Supply

The DDR PHY interface of RK3568 chip supports DDR3/DDR3L/DDR4/LPDDR4/LPDDR4x level standards. RK3568 DDR PHY has two power supplies, DDRPHY_VDDQ and DDRPHY_VDDQL. For power supply introduction, please refer to Section **2.1.7.5 DDR power supply design and power-on sequence requirements**. When designing a product, please confirm whether it meets the design requirements according to the use of DDR.

Similarly, use DC/DC for power supply; different DDR with different peak current, please evaluate the peak current according to the actual selected DDR. For a single LPDDR3 or a single LPDDR4 or a single LPDDR4x or two 16bit DDR3/3L or two 16bit DDR4, 1A DC/DC can be selected; for more than two DDR3 or DDR4, it is recommended to use a DC/DC above 2A. In addition, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

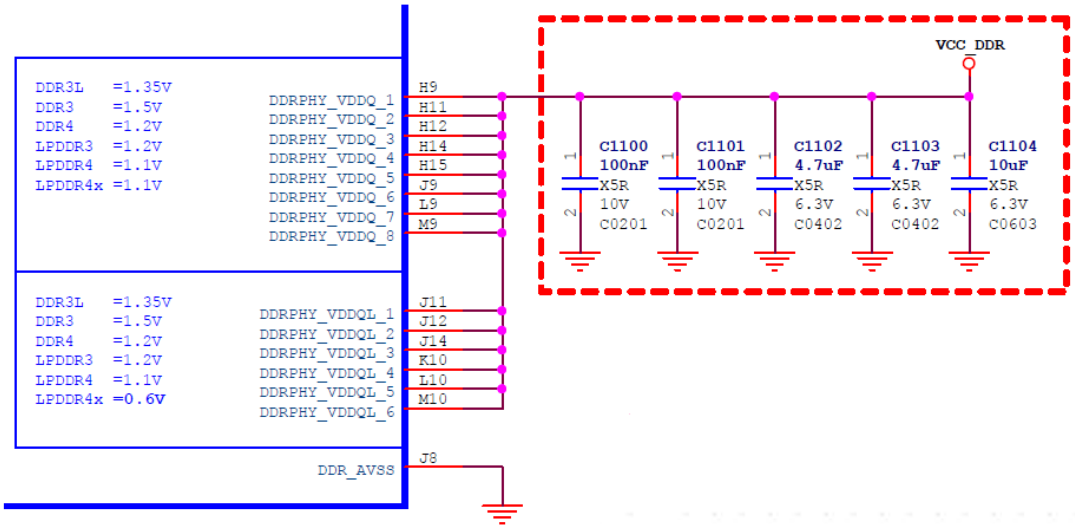


Figure 2-50 RK3568 VCC_DDR power pin in DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 mode

Place the C1100, C1101, C1102, C1103 and C1104 capacitors in the figure above on the back of the RK3568 chip during layout, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

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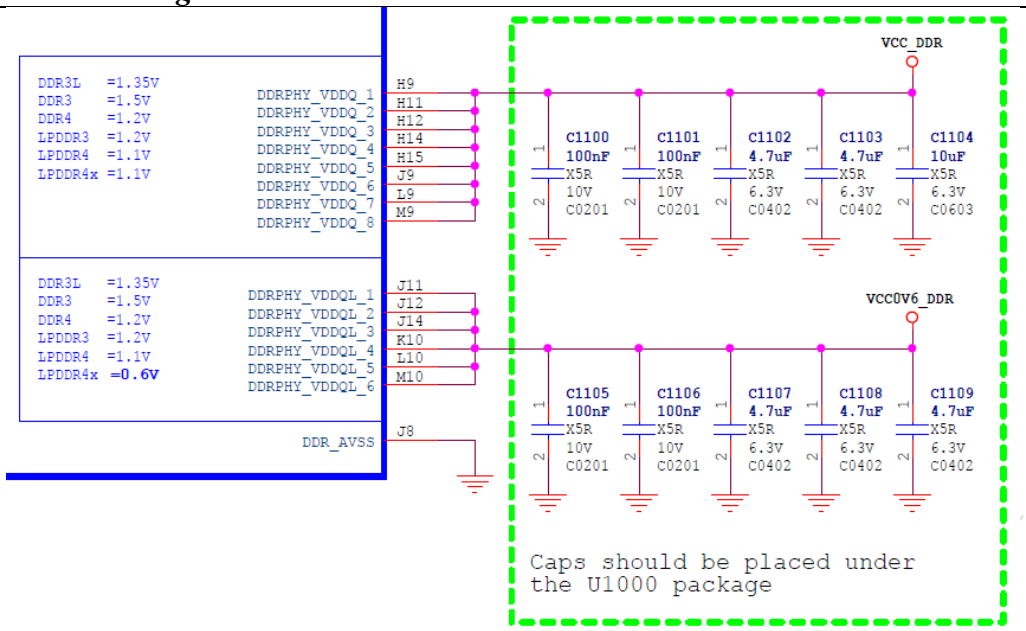



Figure 2-51 RK3568 VCC_DDR and VCC0V6_DDR power pins in LPDDR4x mode

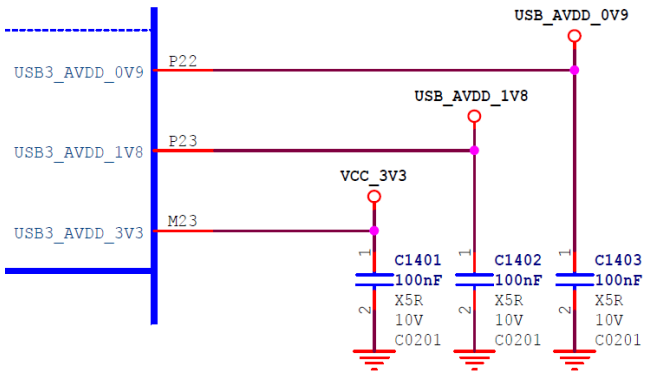
Place the C1100, C1101, C1102, C1103, C1104, C1105, C1106, C1107, C1108 and C1109 capacitors in the figure above on the back of the RK3568 chip during layout, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

#### 2.2.2.9 USB2.0 PHY Power Supply

RK3568 has four USB2.0 interfaces, and USB3_OTG0_DP/M, USB3_HOST1_DP/M with MULTI_PHY0, MULTI_PHY1 can form a USB3.0 interface. For details, please refer to **Section 2.3.4 USB2.0/USB3.0 Circuit**.

The USB3_AVDD_0V9, USB3_AVDD_1V8, USB3_AVDD_3V3 supply power to the USB3_OTG0_DP/M and USB3_HOST1_DP/M PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 reference schematic.

The USB2_AVDD_0V9, USB2_AVDD_1V8, and USB2_AVDD_3V3 supplies power to the USB2_HOST2_DP/M and USB2_HOST3_DP/M PHY. Please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

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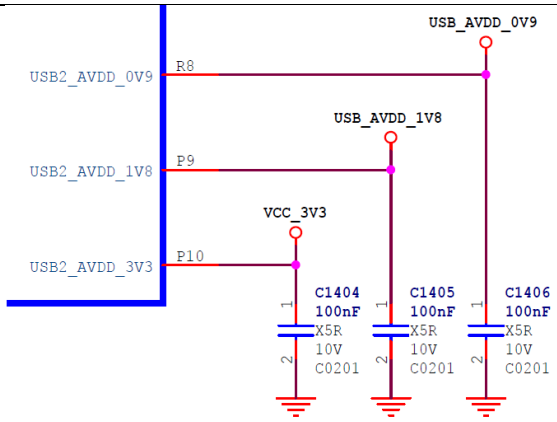


Figure 2-52 RK3568 USB2.0 PHY power pin

- USB3_AVDD_0V9: Peak current 5mA
- USB3_AVDD_1V8: Peak current 30mA
- USB3_AVDD_3V3: Peak current 10mA
- USB2_AVDD_0V9: Peak current 5mA
- USB2_AVDD_1V8: Peak current 30mA
- USB2_AVDD_3V3: Peak current 10mA

It is recommended to use LDO for power supply, PSRR@1KHz should be greater than 65dB, and the power supply capacity should be more than 200mA.

- 0.9V AC requirement: <25mV;
- 1.8V AC requirement: <50mV;
- 3.3V AC requirement: <200mV;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

**Since the firmware of the RK3568 chip must be downloaded from the USB3_OTG0_DP/M interface, USB3_AVDD_0V9, USB3_AVDD_1V8, USB3_AVDD_3V3 must be powered in the first time power-on.**

If USB2_HOST2_DP/M and USB2_HOST3_DP/M are not used, then USB2_AVDD_0V9, USB2_AVDD_1V8, USB2_AVDD_3V3 could be unpowered, and they are recommended to be grounded. **But attention please: when the PHY is not powered, if the USB controller node corresponding to PHY in the kernel DTS is not disabled, it will cause to be stuck in the initialization of the USB controller during kernel initialization.**

#### 2.2.2.10 MULTI PHY Power Supply

The RK3568 has three MULTI PHY interfaces:

MULTI_PHY0 is the function multiplexing of USB3.0 OTG0 SS signal and SATA0;

MULTI_PHY1 is the function multiplexing of USB3.0 HOST1 SS signal, SATA1 and QSGMII_M0;

MULTI_PHY2 is the function multiplexing of PCIe2.0, SATA2 and QSGMII_M1;

MULTI_PHY_AVDD_0V9_1, MULTI_PHY_AVDD_0V9_2 and MULTI_PHY_AVDD_1V8 supply power to MULTI_PHY0, 1, 2, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

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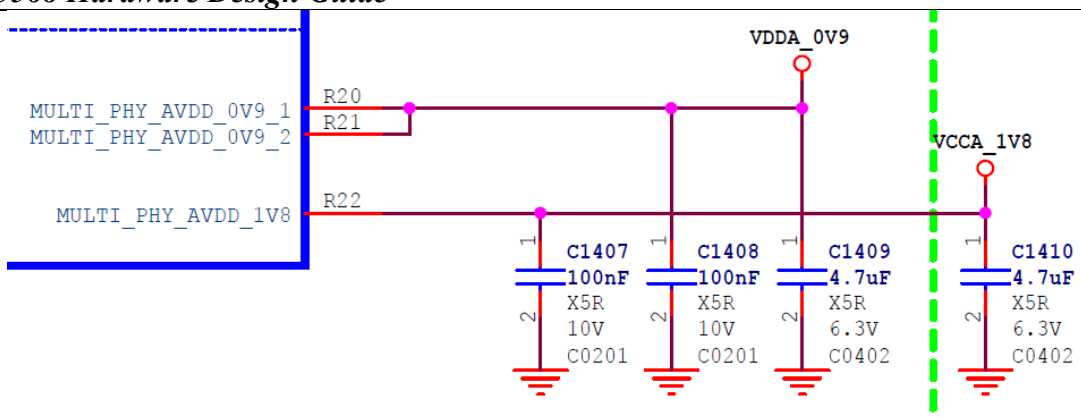


Figure 2-53 RK3568 MULTI_PHY power pin

- MULTI_PHY_AVDD_0V9: Peak current 150mA
- MULTI_PHY_AVDD_1V8: Peak current 21mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MULTI_PHY0/1/2 functions are not used, then MULTI_PHY_AVDD_0V9 and MULTI_PHY_AVDD_1V8 can be powered off, and grounding is recommended.

#### 2.2.2.11 PCIe3.0 PHY Power Supply

The RK3568 has a PCIe3.0 interface.

PCIE30_AVDD_0V9_1, PCIE30_AVDD_0V9_2, and PCIE30_AVDD_1V8 supply power to PCIe3.0 PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

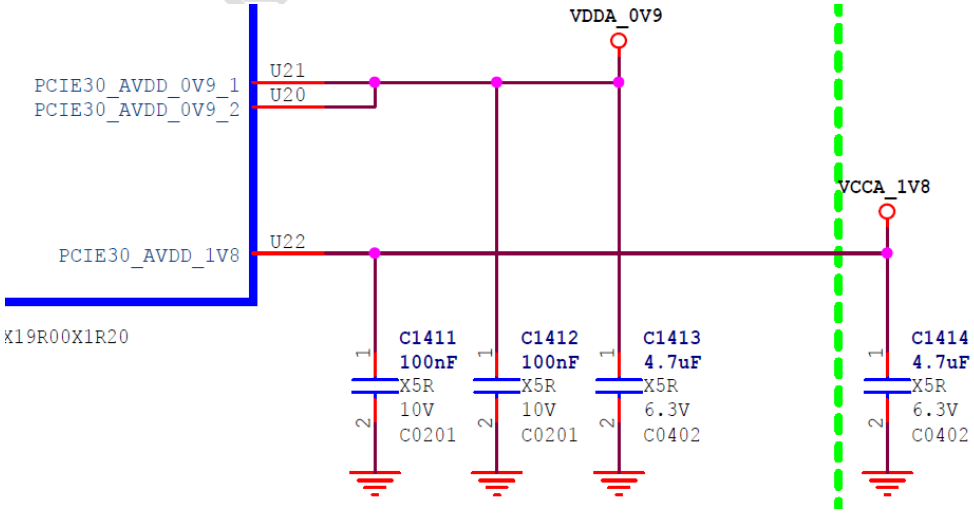


Figure 2-54 RK3568 PCIe3.0 PHY power pin

- PCIE30_AVDD_0V9: Peak current 160mA

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- PCIE30_AVDD_1V8: Peak current 60mA
- It is recommended to use LDO for power supply,
- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the PCIe3.0 function is not used, then PCIE30_AVDD_0V9 and PCIE30_AVDD_1V8 do not need to be powered. Grounding is recommended.

#### 2.2.2.12 MIPI CSI RX PHY Power Supply

The RK3568 has a MIPI CSI RX interface.

MIPI_CSI_RX_AVDD_0V9, and MIPI_CSI_RX_AVDD_1V8 supply power to MIPI CSI RX PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

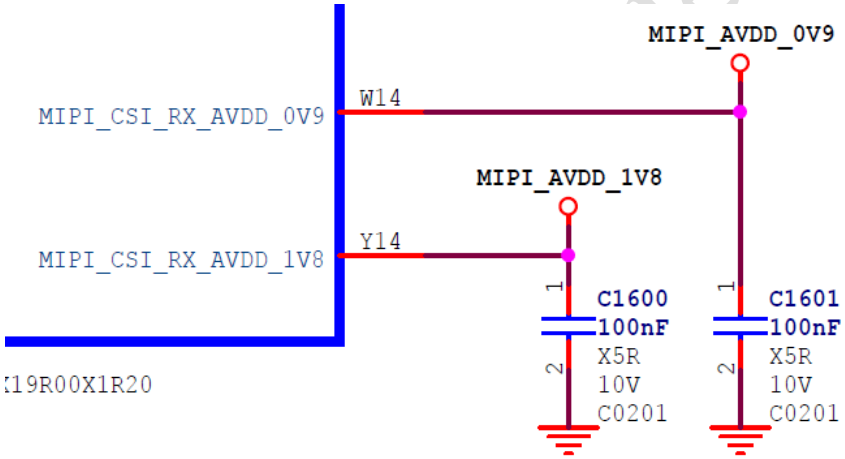


Figure 2-55 RK3568 MIPI CSI RX PHY power pin

- MIPI_CSI_RX_AVDD_0V9: Peak current 10mA
- MIPI_CSI_RX_AVDD_1V8: Peak current 2.5mA
  - It is recommended to use LDO for power supply,
- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI CSI RX function is not used, MIPI_CSI_RX_AVDD_0V9 and MIPI_CSI_RX_AVDD_1V8 can be unpowered, and grounding is recommended.

#### 2.2.2.13 MIPI DSI TX0/LVDS PHY Power Supply

The RK3568 has a MIPI DSI TX0 and a LVDS TX Combo PHY interface.

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MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 and MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 supply power to MIPI DSI TX0 and LVDS TX Combo PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

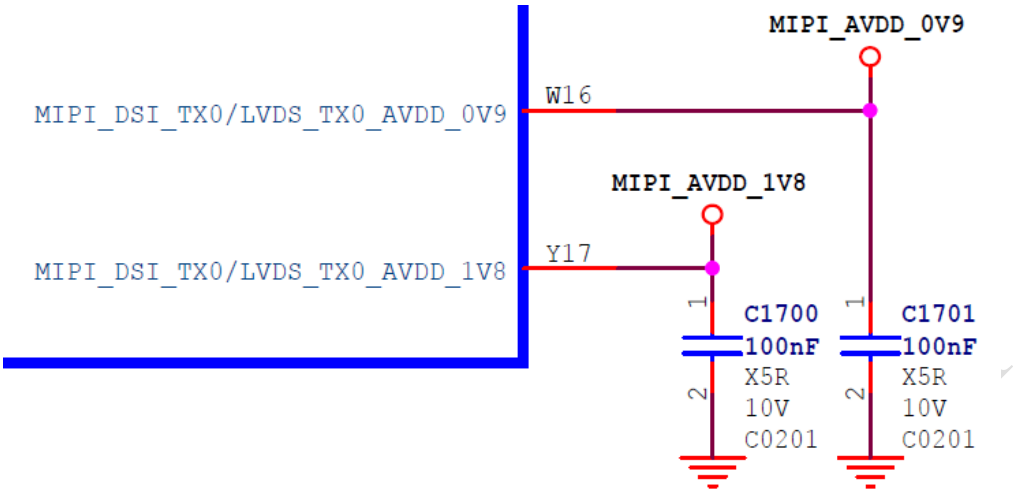


Figure 2-56 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY power pin

- MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9: Peak current 50mA
- MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8: Peak current 15mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI DSI TX0 and LVDS TX functions are not used, MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 and MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 can be powered off, and grounding is recommended.

#### 2.2.2.14 MIPI DSI TX1 PHY Power Supply

The RK3568 has a MIPI DSI TX1 PHY interface.

MIPI_DSI_TX1_AVDD_0V9, and MIPI_DSI_TX1_AVDD_1V8 power supplies which supply power to MIPI DSI TX1 PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

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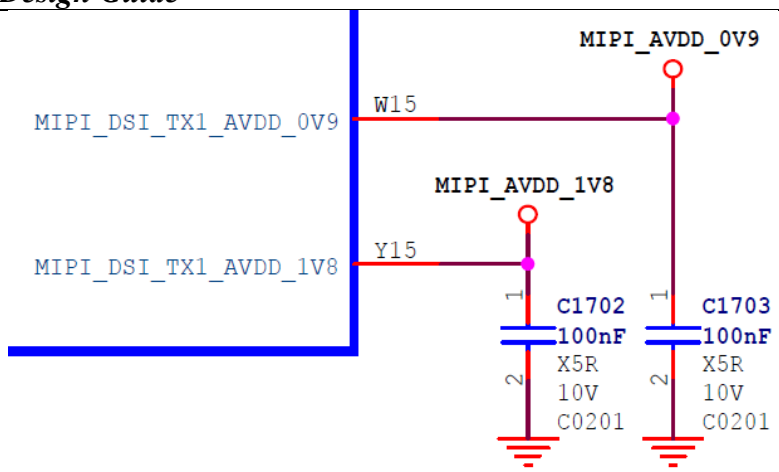


Figure 2-57 RK3568 MIPI DSI TX1 PHY power pin

- MIPI_DSI_TX1_AVDD_0V9: Peak current 50mA
- MIPI_DSI_TX1_AVDD_1V8: Peak current 15mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI DSI TX1 function is not used, MIPI_DSI_TX1_AVDD_0V9 and MIPI_DSI_TX1_AVDD_1V8 can be powered off, and grounding is recommended.

### 2.2.2.15 eDP PHY Power Supply

The RK3568 has an eDP TX PHY interface.

eDP_TX_AVDD_0V9 and eDP_TX_AVDD_1V8 supply power to eDP TX PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

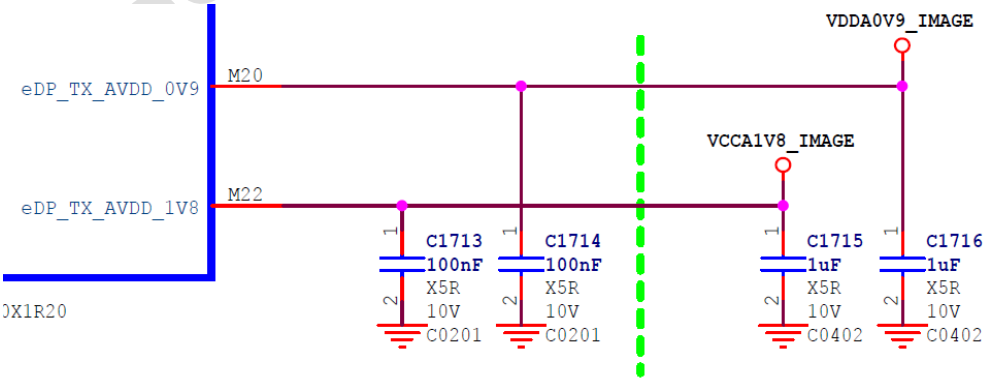


Figure 2-58 RK3568 eDP TX PHY power pin

- eDP_TX_AVDD_0V9: Peak current 150mA
- eDP_TX_AVDD_1V8: Peak current 100mA

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It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mVpower supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the eDP TX function is not used, then eDP_TX_AVDD_0V9 and eDP_TX_AVDD_1V8 do not need to be powered, and grounding is recommended.

#### 2.2.2.16 HDMI2.0 PHY Power Supply

The RK3568 has an HDMI2.0 TX PHY interface.

HDMI_TX_AVDD_0V9_1, HDMI_TX_AVDD_0V9_2 and HDMI_TX_AVDD_1V8 supply power to HDMI2.0 TX PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

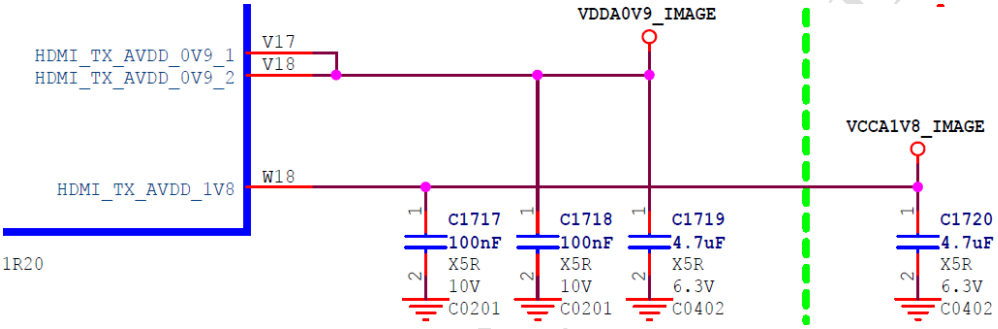


Figure 2-59 RK3568 HDMI2.0 TX PHY power pin

- HDMI_TX_AVDD_0V9: Peak current 25mA
- HDMI_TX_AVDD_1V8: Peak current 16mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the HDMI2.0 TX function is not used, then HDMI_TX_AVDD_0V9 and HDMI_TX_AVDD_1V8 do not need to be powered, they are recommended to be grounded.

#### 2.2.2.17 SARADC/OTP Power Supply

The RK3568 has a SARADC, which can support 8 channels. SARADC_AVDD_1V8 supplies power to SARADC. Please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

- SARADC_AVDD_1V8: Peak current 1.5mA

It is recommended to use LDO for power supply,

- PSRR@1KHz should >65dB;

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- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

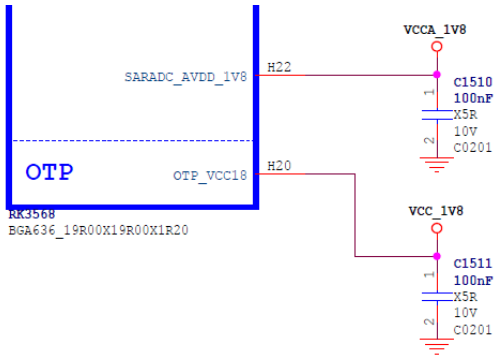


Figure 2-60 RK3568 SARADC and OTP power pin

The RK3568 has an OTP, OTP_VCC18 supplies power to OTP, please do not delete the capacitor in the RK3568 chip reference schematic.

- OTP_VCC18: Peak current 59mA

  LDO or DC/DC can be used to supply power to OTP.

  A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

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## 2.2.3 RK809-5 Solution Introduction

### 2.2.3.1 RK809-5 Block Diagram

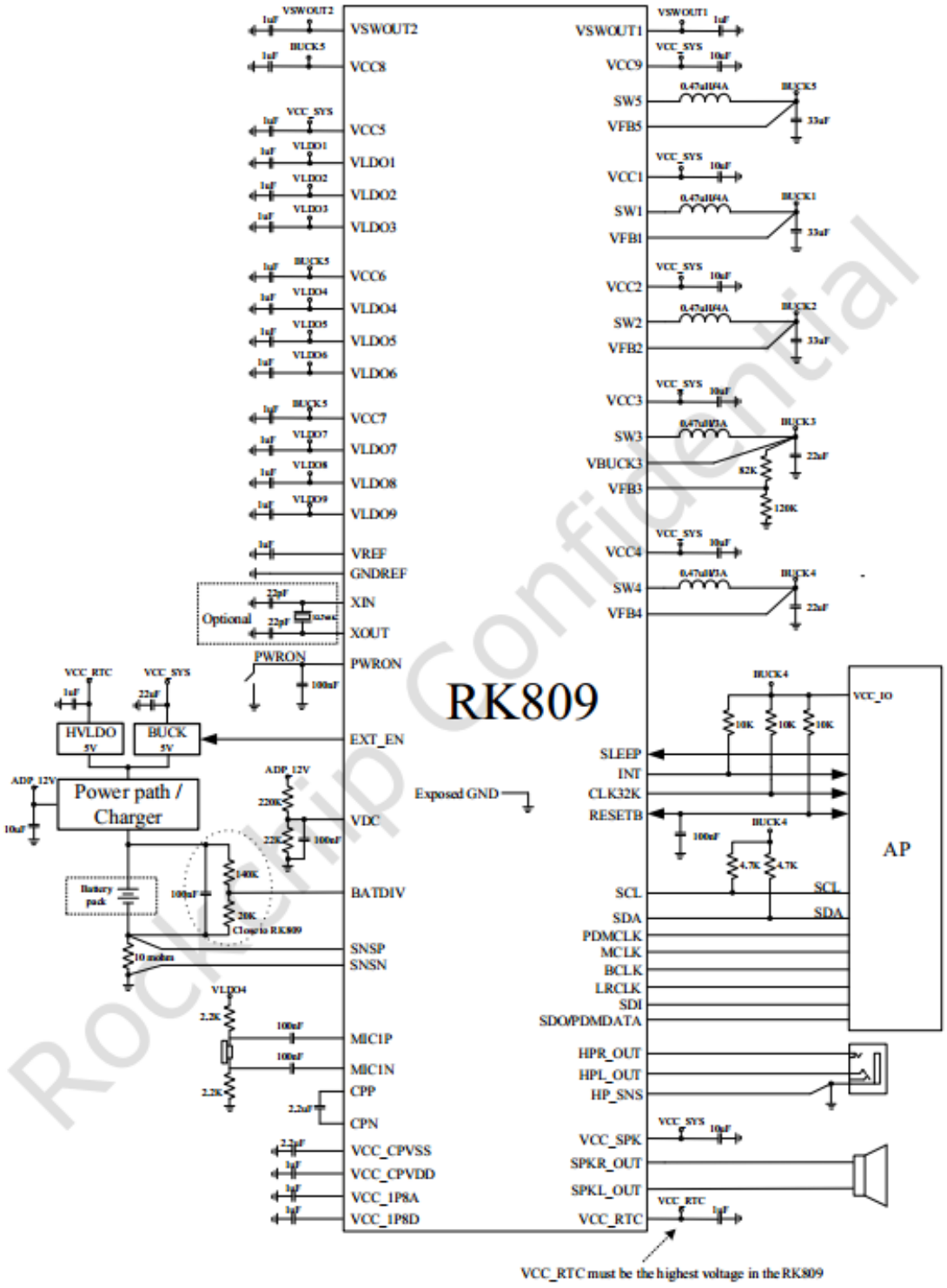


Figure 2-61 RK809-5 block diagram

### 2.2.3.2 RK809-5 Features

- Power input range: 2.7V-5.5V
- Accurate fuel gauge with two ADC of separate battery voltage and current
- Built-in real-time clock (RTC)
- Very low standby current of 35uA (at 32KHz clock frequency)

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- Support real ground class-AB PA to drive Head-phone
- 1.3W Class-D power amplifier without filter inductor
- Fixed and programmable optional power start sequence control
- Built-in high-performance audio codec
  - Built-in independent PLL
  - Support microphone input
  - Both DAC and ADC support I2S digital input
  - Support ALC, limiter and noise gate
  - Support programmable digital and analog gain
  - Support 16bits-32bits bit rate
  - Sampling rate up to 192kHz
  - The software supports two working mode configurations of master and slave
  - Support three I2S formats (standard, left-aligned, right-aligned)
  - Support PDM mode (external input PCLK)
- Power channels:
  - BUCK1: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK2: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK3: Synchronous step-down DC-DC converter, 1.5A max
  - BUCK4: Synchronous step-down DC-DC converter, 1.5A max
  - BUCK5: Synchronous step-down DC-DC converter, 2.5A max
  - LDO1-LDO2, LDO4~LDO9: Low-dropout linear regulator, 400mA max
  - LDO3: Low-noise and high PSRR low-dropout linear regulator, 100mA max
  - Switch1: Switch, 2.1A max, Rdson=90 mohm
  - Switch2: Switch, 2.1A max, Rdson=100 mohm
- Package: 7mmx7mm QFN68

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### 2.2.3.3 RK3568+RK809-5 Power Tree

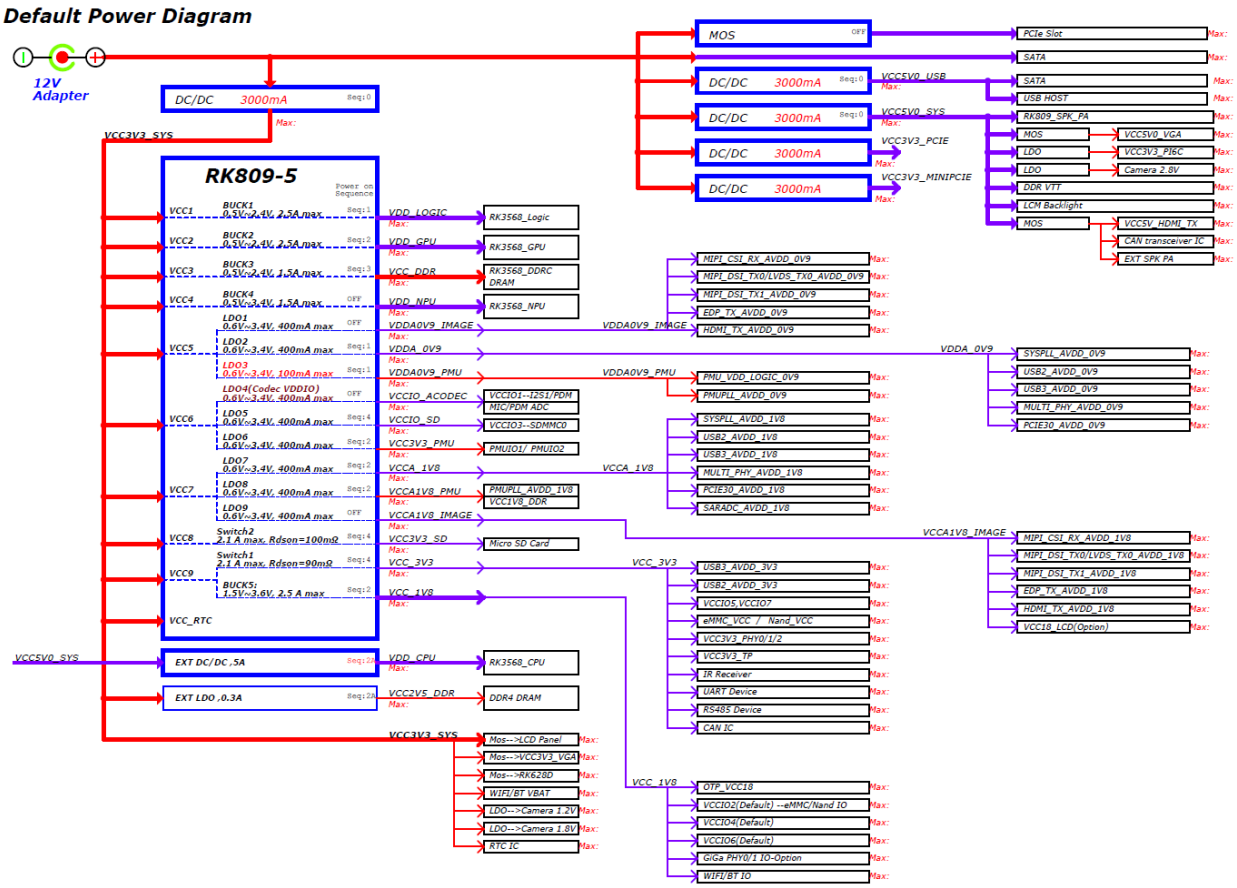


Figure 2-62 RK3568 and RK809-5 power tree

### 2.2.3.4 RK809-5 Power-on Sequence

The power-on sequence of RK809-5 has been solidified and cannot be changed. Note that the power-on sequence of RK809-5 is different with the power-on sequence of RK809-1, RK809-2 and RK809-3, and cannot be mixed.

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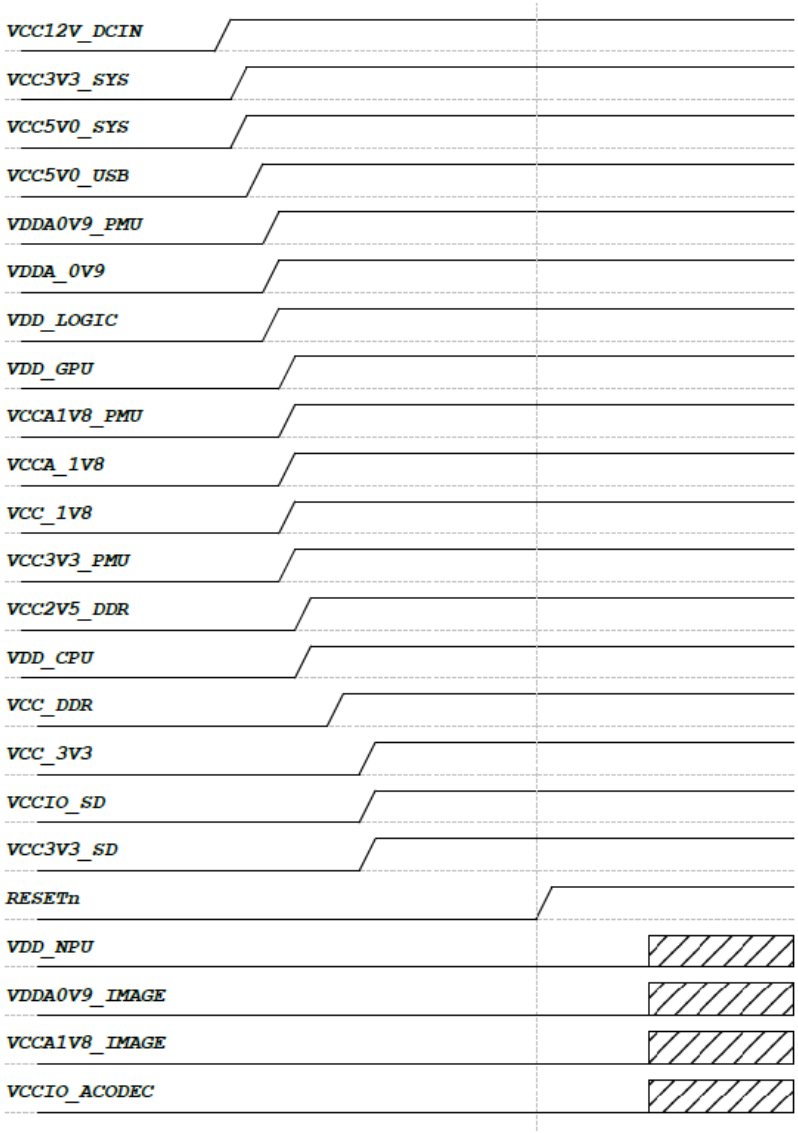


| Power Supply | PMIC Channel | Supply Limit | Power Name | Time Slot | Default Voltage | Default ON/OFF | Work Voltage | Peak Current | Sleep Current |
|---|---|---|---|---|---|---|---|---|---|
| VCC3V3_SYS | RK809_BUCK1 | 2.5A | VDD_LOGIC | Slot:1 | 0.9V | ON | 0.9V | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK2 | 2.5A | VDD_GPU | Slot:2 | 0.9V | ON | DVFS | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK3 | 1.5A | VCC_DDR | Slot:3 | ADJ FB=0.8V | ON | 1.2V (DDR4) | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK4 | 1.5A | VDD_NPU | N/A | 0V | OFF | DVFS | TBD | TBD |
| VCC3V3_SYS | RK809_LDO1 | 0.4A | VDDA0V9_IMAGE | N/A | 0V | OFF | 0.9V | TBD | TBD |
| | RK809_LDO2 | 0.4A | VDDA_0V9 | Slot:1 | 0.9V | ON | 0.9V | TBD | TBD |
| | RK809_LDO3 | 0.1A | VDDA0V9_PMU | Slot:1 | 0.9V | ON | 0.9V | TBD | TBD |
| VCC3V3_SYS | RK809_LDO4 | 0.4A | VCCIO_ACODEC | N/A | 0V | OFF | 3.3V | TBD | TBD |
| | RK809_LDO5 | 0.4A | VCCIO_SD | Slot:4 | 3.3V | ON | 3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V) | TBD | TBD |
| | RK809_LDO6 | 0.4A | VCC3V3_PMU | Slot:2 | 3.3V | ON | 3.3V | TBD | TBD |
| VCC3V3_SYS | RK809_LDO7 | 0.4A | VCCA_1V8 | Slot:2 | 1.8V | ON | 1.8V | TBD | TBD |
| | RK809_LDO8 | 0.4A | VCCA1V8_PMU | Slot:2 | 1.8V | ON | 1.8V | TBD | TBD |
| | RK809_LDO9 | 0.4A | VCCA1V8_IMAGE | N/A | 0V | OFF | 1.8V | TBD | TBD |
| VCC3V3_SYS | RK809_SW2 100mohm | 2.1A | VCC3V3_SD | Slot:4 | 3.3V | ON | 3.3V | TBD | TBD |
| VCC3V3_SYS | RK809_SW1 90mohm | 2.1A | VCC_3V3 | Slot:4 | 3.3V | ON | 3.3V | TBD | TBD |
| | RK809_BUCK5 | 2.5A | VCC_1V8 | Slot:2 | 1.8V | ON | 1.8V | TBD | TBD |
| | RK809_RESETn | | | Slot:4+5 | | | | | |
| VCC12V_DCIN | EXT BUCK | 3.0A | VCC3V3_SYS | Slot:0 | 3.3V | ON | 3.3V | TBD | TBD |
| VCC12V_DCIN | EXT BUCK | 3.0A | VCC5V0_SYS | Slot:0 | 5.0V | ON | 5.0V | TBD | TBD |
| VCC5V0_SYS | EXT BUCK | 6.0A | VDD_CPU | Slot:2A | 1.025V | ON | DVFS | TBD | TBD |
| VCC3V3_SYS | EXT LDO | 0.3A | VCC2V5_DDR | Slot:2A | 2.5V | ON | 2.5V | TBD | TBD |
| | | | | | | | | | |

Figure 2-63 RK809-5 power-on sequence

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**2.2.3.5 Notices of RK809-5**

- Please select the load capacitance of 32.768KHz crystal according to the CL capacitance value of the crystal actually used. It is recommended to choose the capacitance not less than 18pF. If the load capacitance is too low, it may cause unstable start-up. The recommended value is 22pF.

---

Note

*In order to reduce the power consumption, the crystal oscillation of the PMIC RTC is relatively weak. Using an ordinary oscilloscope on the XOUT or XIN pins cannot detect the oscillation signal, or the oscilloscope probe will stop oscillation when it touches it. Please test the CLK32K pin for the 32.768k signal.*

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- VCC_RTC (Pin45) of RK809-5: It is the internal digital logic, part of analog control and RTC clock power supply pin of RK809 chip. The design of this pin requires that the power supply voltage must be the highest voltage among all the power supply pins of RK809-5 or be greater than Vmax-0.3V (except for VCC_SPK_HP power supply), so VCC_RTC must be powered on first, or powered on together with other power supplies. It is not allowed to supply other power sources before VCC_RTC.
  It is recommended to connect the same power supply with VCC9 (Pin54) of RK809-5;
- If you need button batteries to save the real-time clock, it is recommended to use an external RTC IC. The RTC current of RK809-5 is about 35~50μA, and when an external RTC IC is used as the real-time clock, and you need time alarm clock PowerOn function, please contact Rockchip to provide the reference circuit. The built-in RTC of RK809-5 supports time alarm clock PowerOn function. To use an external RTC IC, you must confirm whether its IO level matches the power supply voltage of the RTC chip;
- Pin 67 (RESETB) of RK809-5 needs a 100nF capacitor to improve the anti-interference ability and cannot be deleted at will.
- The SDA\SCL\INT\CLK32K\RESETB GPIOs of PMIC RK809-5 are open-drain output, and their highest allowable input voltage is the voltage of VCC_RTC, they need to add pull-up resistors externally or use the pull-up resistors inside RK3568 IO. SCL\SDA\SLEEP\PWRON\RESETB as input VL\VH are fixed to 0.4V\1.26V.
- If Gas Gauge is not used, it is recommended that Pin56 (BATDIV), Pin62 (SNSP), and Pin63 (SNSN) are grounded. If you want to enable it, please contact Rockchip to provide a reference circuit.
- I2S: The VCCIO of pin LRCK\BCLK\MCLK\SDI\PDMCLK are connected to LDO4, so LDO4 is generally allocated to the power domain where the I2S of the controller is located for power supply at the same time.
- The DC-DC inductor reference value of RK809-5 is: inductance 0.47μH, saturation current above 3.5A, DCR less than 50mΩ (in order to achieve better conversion efficiency, it is recommended to choose DCR less than 20mΩ).
- The input capacitance of BUCK1/BUCK2 of RK809-5 must be greater than 10μF, and the output capacitance must be greater than 30μF to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- The input capacitance of BUCK3 of RK809-5 must be greater than 10μF, and the output capacitance must be greater than 30μF to ensure a better decoupling effect. The output voltage value is determined by the

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external resistor, and the voltage value must be matched according to the DDR model used in the project. The reference voltage is 0.8V. Select the voltage-dividing resistor RH=(VBUCK3-0.8)*RL/0.8, RH and RL are the voltage-dividing pull-up resistor and pull-down resistor respectively, the resistor value is recommended to be between 10KΩ and 1MΩ, and the accuracy is 1%. It is recommended to refer to the parameters provided by the reference design.

- The input capacitance of BUCK4 of RK809-5 must be greater than 10μF, and the output capacitance must be greater than 30μF to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- The input capacitance of BUCK5 of RK809-5 must be greater than 10μF, and the output capacitance must be greater than 33μF to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- LDO power supply: VCC5\VCC6\VCC7 are the LDO power supply input pin, which support at least 2V input, but the output current will drop to 50% of the rated output when 2V is input.
- VCC9: is not only the power supply input pin of VSWOUT1 and BUCK5, but is also the chip under-voltage and over-voltage protection detection pin. If the voltage of VCC9 is lower than 3.0V after power-on, it will automatically shut down.
- RK809-5 power on and off conditions:

  VDC boot process:

  - VCC_RTC has powered and must be greater than 3.0V;
  - The value of VDC pin is higher than 0.55V, and the recommended value is about 1.2V;
  - EXT_EN outputs high level;
  - VCC9 needs to exceed 3.0V within 1.5ms of EXT_EN output high level, otherwise it will not turn on;
  - Start the power-on process, each DC/DC, LDO is powered on according to the sequence;
  - After starting up, VDC can be pulled down or kept at high level without affecting the starting state.

  Power Key boot process:

  - VCC_RTC has be powered and must be greater than 3.0V;
  - PWRON pin are pulled down by more than 500ms;
  - EXT_EN outputs high level;
  - VCC9 needs to exceed 3.0V within 1.5ms of EXT_EN output high level, otherwise it will not turn on;
  - Start the power-on process, each DC/DC, LDO is powered on according to the sequence.

  Alarm boot process:

  - VCC_RTC has be powered and must be greater than 3.0V;
  - Alarm timing time is up, and turn on the timing boot function;
  - EXT_EN outputs high level;
  - VCC9 needs to exceed 3.0V within 1.5ms of EXT_EN output high level, otherwise it will not turn on;
  - Start the power-on process, each DC/DC, LDO is powered on according to the sequence.

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Shut down:

- VCC9 voltage is lower than the under voltage design value;
- I2C command shutdown;
- Over temperature protection shutdown (145 degrees);
- Press and hold Power Key for more than six seconds to force shutdown.

#### 2.2.3.6 RK809-5 Design Description

Please refer to RK PMIC related design document "AN_RK809_V1.1" for detailed design instructions of RK809-5.

### 2.2.4 Discrete Power Supply Solution Introduction

#### 2.2.4.1 Power Tree of RK3568+Discrete Power（Based NVR_DEMO）

Mainly for products with low requirements of standby power.

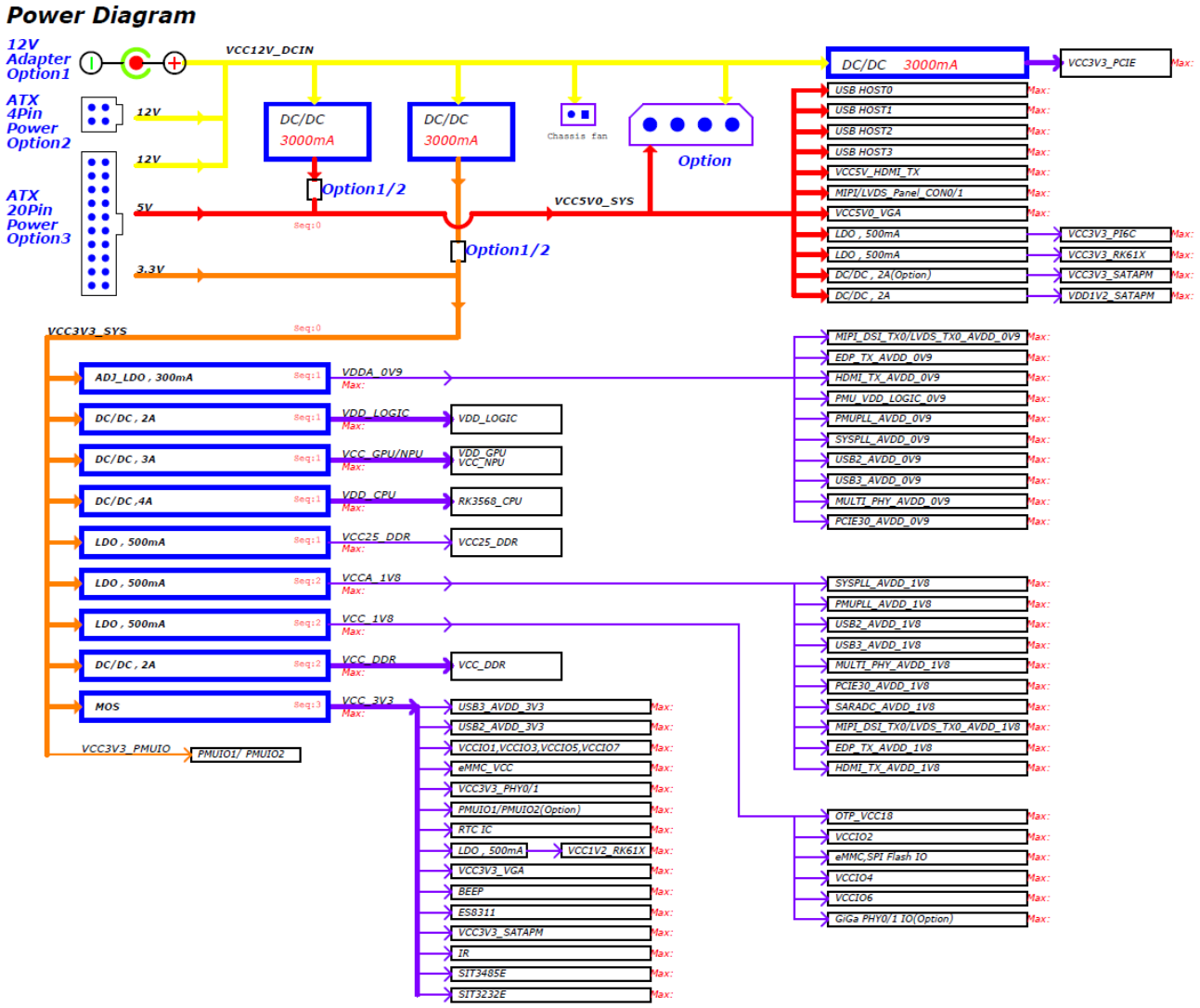


Figure 2-64 RK3568 + discrete power architecture

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### 2.2.4.2 Power-on and Power-off Sequence of Discrete Power

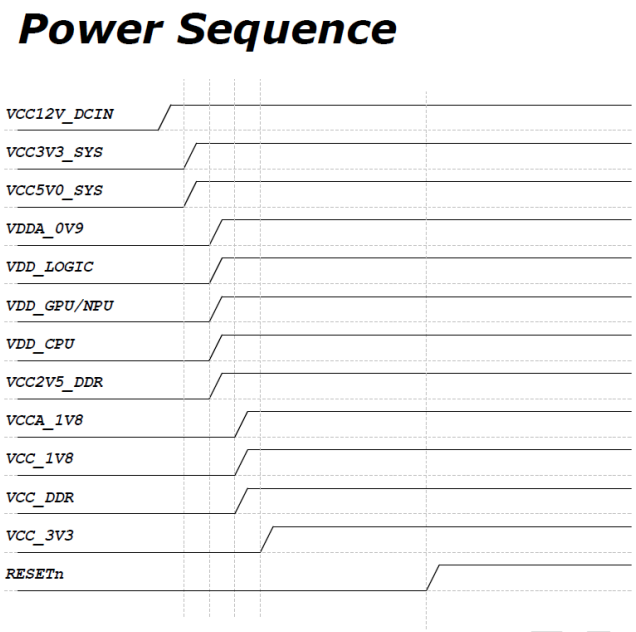


Figure 2-65 Discrete power power-on sequence

The power-on sequence of each power supply of RK3568 chip: in theory, follow the low-voltage first, high-voltage second, and after the last one voltage is stable, RESETn can be released after at least 10ms;

Power-off sequence: During power-off, RESETn must be pulled down first, and then each power supply can be powered off. If there is a product that needs to be powered on and off quickly, pay attention to the discharge time of the capacitor. If the power is not completely powered off and then powered on again, it may cause the system to work abnormally; In addition, if you use SPI Flash, it is recommended to use a reset IC with a threshold of 2.93V, when the power supply of the SPI Flash drops to 2.93V, the reset must be pulled low first to prevent the SPI Flash data error caused by the out-of-control and disoperation of the under-voltage logic during the power down process.

### 2.2.4.3 Notices of Discrete Power Supply

- VDD_CPU uses dynamic voltage and frequency regulation. It is not recommended to use together with other power supplies. Please refer to the reference design for BUCK model requirements, and using I2C voltage regulation. If you have to replace with other models, the BUCK with a power supply capacity of ≥4A can be selected. If it is not I2C voltage regulation, PWM can be used for voltage regulation. Please refer to the reference design for voltage regulation parameters, the voltage regulation range is 0.8-1.2V, and the default voltage is about 0.938V (note that the software configuration must be filled in according to actual values, otherwise, inaccurate voltage regulation will occur).

Other requirements of BUCK are as follows:

1）The output voltage accuracy is required to be ±1.5%;

2）BUCK transient response requirements: $I_{load}$=BUCK Max current*10%-BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±5%.

The input capacitance of BUCK must be greater than 22μF, and the output capacitor has to meet the requirement of VDD_CPU power supply with a total capacitance greater than 135μF (it is recommended to reserve one or two 22μF capacitors, which can be leave floating by default), to ensure that the power supply ripple is within

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80mV, then avoid large power supply ripples under heavy load conditions

- VDD_GPU and VDD_NPU adopt dynamic voltage and frequency regulation, they can be used together for power supply according to different cases, and for example, when it is not sensitive to working power consumption. Please refer to the reference design for selecting BUCK models. If you have to replace with other models, the power supply capacity of the BUCK should be ≥3A and use PWM for voltage regulation, please refer to the reference design for voltage regulation parameters, the voltage regulation range is 0.81-1.1V, and the default voltage is about 0.92V (note that the software configuration must be filled in according to the actual values, otherwise, inaccurate voltage regulation will occur).

  Other requirements of BUCK are as follows:

1）The output voltage accuracy is required to be ±1.5%;

2）BUCK transient response requirements: Iload=BUCK Max current*10%-BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±5%.

The input capacitance of BUCK must be greater than 10μF, and the output capacitor should meet the requirement of VDD_GPU and VDD_NPU power supply with a total capacitance greater than 135μF (it is recommended to reserve one or two 22μF capacitors, which cannot be attached by default), to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

- VDD_LOGIC defaults to a fixed voltage of about 0.92V, and it is reserved for dynamic voltage adjustment. It is not recommended to combine with other power supplies. The BUCK model requires refer to the reference design. If you need to replace other models, you need to select a BUCK with a power supply capacity of ≥1.5A, reserved PWM voltage regulation, the voltage regulation parameters can refer to the reference design, the voltage adjustment range is 0.81-1.0V, and the default voltage is about 0.92V (note that the software configuration must be filled in according to the actual, otherwise the voltage adjustment problem will be inaccurate).

Other requirements of BUCK are as follows:

1）The output voltage accuracy is required to be ±1.5%;

2）BUCK transient response requirements: Iload=BUCK Max current*10%-BUCK Max current*80% jump, slope 1A/μs, ripple requirement within ±5%.

The input capacitance of BUCK must be greater than 10μF, and the output capacitor needs to meet the requirement of VDD_LOGIC power supply with a total capacitance greater than 99μF (it is recommended to reserve 1-2 22μF capacitors, which can be hanged up by default), to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

- **VCC_3V3 power-on sequence must meet the requirements, and the MOS control circuit is not allowed to be deleted;**
- The reset IC must be an open-leakage output, which is active at low level. The power supply of the reset IC needs to be connected to VCC3V3_PMUIO, which is the same as the power supply of PMUIO1.

### 2.2.5 Standby Control Circuit

If the product requires low-power standby, it is recommended to use the RK809-5 power supply solution.

The following introduces the standby PMIC_SLEEP control circuit using RK809-5:

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When the RK3568 chip is in the normal working mode, the state pin PMIC_SLEEP of the chip will maintain a low level output.

When the system enters the standby mode, the PMIC_SLEEP pin will output a high-level sleep indicator signal. At this time, the PMIC is controlled by the signal to enter the standby state. According to the configuration of the software dts file, part of the power supplies will be turned off, and some of the power supplies will be lowered.

When the system is awakened from the standby mode, the PMIC_SLEEP pin will output a low level for the first time. At this time, the PMIC will resume the working state before standby and restore the power output of each channel.

PMIC_SLEEP is a special function signal, please do not change the usage at will.

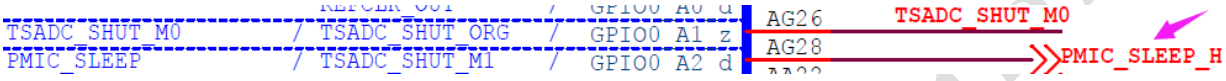


Figure 2-66 RK3568 PMIC_SLEEP output

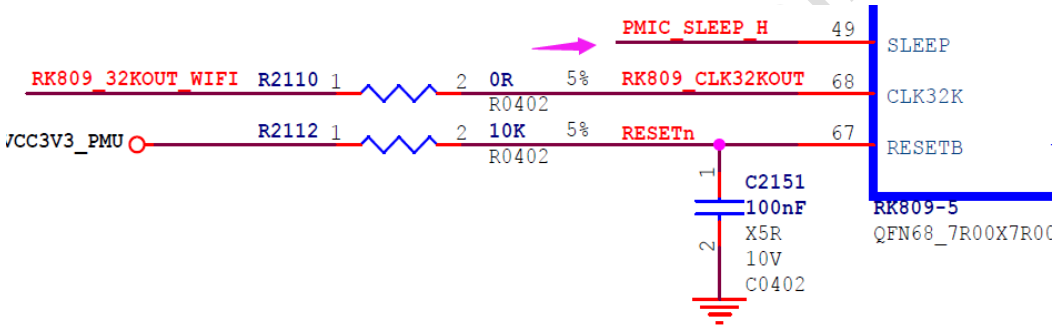


Figure 2-67 RK809-5 PMIC_SLEEP input

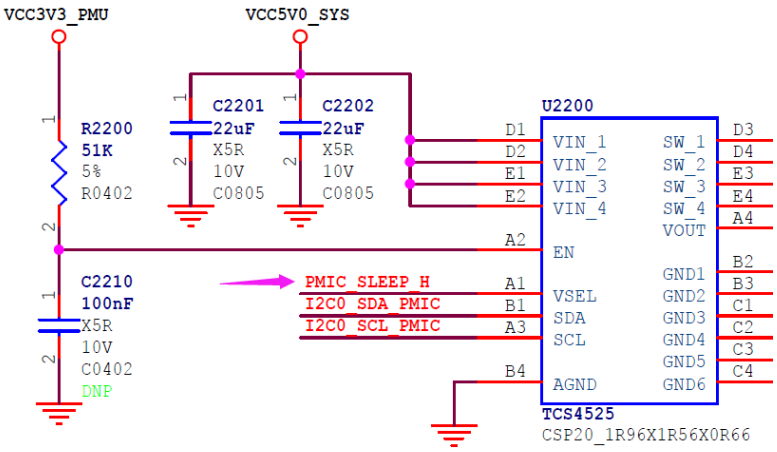


Figure 2-68 The PMIC_SLEEP input of VDD_CPU BUCK

## 2.2.6 Power Peak Current Table

The following data is the peak current of each module, they are used for evaluating power supply solution and PCB Layout, and they are used for reference only.

Note: It cannot be simply added up as the peak current of SOC. Please evaluate the heat dissipation solution according to the average current of the actual scenes.

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Table 2–14 RK3568 peak current table

| Power Name | Voltage（V） | Peak Current(mA) |
|---|---|---|
| PMUPLL_AVDD_0V9 | 0.9 | 10 |
| PMUPLL_AVDD_1V8 | 1.8 | 9 |
| SYSPLL_AVDD_0V9 | 0.9 | 30 |
| SYSPLL_AVDD_1V8 | 1.8 | 18 |
| PMU_VDD_LOGIC_0V9 | 0.9 | 50 |
| VDD_CPU | DVFS | 3000 |
| VDD_GPU | DVFS | 1200 |
| VDD_NPU | DVFS | 1000 |
| VDD_LOGIC | 0.9 | 1200 |
| DDRPHY_VDDQ | 1.1/1.2/1.35/1.5 | TBD |
| DDRPHY_VDDQL | 0.6/1.1/1.2/1.35/1.5 | TBD |
| USB3_AVDD_0V9 | 0.9 | 5 |
| USB3_AVDD_1V8 | 1.8 | 30 |
| USB3_AVDD_3V3 | 3.3 | 10 |
| USB2_AVDD_0V9 | 0.9 | 5 |
| USB2_AVDD_1V8 | 1.8 | 30 |
| USB2_AVDD_3V3 | 3.3 | 10 |
| MULTI_PHY_AVDD_0V9 | 0.9 | 150 |
| MULTI_PHY_AVDD_1V8 | 1.8 | 21 |
| PCIE30_AVDD_0V9 | 0.9 | 160 |
| PCIE30_AVDD_1V8 | 1.8 | 60 |
| MIPI_CSI_RX_AVDD_0V9 | 0.9 | 10 |
| MIPI_CSI_RX_AVDD_1V8 | 1.8 | 2.5 |
| MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 | 0.9 | 50 |
| MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 | 1.8 | 15 |
| MIPI_DSI_TX1_AVDD_0V9 | 0.9 | 50 |
| MIPI_DSI_TX1_AVDD_1V8 | 1.8 | 15 |
| eDP_TX_AVDD_0V9 | 0.9 | 150 |
| eDP_TX_AVDD_1V8 | 1.8 | 100 |
| HDMI_TX_AVDD_0V9 | 0.9 | 25 |
| HDMI_TX_AVDD_1V8 | 1.8 | 16 |
| SARADC_AVDD_1V8 | 1.8 | 1.5 |
| OTP_VCC18 | 1.8 | 59 |
| PMUIO0 | 1.8 | TBD |
| PMUIO1 | 3.3 | TBD |
| PMUIO2/VCCIO1/2/3/4/5/6/7/ | 1.8/3.3 | TBD |

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# 2.3 Functional Interface Circuit Design Guide

## 2.3.1 SDMMC0/1/2

The RK3568 integrates three SDMMC controllers, all of which support SD V3.01 and MMC V4.51 protocols. SDMMC0 and SDMMC1 support up to 200MHz, and SDMMC2 only support up to 150MHz.

### 2.3.1.1 SDMMC0 Interface

- SDMMC0 interface is multiplexed in the VCCIO3 power domain;
- Support System Boot, default allocation of SD card function;
- SDMMC0 is multiplexed with JTAG and other functions, functions selection is realized through the state of SDMMC0_DET by default. Please refer to the introduction in the section **2.1.5** for details;
- VCCIO3 power supply, need external 3.3V or 1.8V power supply,

When connecting an SD card: if it only supports SD2.0 mode: it can directly supply 3.3V power; If you want to support SD3.0 mode compatible with SD2.0 mode: default 3.3V power supply, after negotiating with SD card to run SD3.0 mode, the power supply voltage needs to be switched to 1.8V power supply, RK809-5 LDO5 supplies power to VCCIO3 alone, so this process can be achieved.

When connected a SDIO device: supply 1.8V or 3.3V according to the peripherals and the actual operating mode.

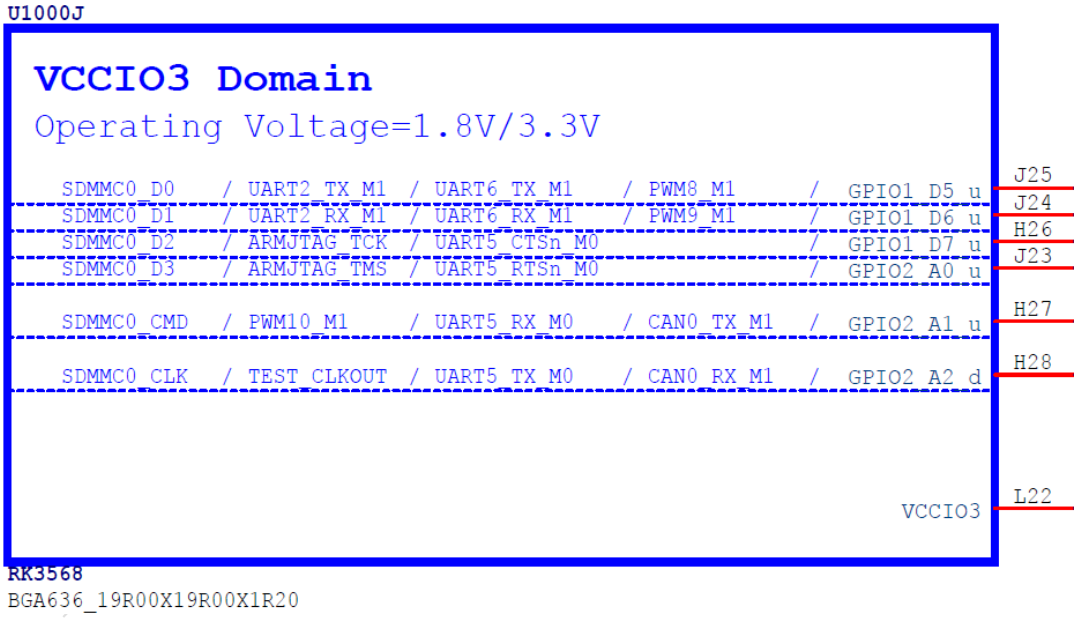


Figure 2-69 RK3568 SDMMC0 interface pin

- When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.
- When using SD card, pay attention to the following items:
  - The supply voltage of VDD pin of the SD card is 3.3V, and the decoupling capacitors are not allowed to be deleted. Place them close to the connector when layout.
  - SDMMC0_D [3:0], SDMMC0_CMD, SDMMC0_CLK need to be connected to a 22ohm resistor in

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series, and SDMMC0_DET to be connected to a 100ohm resistor in series;

- You have to add ESD device when SDMMC0_D [3:0], SDMMC0_CMD, SDMMC0_CLK, SDMMC0_DET signals are close the SD card position. If it requires to support SD3.0 mode, the junction capacitance of the ESD device must be less than 1pF. And if it only requires to support SD2.0 mode, the junction capacitance of the ESD device can be extended to 9pF.

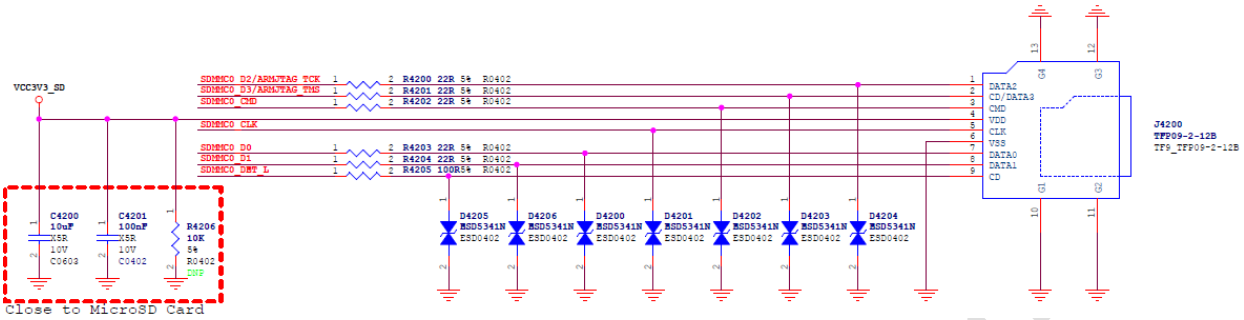


Figure 2-70 SD card interface circuit

- SDMMC0 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Table 2–15 SDMMC0 interface design

| Signal | Internal pull-up and pull-down | Connection mode | Description (chipset) |
|---|---|---|---|
| SDMMC0_D[3:0] | pull up | connect a 22ohm resistor in series, use the corresponding IO internal pull-up resistor | SD data send/receive |
| SDMMC0_CLK | pull down | connect a 22ohm resistor in series | SD clock send |
| SDMMC0_CMD | pull up | connect a 22ohm resistor in series, use the corresponding IO internal pull-up resistor | SD command send/receive |
| SDMMC0_DET | pull up | connect a 100ohm resistor in series, use the corresponding IO internal pull-up resistor | SD card insertion detection |

#### 2.3.1.2 SDMMC1 Interface

- SDMMC1 interface is multiplexed in the VCCIO4 power domain;
- Does not support System Boot, default allocate to SDIO WIFI function;
- VCCIO4 power supply, supplies 1.8V or 3.3V according to the peripheral and the actual operating mode, need to be consistent with the peripheral IO. For the SD card function, pay attention to the power domain voltage, the requirements same as SDMMC0;

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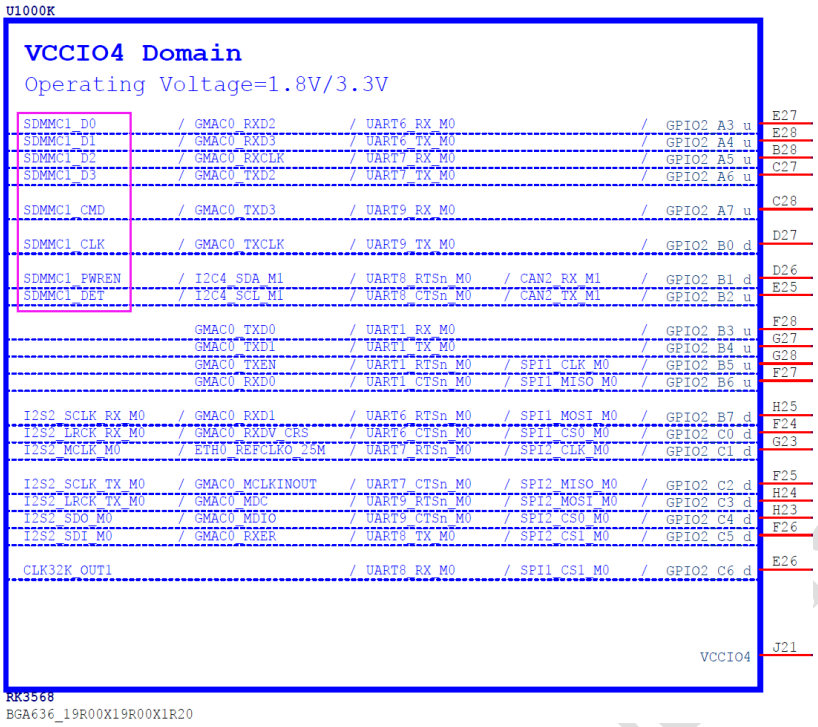


Figure 2-71 RK3568 SDMMC1 interface pin

- SDMMC1 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Table 2–16 SDMMC1 interface design

| Signal | Internal pull-up and pull-down | Connection mode | Description (chipset) |
|---|---|---|---|
| SDMMC1_D[3:0] | pull up | connect a 22ohm resistor in series which can be deleted when the trace is short;<br>use the corresponding IO internal pull-up resistor | SD data send/receive |
| SDMMC1_CLK | pull down | connect a 22ohm resistor in series | SD clock send |
| SDMMC1_CMD | pull up | connection a 22ohm resistor in series which can be deleted when the trace is short;<br>use the corresponding IO internal pull-up resistor | SD command send/receive |

- When connecting SDIO WIFI, you need to consider a low-power standby solution, that is, when using VDD_LOGIC standby and power-off solution, then the relevant control pins of SDIO WIFI need to be moved to the PMUIO1/2 power domain. After VDD_LOGIC is powered off, the IO status of VCCIO1/2/3/4/5/6/7 power domain cannot be maintained.
- When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.

### 2.3.1.3 SDMMC2 Interface

- The SDMMC2 interface is multiplexed in two power domains, one is in the VCCIO5 power domain and

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the other is in the VCCIO6 power domain. Only one of them can be used: either all using VCCIO5 power domain or all using VCCIO6 power domains; in other words, it is not supported that some using VCCIO5 power domain and the rest using VCCIO6 power domain;

- Does not support System Boot;
- Using VCCIO5 or VCCIO6 to supply 1.8V or 3.3V power according to the peripheral and the actual operating mode, and it should be consistent with the peripheral IO. For the SD card function, pay attention to the power domain voltage, please refer to SDMMC0 for detailed requirements;

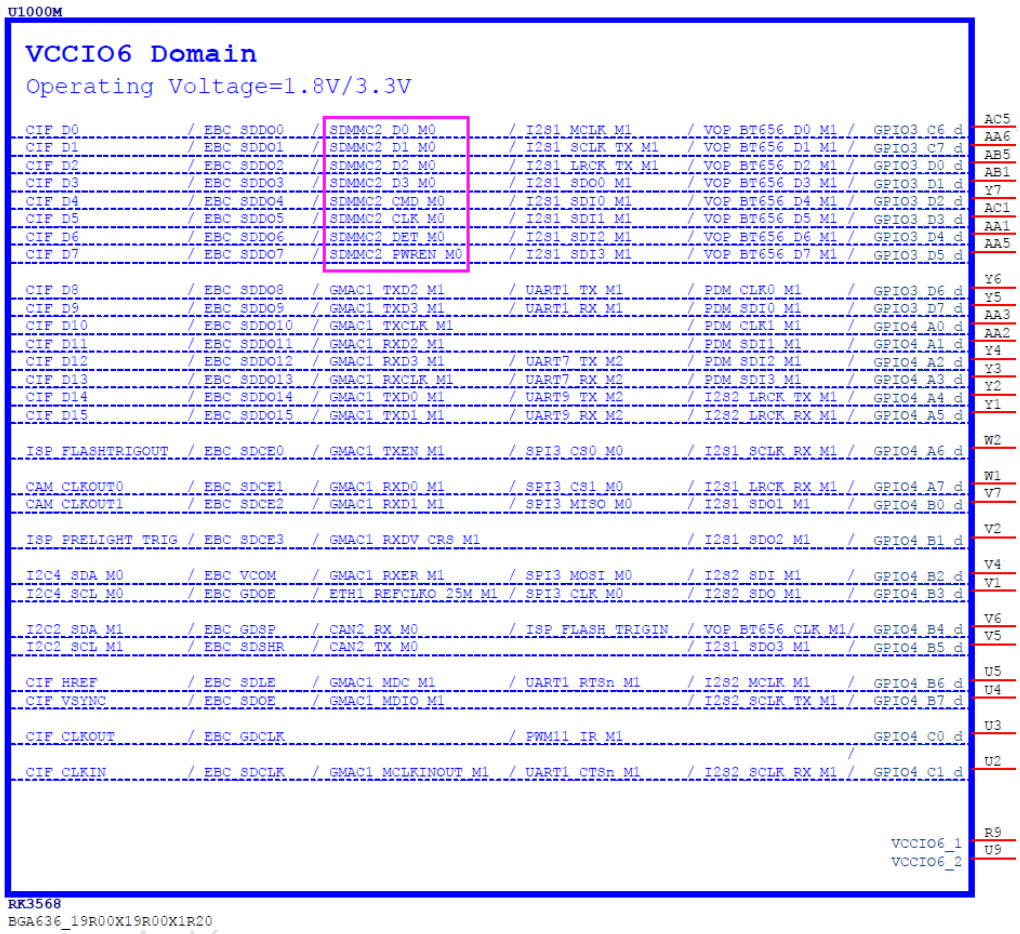


Figure 2-72 RK3568 SDMMC2 interface M0 functional pins

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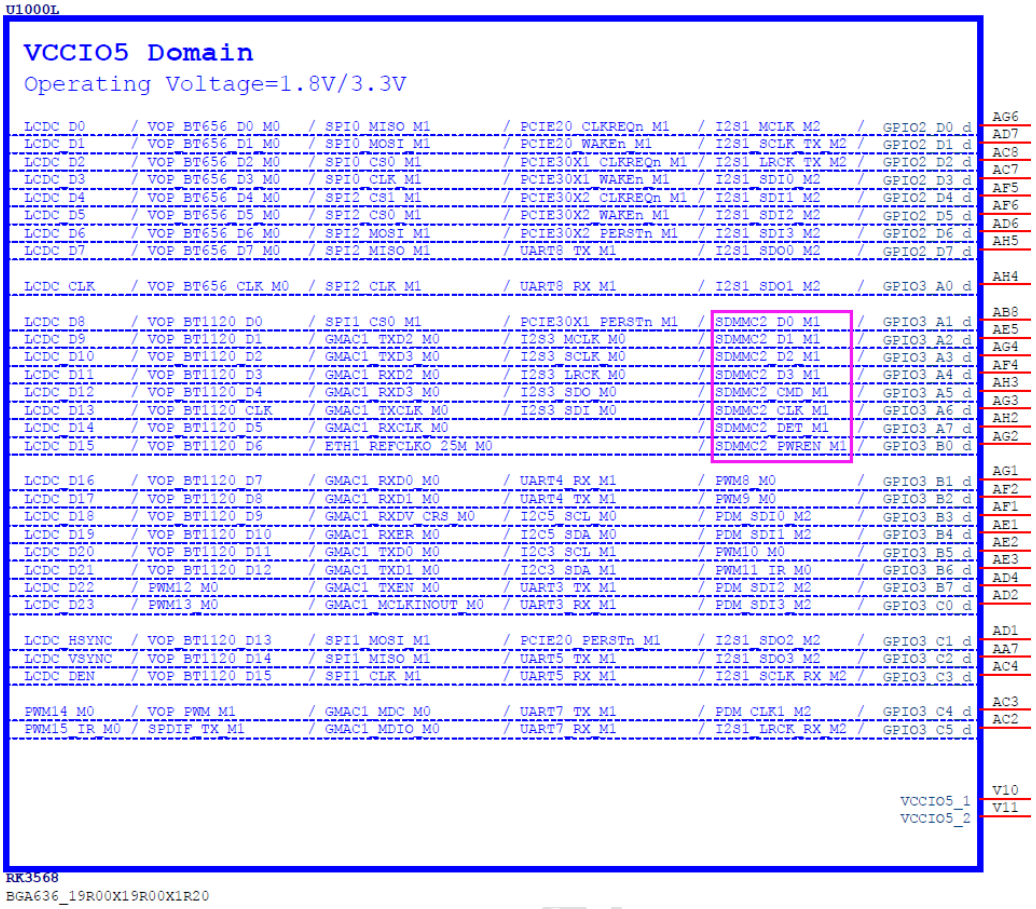


Figure 2-73 RK3568 SDMMC2 interface M1 functional pins

◆ SDMMC2 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Table 2–17 SDMMC2 interface design

| Signal | Internal pull-up and pull-down | Connection mode | Description (chipset) |
|---|---|---|---|
| SDMMC2_D[3:0] | pull up | connect a 22ohm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor | SD data send/receive |
| SDMMC2_CLK | pull down | connect a 22ohm resistor in series | SD clock send |
| SDMMC2_CMD | pull up | connect a 22ohm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor | SD command send/receive |

■ When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.

### 2.3.1.4 Notice of SDIO WIFI Interface

■ Please ensure that the IO level of the module is consistent with the IO level of CPU, otherwise, level

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matching processing is required.

- The crystal load capacitance should be selected according to the CL capacitance value of the crystal actually used, and the frequency tolerance at room temperature should be controlled within 10ppm.
- The antenna reserves a π-type circuit for antenna matching adjustment.
- Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD.
- If you use a module that requires 32.768k clock input, please pay attention to the clock amplitude.
- The schematic design is compatible with multiple modes. In the process of SMT, you must select according to the actual used module, and do not do SMT at will.

### 2.3.2 SARADC Circuit

- The RK3568 integrates a SARADC controller, which can provide 8 SARADC inputs.
- The SARADC_VIN0 of the RK3568 chip is used as the key value input sampling port by default, and is multiplexed as the Recovery mode button (cannot be modified). SARADC_VIN0 is pulled up to VCCA_1V8 through a 10Kohm pull-up resistor, and the default voltage is high voltage (1.8V). Under the premise that there is no key action and the system has burned the firmware, power on and directly enter the system; if the Recovery mode button has been pressed when the system is started, that is, SARADC_VIN0 is kept at low level (0V), RK3568 enters Loader flashing mode. When the PC recognizes the USB device, release the button to restore SARADC_VIN0 to high level (1.8V) for flashing firmware. Therefore, when a product without buttons, if SARADC_VIN0 is left hanged up, it will be unstable, which may affect booting. Therefore, the 10Kohm pull-up resistor of SARADC_VIN0 must be reserved and cannot be deleted to ensure the default normal booting judgment. In addition, for the convenience of development, it is recommended to reserve keys or test points.

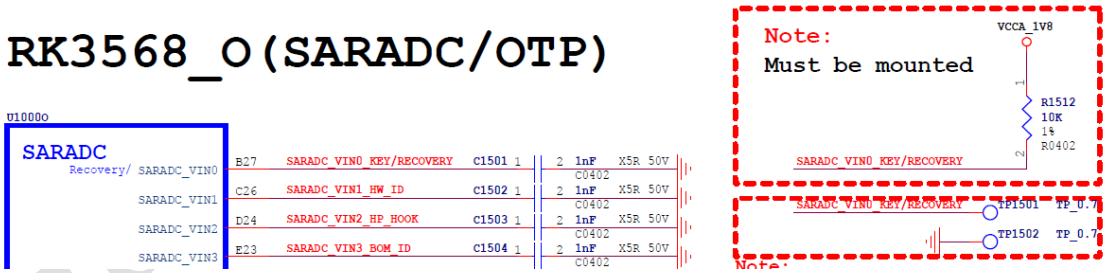


Figure 2-74 SARADC VIN0 interface

- On RK3568, the SARADC sampling range is 0-1.8V, with 10 bits sampling accuracy. The key array is in parallel, and the input key value can be adjusted by increasing or decreasing the keys and adjusting the ratio of the voltage-dividing resistance, so as to realize multi-key input to meet requirements of different customer products. In the process of design, it is recommended that the sampling value of any two keys must be greater than +/-35, that is, the center voltage difference must be greater than 123mV.

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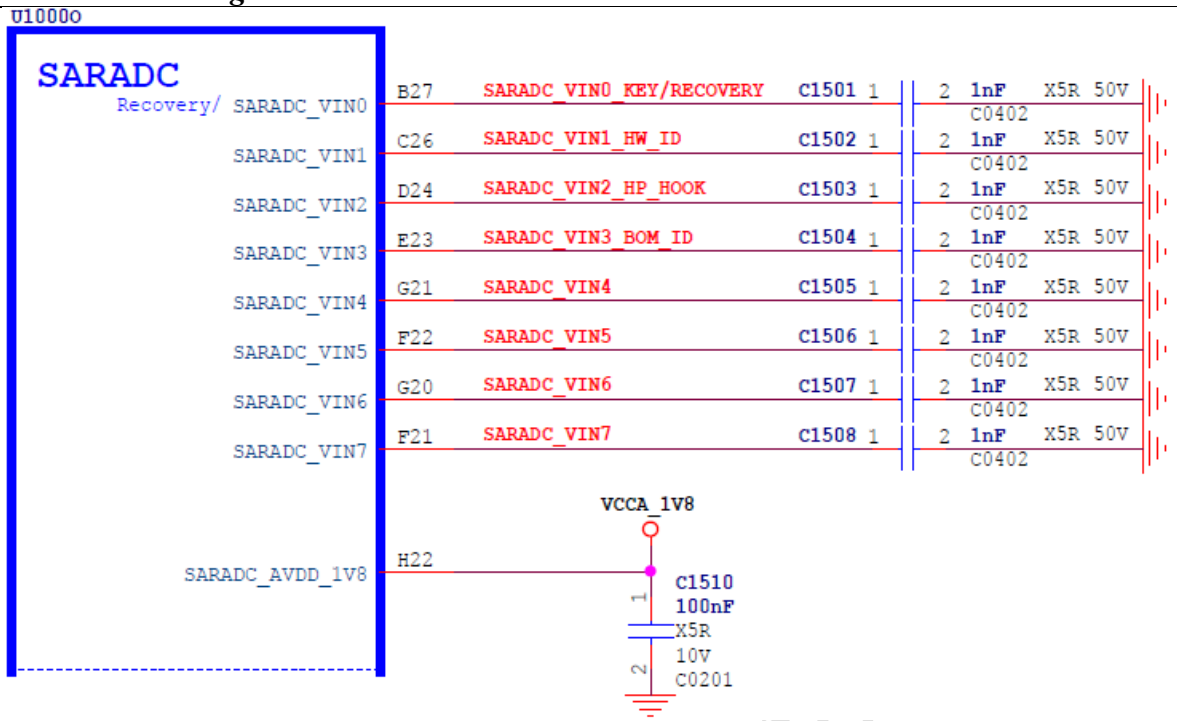


Figure 2-75 RK3568 SARADC module

- Pay attention to the following items in RK3568 SARADC design:
  - The decoupling capacitors of the SARADC_AVDD_1V8 power supply must not be deleted, and they should be placed close to the RK3568 pin during layout.
  - When SARADC_VIN [7:0] is used, a 1nF capacitor must be added close to the pin to eliminate jitter.
  - When it is used for button collection, ESD protection is required close to the button, and the button with 0 key value must be connected in series with a 100ohm resistor to strengthen the anti-static surge capability (if there is only one button, ESD components must be close to the button, first pass ESD components →100ohm resistor→1nF→ chip pin).

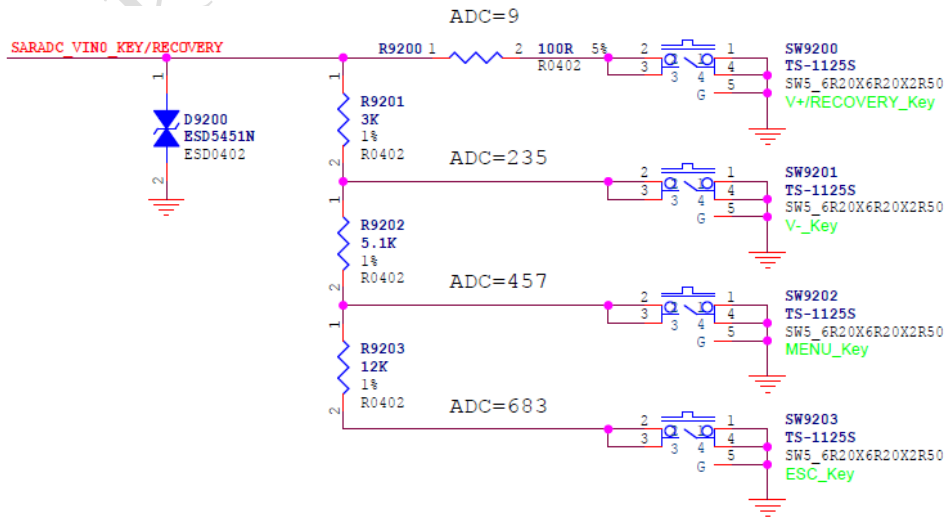


Figure 2-76 The button circuit using SARADC sampling

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### 2.3.3 OTP Circuit

- The RK3568 integrates an 8Kbit OTP, 7Kbit can be used for security applications.
- Support write, read and idle mode, in these modes, OTP_VCC18 pin must be powered.
- The decoupling capacitor of the OTP_VCC18 power supply must not be deleted. Place it close to the RK3568 pin during layout.

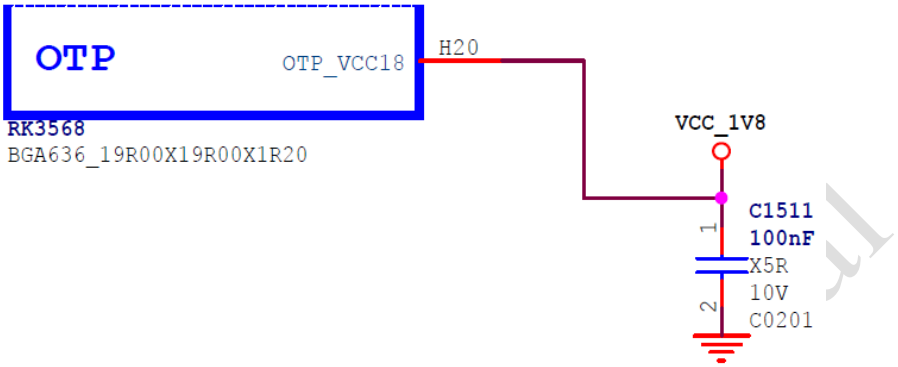


Figure 2-77 RK3568 OTP power pin

### 2.3.4 USB2.0/USB3.0 Circuit

There are one USB3.0 OTG controller, one USB3.0 HOST controller, and two USB2.0 HOST controllers in RK3568, see the pink and green boxes as below:

- The USB SS signal of the USB3.0 OTG controller uses MULTI_PHY0, and the USB LS/FS/HS signal uses USB2.0 OTG0 PHY.
- The USB SS signal of the USB3.0 HOST controller uses MULTI_PHY1, and the USB LS/FS/HS signal uses USB2.0 HOST1 PHY.
- Two USB2.0 HOST controllers use USB2.0 HOST2 PHY and USB2.0 HOST3 PHY respectively.

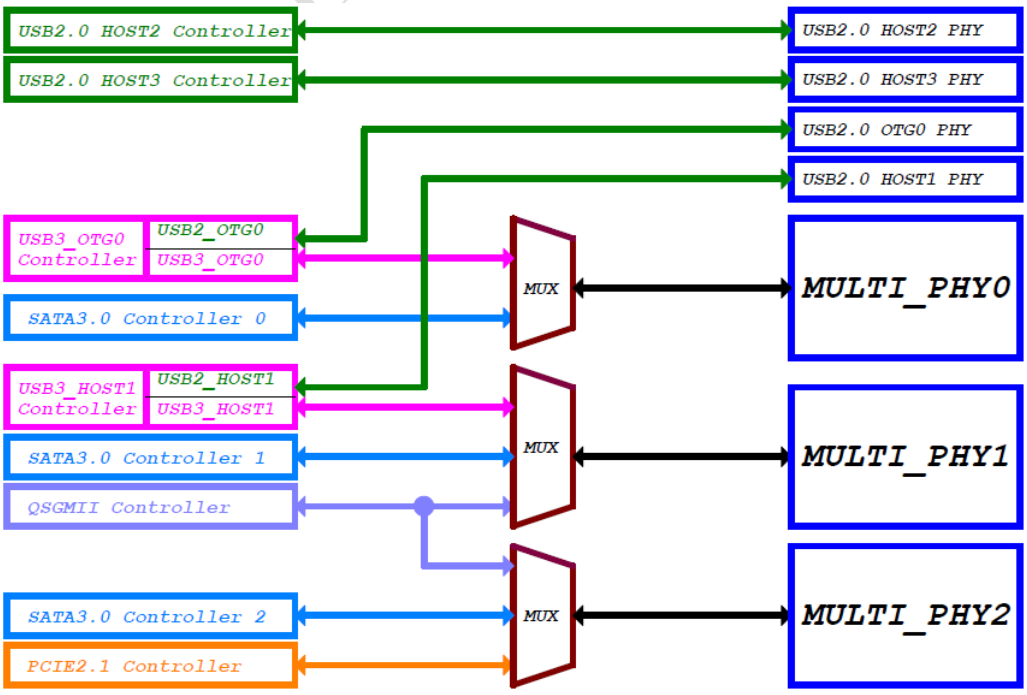


Figure 2-78 Multiplexing relationship between MULTI_PHY0/1and USB3.0 controllers

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- In the USB3.0 OTG0 controller, the USB LS/FS/HS mode signal uses USB2.0 OTG0 PHY, and the USB SS mode signal uses MULTI_PHY0 (multiplexed with the SATA0 controller). The signals in the box below form a complete USB3.0 OTG0 interface, other combinations are not supported;

  If you only need USB2.0 interface, just select the DP/DM signal, and MULTI_PHY0 can be configured as SATA0 function.

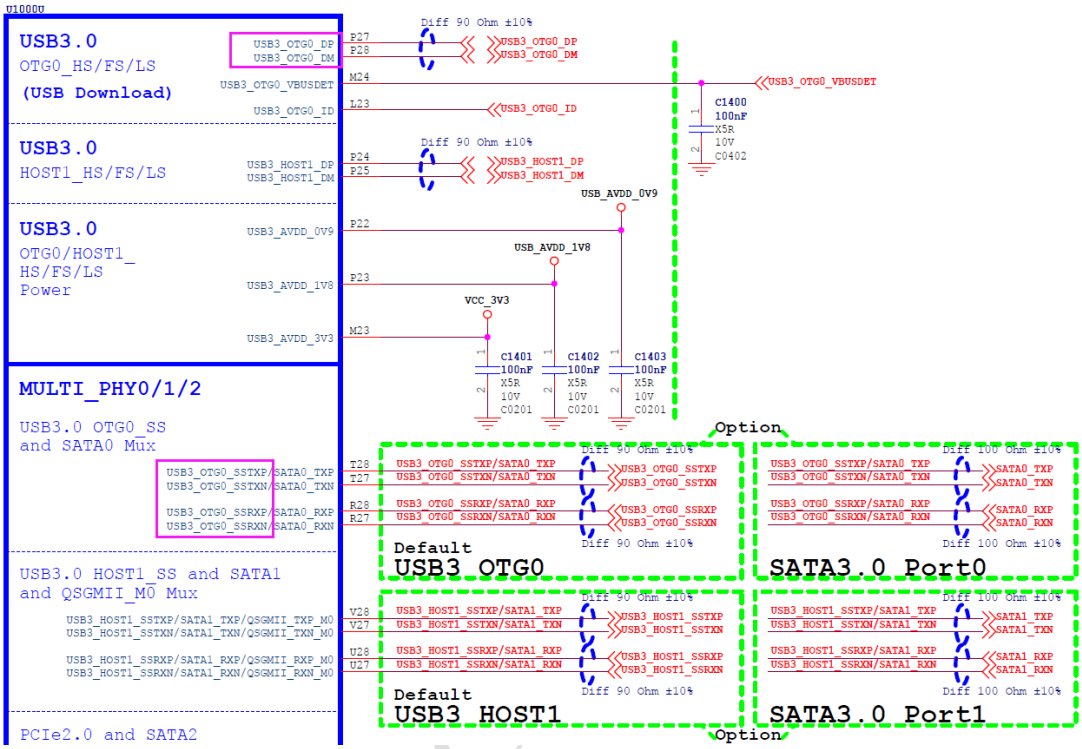


Figure 2-79 USB3.0 OTG0 pin

Note

*Only USB3_OTG0_DP and USB3_OTG0_DM support downloading firmware. If a product does not use this interface, it must be reserved during debugging and production process. Note: USB3_OTG0_VBUSDET must also be connected.*

- In the USB3.0 HOST1 controller, the USB LS/FS/HS mode signal uses USB2.0 HOST1 PHY, and the USB SS mode signal uses MULTI_PHY1 (multiplexed with the SATA1 controller and the QSGMII controller). The signals in the box below form a complete USB3.0 HOST1 interface, other combinations are not supported;

  If you only need USB2.0 interface, just select the DP/DM signal, and MULTI_PHY1 can be configured as SATA1 or QSGMII function.

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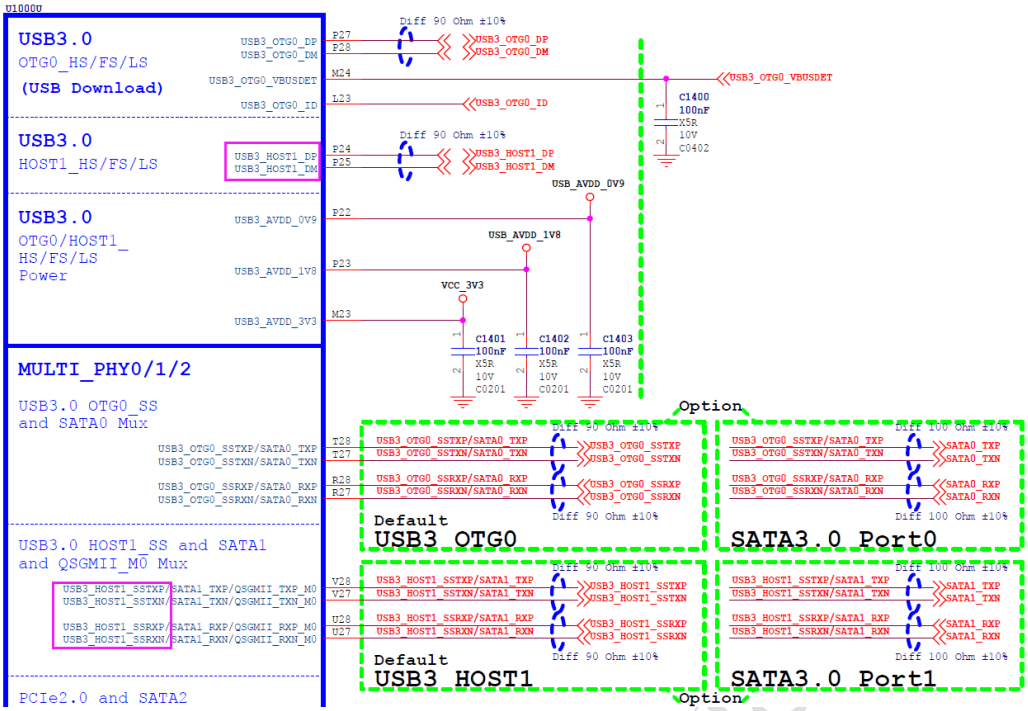


Figure 2-80 USB3.0 HOST1 pin

- The USB2.0 HOST2 controller uses USB2.0 HOST2 PHY, the signals in the box below form the USB2.0 HOST2 interface.

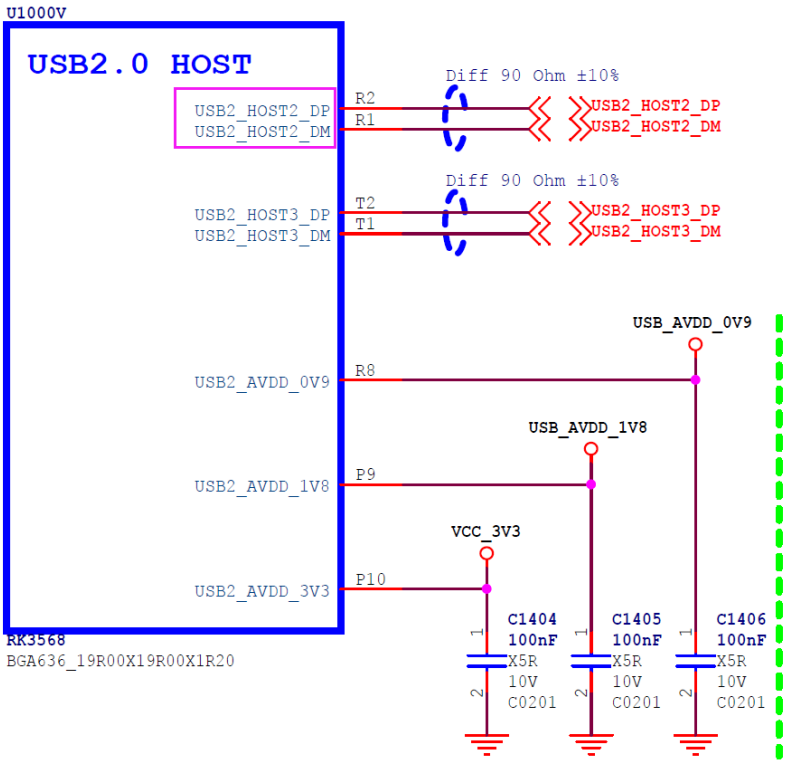


Figure 2-81 USB2.0 HOST2 pin

- The USB2.0 HOST3 controller uses USB2.0 HOST3 PHY, the signals in the box below form the USB2.0 HOST3 interface.

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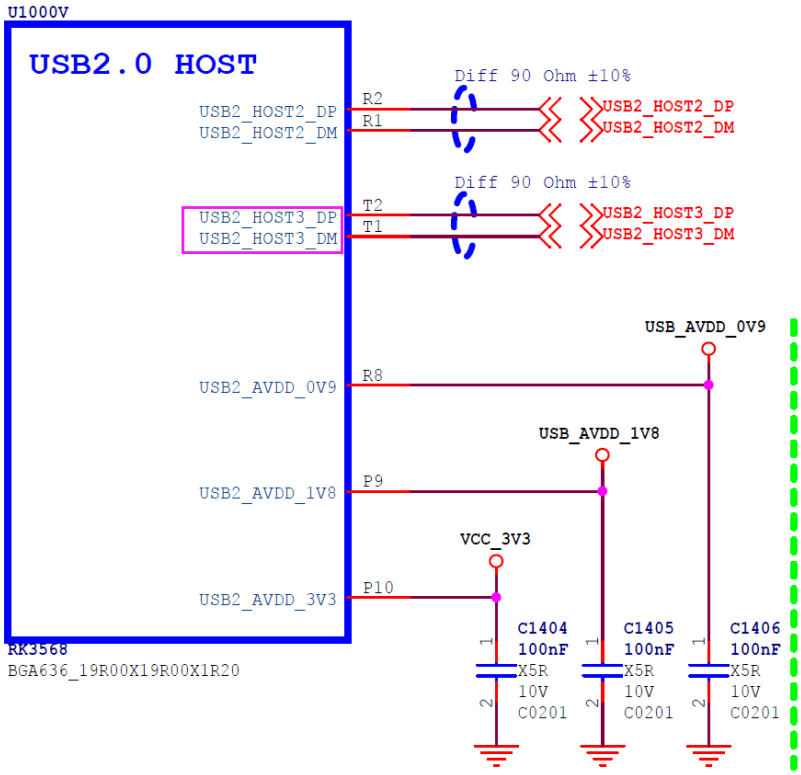


Figure 2-82 USB2.0 HOST3 pin

- Pay attention to the following items in USB2.0/USB3.0 design:
  - Only USB3_OTG0_DP/USB3_OTG0_DM is the system firmware flashing port. If a product does not use this port, this port must be reserved during the debugging and production process, otherwise, firmware flashing is disabled during debugging and production process.
  - There is an internal about 200Kohm resistor in USB3_OTG0_ID to pull up to USB3_AVDD_1V8;
  - USB3_OTG0_VBUSDET is the OTG and Device mode detection pin, high effective, 2.7-3.3V, TYP: 3.0V, it is recommended to place a 100nF capacitor on the pin.

OTG mode can be set to the following three modes:

◆ OTG mode: it can switch to device mode or HOST mode according to the status of the ID pin automatically. When ID pin is pulled high, it is device mode, and when ID pin is pulled low, it is HOST mode. When in device mode, it will also judge whether the VBUSDET pin is high. If it is high, DP will be pulled up and enumeration will start.

◆ Device mode: When set to this mode, ID pin is not needed, just judge whether the VBUSDET pin is high, if it is high, DP will be pulled up and enumeration will start.

◆ HOST mode: When set to this mode, there is no need to care about ID and VBUSDET status. (If the product only needs HOST mode, but only USB3_OTG0_DP/USB3_OTG0_DM is the system firmware flashing port, and this port is needed during debugging and production. So when flashing and adb debugging, it needs to be set to device mode, the USB3_OTG0_VBUSDET signal must also be connected).

◆ Before uboot is up, it is device mode by default. After entering uboot, you can configure these three modes according to actual needs.

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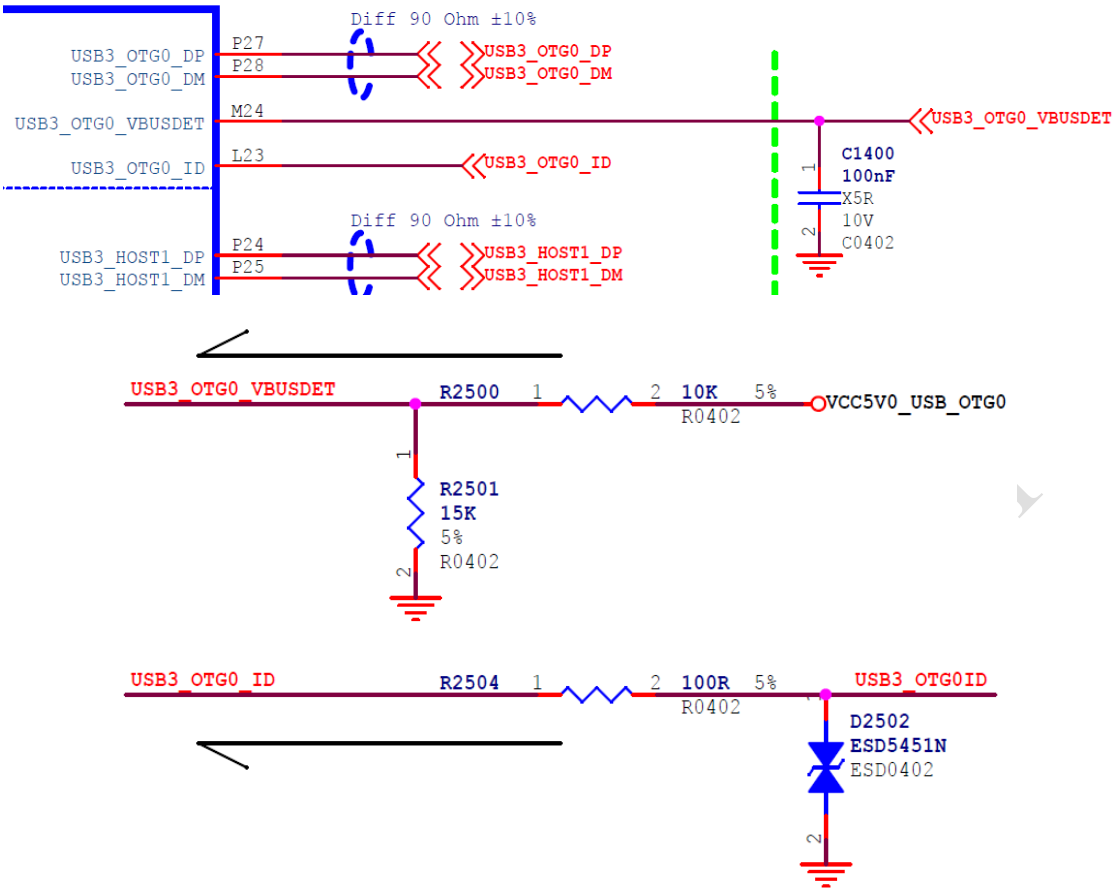


Figure 2-83 RK3568 VBUSDET and ID Circuit

- USB3_AVDD_0V9, USB2_AVDD_0V9, USB3_AVDD_1V8, USB2_AVDD_1V8 power pins and VDDA_0V9, VCCA_1V8 are required to be isolated by magnetic beads, please refer to the reference diagram/ schematic design for the details;

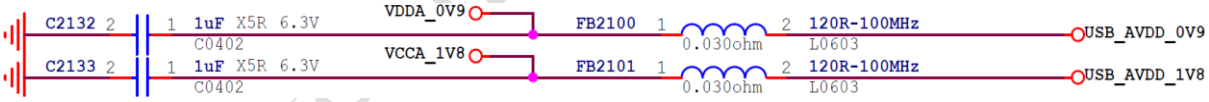


Figure 2-84 USB2.0 PHY power supply magnetic bead isolation circuit

- In order to improve the USB performance, the decoupling capacitors of each power supply of the PHY must not be deleted. Please place them close to the pins during layout;
- In order to strengthen the anti-static and surge capability, ESD devices must be reserved on signal. The ESD parasitic capacitance of the USB2.0 signal cannot exceed 3pF. In addition, the DP/DM of the USB2.0 signal is connected in series with a 2.2ohm resistor to strengthen the anti-static surge capability, it cannot be deleted. The following figure is an example of USB2_HOST2_DP/DM, other USB2.0 interfaces also need to be processed in the same way;

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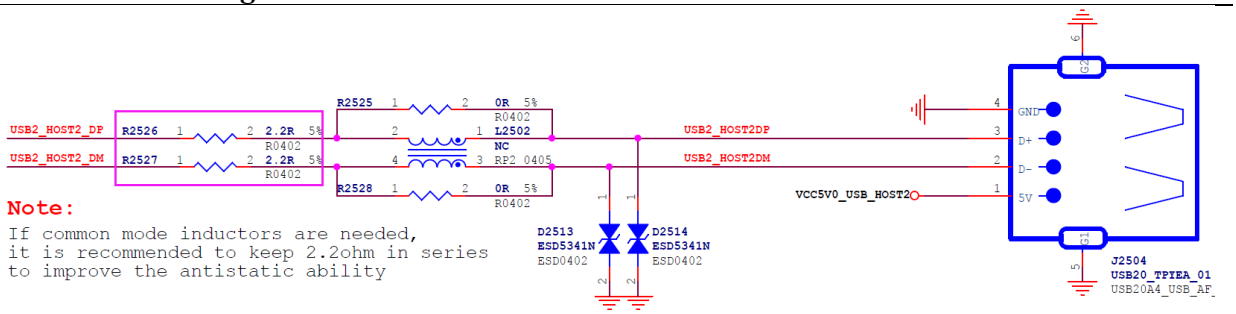


Figure 2-85 USB2.0 signal is connected in series with a 2.2ohm resistor

- In order to suppress electromagnetic radiation, you can consider to reserve a common mode choke on the signal line. In the debugging process, you can choose to use a resistor or a common mode choke according to the actual situation. The diagram below is an example of USB2_HOST2_DP/DM, other USB2.0 interfaces also need to be processed in the same way;

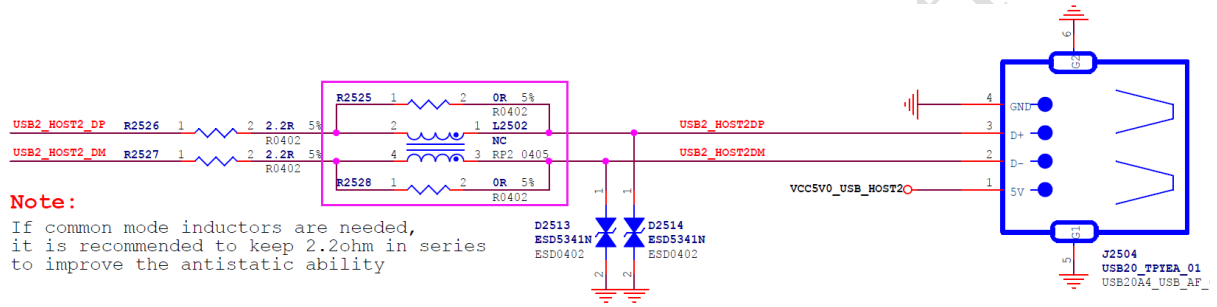


Figure 2-86 USB2.0 signal is connected in series with common mode choke circuit

- If the USB3_OTG0_ID signal is used, in order to strengthen the anti-static and surge capability, ESD devices must be reserved on the signal, and a 100ohm resistor must be connected in series, which cannot be deleted. See the following diagram:


Figure 2-87 USB OTG ID pin circuit

- For the HOST function, it is recommended to add a current-limiting switch for the 5V power supply. The current-limiting size can be adjusted according to application needs. The current-limiting switch is controlled by GPIO, it is recommended to add more than 100μF and 100nF capacitor for the 5V power supply.

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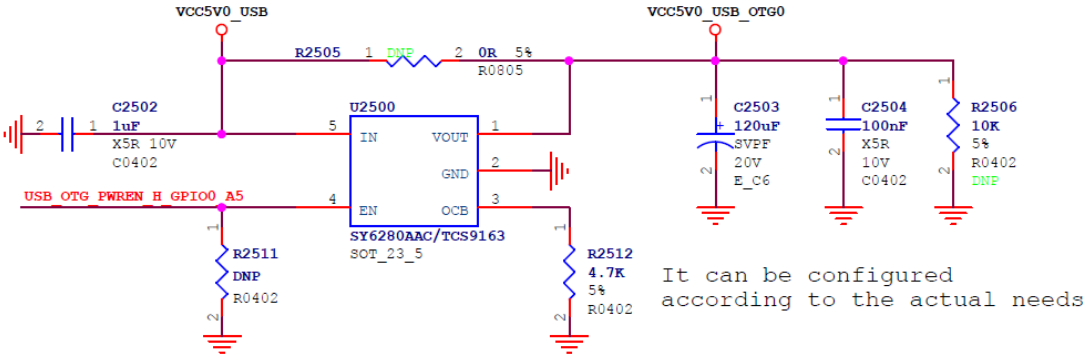


Figure 2-88 USB 5V current-limiting circuit

- It requires to add a 100nF AC coupling capacitor to the SSTXP/N line in the USB 3.0 protocol. The AC coupling capacitor is recommended to use 0201 package for lower ESR and ESL and fewer impedance changes on the line.
- All signals of the USB3 connector must be added with ESD devices which should be placed close to the USB connector. For SSTXP/N, SSRXP/N signals, the ESD parasitic capacitance must not exceed 0.4pF.

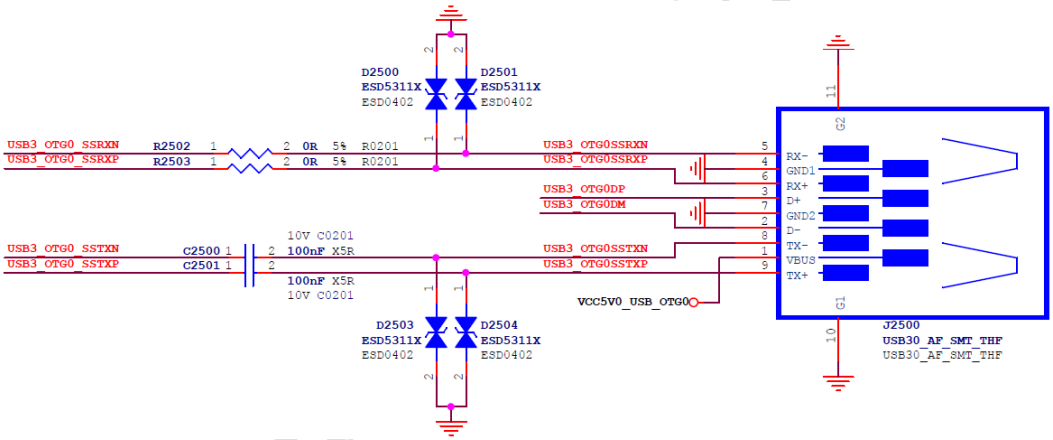


Figure 2-89 USB3.0 ESD circuit

- MULTI_PHY_AVDD_0V9/1V8 power supply pins should be placed 4.7μF and 100nF decoupling capacitors, which must not be deleted. Place them close to the RK3568 pin during layout.

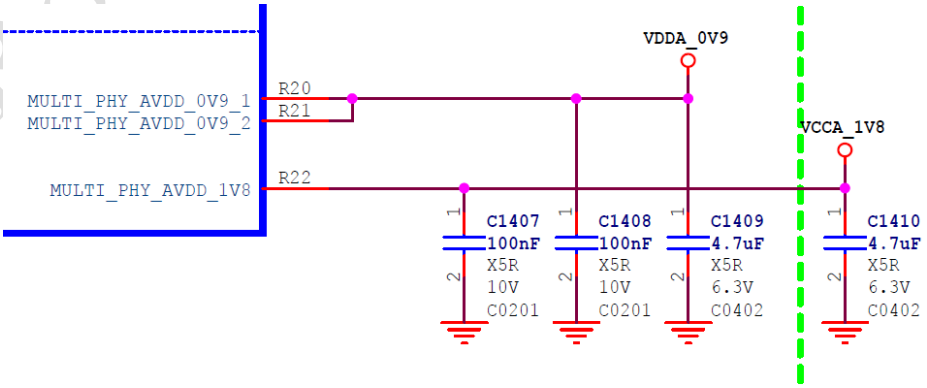


Figure 2-90 MULTI PHY power supply decoupling circuit

- USB2.0/USB3.0 interface matching design recommendations are shown in the following Table.

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Table 2–18 RK3568 USB2.0/USB3.0 interface design

| Signal | Connection mode | Description |
|---|---|---|
| USB3_OTG0_DP/DM | Connect 2.2ohm resistor in series | data input and output in USB HS/FS/LS mode |
| USB3_OTG0_SSTXP/SSTXN | Connect a 100nF capacitor in series (0201 package is recommended) | data output in USB SS mode |
| USB3_OTG0_SSRXP/SSRXN | Connect 0ohm resistor in series | data input in USB SS mode |
| USB3_OTG0_ID | Connect a 100ohm resistor in series (to strengthen the external power supply, the power supply needs to be connected to the same power supply as USB3_AVDD_1V8) | USB OTG ID recognition, required for Micro-USB interface |
| USB3_OTG0_VBUSDET | Resistance voltage-dividing detection | USB OTG insertion detection |
| USB3_HOST1_DP/DM | Connect 2.2ohm resistor in series | data input and output in USB HS/FS/LS mode |
| USB3_HOST1_SSTXP/SSTXN | Connect a 100nF capacitor in series (0201 package is recommended) | data output in USB SS mode |
| USB3_HOST1_SSRXP/SSRXN | Connect 0ohm resistor in series | data input in USB SS mode |
| USB3_HOST2_DP/DM | Connect 2.2ohm resistor in series | data input and output in USB HS/FS/LS mode |
| USB3_HOST3_DP/DM | Connect 2.2ohm resistor in series | data input and output in USB HS/FS/LS mode |

### 2.3.5 SATA3.0 Circuit

There are three SATA3.0 controllers in RK3568, see the blue box below, using MULTI_PHY0/1/2 respectively.

- Support SATA PM function, each port can support 5 devices.
- Support SATA 1.5Gb/s, SATA 3.0Gb/s, SATA 6.0Gb/s speeds.
- Support eSATA.

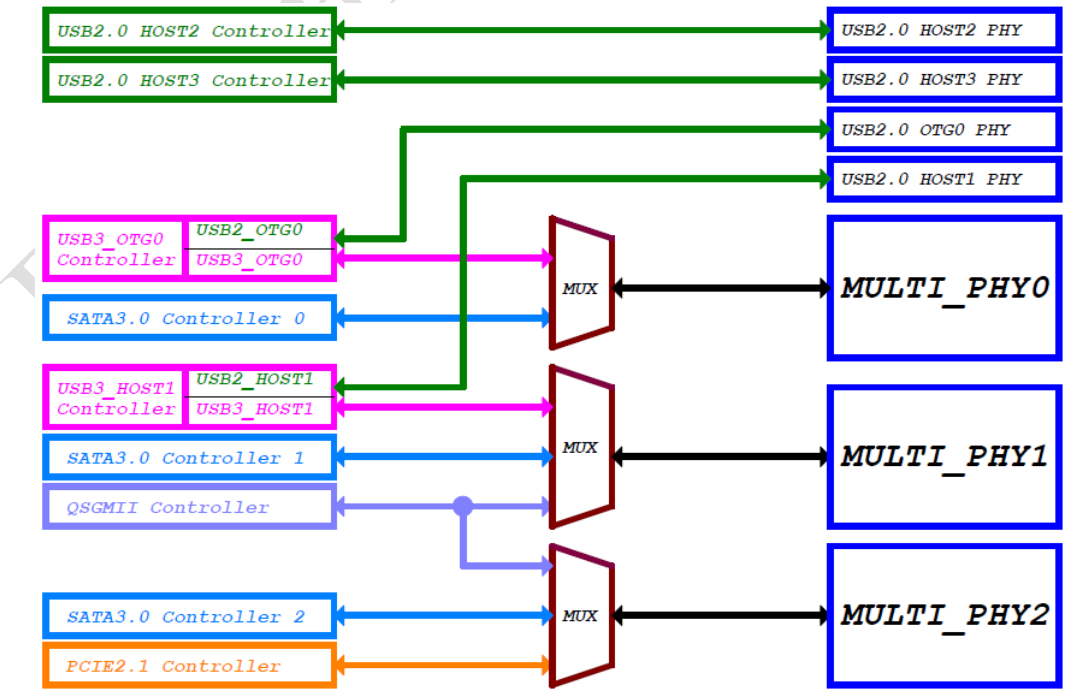


Figure 2-91 MULTI_PHY0/1/2 and SATA3.0 controller multiplexing relationship

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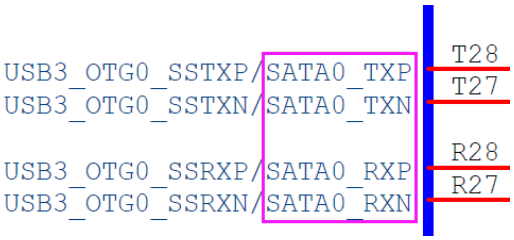
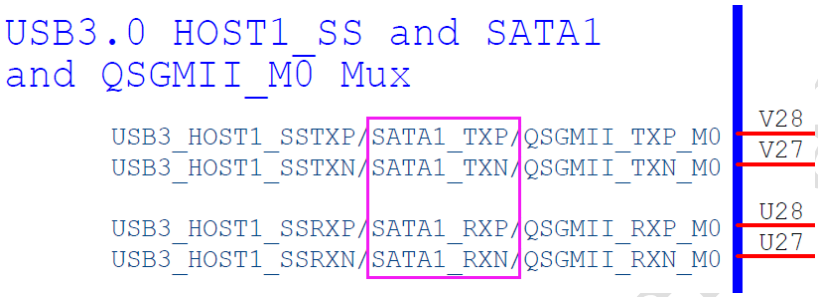
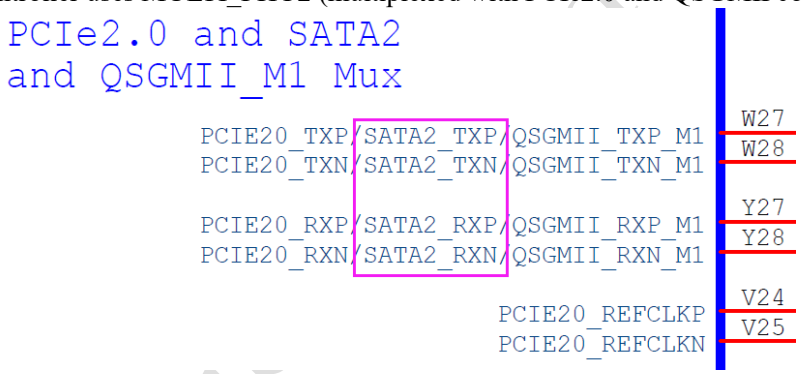
- The SATA0 controller uses MULTI_PHY0 (multiplexed with USB3.0 OTG0 controller).




- The SATA1 controller uses MULTI_PHY1 (multiplexed with USB3.0 HOST1 and QSGMII controller).




- The SATA2 controller uses MULTI_PHY2 (multiplexed with PCIe2.0 and QSGMII controller).




- The related control IOs of SATA0/1/2 controller:

  SATA0_ACT_LED: LED blinking control output when SATA0 interface has data transmission;

  SATA1_ACT_LED: LED blinking control output when SATA1 interface has data transmission;

  SATA2_ACT_LED: LED blinking control output when SATA2 interface has data transmission;

  SATA_CP_DET: Plug in and out detection input of SATA hot-plug device

  SATA_MP_SWITCH: Switch detection input of SATA hot-plug device

  SATA_CP_POD: Power switch output of SATA hot-plug device

  SATA_CP_DET, SATA_MP_SWITCH, SATA_CP_POD are multiplexed with SATA0/1/2 interfaces, which can be configured by register to be SATA0, SATA1 or SATA2.

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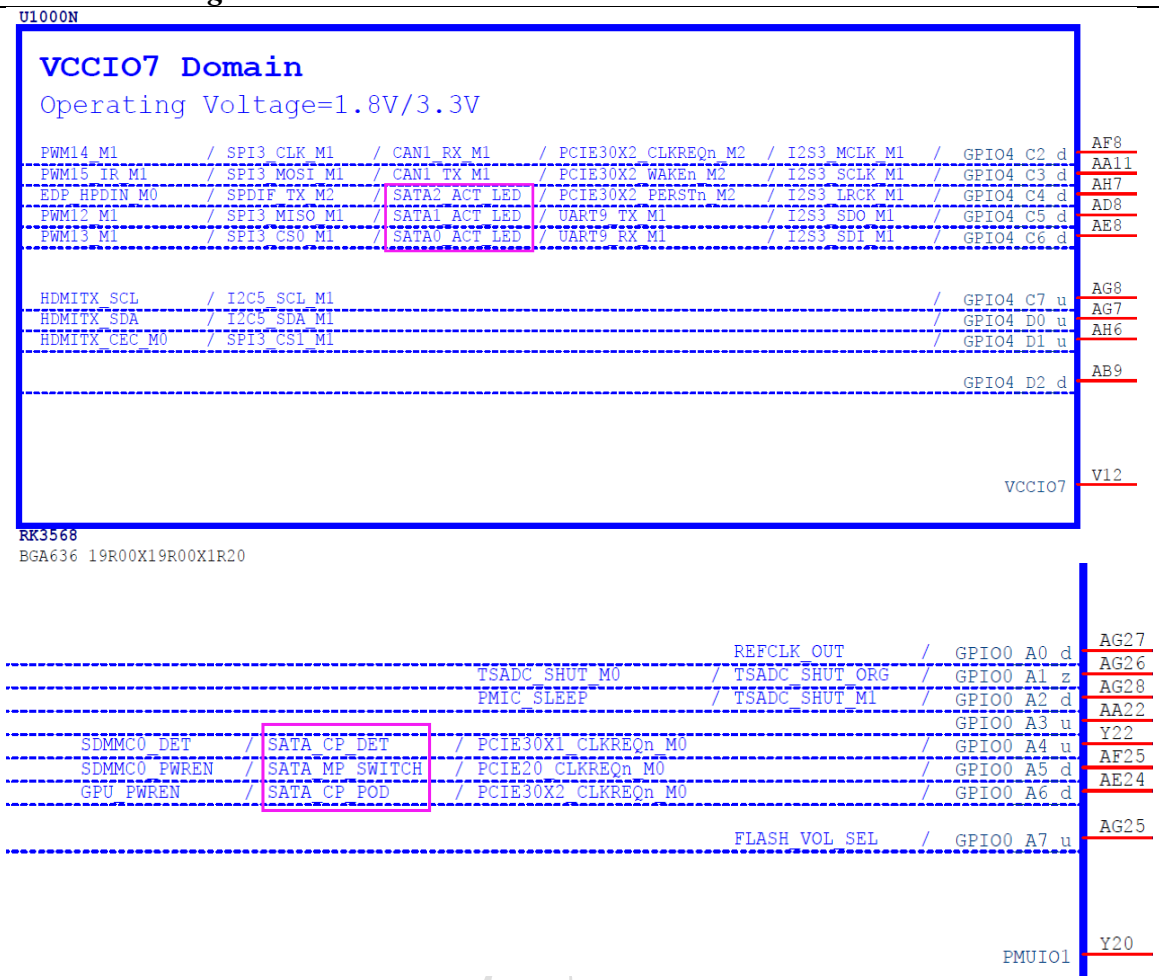
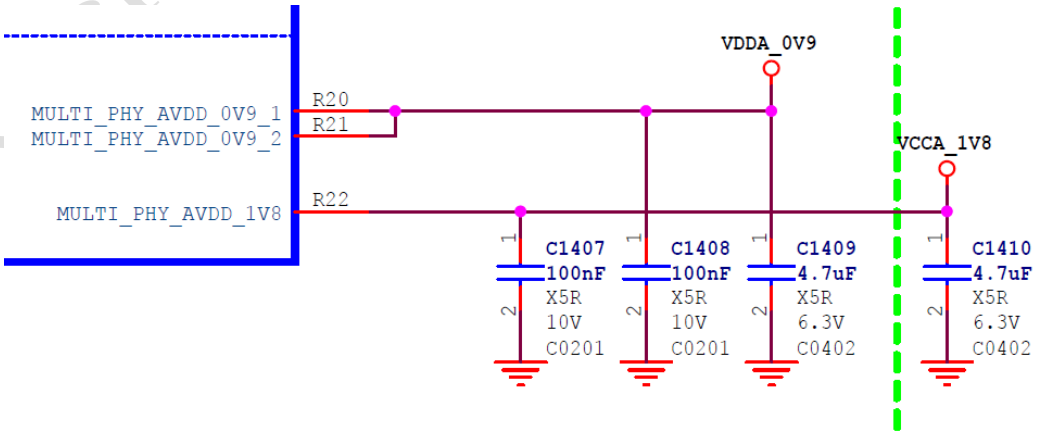



Figure 2-92 SATA0/1/2 related control IO pins

- Pay attention to the following items in SATA design:
  - When designing the slot, the peripheral circuit and power supply should meet the requirements of Spec.
  - MULTI_PHY_AVDD_0V9/1V8 power supply pins should add 4.7μF and 100nF decoupling capacitors, which must not be deleted. Place them close to the RK3568 pin during layout.




  - 10nF AC coupling capacitors connected in series on the TXP/N, RXP/N differential signals of SATA interface. The AC coupling capacitor is recommended to use 0201 package for lower ESR and ESL and fewer impedance changes on the line.
  - ESD devices must be added to all signals of the eSATA interface connector, Place them close to the

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connector during layout. The ESD parasitic capacitance cannot exceed 0.4pF.

- SATA interface matching design recommendations are shown in the following Table.

Table 2–19 RK3568 SATA interface design

| Signal | Connection mode | Description |
|---|---|---|
| SATA0_TXP/TXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data output |
| SATA0_RXP/RXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data input |
| SATA1_TXP/TXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data output |
| SATA1_RXP/RXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data input |
| SATA2_TXP/TXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data output |
| SATA2_RXP/RXN | Connect a 10nF capacitor in series (0201 package is recommended) | SATA data input |

### 2.3.6 QSGMII/SGMII Circuit

There is one QSGMII or SGMII interface in RK3568.

- SGMII (Serial Gigabit Media Independent Interface) converts the RGMII or RMII interface between gigabit MAC and gigabit PHY into a serial interface. Using a SGMII interface is to reduce the number of pins required for the RGMII interface, and the rate of SGMII interface is 1.25Gbps.
- QSGMII (Quad Serial Gigabit Media Independent Interface) is an extension of SGMII. QSGMII interface transfers data between a 4-port gigabit MAC and a 4-port gigabit PHY via a serial line running at a 5Gbps rate. Each Port can run at a 10/100/1000Mbps rate, but RK3568 has only two gigabit MACs inside, that is to say, it can only support 2 Port 10/100/1000Mbps interface via the QSGMII interface.
- QSGMII interface of RK3568 is compatible with SGMII.
- GMAC0/GMAC1 controller used by QSGMII/SGMII and RGMII/RMII interface from MUX to IO are multiplexed.

- QSGMII/SGMII PCS interface is multiplexed to two PHY interfaces: MULTI_PHY1 and MULTI_PHY2, but only one of the PHY interfaces can be used.

  The paths of GMAC0, GMAC1, QSGMII/SGMII PCS and QSGMII/SGMII PHY are shown in the following diagram with green lines.

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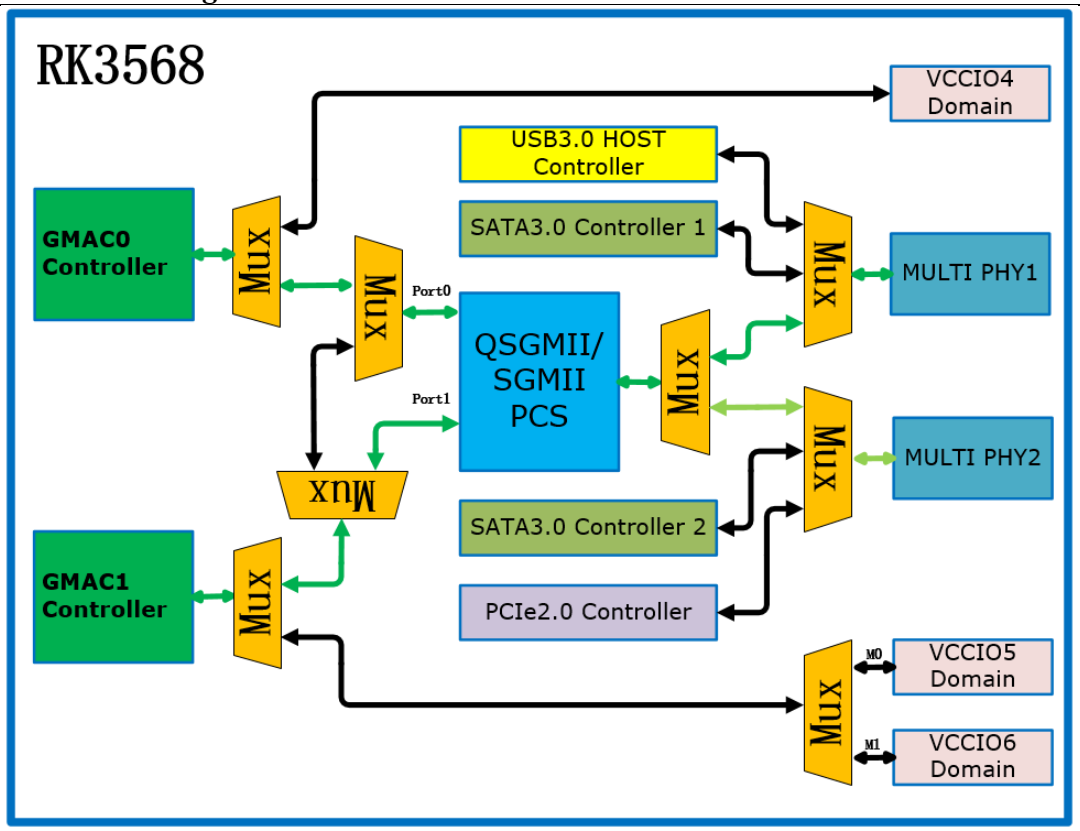


Figure 2-93 The paths of GMAC0, GMAC1, QSGMII/SGMII PCS and QSGMII/SGMII PHY

- The application block diagram of QSGMII using MULTI_PHY1 is as follows (green lines). In this case, the function of GMAC0 and GMAC1 controllers multiplexed to VCCIO4/5/6 is unavailable, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI_PHY1 is unavailable either.

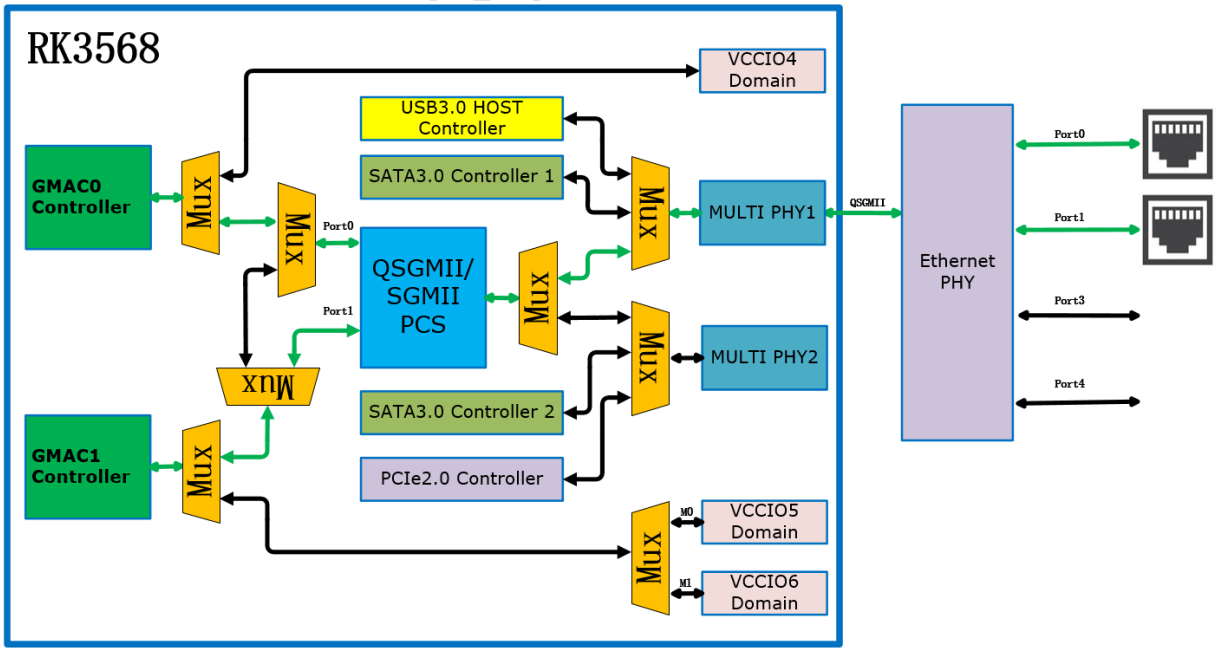


Figure 2-94 The application block diagram of QSGMII-MULTI_PHY1Y1

- The application block diagram of QSGMII using MULTI_PHY2 is as follows (green lines). In this case, the function of GMAC0 and GMAC1 controllers multiplexed to VCCIO4/5/6 is unavailable, the function

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of SATA2 and PCIe2.0 multiplexed by MULTI_PHY2 is unavailable either.

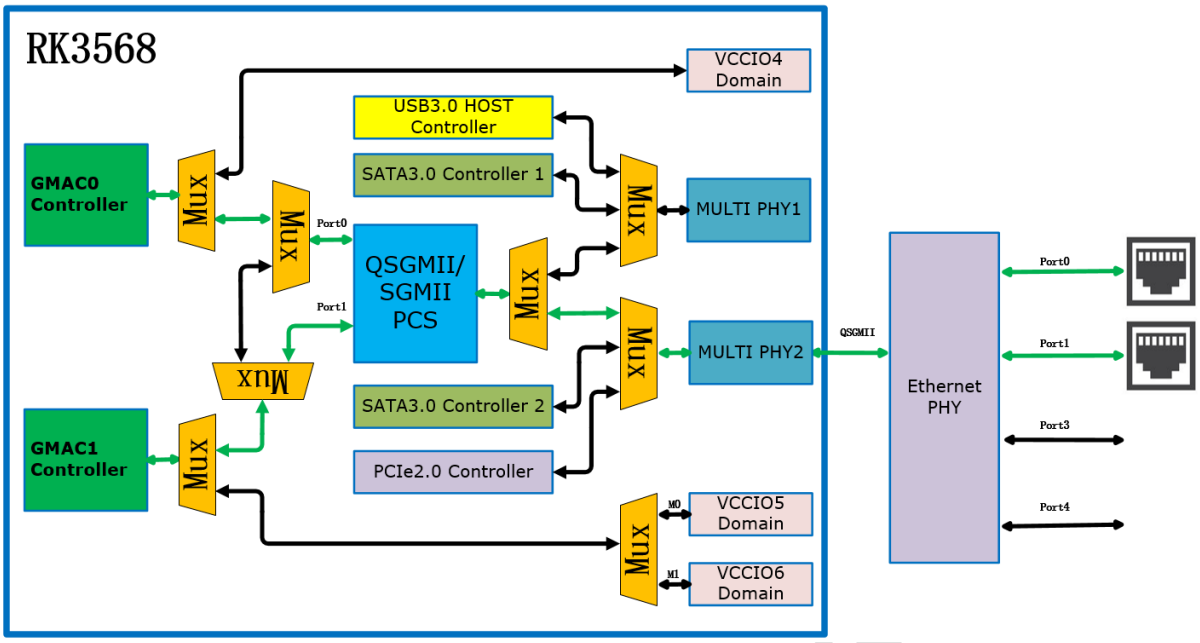
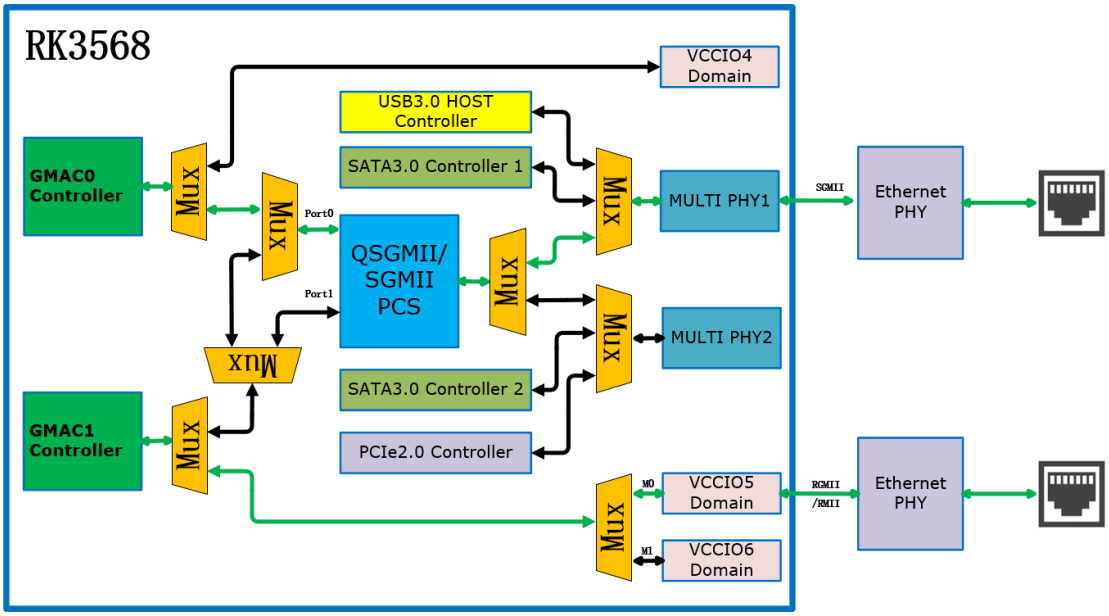



Figure 2-95 The application block diagram of QSGMII-MULTI_PHY2

- The application block diagram of SGMII using MULTI_PHY1 is as follows (green lines), GMAC0 controller or GMAC1 controller are optional.
  - When choosing GMAC0 controller for SGMII, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI_PHY1 is unavailable, the function of GMAC0 multiplexed by VCCIO4 is unavailable either. One of GMAC1 controllers multiplexing to VCCIO5 or VCCIO6 can be selected to implement the second Ethernet port.

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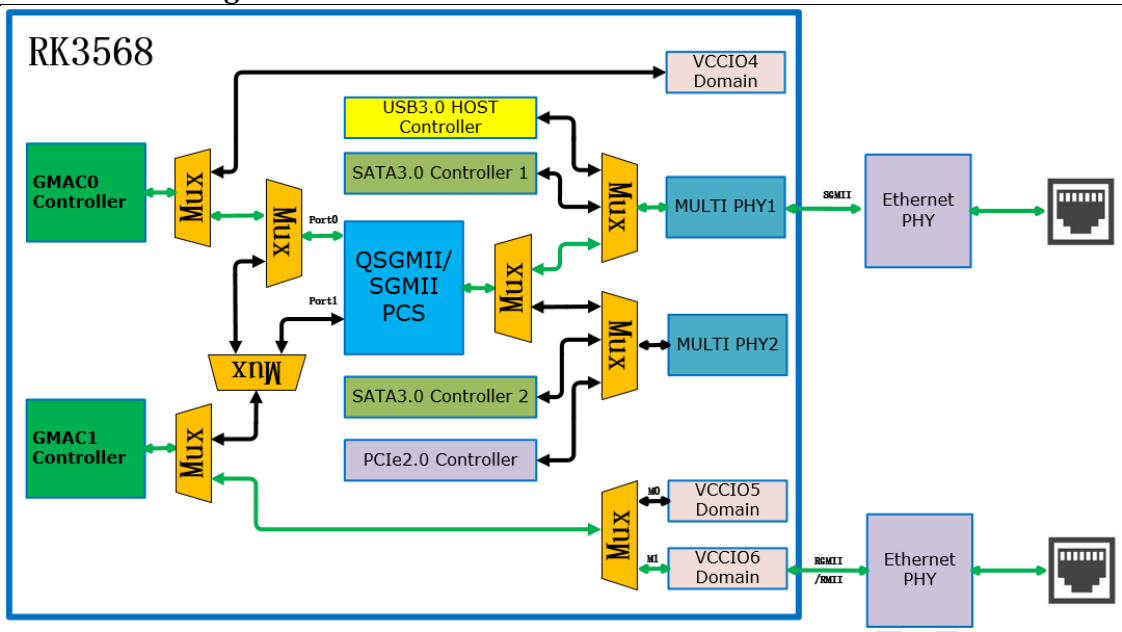


Figure 2-96 The application block diagram of GMAC0-SGMII-MULTI_PHY1

- When choosing GMAC1 controller for SGMII, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI_PHY1 is unavailable, the function of GMAC1 multiplexed by VCCIO5 or VCCIO6 is unavailable either. GMAC0 controller multiplexing to VCCIO4 can implement the second Ethernet port. As shown in the following diagram (green lines).

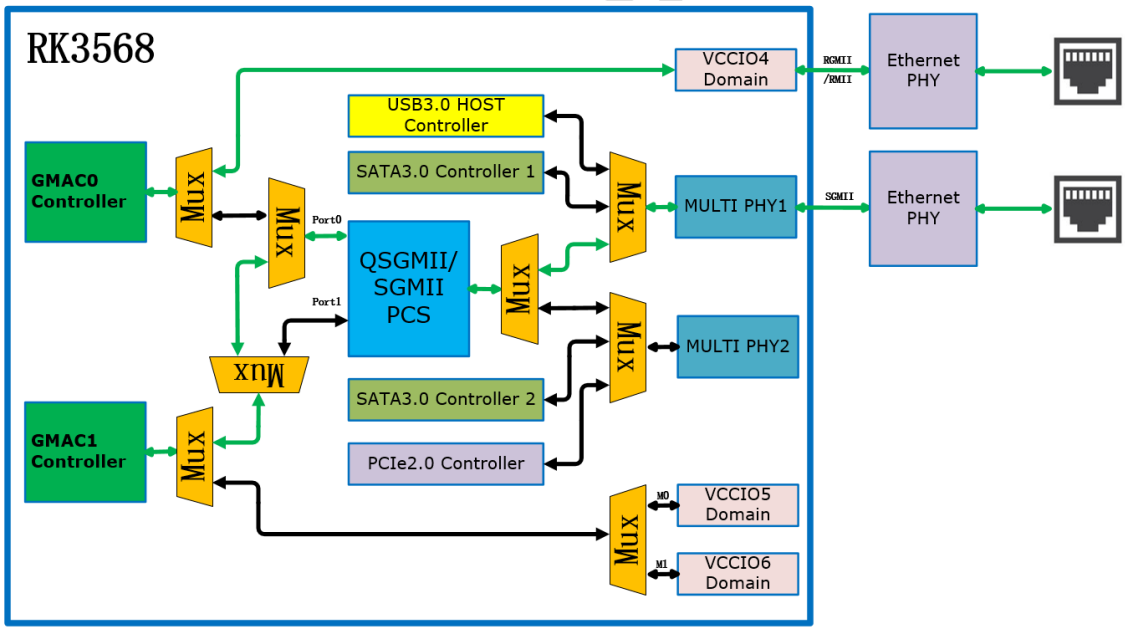


Figure 2-97 The application block diagram of GMAC1-SGMII-MULTI_PHY1

- The application block diagram of SGMII using MULTI_PHY2 is as follows (green lines), GMAC0 controller or GMAC1 controller can be used.
  - When choosing GMAC0 controller for SGMII, the function of SATA2 and PCIe2.0 multiplexed by MULTI_PHY2 is unavailable, the function of GMAC0 multiplexed by VCCIO4 is unavailable either. One of GMAC1 controllers multiplexing to VCCIO5 or VCCIO6 can be selected to implement the second Ethernet port.

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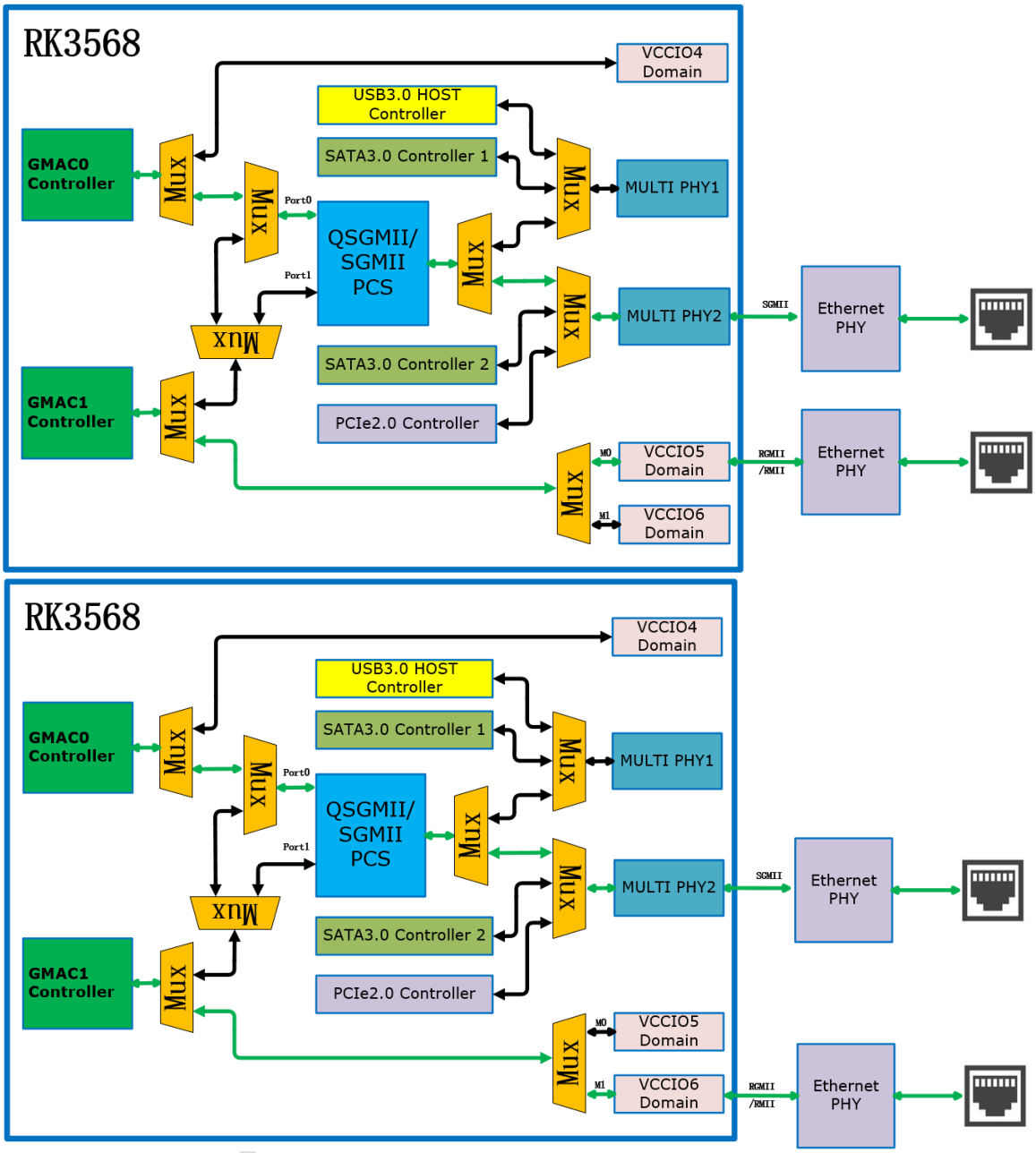


Figure 2-98 The application block diagram of GMAC0-SGMII-MULTI_PHY2

- When choosing GMAC1 controller for SGMII, the function of SATA2 and PCIe2.0 multiplexed by MULTI_PHY2 is unavailable, the function of GMAC1 multiplexed by VCCIO5 or VCCIO6 is unavailable either. GMAC0 controller multiplexing to VCCIO4 can implement the second Ethernet port. As shown in the following diagram (green lines).

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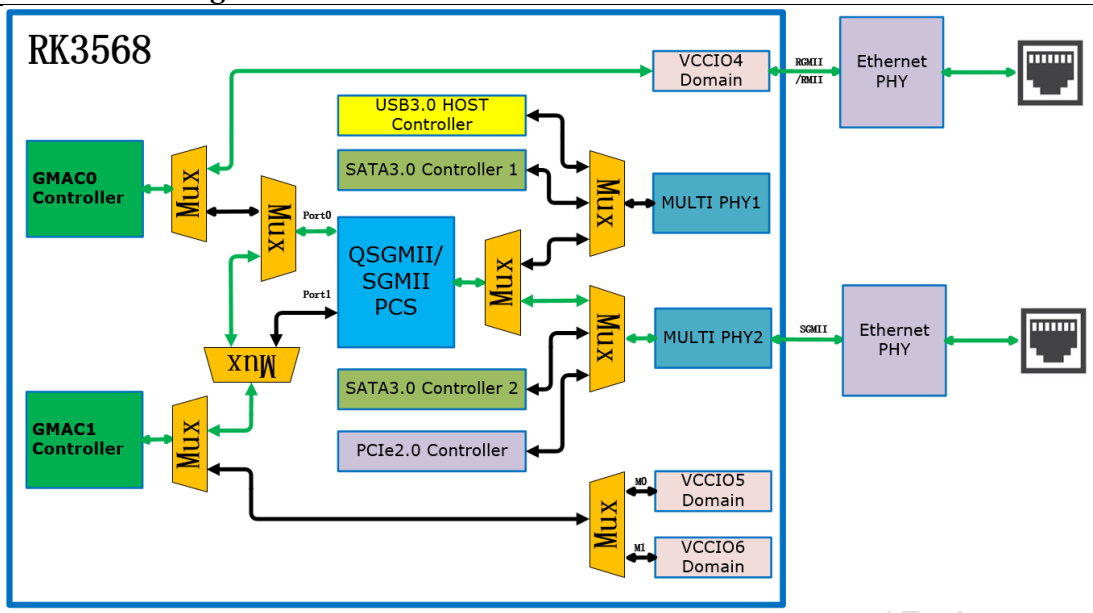
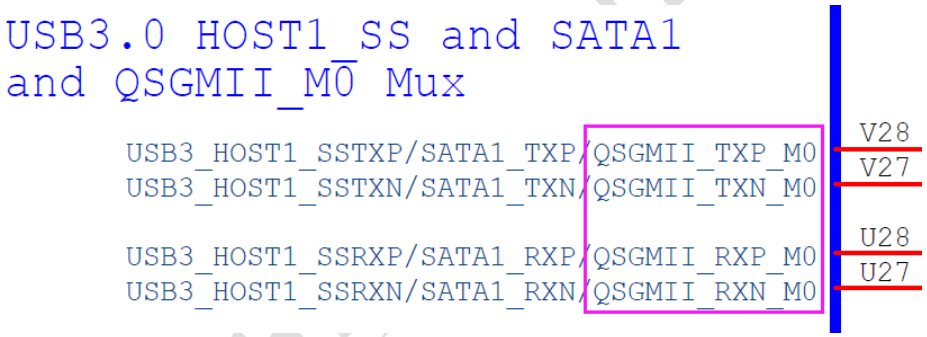
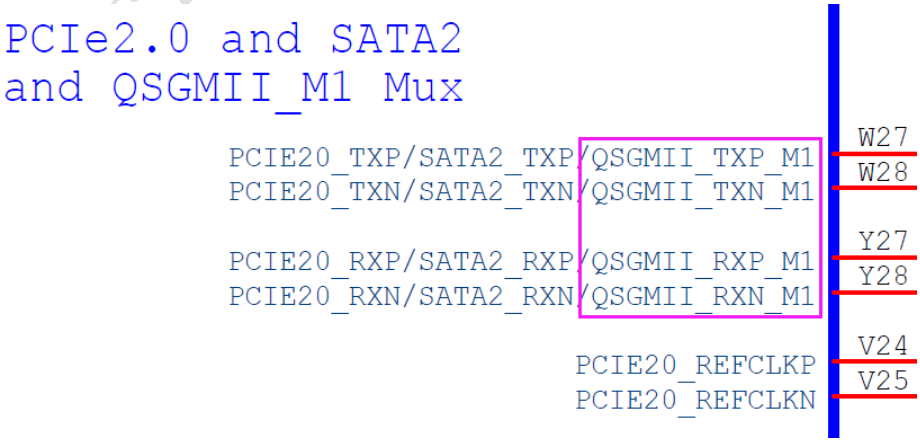



Figure 2-99 The application block diagram of GMAC1-SGMII-MULTI_PHY2

- When QSGMII/SGMII is multiplexed with USB3.0 HOST1 and SATA1 controllers by MULTI_PHY1, the function of QSGMII multiplexed in MULTI_PHY2 is unavailable.




- When QSGMII/SGMII is multiplexed with SATA2 and PCIe2.0 controllers by MULTI_PHY2, the function of QSGMII multiplexed in MULTI_PHY1 is unavailable.




- please notice the following items in QSGMII/SGMII design,:
  - Peripheral circuit and power supply of peripherals should meet the requirements of peripherals.
  - The power pins of MULTI_PHY_AVDD_0V9/1V8 should be placed with 4.7uF and 100nF

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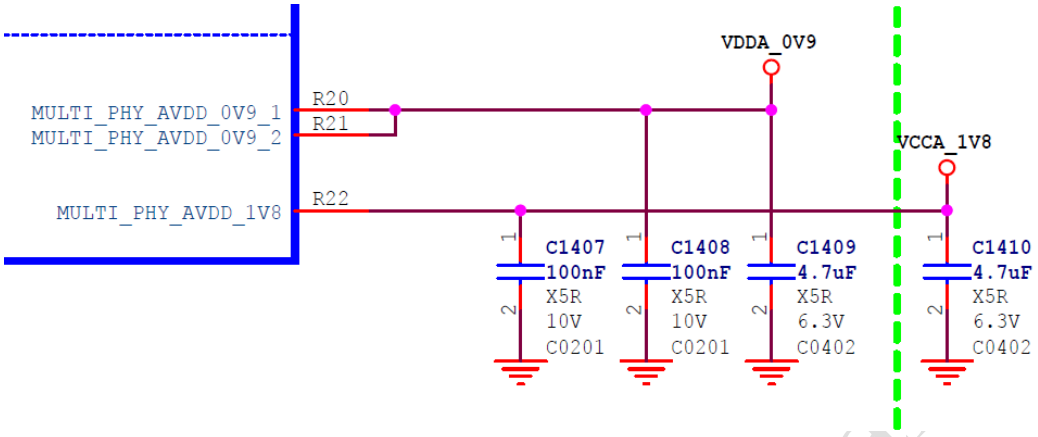
decoupling capacitors, which cannot be deleted. Placed as close to RK3568 pins as possible when layout.




- The 100nF AC coupling capacitor connected in series to TXP/N and RXP/N differential signals of QSGMII/SGMII interface is recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced.
- The matching design recommendations of QSGMII/SGMII interface are shown in the following Table.

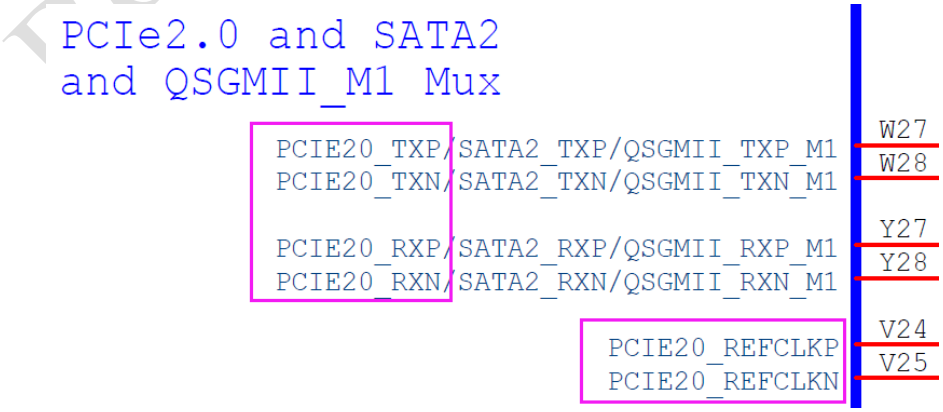
Table 2–20 RK3568 QSGMII/SGMII interface design

| Signal | Connection mode | Description |
|---|---|---|
| QSGMII_TXP/TXN_M0 | Connect in series with a 100Nf capacitor (the 0201 package is recommended) | QSGMII is multiplexed in MULTI_PHY1 data output |
| QSGMII_RXP/RXN_M0 | Connect in series with a 100Nf capacitor (the 0201 package is recommended) | QSGMII is multiplexed in MULTI_PHY1 data output |
| QSGMII_TXP/TXN_M1 | Connect in series with a 100Nf capacitor (the 0201 package is recommended) | QSGMII is multiplexed in MULTI_PHY2 data output |
| QSGMII_RXP/RXN_M1 | Connect in series with a 100Nf capacitor (the 0201 package is recommended) | QSGMII is multiplexed in MULTI_PHY2 data output |

### 2.3.7 PCIe2.0 Circuit

RK3568 has a x1 Lane PCIe2.0 RC Mode controller, which supports RC (Root Complex) mode only.

- PCIe2.0 controller is multiplexed with SATA2 and QSGMII_M1 controllers by MULTI_PHY2.




- PCIE20_REFCLKP/N supports both output and input, and output is provided to EP device by default.

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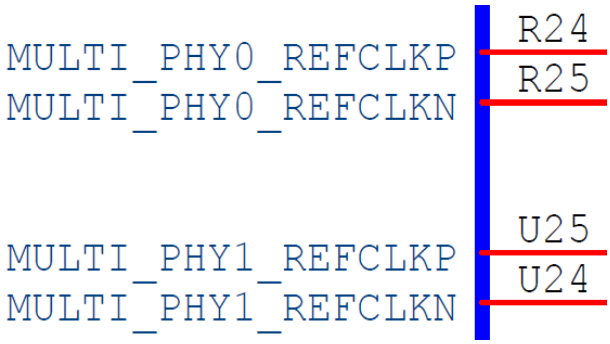
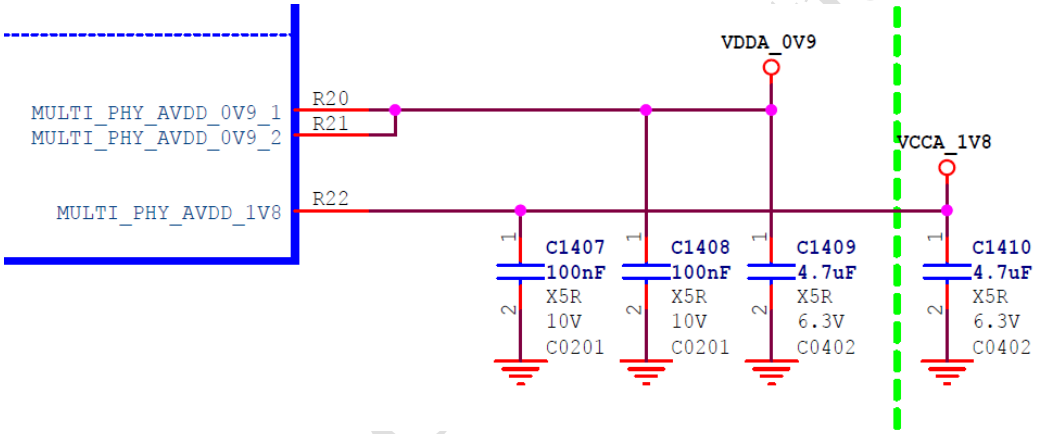
- MULTI PHY0/PHY1 has two pairs of REFCLKs, which are disabled for the moment and hung up.




- please notice the following items in PCIe2.0 design,:
  - When designing Slot, peripheral circuit and power supply should meet the requirements of Spec.
  - The power pins of MULTI_PHY_AVDD_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted. And placed close to RK3568 pins when layout.




  - The 100nF AC coupling capacitor connected in series to TXP/N differential signal of PCIe2.0 interface is recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced.
  - The functional pin must be used by PCIE20_CLKREQn and PCIE20_WAKEn, and they cannot be replaced by GPIO. Please pay special attention to that: choose both_M0 or _M1 or _M2, instead of one is _M0 and the other is _M1.
  - PCIE20_PERSTn can choose functional pin or be replaced by GPIO. If you choose functional pin, PCIE20_PERSTn must be in the same _Mx group as PCIE20_CLKREQn and PCIE20_WAKEn.
  - Standard PCIe Slot：PCIE20_CLKREQn，PCIE20_WAKEn，PCIE20_PERSTn are 3.3V level.
  - It's suggested to add a 100NF capacitor in the Slot pin of PCIE20_PERSTn to enhance the antistatic capability.
  - You can use GPIO when PCIE20_PRSNT is ‘Add In Card’ which means inserting detection pins.
  - The matching design recommendations of PCIe2.0 interface are shown in the following Table.

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Table 2–21 RK3568 PCIe2.0 interface design

| Signal | Connection mode | Description |
|---|---|---|
| PCIE20_TXP/TXN | Connect in series with a 100Nf capacitor (the 0201 package is recommended) | PCIe data output |
| PCIE20_RXP/RXN | Direct connection | PCIe data input |
| PCIE20_REFCLKP/CLKN | Direct connection | PCIe reference clock |
| PCIE20_CLKREQn | Connect in series with a 22ohm resistor | PCIe reference clock request input (RC mode) |
| PCIE20_WAKEn | Connect in series with a 22ohm resistor | PCIe wake-up input(RC mode) |
| PCIE20_PERSTn | Connect in series with a 22ohm resistor | PCIe global reset output(RC mode) |
| PCIE20_PRSNT | Connect in series with a 22ohm resistor | 'Add In Card'-insert test input (RC mode) |

### 2.3.8 PCIe3.0 Circuit

RK3568 has built in a PCIe3.0 x2 Lane Dual Mode controller, a PCIe3.0 x1 Lane RC Mode controller and a PCIe3.0 x2 Lane PHY.

- Support PCIe3.0 x2 Lane RC mode and is compatible with PCIe3.0 x1 Lane RC mode.
- Support PCIe3.0 x2 Lane EP mode and is compatible with PCIe3.0 x1 Lane EP mode.
- Support PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode.

- Connect both PCIe3.0 x2 Lane Dual Mode controller and PCIe3.0 x1 Lane RC Mode controller to PCIe3.0 x2 Lane PHY.

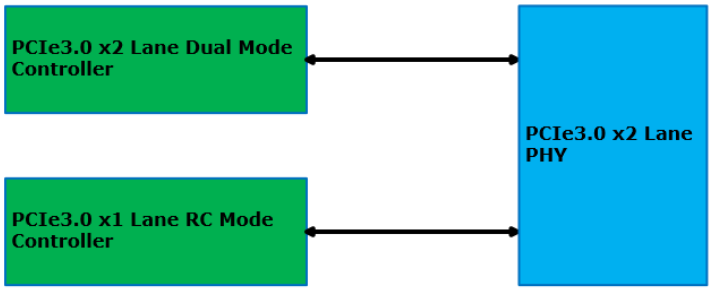


Figure 2-100 PCIe3.0 controller/PCIe3.0 PHY block diagram

- PCIe3.0 x2 Lane RC mode, which is compatible with PCIe3.0 x1 Lane RC mode:

  PCIe3.0 x2 Lane Dual Mode controller usage:
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x2 Lane RC mode, its corresponding signals are PCIE30_TX0P、PCIE30_TX0N、PCIE30_RX0P、PCIE30_RX0N、PCIE30_TX1P、PCIE30_TX1N、PCIE30_RX1P、PCIE30_RX1N.
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30_TX0P、PCIE30_TX0N、PCIE30_RX0P、PCIE30_RX0N.
- PCIe3.0 x2 Lane EP mode is compatible with PCIe3.0 x1 Lane EP mode:

  PCIe3.0 x2 Lane Dual Mode controller usage:
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x2 Lane EP mode, its corresponding signals are PCIE30_TX0P、PCIE30_TX0N、PCIE30_RX0P、PCIE30_RX0N、PCIE30_TX1P、PCIE30_TX1N、PCIE30_RX1P、PCIE30_RX1N.
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane EP mode, its corresponding

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signals are PCIE30_TX0P、PCIE30_TX0N、PCIE30_RX0P、PCIE30_RX0N.

- PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode:

  One uses PCIe3.0 x2 Lane Dual Mode controller, and the other one uses PCIe3.0 x1 Lane RC Mode controller.

  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30_TX0P、PCIE30_TX0N、PCIE30_RX0P、PCIE30_RX0N.
  - When PCIe3.0 x1 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30_TX1P、PCIE30_TX1N、PCIE30_RX1P、PCIE30_RX1N.

- PCIE30_REFCLKP/N supports input only.
  - Require providing HCSL level clock input.
  - Must provide the clock which meets requirement of PCIe3.or above.
  - When you use RK3568 PCIe3.0 x2 Lane RC mode, which is compatible with PCIe3.0 x1 Lane RC mode, the reference clock paths are shown as follows:

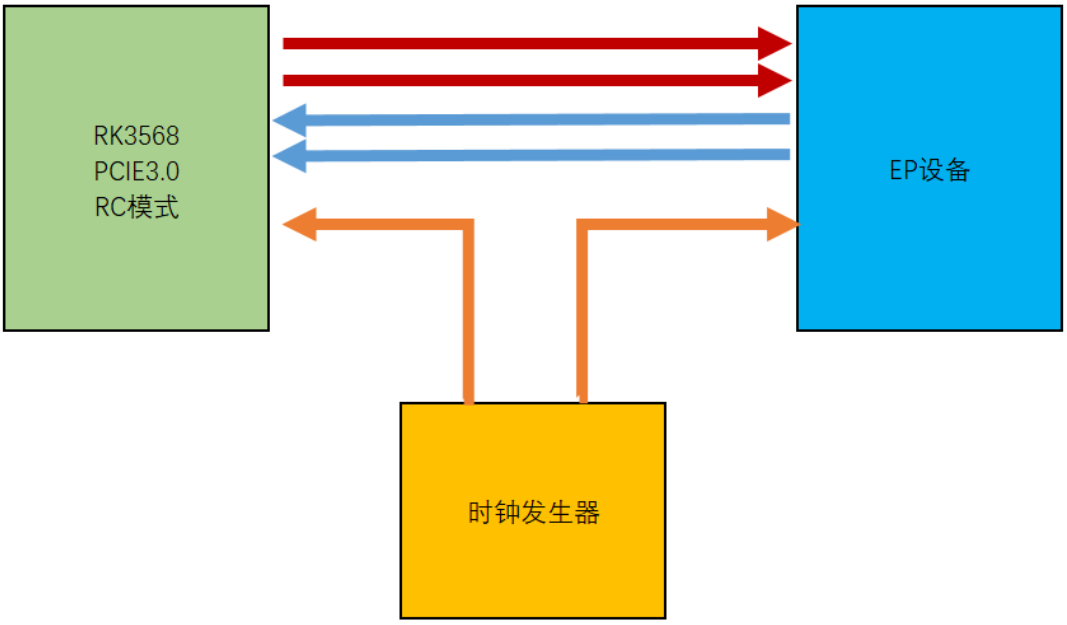


Figure 2-101 Reference clock paths in RK3568 PCIe3.0 x2 Lane RC mode

  - When in RK3568 PCIe3.0 x2 Lane EP mode, which is compatible with PCIe3.0 x1 Lane EP mode, the reference clock paths are shown as follows:

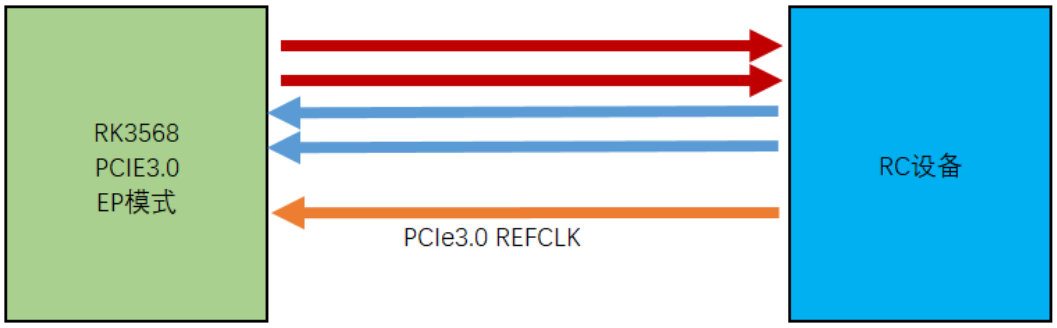


Figure 2-102 Reference clock paths in RK3568 PCIe3.0 x2 Lane EP mode

  - When in RK3568 PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode, the reference clock

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paths are shown as follows:

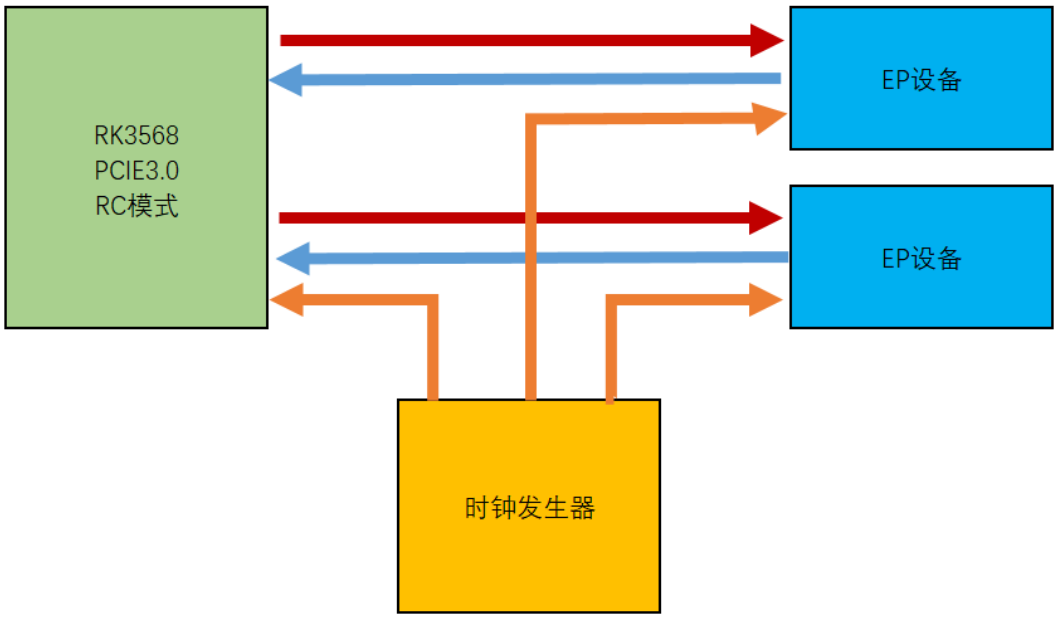


Figure 2-103 The reference clock paths in RK3568 PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode

- Please note the following items in PCIe3.0 design:
  - In the design of slot, peripheral circuit and power supply should meet the requirements of Spec.
  - The power pins of PCIE30_AVDD_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted. And Place them close to RK3568 pins when layout.

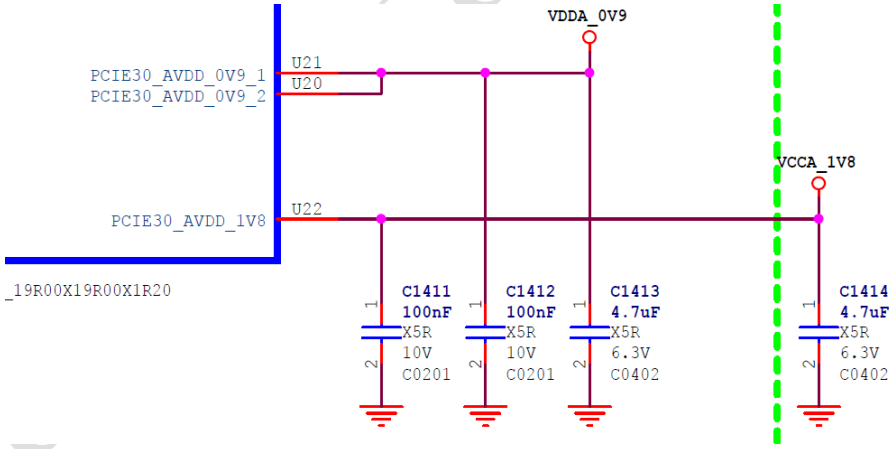


Figure 2–1 The decoupling capacitors of PCIe3.0 PHY power supply

Figure 2-104 PCIe3.0 PHY power decoupling capacitors

  - The 220nF AC coupling capacitor connected in series to TX0P/N and TX1P/N differential signals of PCIe3.0 interface is recommended to use 0201package, if you use lower ESR and ESL, impedance changes on the line can also be reduced.
  - PCIE_RESREF is an external reference resistor pin of PCIe3.0 PHY, which externally connects a 200 Ω resistance to ground with accuracy of 1%.The value of the resistance cannot be changed and it should be placed close to RK3568 chip pins when layout.

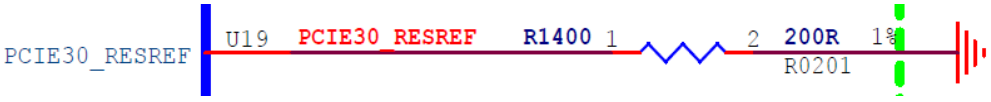


Figure 2-105 PCIe3.0 PHY RESREF pin

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- PCIE30X2_CLKREQn, PCIE30X2_WAKEn and PCIE30X2_PERSTn are corresponding to Lane PCIe3.0 x2 Dual Mode controller.
- PCIE30X1_CLKREQn, PCIE30X1_WAKEn and PCIE30X1_PERSTn are corresponding to Lane PCIe3.0 x1 RC Mode controller.

| | | | | | |
|---|---|---|---|---|---|
| **Option1** | **PCIe3.0 x2Lane** | PCIE30_REFCLK (RC/EP:input) | PCIE30_TX0<br>PCIE30_RX0<br>PCIE30_TX1<br>PCIE30_RX1 | PCIE30X2_CLKREQn<br>PCIE30X2_WAKEn<br>PCIE30X2_PERSTn<br>PCIE30X2_BUTTONRSTn | **RC or EP** |
| **Option2** | **PCIe3.0 x1Lane + PCIe3.0 x1Lane** | PCIE30_REFCLK (RC:input) | PCIE30_TX0<br>PCIE30_RX0 | PCIE30X2_CLKREQn<br>PCIE30X2_WAKEn<br>PCIE30X2_PERSTn<br>PCIE30X2_BUTTONRSTn | **Only RC** |
| | | | PCIE30_TX1<br>PCIE30_RX1 | PCIE30X1_CLKREQn<br>PCIE30X1_WAKEn<br>PCIE30X1_PERSTn<br>PCIE30X1_BUTTONRSTn | **Only RC** |

- PCIE30X2_CLKREQn, PCIE30X1_CLKREQn, PCIE30X2_WAKEn and PCIE30X1_WAKEn must be used as functional pins, and they cannot be replaced by GPIO. Note: select both _M0 or _M1 or _M2 instead of one _M0 and one _M1.
- PCIE30X2_PERSTn and PCIE30X1_PERSTn can be used as functional pins or be replaced by GPIO. If you choose functional pins, PCIE30X2_PERSTn and PCIE30X1_PERSTn must be in the same _Mx group as PCIE30X2_CLKREQn、PCIE30X2_WAKEn and PCIE30X1_CLKREQn、PCIE30X1_WAKEn.
- Standard PCIe Slot：PCIE30X2_CLKREQn、PCIE30X1_CLKREQn、PCIE30X2_WAKEn、PCIE30X1_WAKEn、PCIE30X2_PERSTn and PCIE30X1_PERSTn are 3.3V level.
- It's suggested to add a 100nF capacitor in the Slot pin of PCIE30X2_PERSTn and PCIE30X1_PERSTn to enhance the antistatic capability.
- You can use GPIO when PCIE30_PRSNT is 'Add In Card' which means inserting detection pins.
- The matching design recommendations of PCIe3.0 interface are shown in the following Table.

Table 2–22 RK3568 PCIe3.0 interface design

| Signal | Connection mode | Description |
|---|---|---|
| PCIE30_TX0P/TX0N | Connect in series with a 220nF capacitor(the 0201 package is recommended) | PCIe data output |
| PCIE30_RX0P/RX0N | Direct connection | PCIe data input |
| PCIE30_TX1P/TX1N | Connect in series with a 220nF capacitor(the 0201 package is recommended) | PCIe data output |
| PCIE30_RX1P/RX1N | Direct connection | PCIe data input |
| PCIE30_REFCLKP_IN/ PCIE30_REFCLKN_IN | Direct connection | PCIe reference clock input |
| PCIE30_RESREF | Grounding with 200 Ω/1% resistance | External reference resistor of PCIe3.0 PHY |
| PCIE30X2_CLKREQn | Connect in series with a 22ohm resistor | PCIe reference clock request input (RC mode)<br>PCIe reference clock request output (EP mode) |
| PCIE30X2_WAKEn | Connect in series with a 22ohm resistor | PCIe wake-up input (RC mode)<br>PCIe wake-up output (EP mode) |

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| Signal | Connection mode | Description |
|---|---|---|
| PCIE30X2_PERSTn | Connect in series with a 22ohm resistor | PCIe global reset output (RC mode)<br>PCIe global reset input (EP mode) |
| PCIE30X2_PRSNT | Connect in series with a 22ohm resistor | 'Add In Card'-insert test input (RC mode) |
| PCIE30X1_CLKREQn | Connect in series with a 22ohm resistor | PCIe reference clock request input (RC mode) |
| PCIE30X1_WAKEn | Connect in series with a 22ohm resistor | PCIe wake-up input (RC mode) |
| PCIE30X1_PERSTn | Connect in series with a 22ohm resistor | PCIe global reset output (RC mode) |
| PCIE30X1_PRSNT | Connect in series with a 22ohm resistor | 'Add In Card'-insert test input (RC mode) |

## 2.3.9 Video Input Interface Circuit

### 2.3.9.1 MIPI CSI RX interface

RK3568 has built in a MIPI CSI RX PHY, which supports MIPI V1.2 with 4Lane in total and two pairs of clocks.

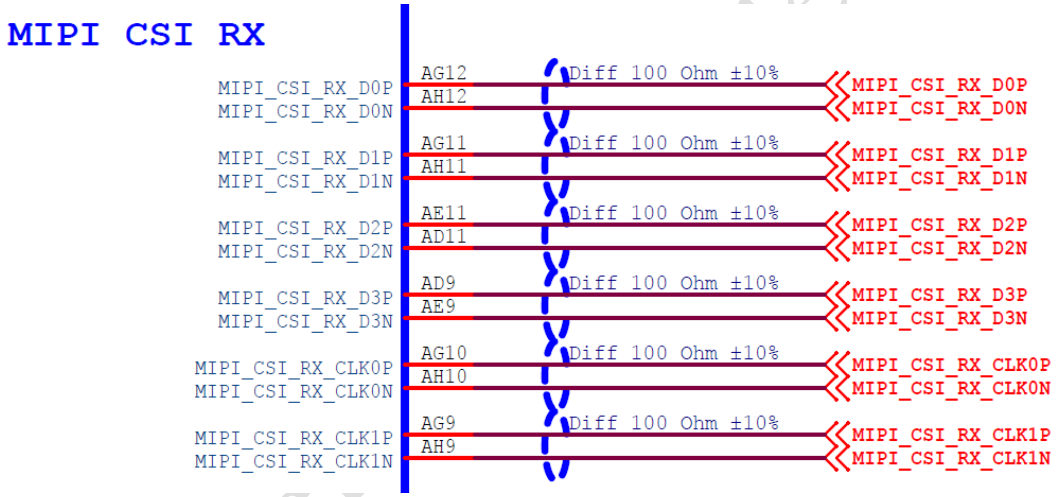


Figure 2-106 RK3568 MIPI CSI RX signal pins

- Support x4Lane mode, refers to MIPI_CSI_RX_CLK0 for MIPI_CSI_RX_D[3:0] data.
- Support x2Lane+x2Lane mode,

  MIPI_CSI_RX_D[1:0] data refers to MIPI_CSI_RX_CLK0,

  MIPI_CSI_RX_D[3:2] data refers to MIPI_CSI_RX_CLK1.

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| | | |
|---|---|---|
| Option1 | Sensor1 x4Lane | MIPI_CSI_RX_D0-3<br>MIPI_CSI_RX_CLK0 |
| Option2 | Sensor1 x2Lane<br>+<br>Sensor2 x2Lane | MIPI_CSI_RX_D0-1<br>MIPI_CSI_RX_CLK0 |
| | | MIPI_CSI_RX_D2-3<br>MIPI_CSI_RX_CLK1 |

Figure 2-107 RK3568 MIPI CSI working mode and data, clock allocation

- Please pay attention to the design of MIPI CSI RX:
  - MIPI_CSI_RX_AVDD_0V9，MIPI_CSI_RX_AVDD_1V8 power pin and VDDA0V9_IMAGE, VCCA1V8_IMAGE are required to be isolated with magnetic beads. Please refer to the schematic design for details;

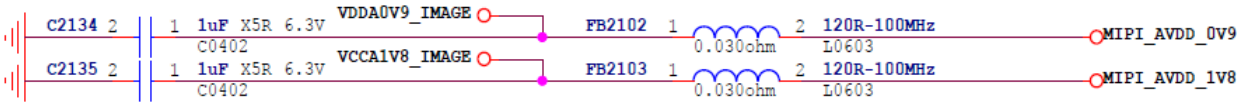


Figure 2-108 MIPI CSI PHY power circuit isolated with magnetic beads

  - To improve MIPI CSI RX performance, the decoupling capacitors of every PHY power supply cannot be deleted, and they should be placed close to power pins when layout.

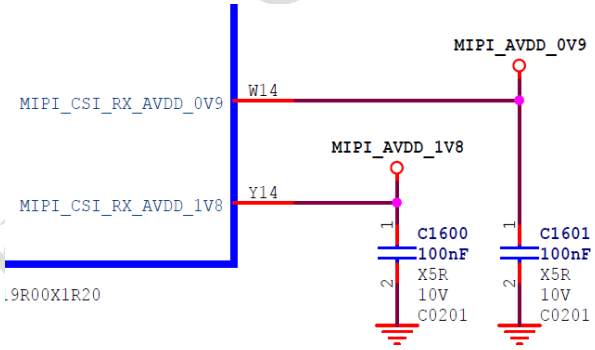


Figure 2-109 MIPI CSI RX PHY power decoupling capacitors

  - The matching design recommendations of MIPI CSI RX interface are shown in the following Table.

Table 2–23 RK3568 MIPI CSI RX interface design

| Signal | Connection mode | Description |
|---|---|---|
| MIPI_CSI_RX_D0P/D0N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. Common mode inductor is reserved for EMI suppression | MIPI CSI data Lane0 input |
| MIPI_CSI_RX_D1P/D1N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. | MIPI CSI data Lane1 input |

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| Signal | Connection mode | Description |
|---|---|---|
| MIPI_CSI_RX_D2P/D2N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. | MIPI CSI data Lane2 input |
| MIPI_CSI_RX_D3P/D3N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. | MIPI CSI data Lane3 input |
| MIPI_CSI_RX_CLK0P/CLK0N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. | MIPI CSI clock0 input |
| MIPI_CSI_RX_CLK1P/CLK1N | Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. | MIPI CSI clock1 input |

#### 2.3.9.2 CIF（DVP）Interface

CIF I/O domain supplies power to VCCIO6. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of product Camera (1.8V or 3.3V). Meanwhile, the pull-up level of I2C must be consistent with the power supply, otherwise it will cause abnormal or unable operation of the Camera. Please note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and may damage the IO.

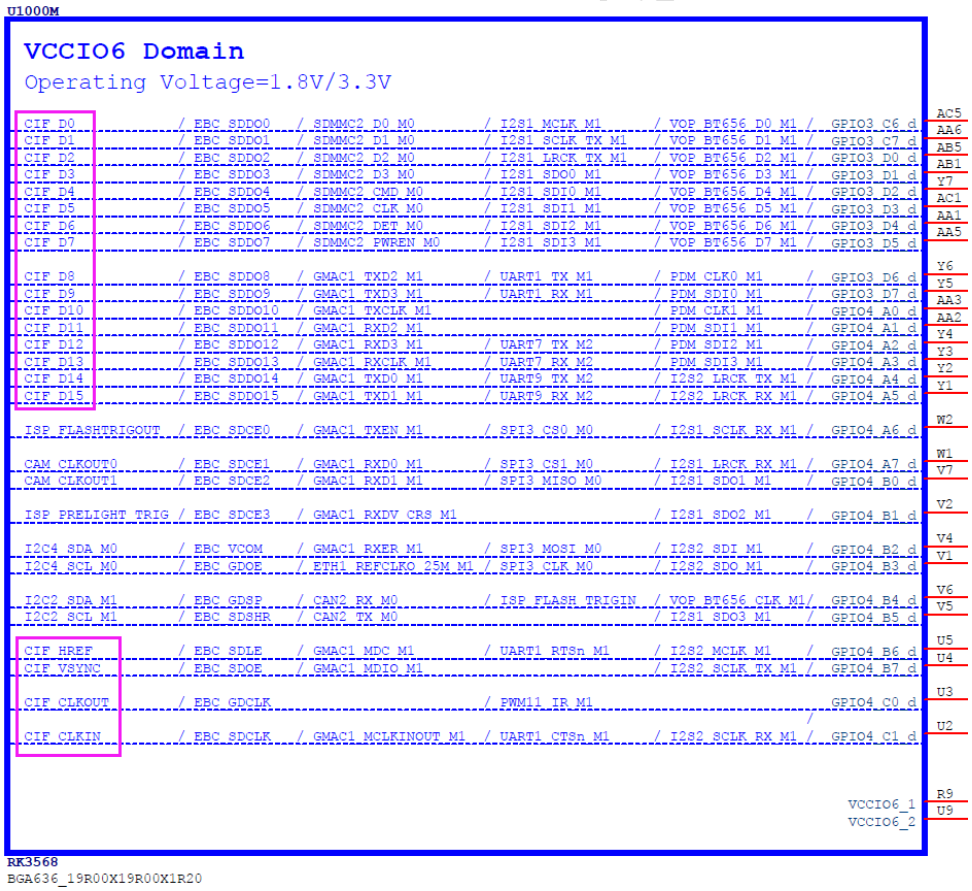


Figure 2-110 RK3568 CIF functional pins

- CIF interface supports following formats:
  - Support BT601 YCbCr 422 8bit input
  - Support BT656 YCbCr 422 8bit input
  - Support RAW 8/10/12bit input

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- Support BT1120 YCbCr 422 8/16bit input, single/dual-edge sampling
- Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

■ Relationship between 8/10/12/16bit data of CIF[15:0] is shown as follows, with high-order aligned.

| Mode | 16bit | 12bit | 10bit | 8bit |
|---|---|---|---|---|
| CIF_D0 | D0 | -- | -- | -- |
| CIF_D1 | D1 | -- | -- | -- |
| CIF_D2 | D2 | -- | -- | -- |
| CIF_D3 | D3 | -- | -- | -- |
| CIF_D4 | D4 | D0 | -- | -- |
| CIF_D5 | D5 | D1 | -- | -- |
| CIF_D6 | D6 | D2 | D0 | -- |
| CIF_D7 | D7 | D3 | D1 | -- |
| CIF_D8 | D8 | D4 | D2 | D0 |
| CIF_D9 | D9 | D5 | D3 | D1 |
| CIF_D10 | D10 | D6 | D4 | D2 |
| CIF_D11 | D11 | D7 | D5 | D3 |
| CIF_D12 | D12 | D8 | D6 | D4 |
| CIF_D13 | D13 | D9 | D7 | D5 |
| CIF_D14 | D14 | D10 | D8 | D6 |
| CIF_D15 | D15 | D11 | D9 | D7 |

Figure 2-111 RK3568 Relationship between data of CIF

■ Data relationship in BT1120 16bit mode is shown as follows, and supports YC Swap.

Table 2–24 RK3568 Data relationship in BT1120 16bit mode

| Pin Name | Default mode | | Swap is enabled | |
|---|---|---|---|---|
| | Pixel #0 | Pixel #1 | Pixel #0 | Pixel #1 |
| CIF_D0 | Y0[0] | Y1[0] | Cb0[0] | Cr0[0] |
| CIF_D1 | Y0[1] | Y1[1] | Cb0[1] | Cr0[1] |
| CIF_D2 | Y0[2] | Y1[2] | Cb0[2] | Cr0[2] |
| CIF_D3 | Y0[3] | Y1[3] | Cb0[3] | Cr0[3] |
| CIF_D4 | Y0[4] | Y1[4] | Cb0[4] | Cr0[4] |
| CIF_D5 | Y0[5] | Y1[5] | Cb0[5] | Cr0[5] |
| CIF_D6 | Y0[6] | Y1[6] | Cb0[6] | Cr0[6] |
| CIF_D7 | Y0[7] | Y1[7] | Cb0[7] | Cr0[7] |
| CIF_D8 | Cb0[0] | Cr0[0] | Y0[0] | Y1[0] |
| CIF_D9 | Cb0[1] | Cr0[1] | Y0[1] | Y1[1] |
| CIF_D10 | Cb0[2] | Cr0[2] | Y0[2] | Y1[2] |
| CIF_D11 | Cb0[3] | Cr0[3] | Y0[3] | Y1[3] |
| CIF_D12 | Cb0[4] | Cr0[4] | Y0[4] | Y1[4] |
| CIF_D13 | Cb0[5] | Cr0[5] | Y0[5] | Y1[5] |
| CIF_D14 | Cb0[6] | Cr0[6] | Y0[6] | Y1[6] |
| CIF_D15 | Cb0[7] | Cr0[7] | Y0[7] | Y1[7] |

■ The pull up/down and matching design recommendations of CIF interface are shown in the following Table.

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Table 2–25 RK3568 CIF interface design

| Signal | Pull up/down Inside | Connection, Mode | Description (chip end) |
|---|---|---|---|
| CIF_D[15:0] | Pull-down | Direct connection, it's recommended to reserve a series resistor near device end. | CIF data input |
| CIF_HREF | Pull-down | Direct connection, it's recommended to reserve a series resistor near device end. | CIF row synchronous input |
| CIF_VSYNC | Pull-down | Direct connection, it's recommended to reserve a series resistor near device end. | CIF field synchronous input |
| CIF_CLKIN | Pull-down | Connect 22ohm resistor in series, close to the device | CIF clock input |
| CIF_CLKOUT | Pull-down | Connect 22ohm resistor in series, close to the chip | CIF clock output, can provide MCLK work clock for device. |

- When the board-to-board connection is through connectors, it is recommended to connect a resistor with a certain resistance in series (between 22ohm and 100ohm, as long as it can meet the SI test), and reserve TVS devices
- Note when designing MIPI CSI RX/CIF:
  - DVDD power supply of Camera is 1.2V/1.5V/1.8V, etc. Please provide accurate power supply according to the specifications of Camera. The reference circuit is 1.2V by default;
  - DVDD current of some Cameras is relatively large, if the current is more than 100mA, it is suggested to use DCDC for power supply;
  - Several power supplies of Camera require the power on sequence, please adjust the power on sequence according to the specifications of Camera, the default power on sequence in the schematic design is 1.8V-->1.2V-->2.8V;
  - When using the Camera with CIF interface, you should pay attention that DOVDD (IO power supply) of Camera must use the same voltage as VCCIO6 power supply;
  - When using two Cameras, the power supply can be separated or combined according to the actual requirements. The power supply in schematic design is separated by default.
  - For cameras with AF function, VCC2V8_AF needs to supply the power separately or shares supply with AVCC2V8_DVP which should be separated by magnetic beads;
  - The decoupling capacitors of all power supplies of Camera should not be deleted, they must be reserved and placed close to the connector;
  - PWDN signal of Camera must be controlled by GPIO, and GPIO level must match with Camera IO level;
  - Reset signal of Camera is suggested to be controlled by GPIO, and GPIO level must match with Camera IO level. The 100nF capacitors of Reset signal should not be deleted and placed near the connector to enhance anti ESD capability;
  - MCLK of Camera can be got from:

    1:CAM_CLKOUT0

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2:CAM_CLKOUT1

3:CIF_CLKOUT

4:REFCLK_OUT

Note: clock level must match with Camera IO level, if not, level conversion or resistor divider must be performed to match the level

- If two Cameras are the same model, note that whether I2C addresses are the same or not. If the address are the same, then two I2C buses are required.

### 2.3.10 Video Output Interface Circuit

RK3568 has a built-in VOP controller, three output Ports, and supports HDMI2.0 TX/MIPI DSI TX0/MIPIO DSI TX1/LVDS TX/eDP TX/RGB/BT1120/BT656 video interface output.

Path diagram of VOP and video interface output:

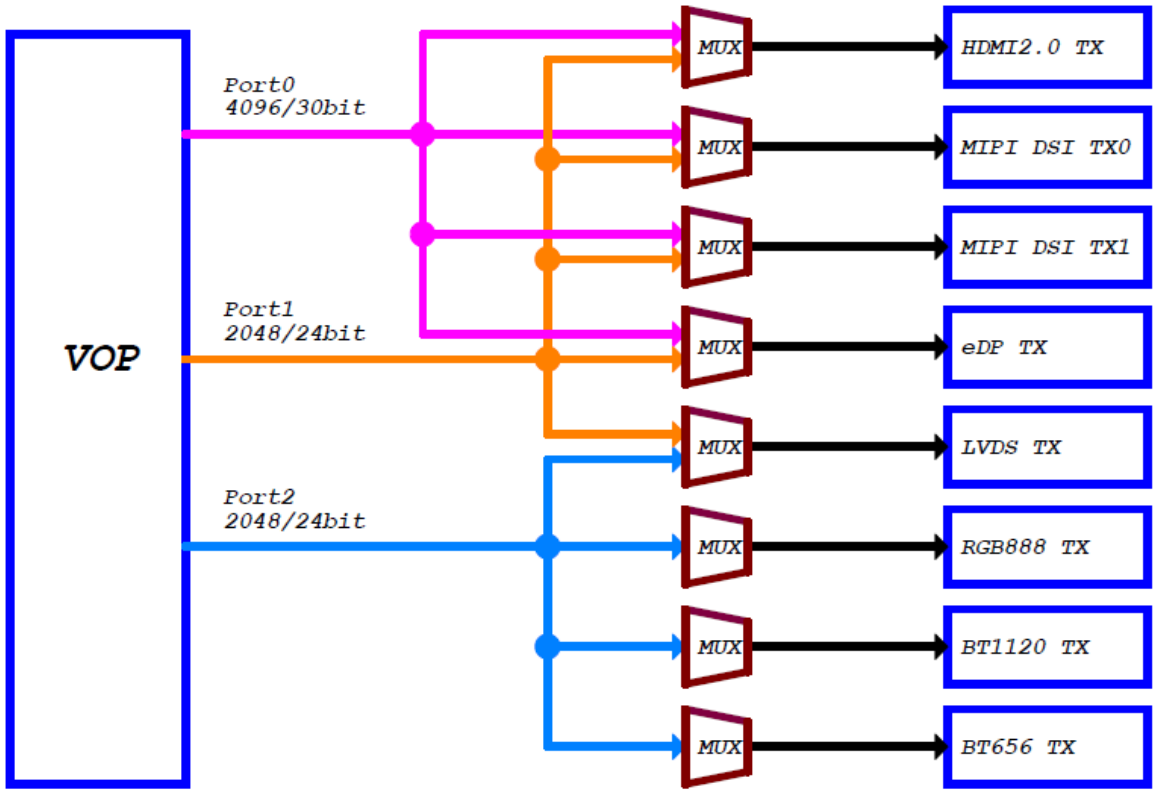


Figure 2-112 RK3568 the output path diagram of VOP and video interface

#### 2.3.10.1 HDMI2.0 TX interface

RK3568 has a built-in HDMI2.0TX PHY with maximum output resolution up to 4096X2160@60Hz.

- TMDS signal is shown in the following diagram, it is required to connect a 2.2ohm resistor in series close to RK3568 end, the resistor cannot be deleted to improve the signal quality and strengthen anti ESD and surge capability.

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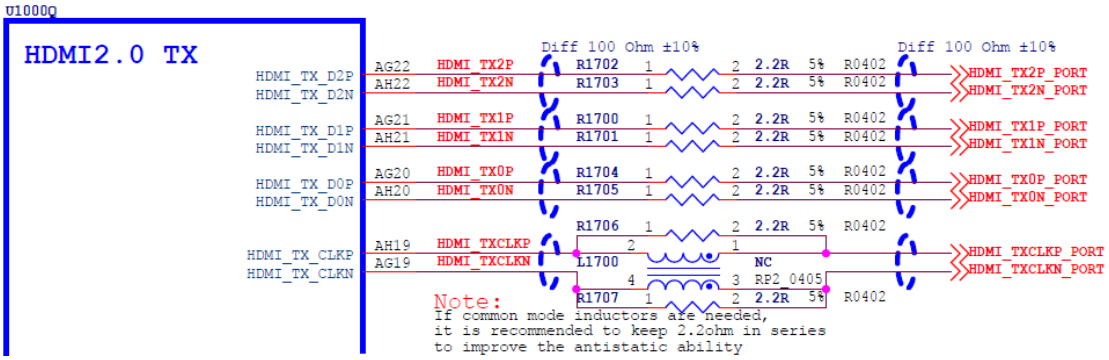


Figure 2-113 RK3568 HDMI2.0 TX PHY TMDS pins

- The power pins of HDMI_TX_AVDD_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted and be placed close to RK3568 pins when layout.

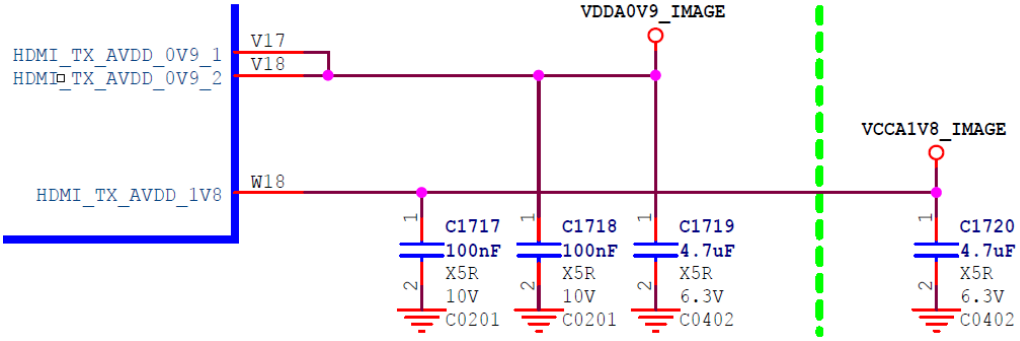


Figure 2-114 RK3568 HDMI2.0 TX PHY power supply decoupling capacitances

- HDMI_TX_REXT is the external reference resistor pin of HDMI2.0TX PHY, connect a 1620Ω/1% resistor to ground，the value of resistance cannot be changed, and place the resistor close to RK3568 pins when layout.


Figure 2-115 RK3568 HDMI2.0 TX PHY REXT pins

- HDMI_TX_HPDIN is a native function of HDMI2.0TX PHY. It supports 5V level, and the effective detection level is 2.4-5.3V. It is recommended to place a 100nF capacitor near the chip pin of RK3568 to eliminate jitter.


Figure 2-116 RK3568 HDMI2.0 TX PHY HPD pins

- Near the end of HDMI connector, it needs to connect a 1Kohm resistor in series to strengthen anti ESD and surge capability., and you need reserve a 100Kohm resistor grounded.

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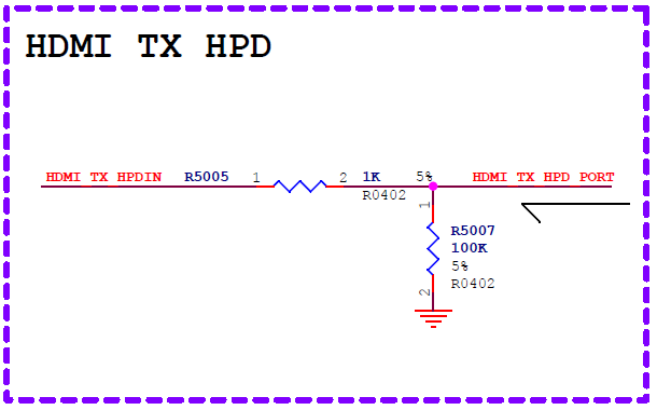


Figure 2-117 RK3568 HDMI2.0 TX PHY HPD circuit

- HDMI_TX_CEC function is multiplexed in two locations, one is in the IO of VCCIO7 power domain, and the other is in the IO of PMUIO2 power domain; It is defined as 3.3V level in the CEC protocol, but the protocol requires that 3.3V voltage is added to the CEC pin by a 27K resistor and leakage current is not allowed to exceed 1.8uA.

**Test ID 7-15: CEC Line Degradation**

| Reference | Requirement |
|---|---|
| [HDMI: Table 4-40]<br>CEC line Electrical Specifications for all Configurations | A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device).<br><br>Maximum CEC line leakage current must be ≤1.8µA |

Figure 2-118 HDMI CEC protocol requirements

When RK3568 IO Domain is not powered on, if there is voltage on IO, it may cause electricity leakage. For example, RK3568 is power-off, and HDMI cable is still connected to Sink end (TV or monitor), at this time, CEC of Sink end is powered, and electricity will leak to RK3568 IO through HDMI cable, which will cause CEC leakage current of more than 1.8uA. Therefore, an isolation circuit needs to be added externally, and the resistance value of R5006 is not allowed to be modified at will. You need to use 27Kohm, and the default choice for Q5002 is 2SK3018. If you want to change to other models, the junction capacitance must be similar. If the junction capacitance is too large, it may not only influence working, but also fail the certification.

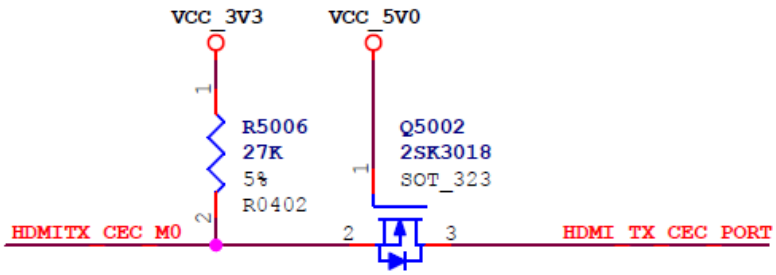


Figure 2-119 HDMI CEC CEC isolating circuit

- HDMI_TX DDC_SCL/DDC_SDA is I2C/DDC bus of HDMI TX controller, its function multiplexes to the IO of VCCIO7 power domain. DDC_SCL/DDC_SDA is defined to 5V level in the protocol, while RK3568 IO doesn't support 5V level, so the level conversion circuit must be added and cannot be deleted,

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Using MOS tube for level conversion by default, and the MOS model is 2SK3018. If you want to change to other models, the junction capacitance must be similar. If the junction capacitance is too large, it may not only influence working, but also fail the certification.

It's recommend to use pull-up resistance with default value, and the value cannot be modified.

D5000 diode cannot be deleted to prevent electric leakage from Sink to VCC_5V0.

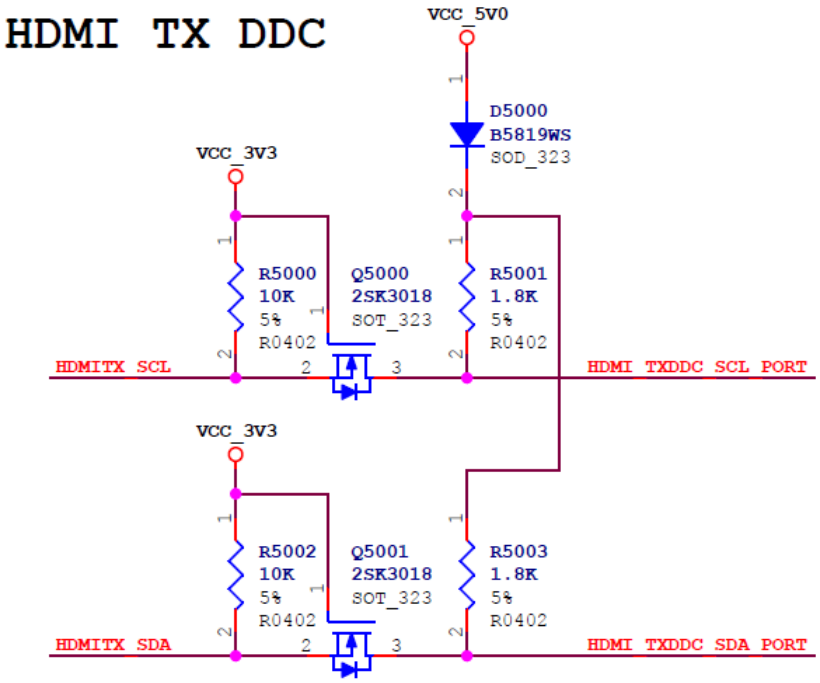


Figure 2-120 HDMI DDC level conversion circuit

- Make sure that Pin18 voltage of HDMI connector is between 4.8-5.3V, and the pin should be placed with 1uF decoupling capacitor, which cannot be deleted. The capacitor should be placed close to HDMI connector pins when layout.
- In order to enhance anti ESD capability, ESD devices must be reserved in signals, ESD parasitic capacitors of HDMI TMDS signal should not exceed 0.4pF, and ESD parasitic capacitors of other signals are recommended not to exceed 1pF.

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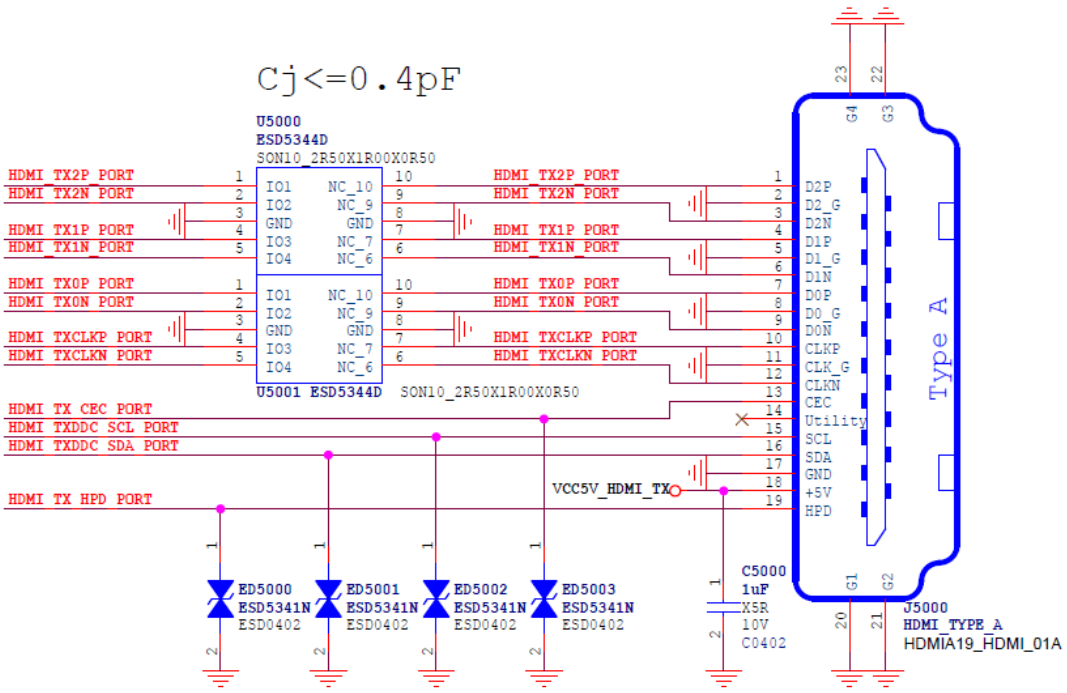


Figure 2-121 ESD circuit of HDMI connector

■ The matching design recommendations of HDMI2.0 TX interface are shown in the following Table.

Table 2–26 RK3568 HDMI2.0 TX interface design

| Signal | Connection mode | Description |
|---|---|---|
| HDMI_TX_D2P/D2N | Connect in series with a 2.2ohm resistor | TMDS data Lane2 output |
| HDMI_TX_D1P/D1N | Connect in series with a 2.2ohm resistor | TMDS data Lane1 output |
| HDMI_TX_D0P/D0N | Connect in series with a 2.2ohm resistor | TMDS data Lane1 output |
| HDMI_TX_CLKP/CLKN | Connect in series with a 2.2ohm resistor<br>Common mode inductor is reserved for EMI suppression | TMDS clock output |
| HDMI_TX_REXT | A 1620/1% ohm resistor grounded | A external reference resistor of HDMI2.0 TX PHY |
| HDMI_TX_HPDIN | Connect in series with a 1000ohm resistor | HDMI IN test |
| HDMITX_CEC | MOS isolation | HDMI CEC signal |
| HDMITX_SCL | MOS level conversion | HDMI DDC clock |
| HDMITX_SDA | MOS level conversion | HDMI DDC data input and output |

### 2.3.10.2 MIPI DSI TX0/LVDS TX interface

RK3568 has a built-in MIPI DSI TX0 and a LVDS TX Combo PHY, it supports version MIPI V1.2 and has total 4Lane. The maximum output resolution of MIPI DSI TX0 is up to 1920×1080@60Hz, and the maximum output resolution of LVDS TX is up to 1280×800@60Hz.

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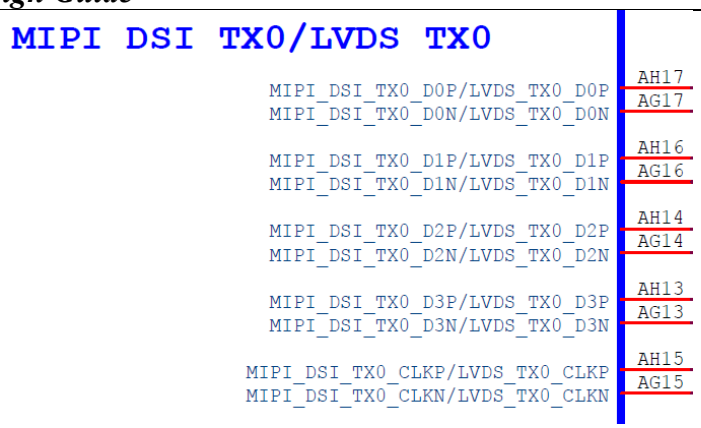


Figure 2-122 RK3568 MIPI DSI TX0/LVDS TX Combo PHY pins

Please note in the design of Mipi DSI tx0 and LVDS TX combo PHY

- It's required to separate MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9, MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 power pins and VDDA0V9_IMAGE, VCCA1V8_IMAGE by magnetic beads. Please refer to schematic design for details;

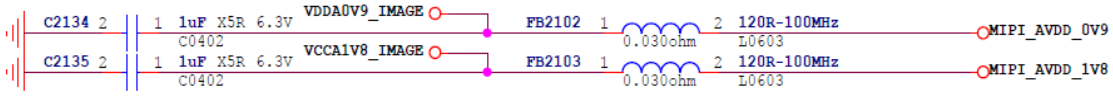


Figure 2-123 Magnetic bead isolation circuit of MIPI DSI PHY power supply

- To improve the performance of MIPI DSI TX0 and LVDS TX Combo PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

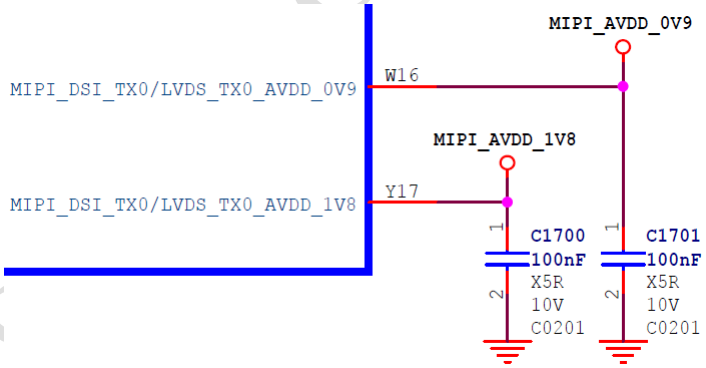


Figure 2-124 RK3568 MIPI DSI TX0/LVDS TX Combo PHY power decoupling capacitors

- The matching design recommendations of MIPI DSI TX0 and LVDS TX Combo PHY interfaces are shown in the following Table.

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Table 2–27 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY interfaces design

| Signal | Connection mode | Description |
|---|---|---|
| MIPI_DSI_TX0_D0P/LVDS_TX0_D0P<br>MIPI_DSI_TX0_D0N/LVDS_TX0_D0N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane0 output or LVDS data Lane0 output |
| MIPI_DSI_TX0_D1P/LVDS_TX0_D1P<br>MIPI_DSI_TX0_D1N/LVDS_TX0_D1N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane1 output or LVDS data Lane1 output |
| MIPI_DSI_TX0_D2P/LVDS_TX0_D2P<br>MIPI_DSI_TX0_D2N/LVDS_TX0_D2N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane2 output or LVDS data Lane2 output |
| MIPI_DSI_TX0_D3P/LVDS_TX0_D3P<br>MIPI_DSI_TX0_D3N/LVDS_TX0_D3N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane3 output or LVDS data Lane3 output |
| MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP<br>MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI clock output or LVDS clock output |

#### 2.3.10.3 MIPI DSI TX1 interface

MIPI DSI TX1 PHY of RK3568 supports version MIPI V1.2 and has total 4Lane. The maximum output resolution of MIPI DSI TX1 is up to 1920X1080@60Hz;

MIPI DSI TX0+MIPI DSI TX1 can support Dual MIPI, and the maximum output resolution is up to 2048X1536@60Hz.

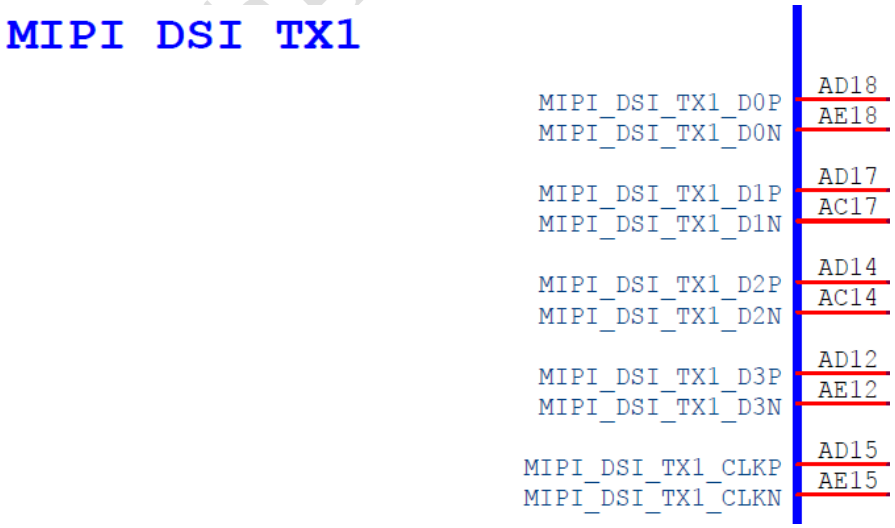


Figure 2-125 RK3568 MIPI DSI TX1 PHY pins

Please note the following items in MIPI DSI TX1 PHY design:

- It's required to separate MIPI_DSI_TX1_AVDD_0V9，MIPI_DSI_TX1_AVDD_1V8 power pins and VDDA0V9_IMAGE, VCCA1V8_IMAGE by magnetic beads. Please refer to schematic design for details;

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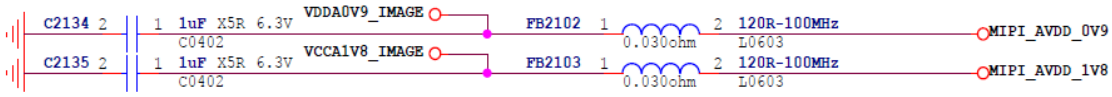


Figure 2-126 Magnetic bead isolation circuit of MIPI DSI TX1 PHY power supply

- To improve the performance of MIPI DSI TX1 PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

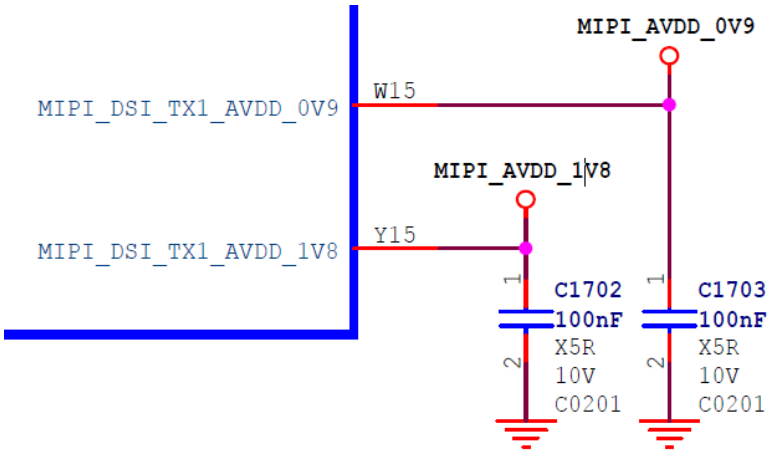


Figure 2-127 RK3568 MIPI DSI TX1 PHY power decoupling capacitors

- The matching design recommendations of MIPI DSI TX1 PHY interfaces are shown in the following Table.

Table 2–28 RK3568 MIPI DSI TX1 PHY interface design

| Signal | Connection mode | Note |
|---|---|---|
| MIPI_DSI_TX1_D0P/D0N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane0 output |
| MIPI_DSI_TX1_D1P/D1N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane1 output |
| MIPI_DSI_TX1_D2P/D2N | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI data Lane2 output |
| MIPI_DSI_TX1_D3P/D3N | Connect directly<br>Common mode inductor is reserved for EMI suppression. | MIPI DSI data Lane3 output |
| MIPI_DSI_TX1_CLKP/CLKN | Connect directly<br>Common mode inductor is reserved for EMI suppression | MIPI DSI clock output |

#### 2.3.10.4 eDP TX interface

The eDP TX PHY of RK3568 supports version eDP V1.3 and has total 4Lane. The maximum output resolution of eDP TX is up to 2560X1600@60Hz.

- Each Lane rate can support to 1.62/2.7Gbps.

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- Support 1Lane or 2Lane or 4Lane mode.
- Support AUX channels with rate up to 1Mbps.

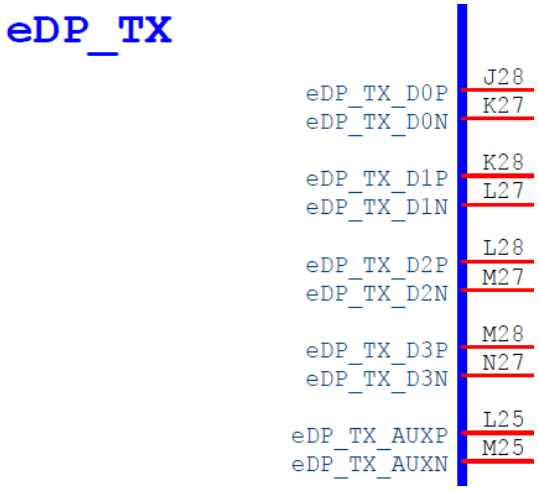


Figure 2-128 RK3568 eDP TX PHY pins

Please note the following items in eDP TX PHY design:

- To improve the performance of eDP TX PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

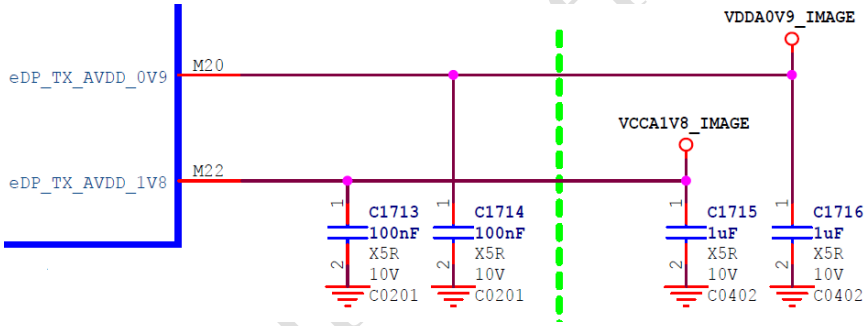


Figure 2-129 Figure 2–2 RK3568 eDP TX PHY power decoupling capacitors

- eDP_TX_D0P/DON, eDP_TX_D1P/D1N, eDP_TX_D2P/D2N and eDP_TX_D3P/D3N need to connect in series to 100nF AC coupling capacitor, and it's recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced. The capacitor should be placed near RK3568 pins when layout.

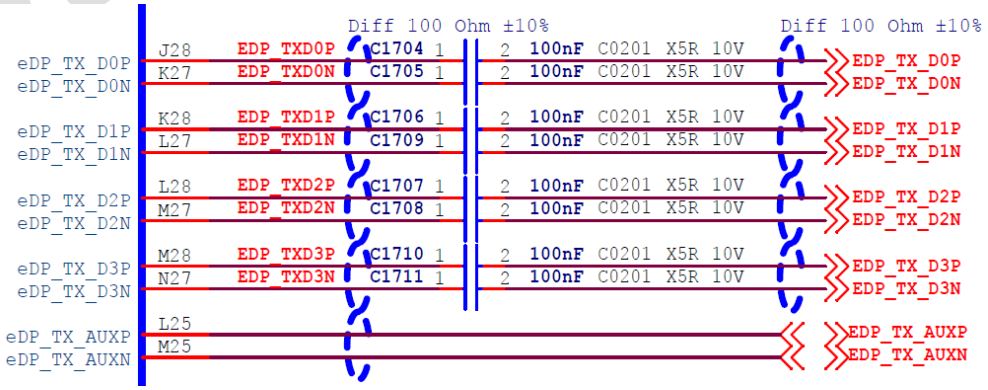


Figure 2-130 RK3568 eDP TX signal AC coupling capacitors

- eDP_TX_AUXP/AUXN need to connect in series to the 100nF AC coupling capacitor near the interface

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end. AUXP requires to reserve a 100K resistor grounded, and 100K resistor of AUXN is reserved and pulls up to 3.3V.

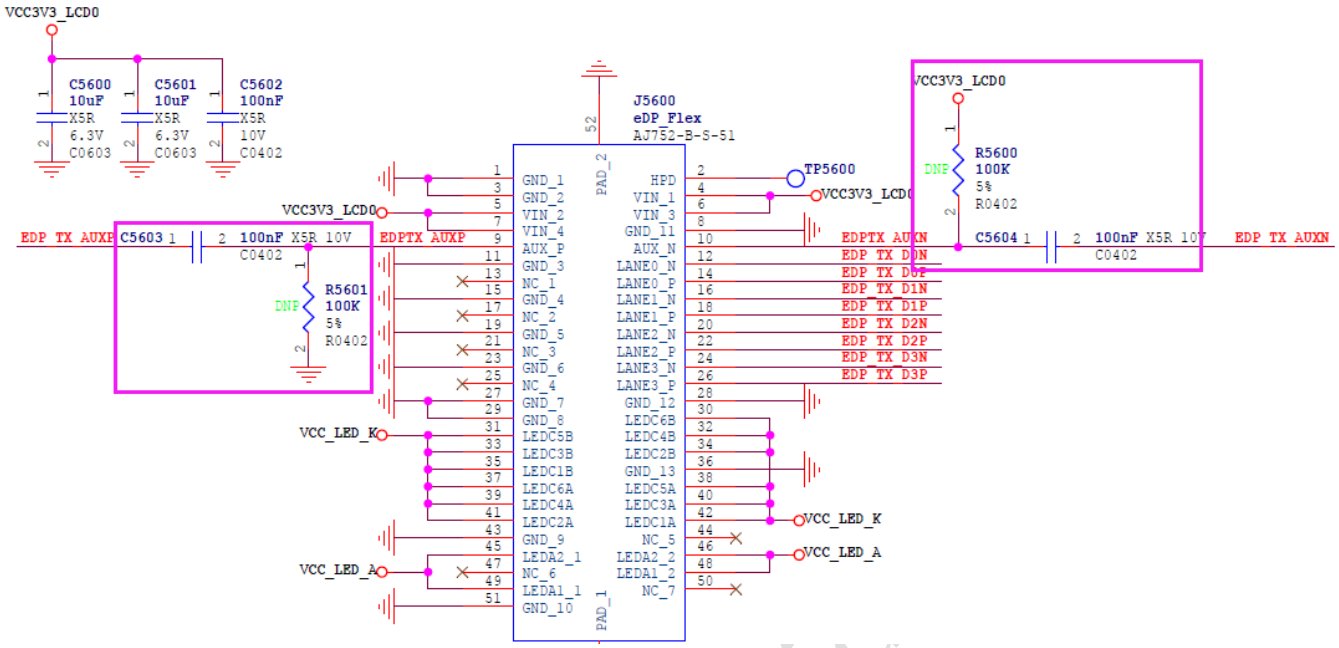


Figure 2-131 RK3568 eDP AUX signal AC coupling capacitors

■ The matching design recommendations of eDP TX PHY interface are shown in the following Table.

Table 2–29 RK3568 eDP TX PHY interface design

| Signal | Connection mode | Description |
|---|---|---|
| eDP_TX_D0P/DON | Connect in series with a 100nf capacitor (the 0201 package is recommended) | eDP data Lane0 output |
| eDP_TX_D1P/D1N | Connect in series with a 100nf capacitor (the 0201 package is recommended) | eDP data Lane1 output |
| eDP_TX_D2P/D2N | Connect in series with a 100nf capacitor (the 0201 package is recommended) | eDP data Lane2 output |
| eDP_TX_D3P/D3N | Connect in series with a 100nf capacitor (the 0201 package is recommended) | eDP data Lane3 output |
| eDP_TX_AUXP/AUXN | Connect in series with a 100nf capacitor | eDP AUX channel |

### 2.3.10.5 RGB TX interface

RK3568 supports parallel 24bit RGB output with maximum output resolution up to 1920X1080@60Hz;

The parallel RGB interface supports the following formats:

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Table 2–30 RK3568 parallel RGB interface formats

| Interface | RGB888 format | RGB666 format | RGB565 format |
|---|---|---|---|
| LCDC_CLK | LCDC_CLK | LCDC_CLK | LCDC_CLK |
| LCDC_HSYNC | LCDC_HSYNC | LCDC_HSYNC | LCDC_HSYNC |
| LCDC_VSYNC | LCDC_VSYNC | LCDC_VSYNC | LCDC_VSYNC |
| LCDC_DEN | LCDC_DEN | LCDC_DEN | LCDC_DEN |
| LCDC_D23 | R7 | R5 | R4 |
| LCDC_D22 | R6 | R4 | R3 |
| LCDC_D21 | R5 | R3 | R2 |
| LCDC_D20 | R4 | R2 | R1 |
| LCDC_D19 | R3 | R1 | R0 |
| LCDC_D18 | R2 | R0 | × |
| LCDC_D17 | R1 | × | × |
| LCDC_D16 | R0 | × | × |
| LCDC_D15 | G7 | G5 | G5 |
| LCDC_D14 | G6 | G4 | G4 |
| LCDC_D13 | G5 | G3 | G3 |
| LCDC_D12 | G4 | G2 | G2 |
| LCDC_D11 | G3 | G1 | G1 |
| LCDC_D10 | G2 | G0 | G0 |
| LCDC_D9 | G1 | × | × |
| LCDC_D8 | G0 | × | × |
| LCDC_D7 | B7 | B5 | B4 |
| LCDC_D6 | B6 | B4 | B3 |
| LCDC_D5 | B5 | B3 | B2 |
| LCDC_D4 | B4 | B2 | B1 |
| LCDC_D3 | B3 | B1 | B0 |
| LCDC_D2 | B2 | B0 | × |
| LCDC_D1 | B1 | × | × |
| LCDC_D0 | B0 | × | × |

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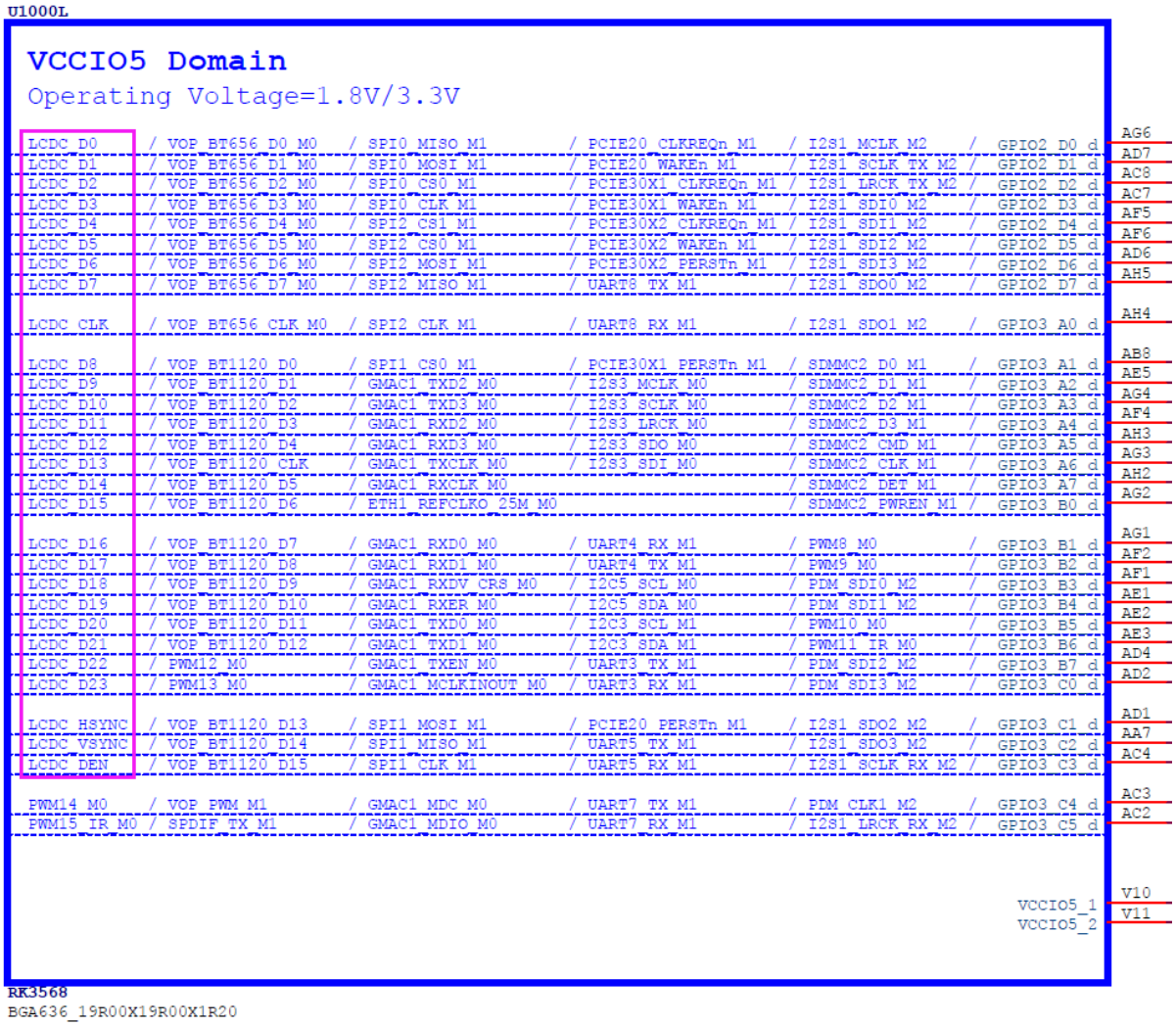


Figure 2-132 RK3568 LCDC functional pins

Please note the following items in parallel RGB interface design:

- Parallel RGB I/O domain supplies power for VCCIO5. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripherals (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve parallel RGB interface performance, the decoupling capacitors of VCCIO5 power supply shouldn't be deleted. Please place them near the pin when layout.

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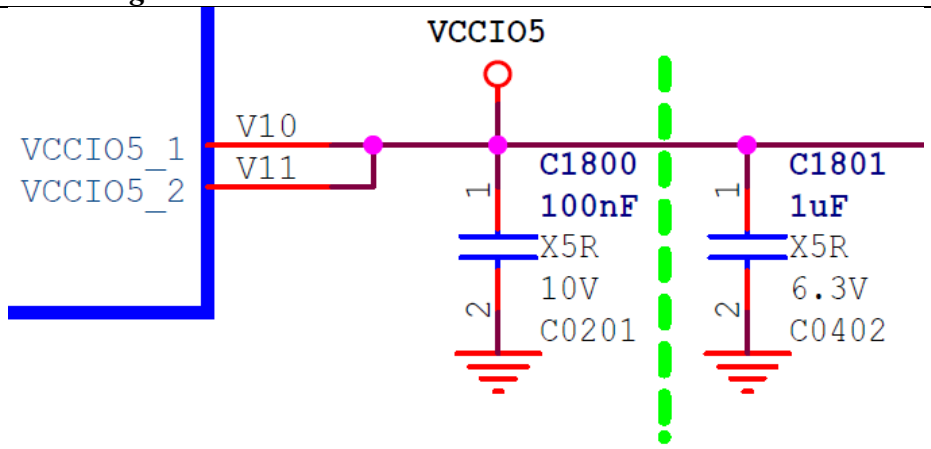


Figure 2-133 The decoupling capacitors of RK3568 VCCIO5 power supply

- The pull up/down and matching design recommendations of parallel RGB interface are shown in the following Table.

Table 2–31 RK3568 parallel RGB interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| LCDC_D[23:0] | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | LCDC data output |
| LCDC_HSYNC | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | LCDC row synchronous output |
| LCDC_VSYNC | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | LCDC field synchronous output |
| LCDC_DEN | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | LCDC data enabling output |
| LCDC_CLK | Pull-down | Connect a 22ohm resistor in series near device end. | LCDC clock output |

- When board to board connection is realized through connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.6 BT1120 TX interface

RK3568 supports 16bit BT1120 output interface with maximum output resolution up to 1920X1080@60Hz;

- Corresponding relationship of BT1120 output interface data, and supports YC Swap.

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Table 2–32 RK3568 BT1120 output formats

| Pin Name | Default format | | Swap open | |
|---|---|---|---|---|
| | Pixel #0 | Pixel #1 | Pixel #0 | Pixel #1 |
| BT1120_D0 | Y0[0] | Y1[0] | Cb0[0] | Cr0[0] |
| BT1120_D1 | Y0[1] | Y1[1] | Cb0[1] | Cr0[1] |
| BT1120_D2 | Y0[2] | Y1[2] | Cb0[2] | Cr0[2] |
| BT1120_D3 | Y0[3] | Y1[3] | Cb0[3] | Cr0[3] |
| BT1120_D4 | Y0[4] | Y1[4] | Cb0[4] | Cr0[4] |
| BT1120_D5 | Y0[5] | Y1[5] | Cb0[5] | Cr0[5] |
| BT1120_D6 | Y0[6] | Y1[6] | Cb0[6] | Cr0[6] |
| BT1120_D7 | Y0[7] | Y1[7] | Cb0[7] | Cr0[7] |
| BT1120_D8 | Cb0[0] | Cr0[0] | Y0[0] | Y1[0] |
| BT1120_D9 | Cb0[1] | Cr0[1] | Y0[1] | Y1[1] |
| BT1120_D10 | Cb0[2] | Cr0[2] | Y0[2] | Y1[2] |
| BT1120_D11 | Cb0[3] | Cr0[3] | Y0[3] | Y1[3] |
| BT1120_D12 | Cb0[4] | Cr0[4] | Y0[4] | Y1[4] |
| BT1120_D13 | Cb0[5] | Cr0[5] | Y0[5] | Y1[5] |
| BT1120_D14 | Cb0[6] | Cr0[6] | Y0[6] | Y1[6] |
| BT1120_D15 | Cb0[7] | Cr0[7] | Y0[7] | Y1[7] |

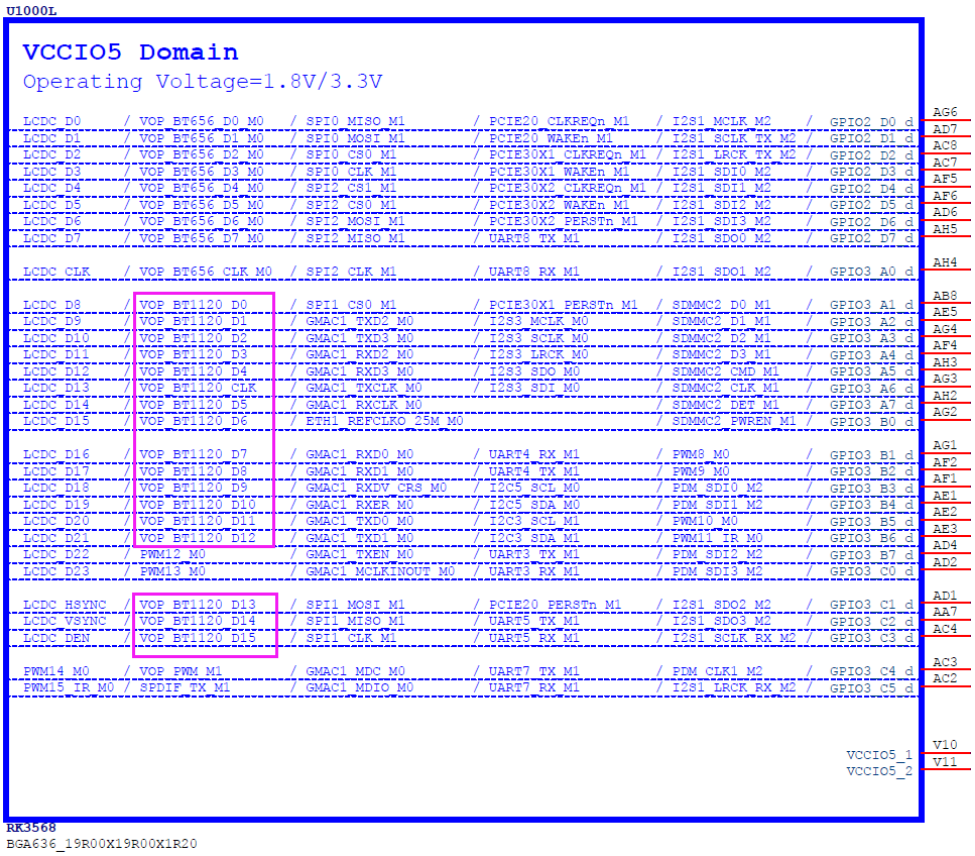


Figure 2-134 RK3568 VOP BT1120 functional pins

Please note the following items in BT1120 output interface design:

- BT1120 output I/O domain supplies power for VCCIO5. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.

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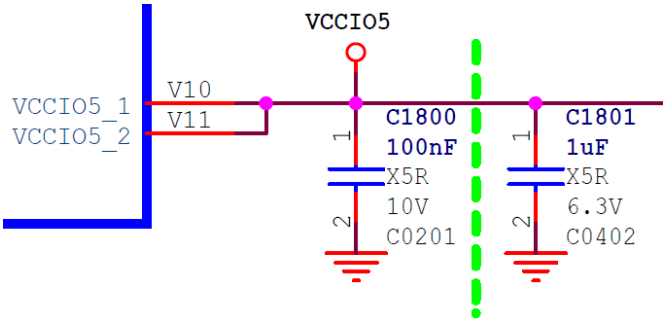
- In order to improve BT1120 output interface performance, the decoupling capacitors of VCCIO5 power supply should not be deleted. Please place them near the pin when layout.




- The pull up/down and matching design recommendations of BT1120 output interface are shown in the following Table.

Table 2–33 RK3568 BT1120 output interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| VOP_BT1120_D[15:0] | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | BT1120 data output |
| VOP_BT1120_CLK | Pull-down | Connect a 22ohm resistor in series near device end. | BT1120 clock output |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.7 BT656 TX interface

RK3568 supports 8bit BT656 output interface and PAL and NTSC, VOP_BT656 interface multiplexes to two power domains, _M0 of VCCIO5 and _M1 of VCCIO6. When selecting, the whole group _M0 or the whole group _M1 is selected, instead of mixing.

- VOP BT656 multiplexes in the interface of VCCIO5 power domain.

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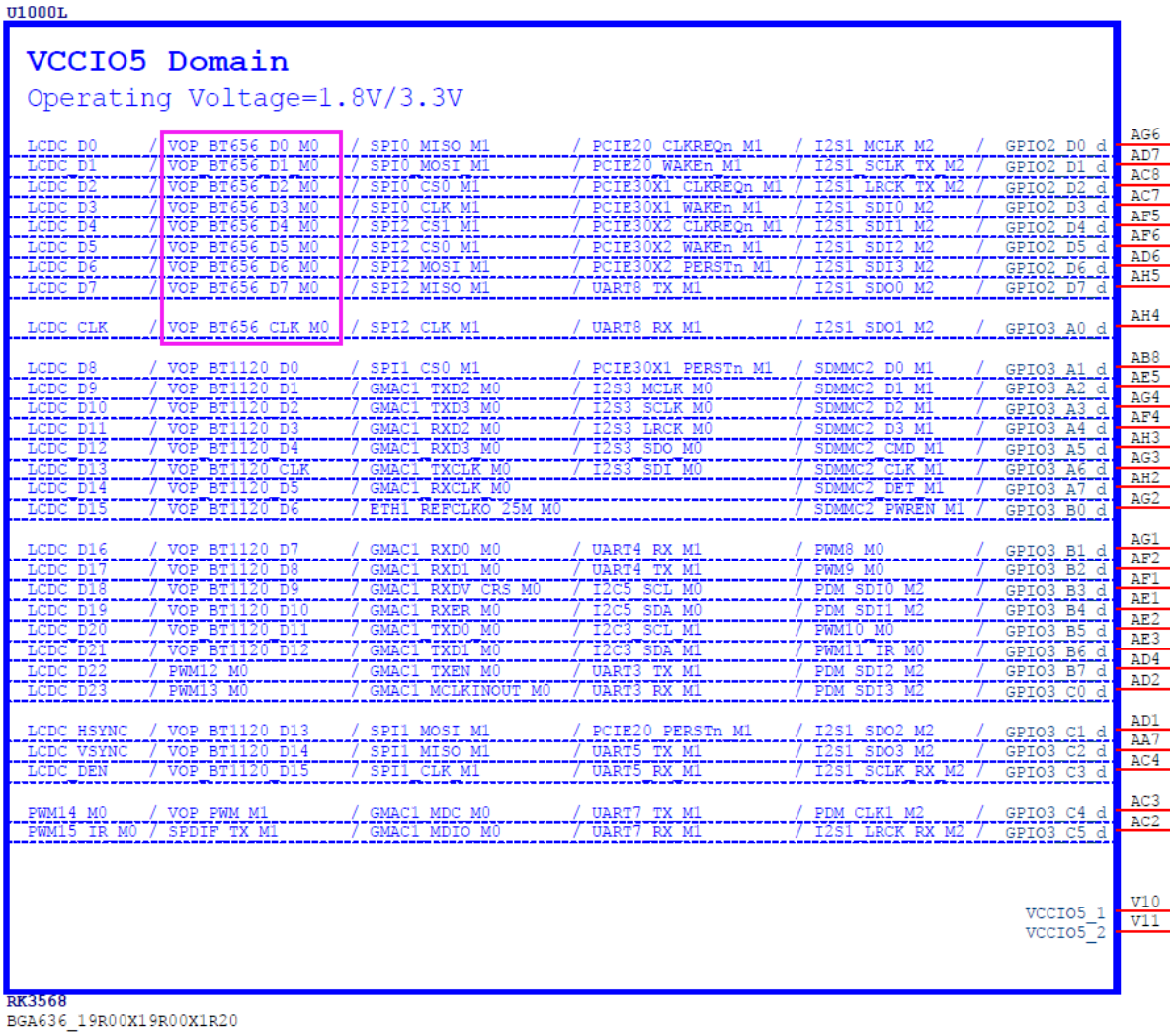


Figure 2-135 RK3568 VOP BT656 M0 functional pins

- VOP BT656 multiplexes in the interface of VCCIO6 power domain.

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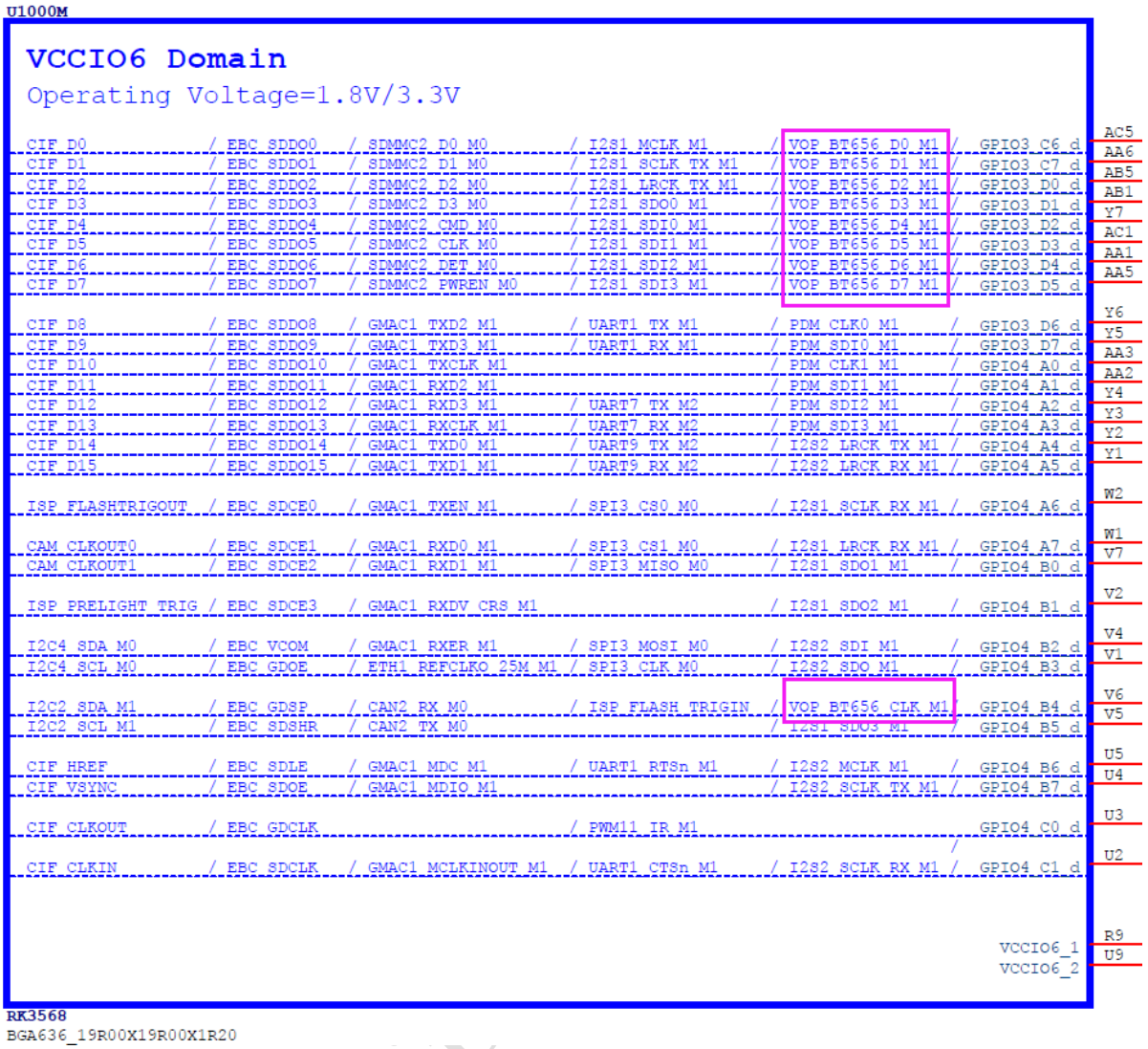


Figure 2-136 RK3568 VOP BT656 M1 functional pins

Please note the following items in BT656 output interface design:

- BT656 M0 output I/O domain supplies power for VCCIO5.In the actual design of products, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral(1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.
- BT656 M1 output I/O domain supplies power for VCCIO6. In the actual design of products, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve BT656 output interface performance, the decoupling capacitors of VCCIO5 or VCCIO6 power supply should not be deleted. Please place them near the pin when layout.

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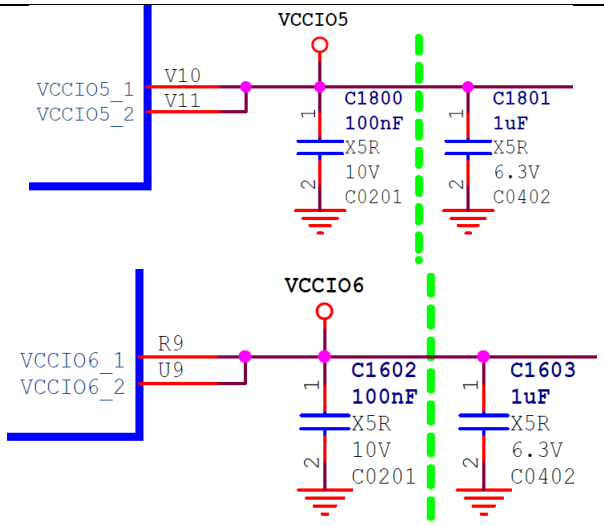


- The pull up/down and matching design recommendations of BT656 output interface are shown in the following Table.

Table 2–34 RK3568 BT656 output interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| VOP_BT656_D[7:0] | Pull-down | Direct connection, it's recommended to reserve a series resistor near chip end. | BT656 data output |
| VOP_BT656_CLK | Pull-down | Connect a 22ohm resistor in series near device end. | BT656 clock output |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.8 EBC TX interface

RK3568 has an EBC interface. EBC is a TCON module used to drive E-ink screen. It supports 8bit/16bit output and EBC interface multiplexes to VCCIO6 power domain.

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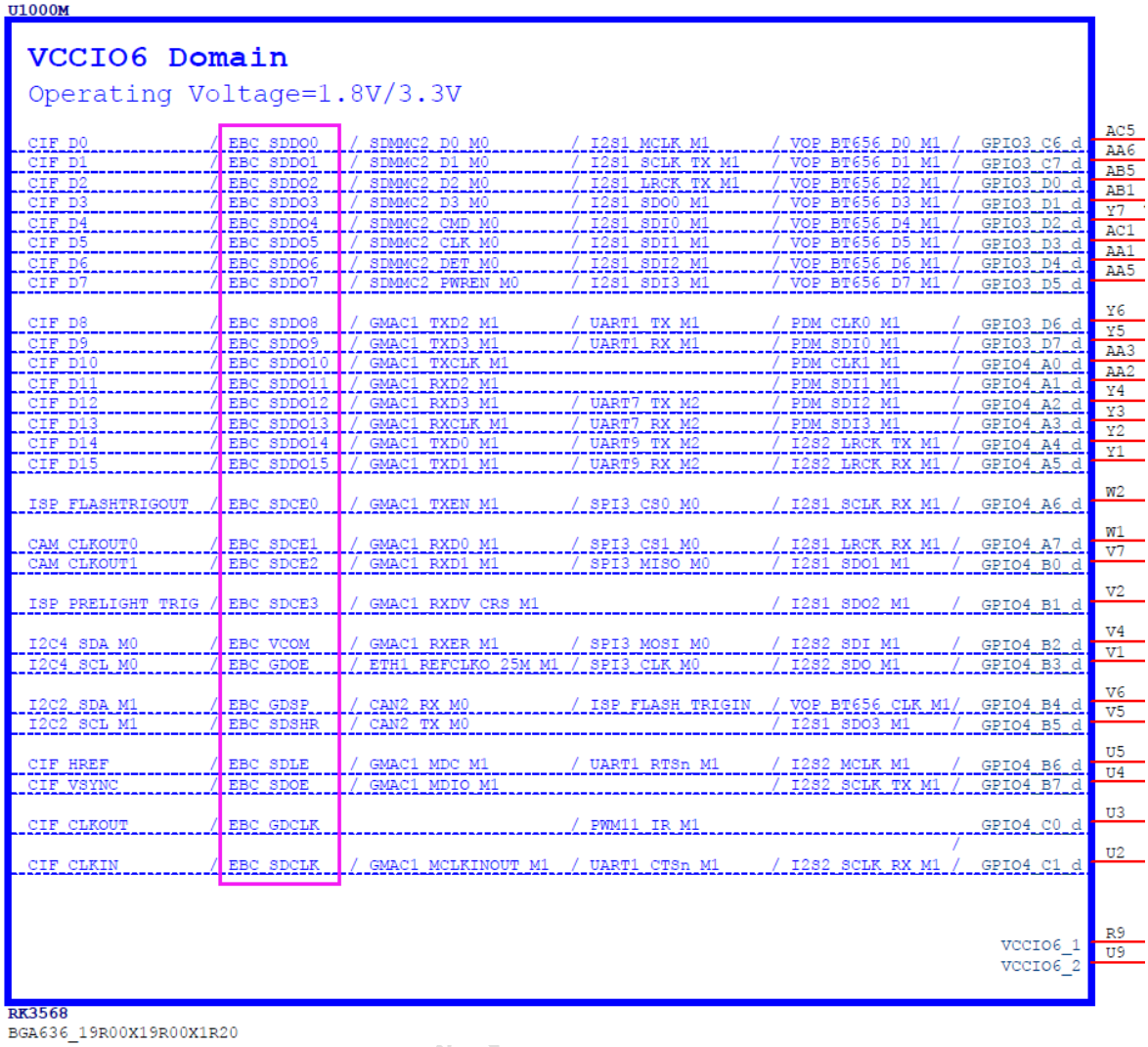


Figure 2-137 RK3568 EBC functional pins

Please note the following items in EBC output interface design:

- EBC output interface domain supplies power for VCCIO6. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve EBC output interface performance, the decoupling capacitors of VCCIO6 power supply should not be deleted. Please place it near the pin when layout.

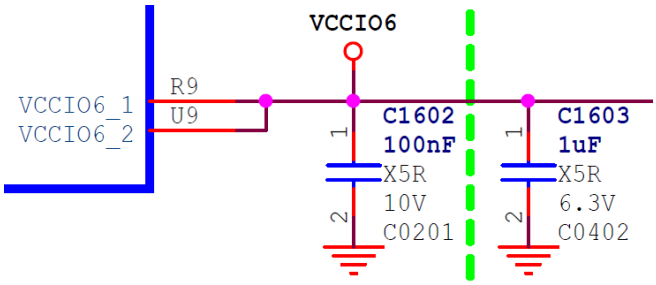


Figure 2-138 The decoupling capacitors of RK3568 VCCIO6 power supply

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- The pull up/down and matching design recommendations of EBC output interface are shown in the following Table.

Table 2–35 RK3568 EBC output interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| EBC_SDDO[15:0] | Pull-down | Direct connection | Source driver data output |
| EBC_SDCE[3:0] | Pull-down | Direct connection | Source chip select/ Start pulse source driver |
| EBC_VCOM | Pull-down | Direct connection | Com voltage control |
| EBC_GDOE | Pull-down | Direct connection | Gate output enable |
| EBC_GDSP | Pull-down | Direct connection | Gate start pulse |
| EBC_SDSHR | Pull-down | Direct connection | Source driven shift register |
| EBC_SDLE | Pull-down | Direct connection | Source data latch enable |
| EBC_SDOE | Pull-down | Direct connection | Source data output enable |
| EBC_GDCLK | Pull-down | Direct connection | Gate driver clock |
| EBC_SDCLK | Pull-down | Direct connection | Source driver clock |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.9 Pay attention to the following items in LCD screen and touch screen design

- Please choose a resistor with 1% accuracy for FB end limiting resistor of LED backlight boost IC, and choose an appropriate package size according to power requirements.
- Please choose the GPIO pulled-down internal and connected to pull-down resistor external for EN/PWM pin of LED backlight boost IC, in order to avoid the flash screen when power on.
- Please choose a filter capacitor with appropriate rated voltage for the drive voltage output of LED backlight.
- Please choose an appropriate model according to working current for the schottky diode of LED backlight boost circuit, and pay attention to the reverse breakdown voltage of the diode, in order to avoid the reverse breakdown when there is no load.
- Please match the inductance, saturation current, DCR, etc. according to actual model for the inductance of LED backlight boost circuit.
- The signal level of screen and touch screen should match IO drive level of the chip, such as RST/ Stand by signal and so on.
- The power supply of screen must be controllable. It is not provided by default when power on.
- The decoupling capacitors of screen and touch screen shall not be deleted, but must be retained.
- I2C bus of TP must add 2.2K and pull up to VCC3V3_TP power supply. It is recommended not to share the bus with other devices. If you must share the bus, pay attention to whether the pull-up power supply and the address conflict or not.

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- For TP ICs with Charge pump, please note rated voltage of capacitors.
- For the screen, when it connects to the board by FPC, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.
- It is recommended to reserve common-mode inductance at the interface of serial interface screen.

#### 2.3.10.10 Please note the following items in VGA interface design

RK3568 itself doesn't support VGA OUT directly, it needs an external conversion chip, you can choose RGB888, HDMI, MIPI, eDP and other interfaces to change to VGA output. Here we mainly describe the related points of using RTD2166.

- The decoupling capacitors of each power supply pin shall not be deleted, and must be retained.
- Pay attention to the requirements of power on sequence.
- If there is a RESET signal in the conversion chip, then it must be controlled by RK3568 GPIO, and the level of RK3568 GPIO must match the IO level of conversion chip. The 100nF capacitor of RESET signal cannot be deleted. Place it near the pin of conversion chip to enhance anti ESD capability.
- RTD2166 Pin32 HPD, 100Kohm resistor grounded should not be deleted.
- RTD2166 peripheral circuit must refer to the reference design circuit directly.
- VGA_HSYNC/VSYNC should support 5V level, and Pin17 must provide a 5V power supply.
- VGA_R/G/B needs to pull down by a 75ohm/1% resistor with 1% accuracy, which cannot be deleted.
- VGA R/G/B filter circuit needs to refer to the requirements of each conversion chip.
- All signals of VGA connector must be added TVS tubes, which should be placed as close as possible to the VGA connector.

### 2.3.11 Audio Interface Circuit

RK3568 has 4 I2S controllers.

- I2S0 controller:
  - Support 8 channels TX and 8 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - It is used by HDMI2.0TX PHY internally in the chip, and the part which isn't multiplexed to IO is used externally.
- I2S1 controller:
  - Support 8 channels TX and 8 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S, PCM and TDM modes.
  - I2S format supports normal, left-aligned and right-aligned formats.

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- PCM format supports early, late1, late2, late3.
- TDM format supports normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift and right shift mode.
- I2S, PCM and TDM modes cannot be used at the same time.

- I2S2 controller:
  - Support 2 channels TX and 2 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S and PCM modes.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - PCM format supports early, late1, late2, late3.
  - I2S and PCM modes cannot be used at the same time.
- I2S3 controller:
  - Support 2 channels TX and 2 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S and PCM modes.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - PCM format supports early, late1, late2, late3.
  - I2S and PCM modes cannot be used at the same time.

RK3568 has 1 PDM controller.

- Support up to 8 channels.
- Bit rate is from 16bits to 24bits.
- Maximum sampling rate is 192 kHz.
- Support master receive mode.

RK3568 has 1 S/PDIF controller.

- Support two 16bit audio data which is saved in the location with 32-bit space.
- Support two phase format stereo audio data output.
- Support 16-bit to 31-bit audio data left-aligned or right-aligned in 32-bit sampled data buffers.
- Support 16-bit, 20-bit and 24-bit audio data transmission in linear PCM mode.
- Support nonlinear PCM transmission.

Connection diagram of I2S playback and record in Master and slave modes.

- RK3568 in Master mode:

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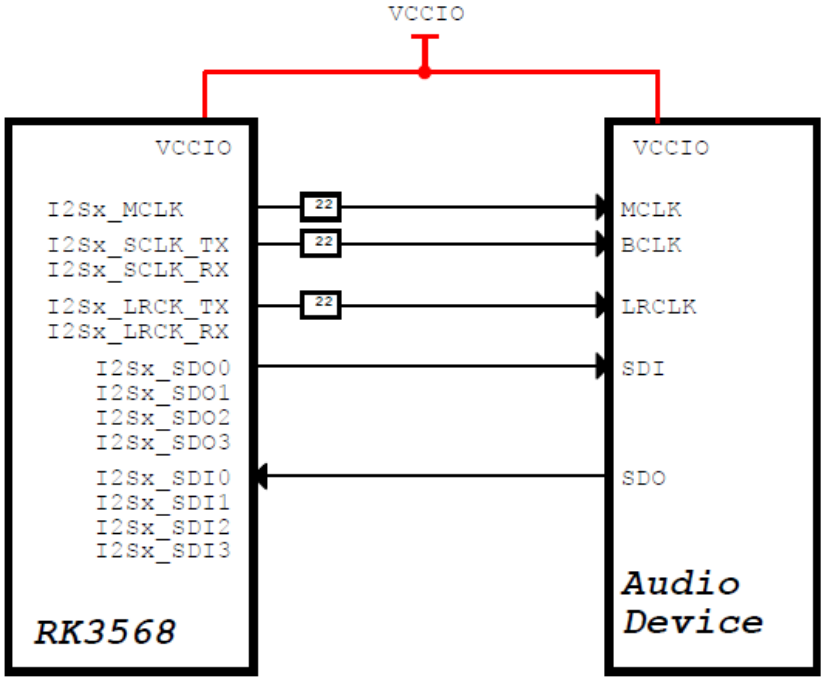


Figure 2-139 Connection diagram of RK3568 I2S in Master mode

- RK3568 in Slave mode:

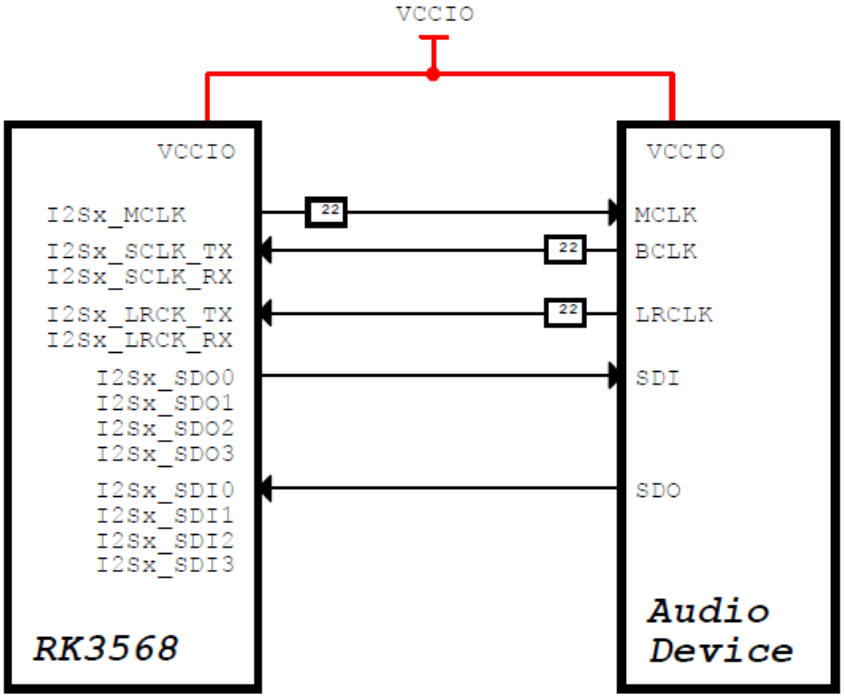


Figure 2-140 Connection diagram of RK3568 I2S in Slave mode

#### 2.3.11.1 I2S1 Interface

I2S1 interface contains independent 8-channel output and 8-channel input. In order to meet the requirements of asynchronous sampling rate of playback and record, two groups (SCLK_TX\LRCK_TX, SCLK_RX\LRCK_RX) of bit clock and frame clock are also provided correspondingly. Note that if SDOx and SDIx refer to only one group of bit/frame clock, SCLK_TX\LRCK_TX is preferred as their common clock.

I2S1 interface pins multiplex in three different power domains:

- I2S1_M0 is multiplexed in the VCCIO1 power domain, the multiplexing relationship is optimized

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according to the frequently used scene, in which three SD0x and SDIx signals are multiplexed together and allocated according to the actual scene demand.

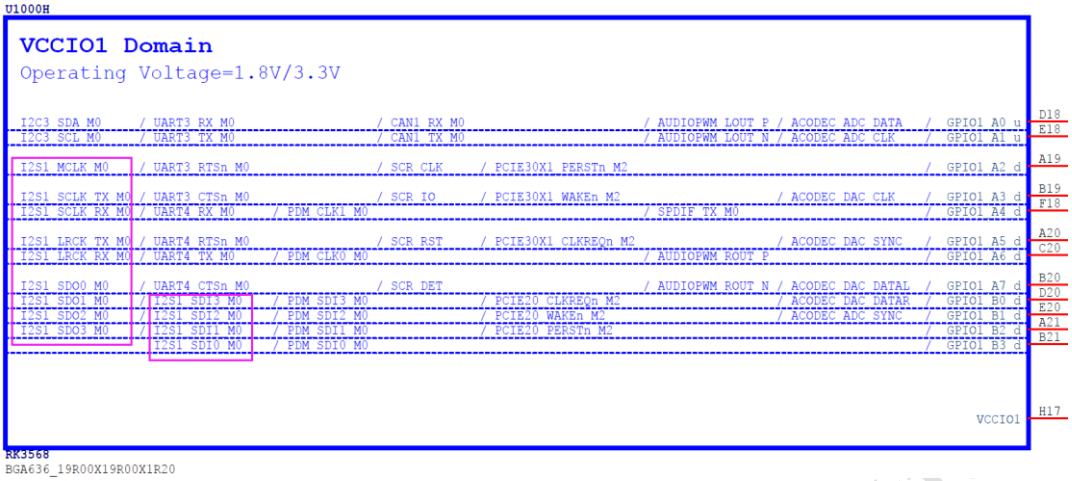


Figure 2-141 RK3568 I2S1 M0 functional pins

- I2S1_M1 is multiplexed in VCCIO6 power domain, and it can support the whole 8CH TX and 8CH RX.

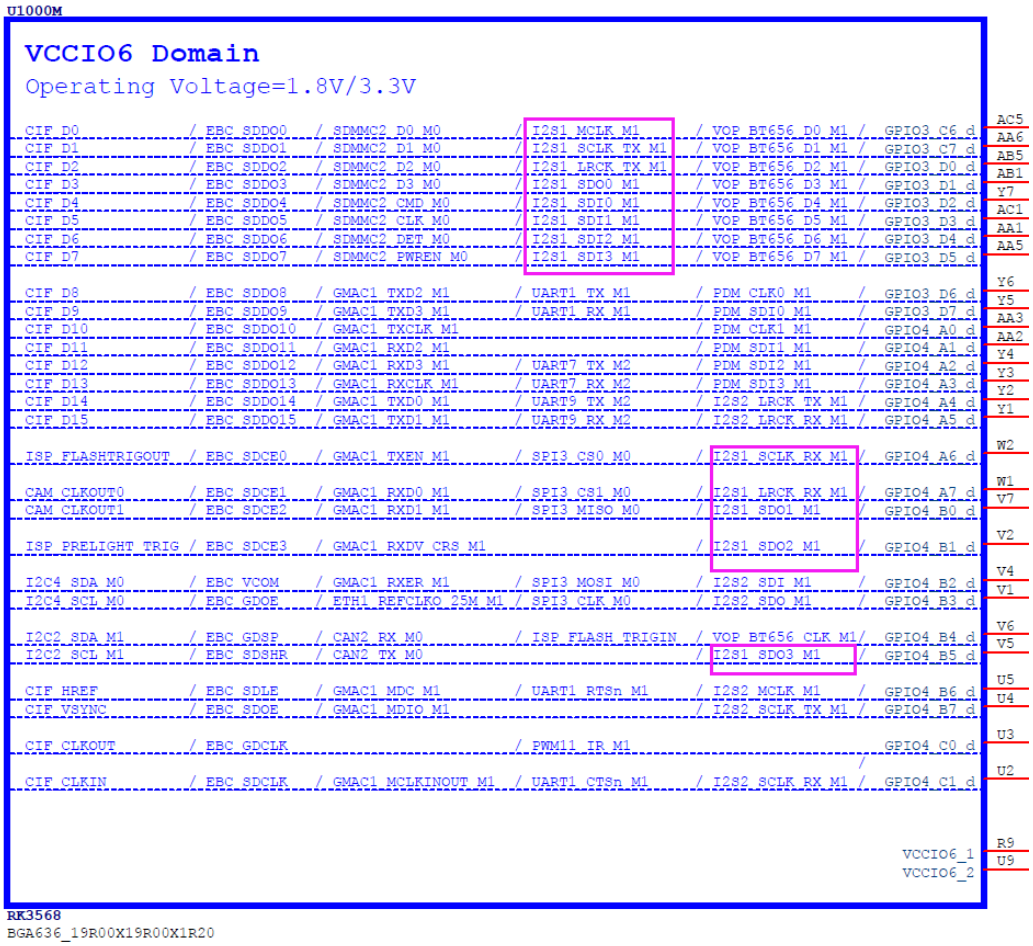


Figure 2-142 RK3568 I2S1 M1 functional pins

- I2S1_M2 is multiplexed in VCCIO5 power domain, and it can support the whole 8CH TX and 8CH RX.

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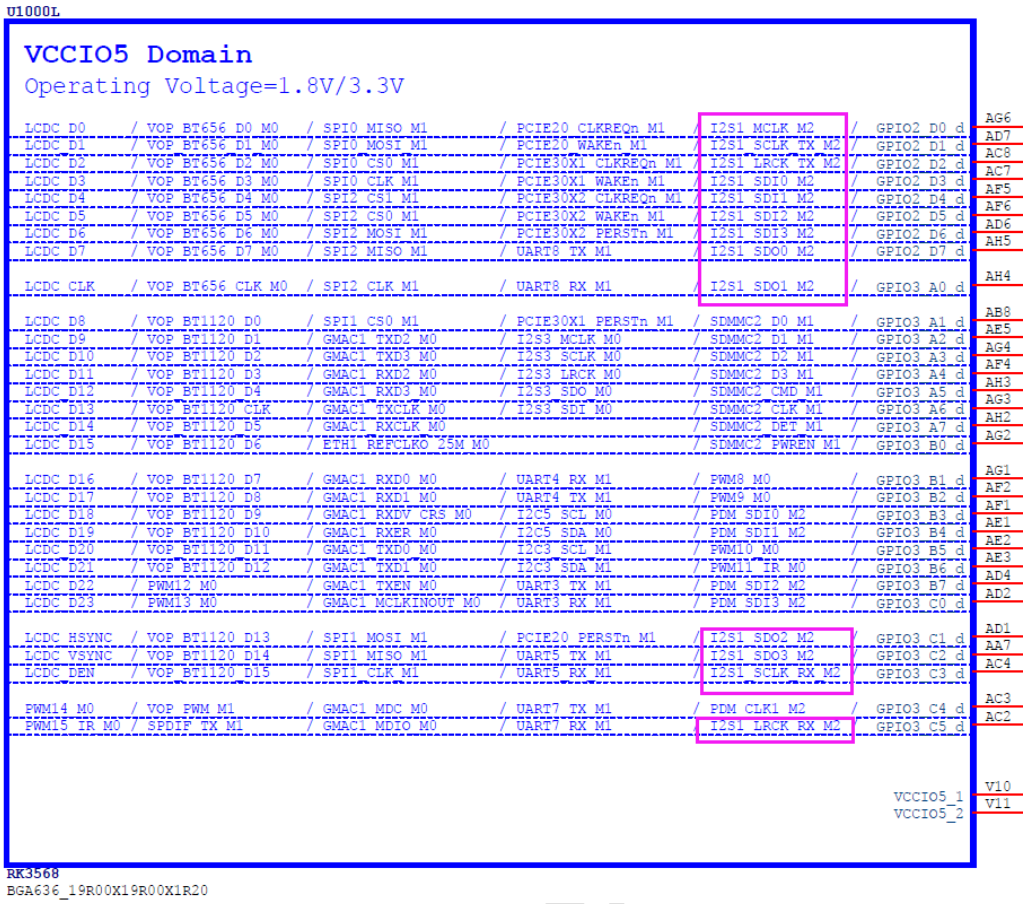


Figure 2-143 RK3568 I2S1 M2 functional pins

In I2S1 interface design, please note:

- I2S1_M0, I2S1_M1 and I2S1_M2 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 or M2 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve I2S1 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S1 interface are shown in the following Table.

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Table 2–36 RK3568 I2S1 interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| I2S1_MCLK | Pull-down | Connect a 22ohm resistor in series | I2S system clock output |
| I2S1_SCLK_TX | Pull-down | Connect a 22ohm resistor in series | I2S continuous SCLK (TX，related AudioPlay) |
| I2S1_LRCK_TX | Pull-down | Connect a 22ohm resistor in series | I2S frame clock for channel selection (TX，related AudioPlay) |
| I2S1_SDO[3:0] | Pull-down | Direct connection | I2S serial data |
| I2S1_SCLK_RX | Pull-down | Connect a 22ohm resistor in series | I2S continuous SCLK (RX，related AudioRecord) |
| I2S1_LRCK_RX | Pull-down | Connect a 22ohm resistor in series | I2S frame clock for channel selection (RX，related AudioRecord) |
| I2S1_SDI[3:0] | Pull-down | Direct connection | I2S serial data |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.2 I2S2 interface

I2S2 interface contains independent 2-channel output and 2-channel input. In order to meet the requirements of asynchronous sampling rate of playback and record, two groups (SCLK_TX\LRCK_TX, SCLK_RX\LRCK_RX) of bit clock and frame clock are also provided correspondingly. Note that if SDOx and SDIx refer to only one group of bit/frame clock, SCLK_TX\LRCK_TX is preferred as their common clock.

I2S2 interface pins multiplex in two different power domains:

- I2S2_M0 is multiplexed in the VCCIO4 power domain.

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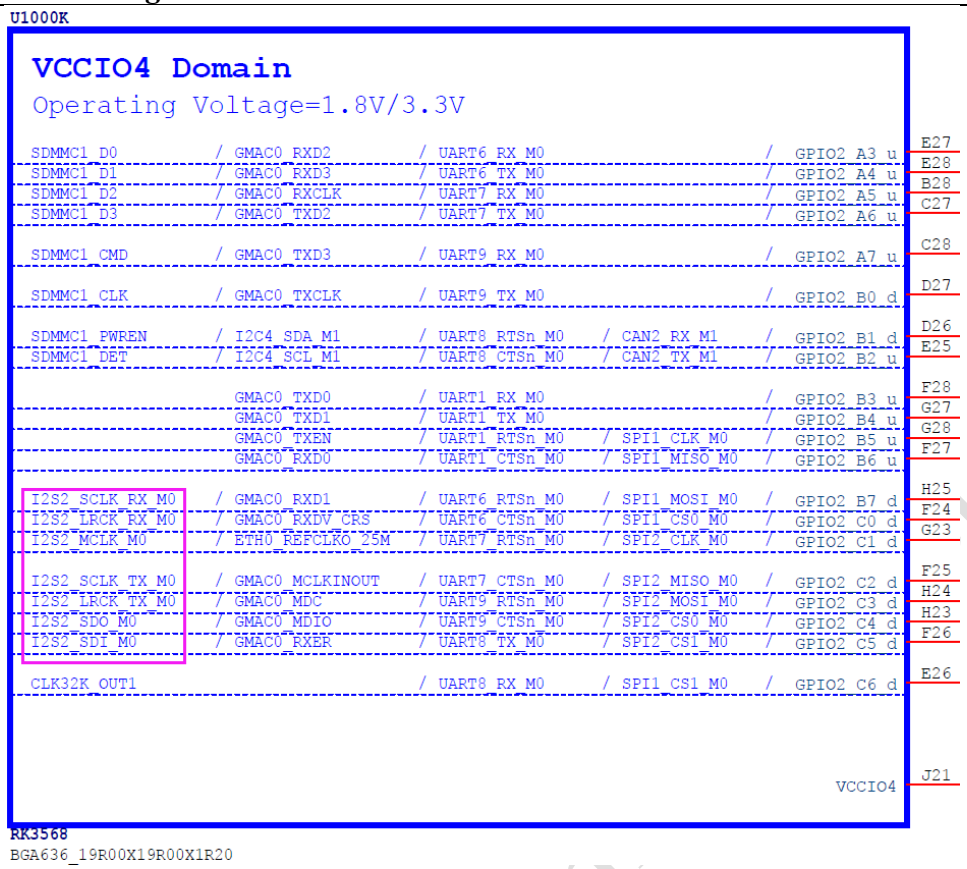


Figure 2-144 RK3568 I2S2 M0 functional pins

- I2S2_M1 is multiplexed in the VCCIO6 power domain.

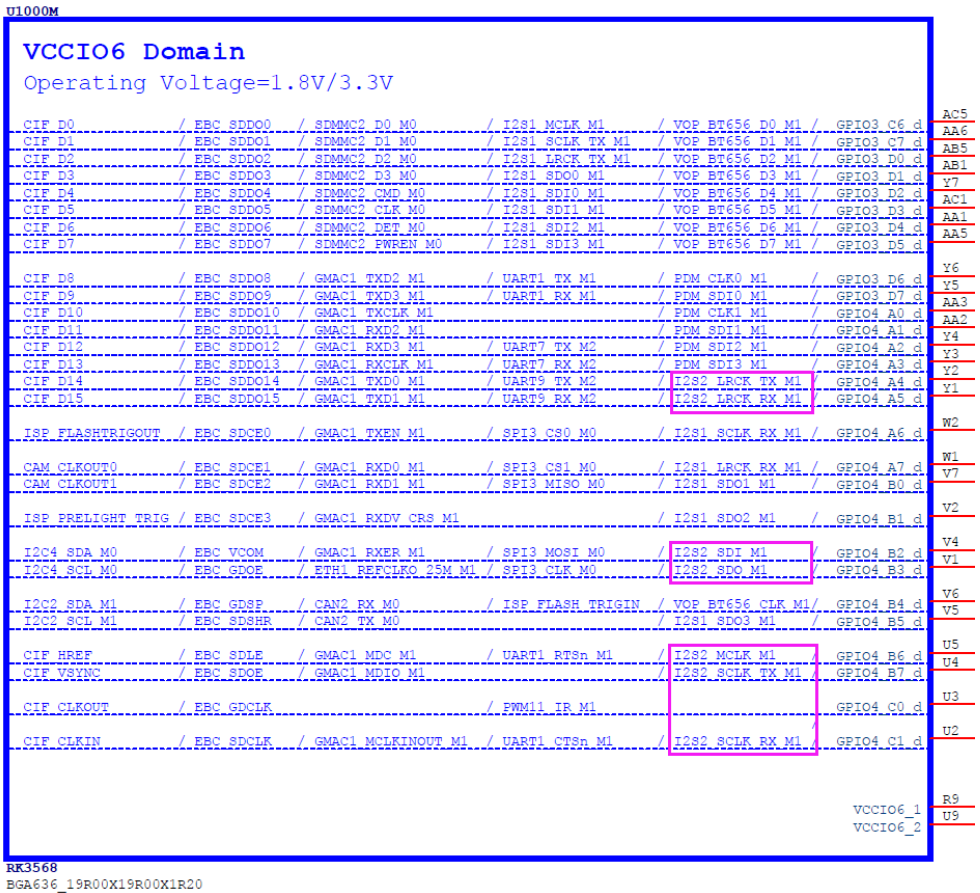


Figure 2-145 RK3568 I2S2 M1 functional pins

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In I2S2 interface design, please note:

- I2S2_M0 and I2S2_M1 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve I2S2 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S2 interface are shown in the following Table.

Table 2–37 RK3568 I2S2 interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| I2S2_MCLK | Pull-down | Connect a 22ohm resistor in series | I2S system clock output |
| I2S2_SCLK_TX | Pull-down | Connect a 22ohm resistor in series | I2S continuous SCLK (TX，related AudioPlay) |
| I2S2_LRCK_TX | Pull-down | Connect a 22ohm resistor in series | I2S frame clock for channel selection (TX，related AudioPlay) |
| I2S2_SDO | Pull-down | Direct connection | I2S serial data |
| I2S2_SCLK_RX | Pull-down | Connect a 22ohm resistor in series | I2S continuous SCLK (RX，related AudioRecord) |
| I2S2_LRCK_RX | Pull-down | Connect a 22ohm resistor in series | I2S frame clock for channel selection (RX，related AudioRecord) |
| I2S2_SDI | Pull-down | Direct connection | I2S serial data |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.3 I2S3 interface

I2S3 interface contains independent 2-channel output and 2-channel input. This group only supports the same sampling rate of playback and record.

I2S3 interface pins multiplex in two different power domains:

- I2S3_M0 is multiplexed in the VCCIO5 power domain.

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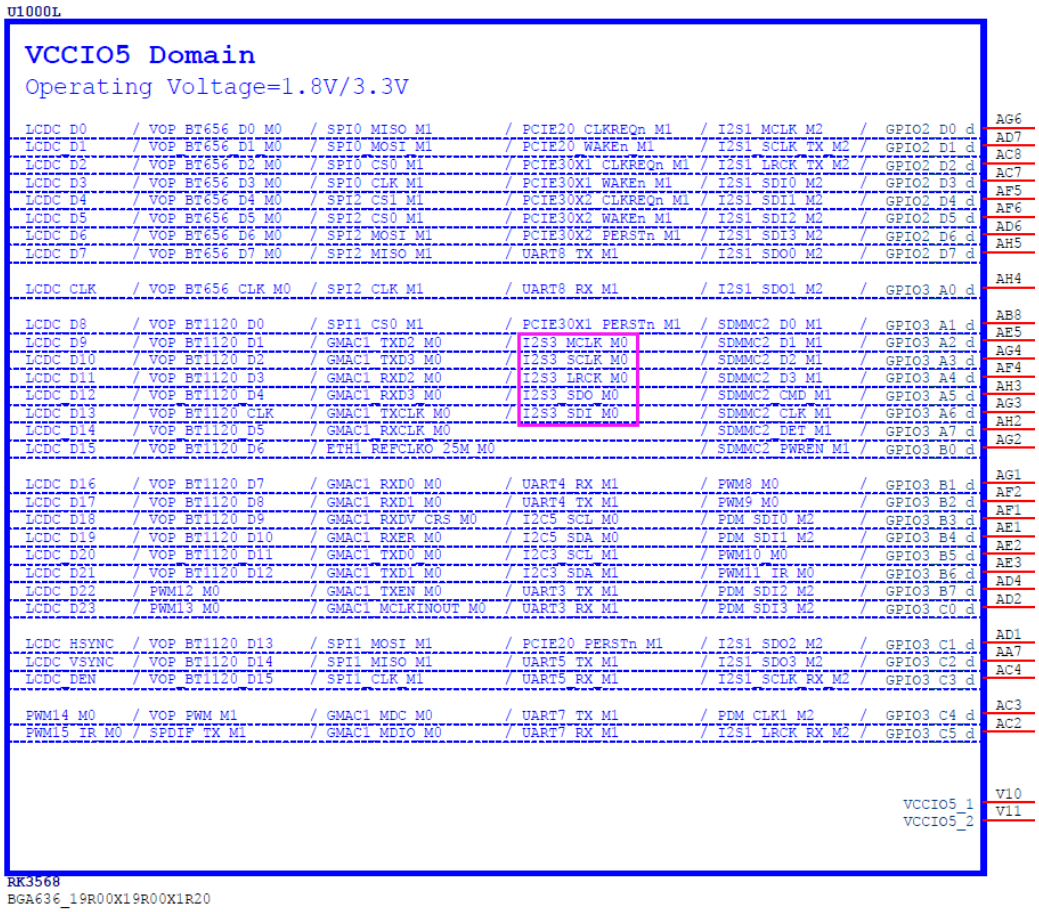


Figure 2-146 RK3568 I2S3 M0 functional pins

- I2S3_M1 is multiplexed in VCCIO7 power domain

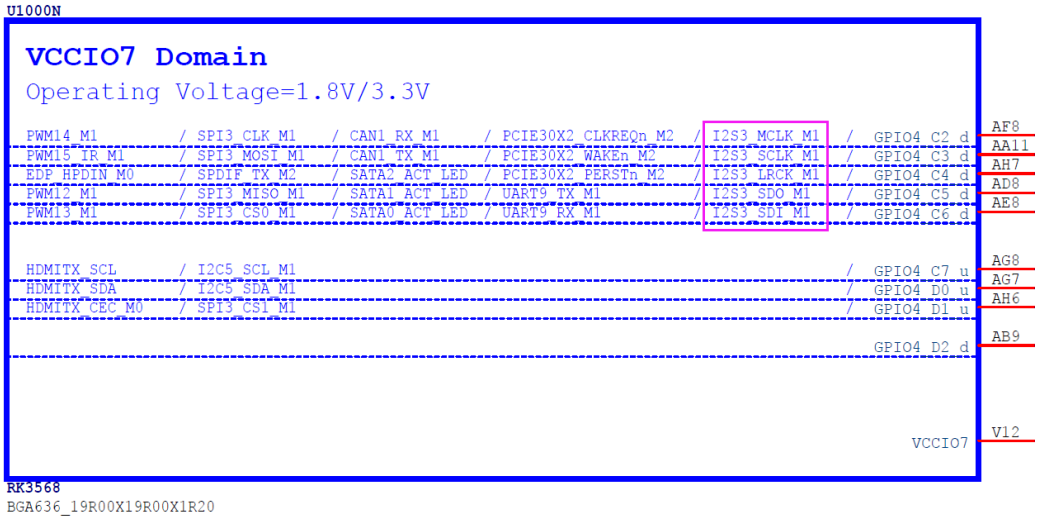


Figure 2-147 RK3568 I2S3 M1 functional pins

In I2S3 interface design, please note:

- I2S3_M0 and I2S3_M1 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and

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they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.

- In order to improve I2S3 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S3 interface are shown in the following Table.

Table 2–38 RK3568 I2S3 interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| I2S3_MCLK | Pull-down | Connect a 22ohm resistor in series | I2S system clock output |
| I2S3_SCLK | Pull-down | Connect a 22ohm resistor in series | I2S continuous SCLK |
| I2S3_LRCK | Pull-down | Connect a 22ohm resistor in series | I2S frame clock for channel selection |
| I2S3_SDO | Pull-down | Direct connection | I2S serial data |
| I2S3_SDI | Pull-down | Direct connection | I2S serial data |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.4 PDM interface

RK3568 provides a group of PDM digital audio interface, and supports up to 8-channel PDM format audio input, the maximum sampling rate is 192kHz, and the bit rate is from 16bits to 32bits, in order to improve the effect caused by clock PCB routing. There are two PDM clocks of the same clock source and phase.

PDM interface pins multiplex in three different power domains:

- PDM_M0 is multiplexed in the VCCIO1 power domain.

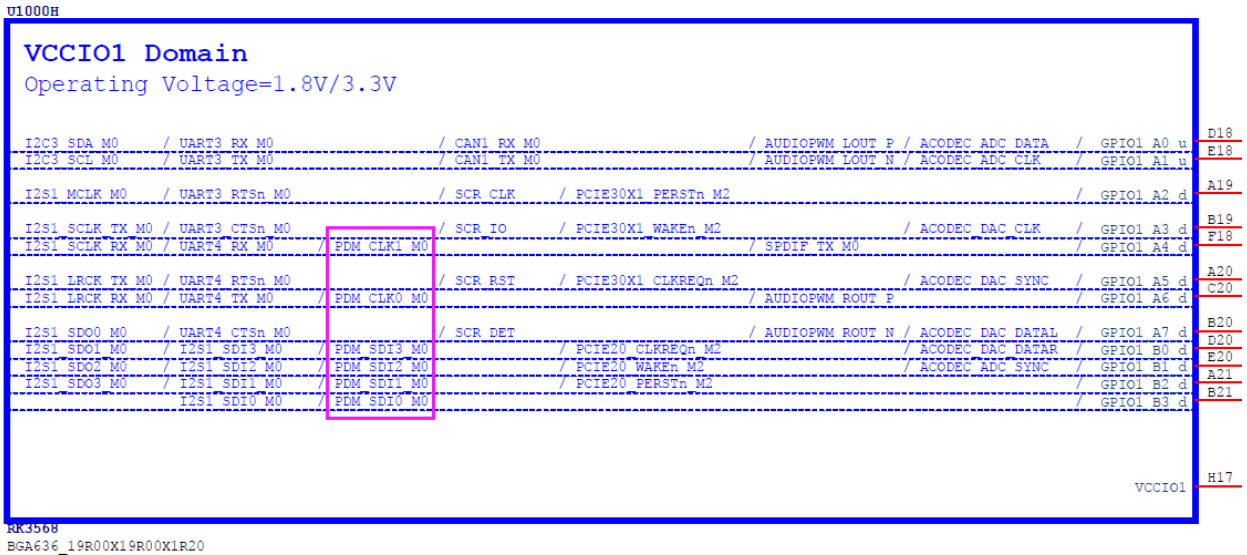


Figure 2-148 RK3568 PDM M0 functional pins

- PDM_M1 is multiplexed in the VCCIO6 power domain.

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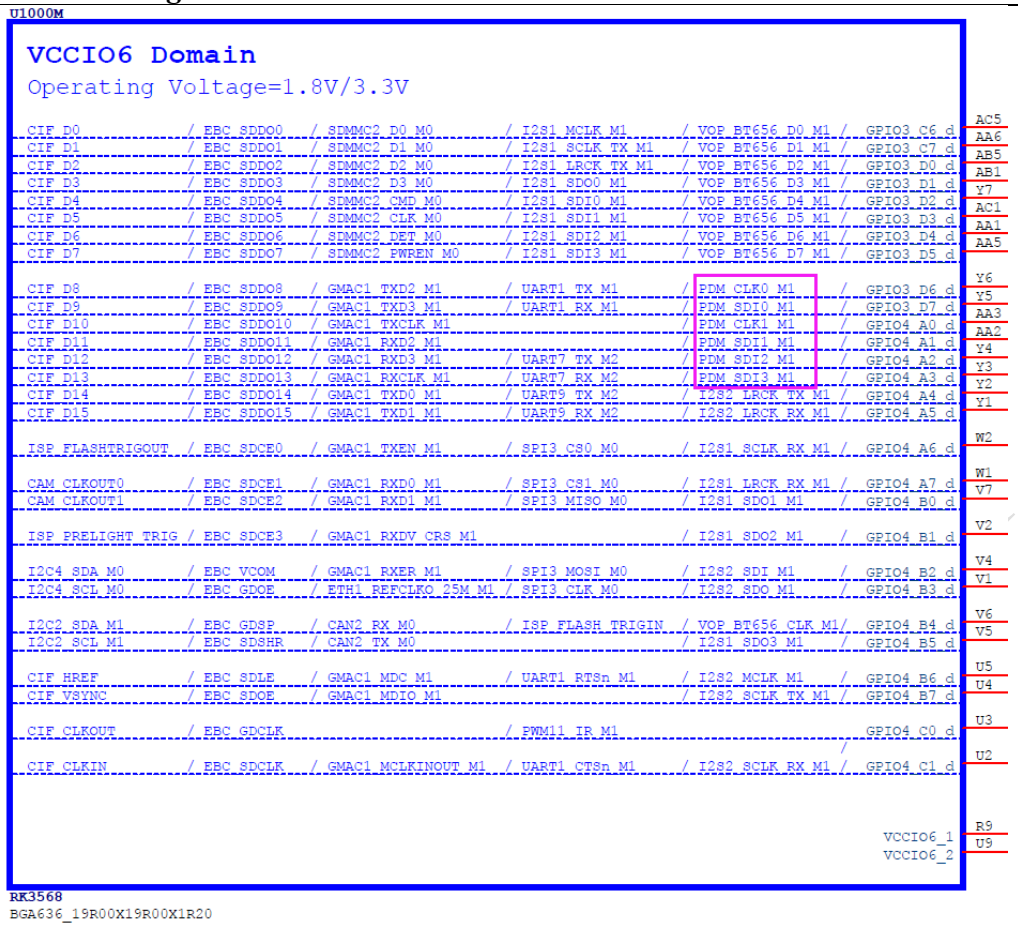


Figure 2-149 RK3568 PDM M1 functional pins

- PDM_M2 is multiplexed in the VCCIO5 power domain.

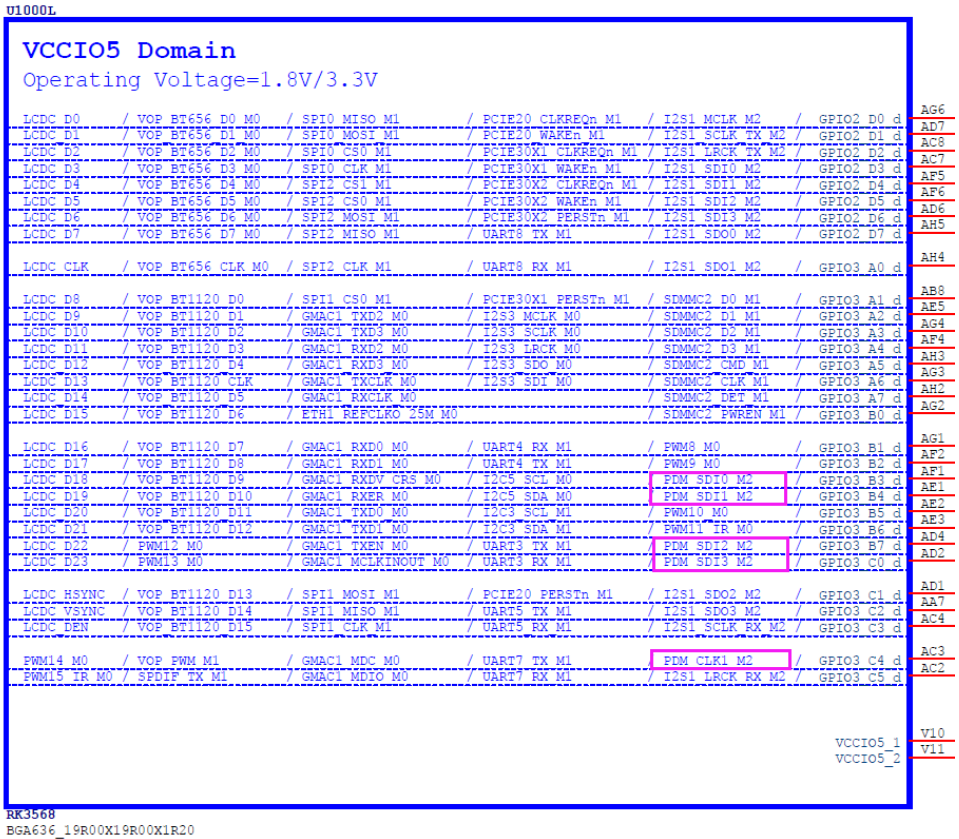


Figure 2-150 RK3568 PDM M2 functional pins

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In PDM interface design, please note:

- PDM_M0, PDM_M1 and PDM_M2 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 or M2 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to PDM peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve PDM interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of PDM interface are shown in the following Table.

Table 2–39 RK3568 PDM interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| PDM_CLK0 | Pull-down | Connect a 22ohm resistor in series | PDM clock 0 output |
| PDM_CLK1 | Pull-down | Connect a 22ohm resistor in series | PDM clock 1 output |
| PDM_SDI[3:0] | Pull-down | Connect a 22ohm resistor in series | PDM data input |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.5 SPDIF interface

RK3568 provides a SPDIF TX digital audio interface which supports up to 24bits resolution. SPDIF is the abbreviation of Sony/Philips Digital Interface Format. As for the transmission carrier, SPDIF is divided into coaxiality and optical fiber, which transmit the same signal depending on different carriers and have different interfaces and connection appearance. The communication rate of SPDIF is usually limited by the carrier, so it is necessary to consider the interface device specifications used in the hardware design. But the optical signal transmission needn't to consider the interface level and impedance problems, the interface is flexible and its anti-interference ability is stronger.

SPDIF interface pins multiplex in three different power domains, VCCIO4, VCCIO5 and VCCIO7.

- The corresponding supply of power domain should be adjusted according to SPDIF peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- The pull up/down and matching design recommendations of optical fiber SPDIF interface are shown in the following Table.

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Table 2–40 RK3568 SPDIF interface design

| Signal | Pull up/down inside | Connection mode | Description (chip end) |
|---|---|---|---|
| SPDIF_TX | Pull-down | Connect a 22ohm resistor in series | SPDIF signal output |

- When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.6 Analog audio interface

If the codec function of RK809-5 is not used, Pin14, 15,16,17,19,40 of RK809-5 must be grounded, and Pin18, 36,37,38,35,39,41,34,32,43,42 can be floated, the pin circuits left must be reserved.

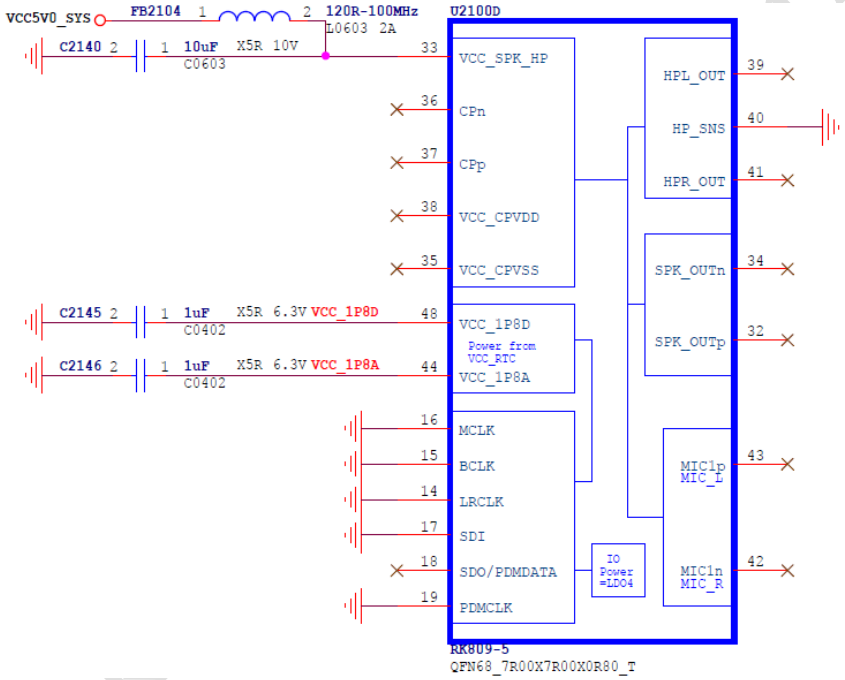


Figure 2-151 Process mode of related pins when RK809-5 Codec module is not used

When using RK809-5 power supply solution, the codec came with RK809-5 can achieve the headset output, 1.3W mono loudspeaker output and one-channel differential or two single-ended audio input functions.

RK3568 is connected to RK809-5 by I2S1 and PDM interfaces.

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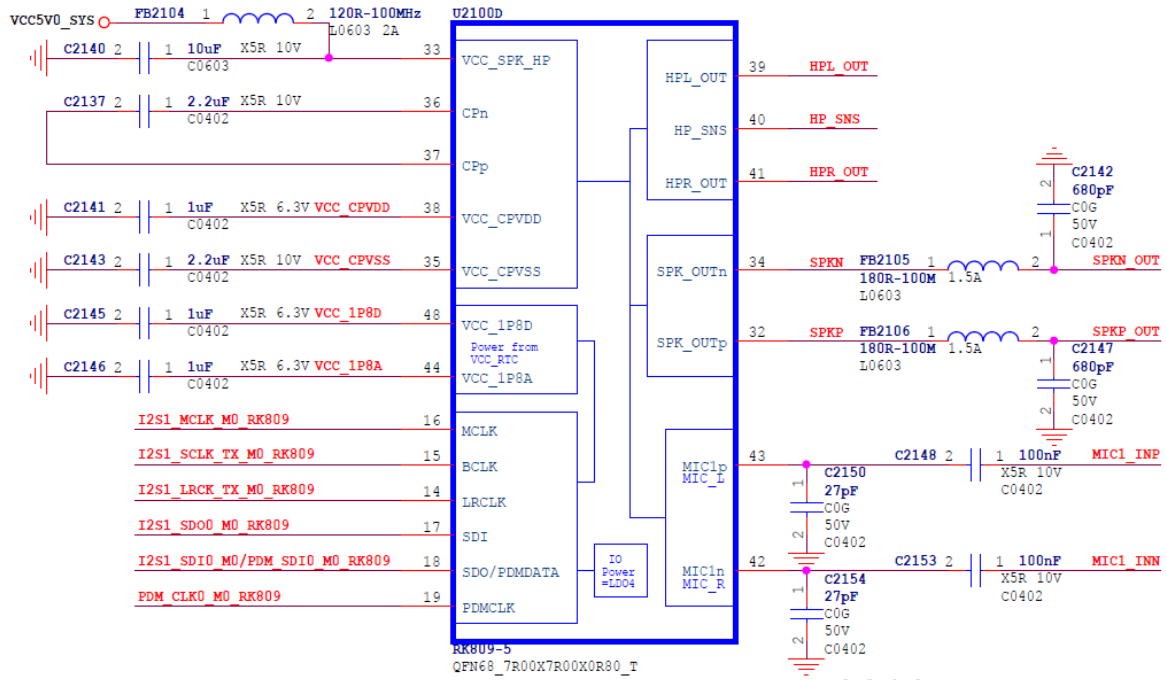
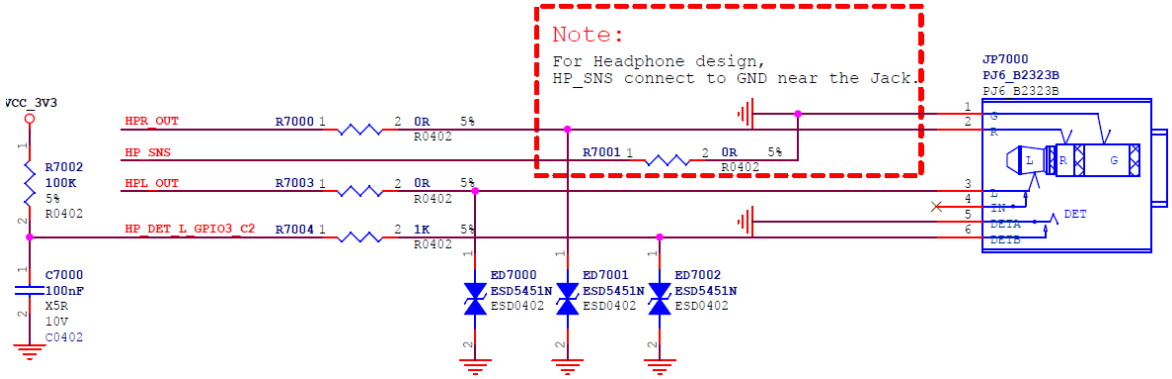



Figure 2-152 RK809-5 Codec module

- The IO level of I2S/PDM interface of RK809-5 is LDO4 output power supply of RK809-5, so I2S/PDM interface power domain level of RK3568 must match LDO4 output power supply voltage; Normally, LDO4 output of RK809-5 supplies power to I2S/PDM interface power domain of RK3568.
- HP_SNS of RK809-5 Codec output is referenced as internal Offset, this pin needs to be connected to GND for reference externally. For the case HPOUT used as LINEOUT for connecting external power amplifier, HPSNS can be grounded near RK809-5. For the earphone output case, HPSNS shall be independently routed to the earphone connector and connected to GND to reduce the level difference between HPSNS and the earphone GND. During routing, it shall be accompanied routing in the middle of HPR/HPL to avoid interference from other signals. The trace is shown in the figure below.

  In addition, ESD devices should be added to HPR_OUT and HPL_OUT to enhance anti ESD capability.

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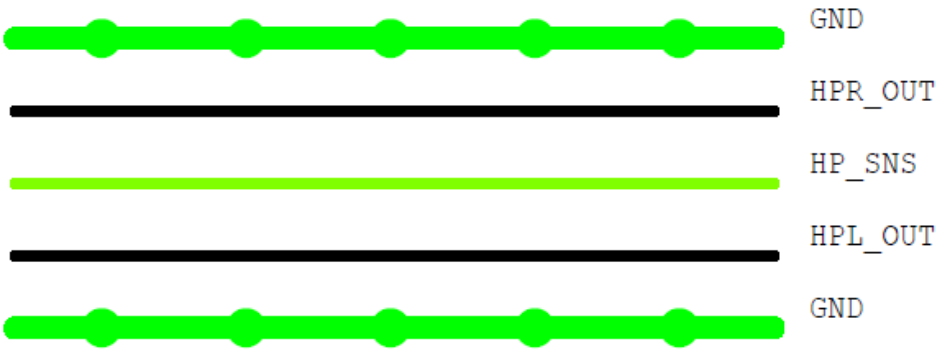


Figure 2-153 RK809 Codec output earphone circuit

- HP_DET of the headset connects a 1K ohm resistor and a 100nF capacitor in series, you should reserve ESD devices to strengthen the ability of anti-static surge.
- RK809-5 Pin33 is not only a speaker power supply, but also an internal Charger pump power supply. The working voltage range is 2.7-5.5V. It is recommended that the LC circuit cannot be deleted, and it should be placed near RK809-5 when layout.

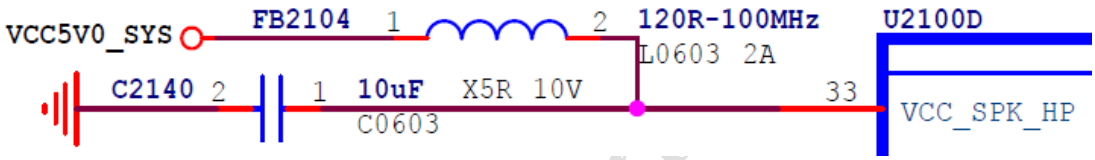


Figure 2-154 RK809-5 SPK/HP power supply pins

- RK809-5 Codec built-in Mono filter-free speaker driver circuit, can provide 1.3W@8ohm driving capacity. It is suitable for low power mono applications, and saves the cost of extra external power. Speaker output filter circuit is close to RK809-5, and ESD protection device is placed near the connector. Note the magnetic bead size in the following figure, the current is not less than 1.5A; if you need higher power or better output tone quality, it is recommended to expand the analog or digital power amplifier.

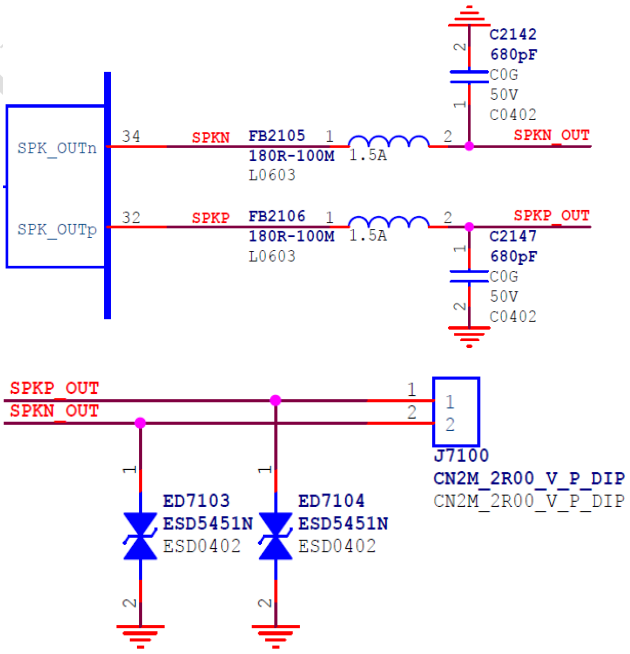


Figure 2-155 RK809-5 SPK output circuit

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- If RK809-5 built-in monophonic speaker drive circuit cannot meet the requirements of driving ability, or needs to achieve stereo function, you can attach independent analog/digital power amplifier.externally. When the analog power/Analog power amplifier is attached externally, HPOUT is used as LINEOUT for output; when the digital power/ power amplifier is attached externally, it can be connected to the I2S interface. You need to pay attention to the power supply design, when the power/ power supply is large, the supply mode should be noted.

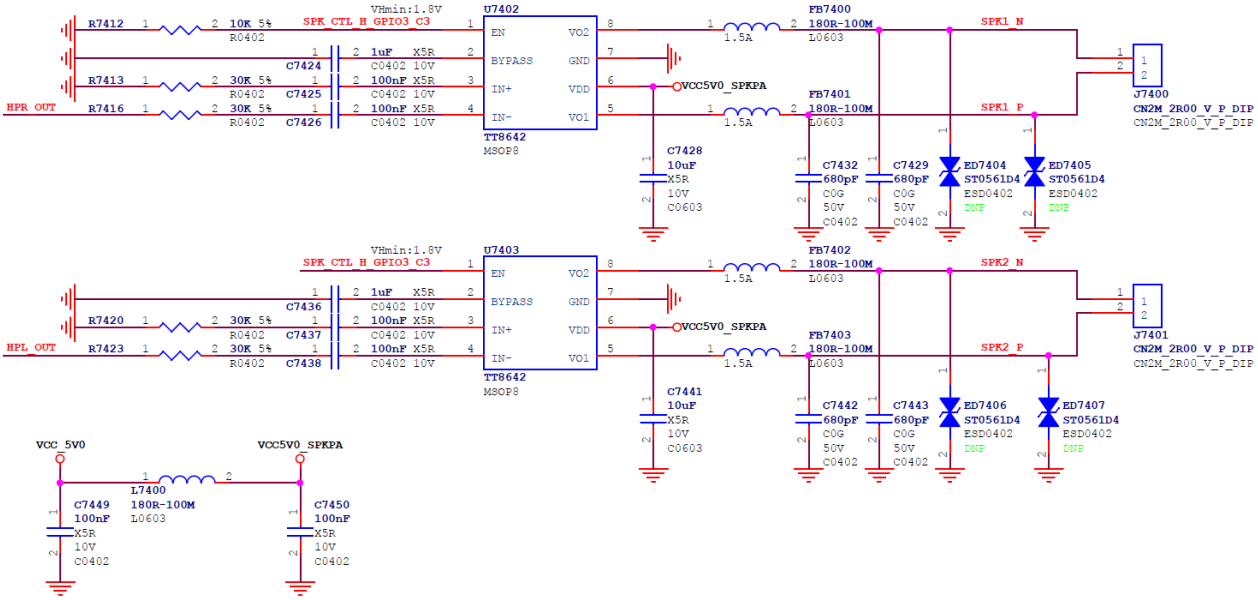


Figure 2-156 External SPK circuit

- Single-MIC circuit

  If using a three-segment headset, the local MIC can be configured as a differential input by using the analog ADC of RK809-5 (differential input provides better recording effect than single-ended input, and bias power supply requires a 68-100ohm resistor and a capacitor more than 1uF for RC filtering).

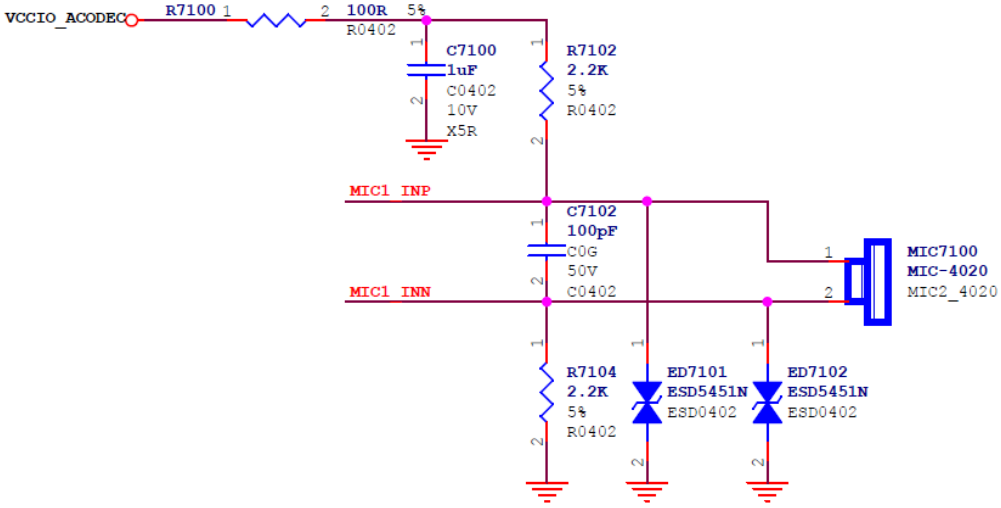


Figure 2-157 Electret MIC differential input circuit

If you use a four-segment headset + local MIC requirements, analog ADC configuration of RK809-5 is separated into two single-ended inputs.

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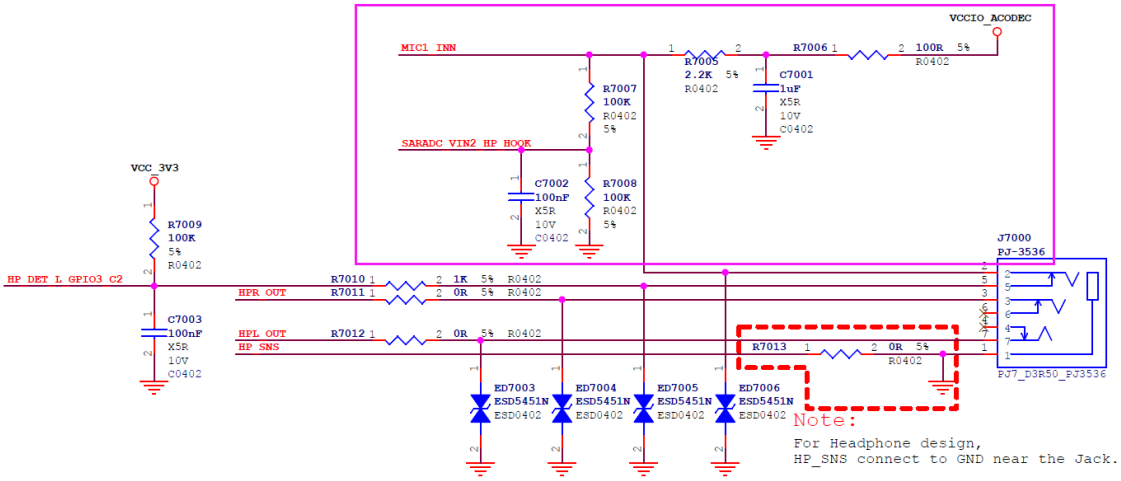


Figure 2-158 Four-segment headset with MIC single-ended input circuit

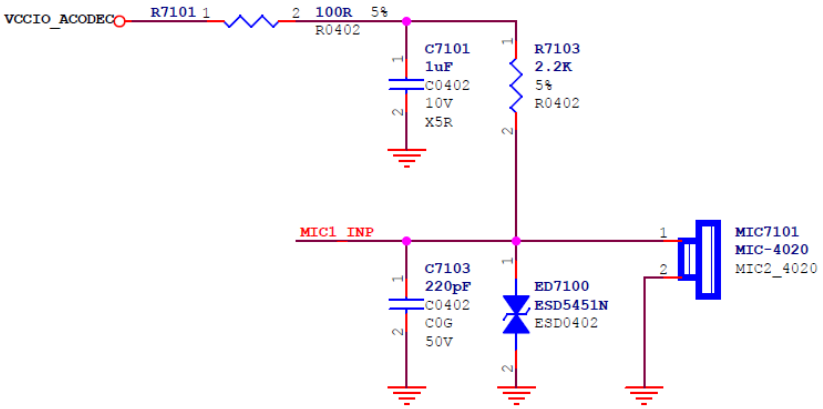


Figure 2-159 Electret MIC single-ended input circuit

Blocking capacitors of MIC shall not be deleted. And it should be placed close to RK809-5 when layout.

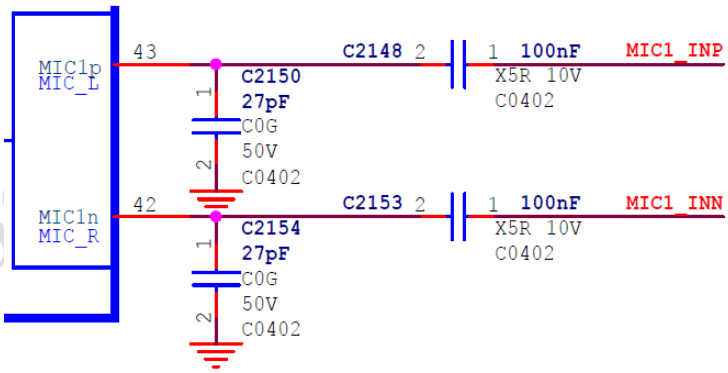


Figure 2-160 RK809-5 MIC input circuit pins

- Array MIC circuit solution

In the reference design of RK3568, multi-scene audio input/output solutions and multi-microphone solutions are provided.

Briefly introduce as follows:

When the ADC integrated by RK809-5 can meet the input requirements, the ADC of RK809-5 is inputted firstly; When you need to use far-field sound pickup and recovery, it is not recommended to use single-ended ADC to connect, and the differential signals input is used by default. If the input interfaces are not enough,

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you need to expand the ADC. By default, audio ADC of PDM interface is used in the current solution, and audio ADC of I2S interface can also be used.

Table 2–41 RK3568 matching relationship between audio applications and the circuit diagram

| Application cases | | Corresponding pages of circuit diagram |
|---|---|---|
| 1 | Three-segment headset | 70.Audio-Headphone Port—**Default circuit** |
| | + Differential microphone | 71.Audio-SingleMic+RK809_SPK—**Default circuit** |
| | + Mono speaker output | 71.Audio-SingleMic+RK809_SPK—**SPK circuit** |
| 2 | Four-segment headset | 70.Audio-Headphone Port—**Option circuit** |
| | + Single-ended microphone | 71.Audio-SingleMic+RK809_SPK—**Option circuit** |
| | + Mono speaker output | 71.Audio-SingleMic+RK809_SPK—**SPK circuit** |
| 3 | Three-segment headset | 70.Audio-Headphone Port—**Default circuit** |
| | + Differential microphone | 71.Audio-SingleMic+RK809_SPK—**Default circuit** |
| | + Mono speaker output | 72.Audio-MicArray+RK809_SPK--**RK809-5 SPK circuit** |
| | + Mono channel audio differential recovery | 72.Audio-MicArray+RK809_SPK--**Option1 circuit** |
| 4 | Three-segment headset | 70.Audio-Headphone Port—**Default circuit** |
| | +Two or four array mic | 72.Audio-MicArray+RK809_SPK—**MicArray circuit** |
| | + Mono speaker output | 72.Audio-MicArray+RK809_SPK--**RK809-5 SPK circuit** |
| | + Mono channel audio differential recovery | 72.Audio-MicArray+RK809_SPK--**Option1 circuit （recommended）** Or 72.Audio-MicArray+RK809_SPK—**Option2 circuit** |
| 5 | Four-segment headset | 70.Audio-Headphone Port—**Option circuit** |
| | +Two or four array mic | 72.Audio-MicArray+RK809_SPK—**MicArray circuit** |
| | + Mono speaker output | 72.Audio-MicArray+RK809_SPK--**RK809-5 SPK circuit** |
| | + Mono channel audio differential recovery | 72.Audio-MicArray+RK809_SPK--**Option1 circuit** |
| 6 | Three or four-segment headset | 70.Audio-Headphone Port—**Default circuit or Option circuit** |
| | +Two or four array mic | 74.Audio-MicArray+EXT Dual_SPK—**MicArray circuit** |
| | + Stereo speaker output | 74.Audio-MicArray+EXT Dual_SPK--**Speaker Output circuit** |
| | +Stereo differential recovery | 74.Audio-MicArray+EXT Dual_SPK—**Loopback circuit** |

- Application case 4 I2S/PDM connection schematic diagram 1:

  Speaker recovery of RK809-5 uses PDM_CLK0+PDM_D0 channel or PDM_CLK1+PDM_D3 (recommended),

  Array microphone uses PDM_CLK1+PDM_D1/2 channel.

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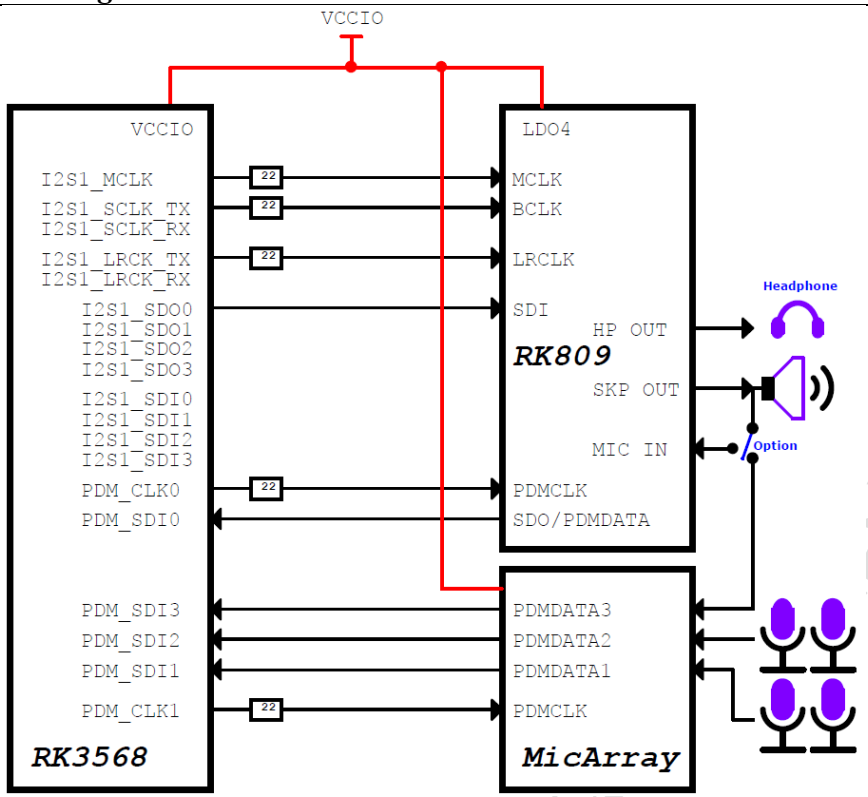


Figure 2-161 Array MIC solution I2S/PDM connection diagram 1

- Application case 6 I2S/PDM connection schematic diagram 2:

  Stereo speaker recovery uses PDM_CLK1+PDM_D3.

  Array microphone uses PDM_CLK1+PDM_D1/2 channel.

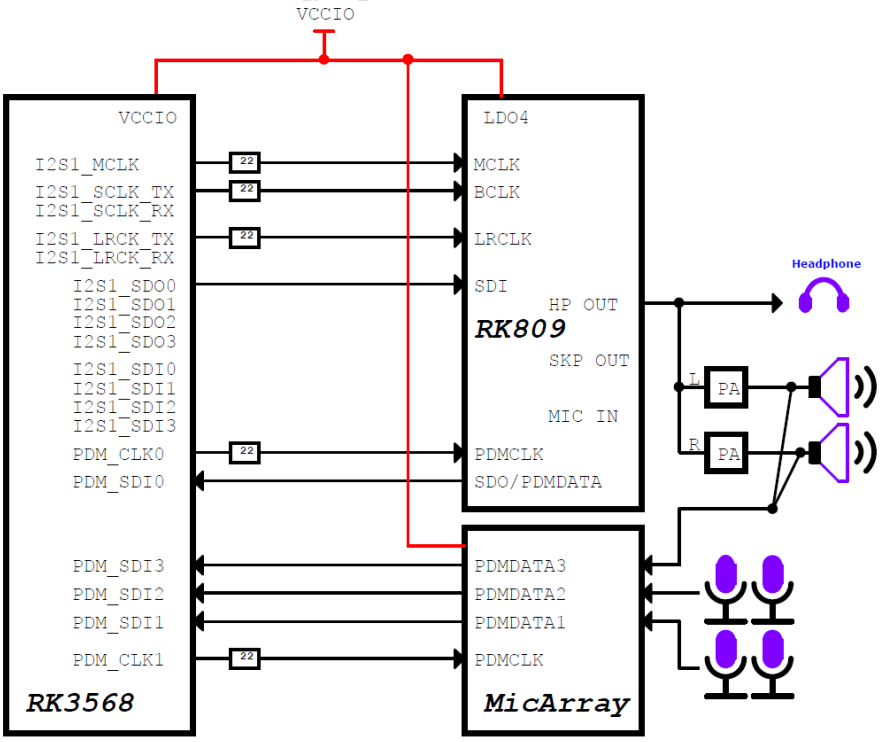


Figure 2-162 Array MIC solution I2S/PDM connection diagram 2

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## 2.3.12 GMAC Interface Circuit

RK3568 has two GMAC controllers, which can provide RMII or RGMII interface to connect external Ethernet PHY, or can also connect external Ethernet PHY through QSGMII/SGMII PCS, QSGMII/SGMII interface, as described in 2.3.6 QSGMII/SGMII circuit.

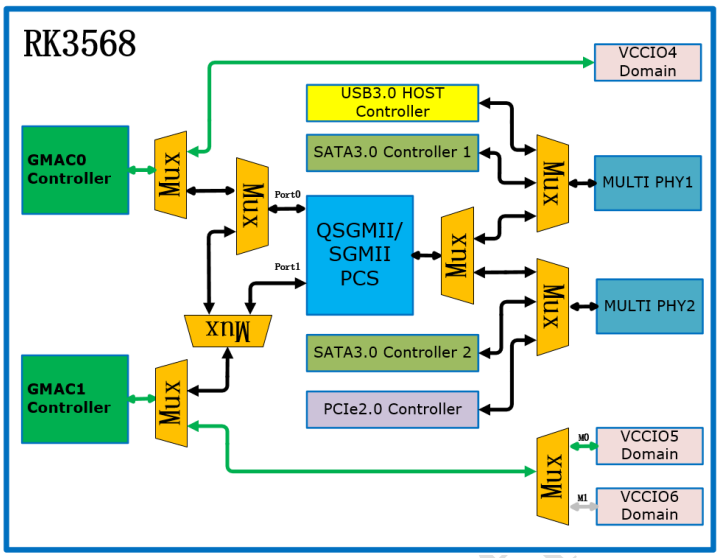


Figure 2-163 Path block diagram of RK3568 GMAC0, GMAC1 reused with IO

GMAC controller supports the following features:

- Support RGMII interface of 10/100/1000 Mbps data transmission rate
- Support RMII interface of 10/100 Mbps data transmission rate

- RGMII/RMII interface of GMAC0 is reused with VCCIO4 power domain

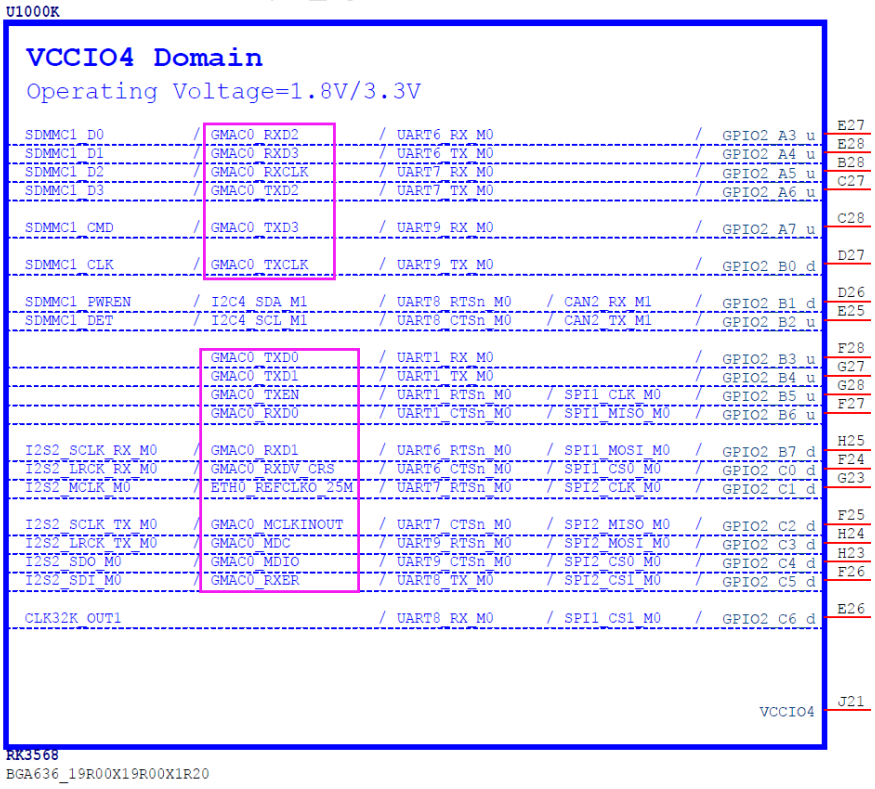


Figure 2-164 RK3568 GMAC0 functional pins

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- RGMII/RMII interface of GMAC0 is reused with VCCIO5 power domain or VCCIO6 power domain, using suffix _M0/_M1/ to distinguish different multiplexing positions. _M0/_M1/ cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for some others.

  - M0 reused with VCCIO5 power domain

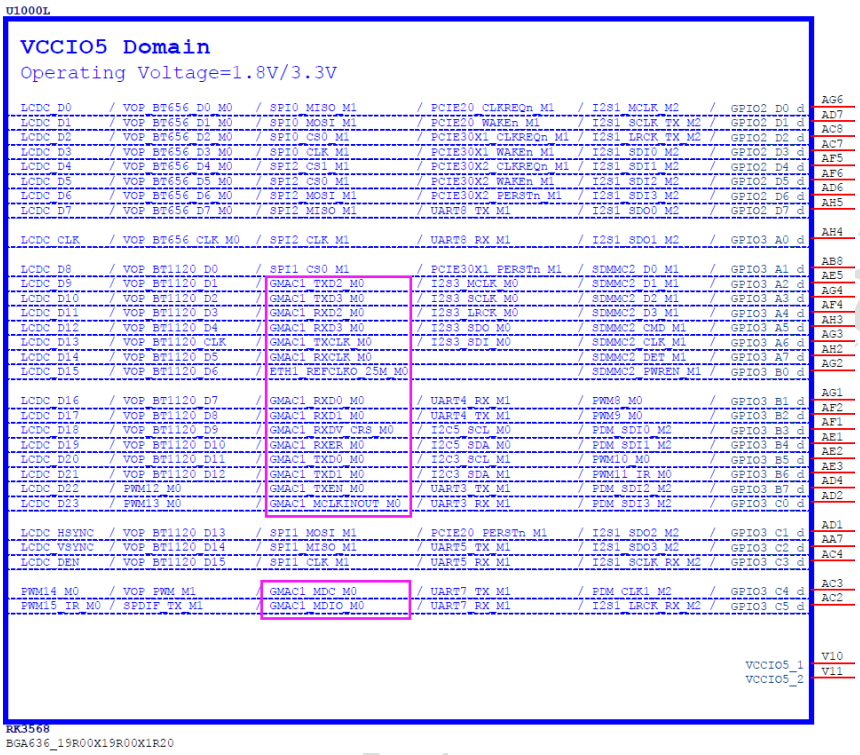


Figure 2-165 RK3568 GMAC1 M0 functional pins

  - M1 reused with VCCIO6 power domain

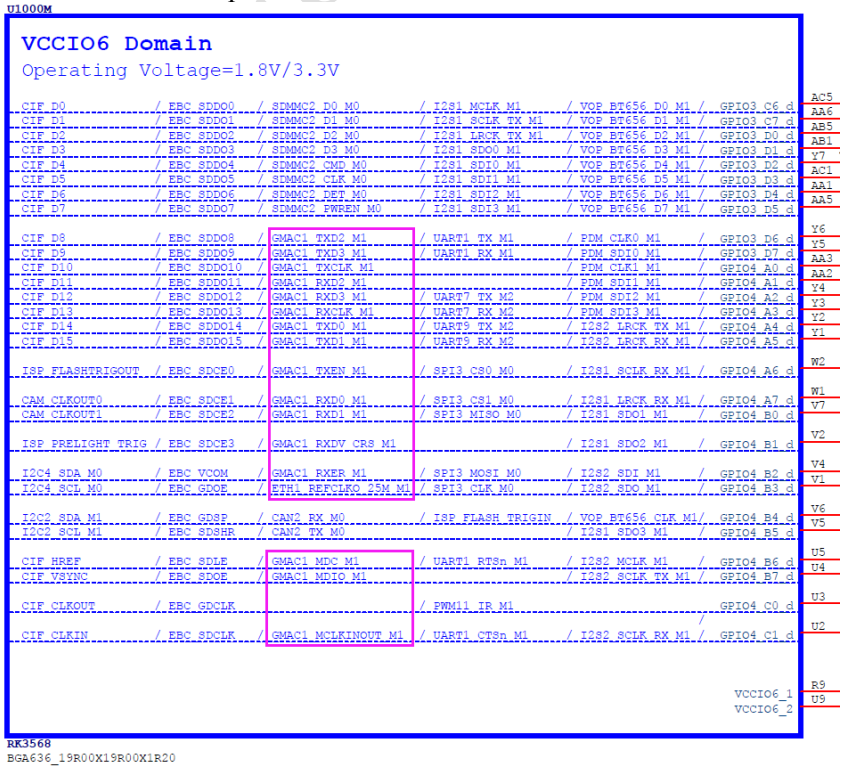


Figure 2-166 RK3568 GMAC1 M1 functional pins

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Notices in the design of RGMII/RMII interface:

- The power of RGMII/RMII interface is supplied by VCCIOx. During actual product design, need to select the corresponding power supply according to the actual IO power supply requirement (1.8V or 3.3V) of the peripherals, which must be matched. Besides, have to make sure the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- Recommend to use 1.8V for RGMII/RMII if possible to get better signal quality.
- In order to improve RGMII/RMII interface performance, the decoupling capacitor of VCCIOx power domain cannot be deleted and it should be placed close to the pin.
- ETH0_REFCLKO_25M requires to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- ETH1_REFCLKO_25M requires to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- TXD0-TXD3,TXCLK,TXEN require to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- RXD0-RXD3,RXCLK,RXDV require to series connect 22 ohm resistor at PHY end to improve the signal quality.
- RGMII/RMII interface pull-up/down and matching design are recommended in the Table below.

Table 2–42 RK3568 RGMII/RMII interface design

| Signal | IO type(chipset end) | Connection mode | RGMII interface | Signal description | RMII interface | Signal description |
|---|---|---|---|---|---|---|
| GMACx_TXD[3:0] | Output | Series connect 22ohm resistor close to RK3568 | RGMIIx_TXD[3:0] | Data sending | RMIIx_TXD[1:0] | Data sending |
| GMACx_TXCLK | Output | Series connect 22ohm resistor close to RK3568 | RGMIIx_TXCLK | Reference clock for data sending | -- | -- |
| GMACx_TXEN | Output | Series connect 22ohm resistor close to RK3568 | RGMIIx_TXEN | Data sending enabled(rising edge) and data sending error (falling edge) | RMIIx_TXEN | The signal used for data sending |
| GMACx_RXD[3:0] | Input | Series connect 22ohm resistor close to PHY end | RGMIIx_RXD[3:0] | Data receiving | RMIIx_RXD[1:0] | Data receiving |
| GMACx_RXCLK | Input | Series connect 22ohm resistor close to PHY end | RGMIIx_RXCLK | Reference clock for data receiving | -- | -- |
| GMACx_RXDV | Input | Series connect 22ohm resistor close to PHY end | RGMIIx_RXDV | Data receiving valid (rising edge) and receiving error (falling edge) | RMIIx_RXDV_CRS | Data receiving valid and carrier sensing |
| GMACx_RXER | Input | Series connect 22ohm resistor close to PHY end | -- | -- | RMIIx_RXER | Error hint for data receiving |
| GMACx_MCLKINOUT | Input/ Output | Output mode: Series connect 22ohm resistor close to RK3568 Input mode: Series connect 22ohm resistor close to PHY end | RGMIIx_MCLKIN_125M | PHY is sending 125MHz to MAC, optional | RMII_MCLKIN_50M or RMII_MCLKOUT_50M | Reference clock of RMII data sending and data receiving |

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| Signal | IO type(chipset end) | Connection mode | RGMII interface | Signal description | RMII interface | Signal description |
|---|---|---|---|---|---|---|
| ETHx_REFCLKO_25M | Output | Series connect 22ohm resistor close to RK3568 | ETHx_REFCLKO_25M | 25MHz clock provided by RK3568 to replace PHY crystal | ETHx_REFCLKO_25M | 25MHz clock provided by RK3568 to replace PHY crystal |
| GMACx_MDC | Output | Series connect 22ohm resistor close to RK3568 | RGMIIx_MDC | Manage data clock | RMIIx_MDC | Manage data clock |
| GMACx_MDIO | Input/Output | Series connect 22ohm resistor, external pull-up 1.5K-1.8Kohm resistor | RGMIIx_MDIO | Manage data output/input | RMIIx_MDIO | Manage data output/input |

- When board-to-board connection is realized by connector, recommend to series connect resistor with a certain value (22ohm-100ohm, as long as it can meet the SI test), and reserved TVS component
- RGMII connection example 1, please refer to the reference design for the details (GEPHY uses external 25MHz crystal as working clock).

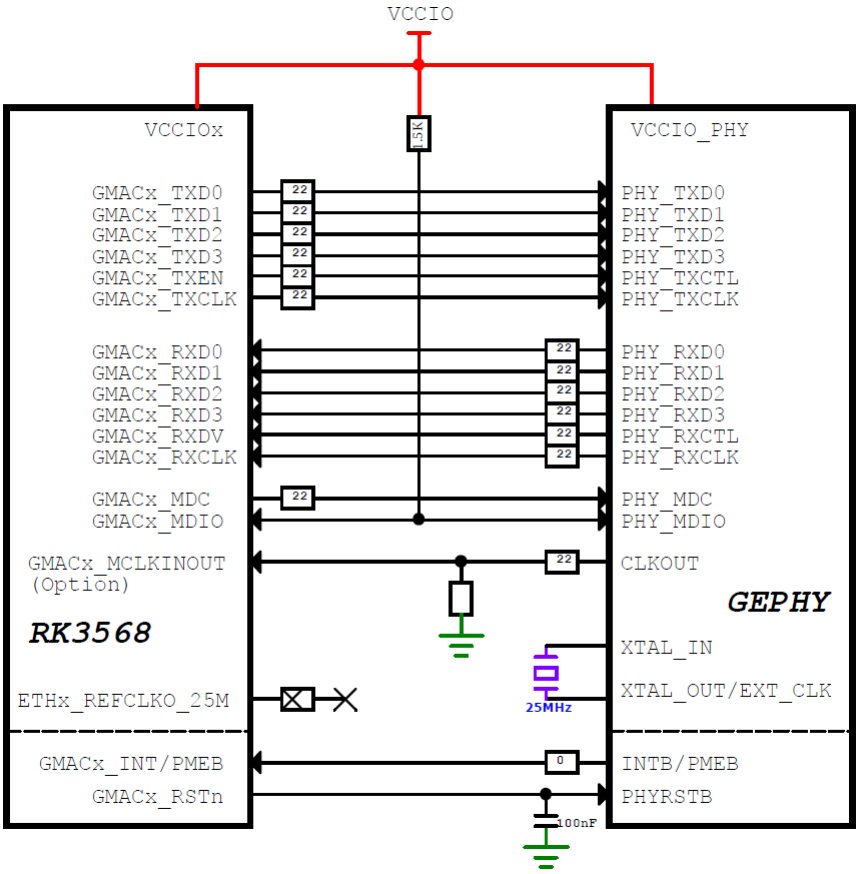


Figure 2-167 RGMII connection example 1

- RGMII connection example 2, please refer to the reference design for details (GEPHY uses the 25MHz provided by RK3568 as working clock).

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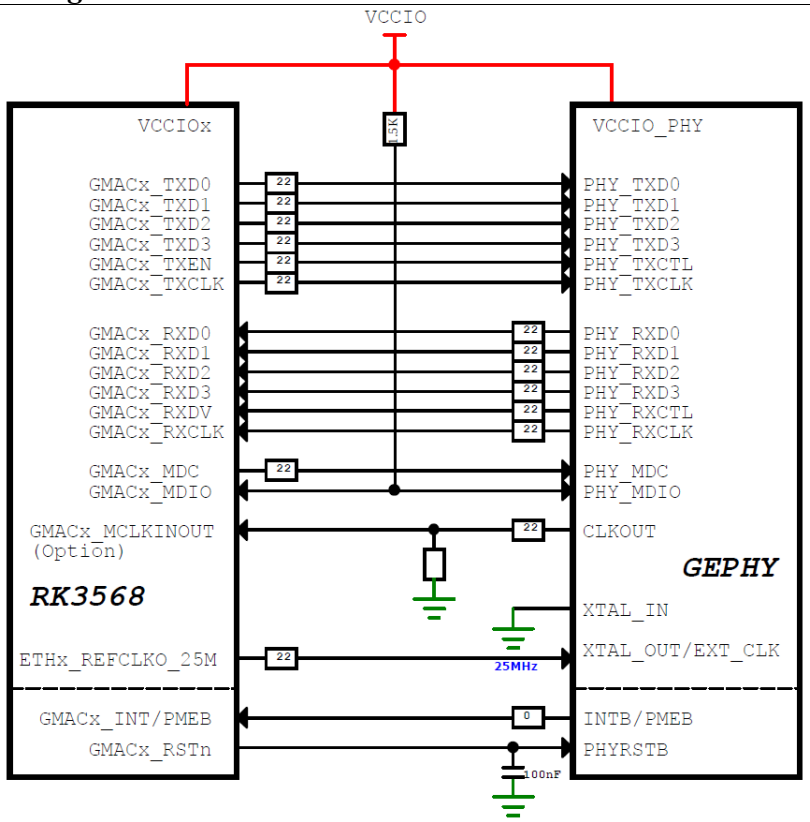


Figure 2-168 RGMII connection example 2

- RMII connection example 1, please refer to the reference design for details (GMACx_MCLKINOUT adopts output mode, that is, used as both FEPHY working clock and reference clock of RMII interface. Some FEPHY doesn't support this mode).

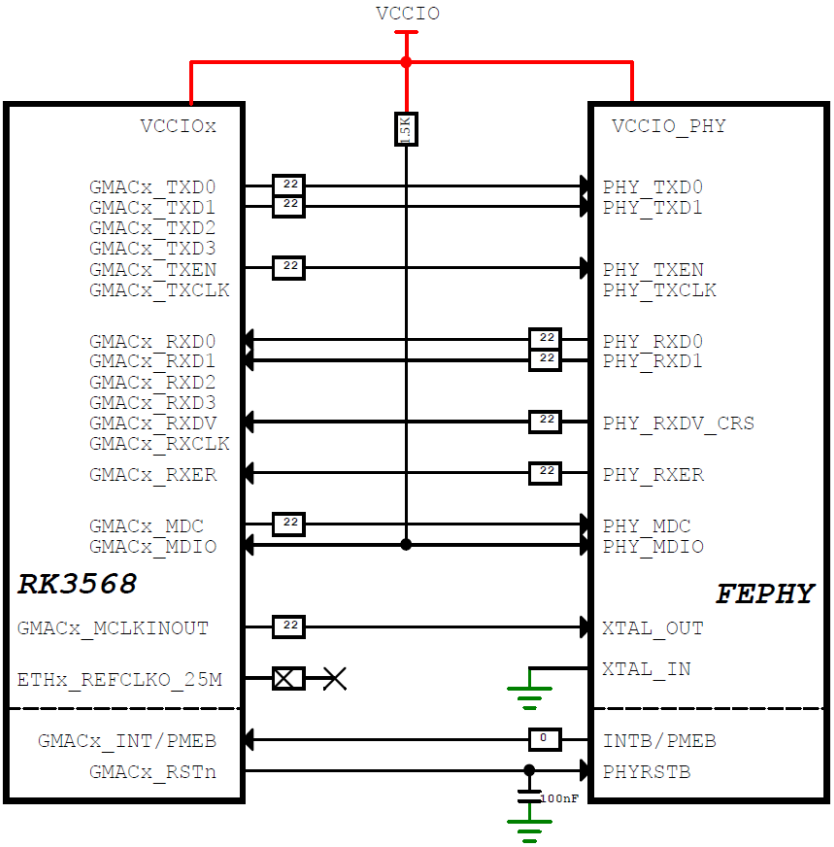


Figure 2-169 RMII connection example 1

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- RMII connection example 2, please refer to the reference design for details (25MHz crystal is used as FEPHYworking clock, GMACx_MCLKINOUT adopts output mode which is used as the reference clock of RMII interface).

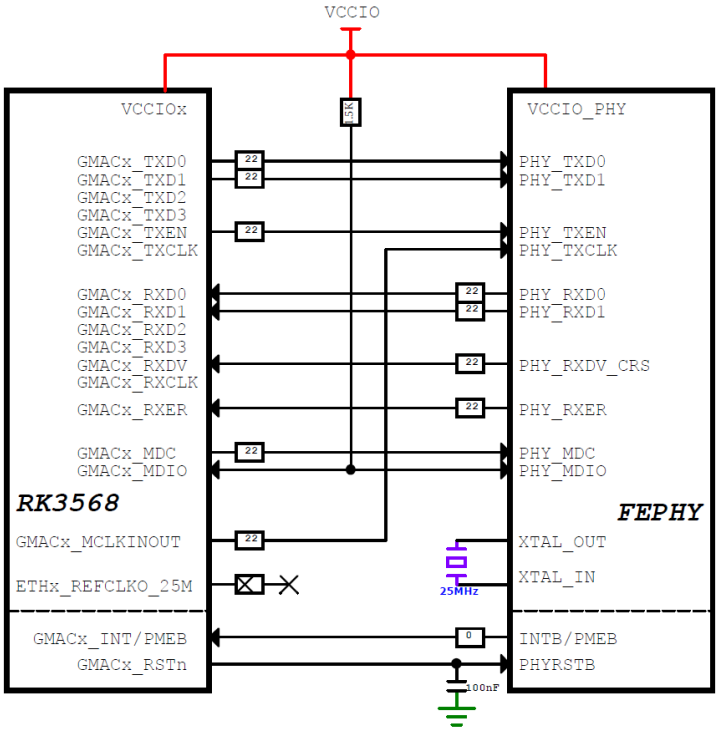


Figure 2-170 RMII connection example 2

- RMII connection example 3, please refer to the reference design for details (using 25MHz provided by RK3568 to replace FEPHY crystal, GMACx_MCLKINOUT adopts output mode which is used as the reference clock of RMII interface).

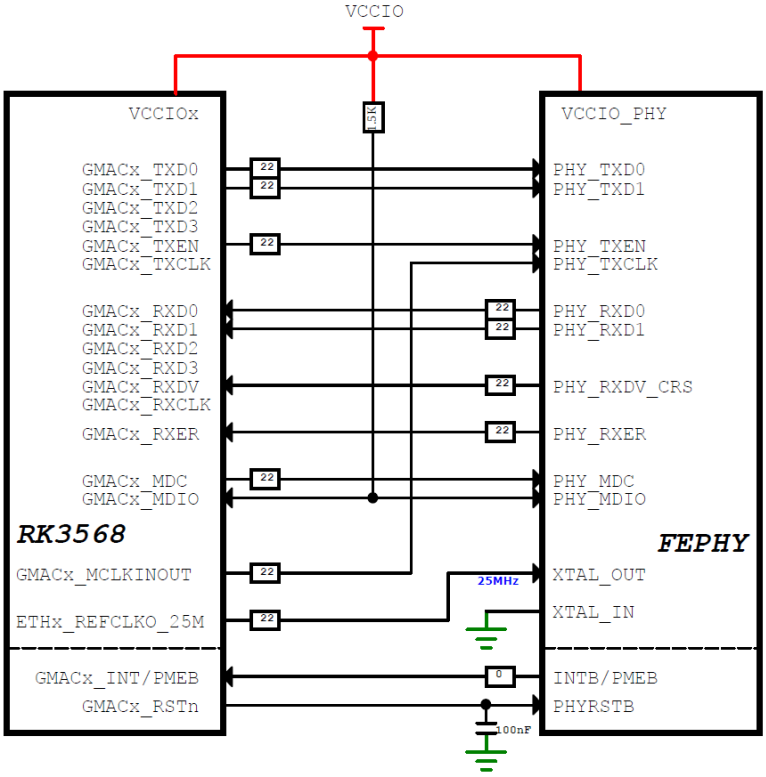


Figure 2-171 RMII connection example 3

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- RMII connection example 4, please refer to the reference design for details (FEPHY uses external 25MHz crystal as working clock, GMACx_MCLKINOUT adopts input mode, and the reference clock of RMII interface is provided by FEPHY).

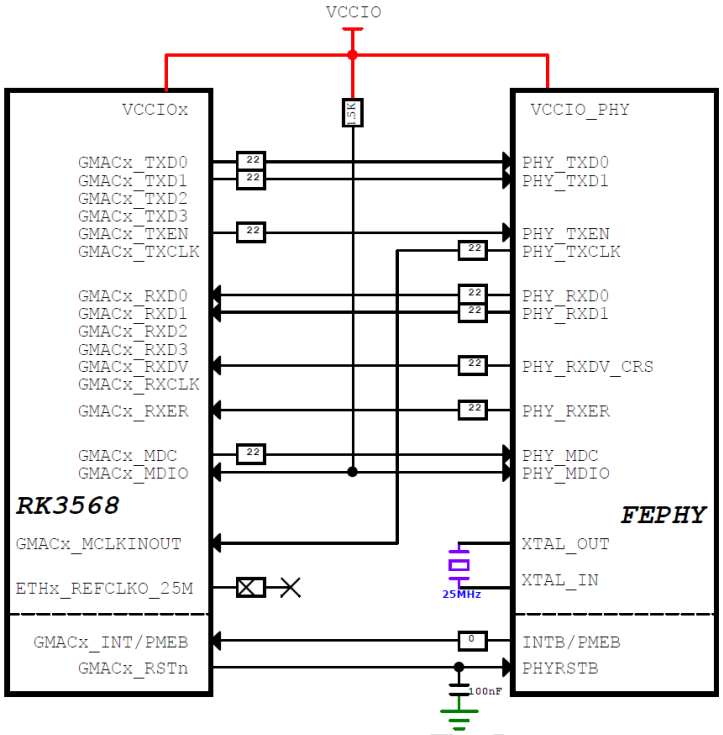


Figure 2-172 RMII connection example 4

- RMII connection example 5, please refer to the reference design for details (using 25MHz provided by RK3568 to replace FEPHY crystal, GMACx_MCLKINOUT adopts input mode and the reference clock of RMII interface is provided by FEPHY).

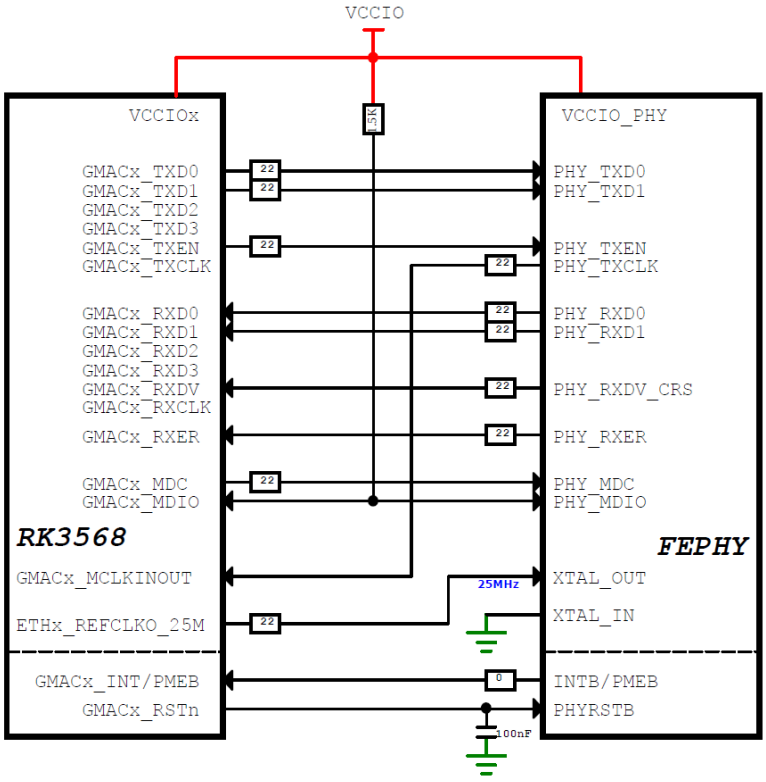


Figure 2-173 RMII connection example 5

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- Reset signal of Ethernet PHY should be controlled by GPIO, and GPIO level must match with PHY IO level. 100nF capacitor should be added close to PHY pin to enhance anti-static ability. Note: RTL8211F/FI reset pin only supports 3.3V level.
- INTB/PMEB of RTL8211F/FI is open drain output. Must add external pull-up resistor. The reference design uses internal pull-up resistor of RK3568 IO by default.
- When PHY uses external crystal, please select the crystal capacitance according to the load capacitance value of the actually used crystal, and the frequency deviation should be controlled within +/-20ppm.
- The resistor externally connected to RSET pin of RTL8211F/FI is 2.49KΩ/1%, which cannot be modified at will.
- MDIO must add external pull-up resistor, with recommended value 1.5-1.8Kohm, and the pull-up power must be consistent with the power.
- The transformer central tap of RTL8211F/FI must be connected according to the reference design. If using other Ethernet PHY, the connection of the transformer central tap should follow the reference design of each Ethernet PHY vendor, because different PHY vendors have different connection methods.
- 1000pF isolation capacitor is recommended to use high-voltage safety capacitor, which has enough electrical clearance to ensure the security of lightning strike.
- The 75 ohm resistor at the high voltage side of the network transformer is recommended to use the package bigger than 0805.
- When the lightning protection level reaches 4KV or above, the lightning protection tube should be added, as ordinary isolation transformer can only meet 2KV grade requirement.
- If there is lightning differential test requirement, need to add TVS tube between MDI differential pair.
- Must confirm whether RJ45 package is consistent with the schematic or not. RJ45 has Tab down and Tab up two type, which signal sequence are just opposite. If using RTL8211F/FI, recommend to use Tab down, MDI sequence is in order.
- The initial hardware configuration of PHY must match with the actual requirement.

### 2.3.13 UART Interface Circuit

RK3568 has 10 UART controllers, which support the following functions:

- All include two 64-byte FIFO used for data receiving and sending.
- Support 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, and 4Mbps.
- Support programmable baud rate, support non-integer clock divider.
- Support interrupt or DMA based mode.
- Support 5-8bit width transmission.

Considering the application flexibility of different products, 10 UARTs are separately reused with several different power domains, using suffix _M0/_M1/_M2 to identify different multiplexing locations. _M0/_M1/_M2 cannot be used at the same time. You can only select one group of them. It doesn't support to select M0 for some signals, while selecting M1 or M2 for other signals.

- RK3568 UART interface distribution.

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Table 2–43 RK3568 UART interface distribution

| UART No. | Reuse status | Reused power domain |
|---|---|---|
| UART0 | None | PMUIO2 |
| UART1 | M0,M1 | M0:VCCIO4<br>M1:VCCIO6 |
| UART2 | M0,M1 | M0:PMUIO2<br>M1:VCCIO3 |
| UART3 | M0,M1 | M0:VCCIO1<br>M1:VCCIO5 |
| UART4 | M0,M1 | M0:VCCIO1<br>M1:VCCIO5 |
| UART5 | M0,M1 | M0:VCCIO3<br>M1:VCCIO5 |
| UART6 | M0,M1 | M0:VCCIO4<br>M1:VCCIO3 |
| UART7 | M0,M1,M2 | M0:VCCIO4<br>M1:VCCIO5<br>M2:VCCIO6 |
| UART8 | M0,M1,M2 | M0:VCCIO4<br>M1:VCCIO5 |
| UART9 | M0,M1,M2 | M0:VCCIO4<br>M1:VCCIO7<br>M2:VCCIO6 |

- **UART2 MO is** Debug UART of RK3568 by default. Please refer to 2.1.6 JTAG and UART Debug circuit for notices.
- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of UART peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- UART interface pull-up/down and matching design are recommended as in the Table below.

Table 2–44 RK3568 UART interface design

| Signal | Connection mode | Description (chipset end) |
|---|---|---|
| UARTx_RX | Direct connection | UART data input |
| UARTx_TX | Direct connection | UART data output |
| UARTx_CTSn | Direct connection | UART allowing to send signal |
| UARTx_RTSn | Direct connection | UART requesting to send signal |

When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (22ohm-100ohm, as long as it can meet the SI test), and reserve TVS component.

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### 2.3.14 SPI Interface Circuit

Besides above FSPI controllers, RK3568 lso has 4 generic SPI controllers, which support the following functions:

- Support master and slave two modes.
- Support 4, 8, 16bit serial data transmission.
- Support full duplex and half duplex mode transmission.

Considering the application flexibility of different products, 4 SPIs are separately reused with different power domains, using suffix _M0/_M1/ to identify different multiplexing locations. _M0/_M1/ cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

- RK3568 SPI interface distribution.

Table 2–45 RK3568 SPI interface distribution

| SPI no. | Reused status | Reused power domain |
|---|---|---|
| SPI0 | M0,M1 | M0:PMUIO2<br>M1:VCCIO5 |
| SPI1 | M0,M1 | M0:VCCIO4<br>M1:VCCIO5 |
| SPI2 | M0,M1 | M0:VCCIO4<br>M1:VCCIO5 |
| SPI3 | M0,M1 | M0:VCCIO6<br>M1:VCCIO7 |

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of SPI peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- SPI interface pull-up/down and matching design are recommended as in the Table below.

Table 2–46 RK3568 SPI interface design

| Signal | Connection mode | Description (chipset end) |
|---|---|---|
| SPIx_CLK | Series connect 22ohm resistor | SPI clock<br>SPI clock |
| SPIx_MOSI | Direct connection | SPI data output(Master) |
| SPIx_MISO | Direct connection | SPI data input(Master) |
| SPIx_CS0 | Direct connection | SPI chip selection 0 |
| SPIx_CS1 | Direct connection | SPI chip selection 1 |

- When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (22ohm-100ohm, as long as it can meet the SI test), and reserve TVS component.

### 2.3.15 CAN Interface Circuit

RK3568 has 3 CAN controllers, which support the following functions:

- Support CAN 2.0B protocol.

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- Support 1Mbps, 8Mbps.

Considering the application flexibility of different products, 3 CANs are separately reused with different power domains, using suffix _M0/_M1 to identify different multiplexing locations. _M0/_M1 cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

- RK3568 CAN interface distribution.

Table 2–47 RK3568 CAN interface distribution

| CAN no. | Reused status | Reused power domain |
|---|---|---|
| CAN0 | M0,M1 | M0:PMUIO2<br>M1:VCCIO3 |
| CAN1 | M0,M1 | M0:VCCIO1<br>M1:VCCIO7 |
| CAN2 | M0,M1 | M0:VCCIO6<br>M1:VCCIO4 |

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of CAN peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- CAN interface pull-up/down and matching design are recommended as in the Table below.

Table 2–48 RK3568 CAN interface design

| Signal | Connection mode | Description (chipset end) |
|---|---|---|
| CANx_RX | Direct connection | CAN data input |
| CANx_TX | Direct connection | CAN data output |

- When using a connector to realize board-to-board connector, recommend to series connect resistor with certain value (22ohm-100ohm, as long as it can meet the SI test), and reserve TVS component.

### 2.3.16 I2C Interface Circuit

RK3568 has 6 I2C controllers, which support the following functions:

- Support I2C bus main mode.
- Support software programmable clock and the transmission speed is up to 400Kbit/sec.
- Support 7bit and 10bit addressing mode.

Considering the application flexibility of different products, 6 I2Cs are separately reused with different power domains, using suffix _M0/_M1 to identify different multiplexing locations. _M0/_M1 cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

- RK3568 I2C interface distribution.

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Table 2–49 RK3568 I2C interface distribution

| I2C No. | Reuse status | Reused power domain |
|---|---|---|
| I2C0 | None | PMUIO2 |
| I2C1 | None | PMUIO2 |
| I2C2 | M0,M1 | M0:PMUIO2<br>M1:VCCIO6 |
| I2C3 | M0,M1 | M0:VCCIO1<br>M1:VCCIO5 |
| I2C4 | M0,M1 | M0:VCCIO6<br>M1:VCCIO4 |
| I2C5 | M0,M1 | M0:VCCIO5<br>M1:VCCIO7 |

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of I2C peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- I2C0 is allocated to PMIC by default, which is convenient for software. Recommend not to change.
- I2C signal SCL, SDA require to connect external pull-up resistor. Select the resistors with different values according to different load of bus. Recommend to connect 2.2kΩ pull-up resistor.
- The addresses of the devices on I2C bus should not conflict. The pull-up power must be consistent with the power supply.
- I2C interface pull-up/down and matching design are recommended as in the Table below.

Table 2–50 RK3568 I2C interface design

| Signal | Connection mode | Description (chipset end) |
|---|---|---|
| I2Cx_SCL | Direct connection | I2C clock |
| I2Cx_SDA | Direct connection | I2C data output/input |

When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (22ohm-100ohm, as long as it can meet the SI test), and reserve TVS component.

### 2.3.17 PWM Interface Circuit

RK3568 has 4 independent PWM controllers, each controller has 4 channels, have up to 16 PWM channels at most, and support the following functions:

- Support capture mode.
- Support continuous mode or one-time mode.
- Optimized infrared application of PWM3, PWM7, PWM11 and PWM15.

Considering the application flexibility of different products, 16 PWMs are separately reused with different power domains, using suffix _M0/_M1 to identify different multiplexing locations.

- RK3568 PWM interface distribution.

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Table 2–51 RK3568 PWM interface distribution

| PWM No. | Reused status | Reused power domain |
|---|---|---|
| PWM0 | M0,M1 | M0:PMUIO2<br>M1:PMUIO2 |
| PWM1 | M0,M1 | M0:PMUIO2<br>M1:PMUIO2 |
| PWM2 | M0,M1 | M0:PMUIO2<br>M1:PMUIO2 |
| PWM3_IR | None | PMUIO2 |
| PWM4 | None | PMUIO2 |
| PWM5 | None | PMUIO2 |
| PWM6 | None | PMUIO2 |
| PWM7_IR | None | PMUIO2 |
| PWM8 | M0,M1 | M0:VCCIO5<br>M1:VCCIO3 |
| PWM9 | M0,M1 | M0:VCCIO5<br>M1:VCCIO3 |
| PWM10 | M0,M1 | M0:VCCIO5<br>M1:VCCIO3 |
| PWM11_IR | M0,M1 | M0:VCCIO5<br>M1:VCCIO6 |
| PWM12 | M0,M1 | M0:VCCIO5<br>M1:VCCIO7 |
| PWM13 | M0,M1 | M0:VCCIO5<br>M1:VCCIO7 |
| PWM14 | M0,M1 | M0:VCCIO5<br>M1:VCCIO7 |
| PWM15_IR | M0,M1 | M0:VCCIO5<br>M1:VCCIO7 |

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of PWM peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (22ohm-100ohm, as long as it can meet the SI test), and reserve TVS component.
- When an IR receiver is used as input, pay attention to the following items:
- If IR receiver is required to support suspend/resume and low power consumption (that is, the VDD_LOGIC power supply shutdown solution), it is recommended to use PWM3 as the input of IR receiver,

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- The power supply of infrared receiver should use VCC3V3_PMU power supply;
- The power supply of IR receiver requires 22-100ohm resistor and capacitor more than 10nF to do RC filtering.
- IR receiver uses 38KHz by default, and software requires fine tune accordingly if changed to other frequency.
- The output pin level of IR receiver must match with RK3568 IO level.
- The output pin of the infrared receiver is recommended to be connected to a 22 ohm resistor in series and a 1nF capacitor to the ground, and then connected to RK3568 to strengthen the anti-static surge capability.

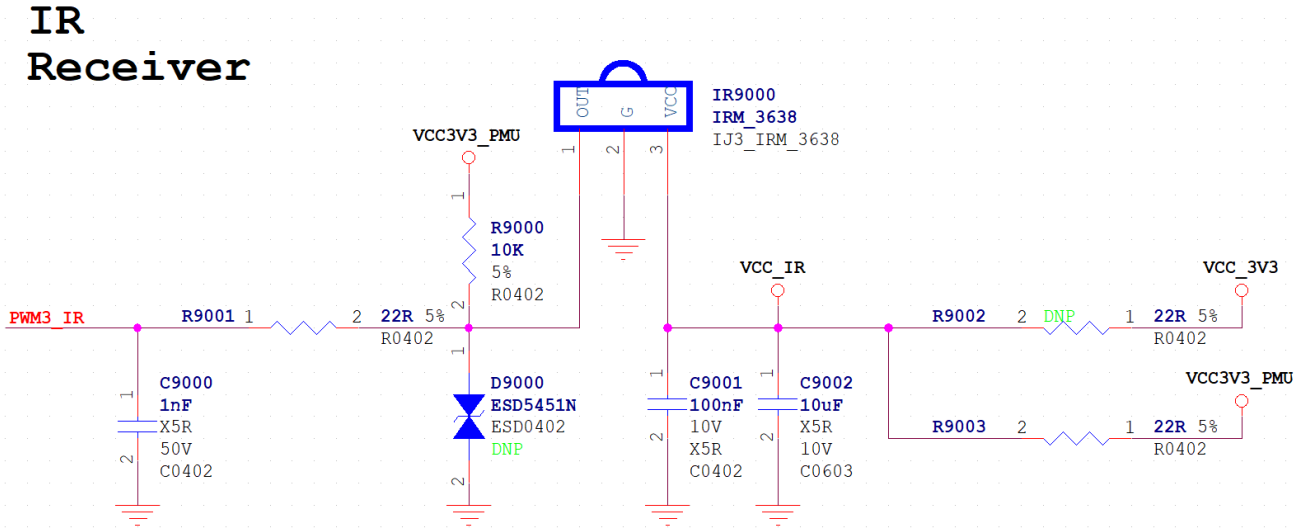


Figure 2-174 IR receiver circuit

- IR receiver layout should be far away from the wireless module antenna, such as WIFI antenna, to avoid the influence of wireless data transmission on the infrared signal receiving.
- IR receiver layout should avoid direct LED light source on the board to avoid the influence of LED flicker frequency on the infrared receiving.
- The whole process of IR signal is recommended to be surrounded by GND. If unable to be grounded, recommend to keep from other signals with the distance >=2 times of linewidth.

### 2.3.18 RK3568 Unused Modules Pins Processing

Please refer to the document of "RK3568_Methods for Processing Unused Pins_V10_20201218_CN.xlsx".

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# 3 PCB Design recommendations

## 3.1 PCB Layers Design

In order to reduce the reflection phenomenon in the process of high-speed signal transmission, impedance matching must be maintained on the signal source, the receiving end and the transmission line. The impedance of a single-ended signal line depends on its line width and its relative position to the reference layer. The line width/line spacing between the differential pairs required for a specific impedance depends on the selected PCB stackup. Since the minimum line width and minimum line distance depend on the PCB type and cost requirements, due to this limitation, the selected PCB stackup must be able to achieve all impedance requirements on the board, including inner and outer layers, single-ended and differential lines, etc.

Layer design rules:

- The layers neighboring to the chip is a ground layer, which provides a reference layer for device layer for routing;
- All signal layers are as close as possible to the ground layer
- Try to avoid two signal layers neighboring directly
- The main power supply is as close to the related ground as possible
- A symmetrical structure design should be adopted in principle. The meaning of symmetry includes: the thickness and type of the media layer, the thickness of the copper foil, and the symmetry of the graphic distribution type (large copper foil layer, circuit layer)

PCB multilayer recommended solution: When designing a specific PCB layers, the above rules should be used flexibly, and the layer arrangement should be determined according to actual requirements instead of applying mechanically. The recommended solutions for frequently used layer arrangements are given below for reference only. In layers setting, if there are neighboring layers for routing, the interlayer crosstalk can be reduced by increasing the distance between neighboring layers. For the case of cross-segmentation, ensure that the key signal must have a relatively complete reference ground plane or provide necessary bridging measures.

6-layer PCB design is recommended for RK3568. The following multilayer structure is an example to help customers in the selection and evaluation of multilayer structure. If you choose another type of multilayer structure, please recalculate the impedance according to the specifications given by PCB manufacturers.

### 3.1.1 Six Layers PCB Design

In the 6-layer PCB design, the reference layer of the top-level signal L1 is L2, and the reference layer of the bottom-level signal L6 is L5. L3 and L5 are also used as reference layer for L4 high-speed signal routing, depending on layers conditions. It is recommended that the layer sequence is `refers to L5, and 1oZ is recommended. The following figure shows the 1.6mm thickness reference layer design. Please adjust Core thickness according to board thickness requirements.

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| Layer No. | sig/pln | Copper thk. before process (oz) | Construction | Finished thikness (um) | Finished thikness (mil) | Tolerance | Dk (1GHz) |
|---|---|---|---|---|---|---|---|
| S/M | | | | 18 | 0.71 | +/-10 | 3.8 |
| 1 | TOP | 1 | | 35 | 1.38 | +/-10 | |
| | | | PP 1080X1(RC64%) | 80 | 3.15 | +/-10 | 4.2 |
| 2 | GND | 1 | | 30 | 1.18 | +/-10 | |
| | | | PP 2116X1(RC50%) | 102 | 4.02 | +/-10 | 4.2 |
| 3 | POWER | 1 | | 30 | 1.18 | +/-10 | |
| | | | Core | 1008 | 39.69 | +/-10 | 4.2 |
| 4 | SIGNAL | 1 | | 30 | 1.18 | +/-10 | |
| | | | PP 2116X1(RC50%) | 102 | 4.02 | +/-10 | 4.2 |
| 5 | GND | 1 | | 30 | 1.18 | +/-10 | |
| | | | PP 1080X1(RC64%) | 80 | 3.15 | +/-10 | 4.2 |
| 6 | BOTTOM | 1 | | 35 | 1.38 | +/-10 | |
| S/M | | | | 18 | 0.71 | +/-10 | 3.8 |
| | | | 总计： | 1598 | 62.91 | | |

Figure 3-1 Six layers PCB design

### 3.1.2 Four Layers PCB Design

In 4-layer PCB design, the reference layer of the top signal L1 is L2, and the reference layer of the bottom signal L4 is L3. It depends on the layers conditions, and 1oZ is recommended. The following figure shows the reference layer of 1.6mm thickness. Please adjust Core thickness according to board thickness requirements.

| Layer No. | sig/pln | Copper thk. before process (oz) | Construction | Finished thikness (um) | Finished thikness (mil) | Tolerance | Dk (1GHz) |
|---|---|---|---|---|---|---|---|
| S/M | | | | 18 | 0.71 | +/-10 | 3.8 |
| 1 | TOP | 1 | | 30 | 1.18 | +/-10 | |
| | | | PP 1080X1(RC68%) | 80 | 3.15 | +/-14 | 4.2 |
| 2 | GND | 1 | | 30 | 1.18 | +/-10 | |
| | | | Core | 1265 | 49.80 | +/-30 | 4.2 |
| 3 | POWER | 1 | | 30 | 1.18 | +/-10 | |
| | | | PP 1080X1(RC68%) | 82 | 3.23 | +/-14 | 4.2 |
| 4 | BOTTOM | 1 | | 30 | 1.18 | +/-10 | |
| S/M | | | | 18 | 0.71 | +/-10 | 3.8 |
| | | | 总计： | 1583 | 62.32 | | |

Figure 3-2 Four layers PCB design

### 3.1.3 RK3568 Fan-out Design

- Ball fan-out design of the outer two circles

For the outermost balls, you can go out from the TOP layer with a line width of 4mil; the signal of the second circle goes out from the middle of the two balls with a line width of 4mil. It is recommended to set a grid and go out from the middle of the two balls.

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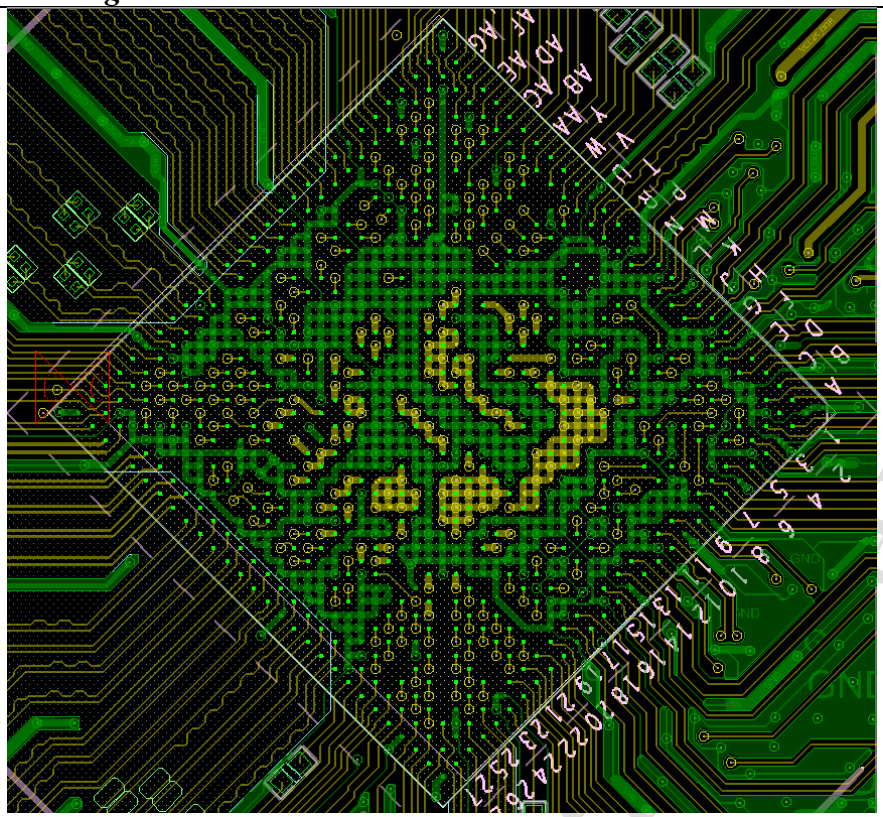

Figure 3-3 RK3568 Fan-out diagram 1

- Ball fan-out design in inner circles

If the signals of the first and second circles are useful, then starts from the third circle, if it needs to change to inner layers. Please make sure to follow the rules of layer changing vias, and it is recommended to place layer changing via at intervals of 2-4 rows, and leave an empty row not placing layer changing vias to keep as large a channel as possible for the ground layer and the power layer.

The ground layer copper covering situation shown in the figure below, there are multiple channels connected with the outside ground, which is good for SI/PI and heat dissipation

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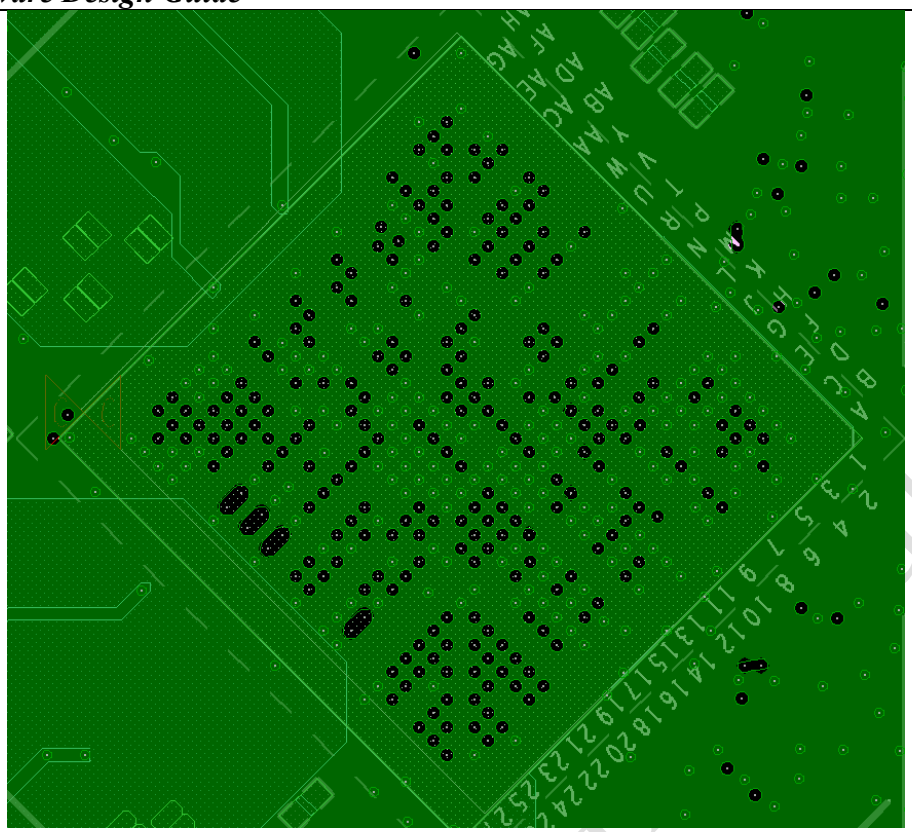

Figure 3-4 RK3568 Fan-out diagram 2

From the power layer copper covering situation shown in the figure below, we can see that, the regular placement of vias make various power sources having as much copper covering channels as possible, and improving the quality of power supply effectively.

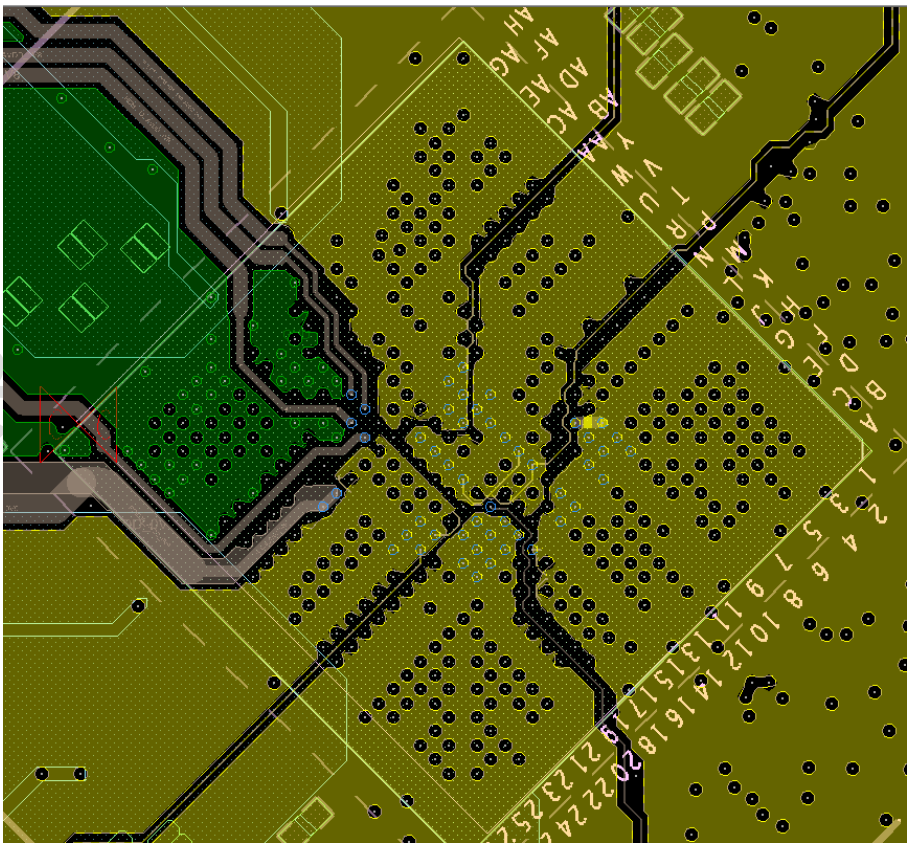

Figure 3-5 RK3568 Fan-out diagram 3

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The trace of bottom layer (the trace of inner layer is similar) is shown in the figure below, the layer-changing vias are set according to the grid and placed in the middle of balls, and 3.5mil line width fanned out between two vias.

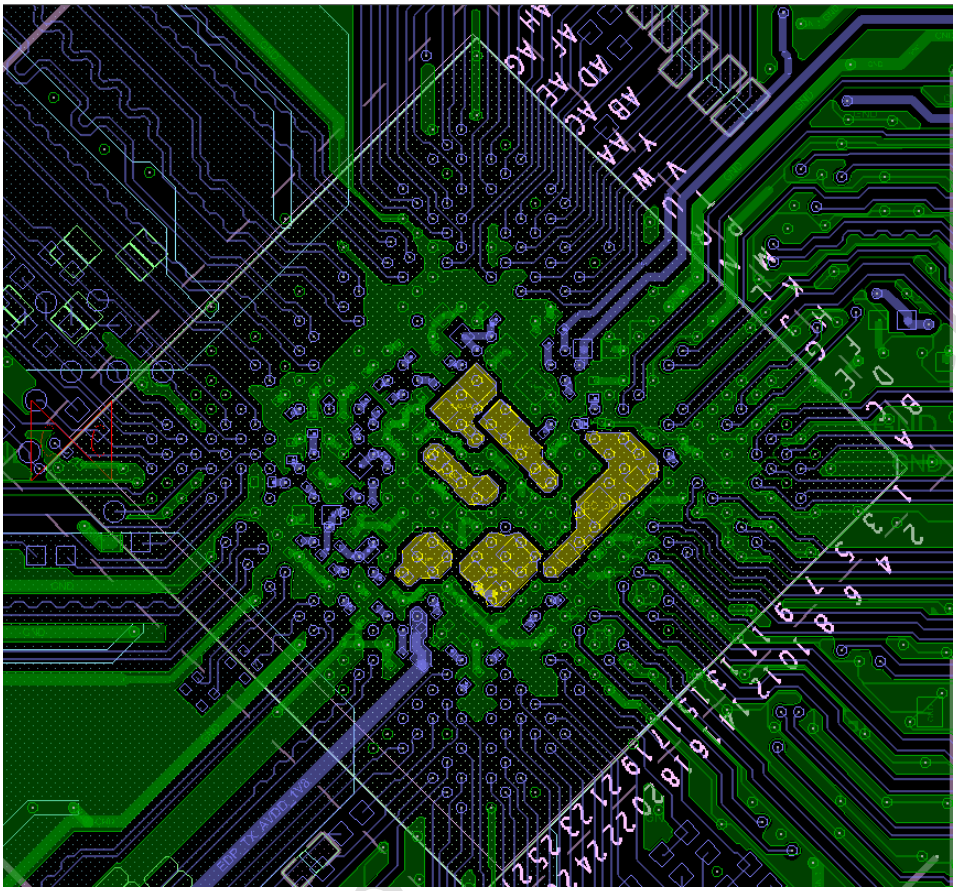

Figure 3-6 RK3568 Fan-out diagram 4

## 3.2 Interface PCB Design Recommendations

For high-speed PCB design constraints, please refer to the introduction and the constraints of the general rules for high-speed PCB design in the "Rockchip_RK3568_High_Speed_PCB_Design_Guide" document

- The length of the trace controlling should include the length of package and the length of via
- Below is a diagram of space between signals

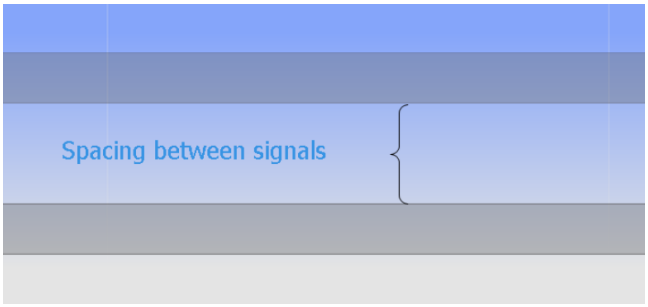


Figure 3-7 A diagram of space between signals

- Below is a diagram of equal length within and between differential pairs

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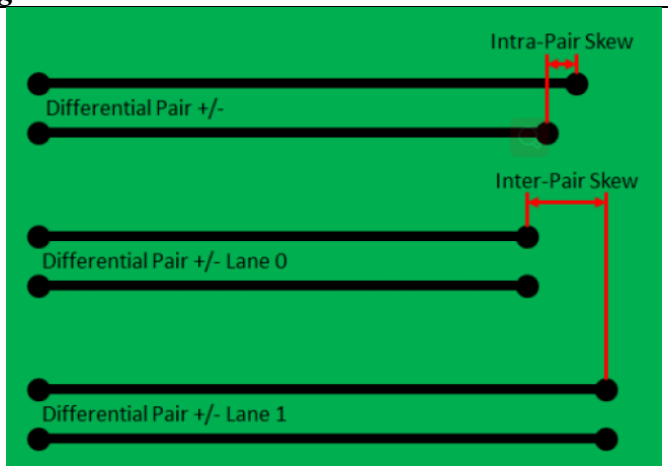


Figure 3-8 A diagram of equal length within and between differential pairs

- When doing equal length inner the differential pair, normally, serpentine line is used to compensate for length differences. In order to reduce the impedance disconnection, the requirements for the serpentine line are as shown in the figure below. In addition, pay attention to that the serpentine line for compensation should be as close as possible to the change point when doing length compensation

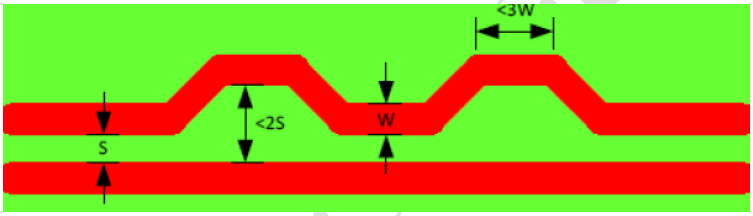


Figure 3-9 A diagram of differential pair length compensation requirements

- When the signal reference plane changes, it should refer to the ground plane too, and the stitching vias should be close to the signal vias; for differential signals, it is recommended that the distance between the stitching vias and the signal vias should be less than 30mil

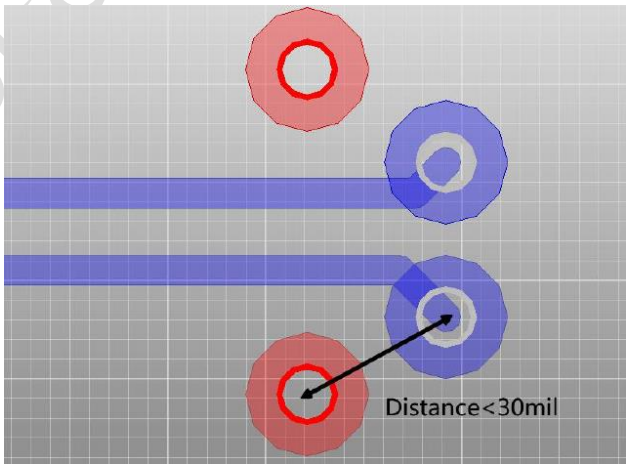


Figure 3-10 Stitching vias requirement diagram

- Try to avoid routing high-speed signals on the edge of the reference plane, otherwise it will affect impedance. It is recommended that the distance from high-speed signal to the edge of the reference plane is greater than or equal to 40mil

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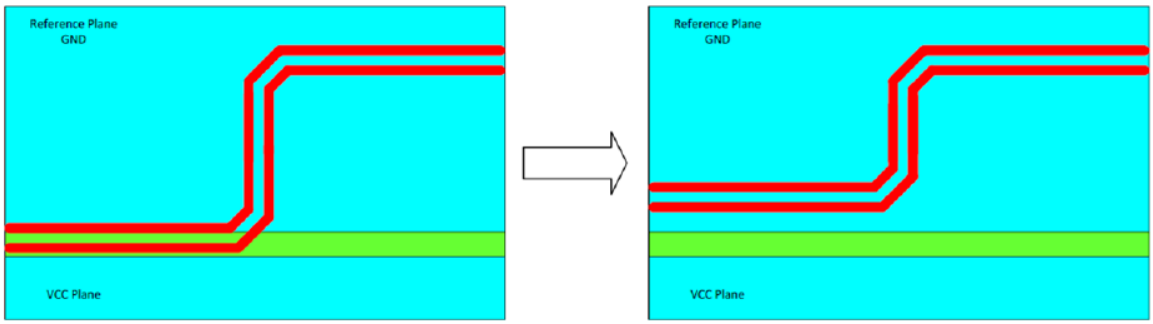


Figure 3-11 Edge requirement of signal reference plane diagram

- For other requirements, please refer to the description in the "Rockchip_RK3568_High_Speed_PCB_Design_Guide" document

### 3.2.1 Clock/Reset Circuit PCB Design

- Please pay attention to the following items in the PCB design of the clock circuit:
  - Give priority to the layout of the crystal circuit, which should be placed on the same layer as the chip and as close as possible to avoid drilling vias. The crystal trace should be as short as possible, away from interference sources, and as far as possible from the edge of the board;
  - The crystal and clock signal traces should be surrounded by ground throughout the whole process, and at least one GND via is added every 200-300mil for the surrounded ground line, and it is necessary to ensure the integrity of the ground reference plane of the neighboring layer;
  - If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground throughout the whole process, to avoid interference;
  - Clock traces Xin, Xout and the projection area under the crystal are prohibited from any traces to avoid noise coupling into the clock circuit;
  - A ground loop can be placed around the top layer under the crystal. The ground loop is connected to the neighboring ground layer through vias to isolate noise;
  - The second layer under the crystal maintains a complete ground reference plane to avoid any trace division, which helps to isolate noise and maintain the crystal output

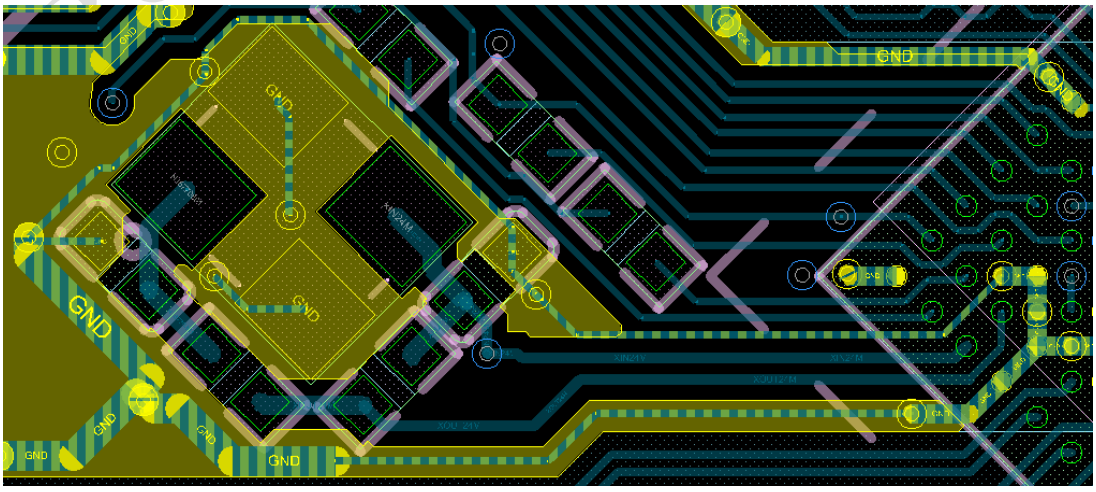


Figure 3-12 RK3568 Crystal layout and routing

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- The decoupling capacitor of the power supply must be placed on the back of the chip pin. Try to go through the capacitor pad and then to the chip pin when routing.

- Pay attention to the following items in the PCB design of the reset circuit:
  - During layout, the RESETn reset signal should be kept away from the edge of the board and metal connectors to prevent the reset module from crashing due to abnormalities caused by ESD.
  - The RESETn filter capacitors layout should be placed as close as possible to the chip pin. The signal must pass through the capacitors before entering the chip. Note that each ground pad of the filter capacitors must be with a 0402 ground via. It is recommended to place more than two grounding vias if space allowed.
  - The RESETn signal should be far away from strong interference signals such as DCDC and RF to prevent interference. If the trace is long, it is recommended to be surrounded by ground and add at least one GND vias every 400 mils.
  - The TVS protection diodes of the RESETn button should be placed as close as possible to the buttons. The signal topology is: button--->TVS--->100 ohm--->Capacitor (near CPU&PMIC) --->CPU&PMIC; when ESD occurs, The ESD current must be attenuated by the TVS components first.

## 3.2.2 PMIC/Power Circuit PCB Design

### 3.2.2.1 RK809-5 power supply PCB design solution

- In the overall layout, from the perspective of power quality, RK809-5 should be placed as close as possible to RK3568 (when considering heat dissipation design, it needs to be placed properly, not too close or too far away. It is recommended that the interval is between 20mm-50mm, and try not to place it on the edge of the board to avoid bad heat dissipation). For placing direction, it is necessary to make the trace (copper covering) of RK809-5 BUCK output to RK3568 be smooth without crossing.
- RK809-5 BUCK1/BUCK2 PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor and VCC1/2 and GND should be as small as possible. The tracing of SW1/2 should be as short as possible to prevent interference to other modules; the tracing of VFB1/2 should be as close as possible to SW1/2. For places that need to place vias: VCC1/2 needs at least 4 pieces 0.5*0.3mm vias, and VBUCK1/2 needs at least 5 pieces 0.5*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

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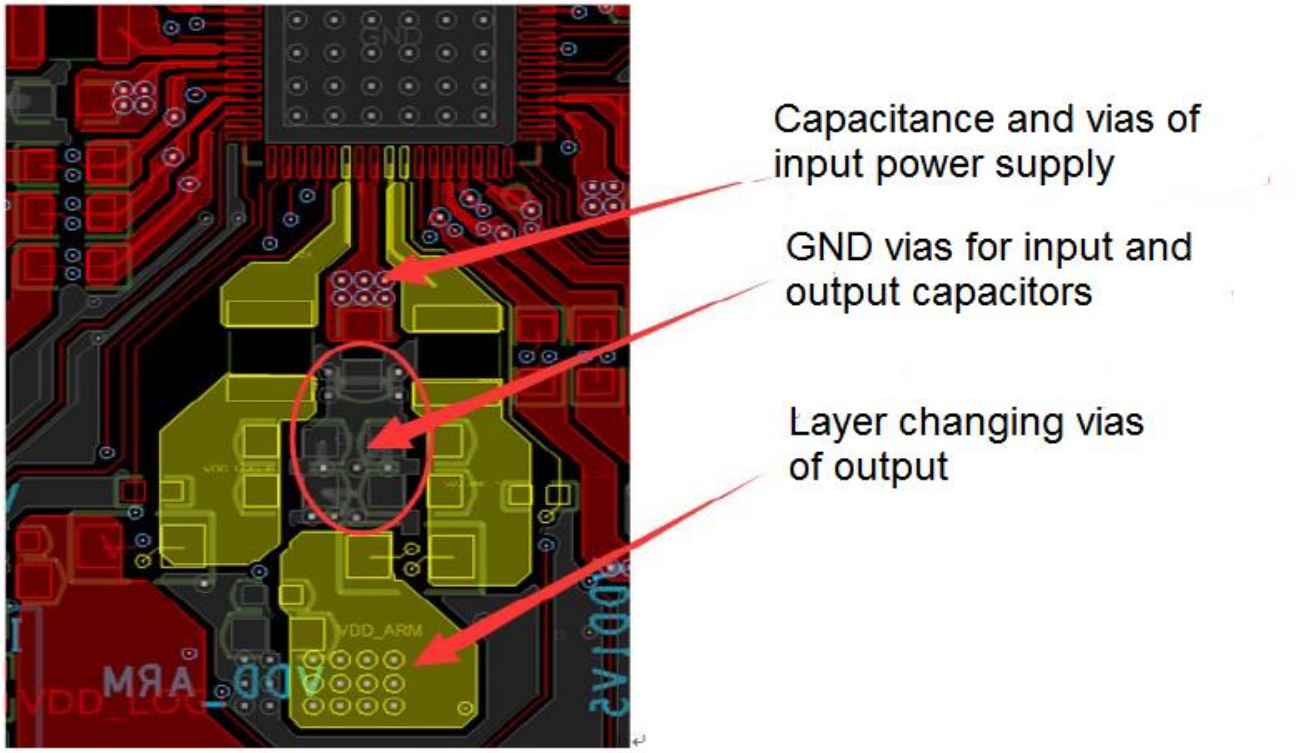


Figure 3-13 RK809-5 BUCK1/BUCK2 Layout and routing

- K809-5 BUCK3 PCB design requirements：

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC3 and GND should be as small as possible. The tracing of SW3 should be as short as possible to prevent interference to other modules; the tracing of VFB3 should be as close as possible to SW3.

For places that need to drill vias, VCC3 needs at least three 0.5*0.3mm vias, and VBUCK3 needs at least five 0.5*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

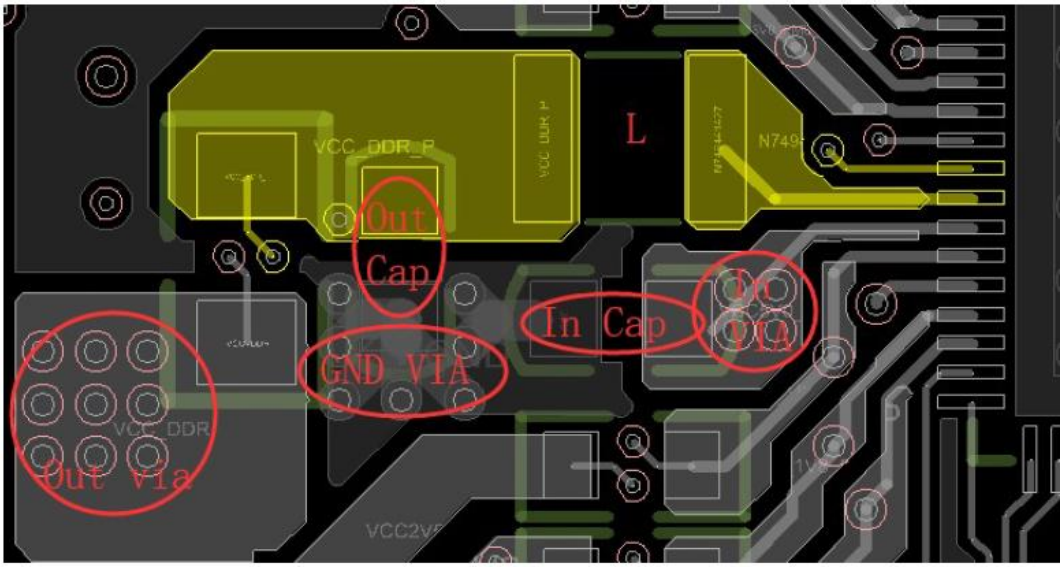


Figure 3-14 RK809-5 BUCK3 Layout and routing

- RK809-5 BUCK4 PCB design requirements：

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The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC4 and GND should be as small as possible. The tracing of SW4 should be as short as possible to prevent interference to other modules; the tracing of VFB4 should be as close as possible to SW4.

For places that need to drill vias, VCC4 needs at least three 0.5*0.3mm vias, and VBUCK4 needs at least five 0.5*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

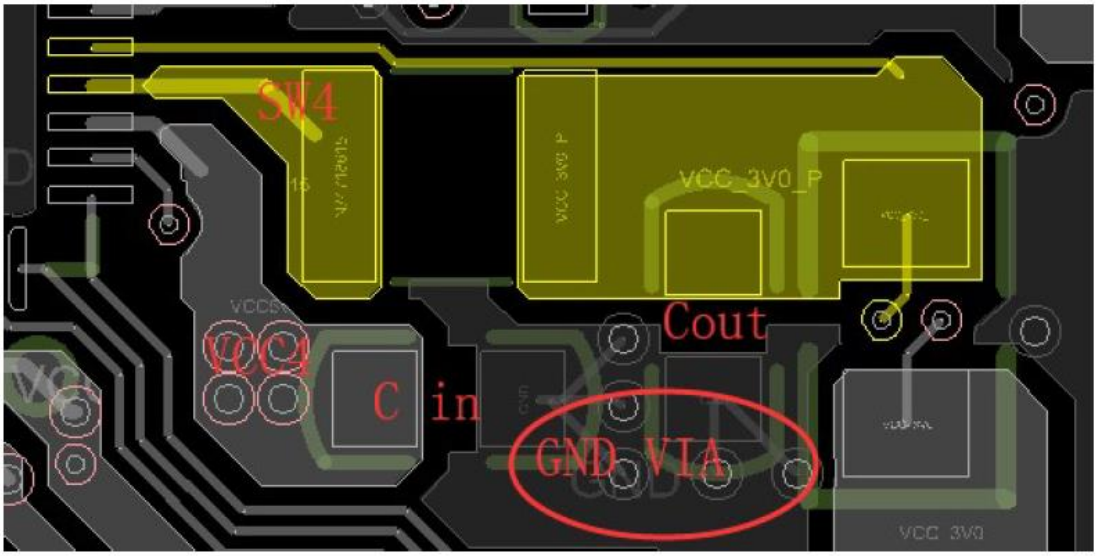


Figure 3-15 RK809-5 BUCK4 Layout and routing

■ RK809-5 BUCK5 PCB design requirements：

The input capacitors must be as close as possible to the chip, and the connection loop between the input capacitors, VCC9 and GND should be as small as possible. The tracing of SW5 should be as short as possible to prevent interference to other modules; the tracing of VFB5 should be as close as possible to SW5.

For places that need to drill vias, VCC9 needs at least three 0.5*0.3mm vias, and VBUCK5 needs at least five 0.5*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

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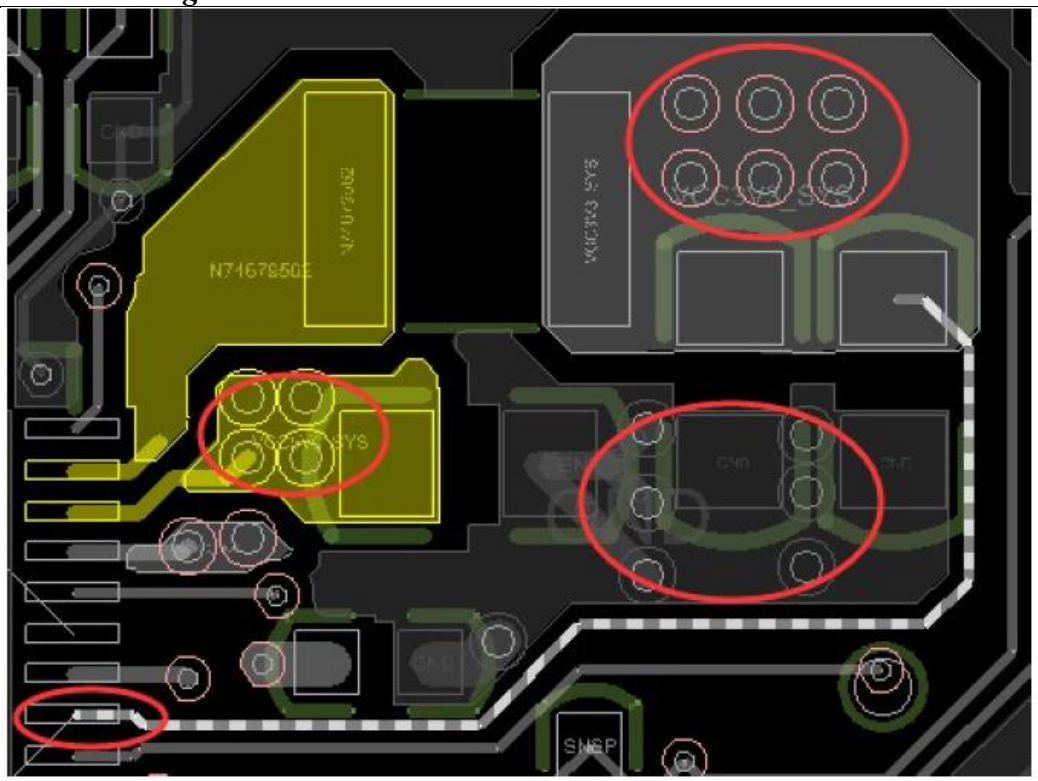


Figure 3-16 RK809-5 BUCK5 Layout and routing

- RK809-5 LDO PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC5/6/7/8 and GND should be as small as possible.

The output capacitor must be as close as possible to the chip, and the connection loop between the output capacitor, LDO1/2/3/4/5/6/7/8/9 and GND should be as small as possible.

- The XIN/XOUT signal traces of the 32.768KHz crystal of RK809-5 should be as short as possible, and the whole process should be surrounded by ground to ensure that there is a complete reference plane and no high-speed signals routing under the crystal circuit.
- The VREF capacitor of RK809-5 must be placed close to the pin and far away from other interference sources. The ground pad of the capacitor must be well grounded, that is, the path between the VREF capacitor ground pad and RK809-5 EPAD must be the shortest and must not be divided by other signals.
- 100nF capacitor of Pin 67 (RESETB) of RK809-5 must be close to RK809-5 pin
- It is recommended that the pins of RK809-5 should not be covered by copper. All pins are connected to the outside through tracing. The width of the tracing should not exceed the width of the pins to prevent the tin linking from pads becoming larger after the board is made.
- The EPAD ground pad of RK809-5 requires enough vias. It is recommended to ensure 5*5 pieces of 0.5*0.3mm or 6*6 pieces of 0.4*0.2mm vias to reduce ground impedance and enhance heat conduction.

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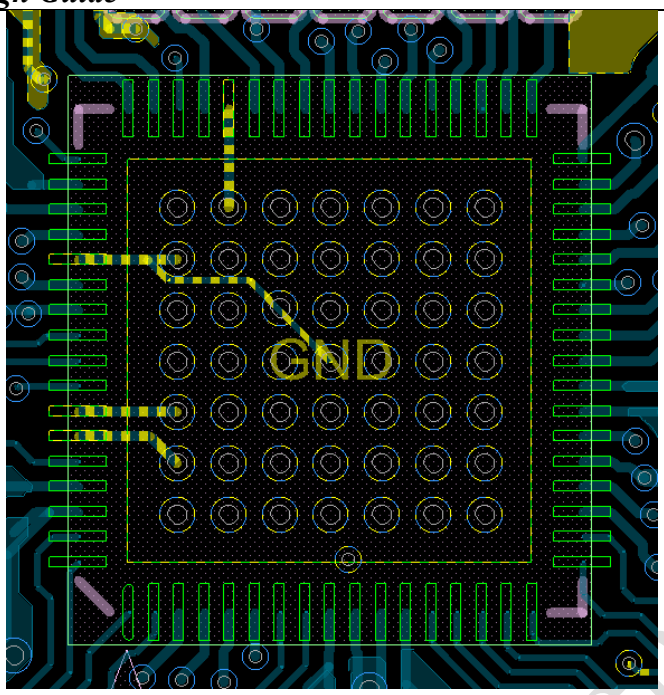


Figure 3-17 RK809-5 EPAD vias layout

#### 3.2.2.2 DC-DC PCB design of discrete power supply

- The input capacitor CIN and output capacitor COUT are placed between VIN pin, VOUT pin and DC/DC GND, try to reduce the loop area between VIN, VOUT and DC/DC GND, so as to reduce the power ripple amplitude , Greatly improve the reliability of the chip, as shown below.

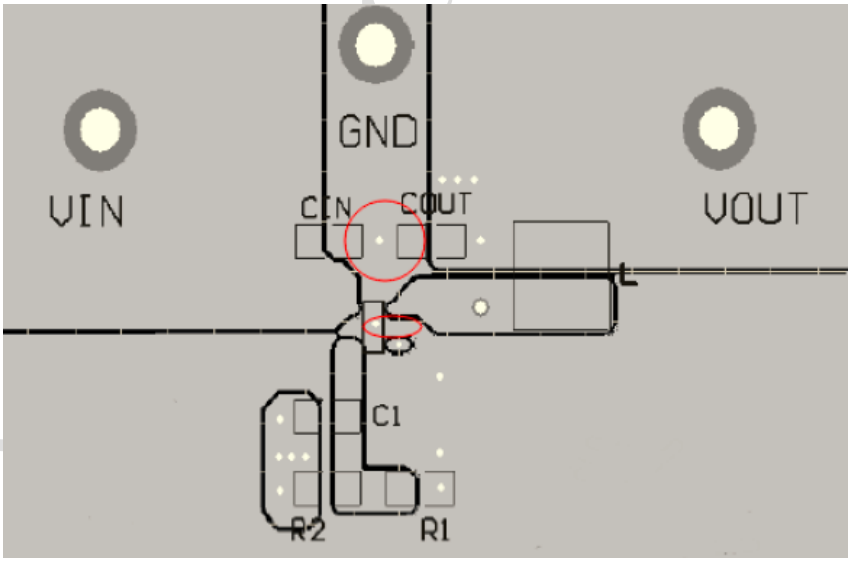


Figure 3-18 Discrete power supply DC/DC layout and routing

- The input capacitor CIN, output capacitor COUT and DC/DC GND require as many vias as possible. It is recommended to have more than four 0503 vias. If the VIN and VOUT power supply have changed layers, it is recommended to place more vias. Four 0503 vias or more are recommended (it is related to the current, which will be described below). The inductance should be as close as possible to the DC/DC, the trace should be as thick and short as possible, and the resistance ground of the FB end should be as far away as possible from the interference source.

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### 3.2.2.3 VDD_CPU DC-DC Power PCB design

- The design of VDD_CPU power supply is very important and directly affects the performance and stability of a product. Please design strictly according to RK's LAYOUT requirements.
- The VDD_CPU power supply uses TCS4525 by default, and the overall layout should close to RK3568 as much as possible. The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor and VIN and GND should be as small as possible. The SW trace should be as short as possible to prevent interference to other modules; the VOUT trace should try to avoid being too close to SW. The connection loop between the output capacitor and GND should be as small as possible.

For places that need to drill vias, VIN needs at least five 0.5*0.3mm vias, and Vbuck output needs at least twelve 0.5*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

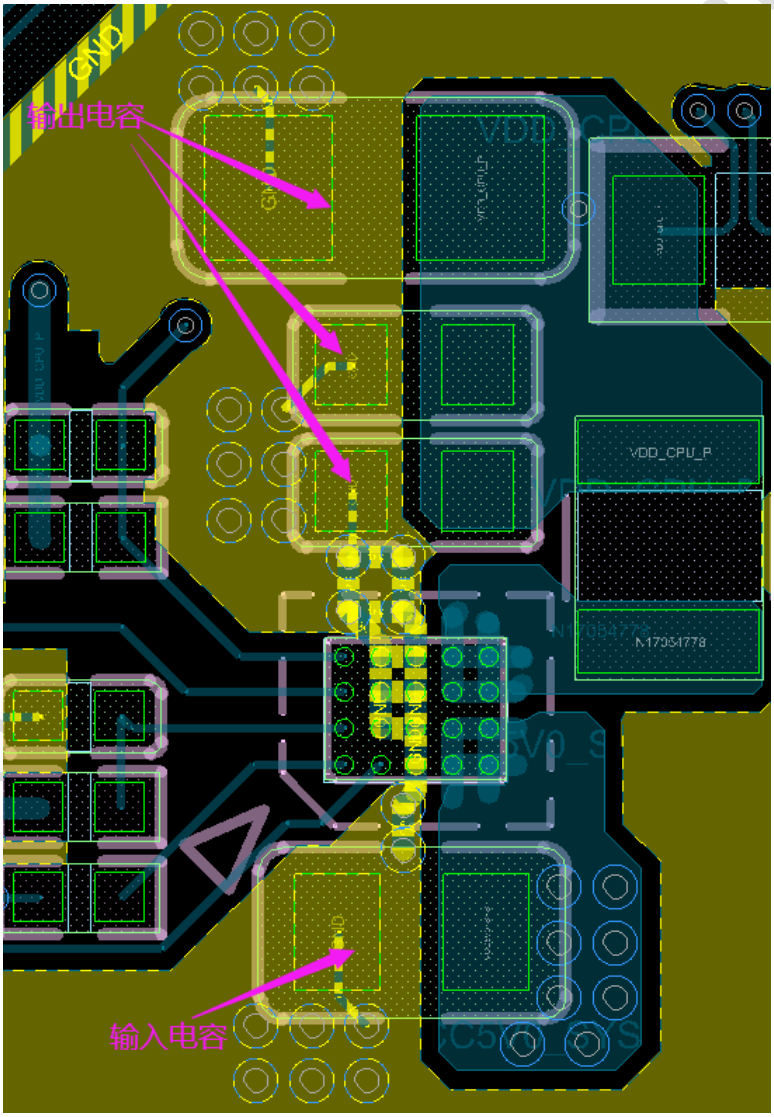


Figure 3-19 VDD_CPU Power supply DC/DC layout and tracing

### 3.2.2.4 VDD_LOGIC,VDD_GPU,VDD_NPU,VDD_CPU power supply DC-DC remote feedback design

- The 100ohm feedback resistor should to be placed close to the output capacitor. One end of the resistor is

connected to the DC-DC output capacitor, the other end is connected to the FB feedback pin of the PMIC, and RK3568 power pin is connected to the most remote load of the same power network at the same time. The width of the feedback trace is 4mil, and it must be routed following the power supply copper to avoid interference; the feedback line is more than 6mil apart from other signals,

Such as the following diagram of VDD_GPU power supply copper-covering and feedback line routing, other power supplies are similar.

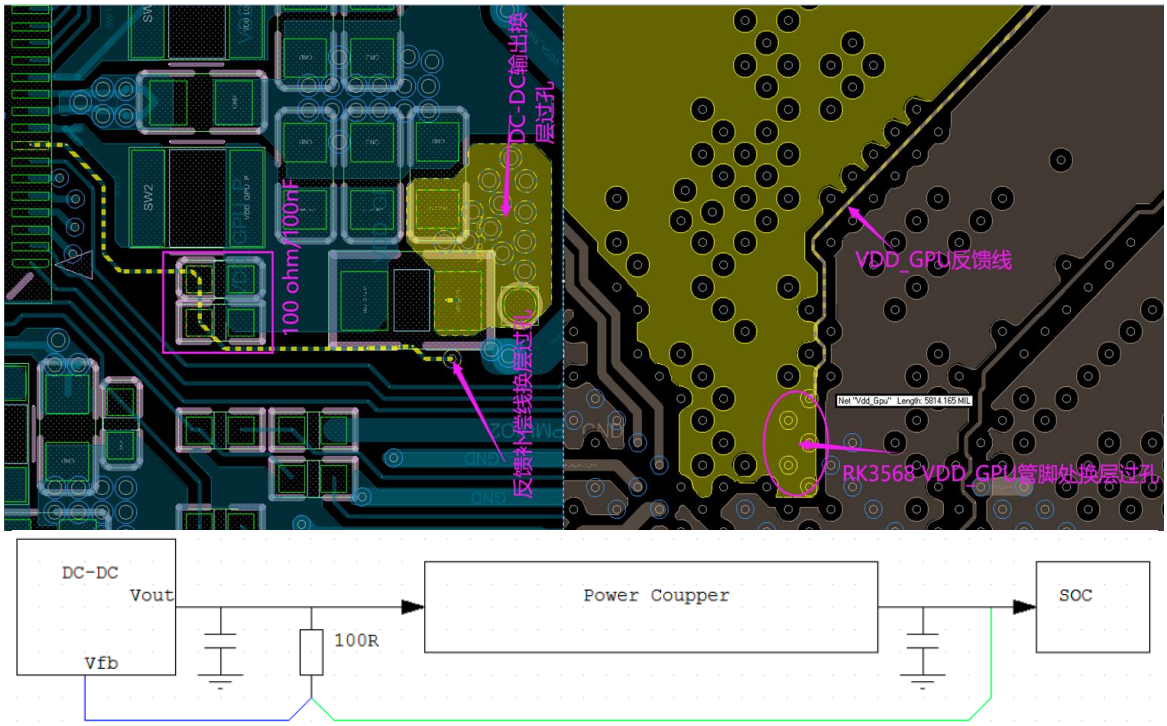


Figure 3-20 A diagram of DC/DC remote feedback design

### 3.2.2.5 RK3568 VDD_CPU Power PCB design

- The copper-covering width of VDD_CPU should meet the current requirement of the chip. The copper-covering connected to the power pins of chip should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of CPU must be enough.
- When changing layer in peripheral, it is necessary for VDD_CPU power supply to drill as many power vias as possible (more than twelve 0.5*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For RK3568 chip VDD_CPU power supply pin, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

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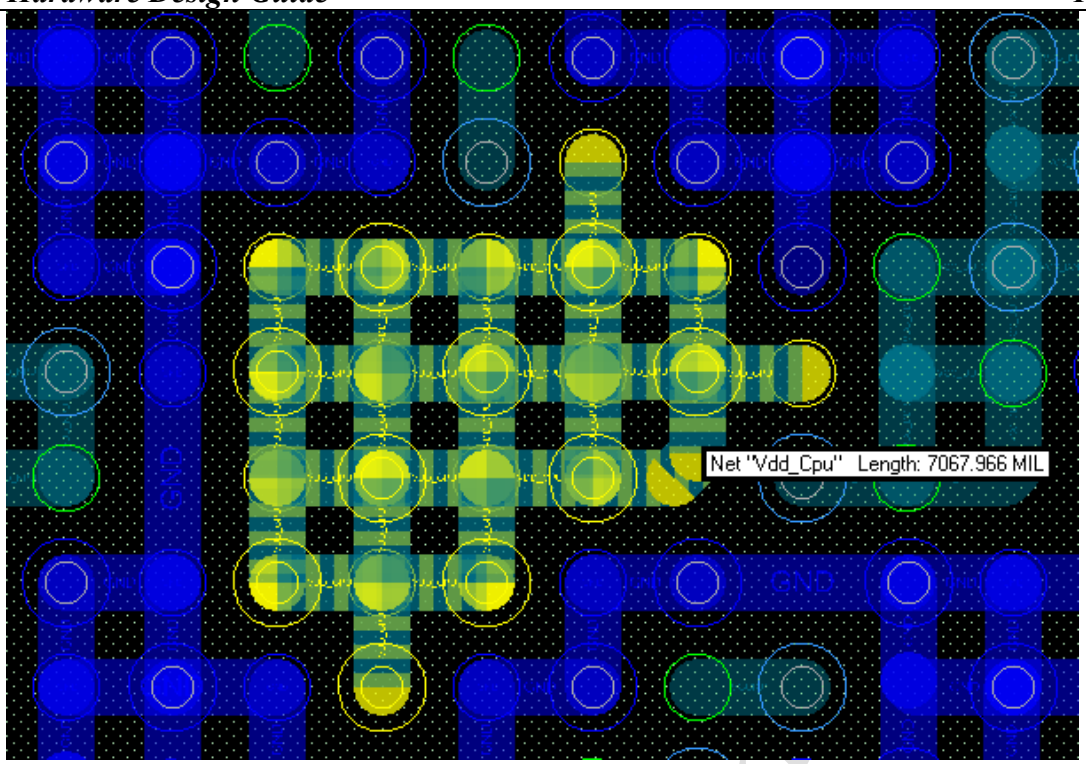


Figure 3-21 RK3568 VDD_CPU Power pin routing and vias

- On the schematic, the decoupling capacitors close to the VDD_CPU power pin of RK3568 must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of decoupling capacitors should be placed as close as possible to RK3568.

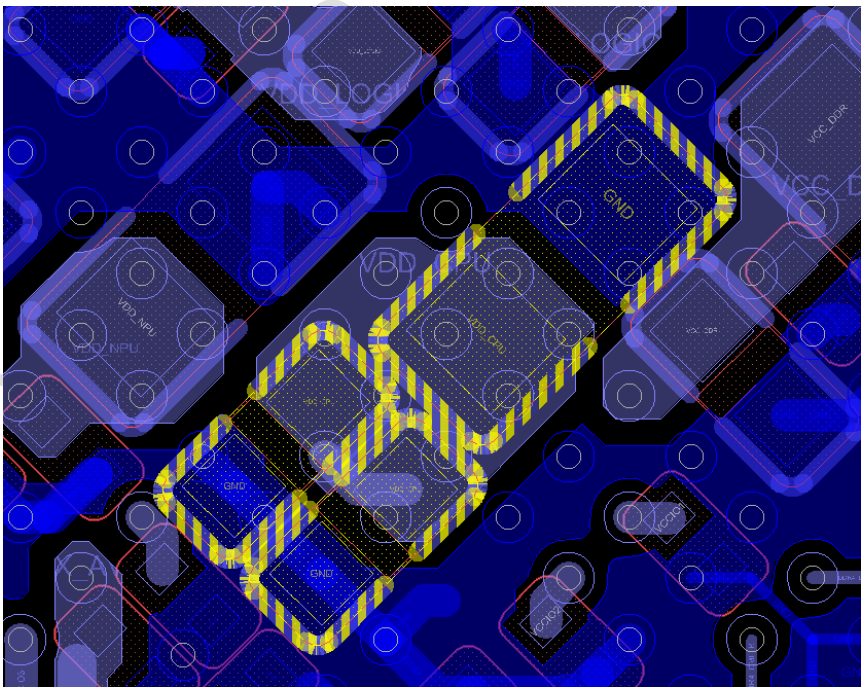

Figure 3-22 Placement of decoupling capacitors on the back of RK3568 VDD_CPU power pins

- The trace width of the VDD_CPU power supply in the CPU area should not be less than 90mil, and the trace width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the

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voltage drop caused by the routing (please do not place layer change vias of other signal at will, they must be placed regularly, try to free up space for power supply and it is good for copper covering of ground)

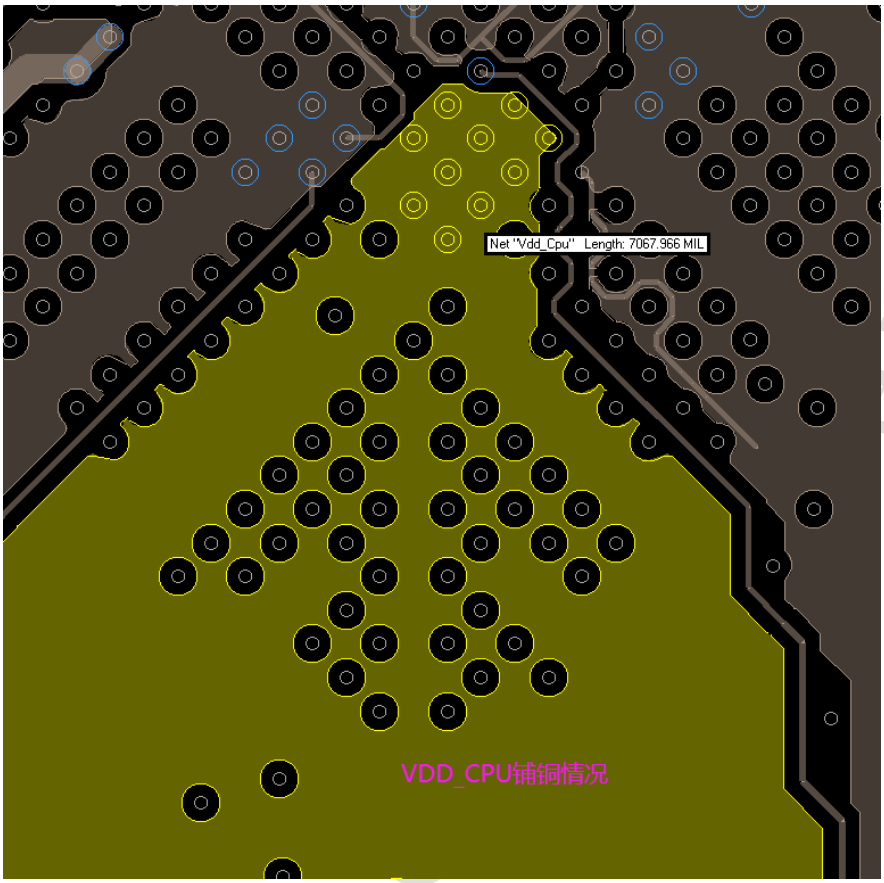


Figure 3-23 Copper-covering on RK3568 VDD_CPU power layer

#### 3.2.2.6 RK3568 VDD_LOGIC Power PCB design

- The copper-covering width of VDD_LOGIC should meet the current requirement of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough
- When changing layer in peripheral, it is necessary for VDD_LOGIC power supply to drill as many power vias as possible (more than twelve 0.5*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD_LOGIC of RK3568, each ball requires a via, and they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

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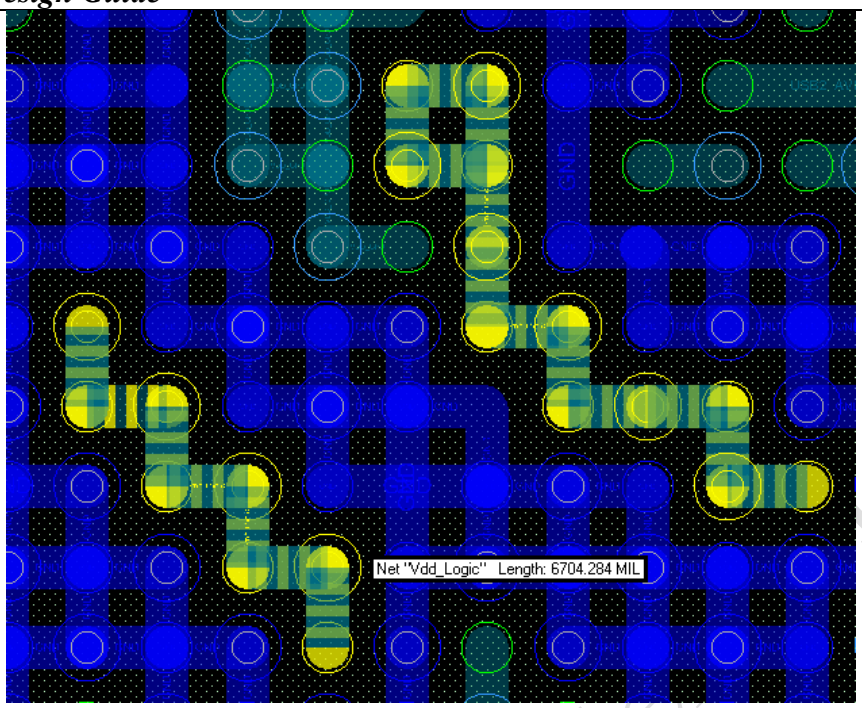


Figure 3-24 RK3568 VDD_LOGIC power supply pin routing and vias

- The decoupling capacitors close to the VDD_LOGIC power pin of RK3568 in the schematic must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of decoupling capacitors should be placed as close as possible to RK3568.

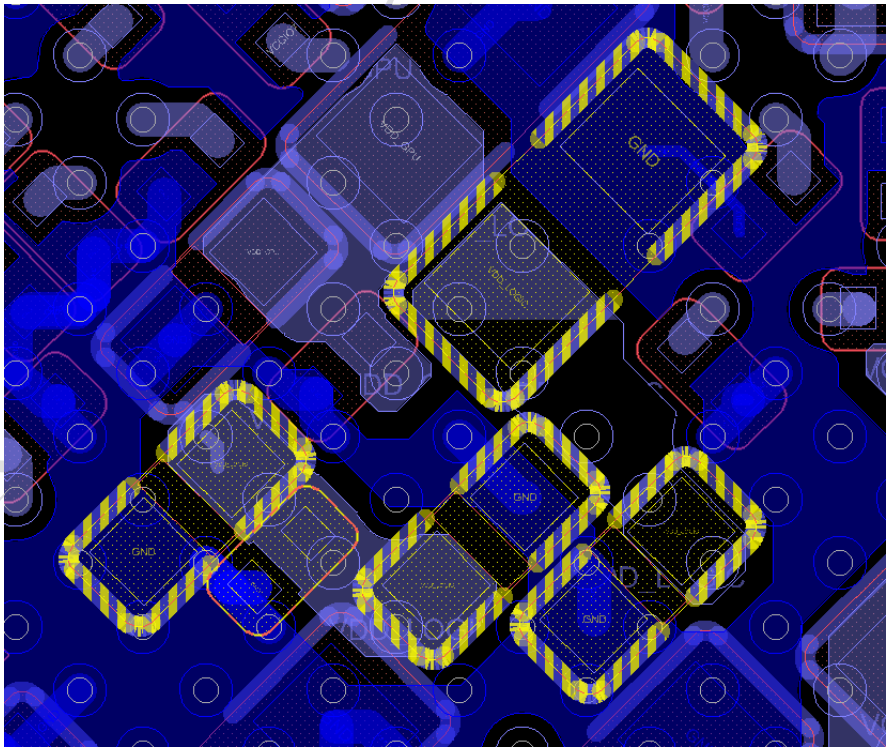

Figure 3-25 Placement of decoupling capacitors on the back of RK3568 VDD_LOGIC power pins

- The width of VDD_LOGIC power supply in the CPU area should not be less than 60mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be

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placed regularly, try to free up space for power supply and it is also good for copper covering of ground)

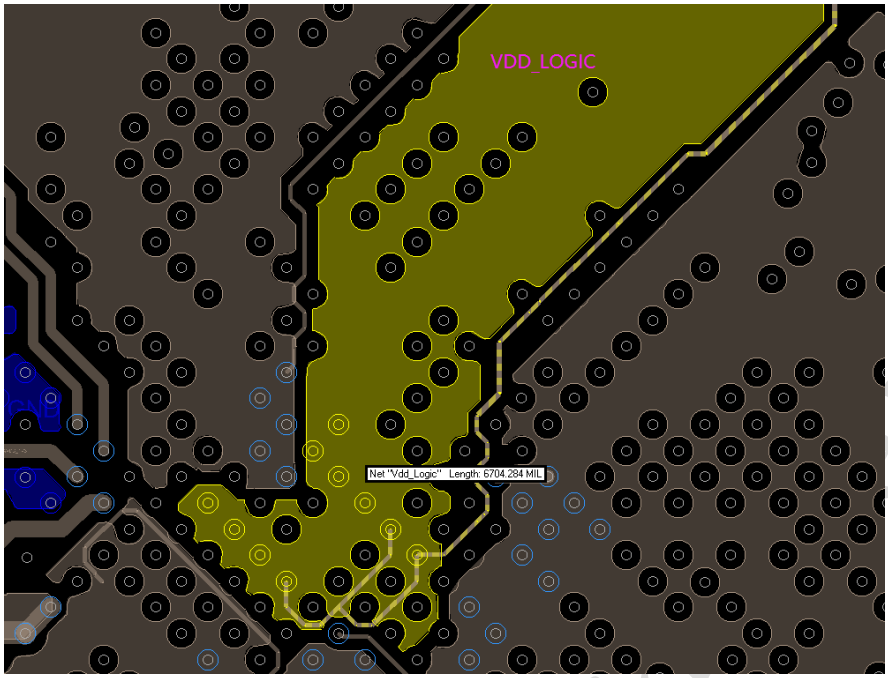


Figure 3-26 Copper-covering on RK3568 VDD_LOGIC power layer

#### 3.2.2.7 RK3568 VDD_GPU Power PCB design

- The copper-covering width of VDD_GPU should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough
- When changing layer in peripheral, it is necessary for VDD_GPU power supply to drill as many power vias as possible (more than five 0.5*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD_GPU of RK3568, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

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Figure 3-27 RK3568 VDD_GPU Power pin traces and vias

- The decoupling capacitors close to the VDD_GPU power pin of RK3568 on the schematic, must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

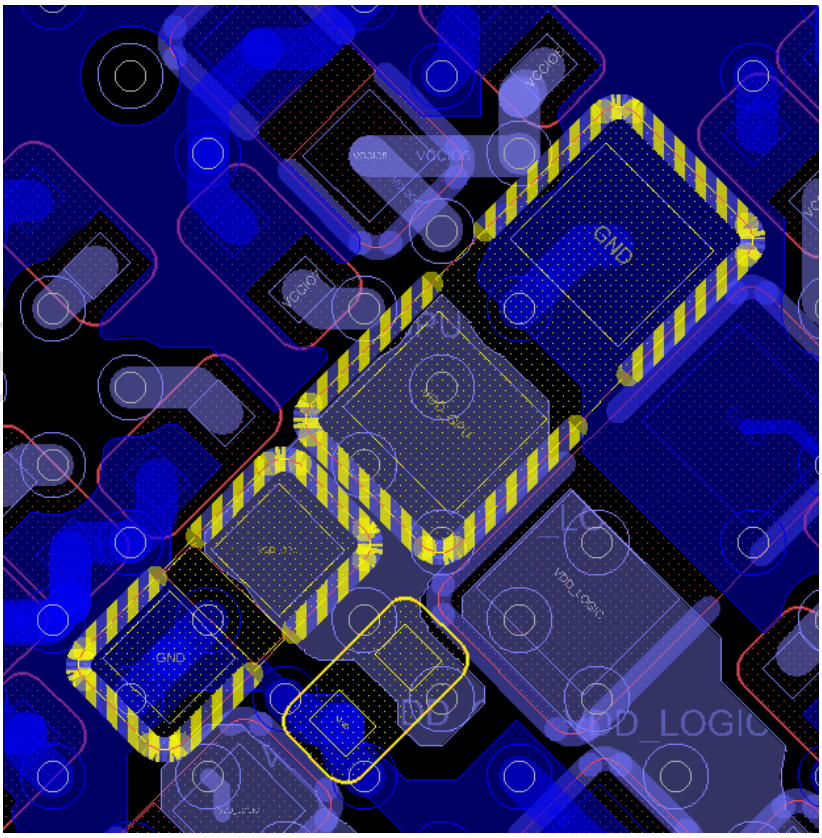

Figure 3-28 Placement of decoupling capacitors on the back of RK3568 VDD_GPU power pins

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- The trace width of the VDD_GPU power supply in the CPU area should not be less than 50mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground)

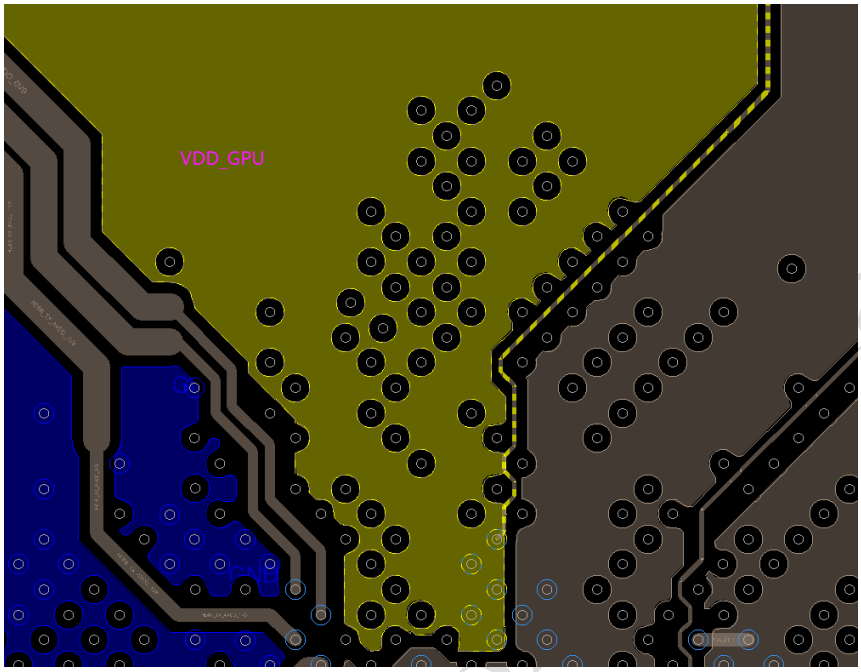


Figure 3-29 Copper covering on RK3568 VDD_GPU power layer

#### 3.2.2.8 RK3568 VDD_NPU Power PCB design

- The copper-covering width of VDD_NPU should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough.
- When changing layer in peripheral, it is necessary for VDD_NPU power supply to drill as many power vias as possible (more than five 0.5*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD_NPU of RK3568, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

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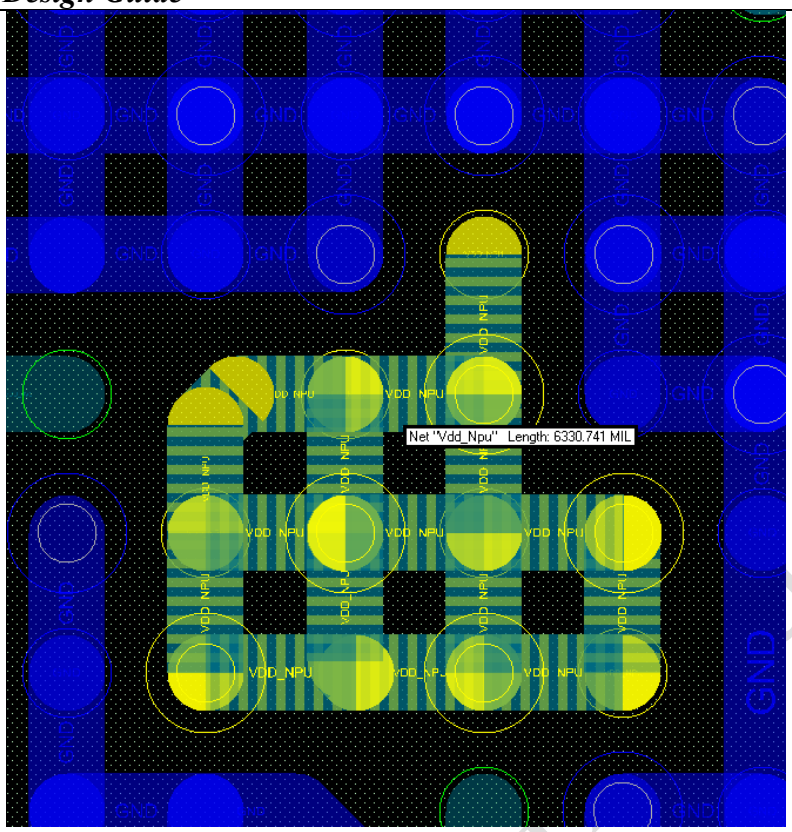


Figure 3-30 RK3568 VDD_NPU Power pin routing and vias

- The decoupling capacitor close to the VDD_NPU power pin of RK3568 on the schematic, must be placed on the back of the corresponding power pin. The GND pad of the capacitor should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

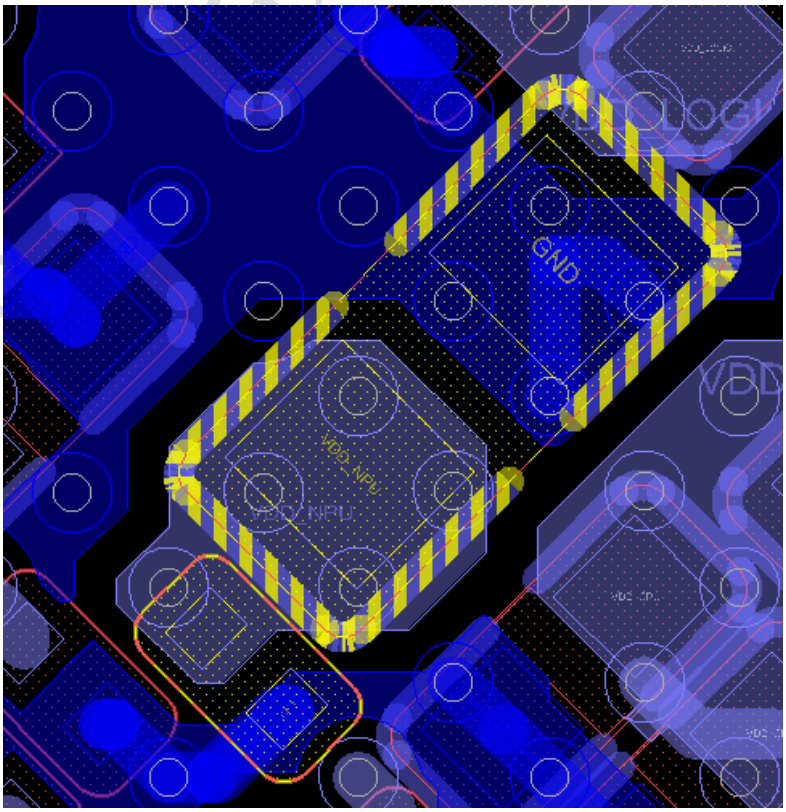


Figure 3-31 Placement of decoupling capacitors on the back of VDD_NPU power

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- The trace width of the VDD_NPU power supply in the CPU area should not be less than 50mil, and the trace width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground)

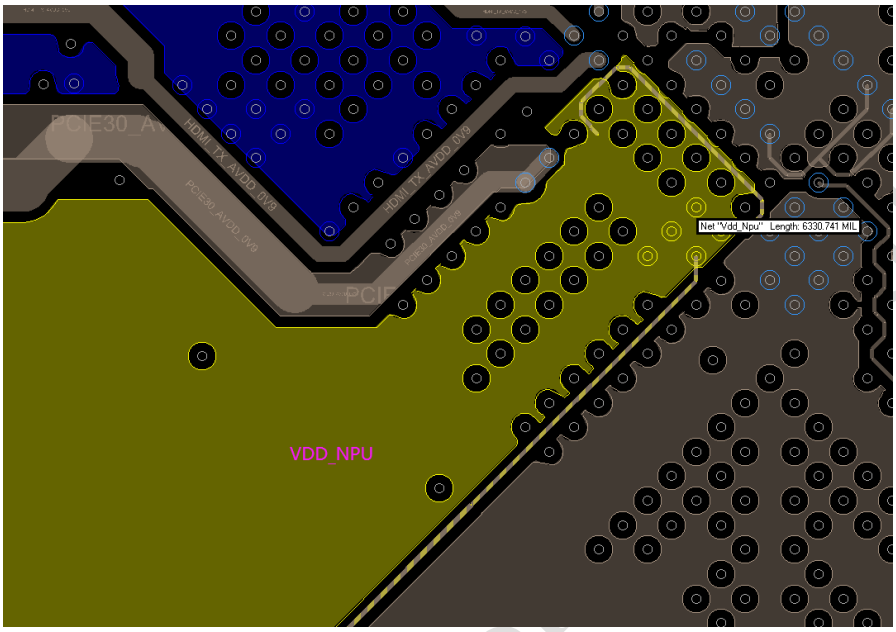


Figure 3-32 Copper covering on RK3568 VDD_NPU power layer

#### 3.2.2.9 RK3568 VCC_DDR Power PCB design

- The copper-covering width of VCC_DDR should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough.
- When changing layer in peripheral, it is necessary for VCC_DDR power supply to drill as many power vias as possible (more than eight 0.5*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VCC_DDR of RK3568, each ball requires a via, and they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

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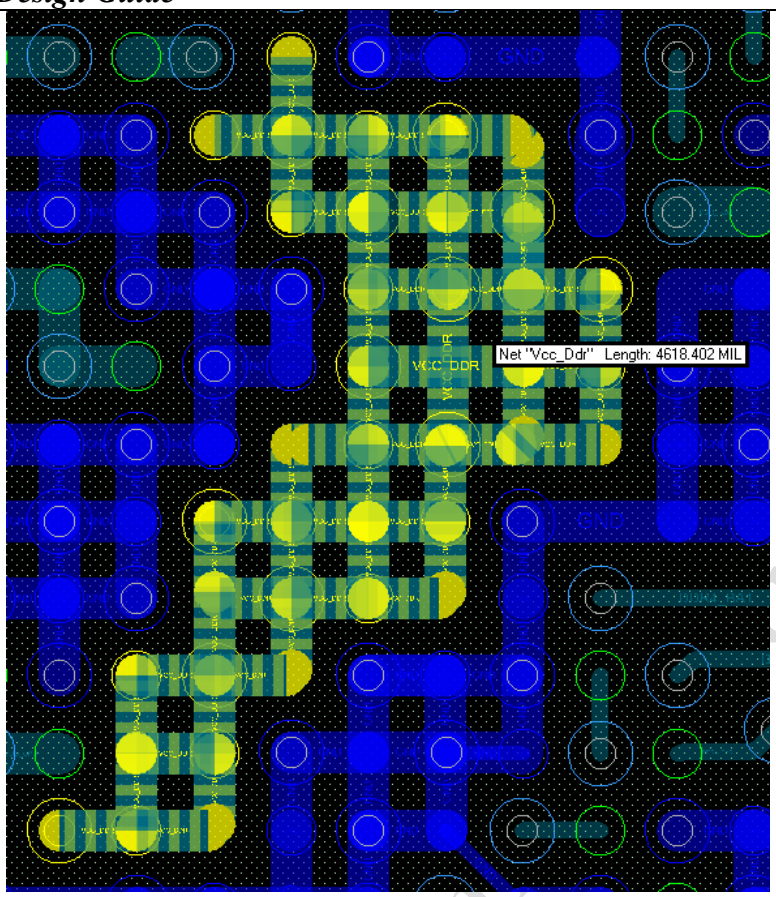


Figure 3-33 RK3568 VCC_DDR power pin routing and vias

When using LPDDR4x：

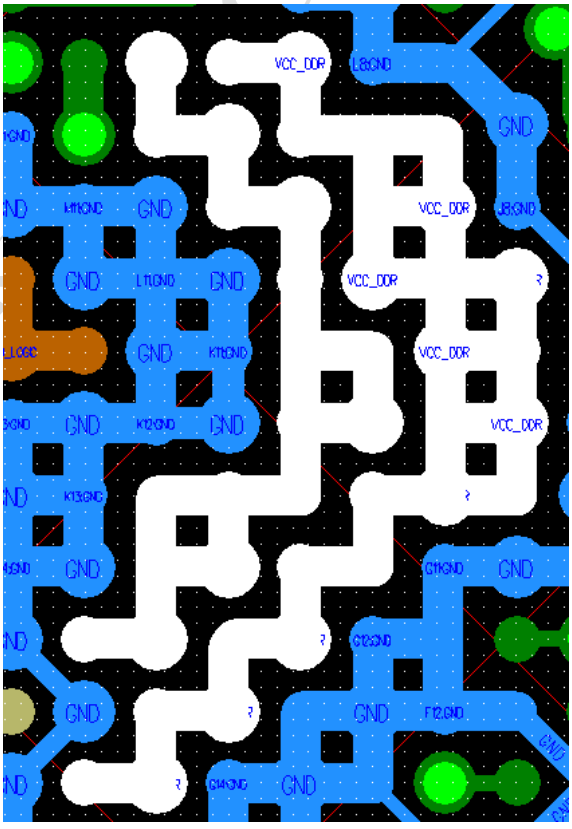


Figure 3-34 RK3568 VCC_DDR/VCC0V6_DDR Power pin routing and vias in LPDDR4x mode

- The decoupling capacitor close to the VCC_DDR power pin of RK3568 on the schematic, must be placed

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on the back of the corresponding power pin. The GND pad of the capacitor should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

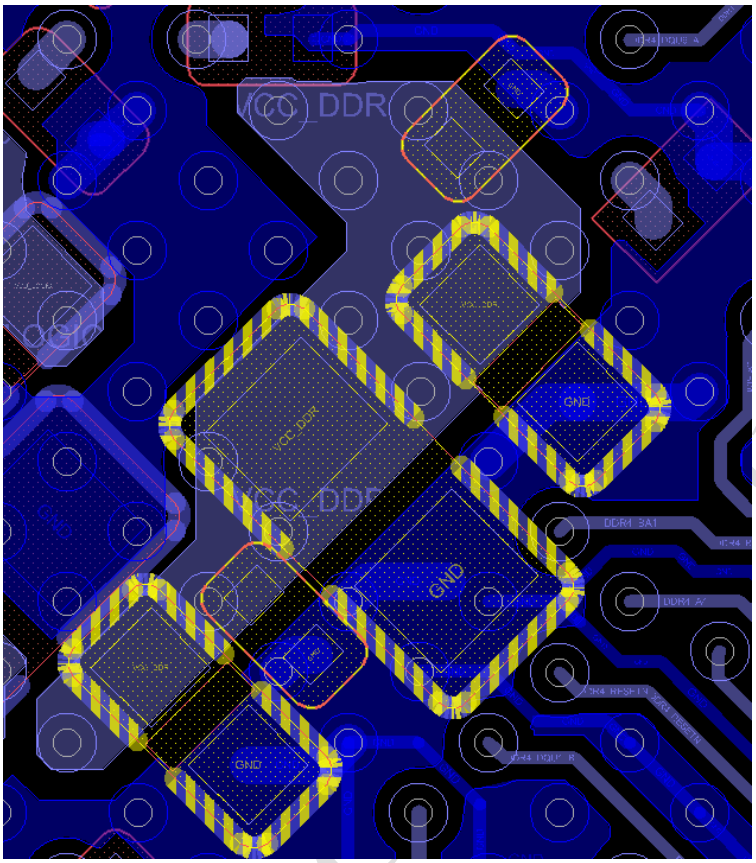


Figure 3-35 Placement of decoupling capacitor on the back of the power supply pin of RK3568 VCC_DDR

When in LPDDR4x mode：

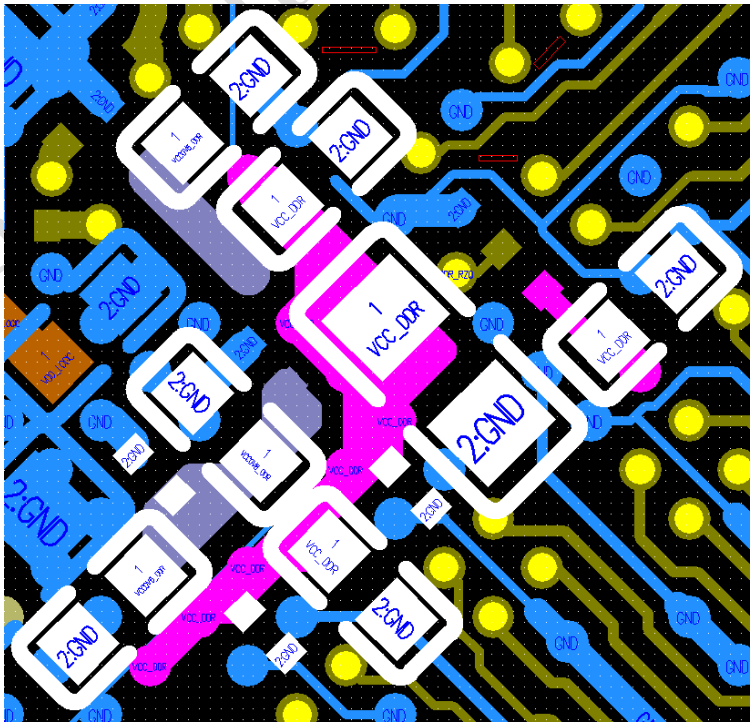


Figure 3-36 Placement of decoupling capacitors on the back of the power supply pins of VCC_DDR/VCC0V6_DDR of RK3568 in LPDDR4x mode

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- The trace width of VCC_DDR power supply in the CPU area should not be less than 120mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground) If it is a 4-layer board, the signal of the bottom layer has to take this plane as reference. Please refer to the description in the DRAM circuit PCB design for attentions.

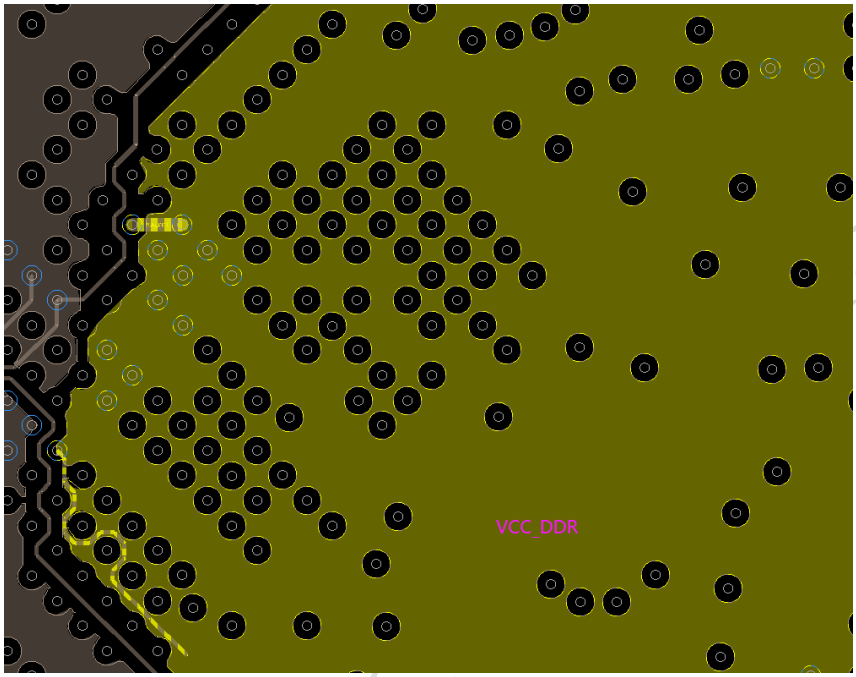


Figure 3-37 Copper covering on RK3568 VCC_DDR power layer

#### 3.2.2.10 RK3568 GND pin PCB design

- For the GND pin of RK3568, ensure that every 1.5 ball correspond to a vias at least, and try to match a via to each ball, which provides better SI and PI conditions and is also helpful for heat dissipation.
- The neighboring layer of RK3568 chip must be a complete GND plane to ensure that the main reference ground is close to the Ball of CPU, to ensure the integrity of the power supply and enhance the heat dissipation of the PCB.
- The GND ball of the same network under RK3568 chip is in a "井" shape on the top layer, and is cross-connected. It is recommended that the trace width is 10mil.

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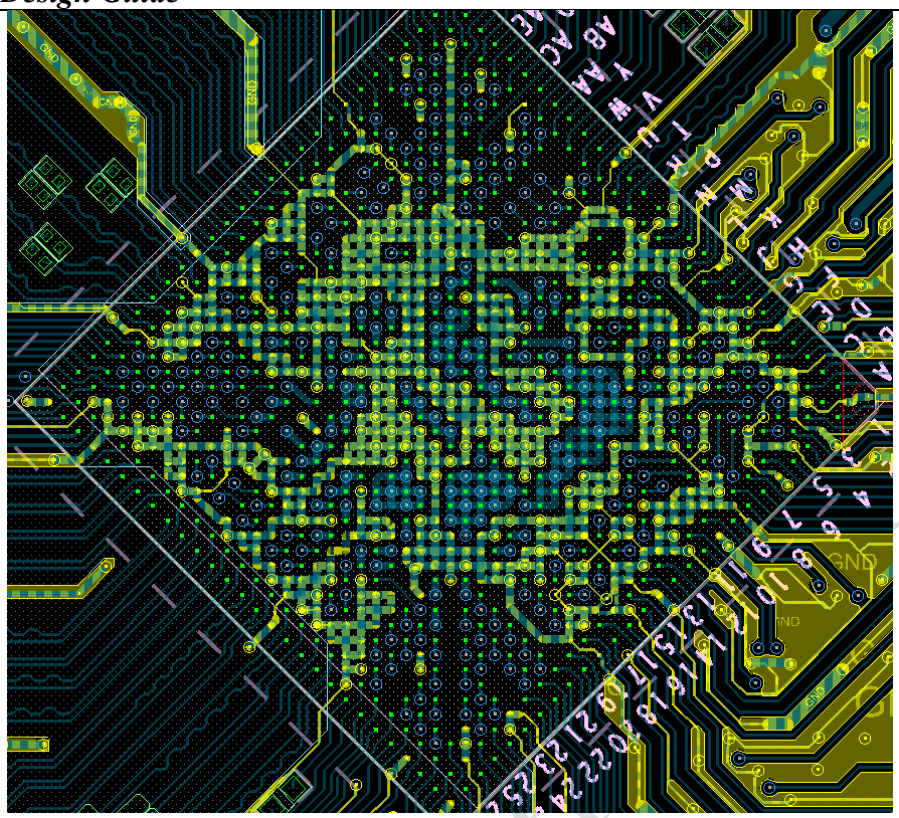

Figure 3-38 RK3568 VSS pin routing and vias

- The layer changing vias of each RK3568 signals should be place in the middle of the ball interval and regularly when layout, as shown in the figure, the ground in the middle of the rk3568 chip has a large area of copper connected with the outer ground copper. On the one hand, it is good for power supply and signal integrity, and on the other hand, it is good for heat dissipation of the chip.

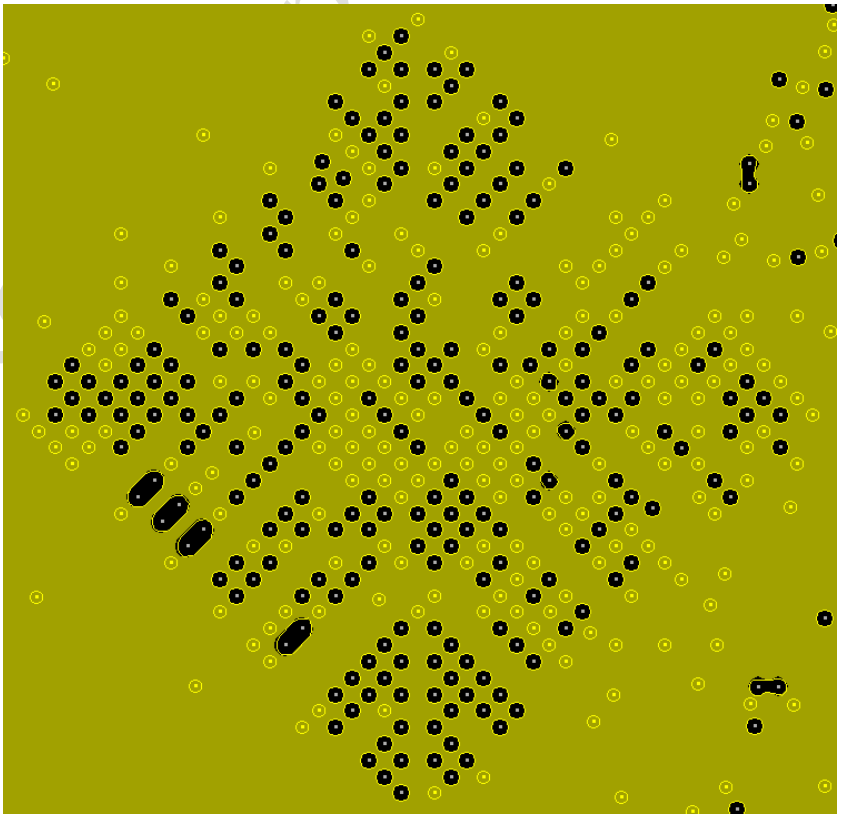

Figure 3-39 Ground copper-covering of RK3568

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#### 3.2.2.11 PCB design of other RK3568 power supplies

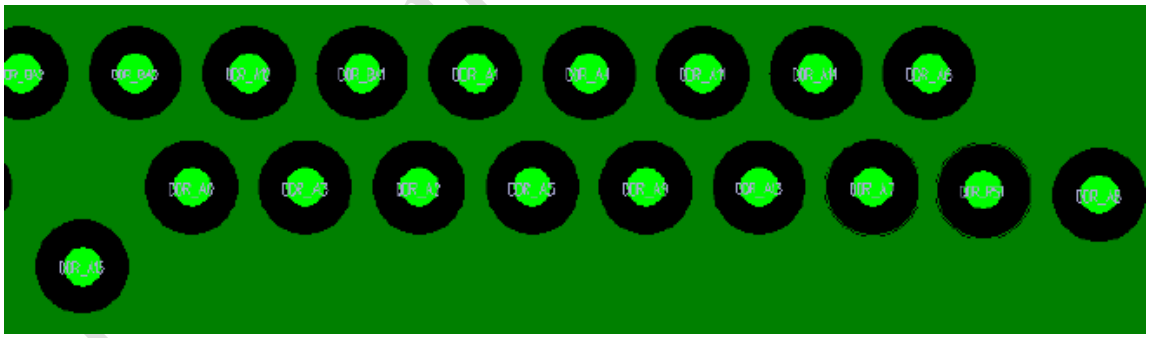
The decoupling capacitors of RK3568 other power supply must be placed on the back of the chip pin. When routing, try to go through the capacitor pad and then to the chip pin.

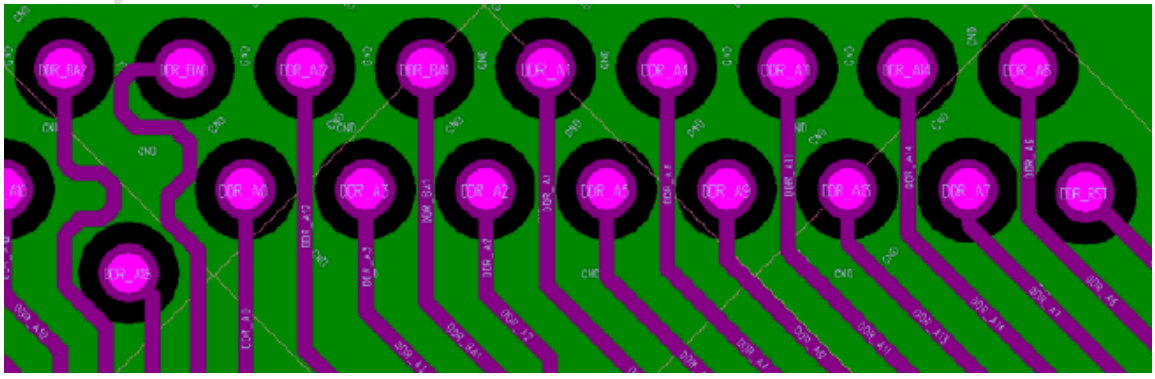
### 3.2.3 DRAM Circuit PCB design

Please apply the DDR reference template provided by Rockchip first.

#### 3.2.3.1 Multilayer structure, impedance control, and other points of attention

- When designing a 6-layer board: It is recommended to take the multilayer structure of TOP-GND-POWER-Signal-GND-Bottom (the structure where the L3 and L4 layers are relatively far apart), and the DDR signal should go on the TOP layer, Signal layer, and Bottom layer as far as possible, so that the return impedance of signals is the smallest. When signal changing layer, a stitching vias must be placed within 30 mils of the signal vias.
- DDR differential impedance is 100Ω ±10%
- DDR single-ended impedance is 50Ω ±10%
- The reference layer of DDR traces should be a complete ground plane to avoid continuous vias blocking the return path of the signal
- DDR signal traces should not go on the edge of the reference plane or the edge of PCB board, otherwise it will have a great impact of impedance. Ensure that the signal traces and the edge of the reference plane are greater than 40mil
- Optimize the position and spacing of layer changing vias, and do not damage the copper-covering of the power layer and the ground layer in a large area. If the copper-covering is divided by vias, it must be routed manually and then connected.





- Avoid that the return path is not connected, as shown in the figures below:

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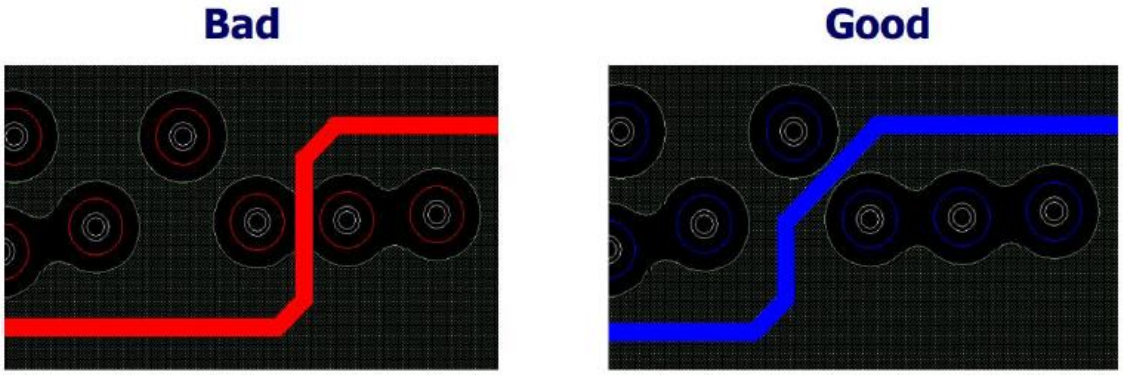


- Keep integrity of VCC_DDR power plane and do not route in the plane.
- Prohibit all DDR signals from crossing different planes
- Under 3200Mbps, the crosstalk between the DQ signals vias will increase, so the crosstalk of the vias must be minimized, please try not to change layers as much as possible. When layer changing is unavoidable, the number of layer changing vias side-by-side to DQ should not exceed two. Moreover, a stitching vias must be placed within 30 mils of the signal vias to provide a continuous return path and reduce crosstalk, and the number of signal layer-changing via must be controlled within two. The reference layer of the signal should be GND layer as much as possible. If it is converted into a power supply, then one stitching capacitor should be added corresponding to every 3 to 4 signal vias.
- VREF traces and other signals are guaranteed to be more than 3 times of line width. It is recommended that VREF be surrounded as much as possible, with the length of 15mil at least and the capacitor should be placed close to the DDR pins.
- The power decoupling capacitors must be placed on the back of the corresponding power pin, it is recommended to refer to the DDR template for placement.
- The decoupling capacitors of DDR VREF pin must be placed close to their respective pins
- Filter capacitor of RESET pin of DDR must be placed close to the pin
- The DDR circuit layout should be as close as possible to inner the board, away from the edge of the board and metal connectors to prevent the DDR module from crashing for abnormalities caused by ESD.

#### 3.2.3.2 DDR3/DDR3L PCB design

- DDR3/DDR3L DQS/DQ/DM Signal routing topology

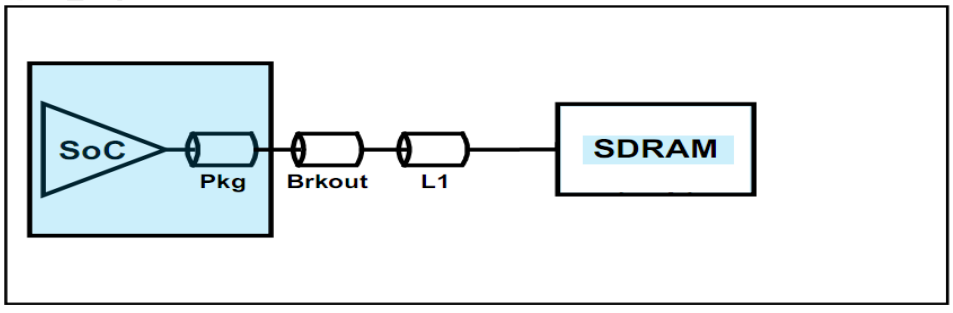


Figure 3-40 DDR3/DDR3L DQS/DQ/DM signal routing topology

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Table 3–1 DDR3/DDR3L DQS/DQ/DM signal impedance and layout requirements

| Parameters | Requirement |
|---|---|
| Single end impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP and DQSN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1500mil |
| Gap requirements between signals in DQ and DM groups | >=2 times the trace width |
| Gap requirements between signals between DQ and DM groups | >=2 times the trace width |
| Gap requirements between DQ/DM and DQS | >=3 times the trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer, in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground wire interval, which can reduce crosstalk and signal impedance |

■ DDR3/DDR3L CLK signal routing topology

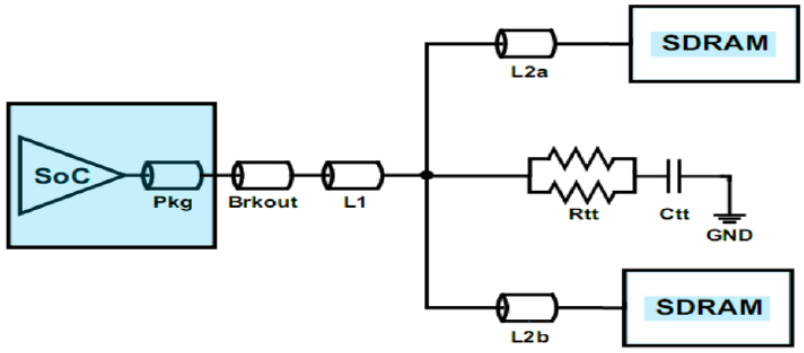


Figure 3-41 DDR3/DDR3L CLK signal routing topology

Clock signal matching method: RC circuit is placed at the branch point to improve the quality of the clock signal

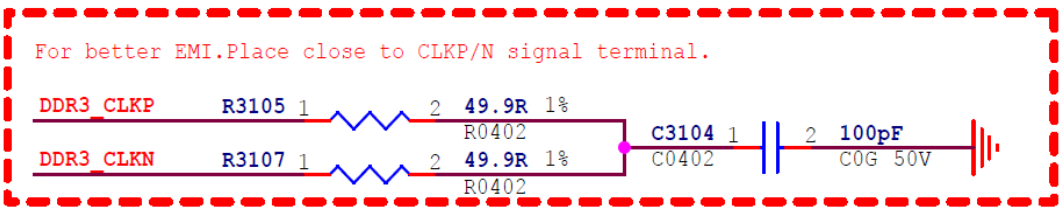


Figure 3-42 DDR3/DDR3L CLK signal RC circuit

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Table 3–2 DDR3/DDR3L CLK signal impedance and layout requirements

| Parameter | Requirements |
|---|---|
| Differential impedance requirements | 100Ω ±10% |
| Equal length requirement between CLK and DQS | Less than 1500mil |
| Equal length requirement between CLKP and CLKN | Less than 12mil |
| Equal length requirement between L2a and L2b | Less than or equal to 20mil |
| Length requirement of L2a, L2b | Less than 600mil, make sure the traces are as short as possible |
| Length control requirements between CLK and CSn/CKE/ODT | Less than 30mil |
| Length control requirements between CLK and other CA/CMD signals except CSn/CKE/ODT | Less than 600mil |
| Gap requirements between CLK and other signals | >=3 times the line width |
| CLK routing requirements | CLK must be surrounded by ground in the whole process, and there must be ground vias within 200mil of ground trace interval |

- DDR3/DDR3L CSn/CKE/ODT signal routing topology

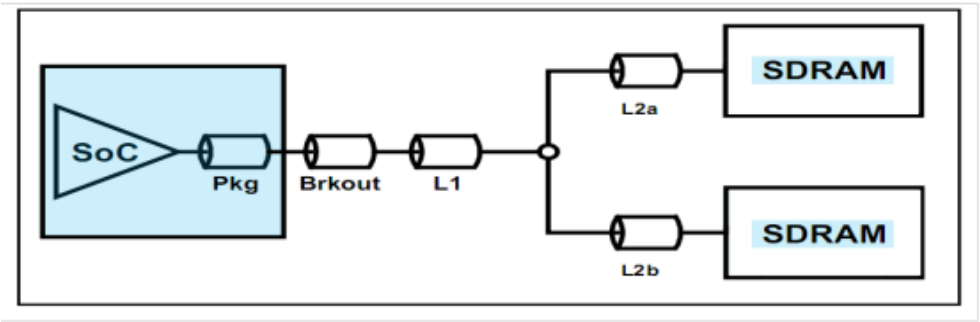


Figure 3-43 DDR3/DDR3L CSn/CKE/ODT signal layout topology

Table 3–3 DDR3/DDR3L CSn/CKE/ODT signal impedance and layout requirements

| Parameter | Requirements |
|---|---|
| Single ended impedance requirements | 50Ω ±10% |
| Equal length requirement between CSn/CKE/ODT and CLK | Less than 30mil |
| Gap requirements between CSn/CKE/ODT and other signals | >=2 times the trace width |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil |
| Length requirements of L2a、L2b trace | Less than 600mil, make sure the traces are as short as possible |
| Routing requirements of 4-layer board | The signal should follow in G-S-S-G way at bottom layer to provide a continuous return path and reduce crosstalk |

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- Other CA/CMD signal of DDR3/DDR3L routing topologies except for CSn/CKE/ODT

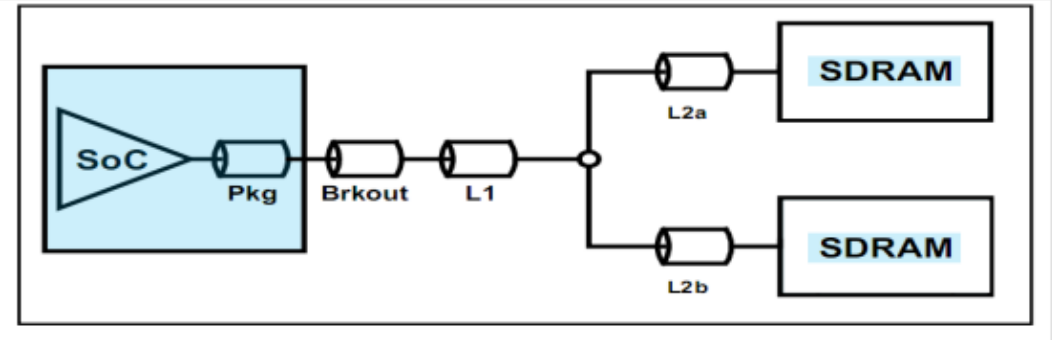


Figure 3-44 Other CA/CMD signal of DDR3/DDR3L layout topology except CSn/CKE/ODT

Table 3–4 Other CA/CMD signal of DDR3/DDR3L layout topology except CSn/CKE/ODT

| parameter | requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirements of other CA/CMD signals and CLK except CSn/CKE/ODT | Less than 600mil |
| Other signal gap requirements | >=2 times the trace width |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil |
| Length requirements of L2a, L2b trace | Less than 600mil, make sure the traces are as short as possible |
| 4-layer board routing requirements | The signal should follow in G-S-S-G way at bottom layer to provide a continuous return path and reduce crosstalk |

#### 3.2.3.3 DDR3/DDR3L+ECC PCB design

- DDR3/DDR3L+ECC DQS/DQ/DM signal routing topology

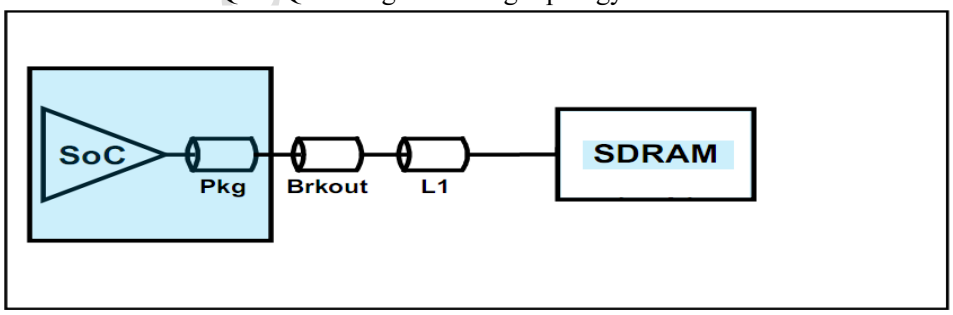


Figure 3-45 DDR3/DDR3L+ECC DQS/DQ/DM signal routing topology

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Table 3–5 DDR3/DDR3L+ECC DQS/DQ/DM signal impedance and layout requirements

| Parameter | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1500mil |
| Gap requirements between signals in DQ and DM groups | >=2 times the trace width |
| Gap requirements between signals between DQ and DM groups | >=2 times the trace width |
| Gap requirements between DQ/DM and DQS | >=3 times the trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer, in G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

- DDR3/DDR3L+ECC CLK signal routing topology

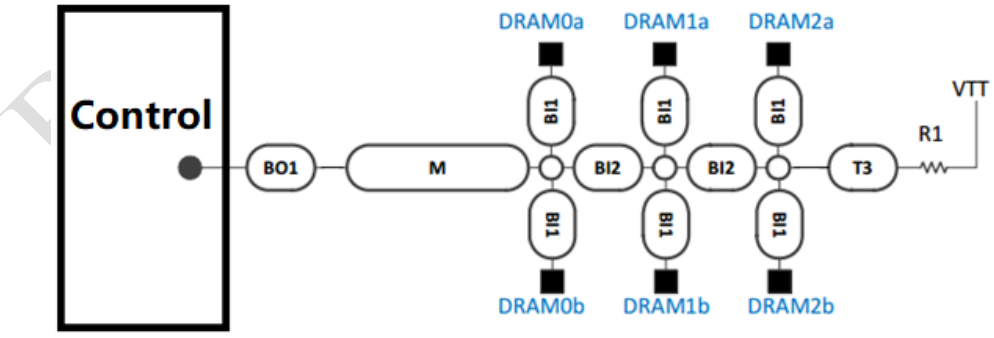


Figure 3-46 DDR3/DDR3L+ECC CLK signal layout topology

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Table 3–6 DDR3/DDR3L+ECC CLK signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential impedance requirements | 100Ω ±10% |
| Equal length requirement between CLK and DQS | Less than 1500mil |
| Equal length requirements between CLKP/CLKN | Less than 12mil |
| Length control requirements between CLK and CSn/CKE/ODT | Less than 60mil |
| Length control requirements between CLK and other CA/CMD signals except CSn/CKE/ODT | Less than 600mil |
| Gap requirements between CLK and other signals | >=3 times the trace width |
| CLK routing requirements | CLK must be surrounded by ground in the whole process, and there must be ground vias within 200mil of ground trace interval |

A 2pF capacitor is connected in parallel between CLKP/N, and it should be as close as possible to RK3568 in layout.

- DDR3/DDR3L+ECC CSn/CKE/ODT signal routing topology

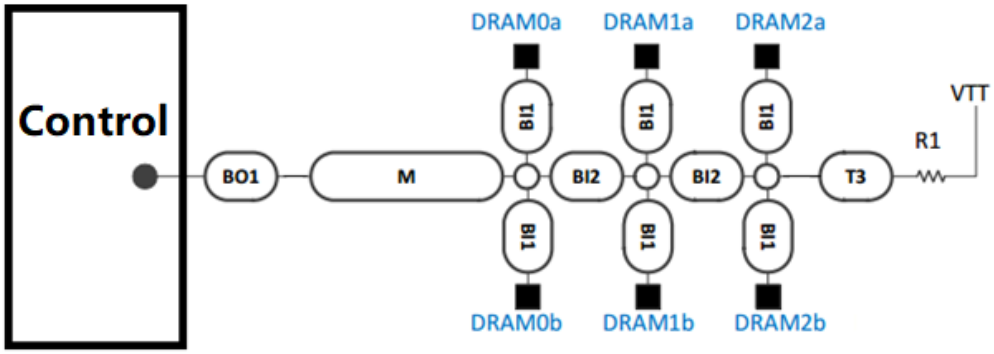


Figure 3-47 DDR3/DDR3L+ECC CSn/CKE/ODT signal routing topology

Table 3–7 DDR3/DDR3L+ECC CSn/CKE/ODT signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| M-section trace impedance requirements | 43Ω ±10% |
| Impedance requirements except for M-segment trace | 50Ω ±10% |
| Equal length requirement between CSn/CKE/ODT and CLK | Less than 60mil |
| Gap requirements between CSn/CKE/ODT and other signals | >=2 times the trace width |

- DDR3/DDR3L+ECC Other CA/CMD signal routing topology except CSn/CKE/ODT

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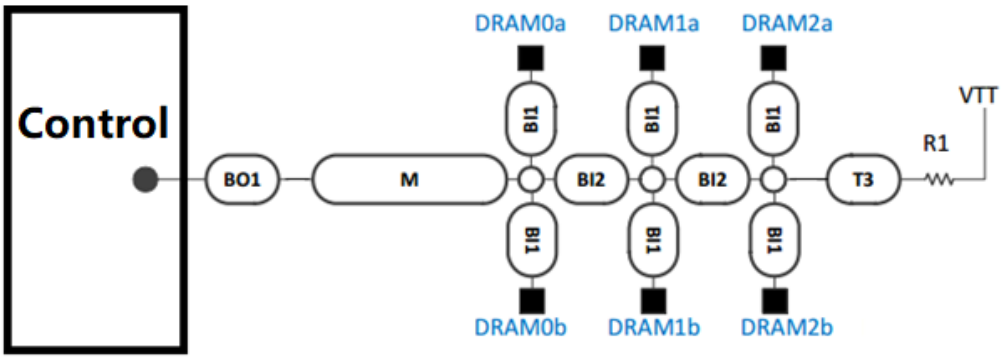


Figure 3-48 DDR3/DDR3L+ECC other CA/CMD signal layout topology except CSn/CKE/ODT

Table 3–8 DDR3/DDR3L+ECC other CA/CMD signal impedance and layout requirements except CSn/CKE/ODT

| Parameters | Requirements |
|---|---|
| M-section trace impedance requirements | 50Ω ±10% |
| Impedance requirements except for M-segment trace | 50Ω ±10% |
| Equal length requirement with CLK | Less than 600mil |
| Gap requirements with other signals | >=2 times the trace width |

#### 3.2.3.4 LPDDR3 PCB Design

Table 3–9 LPDDR3 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |
| Equal length requirements between CLKP/CLKN之 | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1500mil |
| Equal length requirements between CA/CMD and CLK | Less than 30mil |
| Gap requirements between signals in DQ and DM groups | >=2 times the trace width |
| Gap requirements between signals between DQ and DM groups | >=2 times the trace width |
| Gap requirements between DQ/DM and DQS | >=3 times the trace width |
| Gap requirements between CA/CMD and other signals | >=2 times the trace width |
| Gap requirements between CLK and other signals | >=3 times the trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |

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| Parameters | Requirements |
|---|---|
| DQ, DM routing requirements | If the trace is on the surface layer, in G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 times the trace width and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |
| CA.CMD routing requirements of 4-layer board | The signal should follow in the G-S-S-G way at the bottom layer to provide a continuous return path and reduce crosstalk |

#### 3.2.3.5 DDR4 PCB design

- DDR4 DQS/DQ/DM signal routing topology

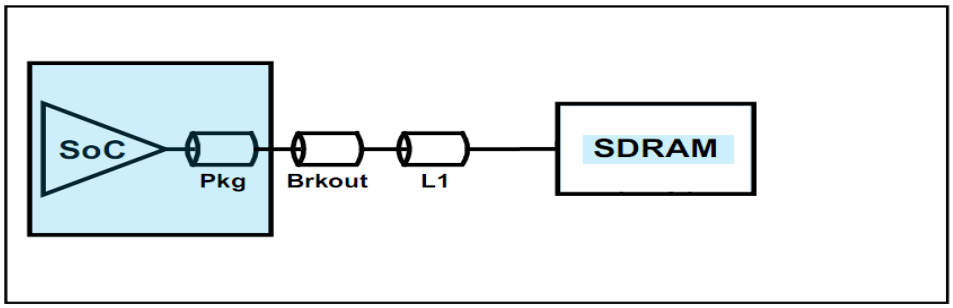


Figure 3-49 DDR4 DQS/DQ/DM signal layout topology

Table 3–10 DDR4 DQS/DQ/DM signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1500mil |
| Gap requirements between signals in DQ and DM groups | >=2 times the trace width |
| Gap requirements between signals between DQ and DM groups | >=2 times the trace width |
| Gap requirements between DQ/DM and DQS | >=3 times the trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer, in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

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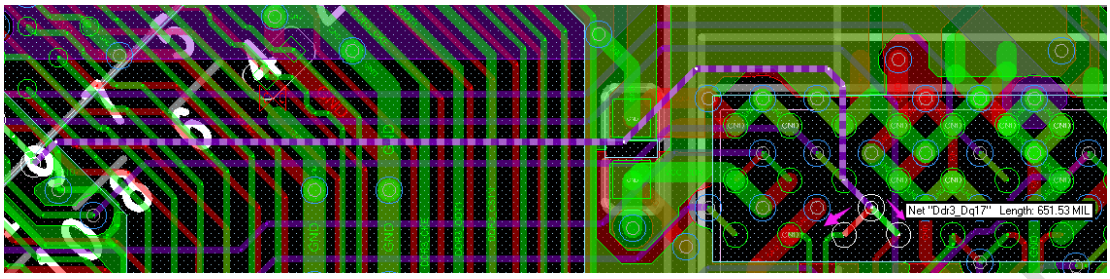
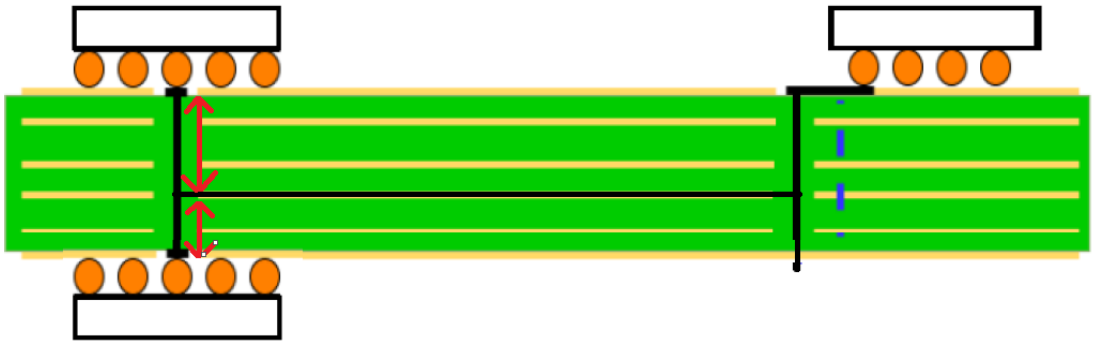
Note:

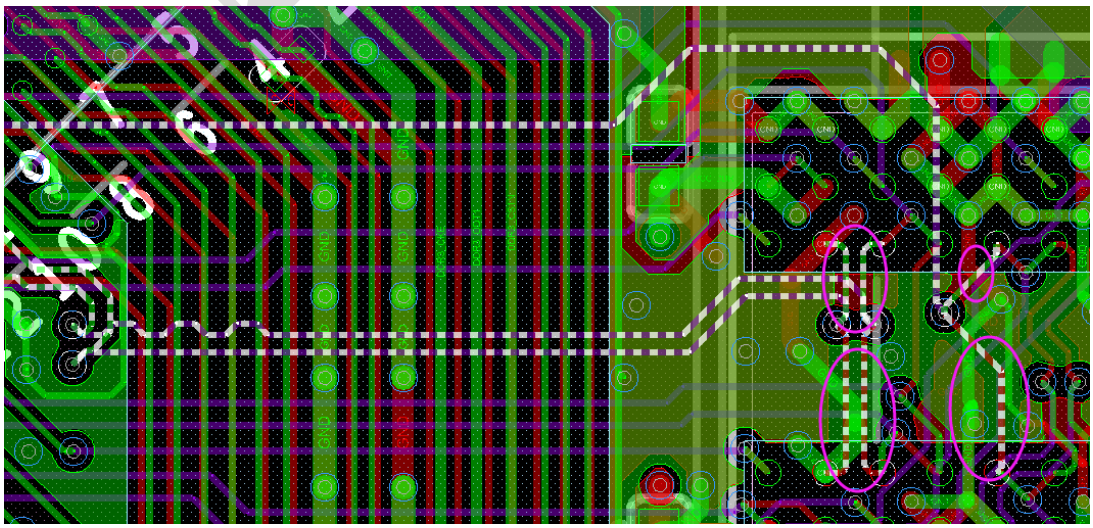
When using 4 pieces of 16bit DDR4, since the DQ/DM/DQS of cs0 and cs1 are shared, in order to get better signal quality, it is recommended to use symmetric placement, adjust the DQ order in the cs1 group to make the branch shortest, as shown in the figure below (see reference schematic for adjusted order)




DM/DQS does not support exchange, branches must be equal in length strictly, and the impact of layer-changing vias paths should be taken in consideration. For example, the controller signal trace is on the L4 layer, and the distance of switching to TOP layer through the via is farther than switching to Bottom layer.



When the branches are equal in length, this impact should be considered. As shown in the figure below, the branch traces of Top layer are short, and the branch traces of Bottom layer are long. This difference needs to be compensated.



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- DDR4 CLK signal routing topology

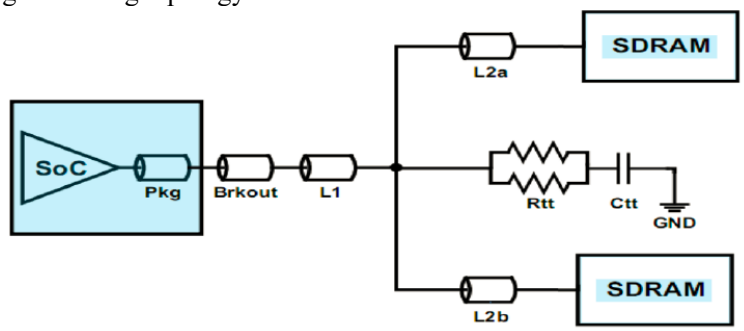


Figure 3-50 DDR4 CLK signal routing topology

Clock signal matching method: Place an RC circuit at the branch point, and it is also necessary to connect a series resistor to the DDR on the branch circuit. The series resistor must be placed at the branch point to improve the quality of the clock signal.


Figure 3-51 RC circuit for DDR4 CLK signal

Table 3–11 DDR4 CLK signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential impedance requirements | 100Ω ±10% |
| Equal length requirement between CLK and DQS | Less than 1500mil |
| Equal length requirements between CLKP/CLKN | Less than 12mil |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil |
| Length requirements of L2a, L2b | Less than 600mil, make sure the traces are as short as possible |
| Length control requirements between CLK and CSn/CKE/ODT | Less than 30mil |
| Length control requirements between CLK and other CA/CMD signals except CSn/CKE/ODT | Less than 600mil |
| Gap requirements between CLK and other signals | >=3 times the trace width |
| CLK routing requirements | CLK must be surrounded by ground in the whole process, and there must be ground vias within 200mil of ground trace interval |

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If it is a 4-layer board, DDR4 needs to rout through the Power layer, then the signal routed on the Power layer must follow in the G-S-S-G mode, as shown in the figure, the blue is the ground trace, and it is recommended to copy the reference PCB directly. Check from beginning to end that is it go with a complete ground trace, it is recommended to directly apply the template provided by RK.

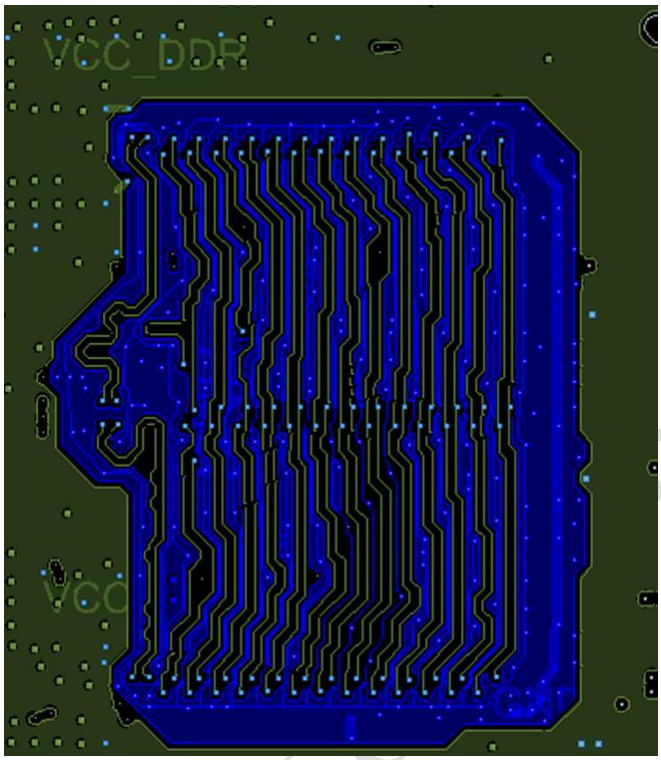


Figure 3-52 CLK/CA/CMD signal routing diagram on the L3 plane of DDR4 4-layer board

- DDR4 CSn/CKE/ODT signal routing topology

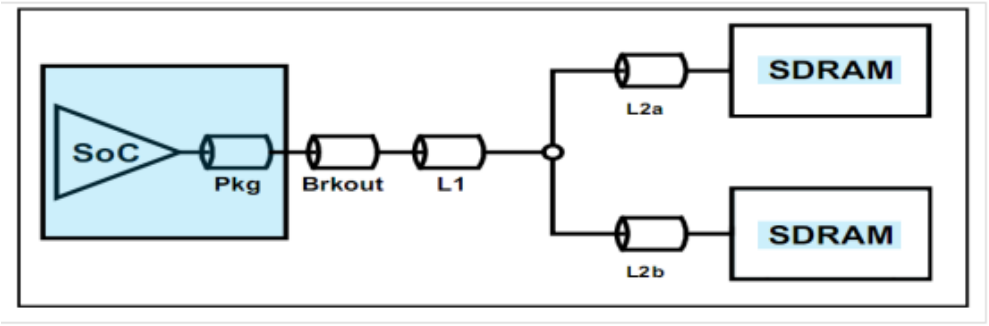


Figure 3-53 DDR4 CSn/CKE/ODT signal routing topology

Table 3–12 DDR4 CSn/CKE/ODT signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirement between CSn/CKE/ODT and CLK | Less than 30mil |
| Gap requirements between CSn/CKE/ODT and other signals | >=2 times the trace width |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil |

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| Parameters | Requirements |
|---|---|
| Length requirements of L2a, L2b | Less than 600mil, make sure the trace is as short as possible |
| Routing requirements for 4-layer board | The signal needs to take G-S-S-G way at the bottom layer to provide a continuous return path and reduce crosstalk |

- Other CA / CMD signal routing topologies except CSN / CKE / ODT when using DDR4

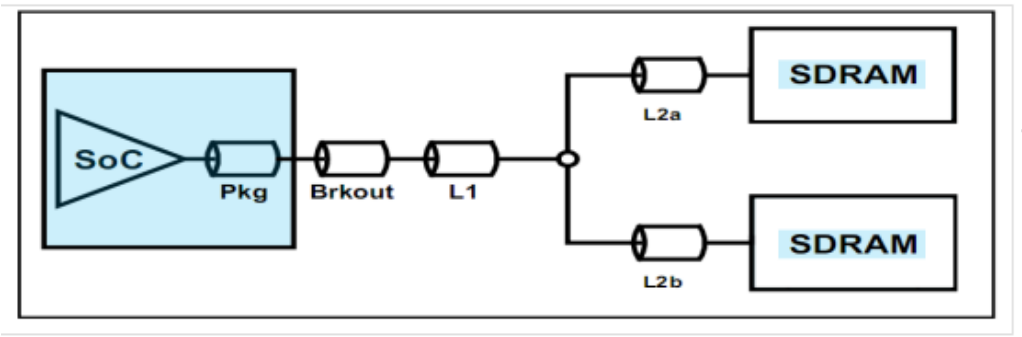


Figure 3-54 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4

Table 3–13 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| The equal length requirements between CLK and other CA/CMD signals except CSn/CKE/ODT | Less than 600mil |
| Other signal gap requirements | >=2 times the trace width |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil |
| Length requirements of L2a, L2b | Less than 600mil, make sure the trace is as short as possible |
| Routing requirements for 4-layer board | The signal is in G-S-S-G way at the bottom layer to provide a continuous return path and reduce crosstalk |

#### 3.2.3.6 DDR4+ECC PCB design

- DDR4+ECC DQS/DQ/DM signal routing topology

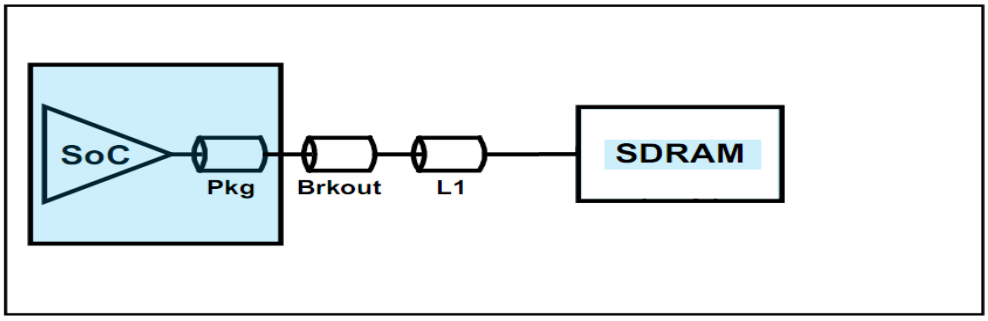


Figure 3-55 DDR4+ECC DQS/DQ/DM signal layout topology

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Table 3–14 DDR4+ECC DQS/DQ/DM signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1500mil |
| Gap requirements between signals in DQ and DM groups | >=2 times the trace width |
| Gap requirements between signals between DQ and DM groups | >=2 times the trace width |
| Gap requirements between DQ/DM and DQS | >=3 times the trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer, in G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 times the line width, and the gap between G-S is 1 time line width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

- DDR4+ECC CLK signal routing topology

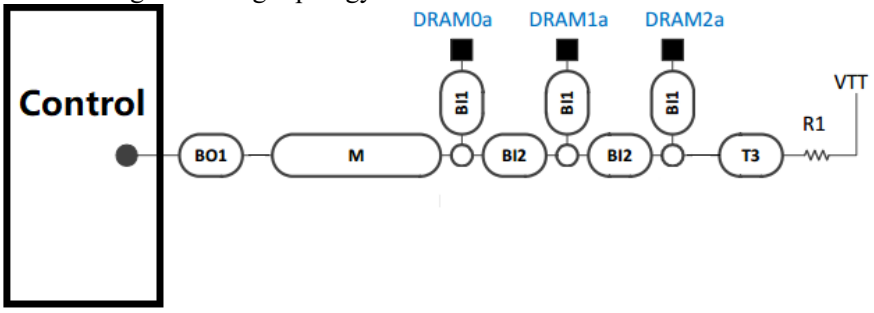


Figure 3-56 DDR4+ECC CLK signal layout topology

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Table 3–15 DDR4+ECC CLK signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential impedance requirements | 100Ω ±10% |
| Equal length requirement between CLK and DQS | Less than 1500mil |
| Equal length requirements between CLKP/CLKN | Less than 12mil |
| Length control requirements between CLK and CSn/CKE/ODT | Less than 60mil |
| Length control requirements between CLK and other CA/CMD signals except CSn/CKE/ODT | Less than 600mil |
| Gap requirements between CLK and other signals | >=3 times the trace width |
| CLK routing requirements | CLK must be surrounded by ground in the whole process, and there must be ground vias within 200mil of ground trace interval |

A 2pF capacitor is connected in parallel between CLKP/N, and its layout should be as close as possible to RK3568.

- DDR4+ECC CSn/CKE/ODT signal routing topology

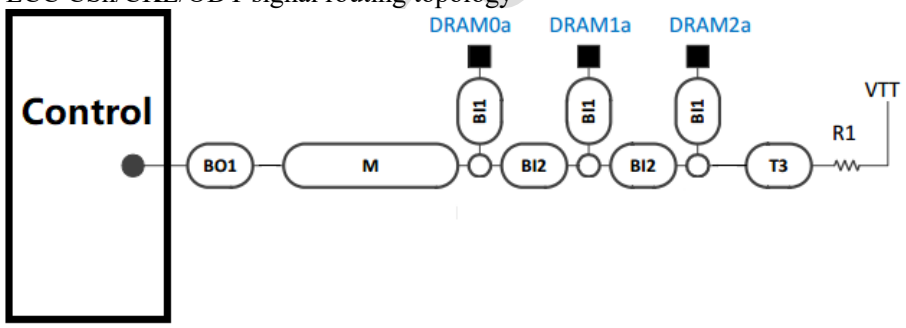


Figure 3-57 DDR4+ECC CSn/CKE/ODT signal routing topology

Table 3–16 DDR4+ECC CSn/CKE/ODT signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| M-section trace impedance requirements | 43Ω ±10% |
| Impedance requirements except for M-segment trace | 50Ω ±10% |
| Equal length requirement between CSn/CKE/ODT and CLK | Less than 60mil |
| Gap requirements between CSn/CKE/ODT and other signals | >=2 times the trace width |

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- DDR4+ECC other CA/CMD signal routing topology except CSn/CKE/ODT

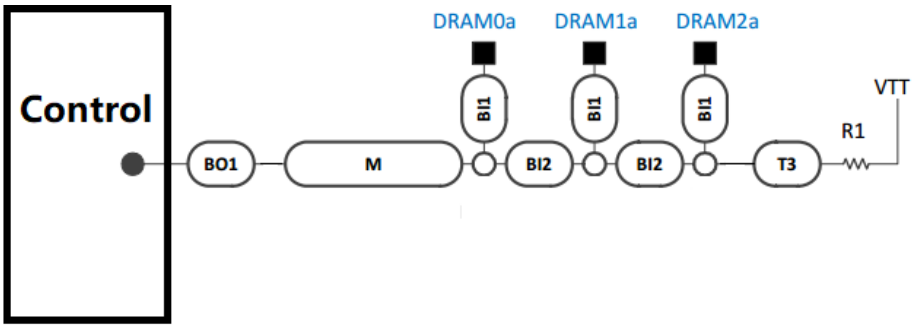


Figure 3-58 DDR4+ECC other CA/CMD signal layout topology except CSn/CKE/ODT

Table 3–17 DDR4+ECC other CA/CMD signal impedance and layout requirements except CSn/CKE/ODT

| Parameters | Requirements |
|---|---|
| M-section trace impedance requirements | 50Ω ±10% |
| Impedance requirements except for M-segment trace | 50Ω ±10% |
| Equal length requirement with CLK | Less than 600mil |
| Gap requirements with other signals | >=2 times the trace width |

### 3.2.3.7 LPDDR4 PCB design

Table 3–18 LPDDR4 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |
| Equal length requirements between CLKP/CLKN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1200mil |
| Equal length requirements between CA/CMD and CLK | Less than 500mil |

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| Parameters | Requirements |
|---|---|
| Gap requirements between signals in DQ and DM groups | >=2 timesthe trace width |
| Gap requirements between signals between DQ and DM groups | >=2 timesthe trace width |
| Gap requirements between DQ/DM and DQS | >=3 timesthe trace width |
| Gap requirements between CA/CMD and other signals | >=2 timesthe trace width |
| Gap requirements between CLK and other signals | >=3 timesthe trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer in the GSSG way (G: ground trace, S: signal trace), the gap between S-S must be >=2 timesthe trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |
| CA.CMD routing requirements for 4-layer boards | The signal should follow in the G-S-S-G way at the bottom layer to provide a continuous return path and reduce crosstalk |

#### 3.2.3.8 LPDDR4x PCB design

Table 3–19 LPDDR4 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Differential impedance requirements | 100Ω ±10% |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN | Less than 12mil |

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| Parameters | Requirements |
|---|---|
| Equal length requirements between CLKP/CLKN | Less than 12mil |
| Equal length requirements between DQS and CLK | Less than 1200mil |
| Equal length requirements between CA/CMD and CLK | Less than 500mil |
| Gap requirements between signals in DQ and DM groups | >=2 timesthe trace width |
| Gap requirements between signals between DQ and DM groups | >=2 timesthe trace width |
| Gap requirements between DQ/DM and DQS | >=3 timesthe trace width |
| Gap requirements between CA/CMD and other signals | >=2 timesthe trace width |
| Gap requirements between CLK and other signals | >=3 timesthe trace width |
| DQS routing requirements | If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace |
| DQ, DM routing requirements | If the trace is on the surface layer, follow in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be >=2 timesthe trace width, and the gap between G-S is 1 timethe trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

## 3.2.4 Flash Circuit PCB design

### 3.2.4.1 eMMC PCB design

Table 3–20 eMMC signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirements between DATA/CMD and CLK/DS | Less than 120mil |
| Total length requirement of PCB trace | Less than 4000mil |
| Gap requirements between eMMC signals | >=2 times the trace width |
| Gap requirements between eMMC | >=3 times the trace width |

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| Parameters | Requirements |
|---|---|
| signal and other signals | |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer changing vias |
| Routing requirements of eMMC CLK/DS | They must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

Other points for attention:

- In the overall layout, place eMMC as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all eMMC signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The 22ohm series matching resistor of eMMC_CLKOUT should be close to CPU (source end), and the trace between CPU pin and the resistor must be controlled within 300mil.
- The 0ohm series matching resistor of eMMC_DATA_STROBE should be close to eMMC, and the trace between the eMMC pin and the resistor must be controlled within 300mil.
- The width of the eMMC power trace should meet the current requirements of VCCIO2 power domain and the corresponding eMMC. It is recommended that the VCCIO2 power domain trace should be more than 12mil, and the power trace of the eMMC should be more than 25mil.
- The decoupling capacitors of eMMC and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- The external capacitor of the VDDi pin of eMMC must be placed close to the corresponding pin, and the trace should be as short and thick as possible
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the eMMC D0 signal, and do not generate additional branches

#### 3.2.4.2 FSPI PCB design

Table 3–21 FSPI signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirement between DATA and CLK | Less than 200mil |
| Total length requirement of PCB trace | Less than 4000mil |
| Gap requirements between FSPI signals | >=2 times the trace width |
| The gap between the FSPI signal and other signals | >=3 times the trace width |
| Layer change via | If it is less than 4, symmetrical stitching vias should be placed close to the layer change via |

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| Parameters | Requirements |
|---|---|
| FSPI CLK routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

Other points for attention:

- In the overall layout, try to place FSPI as close to RK3568 to shorten the trace as much as possible.
- The reference layer of all FSPI signals should be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The 22ohm series matching resistor of FSPI_CLK is close to the CPU (source end), and the trace between CPU pin and the resistor must be controlled within 300mil.
- The width of the FSPI Flash power trace should meet the current requirements of VCCIO2 power domain and the corresponding FSPI. It is recommended that the width of VCCIO2 power domain traces be more than 12mil, and the FSPI power traces should be more than 25mil.
- The decoupling capacitors of FSPI Flash and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the FSPI CLK signal, and do not generate additional branches

#### 3.2.4.3 Nand Flash PCB design

Table 3–22 Nand Flash signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirements between the whole group of signals | Less than 200mil |
| Total length requirement of PCB trace | Less than 4000mil |
| Gap requirements between Nand Flash signals | >=2 times the trace width |
| Gap requirements Nand Flash signal and other signals | >=3 times the trace width |
| Layer change via | If it is less than 4, symmetrical stitching vias should be placed close to the signal layer change via |
| Nand Flash DQS routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

Other points for attention:

- In the overall layout, place Nand Flash as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all Nand Flash signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.

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- The 0ohm series matching resistor of Nand Flash_DQS is close to the end of the Nand Flash, and the trace between the Nand pin and the resistor must be controlled within 300mil.
- The width of the Nand Flash power line should meet the current requirements of the VCCIO2 power domain and the corresponding Nand Flash. It is recommended that the width of VCCIO2 power domain traces be more than 12mil, and Nand Flash power traces should be more than 25mil.
- The decoupling capacitors of Nand Flash and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the Nand D0 signal, and do not generate additional branches

#### 3.2.4.4 Note of eMMC and Nand Flash compatible design PCB

- When dual layout is required for eMMC and Nand Flash compatible design, you need to pay attention to avoid long branches routing, causing abnormal functions. R4003, R4000, R4001 and R4100, R4101, R4102 must be placed on each signal branch point (please refer to RK3568_AIoT_REF_SCH for the tag number)


Figure 3-59 Branch resistances of eMMC and Nand Flash compatible design

As shown in the figure below, R4000 and R4100 are placed on the branch point. When using eMMC, only R4000 is connected instead of R4100 to minimized the influence as much as possible

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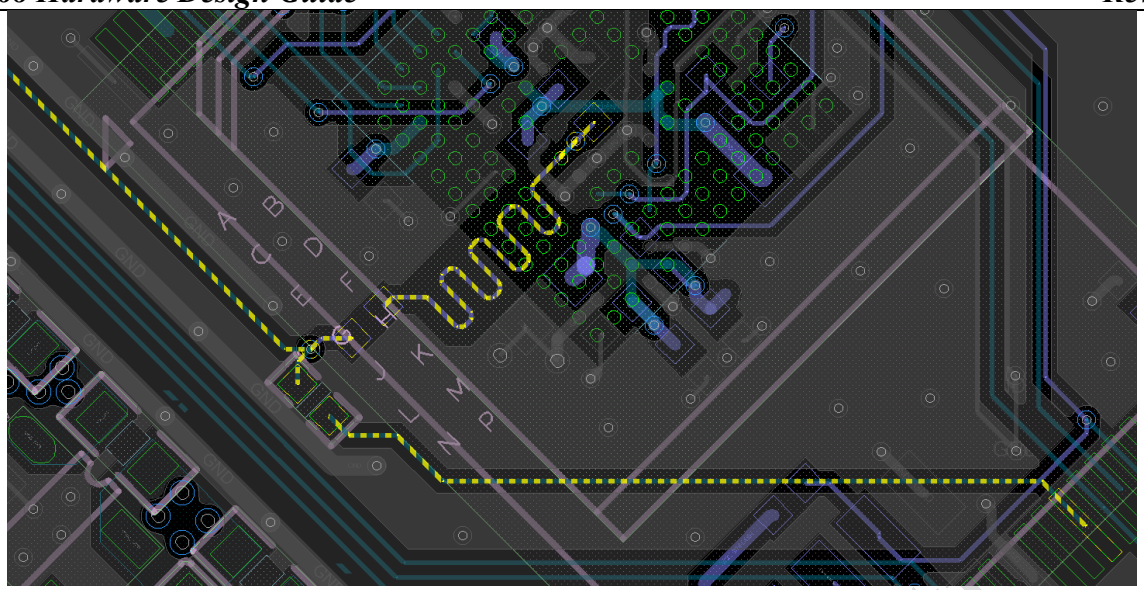

Figure 3-60 Branch resistor layout and routing of eMMC and NAND flash compatible design

- When dual layout is required for compatible design of eMMC and Nand Flash, D0-D7 signals are recommended to use Daisy-chain. The routing must pass through the Nand pins and then connect to the eMMC pins. The eMMC pins should be as close as possible to the Nand pins. If compatible design is not necessary, it is recommended to keep only eMMC instead of Nand Flash to improve the stability of eMMC.

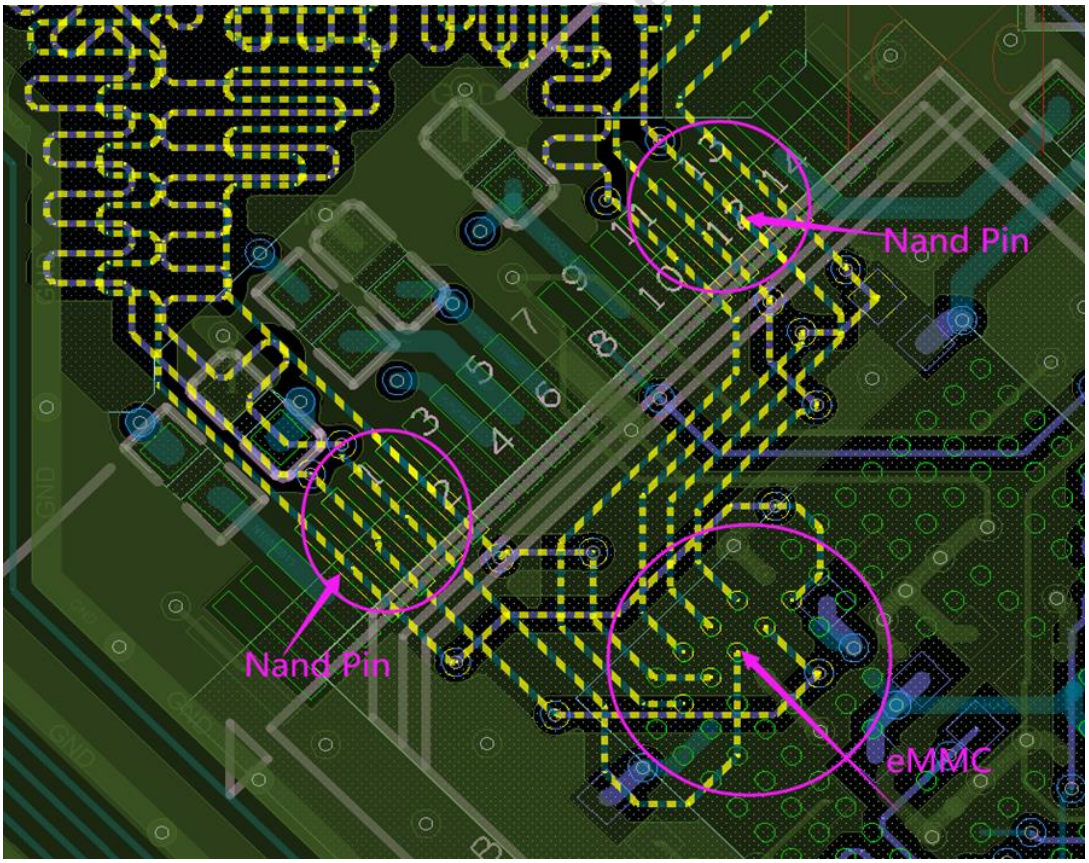


Figure 3-61Figure 3–1 DATA routing of eMMC and Nand Flash compatible design

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### 3.2.5 SDMMC0/1/2 Interface Crcuit PCB Design

Table 3–23 SDMMC0/1/2 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended impedance requirements | 50Ω ±10% |
| Equal length requirements between DATA/CMD and CLK | Less than 120mil |
| Total length requirement of PCB trace | When CLK is less than or equal to 50MHz, less than 6000mil;When CLK is greater than 50MHz, less than 4000mil |
| Gap requirements between SDMMCx signals | >=2 times the trace width |
| Gap requirements between SDMMCx signal and other signals | >=3 times the trace width |
| Layer change vias | If it is less than 4, symmetrical stitching vias should be placed close to the signal layer change via |
| SDMMCx CLK routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

Other points for attention:

- In the overall layout, place SDMMC as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all SDMMCx signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The SDMMCx_CLK series matching resistor is close to CPU, and the trace between CPU pin and the resistor must be controlled within 400mil.
- The VCCIOx power domain where SDMMCx is located is 12mil or more, and the decoupling capacitor must be placed on the back of the corresponding power pin.
- When a card is used, the power capacitor of the card socket must be placed at the power pin of the card socket, and the trace must pass through the capacitor first and then go to the card socket pin. The power trace of the card socket must be 40mil or more; the TVS protection diode of the Micro-SD should be placed as close as possible to the card socket. The signal topology is: Micro-SD card socket --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device first; There should not be stubs on the TVS device trace; the ground pins of TVS are recommended to add ground vias as much as possible, and at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capacity; try to avoid routing in the area under the Micro-SD card socket to avoid coupling when ESD phenomenon occurs.

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### 3.2.6 SARADC/OTP Interface Circuit PCB Design

- The 1nF capacitors of SARADC_VIN0/1/2/3/4/5/6/7 are jitter elimination capacitors, which should be placed as close to the pins of chipset as possible during layout.
- The decoupling capacitor of SARADC_AVDD_1V8 must be placed on the back of the corresponding power pin.
- Keep SARADC_VIN0/1/2/3/4/5/6/7 signals away from digital signals such as LCD and DRAM. Do not rout on the neighboring layers of high-speed signal; do not placing layer change vias near high-speed signals; do not rout through the inductive area.
- If there are buttons, the TVS tube must be placed close to the button. The signal topology is: button --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be stubs on the TVS device trace
- It is recommended to increase ground vias as much as possible for the ground pins of TVS, at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

### 3.2.7 USB2.0 Interface Circuit PCB Design

Table 3–24 USB2.0 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 90Ω ±10% |
| Equal length requirements between DP/DM | Less than 20mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer change via |

- In the overall layout, place the USB connector as close to RK3568 as possible to shorten the trace as much as possible.
- The USB3_AVDD_0V9/1V8/3V3 power supply and USB2_AVDD_0V9/1V8/3V3 decoupling capacitors must be placed on the back of the corresponding power supply pins.
- When the USB differential signal traces need to change layers, ensure that the number of vias on the traces is less than 4(6 at most), and place symmetrical stitching vias close to the signal layer change vias, and ensure that the center distance between the stitching vias and the signal vias should not exceed 30mil
- As far as possible, the reference layer of the USB differential pair should be a complete ground plane. If it is impossible to avoid routing across different planes, it must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval.

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### 3.2.8 USB3.0 Interface Circuit PCB Design

Table 3–25 USB3.0 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 90Ω ±10% |
| Equal length requirements between SSTXP/SSTXN | Less than 12mil |
| Equal length requirements between SSRXP/SSRXN | Less than 12mil |
| Equal length requirements between SSTXP/N and SSRXP/N | Less than 6000mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between SSTX and SSRX signals | >=4 times the trace width |
| SSTX, SSRX signal and other signal gap requirements | >=4 times the trace width |
| Layer change vias | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, place the USB connector as close to RK3568 as possible to shorten the trace as much as possible。
- The decoupling capacitor of MULTI_PHY_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout SSTXP/N and SSRXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of SSTXP/N and SSRXP/N signals should be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the USB connector
- An empty space must be reserved below the USB3 connector pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty space should not be less than the size of the package pad.

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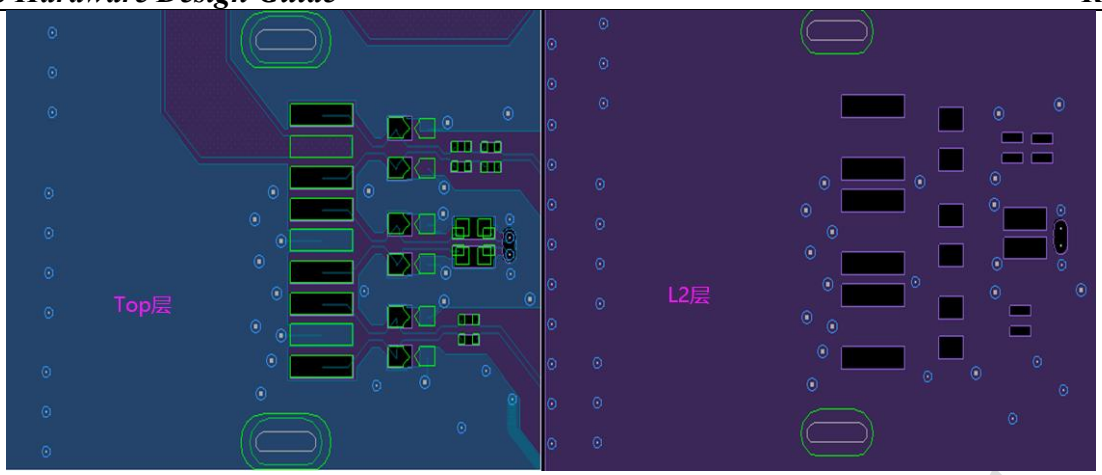


Figure 3-62 Schematic diagram of empty space below the pad of USB3 connector and the pad of AC coupling capacitor

- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure below.


Figure 3-63 PCB fiberweave effect to improve routing way

### 3.2.9 SATA3.0 Interface Circuit PCB Design

Table 3–26 SATA3.0 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements between TXP/TXN | Less than 12mil |
| Equal length requirements between RXP/RXN | Less than 12mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between TX and RX signals | >=4 times the trace width |
| Gap requirements between TX, RX signals and other signals | >=4 times the trace width |
| Layer change vias | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change via |

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- In the overall layout, the SATA connector should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The decoupling capacitor of MULTI_PHY_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N and RXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N and RXP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the SATA connector
- An empty space must be reserved below the SATA connector pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

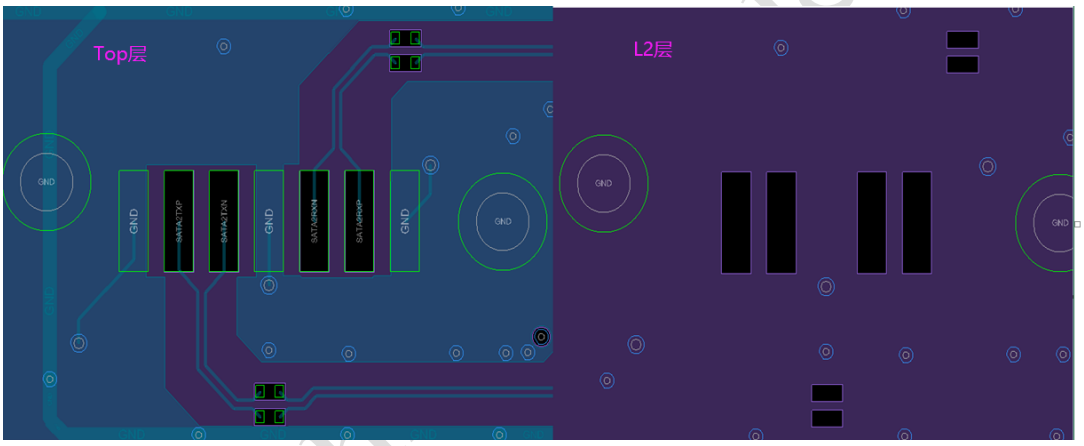


Figure 3-64 Schematic diagram of empty space below the pad of SATA connector and the pad of AC coupling capacitor

- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure3–63.

### 3.2.10 QSGMII/SGMII Interface Circuit PCB Design

Table 3–27 QSGMII/SGMII signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements between TXP/TXN | Less than 12mil |
| Equal length requirements between RXP/RXN | Less than 12mil |

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| Parameters | Requirements |
|---|---|
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between TX and RX signals | >=4 times the trace width |
| Gap requirements between TX, RX signals and other signals | >=4 times the trace width |
| Layer change vias | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, the QSGMII/SGMII PHY connectors should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of MULTI_PHY_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N and RXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N and RXP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the PHY chip.
- An empty layer must be reserved below the QSGMII/SGMII PHY signal pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.
- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure3–63.

### 3.2.11 PCIe2.0 Interface Circuit PCB Design

Table 3–28 PCIe2.0 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Date differential trace impedance requirements | 85Ω ±10% |
| Clock differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements between TXP/TXN | Less than 12mil |
| Equal length requirements between RXP/RXN | Less than 12mil |
| Equal length requirements between REFCLKP/CLKN | Less than 12mil |

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| Parameters | Requirements |
|---|---|
| Total length requirement of PCB trace | Less than 6000mil |
| Equal length requirements between TX and RX traces | Less than 6000mil |
| Gap requirements between TX and RX signals | >=4 times the trace width |
| Gap requirements between TX and RX signals | >=4 times the trace width |
| REFCLKP/N differential routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |
| Layer change via | If it is less than 2, symmetrical stitching vias should be placed close to the signal layer change via |

- In the overall layout, the PCIe Slot should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of MULTI_PHY_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N，RXP/N，REFCLKP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N，RXP/N，REFCLKP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the PCIe Slot.
- An empty space must be reserved below the Slot pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

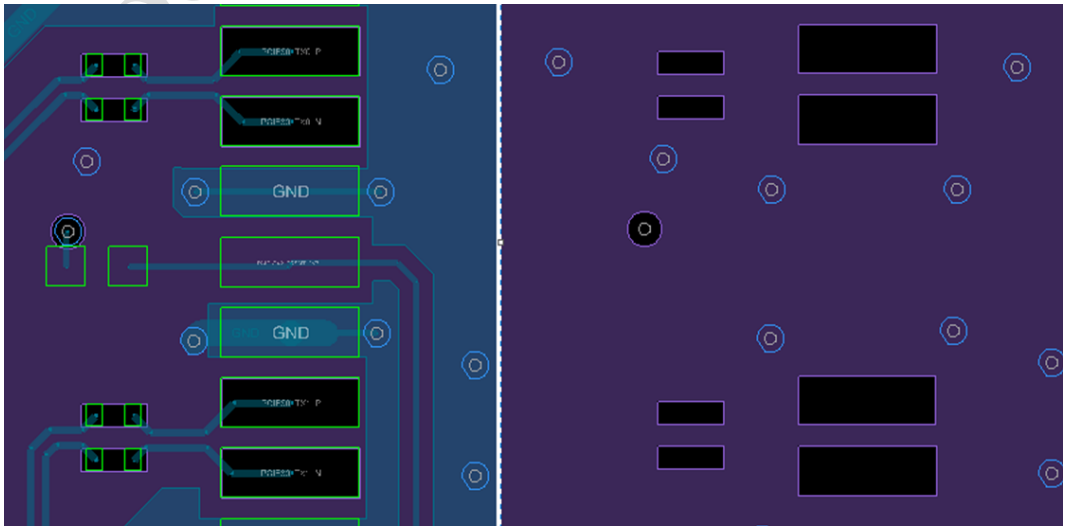


Figure 3-65 Schematic diagram of empty space below the pad of PCIe Slot and the pad of AC coupling capacitor

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- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure 3–63.

### 3.2.12 PCIe3.0 Interface Crcuit PCB Design

Table 3–29 PCIe3.0 signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Date differential trace impedance requirements | 85Ω ±10% |
| Clock differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements between TXP/TXN | Less than 12mil |
| Equal length requirements between RXP/RXN | Less than 12mil |
| Equal length requirements between REFCLKP/CLKN | Less than 12mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Equal length requirements between TX and RX traces | Less than 6000mil |
| Gap requirements between TX and RX signals | >=5 times trace width |
| Gap requirements between TX and RX signals | >=5 times trace width |
| REFCLKP/N differential routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |
| Layer change vias | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change via |

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- In the overall layout, the PCIe Slot should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of PCIE30_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N，RXP/N，REFCLKP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N，RXP/N，REFCLKP/N signals needs to be a complete ground plane to

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avoid continuous vias blocking the return path of the signal.

- Please place AC coupling capacitors symmetrically and close to the PCIe Slot.
- An empty layer must reserve below the Slot pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad as shown in the figure 3–56
- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure 3–63.

### 3.2.13 MIPI CSI RX Interface Circuit PCB Design

Table 3–30 MIPI CSI RX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements within a differential pair | Less than 12mil |
| Equal length requirements between differential pairs | Less than 36mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between MIPI signals | >=3 times the trace width |
| Gap requirements between MIPI signals and other signals | >=3 times the trace width |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, the MIPI CSI device should be placed as close as possible to RK3568, and the trace should be shortened as much as possible.
- The decoupling capacitor of MIPI_CSI_RX_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimize the layer-changing vias. When layer-changing is needed, no more than 4 vias, and place symmetrical stitching vias close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30 mils.
- The reference layer of the MIPI CSI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

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### 3.2.14 CIF Interface Circuit PCB Design

Table 3–31 CIF signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended trace impedance requirements | 50Ω ±10% |
| Equal length requirements between all CIF signals and CIF CLKIN | Less than 180mil |
| Total length requirement of PCB trace | Less than 5000mil |
| Gap requirements between CIF signals | >=2 times the trace width |
| Gap requirements between CIF signal and other signals | >=3 times the trace width |
| CIF CLKIN Routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

- In the overall layout, the CIF device should be placed as close as possible to RK3568, and the trace should be shortened as much as possible.
- The reference layer of all CIF signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The 22ohm series matching resistor of CIF CLKIN is close to the device, and the trace between the pin and resistor of the device end must be controlled within 400mil
- The decoupling capacitor of VCCIO6 must be placed on the back of the corresponding power pin.

### 3.2.15 MIPI DSI TX Interface Circuit PCB Design

Table 3–32 MIPI DSI TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements within the differential pair | Less than 12mil |
| Equal length requirements between differential pairs | Less than 36mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between MIPI signals | >=3 times the trace width |
| Gap requirements between MIPI signals and other signals | >=3 times the trace width |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, the MIPI DSI device should be placed as close to RK3568 as possible, and the trace

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should be shortened as much as possible.

- The decoupling capacitor of MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- The decoupling capacitor of MIPI_DSI_TX1_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of the MIPI differential pair. When layer-changing is needed, no more than 4 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the MIPI DSI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

### 3.2.16 LVDS TX Interface Circuit PCB Design

Table 3–33 LVDS TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements within the differential pair | Less than 20mil |
| Equal length requirements between differential pairs | Less than 60mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between LVDS signals | >=3 times the trace width |
| Gap requirements between LVDS signal and other signal | >=3 times the trace width |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, place the LVDS device as close as possible to RK3568 to shorten the trace as much as possible.
- The decoupling capacitor of MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of LVDS differential pair. When layer-changing is needed, no more than 4 vias and 6 at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the LVDS differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal.

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### 3.2.17 eDP TX Interface Circuit PCB Design

Table 3–34 eDP TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements within the differential pair | Less than 12mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between eDP signals | >=4 times the trace width |
| Gap requirements between eDP signal and other signals | >=4 times the trace width |
| Layer change vias | If they are less than 4, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, place the eDP device as close as possible to RK3568 to shorten the trace as much as possible.
- The decoupling capacitor of eDP_TX_AVDD_0V9/1.8V power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of LVDS differential pair. When layer-changing is needed, no more than 4 vias and 6 at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the eDP_TX differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

### 3.2.18 HDMI TX Interface Circuit PCB Design

Table 3–35 HDMI TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Differential trace impedance requirements | 100Ω ±10% |
| Equal length requirements within the differential pair | Less than 12mil |
| Equal length requirements between clock and data | Less than 480mil |
| Total length requirement of PCB trace | Less than 6000mil |
| Gap requirements between HDMI data signals | >=4 times the trace width |
| Gap requirements between HDMI data and HDMI clock | >=5 times the trace width |
| Layer change vias | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change vias |

- In the overall layout, the HDMI socket should be placed as close as possible to RK3568, and the trace

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should be shortened as much as possible.

- HDMI_TX_AVDD_0V9/1V8 power decoupling capacitors must be placed on the back of the corresponding power pins.
- The trace should be on the top layer as much as possible. When layer changing is needed, drill 2 vias at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30 mils. Try to use arcs or obtuse angles, instead of right angles or acute angles.
- The whole group of differential traces are routed in parallel and surrounded by ground and the gap between the ground trace and the signal is greater than or equal to 4 times the line width, and there must be ground vias within 300 mils of the ground trace interval.
- The reference layer of all signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- An empty layer should be reserved below the pad of the HDMI socket and the pad of the TVS tube to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

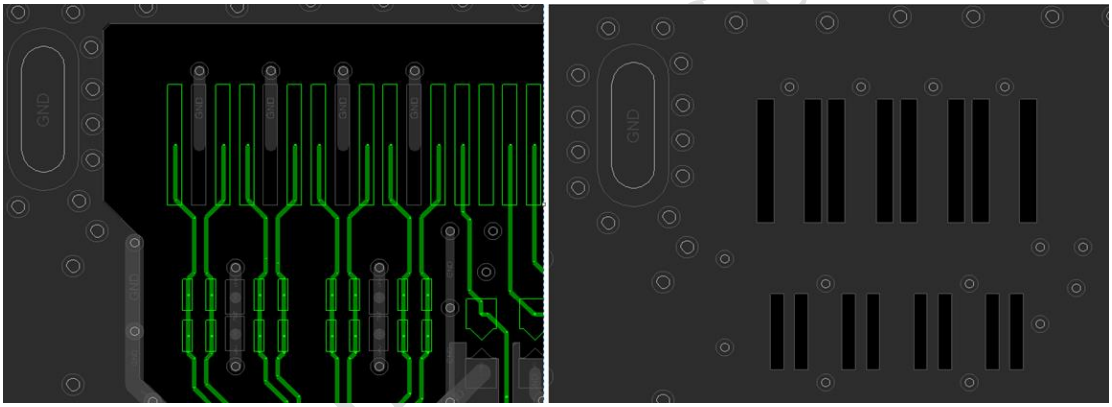

Figure 3-66 Schematic diagram of empty space below the pad of HDMI connector and the pad of TVS diode

- The HDMI TVS tube should be placed as close as possible to the connector. The signal topology is: HDMI connector --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be Stub on the TVS device trace. It is recommended to increase the ground vias as much as possible for the ground pins of TVS, at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

### 3.2.19 RGB TX Interface Circuit PCB Design

Table 3–36 RGB TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended trace impedance requirements | 50Ω ±10% |
| Equal length requirements between all LCDC signals and LCDC CLK | Less than 180mil |
| Total length requirement of PCB trace | Less than 5000mil |

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| | |
|---|---|
| Gap requirements between LCDC signals | >=2 times the trace width |
| Gap requirements between LCDC signal and other signals | >=3 times the trace width |
| LCDC CLK routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

- In the overall layout, the LCDC device should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The 22ohm series matching resistor of LCDC clk is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil
- The reference layer of all LCDC signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The decoupling capacitor of VCCIO5 must be placed on the back of the corresponding power pin.

### 3.2.20 BT1120 TX Interface Circuit PCB Design

Table 3–37 BT1120 TX signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended trace impedance requirements | 50Ω ±10% |
| Equal length requirements between all BT1120 signals and BT1120 CLK | Less than 180mil |
| Total length requirement of PCB trace | Less than 5000mil |
| Gap requirements between BT1120 signals | >=2 times the trace width |
| Gap requirements between BT1120 signal and other signals | >=3 times the trace width |
| BT1120 CLK routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

- In the overall layout, the BT1120 TX device should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The 22ohm series matching resistor of BT1120 CLK is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil
- The reference layer of all BT1120 signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The decoupling capacitor of VCCIO5 must be placed on the back of the corresponding power pin.

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### 3.2.21 Audio Interface Circuit PCB Design

- The LC device of RK809-5 SPK is placed close to RK809
- The VCC_SPK_HP trace of RK809-5 is greater than 50mil.
- SPKP/SPKN follow the differential routing and surrounded by ground in the whole group, with 20mil trace width, and the trace should be shortened as much as possible.
- The left and right channels of HP_L/HP_R should be surrounded by ground separately. If they are not differential lines, they cannot be close together. Otherwise it will reduce the isolation of the left and right channels. It is recommended that the line width be greater than 10mil.
- The HP_SNS network series resistor must be connected to the ground at the pin of the headphone socket to compensate the input and improve the isolation between the left and right channels

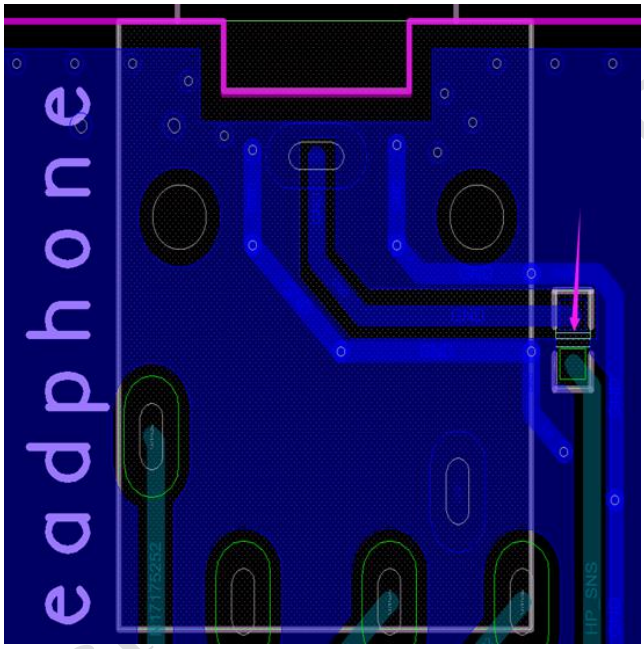


Figure 3-67 RK809-5 HP_SNS resistor layout and routing

- HP_SNS is used as the accompanying ground of HPL/HPR, routing in groups and surrounded by ground in parallel, the trace width of HPL/HPR should not exceed 10mil

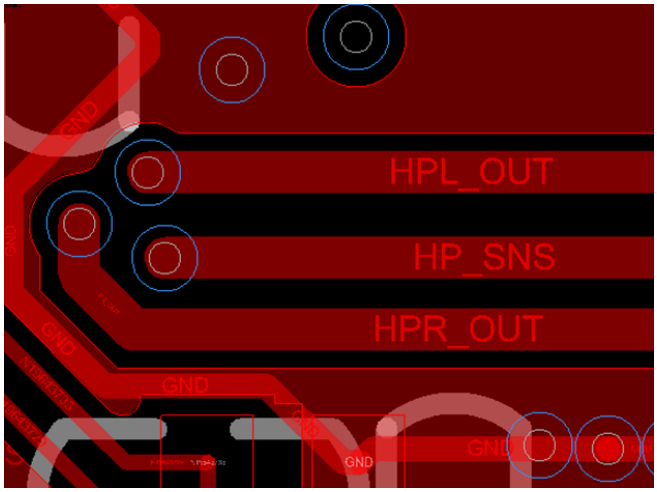


Figure 3-68 RK809-5 HPL/HPR/HP_SNS routing

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- When MIC single-ended connection, MIC1/MIC2 routing separately and are surrounded by ground separately.
- When MIC is differential connection, the MCP/MICN should follow differential routing and the whole group is surrounded by ground.
- MIC trace width is recommended to be more than 8mil
- Keep all audio signals away from high-speed signal lines such as LCD and DRAM. It is forbidden to rout on neighboring layers of high-speed signal traces, and the neighboring layers must be ground planes; it is forbidden to drill layer change vias near high-speed signal traces; do not pass through inductance areas and keep away from RF signals and devices.
- All neighboring layers of audio signals must not be power planes or traces.
- The TVS protection diode of the earphone socket/microphone should be placed as close as possible to the connection socket. The signal topology is: earphone socket/microphone--->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be stubs on the TVS device traces. It is recommended to increase the ground vias as much as possible for the ground pins of TVS, and at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capacity.
- S/PDIF signal is recommended to be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the trace interval of the ground.

## 3.2.22 GMAC Interface Circuit PCB Design

### 3.2.22.1 RGMII interface

Table 3–38 RGMII signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended trace impedance requirements | 50Ω ±10% |
| Equal length requirements between TXD0,TXD1,TXD2,TXD3,TXEN and TXCLK | Less than 120mil |
| Equal length requirements between RXD0,RXD1,RXD2,RXD3,RXDV and RXCLK | Less than 120mil |
| Total length requirement of PCB trace | Less than 5000mil |
| Gap requirements between RGMII signals | >=2 times the trace width |
| Gap requirements between RGMII signal and other signals | >=3 times the trace width |
| TXCLK and RXCLK routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

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**3.2.22.2 RMII interface**

Table 3–39 RMII signal impedance and layout requirements

| Parameters | Requirements |
|---|---|
| Single-ended trace impedance requirements | 50Ω ±10% |
| Equal length requirements between TXD0, TXD1, TXEN, RXD0, RXD1, RXDV, RXER and MCLKINOUT | Less than 300mil |
| Total length requirement of PCB trace | Less than 5000mil |
| Gap requirements between RGMII signals | >=2 times the trace width |
| Gap requirements between RGMII signal and other signals | >=3 times the trace width |
| MCLKINOUT routing requirements | It must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval. |

- In the overall layout, place GEPHY or FEPHY as close to RK3568 as possible to shorten the trace as much as possible.
- The 22ohm series matching resistance of TXD0-TXD3, TXCLK, TXEN is close to the CPU (source end), and the trace between CPU pin and the resistor must be controlled within 400mil.
- The 22ohm series matching resistors of RXD0-RXD3, RXCLK, and RXDV are close to the PHY end, and the trace between the PHY pin and the resistor must be controlled within 400mil.
- The 22ohm series matching resistor of ETH0_REFCLKO_25M and ETH1_REFCLKO_25M is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil.
- ETH0_REFCLKO_25M, ETH1_REFCLKO_25MIt must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval.
- RMII MCLKINOUT output mode: The 22ohm series matching resistor is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil.
- RMII MCLKINOUT input mode: The 22ohm series matching resistor is close to the PHY end, and the trace between the PHY pin and the resistor must be controlled within 400mil.
- The reference layer of all RGMII/RMII signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

Take RTL8211F/FI as an example, the following items are attentions on the PHY side:

- Give priority to the layout of the crystal circuit, which should be on the same layer as the chip and placed as close as possible to avoid drilling vias. The crystal traces should be as short as possible, away from interference sources, and away from the edge of the board as far as possible.
- The crystal and clock signals need to be surrounded by ground throughout the whole process. At least one GND via is added to the ground trace every 100 mils, and the ground reference plane of the neighboring layer must be complete.
- Be sure to confirm whether the RJ45 package is consistent with the schematic. RJ45 has tab down and tab

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up two types, and the signal sequence is just the opposite. If you use RTL8211F/FI, it is recommended to use Tab down, and the MDI sequence is direct.

- The network transformer should be as close to the RJ45 connector as possible, and the MDI trace should not exceed 4.5 inches
- The RSET resistor must be close to the pins of RTL8211F/FI, and the trace must not exceed 800mil, far away from other interference signals.
- The differential impedance of MDI differential signal from PHY to the network transformer is 100Ω ±10%.
- For the differential signals from PHY to the network transformer: MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-, their length deviation in the differential pair is controlled within ±5mil, and the MDI differential pair strictly follows the differential rules for routing. For example, keep the same length, the same width, the same layer and fixed trace spacing, and keep as symmetrical as possible
- The trace length delay between MDI differential pairs is controlled within 800 mils.
- Gap between MDI0/1/2/3: >=3 times the line width
- Gap between MDI0/1/2/3 and other signals: >=4 times the line width.
- Minimizes layer-changing vias on MDI. When layer-changing is unavoidable, two vias at most, and symmetrical ground stitching vias are placed near the signal vias.
- The reference layer of the MDI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- For the MDI differential pair on the high-voltage side of the network transformer, the trace width is recommended to be as thick as possible, and 8mil is recommended
- It is recommended that the 75 ohm resistor trace on the high voltage side of the network transformer be more than 25 mil.
- The center filter capacitor of the network transformer must be close to the corresponding pin of the network transformer
- The decoupling capacitors of PHY chip power supply should be placed as close as possible to the pins of PHY chip. When routing, try to pass the capacitor pads first, and then to the chip pins. The length of the trace between the pins and the capacitor should not exceed 100mil
- For the internal DCDC of RTL8211F/FI, the inductor must be close to the chip pins. The LX trace should be as short and thick as possible, the width should not be less than 60mil, and the length should not exceed 200mil. The output capacitor must be close to the inductor, the trace must pass through the output capacitor first and then to the latter stage. PiN21 and Pin3, 8, 38 must be routed separately in a star shape, and the width of the trace should be more than 30mil
- If the PHY IO is 3.3V, the VCCIO_PHY and VCC3V3_PHY power supply lines must be star-shaped, and the line width should be more than 30mil
- The center pad of PHY chip must be well grounded, and the vias must be placed at least 5X5 piece of 0.5*0.3mm vias
- The grounding of the anti-lightning diode must be well grounded. It is recommended that no less than 3X3 piece of 0.5*0.3mm vias are provided, otherwise the effect of the anti-lightning diode will be

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reduced

- Related components on the high-voltage side of the network transformer must be far away from the main ground of the PCB board
- The RJ45 interface and the high-voltage side of the network transformer belong to the high-voltage area, and copper-covering is forbidden. It is recommended to be separated from the low-voltage area by at least 4mm

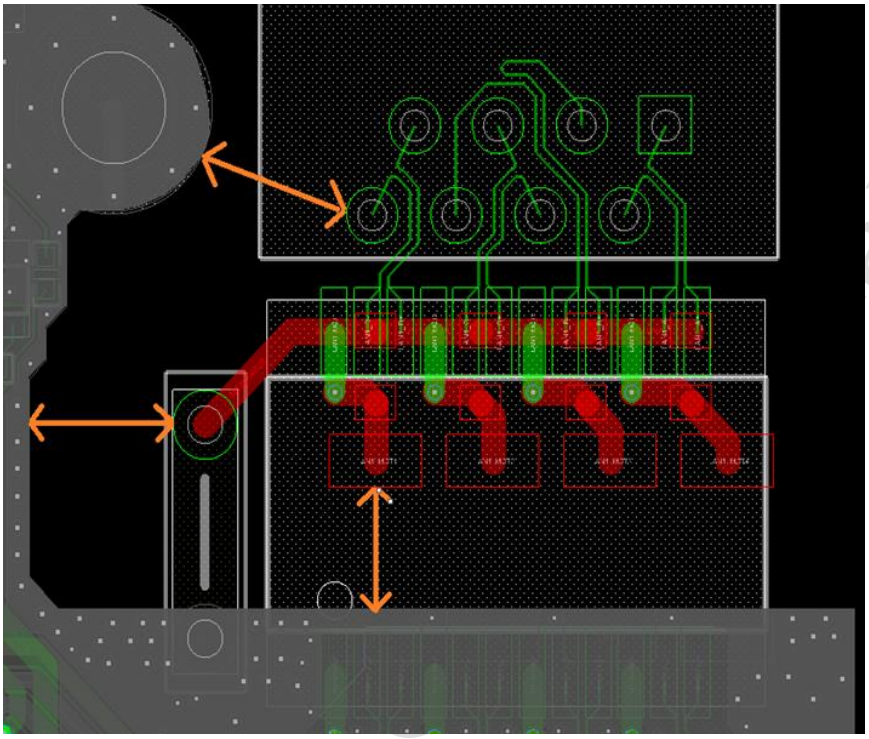

Figure 3-69 Schematic diagram of prohibited routing area for RJ45 interface and network transformer

- If possible, it is recommended to open a creepage of more than 1mm under the network transformer to strengthen the anti-surge capability.

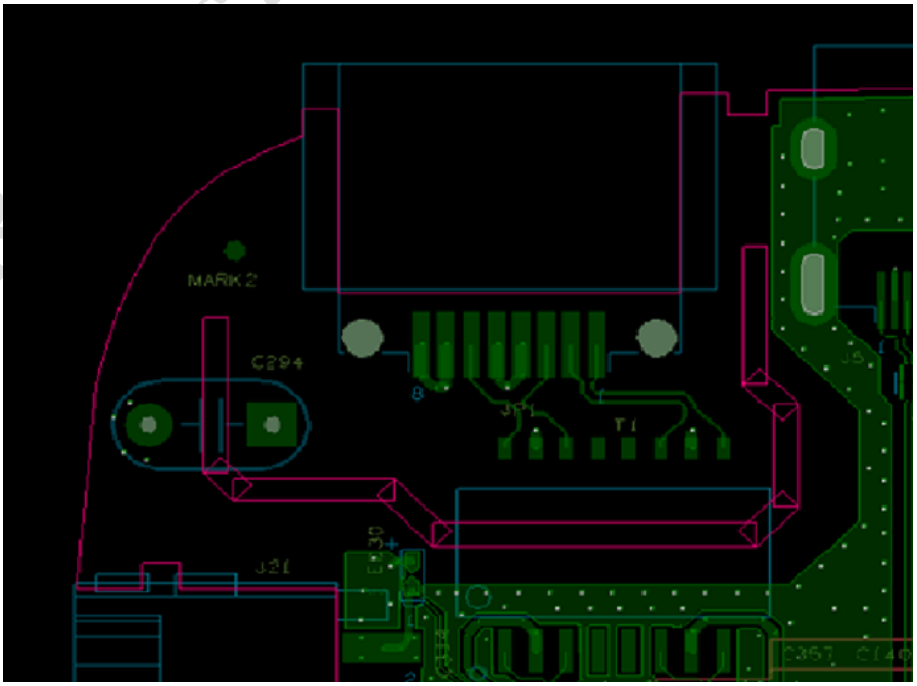


Figure 3-70 Schematic diagram of RJ45 interface and network transformer slotting

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### 3.2.23 WIFI/BT PCB Design

- In the overall layout, the WIFI module should be properly placed, and the module should be far away from DDR, HDMI, USB, LCD circuits, speakers and other easily interfered modules or connectors.
- No trace is allowed on the TOP layer below the module. Make sure that the reference plane is a complete ground plane. It is recommended that SDIO/PCIe/UART/PCM signal trace bypass the projection area of the module and connect to the module pins.
- Give priority to the crystal circuit layout which should be on the same layer as the chip and placed as close as possible to avoid vias. The crystal traces should be as short as possible, away from interference sources and antenna area as far as possible.
- The crystal and clock signals need to be surrounded by ground throughout the whole process. At least one GND via is added to the ground trace every 100 mils, and the ground reference plane of the neighboring layer must be complete.
- If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground all the way to avoid interference.
- 32.768k is routed separately and surrounded by ground, and at least one GND via is added every 400 mil for the ground trace
- For SDIO WIFI, please refer to chapter 3.2.5 requirements for PCB design requirements of SDIO signal
- For PCIe WIFI, please refer to chapter 3.2.11 or 3.2.12 for PCIe signal PCB design requirements
- When layout the inductance of the module, please note that after the trace comes out through the inductance, it passes through the capacitor first, and then enters the module power pin

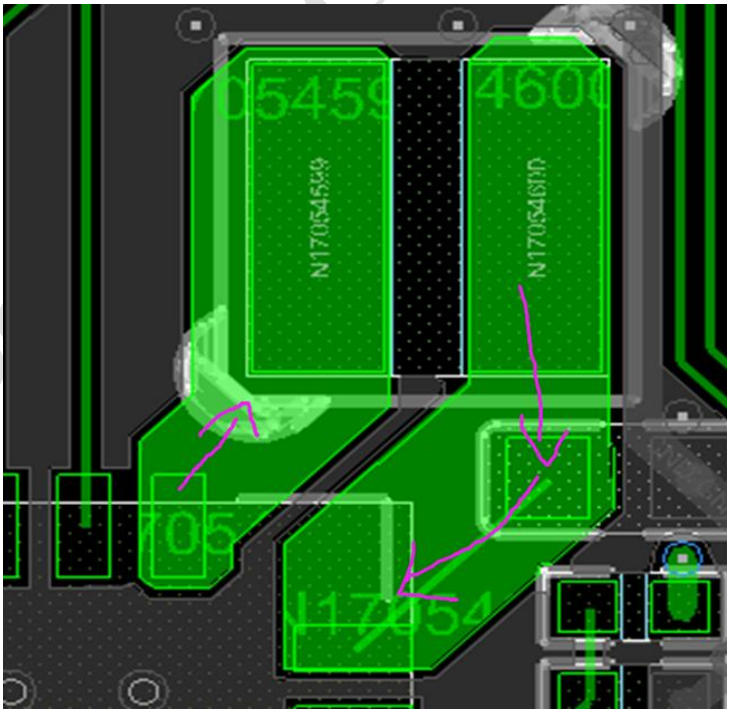

Figure 3-71 Schematic diagram of inductance and capacitance of the WIFI module routing

- The power decoupling capacitor of the module must be close to the power pin of the module
- The width of the VBAT pin trace of the module must be greater than 40mil
- The longer the antenna trace, the greater the energy loss. Therefore, in the design, the antenna path should

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be as short as possible. There should be no branches, and try not to change layers.

- The antenna matching circuit must be close to the antenna connector, and the antenna trace must be 50 ohms to ensure that the reference ground is complete, the impedance does not change suddenly, and no other signal traces or power sources are allowed below; the accompanying ground of the trace needs to be connected to the main ground reference plane by ground wall.

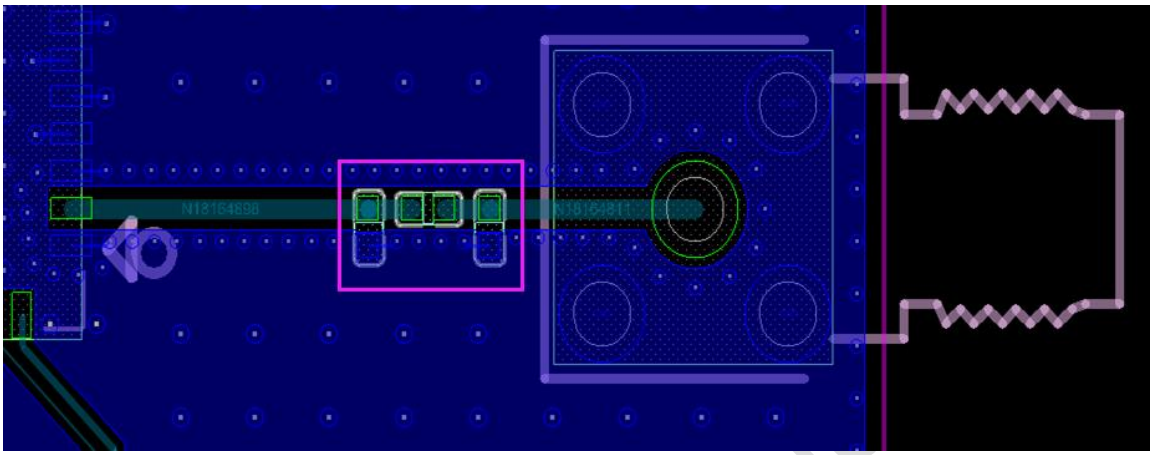

Figure 3-72 Schematic diagram of WIFI module antenna routing

- The antenna of the module and all layers below the antenna routing area are not allowed to other signal traces or power sources
- If it is a 2X2 MIMO antenna interface, the exit direction between the two antenna ports has to consider the location of the two antennas where should be as far away as possible to avoid interference, and vertical placement is recommended to avoid mutual interference

### 3.2.24 VGA OUT PCB Design

- In the overall layout, the VGA connector should be placed as close to the conversion chip as possible, and the VGA analog signal trace should be shortened as much as possible.
- The decoupling capacitors for the power supply of the conversion chip should be placed as close as possible to the power supply pins of the conversion chip.
- The VGA_R/G/B trace width should be as thick as possible, and it is recommended to be more than 12mil.
- The length difference between VGA_R/G/B must not exceed 200mil
- VGA_R/G/B 75ohm resistor must be placed close to the chip
- The VGA_R/G/B filter circuit must be placed close to the VGA connector
- VGA_R/G/B signals are required to be surrounded by ground separately in the whole process, and there must be ground vias within 300 mils of the ground traces.
- The neighboring layer of VGA_R/G/B signal must be ground plane instead of power plane
- Keep VGA_R/G/B signals away from high-speed signal lines such as LCD, DRAM, etc. It is forbidden to route on the neighboring layers of high-speed signal trace; it is forbidden to drill vias to change layers near high-speed signal traces; do not route through inductance areas; keep away from RF signals and devices.

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- The RC filter of VGA_HSYNC/VSYNC must be placed close to VGA connector, and the trace must not exceed 6 inches
- All signal TVS diode of VGA connector should be placed as close as possible to the connector. The signal topology is: VGA socket--->TVS--->chip pins; when an ESD phenomenon occurs, the ESD current must be attenuated by the TVS device first; There should not be stubs on the TVS device trace.
- It is recommended to increase the ground vias as much as possible for the ground pins of TVS, at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

### 3.2.25 LCD Screen and Touch Screen PCB Design

- Please place the current limiting resistor on the FB side of the LED backlight IC close to the screen connector instead of DC-DC.
- For backlight boost circuit, please pay attention to capacitor placement and power supply trace to ensure that the power supply's charging and discharging loop is minimized.
- If there are reserved test points for the screen and touch screen connectors, they should be close to the connector and the stub on the trace should be as short as possible.

### 3.2.26 Camera PCB Design

- When the camera is with a connector: when the MIPI differential signal passes through the connector, the GND pin must be used for isolation between neighboring differential signal pairs.
- For CIF/MIPI and other signals, if there is a board-to-board connection is realized through the connector, it is recommended that all signals be connected in series with a certain resistance (between 2.2ohm-10ohm as long as it can meet the SI test), and reserved TVS device.
- If the camera connector has reserved test points, it should be close to the connector and the stub on the trace should be as short as possible
- The decoupling capacitors of the AVDD/DOVDD/DVDD power supply of the connector should be placed as close to the camera connector as possible.
- The camera layout needs to be far away from high-power radiating devices, such as GSM antennas.
- Please refer to section 3.2.13 for MIPI CSI RX signal PCB design requirements
- Please refer to section 3.2.14 For CIF signal PCB design requirements

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# 4 Thermal Design Suggestion

Good thermal design is especially important for the improvement of RK3568 product performance, system stability, and product safety

## 4.1 Thermal Simulation Result

Aiming at RK3568 FCBGA636_19x19mm_Pitch 0.65mm package, the EVB which is based on 4 layer PCB and Finite Element Modeling (FEM) to obtain a thermal resistance simulation report. The report is based on JEDEC JESD51-2 standard. The system design and application environment may be different from JEDEC jesd51-2 standard, which needs to be analyzed according to actual application conditions.

Note

*Thermal resistance is the reference value when there is no radiator on PCB. The detailed temperature is related to the board's size, thickness, material and other physical factors.*

### 4.1.1 Result Overview

Thermal resistance simulation results are as follows:

Table 4–1 RK3568 thermal resistance simulation report results

| Package (EHS-FCBGA) | $\theta_{JA}$(℃/W) | $\theta_{JB}$(℃/W) | $\theta_{JC}$(℃/W) |
|---|---|---|---|
| JEDEC PCB | 15.925 | 10.813 | 0.487 |

Note: The simulated data is only used for reference only.

### 4.1.2 PCB Description

The PCB structure used for thermal resistance simulation is as follows:

Table 4–2 RK3568 PCB structure used for thermal resistance simulation

| | | |
|---|---|---|
| EVB PCB | PCB Dimension（L x W） | 114.3 x 101.6mm |
| | PCB Thickness | 1.6mm |
| | Number of Cu Layer | 4-layers |

### 4.1.3 Terms Interpretation

Terms in this chapter are explained below：

- $T_J$: The maximum junction temperature；
- $T_A$: The ambient or environment temperature；
- $T_C$: The maximum compound surface temperature；
- $T_B$: The maximum surface temperature of PCB bottom；
- P: Total input power

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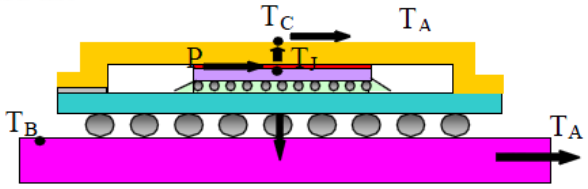
The thermal parameter can be define as following

**1.** *Junction to ambient thermal resistance,* $\theta_{JA}$**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$

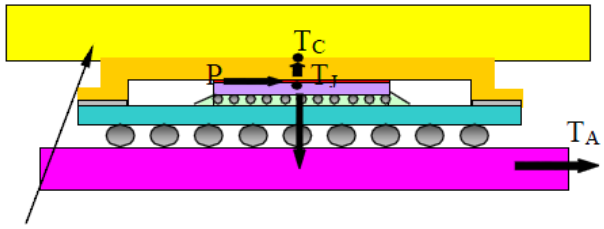



**Thermal Dissipation of EHS-FCBGA**

Figure 4-1 $\theta_{JA}$ definition

**2.** *Junction to case thermal resistance,* $\theta_{JC}$**, defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad ; \qquad (2)$$

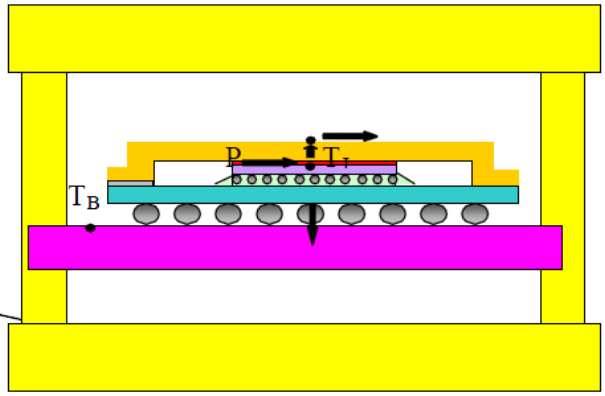



**Attach a block with constant temperature onto package.**

Figure 4-2 $\theta_{JC}$ definition

**3.** *Junction to board thermal resistance,* $\theta_{JB}$**, defined as:**

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad ; \qquad (3)$$




**Attach a block with constant temperature**

Figure 4-3 $\theta_{JB}$ definition

## 4.2 Thermal Control Method inside the Chip

### 4.2.1 Thermal Control Strategy

In Linux kernel, it defines one thermal control frame called Linux Generic Thermal System Drivers, which can

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control system temperature through different strategies. Currently below 3 strategies are commonly used:

- Power_allocator: Introduce PID (percentage-integral-differential) control to dynamically allocate power for cooling device according to current temperature, when the temperature is low, the power that can be allocated is larger, that is, the frequency that can be operated is higher. As the temperature rises, the power that can be allocated is gradually reduced, and the frequency that can be operated is gradually reduced, so as to achieve the effect of limiting frequency according to temperature.
- Step_wise: Limit frequency step by step according to current temperature.
- Fair share: The cooling devices with more frequency gears will give priority to frequency reduction
- Userspace: Do not limit frequency.

There is a T-sensor inside the RK3568 to detect the on-chip temperature, and the Power_allocator strategy is used by default

### 4.2.2 Temperature Control Configuration

RK3568 SDK can provide temperature control strategies for CPU and GPU separately, please refer to the document for detailed configurations: “Rockchip_Developer_Guide_Thermal_CN.pdf”.

## 4.3 Thermal Design Reference

### 4.3.1 Circuit Schematic Thermal Design Reference

- Under the condition of stability, provide overall power efficiency, such as using as less as high-voltage LDOs, and reduce the heat generated by the power supply itself during the power conversion process
- According to actual products, try not to supply power to the modules that are not used by the chip or do power down processing by software
- Choose a material with a large thermal conductivity, and re-estimate the size of the radiator to be used according to the "Calculation of Radiator Size" according to the product definition, usage environment and other conditions. It is recommended to use a larger radiator as much as possible

### 4.3.2 PCB Thermal Design Reference

For RK3568 products, RK3568 chip is the device that generates the most heat, so all heat dissipation treatments should be based on the chip.

Except RK3568, other main heating devices include: PMIC, charging IC and related inductors, backlight IC and related inductors.

- Reasonable structural design can ensure that there is a heat exchange path between the internal machine and air.
- In the overall layout, the components with high power consumption or heat generation should be uniformly distributed to avoid local overheating. It is recommended RK3568 and RK809-5 should be placed appropriately, not too close or too far away. It is recommended that the distance between the two is 20mm-50mm. Avoid to place them on the edge of the board, for bad heat dissipation.
- It is recommended to use a 6-layer board or more to increase the copper of the board as much as possible.

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It is recommended to use a copper thickness of 1oz, and try to use much ground layers as possible. Other layers should follow the power and signal routing rules, and try to place as much ground copper as possible, with the help of a large area of copper for dissipates heat.

- RK3568 VDD_LOGIC, VDD_GPU, VDD_NPU, VDD_CPU, VCC_DDR have relatively large currents, the routing or copper must meet the current-carrying capacity, otherwise it may increase the temperature rise
- For chips with EPAD, drill as many vias as possible on the EPAD, the neighboring layer must be a ground layer, and the copper on the back side should be as complete as possible. It is recommended that the copper on the back should be bare copper, which is good for heat dissipation.
- The GND pins of RK3568 chip is routed in "井" shape on the top layer and are cross-connected. It is recommended that the trace width is 10mil, which is beneficial to the heat dissipation of the chip.
- For the GND pin of RK3568 chip, it is recommended to try to ensure that each ball has a corresponding ground via. At least ensure that every 1.5 ball corresponds to one via to increase the heat conduction path. The neighboring layer must be a ground layer, which is good for heat dissipation of the chip.
- For decoupling capacitor ground pad on the back of RK3568 chip, it is recommended to use full copper covering, do not use flower holes to connect, try to make the ground copper as complete as possible to improve heat dissipation
- In empty areas, without damaging the power layer, try to increase ground vias and increase heat conduction paths to improve heat dissipation

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# 5 ESD/EMI Protection Design

## 5.1 Overview

This chapter provides ESD/EMI protection design suggestion for RK3568 product design to help customers to improve anti-static and anti-electromagnetic interference ability of product.

## 5.2 Terms Interpretation

Terms of this chapter are explained as below：

- ESD: Electro-Static discharge；
- EMI: Electromagnetic Interference, including conduction interference and radiation interference

## 5.3 ESD Protection

- Ensure reasonable mold design, retract connectors in the shell as much as possible, so that the distance from static electricity to the internal circuit becomes longer and the energy becomes weaker. The test standard changes from contact discharge conditions to air discharge, etc.
- Protect and isolate sensitive components in PCB layout.
- Try best to put the RK3568 and core components in the center of PCB layout. If it may not be able to put them in the center, ensure that the shielding cover has 2mm distance at least from the board edge and is connected to GND safely
- PCB layout is based on function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the parts that are easy to produce interference;
- Place ESD components reasonably. Generally place then near the source, that is, place ESD components in the junction or where electrostatic discharge.
- The layout of the components should be far away from the edge of the board and a certain distance from the connector
- The PCB surface should have a good GND loop, and each connector should be with good GND connection loop on the surface. If there is a shielding cover, it should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area;
- Do not go through the edge of surface layer and make as many ground vias as possible.
- Isolate signal from ground if necessary.
- Expose GND copper of PCB as much as possible, in order to strengthen the electrostatic discharge effect, or to facilitate to add foam and other remedial measures
- If there is a board-to-board connection through the connector, it is recommended that all signals be connected in series with a certain resistance (between 2.2ohm-10ohm, as long as it can meet the SI test), and reserved TVS devices, which can improve antistatic surge capacity

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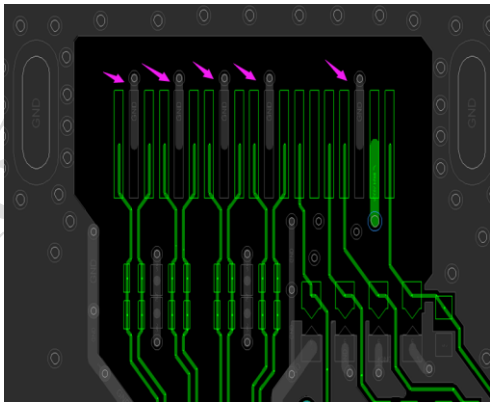
- The 100nF capacitor of the nPOR pin of RK3568 must be placed close to the pin, and the ground pad of the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.
- The distance between key signals such as Reset, clock, interrupt and other sensitive signals from the edge of the board should not be less than 5mm
- If other peripheral chips have Reset pins, it is recommended to add a 100nF capacitor close to the pin. The ground pad of the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.
- When the whole device is designed as a ground-floated device, it is recommended not to design each interface with separate ground.
- When the device casing is metal, with a three holes power, and the metal casing must be well connected to the ground.
- Reserve the shielding cover position. The shielding cover should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area.
- Isolate from PCB, so that static electricity can only be released in some areas, such as the ground pin of the connector is connected with the inner layer through a separate vias, keep out the surface PCB, and keep the surface ground copper and pins as far away as possible, that is, keep sensitive signals away from electrostatic discharge areas (surface copper), etc., as shown in the figure, isolate the distance between HDMI signal and GND on the surface.



## 5.4 EMI Protection

- Electromagnetic interference has three factors: interference sources, coupling channels and sensitive devices. We have no way to deal with sensitive devices, so EMI problem can only start with interference sources and coupling channels. The best way to resolve EMI issues is to eliminate interference source. If it cannot eliminate, try to cut off coupling channels or avoid antenna effect.
- It is difficult to eliminate interference source on PCB. We can take actions such as filtering, grounding, balancing, resistance controlling, improving signal quality (e.g. termination connection) etc. Generally several methods will be applied together, but the basic requirement is good grounding.
- The commonly used EMI materials include shielding cover, special filter, resistor, capacitor, inductor,

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magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread frequency device etc.

- The rules to select filters: if the load (receiver) is high resistance (regular single ended signal interface is high resistance, such as SDIO, RBG, CIF etc.), select capacitive filter components and parallel connect to circuit; if the load (receiver) is low resistance (such as power output interface), select inductive filter component and serial connect to circuit. After using the filter device, the signal quality cannot exceed its SI permission. Differential interface usually uses common mode choke to suppress EMI.
- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should comply with relevant technical standards.
- RK3568 spread spectrum function is divided into modules. The degree of spreading depends on the signal requirements of the relevant part. See RK3568 spreading instructions for detailed measures;
- Please don't delete the RC circuit between DDR3_CLKP/N, DDR4_CLKP/N, LPDDR3_CLKP/N, which can improve EMI
- It is recommended to keep the matching resistance of all clocks connected in series, which will provide matching impedance, and improve the improvement measures of signal quality
- At the DC power input, the common mode inductance or EMI filter of the power supply can be reserved if possible
- Add reserved common mode inductance or filter circuit at USB, HDMI, VGA, screen connector and other interfaces
- When a radiator is added, it should be noted that the radiator may also couple EMI energy and generate radiation. When selecting a radiator, in addition to meeting the thermal design requirements, it should also meet the EMI test requirements. Grounding conditions should be reserved for the radiator. When grounding is required, the radiator should be grounded. It is not easy to clarify the number of grounding points and how to choose the grounding point. It needs to be adjusted according to the actual test of the first version of hardware in the laboratory.
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add the following requirements:
  - Try best to ensure the integrity of the signal;
  - Differential line should in equal length and be tight coupling to ensure the symmetry of the differential signal, minimize the misplacement of differential signals to avoid EMI problems caused by phase mismatch;
  - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from shell to other signal lines.
  - The matching resistors of all clocks connected in series should be placed close to CPU (source end), and traces between CPU pins and the resistors must be controlled within 400 mils.
  - If the PCB exceeds 4 layers, it is recommended that all clock signals go to the inner layer as much as possible
  - To prevent power radiation, the copper of the power supply layer must be retracted, with one H (the

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thickness of the medium between the power supply and ground) as the unit, and it is recommended to indented by 20H

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# 6 Soldering Process

## 6.1 Overview

RK3568 are ROHS certified products, that is, they are all Lead-free products. This chapter regulates basic temperature settings of each period when customers use the chipset to SMT. It mainly introduces process control when using RK3568 chipset to do reflow soldering: lead-free process and mixed process.

## 6.2 Terms Interpretation

Terms in this chapter are explained below:

- Lead-free: Lead-free process；
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and the lead-free solder paste are used in the pure lead-free process;
- Reflow profile: reflow soldering
- Restriction of Hazardous Substances (ROHS): instructions for restricting use of certain hazardous components in electrical and electronic equipment;
- Surface Mount Technology(SMT)；
- Sn-Pb: Sn-Pb mixing process refers to using lead solder paste and a mixed soldering process with both lead-free BGA and lead IC;

## 6.3 Reflow Soldering Requirements

### 6.3.1 Solder Paste Composition Requirements

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10℃, it should be returned to normal temperature before use, and the return time should be 3~4 hours and the time should be recorded.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes. After stirring, it will flow naturally.

### 6.3.2 SMT Profile

Since RK3568 chipset are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020D process requirements, and customers need to adjust according to actual production conditions.

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| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_p$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body temperature ($T_p$)* | See classification temp in Table 4.1 | See classification temp in Table 4.2 |
| Time ($t_p$)** within 5 °C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25 °C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Figure 6-1 Reflow soldering profile classification

| Package Thickness | Volume mm³ <350 | Volume mm³ 350 - 2000 | Volume mm³ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm - 2.5 mm | 260 °C | 250 °C | 245 °C |
| >2.5 mm | 250 °C | 245 °C | 245 °C |

Figure 6-2 Heat resistance of lead-free process device packages standard

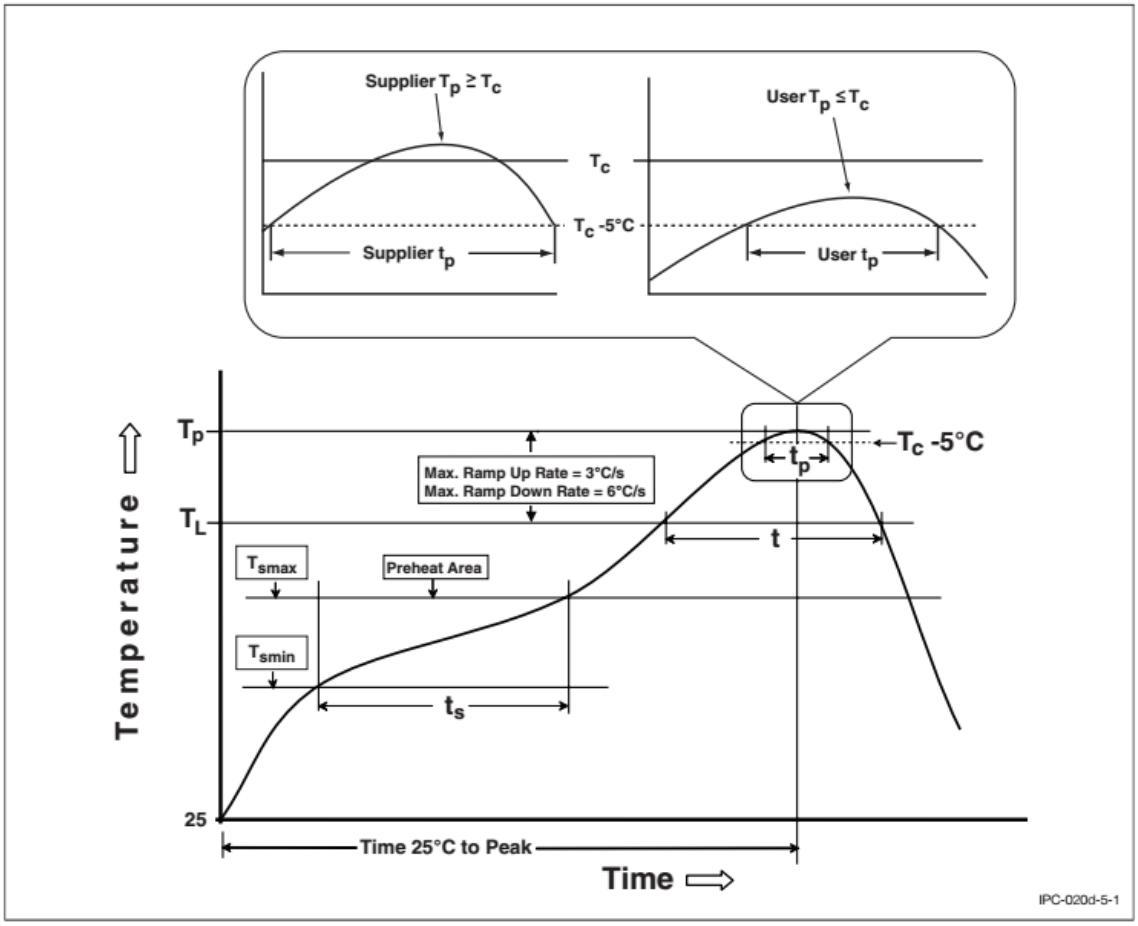


Figure 6-3 Lead-free reflow profile

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### 6.3.3 SMT Recommendation Profile

The SMT profile recommended by RK is shown in Figure 6-4：

| Step 1<br>Board Preheat | Step 2<br>Soak Time | Step 3<br>Peak Reflow & Time Above 220 °C | Step 4<br>Cool Down |
|---|---|---|---|
| Start with solder joint temp ≤ 40°C | After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer) | Solder Joint Temp 230 – 250°C<br>Above ≥217°C 60 – 90 sec<br>Max delta-t of solder joint temperature at peak reflow ≤10°C | Substrate MAX Temperature ≤260°C<br>Die Peak Temperature ≤300°C |
| Rising Ramp Rate 0.5 – 2.5° C/ Sec. | Solder Joint Temp: 200 to 220°C | | Cooling Ramp Rate -0.5 to – 2.0°C/sec |
| Board Preheat Solder Joint Temp: 125 – 150°C | Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec. | Peak Temp Range, and Time Above ≥217°C spec's met. | PCB land/pad temperature needs to be at 100 – 130°C ±5°C when removing board from rework machine bottom heater at end of component removal operation or ≤80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation. |
| Preheat with bottom heater, before nozzle is lowered | Nozzle has lowered to reflow component | Nozzle is down during peak reflow | Nozzle raises to home position when solder joint reaches peak temp range |

Figure 6-4 Lead-free reflow soldering process recommended profile parameters

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# 7 Packages and Storage Conditions

## 7.1 Overview

This chapter introduces the storage and directions for RK3568 usage to ensure the safety and correct usage of products.

## 7.2 Terms Interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking moisture barrier bag to reflow soldering;
- HIC: Humidity Indicator Card
- MSL: Moisture Sensitivity Level
- MBB: Moisture Barrier Bag
- Rebake: to bake again
- Solder Reflow
- Shell Life
- Storage environment

## 7.3 Moisture Packages

The dry vacuum package material of product is shown as follows：

- Desiccant；
- Six-point humidity card；
- Moisture barrier bag: aluminum foil, silver opaque, with a mark of moisture sensitivity level;

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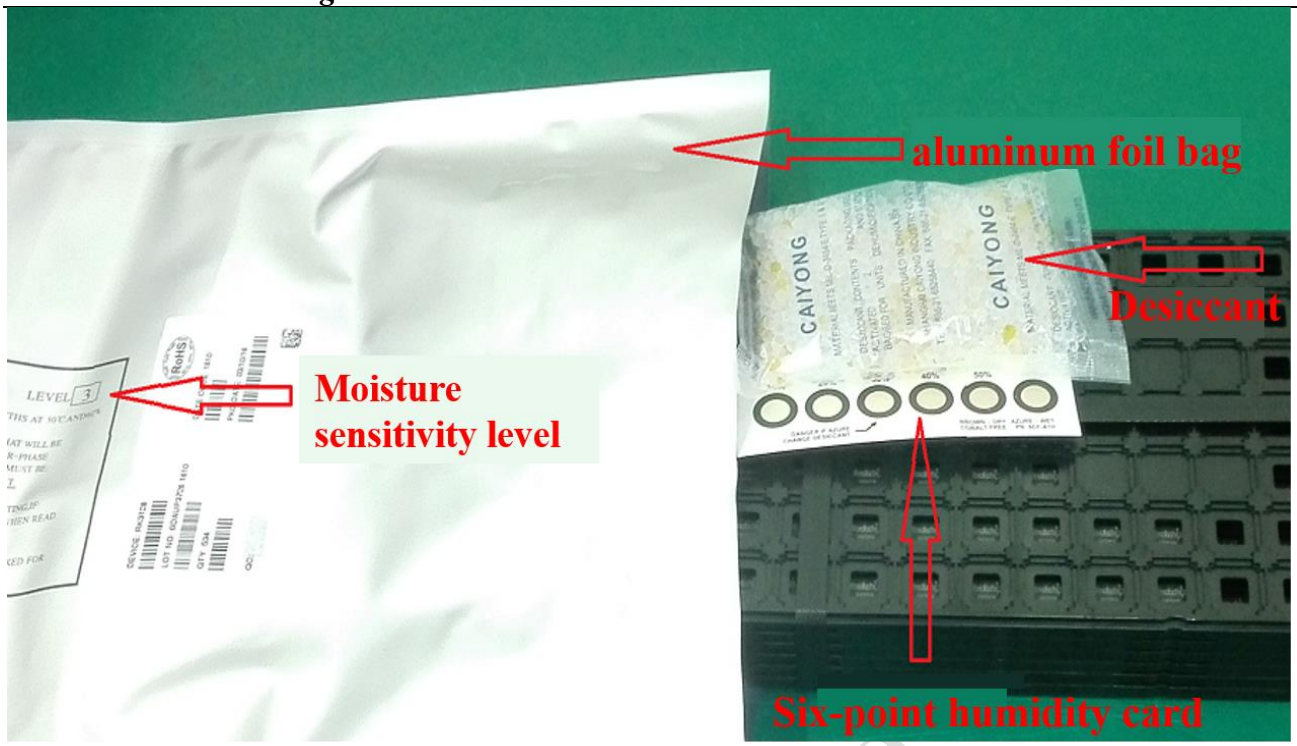


Figure 7-1 Chipset dry vacuum package

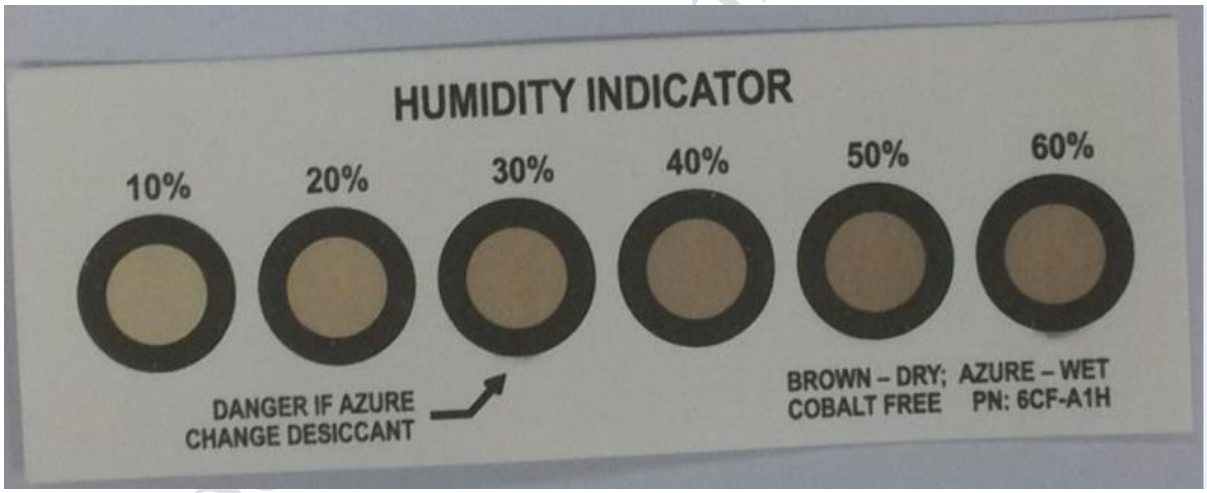


Figure 7-2 Six-point humidity card

## 7.4 Product Storage

### 7.4.1 Storage Environment

The product is stored in vacuum packaging, and the storage time can reach 12 months when the temperature is ≦40℃ and the relative humidity is <90%.

### 7.4.2 Exposure Time

For environmental conditions: <30℃ and humidity 60%, please refer to Table 7-1 below.

The MSL level of RK3568 chipset is 3 and is very sensitive to humidity. If package is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of

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chip failure.

Table 7–1 Moisture Sensitivity Levels (MSL)

| MSL Level | Exposure time<br>Factory environmental conditions:≦30℃ /60％RH |
|---|---|
| 1 | Unlimited at ≤300 ℃/85％RH |
| 2 | 1 year |
| 2a | 4 weeks |
| 3 | 168 hours |
| 4 | 72 hours |
| 5 | 48 hours |
| 5a | 24 hours |
| 6 | Mandatory bake before use, and must be reflowed within the time limit specified on the label |

## 7.5 Usage of Moisture Sensitive Products

After RK3568 packages are opened, it must meet the following conditions before reflow soldering：

- Continuous or cumulative exposure time is within 168 hours, and factory environment is ≦30℃/60％ RH;
- Stored in <10% RH environment;
- Chips must be baked to remove internal moisture under the following conditions to avoid layered or popcorn problems during reflow:
- When humidity indicator card is at 23±5°C, >10% points have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 7-2 below for the time for chip re-baking:

Table 7–2 RK3568 Re-bake reference table

| Package Body | MSL | High Temp Bake @125℃ +10/-0℃ | | Medium Temp Bake @90℃+8/-0℃ | | Low Temp Bake @40℃ +5/-0℃ | |
|---|---|---|---|---|---|---|---|
| | | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h |
| Thickness ≤1.4mm | 3 | 9 hours | 7 hours | 33 hours | 23 hours | 13 days | 9 days |

Note

*The Table shows the minimum baking time necessary after damp.*

*Low temperature baking is preferred.*

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