

# RK3568 Hardware Design Guide

Release Version: V1.2 Release Date: 2022-01-26

2004

#### DISCLAIMER

THIS DOCUMENT IS PROVIDED "AS IS". ROCKCHIP ELECTRONICS CO., LTD.("ROCKCHIP")DOES NOT PROVIDE ANY WARRANTY OF ANY KIND, EXPRESSED, IMPLIED OR OTHERWISE, WITH RESPECT TO THE ACCURACY, RELIABILITY, COMPLETENESS,MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY REPRESENTATION, INFORMATION AND CONTENT IN THIS DOCUMENT. THIS DOCUMENT IS FOR REFERENCE ONLY. THIS DOCUMENT MAY BE UPDATED OR CHANGED WITHOUT ANY NOTICE AT ANY TIME DUE TO THE UPGRADES OF THE PRODUCT OR ANY OTHER REASONS.

#### **Trademark Statement**

"Rockchip", "瑞芯微", "瑞芯" shall be Rockchip's registered trademarks and owned by Rockchip. All the other trademarks or registered trademarks mentioned in this document shall be owned by their respective owners.

#### All rights reserved. ©2020. Rockchip Electronics Co., Ltd.

Beyond the scope of fair use, neither any entity nor individual shall extract, copy, or distribute this document in any form in whole or in part without the written approval of Rockchip.

瑞芯微电子股份有限公司 Rockchip Electronics Co., Ltd. Address: No. 18 Building, A District, No.89, software Boulevard Fuzhou, Fujian, PRC Website: <u>www.rock-chips.com</u> Customer service tel.: +86-4007-700-590 Customer service fax: +86-591-83951833 Customer service e-mail: <u>FAE@rock-chips.com</u>

Rockc

# Preface

#### **Overview**

This document presents the key points of hardware design and notices for RK3568 processors, aiming to help customers shorten developing period of product, improving product design stability and reducing fault rate. Please refer to the requirements of this guide for hardware design, and use the relevant core templates released by Rockchip. If you need to modify for special reasons, please strictly follow the design rule of ridentia high-speed-digital-circuit and Rockchip Schematic&PCB checklist requirements.

#### **Chipset Model**

This document is suitable for the following chipset model: RK3568

#### **Intended Audience**

This document (this guide) is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers •

# **Revision History**

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Remark
V1.2	Zhangdz	2021-10-14	1:Update the description of ECC (Section 2.1.7.2)	
V1.1	Zhangdz	2021-06-08	<ol> <li>Update the description of wake-up and standby of infrared receiver (Section 2.3.17)</li> <li>Add IO Domain power supply and software configuration attentions (Section 2.1.11)</li> <li>Update the DCDC power supply capacity requirements of VDD_NPU and VDD_LOGIC power supplies, which require 2A or more (Section 2.2.2.6 and 2.2.2.7)</li> <li>VDD_LOGIC peak current is updated to 1.2A (Section 2.2.6)</li> <li>Add a description of the module that does not supply power, and the corresponding node in DTS should be disabled (Section 2.2.2.1)</li> </ol>	
V1.0	Zhangdz	2021-04-16	The initial release version	

Rocken

# Acronyms

Acronyms include the abbreviations of commonly used phrases in this document:

ARM	Advanced RISC Machine	享仍特简指众生计算机
		高级精简指令集计算机
CAN	Controller Area Network	控制器局域网络
CEC	Consumer Electronics Control	消费电子控制
CIF	Camera Input Format	相机并行接口
CPU	Central processing unit	中央处理器
CSI	Camera Serial Interface	相机串行接口
DC/DC	Direct current-Direct current converter	直流/直流变换器
DDR	Double Data Rate	双倍速率同步动态随机存储器
DP	DisplayPort	显示接口
DSI	Display Serial Interface	显示串行接口
EBC	E-book controller	电子书控制器
eDP	Embedded DisplayPort	嵌入式数码音视讯传输接口
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
ESD	Electro-Static discharge	静电释放
ESR	Equivalent Series Resistance	等效电阻
Flash_VOL_SEL	Flash voltage selection	eMMC/Nand Flash IO电压选择
FSPI	Flexible Serial Peripheral Interface	灵活串行外设接口
GPU	Graphics Processing Unit	Figure形处理单元
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
HPD	Hot Plug Detect	热插拔检测
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总 线)
I2S	Inter-IC Sound	集成电路内置音频总线
ISP	Image Signal Processing	Figure像信号处理
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议(IEEE 1149.1兼容)
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LCDC	LCD Controller	LCD 控制器并行接口
LCM	LCD Module	LCD显示模组
LVDS	Low-Voltage Differential Signaling	低电压差分信号
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
NPU	Neural network Processing Unit	神经网络处理器
РСВ	Printed Circuit Board	印制电路板

KKJJ00 Huruw	are Design Guide	KeV V 1.2
PCIe	Peripheral Component Interconnect -express	外设组件互联标准
РСМ	Pulse Code Modulation	脉冲编码调制
PDM	Pulse density modulation	脉冲密度调制
PLL	Phase-locked loop	锁相环
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
PWM	Pulse width modulation	脉冲宽度调制
QSGMII	Quad Serial Gigabit Media Independent Interface	四串行千兆媒体独立接口
RGB	RGB color mode is a color standard in industry	RGB色彩模式,是工业界的一种颜 色标准
GMAC	Gigabit Media Access Controller	千兆媒体访问控制器
RGMII	Reduced Gigabit Media Independent Interface	简化千兆媒体独立接口
RMII	Reduced Media Independent Interface	简化媒体独立接口
RK	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
SARADC	successive approximation register Analog to digital converter	逐次逼近寄存器型模数转换器
SATA	Serial Advanced Technology Attachment	串行高级技术附件
SCR	Smart Card Reader	智能卡读卡器
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output Card	安全数字输入输出卡
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SGMII	Serial Gigabit Media Independent Interface	串行千兆媒体独立接口
SPDIF	Sony/Philips Digital Interface Format	SONY、PHILIPS数字音频接口
SPI	Serial Peripheral Interface	串行外设接口
SubLVDS	Sub- Low-Voltage Differential Signaling	低摆幅差分信号技术
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
TSADC	Temperature sensing A / D converter	温度感应模数转换器
UART	Universal Asynchronous Receiver / Transmitter	通用异步收发传输器
VOP	Video Output Processor	视频输出处理器
VPU	Video Processing Unit	视频处理器
	Universal Serial Bus 2.0	通用电行台建
USB2.0	Universal Serial Bus 2.0	通用串行总线

## Contents

Contents	
Figures	VIII
Tables	XV
1 System Introduction	
1.1 Overview	
1.2 Block Diagram	
1.3 Application Block Diagram	
1.3.1 RK3568 EVB Application Block Diagram	
1.3.2 RK3568 Smart NVR Application Block Diagram	
1.3.2 RK3568 Smart NVR Application Block Diagram         2 Schematic Design Recommendation	
2.1 Minimum System Design	
2.1.1 Clock Circuit	
2.1.2 Reset/watchdog/TSADC Circuit	6
2.1.3 PMU Circuit	
2.1.4 System Boot Sequence	
2.1.5 System Initialization Configuration Signal	
2.1.6 JTAG and UART Debug Circuit	
2.1.7 DDR Circuit	
2.1.8 eMMC Circuit	
2.1.9 FSPI Flash Circuit	
2.1.10 Nand Flash Circuit	
2.1.11 GPIO Circuit	
2.2 Power Supply Design	
2.2.1 RK3568 Power Supply Introduction	
2.2.2 Power Supply Design Suggestion	
2.2.3 RK809-5 Solution Introduction	
2.2.4 Discrete Power Supply Solution Introduction	59
2.2.5 Standby Control Circuit	
2.2.6 Power Peak Current Table	
2.3 Functional Interface Circuit Design Guide	
2.3.1 SDMMC0/1/2	
2.3.2 SARADC Circuit	69
2.3.3 OTP Circuit	
2.3.4 USB2.0/USB3.0 Circuit	
2.3.5 SATA3.0 Circuit	
2.3.6 QSGMII/SGMII Circuit	
2.3.7 PCIe2.0 Circuit	
2.3.8 PCIe3.0 Circuit	
Copyright © 2022 Rockchip Electronics Co., Ltd.	V

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
2.3.9 Video Input Interface Circuit	
2.3.10 Video Output Interface Circuit	
2.3.11 Audio Interface Circuit	118
2.3.12 GMAC Interface Circuit	137
2.3.13 UART Interface Circuit	144
2.3.14 SPI Interface Circuit	146
2.3.15 CAN Interface Circuit	146
2.3.16 I2C Interface Circuit	147
2.3.17 PWM Interface Circuit	148
2.3.18 RK3568 Unused Modules Pins Processing	150
3 PCB Design recommendations	
3.1 PCB Layers Design	
3.1.1 Six Layers PCB Design	
3.1.2 Four Layers PCB Design	152
3.1.3 RK3568 Fan-out Design	
3.2 Interface PCB Design Recommendations	
3.2.1 Clock/Reset Circuit PCB Design	
3.2.2 PMIC/Power Circuit PCB Design	158
3.2.3 DRAM Circuit PCB design	
3.2.4 Flash Circuit PCB design	
3.2.5 SDMMC0/1/2 Interface Crcuit PCB Design	199
3.2.6 SARADC/OTP Interface Circuit PCB Design	200
3.2.7 USB2.0 Interface Circuit PCB Design	200
3.2.8 USB3.0 Interface Circuit PCB Design	201
3.2.9 SATA3.0 Interface Circuit PCB Design	202
3.2.10 QSGMII/SGMII Interface Circuit PCB Design	203
3.2.11 PCIe2.0 Interface Circuit PCB Design	204
3.2.12 PCIe3.0 Interface Crcuit PCB Design	206
3.2.13 MIPI CSI RX Interface Circuit PCB Design	207
3.2.14 CIF Interface Circuit PCB Design	208
3.2.15 MIPI DSI TX Interface Circuit PCB Design	208
3.2.16 LVDS TX Interface Circuit PCB Design	209
3.2.17 eDP TX Interface Circuit PCB Design	210
3.2.18 HDMI TX Interface Circuit PCB Design	210
3.2.19 RGB TX Interface Circuit PCB Design	211
3.2.20 BT1120 TX Interface Circuit PCB Design	212
3.2.21 Audio Interface Circuit PCB Design	213
3.2.22 GMAC Interface Circuit PCB Design	214
3.2.23 WIFI/BT PCB Design	218
3.2.24 VGA OUT PCB Design	219
Committee 2022 Deschables Florenzaise Constant	171

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
3.2.25 LCD Screen and Touch Screen PCB Design	
3.2.26 Camera PCB Design	
4 Thermal Design Suggestion	
4.1 Thermal Simulation Result	
4.1.1 Result Overview	
4.1.2 PCB Description	
4.1.3 Terms Interpretation	
4.2 Thermal Control Method inside the Chip	
4.2.1 Thermal Control Strategy	
4.2.2 Temperature Control Configuration	
4.3 Thermal Design Reference	
4.3.1 Circuit Schematic Thermal Design Reference	
4.3.2 PCB Thermal Design Reference	
5 ESD/EMI Protection Design	
5.1 Overview	
5.2 Terms Interpretation	
5.3 ESD Protection	
5.4 EMI Protection	
6 Soldering Process	
6.1 Overview	
6.2 Terms Interpretation	
6.3 Reflow Soldering Requirements	
6.3.1 Solder Paste Composition Requirements	
6.3.2 SMT Profile	
6.3.3 SMT Recommendation Profile	
7 Packages and Storage Conditions	
7.1 Overview	
7.2 Terms Interpretation	
7.3 Moisture Packages	
7.4 Product Storage	
7.4.1 Storage Environment	
7.4.2 Exposure Time	
7.5 Usage of Moisture Sensitive Products	

# Figures

Figure 1-1 RK3568 block diagram	1
Figure 1-2 RK3568 EVB application block diagram	2
Figure 1-3 RK3568 Smart NVR application block diagram	3
Figure 2-1 RK3568 Crystal circuit and components parameters	4
Figure 2-2 RK3568 the 32.768KHz clock input pin in standby	5
Figure 2-3 RK3568 reset input (RK809-5 solution)	6
Figure 2-4 RK3568 reset input (discrete power solution)	7
Figure 2-5 RK3568 the path of reset signal	7
Figure 2-6 RK3568 VCCIO2 power supply and FLASH_VOL_SEL	9
Figure 2-7 RK3568 SDMMC0/ARM JTAG multiplexed pins and SDMMC0 DET pin	9
Figure 2-8 RK3568 JTAG connection schematic	10
Figure 2-9 RK3568 ARM JTAG pin	11
Figure 2-10 RK3568 UART2 M0 pin	11
Figure 2-11 RK3568 Debug UART2 Connection diagram	11
Figure 2-12 RK3568 16bit ECC DDR3/DDR3L processing method	15
Figure 2-13 RK3568 16bit ECC DDR4 processing method	15
Figure 2-14 RK3568 DDR_RZQ pin	16
Figure 2-15 DDR3/DDR3L VREF circuit	16
Figure 2-15 DDR3/DDR3L VREF circuit	17
Figure 2-17 DDR4 VREF circuit	17
Figure 2-18 DDR3/DDR3L T topology	18
Figure 2-19 The CLKP/CLKN termination of DDR3/DDR3L T topology	
Figure 2-20 DDR3/DDR3L Fly-by topology	19
Figure 2-21 DDR4 T topology	19
Figure 2-22 The CLKP/CLKN termination of DDR4 T topology	
Figure 2-23 DDR4 Fly-by topology	20
Figure 2-24 LPDDR3 point-to-point topology	21
Figure 2-25 LPDDR3 CLKP/CLKN termination	21
Figure 2-26 LPDDR4 point-to-point topology	21
Figure 2-27 LPDDR4X point-to-point topology	22
Figure 2-28 RK809-5 BUCK3 parameters regulation	23
Figure 2-29 Power selection of LPDDR4/LPDDR4x compatible design	23
Figure 2-30 DDR3 SDRAM power up sequence	24
Figure 2-31 LPDDR3 SDRAM power up sequence	24
Figure 2-32 DDR4 SDRAM power up sequence	24
Figure 2-33 LPDDR4/4x SDRAM power up sequence	25
Figure 2-34 eMMC_D0 test point	26
Figure 2-35 eMMC connection diagram	26

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Figure 2-36 Connection diagram of eMMC and Nand Flash in compatible design	27
Figure 2-37 eMMC power up and power down sequence	
Figure 2-38 FSPI_CLK test point	29
Figure 2-39 FSPI Flash connection diagram	29
Figure 2-40 Flash_D0 test point	
Figure 2-41 Nand Flash connection diagram	
Figure 2-42 Nand Flash power up and down sequence	
Figure 2-43 RK3568 PMU PLL power pin	40
Figure 2-44 RK3568 SYS PLL power pin	40
Figure 2-45 RK3568 PMU_VDD_LOGIC_0V9 power pin	41
Figure 2-46 RK3568 VDD_CPU power pin and power supply DC/DC	
Figure 2-47 RK3568 VDD_GPU power pin	43
Figure 2-48 RK3568 VDD_NPU power pin	43
Figure 2-49 RK3568 VDD_LOGIC power pin	44
Figure 2-50 RK3568 VCC_DDR power pin in DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 mode	44
Figure 2-51 RK3568 VCC_DDR and VCC0V6_DDR power pins in LPDDR4x mode	45
Figure 2-52 RK3568 USB2.0 PHY power pin	46
Figure 2-53 RK3568 MULTI_PHY power pin	47
Figure 2-54 RK3568 PCIe3.0 PHY power pin	47
Figure 2-55 RK3568 MIPI CSI RX PHY power pin	48
Figure 2-56 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY power pin	49
Figure 2-57 RK3568 MIPI DSI TX1 PHY power pin	50
Figure 2-58 RK3568 eDP TX PHY power pin	50
Figure 2-59 RK3568 HDMI2.0 TX PHY power pin	51
Figure 2-60 RK3568 SARADC and OTP power pin	
Figure 2-61 RK809-5 block diagram	53
Figure 2-62 RK3568 and RK809-5 power tree	55
Figure 2-63 RK809-5 power-on sequence	56
Figure 2-64 RK3568 + discrete power architecture	59
Figure 2-65 Discrete power-on sequence	60
Figure 2-66 RK3568 PMIC_SLEEP output	62
Figure 2-67 RK809-5 PMIC_SLEEP input	62
Figure 2-68 The PMIC_SLEEP input of VDD_CPU BUCK	62
Figure 2-69 RK3568 SDMMC0 interface pin	64
Figure 2-70 SD card interface circuit	65
Figure 2-71 RK3568 SDMMC1 interface pin	66
Figure 2-72 RK3568 SDMMC2 interface M0 functional pins	67
Figure 2-73 RK3568 SDMMC2 interface M1 functional pins	68
Figure 2-74 SARADC VIN0 interface	69
Figure 2-75 RK3568 SARADC module	70
Copyright © 2022 Rockchip Electronics Co., Ltd.	IX

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Figure 2-76 The button circuit using SARADC sampling	70
Figure 2-77 RK3568 OTP power pin	71
Figure 2-78 Multiplexing relationship between MULTI_PHY0/1and USB3.0 controllers	71
Figure 2-79 USB3.0 OTG0 pin	72
Figure 2-80 USB3.0 HOST1 pin	73
Figure 2-81 USB2.0 HOST2 pin	73
Figure 2-82 USB2.0 HOST3 pin	74
Figure 2-83 RK3568 VBUSDET and ID Circuit	75
Figure 2-84 USB2.0 PHY power supply magnetic bead isolation circuit	75
Figure 2-85 USB2.0 signal is connected in series with a 2.20hm resistor	76
Figure 2-86 USB2.0 signal is connected in series with common mode choke circuit	76
Figure 2-87 USB OTG ID pin circuit	76
Figure 2-88 USB 5V current-limiting circuit.	77
Figure 2-89 USB3.0 ESD circuit	77
Figure 2-90 MULTI PHY power supply decoupling circuit	77
Figure 2-91 MULTI_PHY0/1/2 and SATA3.0 controller multiplexing relationship	78
Figure 2-92 SATA0/1/2 related control IO pins	
Figure 2-93 The paths of GMAC0, GMAC1, QSGMII/SGMII PCS and QSGMII/SGMII PHY	
Figure 2-94 The application block diagram of QSGMII-MULTI_PHY1Y1	
Figure 2-95 The application block diagram of QSGMII-MULTI_PHY2	
Figure 2-96 The application block diagram of GMAC0-SGMII-MULTI_PHY1	
Figure 2-97 The application block diagram of GMAC1-SGMII-MULTI_PHY1	
Figure 2-98 The application block diagram of GMAC0-SGMII-MULTI_PHY2	
Figure 2-99 The application block diagram of GMAC1-SGMII-MULTI_PHY2	
Figure 2-100 PCIe3.0 controller/PCIe3.0 PHY block diagram	
Figure 2-101 Reference clock paths in RK3568 PCIe3.0 x2 Lane RC mode	90
Figure 2-102 Reference clock paths in RK3568 PCIe3.0 x2 Lane EP mode	90
Figure 2-103 The reference clock paths in RK3568 PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC n	10de91
Figure 2-104 PCIe3.0 PHY power decoupling capacitors	91
Figure 2-105 PCIe3.0 PHY RESREF pin	91
Figure 2-106 RK3568 MIPI CSI RX signal pins	93
Figure 2-107 RK3568 MIPI CSI working mode and data, clock allocation	94
Figure 2-108 MIPI CSI PHY power circuit isolated with magnetic beads	94
Figure 2-109 MIPI CSI RX PHY power decoupling capacitors	94
Figure 2-110 RK3568 CIF functional pins	95
Figure 2-111 RK3568 Relationship between data of CIF	96
Figure 2-112 RK3568 the output path diagram of VOP and video interface	98
Figure 2-113 RK3568 HDMI2.0 TX PHY TMDS pins	99
Figure 2-114 RK3568 HDMI2.0 TX PHY power supply decoupling capacitances	99
Figure 2-115 RK3568 HDMI2.0 TX PHY REXT pins	99
Copyright © 2022 Rockchip Electronics Co., Ltd.	Х

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Figure 2-116 RK3568 HDMI2.0 TX PHY HPD pins	
Figure 2-117 RK3568 HDMI2.0 TX PHY HPD circuit	100
Figure 2-118 HDMI CEC protocol requirements	100
Figure 2-119 HDMI CEC CEC isolating circuit	100
Figure 2-120 HDMI DDC level conversion circuit	101
Figure 2-121 ESD circuit of HDMI connector	
Figure 2-122 RK3568 MIPI DSI TX0/LVDS TX Combo PHY pins	
Figure 2-123 Magnetic bead isolation circuit of MIPI DSI PHY power supply	
Figure 2-124 RK3568 MIPI DSI TX0/LVDS TX Combo PHY power decoupling capacitors	
Figure 2-125 RK3568 MIPI DSI TX1 PHY pins	104
Figure 2-126 Magnetic bead isolation circuit of MIPI DSI TX1 PHY power supply	
Figure 2-127 RK3568 MIPI DSI TX1 PHY power decoupling capacitors	
Figure 2-128 RK3568 eDP TX PHY pins.	
Figure 2-129 Figure 2–129 RK3568 eDP TX PHY power decoupling capacitors	
Figure 2-130 RK3568 eDP TX signal AC decoupling capacitors	
Figure 2-131 RK3568 eDP AUX signal AC decoupling capacitors	107
Figure 2-132 RK3568 LCDC functional pins.	
Figure 2-133 The decoupling capacitors of RK3568 VCCIO5 power supply	110
Figure 2-134 RK3568 VOP BT1120 functional pins	
Figure 2-135 RK3568 VOP BT656 M0 functional pins	
Figure 2-136 RK3568 VOP BT656 M1 functional pins	114
Figure 2-137 RK3568 EBC functional pins	116
Figure 2-138 The decoupling capacitors of RK3568 VCCIO6 power supply	116
Figure 2-139 Connection diagram of RK3568 I2S in Master mode	120
Figure 2-140 Connection diagram of RK3568 I2S in Slave mode	
Figure 2-141 RK3568 I2S1 M0 functional pins	121
Figure 2-142 RK3568 I2S1 M1 functional pins	121
Figure 2-143 RK3568 I2S1 M2 functional pins	
Figure 2-144 RK3568 I2S2 M0 functional pins	124
Figure 2-145 RK3568 I2S2 M1 functional pins	124
Figure 2-146 RK3568 I2S3 M0 functional pins	
Figure 2-147 RK3568 I2S3 M1 functional pins	
Figure 2-148 RK3568 PDM M0 functional pins	127
Figure 2-149 RK3568 PDM M1 functional pins	
Figure 2-150 RK3568 PDM M2 functional pins	
Figure 2-151 Process mode of related pins when RK809-5 Codec module is not used	130
Figure 2-152 RK809-5 Codec module	131
Figure 2-153 RK809 Codec output earphone circuit	132
Figure 2-154 RK809-5 SPK/HP power supply pins	
Figure 2-155 RK809-5 SPK output circuit	132
Copyright © 2022 Rockchip Electronics Co., Ltd.	XI

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Figure 2-156 External SPK circuit	
Figure 2-157 Electret MIC differential input circuit	
Figure 2-158 Four-segment headset with MIC single-ended input circuit	134
Figure 2-159 Electret MIC single-ended input circuit	134
Figure 2-160 RK809-5 MIC input circuit pins	134
Figure 2-161 Array MIC solution I2S/PDM connection diagram 1	
Figure 2-162 Array MIC solution I2S/PDM connection diagram 2	136
Figure 2-163 Path block diagram of RK3568 GMAC0, GMAC1 reused with IO	137
Figure 2-164 RK3568 GMAC0 functional pins	137
Figure 2-165 RK3568 GMAC1 M0 functional pins	138
Figure 2-166 RK3568 GMAC1 M1 functional pins	
Figure 2-167 RGMII connection example 1	
Figure 2-168 RGMII connection example 2	141
Figure 2-169 RMII connection example 1	141
Figure 2-170 RMII connection example 2	142
Figure 2-171 RMII connection example 3	142
Figure 2-172 RMII connection example 4	
Figure 2-173 RMII connection example 5	143
Figure 2-174 IR receiver circuit	
Figure 3-1 Six layers PCB design	
Figure 3-2 Four layers PCB design	152
Figure 3-3 RK3568 Fan-out diagram 1	
Figure 3-4 RK3568 Fan-out diagram 2	
Figure 3-5 RK3568 Fan-out diagram 3	154
Figure 3-6 RK3568 Fan-out diagram 4	155
Figure 3-7 A diagram of space between signals	155
Figure 3-8 A diagram of equal length within and between differential pairs	156
Figure 3-9 A diagram of differential pair length compensation requirements	
Figure 3-10 Stitching vias requirement diagram	156
Figure 3-11 Edge requirement of signal reference plane diagram	157
Figure 3-12 RK3568 Crystal layout and routing	157
Figure 3-13 RK809-5 BUCK1/BUCK2 Layout and routing	159
Figure 3-14 RK809-5 BUCK3 Layout and routing	159
Figure 3-15 RK809-5 BUCK4 Layout and routing	160
Figure 3-16 RK809-5 BUCK5 Layout and routing	161
Figure 3-17 RK809-5 EPAD vias layout	162
Figure 3-18 Discrete power supply DC/DC layout and routing	162
Figure 3-19 VDD_CPU Power supply DC/DC layout and tracing	
Figure 3-20 A diagram of DC/DC remote feedback design	164
Figure 3-21 RK3568 VDD_CPU Power pin routing and vias	165
Copyright © 2022 Rockchip Electronics Co., Ltd.	XII

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Figure 3-22 Placement of decoupling capacitors on the back of RK3568 VDD_CPU power pins	
Figure 3-23 Copper-covering on RK3568 VDD_CPU power layer	
Figure 3-24 RK3568 VDD_LOGIC power supply pin routing and vias	167
Figure 3-25 Placement of decoupling capacitors on the back of RK3568 VDD_LOGIC power pins	167
Figure 3-26 Copper-covering on RK3568 VDD_LOGIC power layer	
Figure 3-27 RK3568 VDD_GPU Power pin traces and vias	
Figure 3-28 Placement of decoupling capacitors on the back of RK3568 VDD_GPU power pins	
Figure 3-29 Copper covering on RK3568 VDD_GPU power layer	170
Figure 3-30 RK3568 VDD_NPU Power pin routing and vias	171
Figure 3-31 Placement of decoupling capacitors on the back of VDD_NPU power	171
Figure 3-32 Copper covering on RK3568 VDD_NPU power layer	172
Figure 3-33 RK3568 VCC_DDR power pin routing and vias	173
Figure 3-34 RK3568 VCC_DDR/VCC0V6_DDR Power pin routing and vias in LPDDR4x mode	
Figure 3-35 Placement of decoupling capacitor on the back of the power supply pin of RK3568 VCC_D	DR174
Figure 3-36 Placement of decoupling capacitors on the back of the power supply	pins of
VCC_DDR/VCC0V6_DDR of RK3568 in LPDDR4x mode	174
Figure 3-37 Copper covering on RK3568 VCC_DDR power layer	175
Figure 3-38 RK3568 VSS pin routing and vias	176
Figure 3-39 Ground copper-covering of RK3568	
Figure 3-40 DDR3/DDR3L DQS/DQ/DM signal routing topology	178
Figure 3-41 DDR3/DDR3L CLK signal routing topology	179
Figure 3-42 DDR3/DDR3L CLK signal RC circuit	179
Figure 3-43 DDR3/DDR3L CSn/CKE/ODT signal routing topology	
Figure 3-44 Other CA/CMD signal of DDR3/DDR3L routing topology except CSn/CKE/ODT	
Figure 3-45 DDR3/DDR3L+ECC DQS/DQ/DM signal routing topology	
Figure 3-46 DDR3/DDR3L+ECC CLK signal routing topology	
Figure 3-47 DDR3/DDR3L+ECC CSn/CKE/ODT signal routing topology	
Figure 3-48 DDR3/DDR3L+ECC other CA/CMD signal routing topology except CSn/CKE/ODT	
Figure 3-49 DDR4 DQS/DQ/DM signal routing topology	
Figure 3-50 DDR4 CLK signal routing topology	
Figure 3-51 RC circuit for DDR4 CLK signal	
Figure 3-52 CLK/CA/CMD signal routing diagram on the L3 plane of DDR4 4-layer board	
Figure 3-53 DDR4 CSn/CKE/ODT signal routing topology	
Figure 3-54 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4	
Figure 3-55 DDR4+ECC DQS/DQ/DM signal routing topology	
Figure 3-56 DDR4+ECC CLK signal routing topology	
Figure 3-57 DDR4+ECC CSn/CKE/ODT signal routing topology	191
Figure 3-58 DDR4+ECC other CA/CMD signal routing topology except CSn/CKE/ODT	
Figure 3-59 Branch resistances of eMMC and Nand Flash compatible design	197
Figure 3-60 Branch resistor layout and routing of eMMC and NAND flash compatible design	
Copyright © 2022 Rockchip Electronics Co., Ltd.	XIII

RK3568 Hardware Design GuideR	ev V1.2
Figure 3-61 Figure 3–61 DATA routing of eMMC and Nand Flash compatible design	198
Figure 3-62 Schematic diagram of empty space below the pad of USB3 connector and the pad of AC	coupling
capacitor	202
Figure 3-63 PCB fiberweave effect to improve routing way	202
Figure 3-64 Schematic diagram of empty space below the pad of SATA connector and the pad of AC	coupling
capacitor	203
Figure 3-65 Schematic diagram of empty space below the pad of PCIe Slot and the pad of AC coupling of	capacitor
	205
Figure 3-66 Schematic diagram of empty space below the pad of HDMI connector and the pad of TVS dic	ode.211
Figure 3-67 RK809-5 HP_SNS resistor layout and routing	213
Figure 3-68 RK809-5 HPL/HPR/HP_SNS routing	213
Figure 3-69 Schematic diagram of prohibited routing area for RJ45 interface and network transformer	217
Figure 3-70 Schematic diagram of RJ45 interface and network transformer slotting	217
Figure 3-71 Schematic diagram of inductance and capacitance of the WIFI module routing	218
Figure 3-72 Schematic diagram of WIFI module antenna routing	219
Figure 4-1 $\theta_{JA}$ definition	222
Figure 4-2 $\theta_{JC}$ definition	222
Figure 4-3 $\theta_{JB}$ definition	
Figure 6-1 Reflow soldering profile classification	230
Figure 6-2 Heat resistance of lead-free process device packages standard	230
Figure 6-3 Lead-free reflow profile	230
Figure 6-4 Lead-free reflow soldering process recommended profile parameters	231
Figure 7-1 Chipset dry vacuum package	233
Figure 7-2 Six-point humidity card	233
Figure 7-1 Chipset dry vacuum package Figure 7-2 Six-point humidity card	

## **Tables**

Table 2–1 RK3568 24MHz clock requirements	4
Table 2–2 RK3568 32.768KHz clock requirements	5
Table 2–3 RK3568 System initialization configuration signal description	10
Table 2–4 RK3568 JTAG debug interface signal	
Table 2–5 RK3568 DDR PHY I/O map	12
Table 2–6 RK3568 eMMC interface design	26
Table 2–7 RK3568 FSPI interface design	29
Table 2–8 RK3568 Nand Flash interface design	31
Table 2–9 RK3568 GPIO power pins description	33
Table 2–10 RK3568 power supply requirements	
Table 2–11 RK3568 power supply requirement of each module for the first powered on	37
Table 2–12 RK3568 standby power supply requirements	
Table 2–13 RK3568 internal PLL Introduction      Table 2–14 RK3568 peak current table	
Table 2–14 RK3568 peak current table	63
Table 2–15 SDMMC0 interface design	65
Table 2–16 SDMMC1 interface design	66
Table 2–17 SDMMC2 interface design	68
Table 2–18 RK3568 USB2.0/USB3.0 interface design	78
Table 2–19 RK3568 SATA interface design	81
Table 2–20 RK3568 QSGMII/SGMII interface design	87
Table 2–21 RK3568 PCIe2.0 interface design.	89
Table 2–22 RK3568 PCIe3.0 interface design	92
Table 2–23 RK3568 MIPI CSI RX interface design.	94
Table 2–24 RK3568 Data relationship in BT1120 16bit mode	96
Table 2–25 RK3568 CIF interface design	97
Table 2–26 RK3568 HDMI2.0 TX interface design	102
Table 2–27 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY interfaces design	104
Table 2–28 RK3568 MIPI DSI TX1 PHY interface design	105
Table 2–29 RK3568 eDP TX PHY interface design	107
Table 2–30 RK3568 parallel RGB interface formats	108
Table 2–31 RK3568 parallel RGB interface design	110
Table 2–32 RK3568 BT1120 output formats	
Table 2–33 RK3568 BT1120 output interface design.	112
Table 2–34 RK3568 BT656 output interface design	115
Table 2–35 RK3568 EBC output interface design	117
Table 2–36 RK3568 I2S1 interface design	
Table 2–37 RK3568 I2S2 interface design	125
Table 2–38 RK3568 I2S3 interface design	127

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Table 2–39 RK3568 PDM interface design	129
Table 2-40 RK3568 SPDIF interface design	130
Table 2-41 RK3568 matching relationship between audio applications and the circuit diagram	135
Table 2–42 RK3568 RGMII/RMII interface design	139
Table 2–43 RK3568 UART interface distribution	145
Table 2-44 RK3568 UART interface design	145
Table 2–45 RK3568 SPI interface distribution	146
Table 2–46 RK3568 SPI interface design	146
Table 2–47 RK3568 CAN interface distribution	147
Table 2–48 RK3568 CAN interface design	147
Table 2–49 RK3568 I2C interface distribution	148
Table 2–50 RK3568 I2C interface design	148
Table 2–51 RK3568 PWM interface distribution	149
Table 3-1 DDR3/DDR3L DQS/DQ/DM signal impedance and routing requirements	179
Table 3-2 DDR3/DDR3L CLK signal impedance and routing requirements	
Table 3-3 DDR3/DDR3L CSn/CKE/ODT signal impedance and routing requirements	
Table 3-4 Other CA/CMD signal of DDR3/DDR3L routing topology except CSn/CKE/ODT	
Table 3-5 DDR3/DDR3L+ECC DQS/DQ/DM signal impedance and routing requirements	
Table 3-6 DDR3/DDR3L+ECC CLK signal impedance and routing requirements	
Table 3-7 DDR3/DDR3L+ECC CSn/CKE/ODT signal impedance and routing requirements	
Table 3-8 DDR3/DDR3L+ECC other CA/CMD signal impedance and routing requirement	ts except
CSn/CKE/ODT	184
Table 3-9 LPDDR3 signal impedance and routing requirements	184
Table 3-10 DDR4 DQS/DQ/DM signal impedance and routing requirements	
Table 3-11 DDR4 CLK signal impedance and routing requirements	187
Table 3-12 DDR4 CSn/CKE/ODT signal impedance and routing requirements	
Table 3–13 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4	
Table 3-14 DDR4+ECC DQS/DQ/DM signal impedance and routing requirements	190
Table 3–15 DDR4+ECC CLK signal impedance and routing requirements	191
Table 3-16 DDR4+ECC CSn/CKE/ODT signal impedance and routing requirements	191
Table 3-17 DDR4+ECC other CA/CMD signal impedance and routing requirements except CSn/CKE/C	DDT192
Table 3–18 LPDDR4 signal impedance and routing requirements	192
Table 3–19 LPDDR4 signal impedance and routing requirements	193
Table 3-20 eMMC signal impedance and routing requirements	194
Table 3-21 FSPI signal impedance and routing requirements	195
Table 3-22 Nand Flash signal impedance and routing requirements	196
Table 3–23 SDMMC0/1/2 signal impedance and routing requirements	199
Table 3-24 USB2.0 signal impedance and routing requirements	
Table 3-25 USB3.0 signal impedance and routing requirements	201
Table 3–26 SATA3.0 signal impedance and routing requirements	
Copyright © 2022 Rockchip Electronics Co., Ltd.	XVI

RK3568 Hardware Design Guide	<i>Rev V1.2</i>
Table 3-27 QSGMII/SGMII signal impedance and routing requirements	
Table 3–28 PCIe2.0 signal impedance and routing requirements	
Table 3–29 PCIe3.0 signal impedance and routing requirements	
Table 3–30 MIPI CSI RX signal impedance and routing requirements	207
Table 3–31 CIF signal impedance and routing requirements	
Table 3–32 MIPI DSI TX signal impedance and routing requirements	
Table 3–33 LVDS TX signal impedance and routing requirements	
Table 3–34 eDP TX signal impedance and routing requirements	210
Table 3–35 HDMI TX signal impedance and routing requirements	210
Table 3–36 RGB TX signal impedance and routing requirements	
Table 3–37 BT1120 TX signal impedance and routing requirements	
Table 3–38 RGMII signal impedance and routing requirements	214
Table 3–39 RMII signal impedance and routing requirements	
Table 4–1 RK3568 thermal resistance simulation report results	
Table 4–2 RK3568 PCB structure used for thermal resistance simulation	
Table 7–1 Moisture Sensitivity Levels (MSL)	234
Table 7–2 RV11XX chipset Re-bake reference table	234
COR	
e ching	

#### **1** System Introduction

#### 1.1 Overview

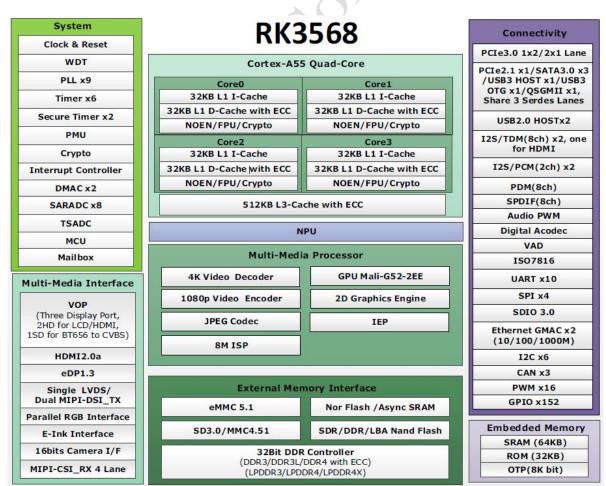
RK3568 is a low-power and high-performance processor designed for personal mobile Internet devices and AIoT devices.

RK3568 provides many powerful embedded hardware engines to optimize the performance of advanced applications. RK3568 supports almost all formats of H.264 4k@60fps decoding, and supports H.265 4k@60fps decoding, H.264/H.265 1080p@60fps encoding, and high-quality JPEG encoding/decoding.

RK3568 embedded 3D GPU is fully compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1; the special 2D hardware engine maximizes the display performance and provides a smooth operating experience also.

The built-in NPU supports INT8/INT16 mixed operation. Due to strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

There are high-performance external memory interfaces in RK3568 to ensure high-capacity and high-stability system operating memory bandwidth, and it supports multiple memory models such as DDR3, DDR3L, LPDDR3, DDR4, LPDDR4, LPDDR4X, etc.



#### **1.2 Block Diagram**

Figure 1-1 RK3568 block diagram

#### **1.3 Application Block Diagram**

#### 1.3.1 RK3568 EVB Application Block Diagram

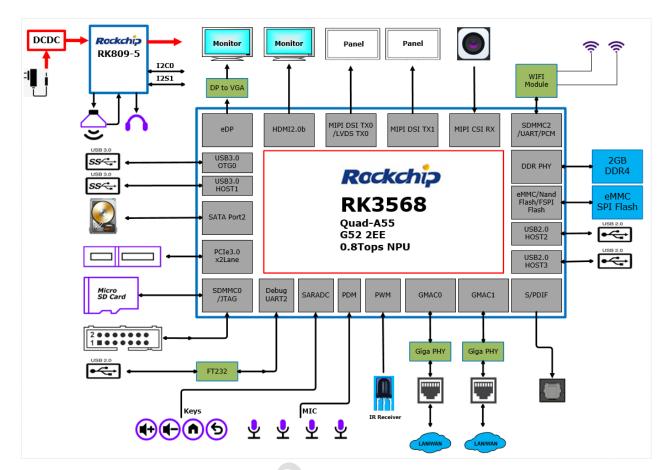


Figure 1-2 RK3568 EVB application block diagram

Rockey

1.3.2 RK3568 Smart NVR Application Block Diagram

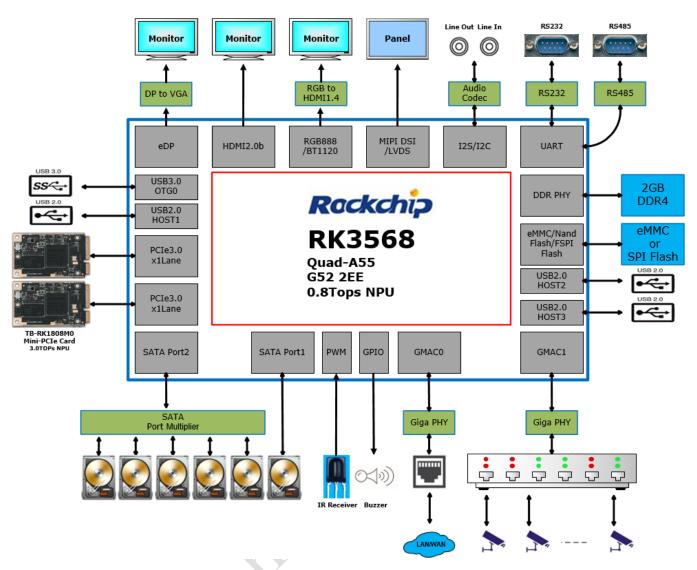


Figure 1-3 RK3568 Smart NVR application block diagram

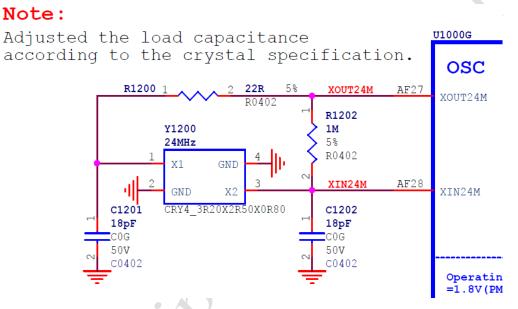
The figures above are example application block diagrams of RK3568, please refer to the reference design schematic released by RK for more details.

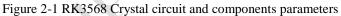
#### 2 Schematic Design Recommendation

#### 2.1 Minimum System Design

#### 2.1.1 Clock Circuit

- The oscillator circuit inside RK3568 and the external 24MHz crystal form the system clock, as shown in Figure 2-1.
- The 220hm resistor connected to the XOUT24M network in series must be added to limit current and prevent overdrive.
- The 1M ohm resistor between XOUT24M and XIN24M network cannot be modified at will.







The load capacitances of crystal should be selected according to the CL capacitance value of the crystal actually used, and the frequency tolerance at room temperature should be controlled within 20ppm.

18pF is the capacitance value of the crystal selected by RK, not a general value, and COG or NPO material are recommended. It is recommended to use 4Pin SMT crystal, with 2 GND pins fully connected with the ground of the PCB to enhance ESD anti-interference ability

• The system clock can also be directly generated by an external active crystal circuit with a clock amplitude of 1.8V. When working, the clock is input through the XIN24M pin, and the XOUT24M pin can be floated. The clock parameters are shown in the following Table 2-1:

	14010 2	1100550021011	2 elock requireme	21105
Parameters		Spec	Description	
rarameters	Min.	Max.	Unit	Description
Frequency	2	4.000000	MHz	
Frequency tolerance		+/-20	ppm	
Clock amplitude		1.8	V	Peak-to-peak
Operating temperature	-20	80	°C	
ESR	/	40	Ohm	

Table 2-1 RK3568 24MHz clock requirements

- When RK3568 is in standby, you can choose to switch the working clock source to the clock provided by the PMU\_PVTM module or an external 32.768KHz clock. Turn off the OSC oscillator circuit to get better standby power consumption. At this time, only the IO interrupt in the PMUIO1 and PMUIO2 power domain are supported to wake up. If the required wake-up source is related to the 24MHz clock, the 24MHz clock cannot be turned off.
- The clock oscillation loop integrated in PVTM (Process-Voltage-Temperature Monitor) module can generate a clock, its frequency is determined by the delay unit of the clock oscillation loop circuit. The generated clock can be used as a clock source for the chip in standby; the external clock 32.768KHz will reach optimal chip standby power consumption when RK3568 chip in sleeps, and the PVTM module can also be turned off at this time.
- The external 32.768KHz clock can be obtained from PMIC or external RTC clock source. The 32.768KHz clock input pin of RK3568 is shown in the figure below:

CLK32K_IN	/ CLK32K_OUT0	/ PCIE30X2_BUTTONRSTn	/	GPIO0 B0 u	AD23
	Figure 2-2 RI	K3568 the 32.768KHz clock input pin in standby			

• The external 32.768kHz RTC clock parameters are shown in Table 2-2 below

Parameters		Spec	- Description		
rarameters	Min.	Max.	Unit	Description	
Frequency	32.76	58000	kHz		
Frequency	+/	-30	nnm		
tolerance	17.	-30	ppm		
Clock amplitude	0.65*VDD	VDD+0.3V	V	VDD:PMUIO2 voltage	
Operating	-20	80	°C		
temperature	-20	80	C		
Duty Ratio	5	0	%		

#### Table 2–2 RK3568 32.768KHz clock requirements

# Note

When using this function, the IOMUX pin must be set to CLK32K\_IN function, and the input amplitude must meet the power supply requirements of PMUIO2 Domain.

- RK3568 can provide working clocks to peripherals:
  - REFCLK\_OUT: 24MHz clock output as default, which can be provided to Camera and other devices as working clock
  - CLK32K\_OUT0: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock
  - CLK32K\_OUT1: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock

- ETH0\_REFCLKO\_25M: 25MHz clock output, which can be provided to Ethernet PHY and other devices as working clock
- ETH1\_REFCLKO\_25M\_M0/ETH1\_REFCLKO\_25M\_M1: 25MHz clock output, which can be provided to Ethernet PHY and other devices as working clock
- CIF\_CLKOUT: 24MHz clock output by default, other frequency value can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock
- CAM\_CLKOUT0: 24MHz clock output by default, other frequency points can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock
- CAM\_CLKOUT1: 24MHz clock output by default, other frequency value can be obtained according to PLL frequency division, which can be provided to Camera and other devices as working clock



The IO Domains where the above clocks are located must match the IO level of connected peripherals. If they do not match, a level conversion circuit must be added.

Please evaluate whether they can meet the clock requirements of the peripheral device.

#### 2.1.2 Reset/watchdog/TSADC Circuit

The hardware reset signal of RK3568 is input through Pin AH27 (NPOR\_u), which must be controlled externally and is active at low level. In order to ensure the stability and normal operation of the chip, the minimum reset time required is 100 cycles of the 24MHz main clock, that is, at least 4us or more.

Pin AH27 (NPOR\_u) has to add a 100nF capacitor to eliminate jitter of the reset signal, enhance anti-interference ability, and prevent abnormal system reset caused by false triggering.

The pull-up power of the RESETn network must be consistent with the IO domain (PMUIO1) where the nPOR pin is located.

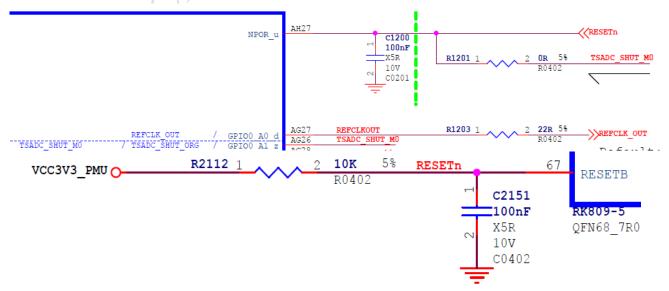


Figure 2-3 RK3568 reset input (RK809-5 solution)

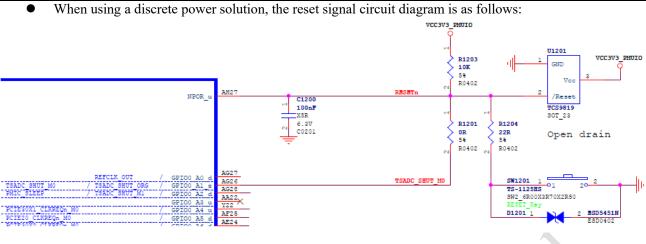


Figure 2-4 RK3568 reset input (discrete power solution)

Note: The reset IC must be with open-drain output, and low level active.

- The RK3568 chip integrates a Watchdog Timer. When a reset signal is generated, a low level will be output through TSADC\_SHUT\_M0 or TSADC\_SHUT\_M1 pin, and then resets RK3568 by hardware.
- The RK3568 chip integrates two TSADC (Temperature-Sensor ADC) modules. When the temperature inside the chip exceeds the threshold, the internal TSHUT signal can be passed to the CRU module and reset RK3568 chip, or it can output low level through TSADC\_SHUT\_M0 or TSADC\_SHUT\_M1 pin to reset RK3568 by hardware. As shown in the figure above, the TSADC\_SHUT\_M0 network is connected to the RESETn network.
- RK3568 reset signal path diagram is as follows:

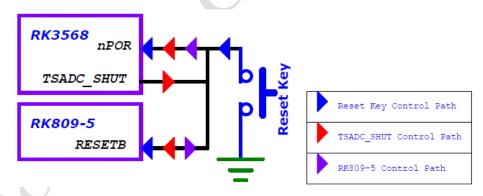


Figure 2-5 RK3568 the path of reset signal

• When the RESETB pin of RK809-5 is powered on for the first time, after all power supplies are powered on, RESETB will change from low level to high level (open drain output) after delaying the set time, to complete the power-on reset process; when RK809-5 is in working or sleep mode, if the RESETB pin is pulled low, RK809-5 will also be restarted. The restart power-on sequence is the same as the first time power-on.

#### 2.1.3 PMU Circuit

In order to meet the requirement of low power consumption products, RK3568 has designed a power management unit (PMU) to control and manage the internal power supply of the chip.

This module supports registers inside chip or PMUIO power domain IO control peripheral power circuit, *Copyright* © 2022 *Rockchip Electronics Co., Ltd.* 

#### **RK3568 Hardware Design Guide**

realize power on and power off to other functional modules, and also support IO interrupt wake-up, so as to realize the chip's standby and wake-up functions.

#### 2.1.4 System Boot Sequence

The RK3568 chip supports multiple booting ways. After chip reset, the boot code integrated inside the chip will automatically boot in the following sequence:

- Serial Nor Flash (FSPI)
- Serial Nand Flash (FSPI)
- Nand Flash
- eMMC
- SDMMC0 Card

If there is no boot code in the above devices, you can download the system code to these devices through the USB3\_OTG0\_DP/USB3\_OTG0\_DM signal of the USB3.0 OTG0 interface.

#### 2.1.5 System Initialization Configuration Signal

There are two important signals in RK3568 will affect the system boot configuration, which need to be configured and kept stable before power-on. They are:

- FLASH\_VOL\_SEL pin (Pin AG25): hardware configuration VCCIO2 power domain IO driver voltage
- SDMMC0\_DET pin (Pin Y22): determine whether VCCIO3 power domain IO is SDMMC0 or JTAG function

After the system reset, the chip will configure the default power-on function of the corresponding module according to the input level of the two pins

- The IO drive voltage mode of RK3568 VCCIO2 power domain is configured by hardware by default. Because it belongs to FLASH power domain, it's used during system boots. Therefore, when the system is booting, the IO drive voltage mode must be set through the hardware configuration first instead of setting by register operation, as shown below:
  - When VCCIO2 voltage is connected to 1.8V, FLASH\_VOL\_SEL must be high;
  - When VCCIO2 voltage is connected to 3.3V, FLASH\_VOL\_SEL must be low;
  - If the IO power supply is changed, the FLASH\_VOL\_SEL pin must be changed synchronously, they cannot be mismatch, otherwise the function will be abnormal or the chip may even be damaged.

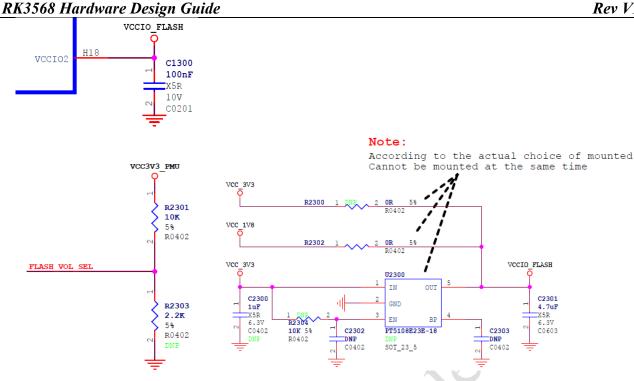


Figure 2-6 RK3568 VCIO2 power supply and FLASH\_VOL\_SEL

The ARM JTAG function of RK3568 is reused with the SDMMC0 function, and the IOMUX function is switched through the SDMMC0 DET pin. Therefore, you have to finish configuration operate of this pin before power-on, otherwise the ARM JTAG function has no output that will affect the debugging during booting, no output from SDMMC0 will affect the boot function of SDMMC0.

pera	ting	g	NOT.	tage	=1	•8V,	/3	.3V									705
SDMMC0		/		_TX_M1	7	UART6		_		PWM8	_		/	GPI01	D5	u	J25 J24
SDMMC0		/		_RX_M1	/	UART6				PWM9	_M1		/	GPI01			H26
SDMMC0		14	ARMJT		/	UART5							/	GPI01			J23
SDMMC0	_D3	/	ARMJT	AG_TMS	/	UART5	_RTS	Sn_MO					/	GPIO2	A0	u	
SDMMC0	_CMD	/	PWM10	_M1	/	UART5	RX	M0	/	CAN0	TX	<u>M1</u>	/	GPIO2	A1	u	H27
SDMMC0	CLK	/	TEST	CLKOUT	/	UART5	ΤX	M0	/	CAN0	RX	M1	/	GPIO2	A2	d	H28
																	L22
														V	CCI	03	

Figure 2-7 RK3568 SDMMC0/ARM JTAG multiplexed pins and SDMMC0 DET pin

If this pin is detected as high level, the corresponding IO will be switched to ARM JTAG function;

When it is detected as low level (If there is no special requirement, most SD card insertion will pull down this

pin), the corresponding IO is switched to the SDMMC0 function.

After the system is up, it can be switched to register to control IOMUX, then the pin can be released.

In order to query easily, the configuration status and function of the two pins are shown as follows:

Signal name	Internal up and down	Description
FLASH_VOL_SEL	Pull up	IO drive voltage mode of FLASH VCCIO2 power domain: 0: IO level mode is 3.3V; 1: IO level mode is 1.8V
SDMMC0_DET	Pull up	SDMMC0/ARM JATG pin multiplexing selection control signal: 0: Recognized as SD card insertion, SDMMC0/ARM JATG pins are multiplexed as SDMMC0 function; 1: Not recognized as SD card insertion, SDMMC0/ARM JATG pins are multiplexed as ARM JTAG function (Default)

Table 2-3 RK3568 System initialization configuration signal description

#### 2.1.6 JTAG and UART Debug Circuit

The ARM JTAG interface of RK3568 conforms to the IEEE1149.1 standard. The PC can be connected to the DSTREAM emulator through SWD mode (two-wire mode) to debug ARM Core inside the chip.

When connecting to emulator during booting, you need to ensure that the SDMMC0\_DET pin is at a high level, otherwise the JTAG debugging mode cannot be entered. The management configuration is described in the previous sections.

After the system is up, it will switch to control IOMUX by register. The ARM JTAG interface introduction is shown in the following Table:

Table 2-4 RK3568 JTAG debug interface signal

Signal name	Description
ARM_JTAG_TCK	Clock input in SWD mode
ARM_JTAG_TMS	Data input and output in SWD mode

The connection way of JTAG and the definition of standard connector pins are shown in the figure below:

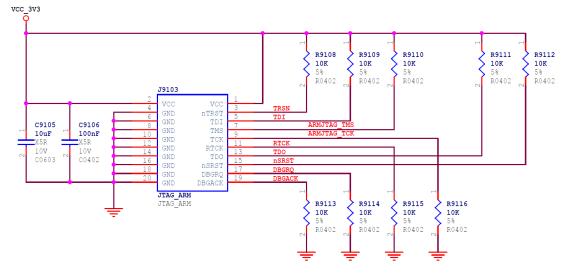


Figure 2-8 RK3568 JTAG connection schematic

• If there is no SD Card function, it is recommended to reserve the ARM JTAG function to facilitate debug. The reserved circuit is as shown in the figure below:

Note that the VCCIO3 power supply must be powered, and the power supply voltage could be VCCIO\_SD or VCC 3V3

#### U1000J VCCIO3 Domain Operating Voltage=1.8V/3.3V RMJTAG TCK QTP1304 TP1305 R1302 R0402 22R R0402 TP 0.7 For ARM JTAG 1F23 SDMMC0\_CMD / PWM10\_M1 / UART5\_RX\_M0 / CANO TX M1 GPIO2 A1 <u>K40</u> × / CAN0\_RX\_M1 SDMMC0\_CLK / TEST\_CLKOUT / UART5\_TX\_M0 / GPIO2 A2 VCCIO SD 1G19 VCCI03 c1301 100nF X5R BGA698\_65Rx65Rx45R\_S 10V C0201

Figure 2-9 RK3568 ARM JTAG pin

- The MCU\_JTAG module of RK3568 is temporarily not released, no special processing is required.
- The UART2\_RX\_M0/UART2\_TX\_M0 is used for RK3568 UART Debug by default, with default baud rate 1500000M.

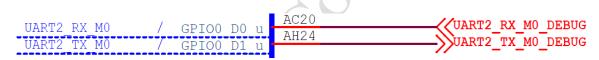


Figure 2-10 RK3568 UART2 M0 pin

The 100ohm resistor connected in series with UART2\_RX\_M0/UART2\_TX\_M0 shall not be deleted, and TVS tube shall be added to strengthen the anti-static surge capability and prevent the chip pins from being damaged during the development process. It is recommended to reserve 2.54 pins as much as possible. If conditions are not allowed, it is recommended to use test points above 0.7mm or larger to facilitate soldering.

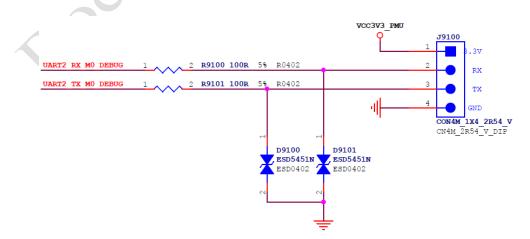


Figure 2-11 RK3568 Debug UART2 Connection diagram

#### 2.1.7.1 DDR Controller Introduction

The RK3568 DDR controller interface supports JEDEC SDRAM standard interface with following features:

- Support DDR3/DDR3L/LPDDR3/DDR4/LPDDR4X, etc.
- Support 32-bits data bus width, 2 ranks (chip selects), totally 8GB (max) address;
- Support Power Down, Self-Refresh and other modes;
- Compensate the PCB delay through software;
- For DDR3/DDR3L/DDR4, support 8 bits ECC;
- Programmable output and ODT impedance with dynamic PVT compensation.

#### 2.1.7.2 Circuit Design Suggestion

The schematic of RK3568 DDR PHY and each DRAM need to be consistent with the reference design diagram, including power supply decoupling capacitors.

RK3568 supports DDR3/DDR3L, LPDDR3, DDR4 or LPDDR4/LPDDR4X. These DRAM have different I/O signals. Choose the signal according to the DRAM type. The RK3568 DDR PHY I/O Map is as follows:

	DDR4	-5 RK3568 DDR PHY D LPDDR4/LPDDR4x	DDR3	LPDDR3
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_D15
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_D14
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_D10
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_D9
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_D13
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_D12
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_D8
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_D11
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_D25
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_D24
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_D28
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_D29
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_D26
DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_D31
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_D30
DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_D27
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_D1
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_D5
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_D6
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_D4
DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_D2

Table 2-5 RK3568 DDR PHY I/O map

#### **RK3568 Hardware Design Guide**

K3568 Hardware	Design Guide			<i>Rev V1.2</i>
	DDR4	LPDDR4/LPDDR4x	DDR3	LPDDR3
DDR DQ5 B	DDR4 DQU6 B	LPDDR4 DQ5 B	DDR3 DQ21	LPDDR3 D3
DDR DQ6 B	DDR4 DQU4 B	LPDDR4 DQ6 B	DDR3 DQ22	LPDDR3 D7
DDR DQ7 B	DDR4 DQU2 B	LPDDR4 DQ7 B	DDR3 DQ23	LPDDR3 D0
DDR DM0 B	DDR4 DMU B	LPDDR4 DM0 B	DDR3 DM2	LPDDR3 DM0
DDR DQS0P B	DDR4 DQSU P B	LPDDR4 DQS0P B	DDR3 DQS2P	LPDDR3 DQS0P
DDR DQS0N B	DDR4 DQSU N B	LPDDR4 DQS0N B	DDR3 DQS2N	LPDDR3 DQS0N
DDR DQ8 B	DDR4 DQL0 B	LPDDR4 DQ8 B	DDR3 DQ24	LPDDR3 D18
DDR DQ9 B	DDR4 DQL2 B	LPDDR4 DQ9 B	DDR3 DQ25	LPDDR3 D19
DDR DQ10 B	DDR4 DQL4 B	LPDDR4 DQ10 B	DDR3 DQ26	LPDDR3 D22
DDR DQ11 B	DDR4 DQL6 B	LPDDR4 DQ11 B	DDR3 DQ27	LPDDR3_D23
DDR DQ12 B	DDR4 DQL7 B	LPDDR4 DQ12 B	DDR3 DQ28	LPDDR3 D16
DDR DQ13 B	DDR4 DQL5 B	LPDDR4 DQ13 B	DDR3 DQ29	LPDDR3 D17
DDR DQ14 B	DDR4 DQL1 B	LPDDR4 DQ14 B	DDR3 DQ30	LPDDR3 D20
DDR DQ15 B	DDR4 DQL3 B	LPDDR4 DQ15 B	DDR3 DQ31	LPDDR3 D21
DDR DM1 B	DDR4 DML B	LPDDR4 DM1 B	DDR3 DM3	LPDDR3 DM2
DDR DQS1P B	DDR4 DQSL P B	LPDDR4 DQS1P B	DDR3 DQS3P	LPDDR3 DQS2P
DDR DQS1N B	DDR4 DQSL N B	LPDDR4 DQS1N B	DDR3 DQS3N	LPDDR3 DQS2N
DDR ECC DQ0	DDR4 ECC DQ7	-	DDR3 ECC DQ0	-
DDR ECC DQ1	DDR4 ECC DQ0	-	DDR3 ECC DQ1	-
DDR ECC DQ2	DDR4 ECC DQ2	-	DDR3 ECC DQ2	-
DDR ECC DQ3	DDR4 ECC DQ1	-	DDR3 ECC DQ3	-
DDR ECC DQ4	DDR4 ECC DQ6	-	DDR3 ECC DQ4	-
DDR ECC DQ5	DDR4 ECC DQ4	-	DDR3 ECC DQ5	-
DDR ECC DQ6	DDR4 ECC DQ3	-	DDR3 ECC DQ6	-
DDR ECC DQ7	DDR4 ECC DQ5	-	DDR3 ECC DQ7	-
DDR ECC DM	DDR4 ECC DM	-	DDR3 ECC DM	-
DDR ECC DQSP	DDR4 ECC DQSP	-	DDR3 ECC DQSP	-
DDR ECC DQSN	DDR4 ECC DQSN	-	DDR3 ECC DQSN	-
AC0	DDR4 A0	LPDDR4 CLKP B	DDR3 A9	-
AC1	DDR4 A1	-	DDR3 A2	-
AC2	DDR4 A2	LPDDR4 A1 A	DDR3 A4	LPDDR3 A6
AC3	DDR4 A3	LPDDR4 CKE1 A	DDR3 A3	-
AC4	DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3
AC5	DDR4 A5	LPDDR4 A5 B	DDR3 A11	LPDDR3 A2
AC6	DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1
AC7	DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	-
AC8	DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9
AC9	DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	-
AC10	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	-
AC11	DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8
AC12	DDR4_A12	LPDDR4_A3_A	DDR3_BA2	-
AC13	DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0
AC14	DDR4_A14_WEN	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5
AC15	DDR4_A15_CASN	LPDDR4_A2_A	DDR3_A0	-
AC16	DDR4_A16_RASN	LPDDR4_A5_A	DDR3_RASN	LPDDR3_A7
AC17	DDR4_ACTN	LPDDR4_CKE1_B	DDR3_CASN	-
AC18	DDR4_BA0	LPDDR4_A2_B	DDR3_A1	-
AC19	DDR4 BA1	LPDDR4 A4 B	DDR3 A12	LPDDR3 A4

Copyright © 2022 Rockchip Electronics Co., Ltd.

#### **RK3568 Hardware Design Guide**

Rev I	V <b>1.2</b>
-------	--------------

	DDR4	LPDDR4/LPDDR4x	DDR3	LPDDR3
AC20	DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEN	-
AC21	DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	-
AC22	DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE
AC23	DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP
AC24	DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN
AC25	DDR4_CS0N	LPDDR4_CS0N_A	DDR3_ODT1	LPDDR3_ODT0
AC26	DDR4_CS1N	LPDDR4_CS1N_A	DDR3_CS1N	LPDDR3_ODT1
AC27	DDR4_ODT0	LPDDR4_CS1N_B	DDR3_ODT0	LPDDR3_CS1N
AC28	DDR4_ODT1	LPDDR4_CS0N_B	DDR3_CS0N	LPDDR3_CS0N
AC29	DDR4_RESETN	LPDDR4_RESETN	DDR3_RESETN	-

#### ■ For DDR3/DDR3L:

Support the entire group swap between Byte; support DQ swap within Byte;

The CA sequence cannot be swapped and must be allocated according to the schematic design ; If need to support the template with a total bit width of 16bit and a template with a total bit width

compatible of 16bit/32bit, it's must use the template provided by RK, and no difference is allowed.

■ For DDR3/DDR3L and ECC:

ECC Byte is fixed, cannot swap with other Bytes; Support the entire group swap among other bytes; Support DQ swap within Byte;

The CA sequence cannot be swapped and must be allocated according to the schematic design .

■ For LPDDR3:

It is necessary to maintain the one-to-one connection between LPDDR3 D0-D7 and LPDDR3\_D0-D7 of

controller, as well as the corresponding relationship between the associated DQS and DM, does not support adjustment. Other Bytes support the entire group swap;

Support DQ swap within other Bytes;

The CA sequence cannot be swapped and must be allocated according to the schematic design .

■ For DDR4:

Support the entire group swap between Byte; support DQ swap within Byte;

The CA sequence cannot be swapped and must be allocated according to the schematic design ;

If need to support the template with a total bit width of 16bit and a template with a total bit width compatible of 16bit/32bit, it's must use the template provided by RK, and no difference is allowed.

■ For DDR4 and ECC:

ECC Byte is fixed, cannot swap with other Bytes;

The DQ sequence in the ECC Byte does not support swapping, and the DQ in other Bytes does not support swapping also, and must be allocated according to the reference diagram;

The CA sequence cannot be swapped, must be allocated according to the schematic design .

■ For LPDDR4/LPDDR4X:

All DQ and CA sequences cannot be swapped, must be allocated according to the schematic design .

8bits ECC function is supported in DDR3/DDR3L/DDR4 mode, requirements for the DDR with ECC function:

Select the same model of 8bit or 16bit DDR, the row/bank/col must be the same as the main DDRs(the Copyright © 2022 Rockchip Electronics Co., Ltd. 14

two DDRs you have already selected), and the rate must be greater than or equal to the main DDRs, it is recommended to use the same model as the main DDRs.

When using 16bit ECC DDR, since RK3568 only supports 8bits ECC, one of the Bytes of the 16bit ECC needs to be processed as shown below:

DDR3/DDR3L 16bit ECC processing method: as shown below, DMU pin is connected to power, DQSU pin is connected to power, DQSU pin is grounded.

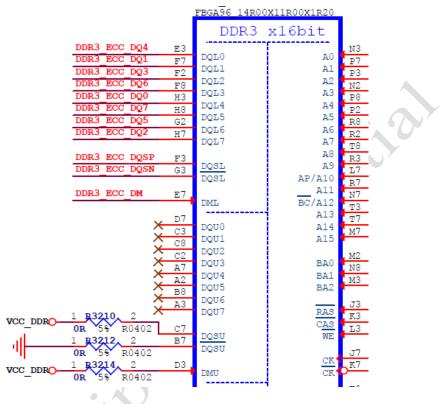


Figure 2-12 RK3568 16bit ECC DDR3/DDR3L processing method

 DDR4 16bit ECC process method: as shown below, DMU\_n/DBIU\_n pin is connected to power, DQSU\_P pin is connected to power, DQSU\_N pin is grounded.

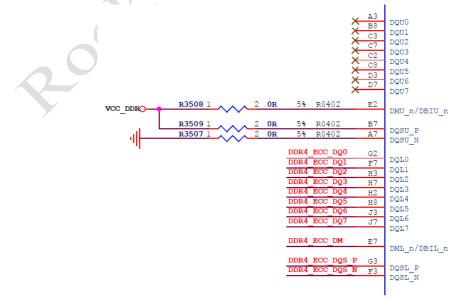


Figure 2-13 RK3568 16bit ECC DDR4 processing method

RK3568 DDR PHY's DDR\_RZQ (Pin H7) pin connection method:

- For DDR3/DDR3L/DDR4/LPDDR3, DDR\_RZQ pin must be grounded with a 120ohm 1% resistor.
- For LPDDR4/LPDDR4X, a 120ohm 1% resistor is connected to DDRPHY\_VDDQ power (VCC\_DDR).

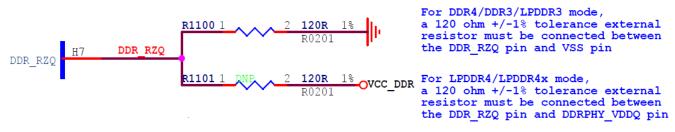


Figure 2-14 RK3568 DDR\_RZQ pin

RK3568 DDR PHY can provide voltage to VREFDQ or VREFCA of DRAM, that is, DDR\_VREFOUT pin (Pin P8) can output a voltage to DRAM as VREF voltage.

For DDR3/DDR3L: the default voltage of VREFDQ (VREF\_DDR\_DQ network) provided for DDR3/DDR3L is 0.75V/0.675V, and the voltage can be adjusted through registers according to the actual needs. The VREFCA of DDR3/DDR3L still uses two 1Kohm 1% resistor for voltage-dividing.

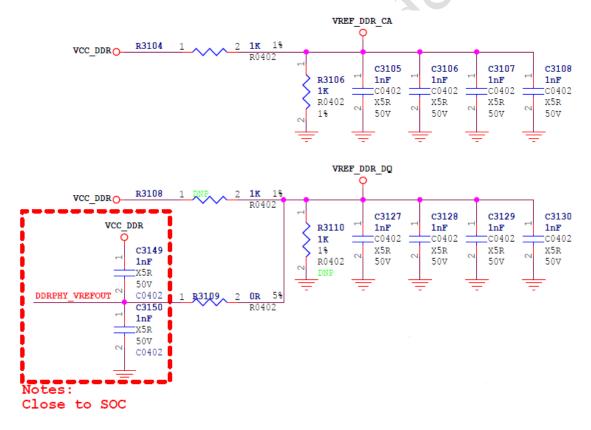
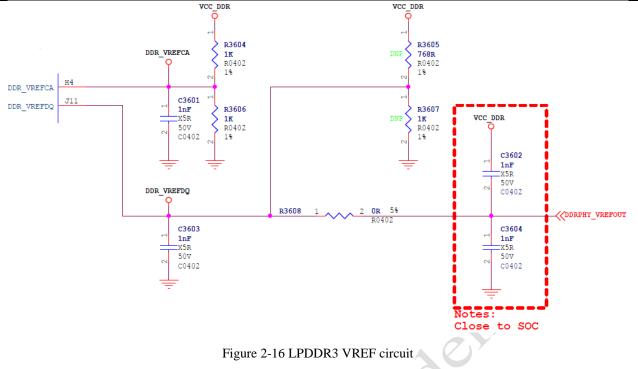
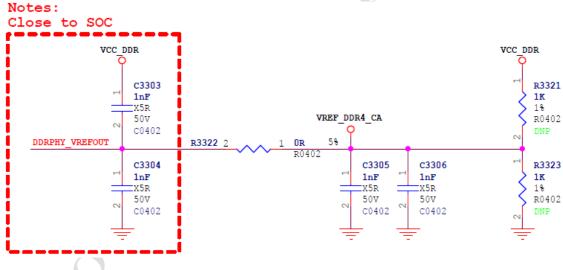


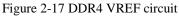
Figure 2-15 DDR3/DDR3L VREF circuit

For LPDDR3: the voltage of VREFDQ provided for LPDDR3 is related to the configuration of ODT, and the voltage can be adjusted through registers according to the actual needs. The VREFCA of LPDDR3 still uses two 1Kohm 1% resistor for voltage-dividing.



For DDR4: the default voltage of VREFCA (VREF\_DDR4\_CA network) provided for DDR4 is 0.6V, and the voltage can be adjusted through registers according to the actual needs.





■ For LPDDR4/LPDDR4X: when it is not used, leave floating.

Note: the 1nF capacitors connected to the ground and power of DDRPHY\_VREFOUT network cannot be deleted or modified randomly; the VREF pins of DDR must be with a 1nF decoupling capacitor, and the capacity cannot be modified randomly.

#### 2.1.7.3 DDR Peripheral Circuit Design

- The ZQ of DDR3/DDR3L/DDR4/LPDDR3 must connect a 240 ohm 1% resistor to ground;
- The ZQ of LPDDR4 must connect a 240 ohm 1% resistor to the VCC\_DDR power;
- The ZQ of LPDDR4x must connect a 240 ohm 1% resistor to the VCC0V6\_DDR power;
- It is recommended to reserve a 1nF capacitor for the DDR RESET pin to improve the anti-ESD interference capability

Copyright © 2022 Rockchip Electronics Co., Ltd.

- For 16bit DDR4 template, reserved to support DDP (Dual-Die Package), the default configuration parameter is SDP (Single-Die Package). When DDP is needed, the following parameters should be updated synchronously:
  - 1) DDR4 M9 pin connect to DDR\_BG1 net of SOC
  - 2) DDR4 T7 pin connect to GND
  - 3) DDR4 E9 pin connect to GND by 2400hm 1% resistor

### 2.1.7.4 DDR Topology and Matching Design

For DDR3/DDR3L 4 16bit 2CS, DQ uses T topology (one drive two), CA uses double T topology (one drive four).

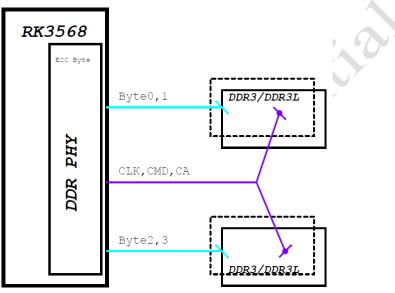
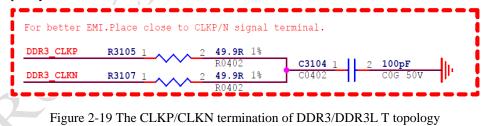


Figure 2-18 DDR3/DDR3L T topology

Clock matching mode: Place the RC circuit at the branch point as shown in the figure below, which can improve signal quality and reduce EMI.



■ For DDR3/DDR3L+ ECC six 16bit 2CS, DQ uses T topology (one drive two), CA uses Fly-by topology (one drive six).

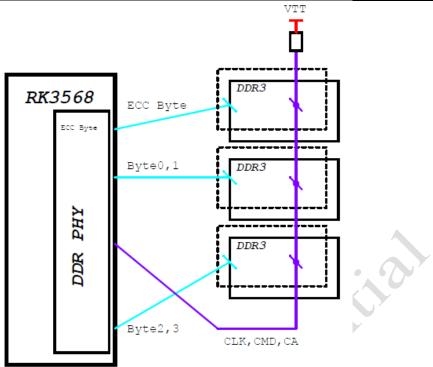


Figure 2-20 DDR3/DDR3L Fly-by topology

Clock, control, address line signal matching mode: add 390hm resistor to the VTT power at the end, please refer circuit shown in the schematic design.

In addition, a 2pF capacitor is reserved for connecting between the clock P and the clock N near RK3568, whether to add the capacitor according to the actual debugging, and the signal quality can be improved.

For DDR4 two 16bit 1CS, DQ uses point-to-point connection (one drive one), CA uses T topology (one drive two).

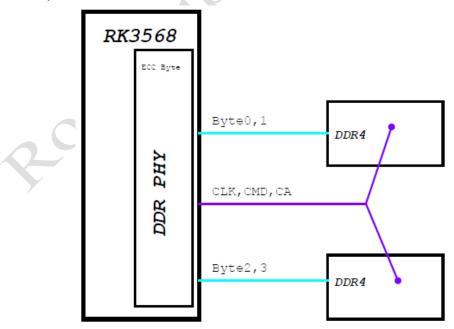


Figure 2-21 DDR4 T topology

Clock signal matching method: Place the RC circuit at the branch point, it is also necessary to connect resistors in series to DDR4 on the branch line, and the series resistor must be placed at the branch point to Copyright © 2022 Rockchip Electronics Co., Ltd. 19

improve the quality of the clock signal.

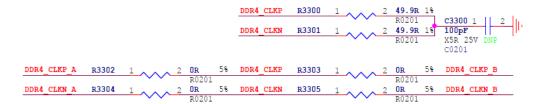


Figure 2-22 The CLKP/CLKN termination of DDR4 T topology

For DDR4 and ECC 3 16bit 1CS, DQ uses point-to-point connection (one drive one), CA uses Fly-by topology (one drive three).

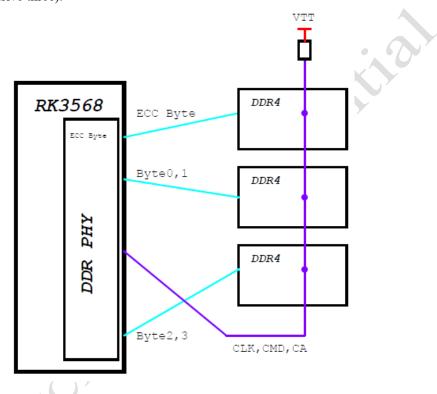


Figure 2-23 DDR4 Fly-by topology

Clock, control, address line signal matching mode: Add 39ohm resistor to the VTT power at the end, refer to the circuit shown in the reference diagram/ schematic design.

In addition, a 2pF capacitor is reserved for connecting between the clock P and the clock N near RK3568, and the signal quality can be improved.

Note: When chooses a VTT power chip, it needs to support DDR4.

■ For LPDDR3 1 32bit, DQ and CA use point-to-point topology.

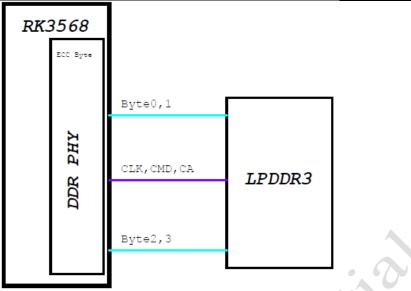


Figure 2-24 LPDDR3 point-to-point topology

Clock matching method: the RC circuit is placed at the end of the line, as shown in the figure below, which can improve signal quality and reduce EMI.

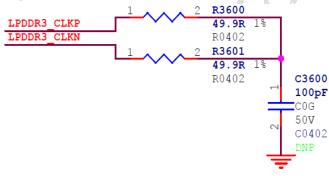


Figure 2-25 LPDDR3 CLKP/CLKN termination

■ For one 32bit LPDDR4, DQ and CA use point-to-point topology.

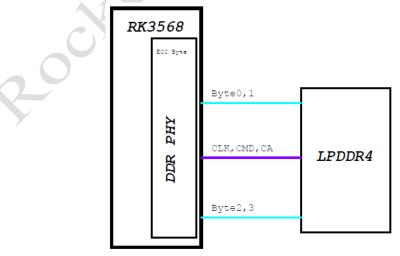


Figure 2-26 LPDDR4 point-to-point topology

Matching method: The DQ, CLK, CMD and CA of LPDDR4 all support ODT, all use point-to-point connection.

For one 32bit LPDDR4X, DQ and CA use point-to-point topology.

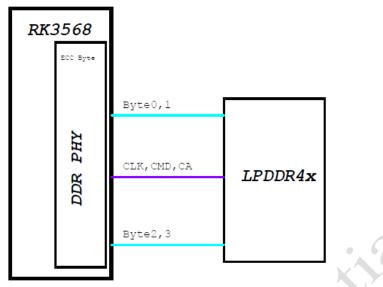


Figure 2-27 LPDDR4X point-to-point topology

Matching method: The DQ, CLK, CMD and CA of LPDDR4X all support ODT, all use point-to-point connection.

## 2.1.7.5 DDR Power Design and Power up Sequence Requirement

RK3568 DDR PHY have two groups of power supplies, DDRPHY\_VDDQ和DDRPHY\_VDDQL.

- For DDR3: DDRPHY\_VDDQ for 1.5V, DDRPHY\_VDDQL for 1.5V
- For DDR3L: DDRPHY VDDQ for 1.35V, DDRPHY VDDQL for 1.35V
- For LPDDR3: DDRPHY\_VDDQ for 1.2V, DDRPHY\_VDDQL for 1.2V (Actually supply 1.25V for improved compatibility)
- For DDR4: DDRPHY\_VDDQ for 1.2V, DDRPHY\_VDDQL for 1.2V
- For LPDDR4: DDRPHY VDDQ for 1.1V, DDRPHY VDDQL for 1.1V
- For LPDDR4X: DDRPHY\_VDDQ for 1.1V, DDRPHY\_VDDQL for 0.6V

Notes of power supply circuit:

When using the RK809-5 power solution, it is important to note that according to the actual use of DRAM particles, the voltage divider resistance value of RK809-5 FB3 (pin27) should be modified synchronously to make the VCC\_DDR output voltage match the particle.

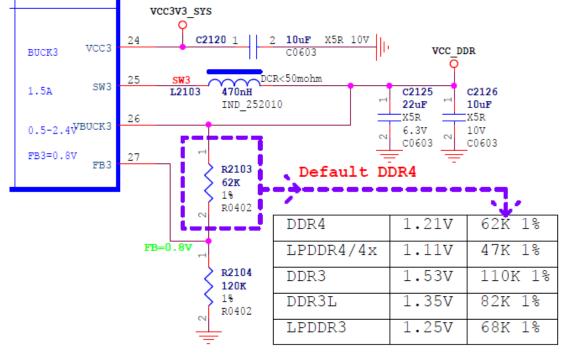


Figure 2-28 RK809-5 BUCK3 parameters regulation

- When using discrete power supply solution, the voltage-dividing resistance value of power supply BUCK should be modified synchronously to make the VCC\_DDR output voltage match with the DRAM.
- RK3568 reference template provides LPDDR4 and LPDDR4X compatible design
   "RK3568\_Template\_LP4XD200P132SD6\_43x28\_1600MHz", it should be noted that the circuit must be
   selected according to the actual materials. When using LPDDR4, only need to connect the R3804 resistor
   as shown below, all component s in the green box below are not needed; when using LPDDR4X, R3804
   is not connected, all components in the green box below are needed.

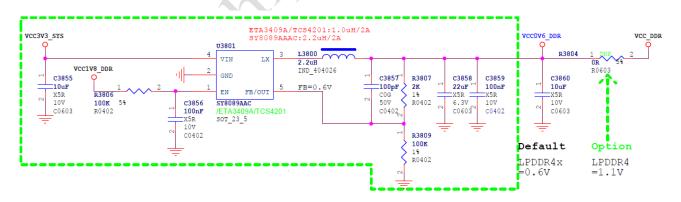


Figure 2-29 Power selection of LPDDR4/LPDDR4x compatible design

For all types of DRAM power-up sequence, please refer to JEDEC standards:

■ The power-up sequence of DDR3/DDR3L SDRAM is shown in the figure below:

- Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.</li>
  - · VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
  - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- · Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2-30 DDR3 SDRAM power up sequence

■ The power-up sequence of LPDDR3 SDRAM is shown in the figure below:

After	Applicable Conditions	
Ta is reached	$V_{\rm DD1}$ must be greater than $V_{\rm DD2}$ —200mV	
	$V_{\rm DD1}$ and $V_{\rm DD2}$ must be greater than $V_{\rm DDCA}$ —200mV	
	$V_{\rm DD1}$ and $V_{\rm DD2}$ must be greater than $V_{\rm DDQ}$ —200mV	
	$V_{\rm Ref}$ must always be less than all other supply voltages	

Figure 2-31 LPDDR3 SDRAM power up sequence

■ The power-up sequence of DDR4 SDRAM is shown in the figure below:

Apply power (RESET\_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET\_n needs to be maintained for minimum 200us with stable power. CKE is pulled "Low" anytime before RESET\_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V<sub>DD</sub> min must be no greater than 200ms; and during the ramp, V<sub>DD</sub> ≥ V<sub>DDQ</sub> and (V<sub>DD</sub>-V<sub>DDQ</sub>) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.</li>

+  $V_{\text{DD}}$  and  $V_{\text{DDQ}}$  are driven from a single power converter output, AND

• The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side. In addition,  $V_{TT}$  is limited to TBDV max once power ramp is finished, AND

VrefCA tracks TBD.

or

- Apply  $V_{\text{DD}}$  without any slope reversal before or at the same time as  $V_{\text{DDQ}}$
- Apply V<sub>DDQ</sub> without any slope reversal before or at the same time as V<sub>TT</sub> & VrefCA.
- · Apply VPP without any slope reversal before or at the same time as VDD.

• The voltage levels on all pins other than  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  must be less than or equal to  $V_{DDQ}$  and  $V_{DD}$  on one side and must be larger than or equal to  $V_{SSQ}$  and  $V_{SS}$  on the other side.

#### Figure 2-32 DDR4 SDRAM power up sequence

■ The power-up sequence of LPDDR4/4x SDRAM is shown in the figure below:

 While applying power (after Ta), RESET\_n is recommended to be LOW (≤0.2 x V<sub>DD2</sub>) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V<sub>DD1</sub> must ramp at the same time or earlier than V<sub>DD2</sub>. V<sub>DD2</sub> must ramp at the same time or earlier than V<sub>DDQ</sub>.

After Applicable Conditions	
	V <sub>DD1</sub> must be greater than V <sub>DD2</sub>
Ta is reached	$V_{DD2}$ must be greater than $V_{DDQ}$ - 200 mV

# Table 5 — Voltage Ramp Conditions

NOTE 1 Ta is the point when any power supply first reaches 300 mV.

NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

NOTE 5 The voltage difference between any of V<sub>SS</sub> and V<sub>SSQ</sub> pins must not excess 100 mV.

Figure 2-33 LPDDR4/4x SDRAM power up sequence

#### 2.1.7.6 DDR Support List

For the DDR support list, please refer to the document "Rockchip\_Support\_List\_DDR", which can be

downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s\_pctim\_aiomsg

### 2.1.8 eMMC Circuit

#### 2.1.8.1 eMMC Controller Introduction

The features of RK3568 eMMC controller are as follows:

- Compatible with standard iNAND interface;
- Compatible with the 4.41,4.51,5.0, and 5.1 specifications;
- Support three data bus widths of 1-bit, 4-bit and 8-bit;
- Support HS200 mode;
- Support CMD Queue;

#### 2.1.8.2 eMMC Circuit Design Suggestion

RK3568 eMMC interface is multiplexed with Nand Flash and FSPI Flash interface, in the design of eMMC interface, please refer to the schematic for the eMMC signal connection method, including the decoupling capacitors of each power supply.

The boot code is placed in eMMC, when using eMMC, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the EMMC\_D0 or EMMC\_CLK network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the EMMC\_D0 or EMMC\_CLK short to ground, and power on, RK3568 will enter into the Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of EMMC\_D0 or EMMC\_CLK, otherwise the flashing will fail).

Normally, it is not recommended to update the firmware in this way, because improper operation may cause Copyright © 2022 Rockchip Electronics Co., Ltd. 25

IO damage.

TP1301 TP_0.7	Note: For eMMC or Nand Flash: If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Figure 2-34 eMMC\_D0 test point

### 2.1.8.3 eMMC Topology and Matching Method Design

■ eMMC connection diagram:

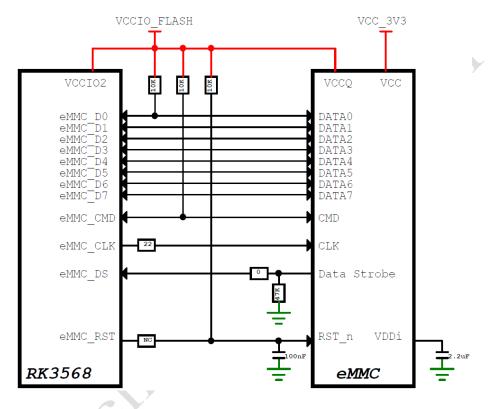


Figure 2-35 eMMC connection diagram

eMMC interface pull up and down and matching design suggestions as shown in Table 2-6:

Signal	Internal pull up/down	Connection mode	Description(chipset))
eMMC_D[7:0]	pull up	direct connection, D0 external pull-up with a 10K ohm resistor, other data use the pull-up resistor inside the RK3568 chip	eMMC data send/receive
eMMC_CLK	pull down	connect 220hm resistor in series with RK3568	eMMC clock send
eMMC_CMD	pull up	direct connection, D0 external pull-up with a 10K ohm resistor	eMMC command send/receive
eMMC_DATA_ Strobe	pull down	connect a 00hm resistor in series with the eMMC, and reserve a 47K ohm pull-down resistor	eMMC data and command receive refer to Strobe

### Table 2-6 RK3568 eMMC interface design

• Connection diagram of eMMC and Nand Flash in compatible design:



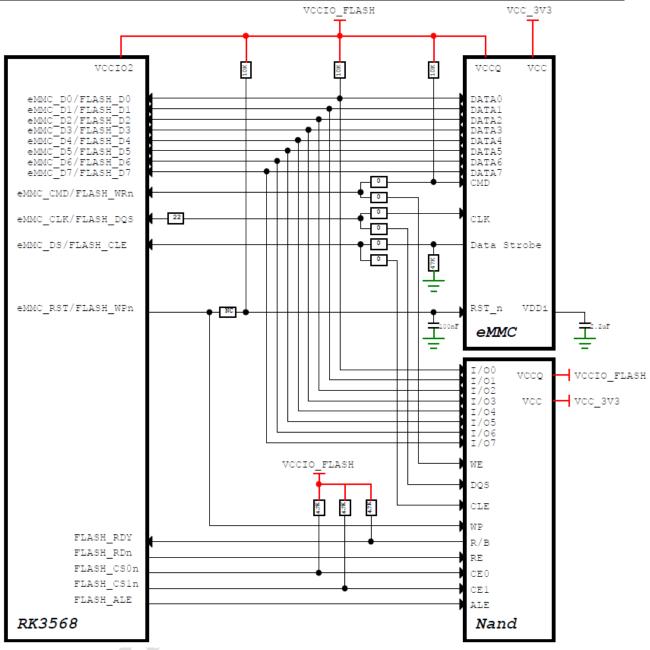


Figure 2-36 Connection diagram of eMMC and Nand Flash in compatible design

In compatible design, there will be branches in the multiplexed signal routing. To ensure that the impact of eMMC signal quality is minimized, the three signals eMMC\_CMD/FLASH\_WRn, eMMC\_CLK/FLASH\_DQS, eMMC\_DS/FLASH\_CLE should reserve series resistors at the branch points. For example: when using eMMC, the 0ohm resistors that branch to the eMMC are needed, and the 0ohm resistors that branch to the Nand Flash are not needed, which will minimize the branching impact in routing. D0-D7 can minimize the branching impact through PCB Layout (For Nand, the D0 pull-up resistor cannot be connected, please refer to the PCB Layout design below.

#### 2.1.8.4 eMMC Power up Sequence Requirement

The eMMC interface of RK3568 belongs to VCCIO2 power domain, only one power supply, so there is no sequence requirements.

The eMMC have two sets of power supplies, refer to JEDEC standard for power-on sequence:

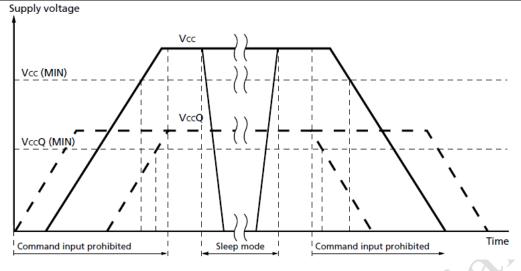


Figure 2-37 eMMC power up and power down sequence

### 2.1.8.5 eMMC Support List

For RK3568 eMMC support list, please refer to the document "RKeMMCSupportList", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s\_pctim\_aiomsg

# 2.1.9 FSPI Flash Circuit

### 2.1.9.1 FSPI Flash ( Boot is supported ) Interface Introduction

FSPI is a flexible serial interface controller. There is a FSPI controller in RK3568 chip, which can be used to connect FSPI devices.

The features of RK3568 FSPI controller are as follows:

- Support serial NOR and NAND FLASH;
- Support SDR mode;
- Support single/dual/four-line mode;

# 2.1.9.2 FSPI Flash Circuit Design Suggestion

FSPI Flash interface of RK3568 is multiplexed with Nand Flash and eMMC interface. In FSPI Flash interface design, please refer to the schematic for the FSPI Flash signal connection mode, including the decoupling capacitors for each power supply.

The boot code is placed in FSPI Flash, when using the FSPI Flash, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the FSPI\_CLK network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the FSPI\_CLK short to ground, and then power on, RK3568 will enter Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of FSPI\_CLKK, and otherwise the flashing will fail).

Normally, it is not recommended to update the firmware in this way, because improper operation may cause IO damage.

 FSPI\_CLK/FLASH\_ALE
 TP1302
 TP\_0.7
 Note:

 TP1303
 TP\_0.7
 For SPI Flash:
 If FSPI\_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

Figure 2-38 FSPI\_CLK test point

## 2.1.9.3 FSPI Flash Topology and Matching Design

FSPI Flash connection diagram:

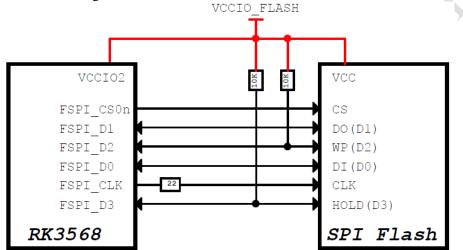


Figure 2-39 FSPI Flash connection diagram

■ FSPI interface pull up and down and matching design suggestions as shown in Table 2-7: Table 2–7 RK3568 FSPI interface design

Signal	Internal pull up/down	Connection mode	Description(chipset)
FSPI_D[3:0]	D2 pull down D0/D1/D3 pull up	direct connection, D2, D3 external pull-up with a 10K ohm resistor,	FSPI data send/receive
FSPI0_CLK	pull down	connect 220hm resistor in series with RK3568	FSPI clock send
FSPI0_CS0n	pull up	direct connection	FSPI chip select signal

### 2.1.9.4 FSPI Power up Sequence Requirement

The FSPI Flash interface of RK3568 chip belongs to the VCCIO2 power domain, only one power supply, so there is no sequence requirements.

The SPI Flash have only one power supply, the power supply must be the same as the VCCIO2 power domain power supply.

### 2.1.9.5 SPI Flash Support List

For RK3568 SPI Flash support list, please refer to the document "RK SpiNor and SLC Nand SupportLis", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s\_pctim\_aiomsg

### 2.1.10.1 Nand Flash Controller Introduction

RK3568 Nand Flash controller supports the following features:

- Support asynchronous Nand Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support ONFI synchronous Nand Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support Toggle Flash interface, 8bits data bus width, support up to 2 chip selects;
- Support SLC, MLC, TLC Flash;
- Support ECC and so on;

#### 2.1.10.2 Nand Flash Circuit Design Suggestion

The Nand Flash interface of RK3568 is multiplexed with FSPI Flash and eMMC interface. In Nand Flash interface design, please refer to the schematic for the Nand Flash signal connection mode, including the decoupling capacitors for each power supply.

The reference schematic is compatible with different types of Nand Flash. Please select the peripherals according to the model actually used. When using Nand Flash in DDR mode, Pin28 and 45 of Nand Flash should be connected to the VCCIO\_FLASH power; and Pin38 of some SLC is for protection. If such Flash are used, Pin38 leave floating

The boot code is placed in Nand Flash, when using the Nand Flash, it must be noted that whether the IO drive voltage mode configuration of RK3568 VCCIO2 power domain is matched with the actual supply voltage, please see Section 2.1.5 System Initialization Configuration Signal for details.

During the design, be sure to reserve test points on the Flash\_D0 network, in order to prevent the abnormal booting caused by flashing a wrong firmware during the development process. Make the Flash\_D0 short to the ground, and power on, RK3568 will enter the Maskrom mode, then download a new firmware through the PC tool (after the PC tool recognizes the Maskrom, it must release the grounding short circuit of Flash\_D0, otherwise the flashing will fail)..

Normally, it is not recommended to update the firmware in this way, because improper operation may cause IO damage.

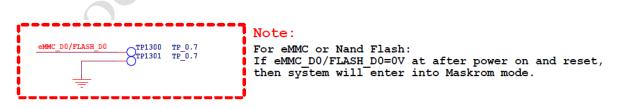


Figure 2-40 Flash\_D0 test point

### 2.1.10.3 Nand Flash Topology and Matching Design

■ Nand Flash connection diagram:

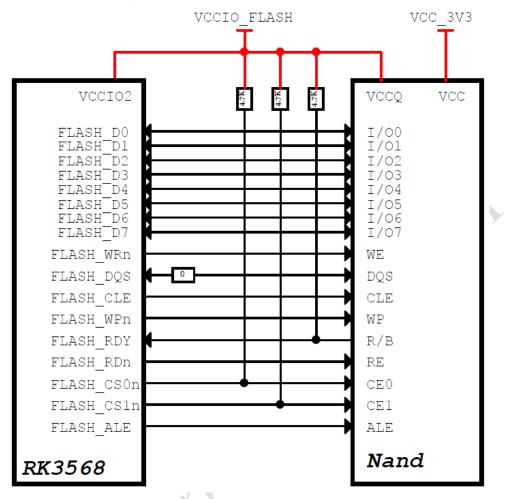


Figure 2-41 Nand Flash connection diagram

■ Nand Flash interface pull up and down and matching design suggestions as shown in Table 2-8:

Signal	Internal pull up/down	Connection mode	Description(chipset)
Flash D[7:0]	pull up	direct connection	Nand Flash data send and receive
Flash_WRn	pull up	direct connection	Nand Flash write enable
Flash_DQS	pull down	connect 220hm resistor in series with RK3568	Nand Flash data strobe
Flash_CLE	pull down	direct connection	Nand Flash command latch enable
Flash_WPn	pull down	direct connection	Nand Flash write protected
Flash_RDY	pull up	direct connection, external pull-up with a 4.7K ohm resistor	Nand Flash ready/busy
Flash_RDn	pull up	direct connection	Nand Flash read enable
Flash_CS0n	pull up	direct connection, external pull-up with a 4.7K ohm resistor	Nand Flash chip select 0
Flash_CS1n	pull up	direct connection, external pull-up with a 4.7K ohm resistor	Nand Flash chip select 1
Flash_ALE	pull down	direct connection	Nand Flash address latch enable

Table 2–8 RK3568 Nand Flash interface design

■ When using eMMC and Nand Flash compatible design, please see eMMC circuit description.

#### 2.1.10.4 Nand Flash Power up Sequence Requirement

The Nand Flash interface of RK3568 chip belongs to the VCCIO2 power domain, only one power supply, so

there are no sequence requirements.

- The Nand Flash have only one power supply, the power supply must be the same as the VCCIO2 power domain power supply.
- The Nand Flash have two sets of power supplies, refer to JEDEC standard for power-on sequence:

Some NAND Flash devices do not support  $V_{CCQ}$ . For these devices all references to  $V_{CCQ}$  are replaced with  $V_{CC}$ .

SpecTek NAND Flash devices are designed to prevent data corruption during power transitions.  $V_{\rm CC}$  is internally monitored. (The WP# signal supports additional hardware protection during power transitions. When ramping  $V_{\rm CC}$  and  $V_{\rm CCQ}$ , use the following procedure to initialize the device:

- 1. Ramp V<sub>CC</sub>.
- 2. Ramp  $V_{CCO}$  and  $V_{CCO}$  must not exceed  $V_{CC}$ .
- 3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 29). The R/B# signal becomes valid when 50µs has elapsed since the beginning the VCC ramp, and 10µs has elapsed since  $V_{CCQ}$  reaches  $V_{CCQ}$  (MIN) and  $V_{CC}$  reaches  $V_{CC}$  (MIN).
- 4. If not monitoring R/B#, the host must wait at least 100µs after  $V_{\rm CCQ}$  reaches  $V_{\rm CCQ}$  (MIN) and  $V_{\rm CC}$  reaches  $V_{\rm CC}$  (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
- 5. If  $V_{CCQ}$  is in the 1.8V operational range, then the asynchronous interface is active by default for each target. Each LUN draws less than an average of  $I_{ST}$  measured over intervals of 1ms until the RESET (FFh) command is issued.
- 6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for <sup>t</sup>POR after a RESET command is issued. LUN0 of each target is selected by default after power-on. The RESET busy time can be monitored by polling R/B# or by using the READ STATUS (70h) command. For multi-LUN configurations the READ STATUS ENHANCED (78h) command should be used to check initialization status of each LUN on the target. The host must not issue an additional RESET (FFh) command during <sup>t</sup>POR.
- 7. The device is now initialized and ready for normal operation.

At power-down,  $V_{\rm CCQ}$  must go LOW, either before, or simultaneously with,  $V_{\rm CC}$  going LOW.

When  $V_{CCQ}$  = 0V, the host must keep RE\_t/RE\_c, DQS\_t/DQS\_c signals LOW. RE\_t/RE\_c, DQS\_t/DQS\_c signals maybe ramped with  $V_{CCQ}$  during power up but not exceed  $V_{CCQ}$ . When  $V_{CCQ}$  = 0V, the host must keep DQ[7:0] signals LOW or they can be left High-Z. DQ[7:0] signals may be ramped with  $V_{CCQ}$  during power up but not exceed  $V_{CCQ}$ . It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND  $V_{CCQ}$  voltage is below  $V_{CCQ,min}$ . R/B# signals maybe ramped with  $V_{CCQ}$  during power up but not exceed  $V_{CCQ}$ .

Figure 2-42 Nand Flash power up and down sequence

#### 2.1.10.5 Nand Flash Support List

For RK3568 Nand Flash support list, please refer to the document "RK Nand Flash SupportList", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s pctim aiomsg

### 2.1.11 GPIO Circuit

In RK3568, there are three types of GPIO: only support 1.8V, only support 3.3V, and support configurable 1.8V/3.3V two voltages.

#### 2.1.11.1 GPIO Pins Description

For example, the function SDMMC1\_D0, GMAC0\_RXD2 and UART6\_RX\_M0 in the figure below are multiplexed on GPIO2\_A3, and only one of the functions can be selected for use when assigning.



SDMMC1\_D0

/ GPIO2 A3 u

/ GMAC0\_RXD2 / UART6\_RX\_M0

- Except for boot related GPIO, the rest of IOs are reset to input by defaults;
- GPIOx xx u where u indicates that the default state of this IO reset is internal pull-up;
- GPIOx xx d where d indicates that the default state of this IO reset is internal pull-down;
- GPIOx\_xx\_z where \_z indicates that the default state of this IO reset is high impedance;
- The name suffix of each function with \_M0 or M1 or \_M2 indicates that the same function is multiplexed on different IO, only one of them can be selected at the same time. For example, when selecting the UART2 function, the UART2\_TX\_M0 and UART2\_RX\_M0 combination must be selected. The combination of UART2\_TX\_M0 and UART2\_RX\_M1 is not supported. This is the constraint for all functions with different IOMUX.

#### 2.1.11.2 GPIO Drive Capability

In RK3568, GPIO provides multiple levels of adjustable driving strength. Most are Level 0-5 and some GPIO can achieve Level 0-11 adjustment levels. For details, please refer to the "RK3568\_PinOut" document. In addition, depending on the type of GPIO, the initial default driving strength is different. Please refer to the chip TRM for configuration modification, or refer to Table 5 "SupportDriveStrength" and "DefaultIO DriveStrength" columns in the "RK3568\_PinOut" document.

#### 2.1.11.3 GPIO Power

Table 2-9 RK3568 GPIO power pins description **Power domain GPIO** Type Pin name Description PMUI00 1.8V PMUPLL\_AVDD\_1V8 1.8V Only IO supply for this GPIO domain (group). PMUI01 3.3V PMUI01 3.3V Only IO supply for this GPIO domain (group). PMUIO2 1.8V/3.3V PMUIO2 1.8V or 3.3V IO supply for this GPIO domain (group). 1.8V/3.3V VCCI01 1.8V or 3.3V IO supply for this GPIO domain (group). VCCI01 1.8V/3.3V VCCIO2 VCCIO2 1.8V or 3.3V IO supply for this GPIO domain (group). VCCIO3 1.8V/3.3V VCCIO3 1.8V or 3.3V IO supply for this GPIO domain (group). VCCIO4 VCCIO4 1.8V/3.3V 1.8V or 3.3V IO supply for this GPIO domain (group). VCCI05 1.8V/3.3V VCCI05 1.8V or 3.3V IO supply for this GPIO domain (group). VCCIO6 1.8V/3.3V VCCIO6 1.8V or 3.3V IO supply for this GPIO domain (group). VCCI07 1.8V/3.3V VCCI07 1.8V or 3.3V IO supply for this GPIO domain (group).

The power pins of the GPIO power domain are described as follows:

PMUIO0 and PMUIO1 are fixed-level power domains which cannot be configured;

PMUIO2 and VCCIO1, VCCIO [3:7] power domains require that their hardware power supply voltages must be consistent with the software configuration correspondingly:

When the hardware IO is connected to 1.8V, the software voltage configuration should be set to 1.8V accordingly; When the hardware IO is connected to 3.3V, the software voltage configuration should be set to **3.3V accordingly;** 

There is no need to configure VCCIO2 power domain by software, but its hardware power supply and FLASH VOL SEL status must be matched:

- When VCCIO2 voltage is connected to 1.8V, FLASH\_VOL\_SEL must be high;
- When VCCIO2 voltage is connected to 3.3V, FLASH VOL SEL must be low;

**Otherwise:** 

- If the software configuration is 1.8V, but the hardware power supply is 3.3V, it will cause the low withstand voltage circuit working in overvoltage state, and the IO will be damaged after long time working;
- If the software configuration is 3.3V, but the hardware power supply is 1.8V, the circuit will work abnormally; ALCON

For example, the default dts configuration is as follows:

```
&pmu io domains {
```

```
status = "okay";
```

```
pmuio1-supply = <&vcc 3v3>;
```

```
pmuio2-supply = <&vcc 3v3>;
```

vccio1-supply = <&vcc 3v3>;

vccio3-supply = <&vcc 3v3>;

```
vccio4-supply = <\&vcc | 1v8 >;
```

vccio5-supply = <&vcc 3v3>;

```
vccio6-supply = <&vcc 1v8>;
```

```
vccio7-supply = <&vcc 3v3>;
```

```
};
```

If the actual VCCIO4 power supply is 3.3V, then dts needs to be updated to:

```
&pmu io domains {
```

```
status = "okay";
pmuio1-supply = <&vcc 3v3>;
pmuio2-supply = <&vcc 3v3>;
vccio1-supply = <&vcc 3v3>;
vccio3-supply = <&vcc 3v3>;
vccio4-supply = <&vcc 3v3>;
vccio5-supply = <&vcc 3v3>;
vccio6-supply = <&vcc 1v8>;
vccio7-supply = <&vcc 3v3>;
```

```
};
```

If other power domains have changed and they must be updated and matched accordingly.

Various documents released by Rockchip have emphasized this notice, please review the voltage Copyright © 2022 Rockchip Electronics Co., Ltd.

34

configuration and hardware power supply of your projects as soon as possible!

Reference documents:

1) DTS configuration documentation: https://redmine.rock-chips.com/documents/106

2) Checklist: Rockchip RK3568 IO Power Domain Description and Checklist V1.0 CN.xlsx

Also, note that the IO level of the power domain should be consistent with the IO level of the peripheral chip/device.

At least one 100nF decoupling capacitor must be placed nearby the power supply pins of each power domain. See the reference schematic for the detailed design and they cannot be deleted at will.

in does not the second s If all IOs in a power domain are not used, then the power supply of this power domain does not need to supply power, and the pin leave floating.

Copyright © 2022 Rockchip Electronics Co., Ltd.

e chine

# 2.2 Power Supply Design

### 2.2.1 RK3568 Power Supply Introduction

#### 2.2.1.1 Power Supply Requirements of RK3568

Table 2-10 RK3568	nower supply	requirements
1aule 2-10 KK5500	power suppry	requirements

Module	Power Pin	Description
PMUPLL	PMUPLL AVDD 0V9、PMUPLL AVDD 1V8	PMU PLL Power
SYSPLL	SYSPLL AVDD 0V9, SYSPLL AVDD 1V8	System PLL Power
CPU	VDD CPU	ARM Power
GPU	VDD GPU	GPU Power
NPU	VDD_NPU	NPU Power
Logic	VDD_LOGIC	SOC Logic Power
PMU Logic	PMU_VDD_LOGIC_0V9	PMU Logic Power
DDR	DDRPHY_VDDQ、 DDRPHY_VDDQL	DDR PHY Power
GPIO	PMUIO0, PMUIO1, PMUIO2, VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7	IO Domain Power
SARADC	SARADC_AVDD_1V8	SAR ADC Power
OTP	OTP_VCC18	OTP Power
USB2.0 PHY	USB3_AVDD_0V9 、 USB3_AVDD_1V8 、 USB3_AVDD_3V3	USB2.0 PHY Power(Controller use USB3.0, it is combined with the SS signal of MULTI PHY0/1 to form a complete USB3.0 interface, so the name starts with USB3)
USB2.0 PHY	USB2_AVDD_0V9 、 USB2_AVDD_1V8 、 USB2_AVDD_3V3	USB2.0 PHY Power
MULTI_PHY	MULTI_PHY_AVDD_0V9 、 MULTI_PHY_AVDD_1V8	MULTI_PHY Power
PCIe3.0 PHY	PCIE30_AVDD_0V9、 PCIE30_AVDD_1V8	PCIe3.0 PHY Power
MIPI CSI RX PHY	MIPI_CSI_RX_AVDD_0V9 MIPI_CSI_RX_AVDD_1V8	MIPI CIS RX PHY Power
MIPI DSI TX0/LVDS TX Combo PHY	MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 、 MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8	MIPI DSI TX0/LVDS TX Combo PHY Power
MIPI DSI TX1 PHY	MIPI_DSI_TX1_AVDD_0V9 、 MIPI_DSI_TX1_AVDD_1V8	MIPI DSI TX1 PHY Power
eDP TX PHY	eDP_TX_AVDD_0V9、 eDP_TX_AVDD_1V8	eDP TX PHY Power
HDMI2.0 TX PHY	HDMI_TX_AVDD_0V9、 HDMI_TX_AVDD_1V8	HDMI2.0 TX PHY Power

#### 2.2.1.2 Power-on Sequence Requirements of RK3568

Theoretically, follow the principle: for the same module, low voltage power on first, high voltage power on later; for the same module with the same voltage can power on together, and there is no timing requirement between different modules, after the last voltage is stable, RESETn can only be released after at least 10ms.

■ The recommended power-on sequence of the digital power supply is as follows:

 $\mathsf{PMU}_\mathsf{VDD}_\mathsf{LOGIC}_\mathsf{0V9} \rightarrow \mathsf{VDD}_\mathsf{LOGIC} \rightarrow \mathsf{VDD}_\mathsf{CPU}/\mathsf{VDD}_\mathsf{GPU}/\mathsf{VDD}_\mathsf{NPU}$ 

The recommended power-on sequence for SARADC is as follows:

VDD\_LOGIC  $\rightarrow$  SARADC\_AVDD\_1V8

- The recommended power-on sequence for OTP is as follows:
- VDD\_LOGIC  $\rightarrow$  OTP\_VCC18
- The recommended power-on sequence for USB PHY is as follows:

 $\text{USB3}\_\text{AVDD}\_0\text{V9} \rightarrow \text{USB3}\_\text{AVDD}\_1\text{V8} \rightarrow \text{USB3}\_\text{AVDD}\_3\text{V3}$ 

USB2\_AVDD\_0V9  $\rightarrow$  USB2\_AVDD\_1V8  $\rightarrow$  USB2\_AVDD\_3V3

■ The recommended power-on sequence for MIPI CSI RX PHY is as follows:

 $MIPI\_CSI\_RX\_AVDD\_0V9 \rightarrow MIPI\_CSI\_RX\_AVDD\_1V8$ 

■ The recommended power-on sequence for MIPI DSI TX0/LVDS Combo PHY is as follows: MIPI DSI TX0/LVDS TX0 AVDD 0V9 → MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_1V8

There is no restriction on other modules power-on sequence.

According to the power network name assigned by the reference schematic, the overall recommended power-on sequence is as follows:

VDDA0V9\_PMU、VDDA\_0V9、VDD\_LOGIC  $\rightarrow$  VCCA1V8\_PMU、VCCA\_1V8、VDD\_GPU、 VCC3V3\_PMU、VCC\_1V8  $\rightarrow$  VDD\_CPU、VCC2V5\_DDR  $\rightarrow$  VCC\_DDR  $\rightarrow$  VCC\_3V3、VCCIO\_SD、 VCC3V3\_SD  $\rightarrow$  RESETn

Intervals>=0us

# 2.2.1.3 Power-off Sequence Requirements of RK3568

During the power-off process, RESETn must be pulled down first, and then each power supply will be powered off.

# 2.2.2 Power Supply Design Suggestion

# 2.2.2.1 Power-on and Standby Circuit Scheme

The power supply status of each module of RK3568 is shown as the following Table when it is first powered on:

Module	Power Pin	Power supply requirements in first power-on
PMUPLL	PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8	Must be powered
SYSPLL	SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8	Must be powered
CPU	VDD_CPU	Must be powered
GPU	VDD_GPU	Can be unpowered
NPU	VDD_NPU	Can be unpowered
Logic	VDD_LOGIC	Must be powered
PMU Logic	PMU_VDD_LOGIC_0V9	Must be powered

Table 2-11 RK3568 power supply requirement of each module for the first powered on

Module	Power Pin	Power supply requirements in first power-on
DDR	DDRPHY_VDDQ、DDRPHY_VDDQL	Must be powered
GPIO	PMUIO0、PMUIO1、PMUIO2	Must be powered
GPIO	VCCIO2	Must be powered
GPIO	VCCIO3	Must be powered
GPIO	VCCI01、VCCI04、VCCI05、VCCI06、VCCI07	Can be unpowered
SARADC	SARADC_AVDD_1V8	Must be powered
OTP	OTP_VCC18	Must be powered
USB2.0 PHY	USB3_AVDD_0V9、USB3_AVDD_1V8、	Must be powered
	USB3_AVDD_3V3、	
USB2.0 PHY	USB2_AVDD_0V9\USB2_AVDD_1V8\USB2_AVDD_3V3	Can be unpowered
MULTI_PHY	MULTI_PHY_AVDD_0V9、MULTI_PHY_AVDD_1V8	Can be unpowered
PCIe3.0 PHY	PCIE30_AVDD_0V9、PCIE30_AVDD_1V8	Can be unpowered
MIPI CSI RX PHY	MIPI_CSI_RX_AVDD_0V9、MIPI_CSI_RX_AVDD_1V8	Can be unpowered
MIPI DSI TX0/LVDS	MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9、	Can be unpowered
Combo PHY	MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8	
MIPI DSI TX1 PHY	MIPI_DSI_TX1_AVDD_0V9、MIPI_DSI_TX1_AVDD_1V8	Can be unpowered
deep TX PHY	eDP_TX_AVDD_0V9、	Can be unpowered
	eDP_TX_AVDD_1V8	
HDMI2.0 TX PHY	HDMI_TX_AVDD_0V9、	Can be unpowered
	HDMI_TX_AVDD_1V8	

Note: If the unused module is not powered, the software is required to disable the configuration of the corresponding node in the DTS, otherwise it may cause the kernel initialization stuck.

The RK3568 chip can support a low-power standby solution. When entering the standby mode, the power supply and power-off conditions are as follows:

Module	Power Pin	Power supply requirements in Low power consumption standby
PMUPLL	PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8	Power must be supplied
SYSPLL	SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8	Can support power off
CPU	VDD_CPU	Can support power off
GPU	VDD_GPU	Can support power off
NPU	VDD_NPU	Can support power off
Logic	VDD_LOGIC	Can support power off
PMU Logic	PMU_VDD_LOGIC_0V9	Power must be supplied
DDR	DDRPHY_VDDQ、 DDRPHY_VDDQL	Power must be supplied

Table 2-12 RK3568 standby power supply requirements

Module	Power Pin	Power supply requirements in Low power consumption standby
GPIO	PMUIO0、PMUIO1、PMUIO2	Power must be supplied
GPIO	VCCIO2	Can support power off
GPIO	VCCIO3	Can support power off
GPIO	VCCIO1、VCCIO4、VCCIO5、VCCIO6、VCCIO7	Can support power off
SARADC	SARADC_AVDD_1V8	Can support power off
OTP	OTP_VCC18	Can support power off
USB2.0 PHY	USB3_AVDD_0V9\USB3_AVDD_1V8\USB3_AVDD_3V3\	Can support power off
USB2.0 PHY	USB2_AVDD_0V9、USB2_AVDD_1V8、USB2_AVDD_3V3	Can support power off
MULTI_PHY	MULTI_PHY_AVDD_0V9、MULTI_PHY_AVDD_1V8	Can support power off
PCIe3.0 PHY	PCIE30_AVDD_0V9、 PCIE30_AVDD_1V8	Can support power off
MIPI CSI RX PHY	MIPI_CSI_RX_AVDD_0V9、MIPI_CSI_RX_AVDD_1V8	Can support power off
MIPI DSI TX0/LVDS Combo PHY	MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8	Can support power off
MIPI DSI TX1 PHY	MIPI_DSI_TX1_AVDD_0V9、MIPI_DSI_TX1_AVDD_1V8	Can support power off
eDP TX PHY	eDP_TX_AVDD_0V9、 eDP_TX_AVDD_1V8	Can support power off
HDMI2.0 TX PHY	HDMI_TX_AVDD_0V9, HDMI_TX_AVDD_1V8	Can support power off

This standby solution can only support IO interrupt wake-up of PMUIO0, PMUIO1 and PMUIO2.

In the standby state, at least the following four groups of power supplies should be kept turning on (refer to the power supply network name in the schematic):

- VCC\_DDR/VCC0V6\_DDR: Provide power for DDR self-refresh (DDR4: 2.5V power supply also needs power supply, LPDDR3/LPDDR4/LPDDR4x: 1.8V power supply also needs power supply);
- VDDA0V9\_PMU: Provide power for the logic of PMUIO0 & PMUIO1 & PMUIO2 power domain; It also provides power for PMUPLL and chip OSC work;
- VCCA1V8\_PMU: Provide power for PMUPLL work; provide IO power for PMUIO0 power domain to maintain output status and interrupt response;
- VCC3V3\_PMU: Provide IO power for PMUIO1 & PMUIO2 power domain to maintain output status and interrupt response;

In standby, if it need to supports USB HID device wake-up, the USB PHY power supply must remain powered; if it need to supports IO interrupt wake-up in VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7, VDD\_LOGIC and VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7 power supply must be kept.

# 2.2.2.2 PLL Power Supply

The PLL of RK3568 chip is distributed in two parts as follows:

	Power	Standby Mode
Inside the PMU unit	PMUPLL_AVDD_0V9、PMUPLL_AVDD_1V8	Can't turn off the power
Modules in the chip	SYSPLL_AVDD_0V9、SYSPLL_AVDD_1V8	Can turn off the power
nicht @ 2022 Deschahim Electronica Carled		

- PMUPLL\_AVDD\_0V9: Peak current 10mA
- PMUPLL\_AVDD\_1V8: Peak current 9mA
- SYSPLL\_AVDD\_0V9: Peak current 30mA
- SYSPLL\_AVDD\_1V8: Peak current 18mA

It is recommended to use LDO for power supply, PSRR@1KHz should be greater than 65dB, and the power supply capacity should be more than 200mA.

0.9V AC requirement: <20mV;

1.8V AC requirement: <50mV;

A stable PLL power supply will improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Refer to the schematic for the detailed number and capacity of the capacitors. Please do not change them at will.

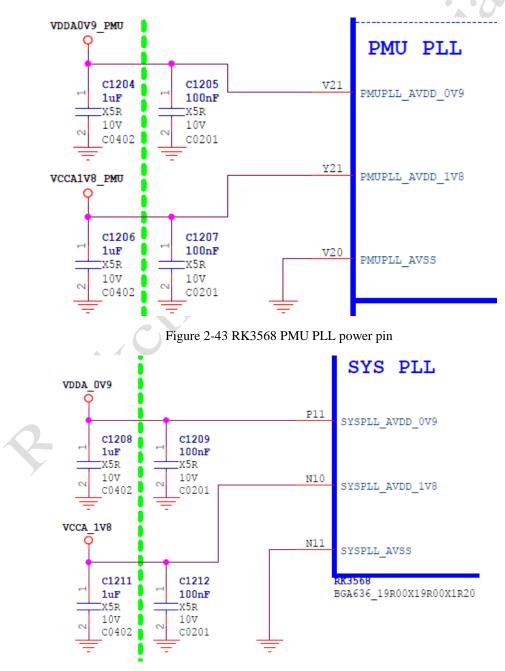


Figure 2-44 RK3568 SYS PLL power pin

The PMU\_VDD\_LOGIC\_0V9 power supply of RK3568 supplies the LOGIC of the internal PMU unit with a peak current of 50mA. Please do not delete the decoupling capacitor in the RK3568 chip reference schematic.

DC/DC or LDO can be used for power supply. From the cost considerations, it can work with

PMUPLL\_AVDD\_0V9 power supply together.

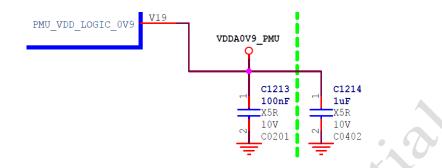


Figure 2-45 RK3568 PMU\_VDD\_LOGIC\_0V9 power pin

## 2.2.2.4 CPU Power Supply

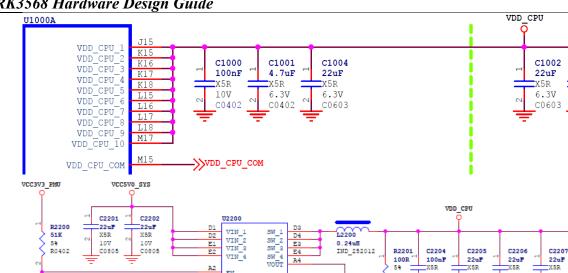
The VDD\_CPU power of RK3568 supplies power to the internal ARM Cortex-A55 core, which is independently powered by DC/DC power supply and supports dynamic frequency and voltage regulation function. The peak current can reach more than 3A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 4A;
- The output voltage accuracy is required at  $\pm 1.5\%$ ;
- BUCK transient response requirements: I<sub>load</sub>=BUCK Max current\*10%~BUCK Max current\*80% jump, slope 1A/µs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1000, C1001, and C1004 capacitors in the figure below on the back of the RK3568 chip during layout. C1002 and C1003 should be as close as possible to RK3568. The total capacitance of the VDD\_CPU power supply must be greater than  $135\mu$ F (it is recommended to reserve one or two  $22\mu$ F capacitors, which cannot be connected by default), in order to ensure that the power supply ripple is within 80mV, then avoid large power supply ripples under heavy load conditions.

The VDD\_CPU\_COM signal is the VDD\_CPU power feedback pin, which needs to be connected to the FB of the DC/DC power supply, which can effectively improve the voltage drop caused by PCB routing and improve the timeliness of power dynamic adjustment.



vou

GND2

GND3

GND4

GND5

GND

CSP20\_1R96X1R56X0R66

EN

Β1 SDA

B4 AGNE

VSEI

SCL

TCS452

PMIC SLEEP

# **RK3568 Hardware Design Guide**

Figure 2-46 RK3568 VDD\_CPU power pin and power supply DC/DC

R0402

107

C0402

OUT

FB DCDC

6.3V C0603

6.37

C0603

6.37

C0603

Feedback from RK3568

### 2.2.2.5 GPU Power Supply

C2210 100nF X5R

C0402

107

The VDD GPU power of RK3568 supplies power to the internal GPU unit. It uses DC/DC power supply and supports dynamic frequency and voltage regulation. The peak current can reach 1.2A. Please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be  $\pm 1.5\%$ ;
- BUCK transient response requirements: Iload=BUCK Max current\*10%~BUCK Max current\*80% jump, slope  $1A/\mu s$ , ripple requirement within  $\pm 3\%$ ;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered. Place the C1012, C1013, and C1014 capacitors in the figure below on the back of the RK3568 chip during

layout. C1015 and C1016 should be as close as possible to RK3568. The total capacitance of the VDD CPU power supply need to be greater than  $90\mu$ F, in order to ensure that the power supply ripple is within 60mV, and avoid large power supply ripples under heavy load conditions.

**Rev V1.2** 

C1003

22uF

X5R

6.3V

C0603

C2208

22**uF** X5R

6.37 0

VDD

RK3568

C0603

0

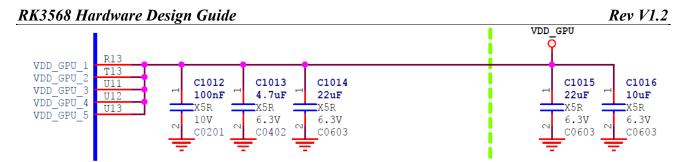


Figure 2-47 RK3568 VDD\_GPU power pin

### 2.2.2.6 NPU Power Supply

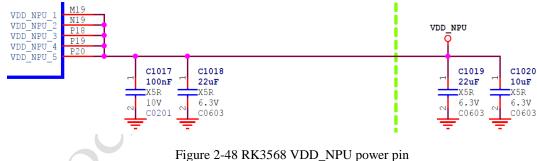
The VDD\_NPU power of RK3568 supplies the internal NPU unit with DC/DC power supply and supports dynamic frequency and voltage regulation. The peak current can reach 1A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be  $\pm 1.5\%$ ;
- BUCK transient response requirements: I<sub>load</sub>=BUCK Max current\*10%~BUCK Max current\*80% jump, slope 1A/µs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1017 and C1018 capacitors in the figure below on the back of the RK3568 chip during layout.

C1019 and C1020 should be as close as possible to RK3568. The total capacitance of the VDD\_CPU power supply need to be greater than  $90\mu$ F, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.



#### 2.2.2.7 Logic Power Supply

The VDD\_LOGIC power of RK3568 supplies power to the internal logic unit. It uses a DC/DC power supply for independent power supply, which can support dynamic frequency and voltage regulation, and the default fixed voltage for power supply. The peak current can reach 1A, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2A;
- The output voltage accuracy is required to be  $\pm 1.5\%$ ;
- BUCK transient response requirements: I<sub>load</sub>=BUCK Max current\*10%~BUCK Max current\*80% jump, slope 1A/µs, ripple requirement within ±3%;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

Place the C1005, C1006, C1007 and C1008 capacitors in the figure below on the back of the RK3568 chip during layout. C1010 and C1011 should be as close as possible to RK3568. The total capacitance of the VDD\_LOGIC power supply need to be greater than 90µF, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

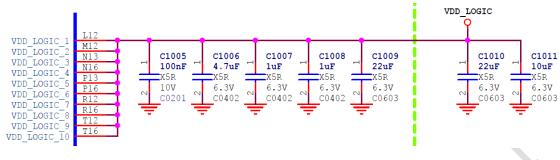


Figure 2-49 RK3568 VDD\_LOGIC power pin

#### 2.2.2.8 DDR Power Supply

The DDR PHY interface of RK3568 chip supports DDR3/DDR3L/DDR4/LPDDR4/LPDDR4x level standards. RK3568 DDR PHY has two power supplies, DDRPHY\_VDDQ and DDRPHY\_VDDQL. For power supply introduction, please refer to Section **2.1.7.5 DDR power supply design and power-on sequence requirements**. When designing a product, please confirm whether it meets the design requirements according to the use of DDR.

Similarly, use DC/DC for power supply; different DDR with different peak current, please evaluate the peak current according to the actual selected DDR. For a single LPDDR3 or a single LPDDR4 or a single LPDDR4x or two 16bit DDR3/3L or two 16bit DDR4, 1A DC/DC can be selected; for more than two DDR3 or DDR4, it is recommended to use a DC/DC above 2A. In addition, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

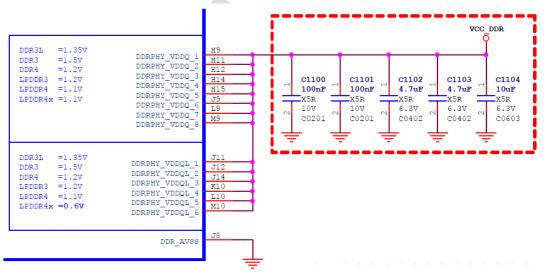


Figure 2-50 RK3568 VCC\_DDR power pin in DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 mode

Place the C1100, C1101, C1102, C1103 and C1104 capacitors in the figure above on the back of the RK3568 chip during layout, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

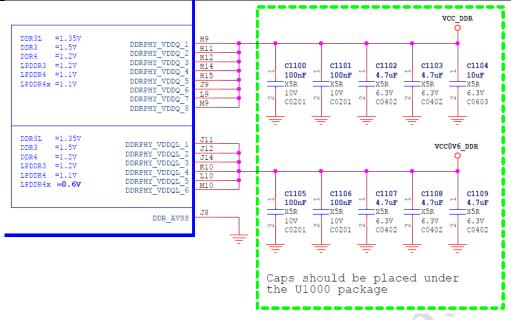


Figure 2-51 RK3568 VCC\_DDR and VCC0V6\_DDR power pins in LPDDR4x mode

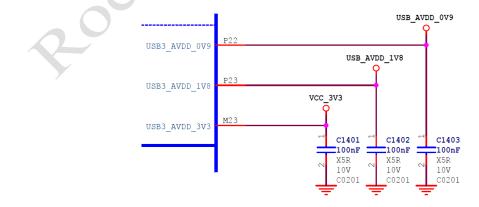
Place the C1100, C1101, C1102, C1103, C1104, C1105, C1106, C1107, C1108 and C1109 capacitors in the figure above on the back of the RK3568 chip during layout, in order to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

### 2.2.2.9 USB2.0 PHY Power Supply

RK3568 has four USB2.0 interfaces, and USB3\_OTG0\_DP/M, USB3\_HOST1\_DP/M with MULTI\_PHY0, MULTI\_PHY1 can form a USB3.0 interface. For details, please refer to **Section 2.3.4 USB2.0/USB3.0 Circuit**.

The USB3\_AVDD\_0V9, USB3\_AVDD\_1V8, USB3\_AVDD\_3V3 supply power to the USB3\_OTG0\_DP/M and USB3\_HOST1\_DP/M PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 reference schematic.

The USB2\_AVDD\_0V9, USB2\_AVDD\_1V8, and USB2\_AVDD\_3V3 supplies power to the USB2\_HOST2\_DP/M and USB2\_HOST3\_DP/M PHY. Please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.



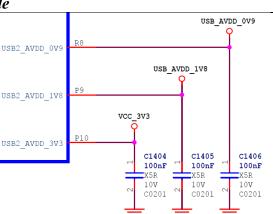


Figure 2-52 RK3568 USB2.0 PHY power pin

- USB3\_AVDD\_0V9: Peak current 5mA
- USB3\_AVDD\_1V8: Peak current 30mA
- USB3\_AVDD\_3V3: Peak current 10mA
- USB2\_AVDD\_0V9: Peak current 5mA
- USB2\_AVDD\_1V8: Peak current 30mA
- USB2\_AVDD\_3V3: Peak current 10mA

It is recommended to use LDO for power supply, PSRR@1KHz should be greater than 65dB, and the power supply capacity should be more than 200mA.

- 0.9 V AC requirement: <25 mV;
- 1.8V AC requirement: <50mV;
- 3.3V AC requirement: <200mV;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

Since the firmware of the RK3568 chip must be downloaded from the USB3\_OTG0\_DP/M interface, USB3 AVDD 0V9, USB3 AVDD 1V8, USB3 AVDD 3V3 must be powered in the first time power-on.

If USB2\_HOST2\_DP/M and USB2\_HOST3\_DP/M are not used, then USB2\_AVDD\_0V9, USB2\_AVDD\_1V8, USB2\_AVDD\_3V3 could be unpowered, and they are recommended to be grounded. But attention please: when the PHY is not powered, if the USB controller node corresponding to PHY in the kernel DTS is not disabled, it will cause to be stuck in the initialization of the USB controller during kernel initialization.

#### 2.2.2.10 MULTI PHY Power Supply

The RK3568 has three MULTI PHY interfaces:

MULTI\_PHY0 is the function multiplexing of USB3.0 OTG0 SS signal and SATA0;

MULTI\_PHY1 is the function multiplexing of USB3.0 HOST1 SS signal, SATA1 and QSGMII\_M0;

MULTI\_PHY2 is the function multiplexing of PCIe2.0, SATA2 and QSGMII\_M1;

MULTI\_PHY\_AVDD\_0V9\_1, MULTI\_PHY\_AVDD\_0V9\_2 and MULTI\_PHY\_AVDD\_1V8 supply power to MULTI\_PHY0, 1, 2, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

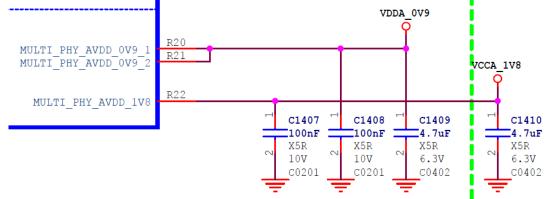


Figure 2-53 RK3568 MULTI\_PHY power pin

- MULTI\_PHY\_AVDD\_0V9: Peak current 150mA
- MULTI\_PHY\_AVDD\_1V8: Peak current 21mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MULTI\_PHY0/1/2 functions are not used, then MULTI\_PHY\_AVDD\_0V9 and MULTI\_PHY\_AVDD\_1V8 can be powered off, and grounding is recommended.

### 2.2.2.11 PCIe3.0 PHY Power Supply

The RK3568 has a PCIe3.0 interface.

PCIE30\_AVDD\_0V9\_1, PCIE30\_AVDD\_0V9\_2, and PCIE30\_AVDD\_1V8 supply power to PCIe3.0 PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

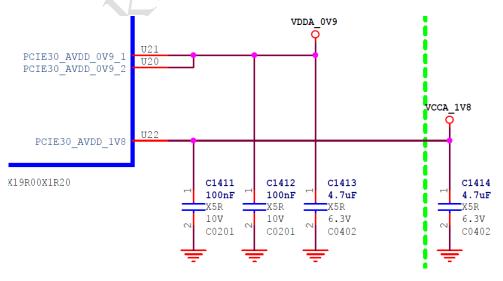


Figure 2-54 RK3568 PCIe3.0 PHY power pin

■ PCIE30\_AVDD\_0V9: Peak current 160mA

- PCIE30\_AVDD\_1V8: Peak current 60mA
- It is recommended to use LDO for power supply,
- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be

placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the PCIe3.0 function is not used, then PCIE30\_AVDD\_0V9 and PCIE30\_AVDD\_1V8 do not need to be powered. Grounding is recommended.

### 2.2.2.12 MIPI CSI RX PHY Power Supply

The RK3568 has a MIPI CSI RX interface.

MIPI\_CSI\_RX\_AVDD\_0V9, and MIPI\_CSI\_RX\_AVDD\_1V8 supply power to MIPI CSI RX PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

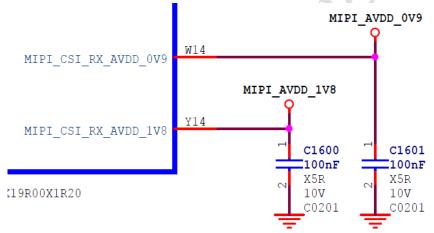


Figure 2-55 RK3568 MIPI CSI RX PHY power pin

- MIPI\_CSI\_RX\_AVDD\_0V9: Peak current 10mA
- MIPI\_CSI\_RX\_AVDD\_1V8: Peak current 2.5mA
  - It is recommended to use LDO for power supply,
- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI CSI RX function is not used, MIPI\_CSI\_RX\_AVDD\_0V9 and MIPI\_CSI\_RX\_AVDD\_1V8 can be unpowered, and grounding is recommended.

# 2.2.2.13 MIPI DSI TX0/LVDS PHY Power Supply

The RK3568 has a MIPI DSI TX0 and a LVDS TX Combo PHY interface.

MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9 and MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_1V8 supply power to MIPI DSI TX0 and LVDS TX Combo PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

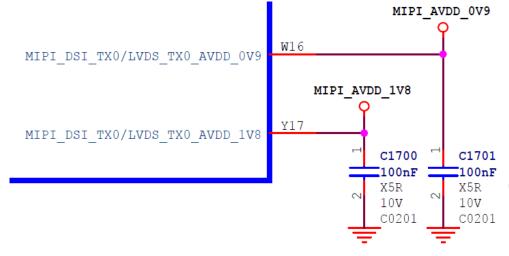


Figure 2-56 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY power pin

- MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9: Peak current 50mA
- MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_1V8: Peak current 15mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be

placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI DSI TX0 and LVDS TX functions are not used, MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9 and MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_1V8 can be powered off, and grounding is recommended.

# 2.2.2.14 MIPI DSI TX1 PHY Power Supply

The RK3568 has a MIPI DSI TX1 PHY interface.

MIPI\_DSI\_TX1\_AVDD\_0V9, and MIPI\_DSI\_TX1\_AVDD\_1V8 power supplies which supply power to MIPI DSI TX1 PHY, please do not delete the magnetic beads and decoupling capacitors in the RK3568 chip reference schematic.

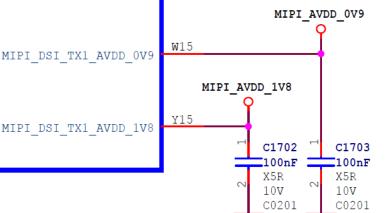


Figure 2-57 RK3568 MIPI DSI TX1 PHY power pin

- MIPI\_DSI\_TX1\_AVDD\_0V9: Peak current 50mA
- MIPI\_DSI\_TX1\_AVDD\_1V8: Peak current 15mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If MIPI DSI TX1 function is not used, MIPI\_DSI\_TX1\_AVDD\_0V9 and MIPI\_DSI\_TX1\_AVDD\_1V8 can be powered off, and grounding is recommended.

### 2.2.2.15 eDP PHY Power Supply

The RK3568 has an eDP TX PHY interface.

eDP\_TX\_AVDD\_0V9 and eDP\_TX\_AVDD\_1V8 supply power to eDP TX PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

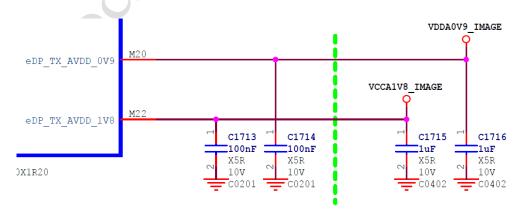


Figure 2-58 RK3568 eDP TX PHY power pin

- eDP TX AVDD 0V9: Peak current 150mA
- eDP\_TX\_AVDD\_1V8: Peak current 100mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mVpower supply capacity above 250mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be

placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the eDP TX function is not used, then eDP\_TX\_AVDD\_0V9 and eDP\_TX\_AVDD\_1V8 do not need to be powered, and grounding is recommended.

### 2.2.2.16 HDMI2.0 PHY Power Supply

The RK3568 has an HDMI2.0 TX PHY interface.

HDMI\_TX\_AVDD\_0V9\_1, HDMI\_TX\_AVDD\_0V9\_2 and HDMI\_TX\_AVDD\_1V8 supply power to

HDMI2.0 TX PHY, please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

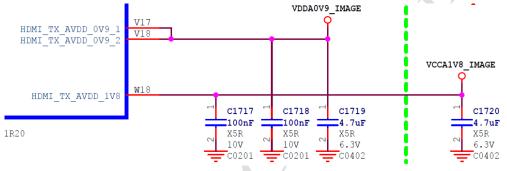


Figure 2-59 RK3568 HDMI2.0 TX PHY power pin

- HDMI\_TX\_AVDD\_0V9: Peak current 25mA
- HDMI TX AVDD 1V8: Peak current 16mA

It is recommended to use LDO for power supply,

- PSRR@1KHz need to >65dB;
- 0.9V AC requirement: <20mV, power supply capacity above 200mA;
- 1.8V AC requirement: <50mV, power supply capacity above 200mA;

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

If the HDMI2.0 TX function is not used, then HDMI\_TX\_AVDD\_0V9 and HDMI\_TX\_AVDD\_1V8 do not need to be powered, they are recommended to be grounded.

#### 2.2.2.17 SARADC/OTP Power Supply

The RK3568 has a SARADC, which can support 8 channels. SARADC\_AVDD\_1V8 supplies power to SARADC. Please do not delete the decoupling capacitors in the RK3568 chip reference schematic.

■ SARADC\_AVDD\_1V8: Peak current 1.5mA

It is recommended to use LDO for power supply,

**PSRR**@1KHz should >65dB;

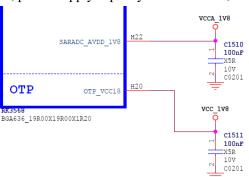


Figure 2-60 RK3568 SARADC and OTP power pin

The RK3568 has an OTP, OTP VCC18 supplies power to OTP, please do not delete the capacitor in the RK3568 chip reference schematic.

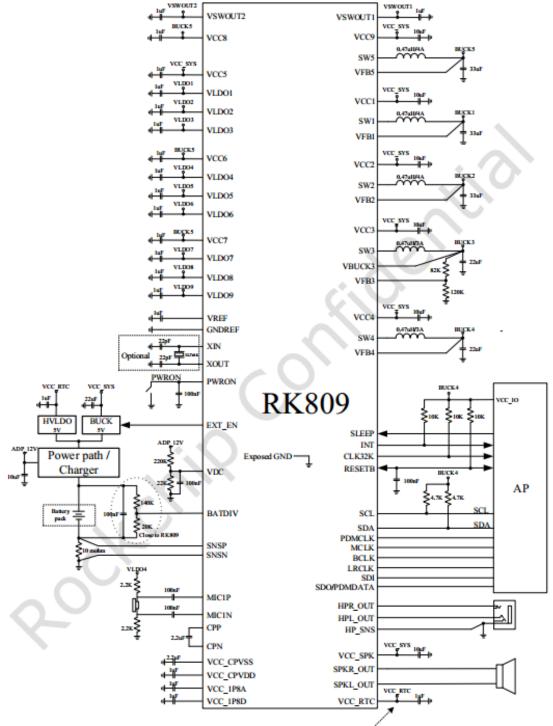
■ OTP VCC18: Peak current 59mA

LDO or DC/DC can be used to supply power to OTP.

A stable power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic for the detailed number and capacity of the capacitors. Please do not change at will.

# 2.2.3 RK809-5 Solution Introduction

#### 2.2.3.1 RK809-5 Block Diagram



VCC\_RTC must be the highest voltage in the RK809

Figure 2-61 RK809-5 block diagram

#### 2.2.3.2 RK809-5 Features

- Power input range: 2.7V-5.5V
- Accurate fuel gauge with two ADC of separate battery voltage and current
- Built-in real-time clock (RTC)
- Very low standby current of 35uA (at 32KHz clock frequency)

Copyright © 2022 Rockchip Electronics Co., Ltd.

#### **RK3568 Hardware Design Guide**

- Support real ground class-AB PA to drive Head-phone
- 1.3W Class-D power amplifier without filter inductor
- Fixed and programmable optional power start sequence control
- Built-in high-performance audio codec
  - Built-in independent PLL
  - Support microphone input
  - ♦ Both DAC and ADC support I2S digital input
  - Support ALC, limiter and noise gate
  - Support programmable digital and analog gain
  - Support 16bits-32bits bit rate
  - Sampling rate up to 192kHz
  - The software supports two working mode configurations of master and slave
  - Support three I2S formats (standard, left-aligned, right-aligned)
  - Support PDM mode (external input PCLK)
- Power channels:
  - ♦ BUCK1: Synchronous step-down DC-DC converter, 2.5A max
  - ♦ BUCK2: Synchronous step-down DC-DC converter, 2.5A max
  - ♦ BUCK3: Synchronous step-down DC-DC converter, 1.5A max
  - ♦ BUCK4: Synchronous step-down DC-DC converter, 1.5A max
  - ♦ BUCK5: Synchronous step-down DC-DC converter, 2.5A max
  - LDO1-LDO2, LDO4~LDO9: Low-dropout linear regulator, 400mA max
  - ◆ LDO3: Low-noise and high PSRR low-dropout linear regulator, 100mA max
  - Switch1: Switch, 2.1A max, Rdson=90 mohm
  - Switch2: Switch, 2.1A max, Rdson=100 mohm
- Package: 7mmx7mm QFN68

2.2.3.3 RK3568+RK809-5 Power Tree

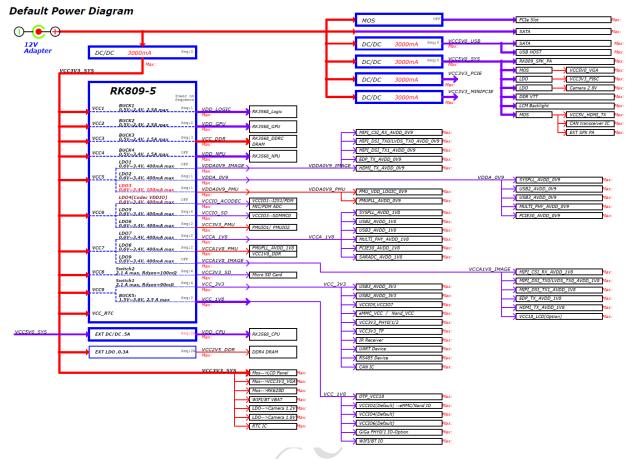


Figure 2-62 RK3568 and RK809-5 power tree

#### 2.2.3.4 RK809-5 Power-on Sequence

The power-on sequence of RK809-5 has been solidified and cannot be changed. Note that the power-on sequence of RK809-1, RK809-2 and RK809-3, and cannot be mixed.

VCC12V_DCIN	
VCC3V3_SYS	
VCC5V0_SYS	
VCC5V0_USB	
VDDA0V9_PMU	
VDDA_0V9	
VDD_LOGIC	
VDD_GPU	
VCCA1V8_PMU	
VCCA_1V8	
VCC_1V8	
VCC3V3_PMU	
VCC2V5_DDR	
VDD_CPU	
VCC_DDR	
VCC_3V3	
VCCIO_SD	
VCC3V3_SD	
RESETn	
VDD_NPU	
VDDA0V9_IMAGE	
VCCA1V8_IMAGE	
VCCIO_ACODEC	

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ΟΝ	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
	RK809_LD01	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
-	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LD05	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
_	RK809_LDO6	0.4A	VCC3V3_РМU	Slot:2	3.3V	ON	3.3V	TBD	TBD
	RK809_LD07	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
VCC3V3_SYS	RK809_LD08	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ΟΝ	1.8V	TBD	TBD
-	RK809_LD09	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3 SYS	<b>RK809_SW1</b> 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ΟΝ	3.3V	TBD	TBD
VCC3V3_373	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ΟΝ	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ΟΝ	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ΟΝ	2.5V	TBD	TBD

Figure 2-63 RK809-5 power-on sequence

2.2.3.5 Notices of RK809-5

Please select the load capacitance of 32.768KHz crystal according to the CL capacitance value of the crystal actually used. It is recommended to choose the capacitance not less than 18pF. If the load capacitance is too low, it may cause unstable start-up. The recommended value is 22pF.

# Mote

In order to reduce the power consumption, the crystal oscillation of the PMIC RTC is relatively weak. Using an ordinary oscilloscope on the XOUT or XIN pins cannot detect the oscillation signal, or the oscilloscope probe will stop oscillation when it touches it. Please test the CLK32K pin for the 32.768k signal.

- VCC\_RTC (Pin45) of RK809-5: It is the internal digital logic, part of analog control and RTC clock power supply pin of RK809 chip. The design of this pin requires that the power supply voltage must be the highest voltage among all the power supply pins of RK809-5 or be greater than Vmax-0.3V (except for VCC\_SPK\_HP power supply), so VCC\_RTC must be powered on first, or powered on together with other power supplies. It is not allowed to supply other power sources before VCC\_RTC. It is recommended to connect the same power supply with VCC9 (Pin54) of RK809-5;
- If you need button batteries to save the real-time clock, it is recommended to use an external RTC IC. The RTC current of RK809-5 is about 35~50µA, and when an external RTC IC is used as the real-time clock, and you need time alarm clock PowerOn function, please contact Rockchip to provide the reference circuit. The built-in RTC of RK809-5 supports time alarm clock PowerOn function. To use an external RTC IC, you must confirm whether its IO level matches the power supply voltage of the RTC chip;
- Pin 67 (RESETB) of RK809-5 needs a 100nF capacitor to improve the anti-interference ability and cannot be deleted at will.
- The SDA\SCL\INT\CLK32K\RESETB GPIOs of PMIC RK809-5 are open-drain output, and their highest allowable input voltage is the voltage of VCC\_RTC, they need to add pull-up resistors externally or use the pull-up resistors inside RK3568 IO. SCL\SDA\SLEEP\PWRON\RESETB as input VL\VH are fixed to 0.4V\1.26V.
- If Gas Gauge is not used, it is recommended that Pin56 (BATDIV), Pin62 (SNSP), and Pin63 (SNSN) are grounded. If you want to enable it, please contact Rockchip to provide a reference circuit.
- I2S: The VCCIO of pin LRCK\BCLK\MCLK\SDI\PDMCLK are connected to LDO4, so LDO4 is generally allocated to the power domain where the I2S of the controller is located for power supply at the same time.
- The DC-DC inductor reference value of RK809-5 is: inductance 0.47µH, saturation current above 3.5A, DCR less than 50mΩ (in order to achieve better conversion efficiency, it is recommended to choose DCR less than 20mΩ).
- The input capacitance of BUCK1/BUCK2 of RK809-5 must be greater than 10µF, and the output capacitance must be greater than 30µF to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- The input capacitance of BUCK3 of RK809-5 must be greater than 10µF, and the output capacitance must be greater than 30µF to ensure a better decoupling effect. The output voltage value is determined by the

external resistor, and the voltage value must be matched according to the DDR model used in the project. The reference voltage is 0.8V. Select the voltage-dividing resistor RH=(VBUCK3-0.8)\*RL/0.8, RH and RL are the voltage-dividing pull-up resistor and pull-down resistor respectively, the resistor value is recommended to be between  $10K\Omega$  and  $1M\Omega$ , and the accuracy is 1%. It is recommended to refer to the parameters provided by the reference design.

- The input capacitance of BUCK4 of RK809-5 must be greater than 10µF, and the output capacitance must be greater than 30µF to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- The input capacitance of BUCK5 of RK809-5 must be greater than  $10\mu$ F, and the output capacitance must be greater than  $33\mu$ F to ensure a better decoupling effect, especially in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;
- LDO power supply: VCC5\VCC6\VCC7 are the LDO power supply input pin, which support at least 2V input, but the output current will drop to 50% of the rated output when 2V is input.
- VCC9: is not only the power supply input pin of VSWOUT1 and BUCK5, but is also the chip under-voltage and over-voltage protection detection pin. If the voltage of VCC9 is lower than 3.0V after power-on, it will automatically shut down.
- RK809-5 power on and off conditions:

VDC boot process:

- VCC\_RTC has powered and must be greater than 3.0V;
- The value of VDC pin is higher than 0.55V, and the recommended value is about 1.2V;
- EXT\_EN outputs high level;
- ♦ VCC9 needs to exceed 3.0V within 1.5ms of EXT\_EN output high level, otherwise it will not turn

on;

• Start the power-on process, each DC/DC, LDO is powered on according to the sequence;

• After starting up, VDC can be pulled down or kept at high level without affecting the starting state. Power Key boot process:

- VCC\_RTC has be powered and must be greater than 3.0V;
- PWRON pin are pulled down by more than 500ms;
- ◆ EXT\_EN outputs high level;
- VCC9 needs to exceed 3.0V within 1.5ms of EXT\_EN output high level, otherwise it will not turn

on;

• Start the power-on process, each DC/DC, LDO is powered on according to the sequence.

Alarm boot process:

- VCC\_RTC has be powered and must be greater than 3.0V;
- Alarm timing time is up, and turn on the timing boot function;
- ◆ EXT\_EN outputs high level;
- VCC9 needs to exceed 3.0V within 1.5ms of EXT\_EN output high level, otherwise it will not turn

on;

• Start the power-on process, each DC/DC, LDO is powered on according to the sequence.

Shut down:

- VCC9 voltage is lower than the under voltage design value;
- I2C command shutdown;
- Over temperature protection shutdown (145 degrees);
- Press and hold Power Key for more than six seconds to force shutdown.

#### 2.2.3.6 RK809-5 Design Description

Please refer to RK PMIC related design document "AN\_RK809\_V1.1" for detailed design instructions of RK809-5.

#### 2.2.4 Discrete Power Supply Solution Introduction

#### 2.2.4.1 Power Tree of RK3568+Discrete Power ( Based NVR\_DEMO )

Mainly for products with low requirements of standby power.

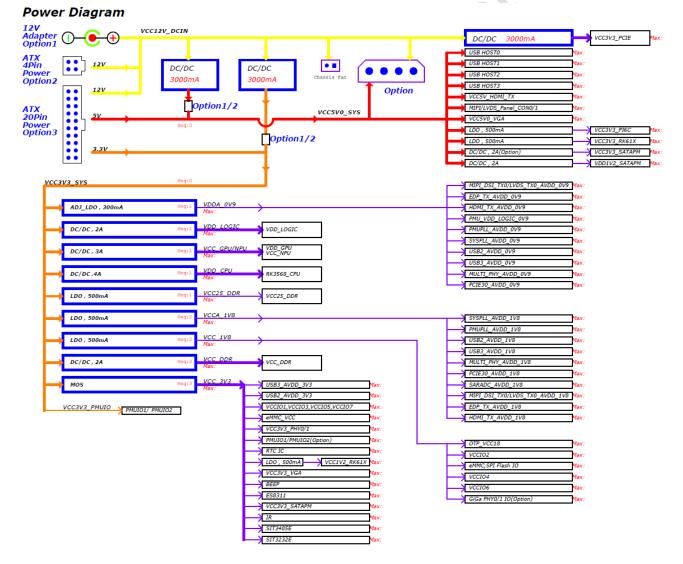


Figure 2-64 RK3568 + discrete power architecture

2.2.4.2 Power-on and Power-off Sequence of Discrete Power

VCC12V_DCIN		_			
	1			 	
VCC3V3_SYS					
VCC5V0_SYS				 	
VDDA_0V9		Γ			
VDD_LOGIC		Γ			
VDD_GPU/NPU		Γ			
VDD_CPU		Γ			
VCC2V5_DDR		Γ			
VCCA_1V8					
VCC_1V8					
VCC_DDR					
VCC_3V3			$ \  \  \  \  \  \  \  \  \  \  \  \  \ $		
RESETn					

Figure 2-65 Discrete power power-on sequence

The power-on sequence of each power supply of RK3568 chip: in theory, follow the low-voltage first, high-voltage second, and after the last one voltage is stable, RESETn can be released after at least 10ms;

Power Seauence

Power-off sequence: During power-off, RESETn must be pulled down first, and then each power supply can be powered off. If there is a product that needs to be powered on and off quickly, pay attention to the discharge time of the capacitor. If the power is not completely powered off and then powered on again, it may cause the system to work abnormally; In addition, if you use SPI Flash, it is recommended to use a reset IC with a threshold of 2.93V, when the power supply of the SPI Flash drops to 2.93V, the reset must be pulled low first to prevent the SPI Flash data error caused by the out-of-control and disoperation of the under-voltage logic during the power down process.

#### 2.2.4.3 Notices of Discrete Power Supply

■ VDD\_CPU uses dynamic voltage and frequency regulation. It is not recommended to use together with other power supplies. Please refer to the reference design for BUCK model requirements, and using I2C voltage regulation. If you have to replace with other models, the BUCK with a power supply capacity of ≥4A can be selected. If it is not I2C voltage regulation, PWM can be used for voltage regulation. Please refer to the reference design for voltage regulation parameters, the voltage regulation range is 0.8-1.2V, and the default voltage is about 0.938V (note that the software configuration must be filled in according to actual values, otherwise, inaccurate voltage regulation will occur).

Other requirements of BUCK are as follows:

1) The output voltage accuracy is required to be  $\pm 1.5\%$ ;

2) BUCK transient response requirements:  $I_{load}$ =BUCK Max current\*10%-BUCK Max current\*80% jump, slope 1A/µs, ripple requirement within ±5%.

The input capacitance of BUCK must be greater than  $22\mu$ F, and the output capacitor has to meet the requirement of VDD\_CPU power supply with a total capacitance greater than  $135\mu$ F (it is recommended to reserve one or two  $22\mu$ F capacitors, which can be leave floating by default), to ensure that the power supply ripple is within

80mV, then avoid large power supply ripples under heavy load conditions

VDD\_GPU and VDD\_NPU adopt dynamic voltage and frequency regulation, they can be used together for power supply according to different cases, and for example, when it is not sensitive to working power consumption. Please refer to the reference design for selecting BUCK models. If you have to replace with other models, the power supply capacity of the BUCK should be ≥3A and use PWM for voltage regulation, please refer to the reference design for voltage regulation parameters, the voltage regulation range is 0.81-1.1V, and the default voltage is about 0.92V (note that the software configuration must be filled in according to the actual values, otherwise, inaccurate voltage regulation will occur).

Other requirements of BUCK are as follows:

1) The output voltage accuracy is required to be  $\pm 1.5\%$ ;

2) BUCK transient response requirements: Iload=BUCK Max current\*10%-BUCK Max current\*80% jump, slope  $1A/\mu s$ , ripple requirement within  $\pm 5\%$ .

The input capacitance of BUCK must be greater than  $10\mu$ F, and the output capacitor should meet the requirement of VDD\_GPU and VDD\_NPU power supply with a total capacitance greater than  $135\mu$ F (it is recommended to reserve one or two  $22\mu$ F capacitors, which cannot be attached by default), to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

■ VDD\_LOGIC defaults to a fixed voltage of about 0.92V, and it is reserved for dynamic voltage adjustment. It is not recommended to combine with other power supplies. The BUCK model requires refer to the reference design. If you need to replace other models, you need to select a BUCK with a power supply capacity of ≥1.5A, reserved PWM voltage regulation, the voltage regulation parameters can refer to the reference design, the voltage adjustment range is 0.81-1.0V, and the default voltage is about 0.92V (note that the software configuration must be filled in according to the actual, otherwise the voltage adjustment problem will be inaccurate).

Other requirements of BUCK are as follows:

1) The output voltage accuracy is required to be  $\pm 1.5\%$ ;

2) BUCK transient response requirements: Iload=BUCK Max current\*10%-BUCK Max current\*80% jump, slope  $1A/\mu s$ , ripple requirement within  $\pm 5\%$ .

The input capacitance of BUCK must be greater than  $10\mu$ F, and the output capacitor needs to meet the requirement of VDD\_LOGIC power supply with a total capacitance greater than  $99\mu$ F (it is recommended to reserve 1-2 22 $\mu$ F capacitors, which can be hanged up by default), to ensure that the power supply ripple is within 60mV, then avoid large power supply ripples under heavy load conditions.

- VCC\_3V3 power-on sequence must meet the requirements, and the MOS control circuit is not allowed to be deleted;
- The reset IC must be an open-leakage output, which is active at low level. The power supply of the reset IC needs to be connected to VCC3V3 PMUIO, which is the same as the power supply of PMUIO1.

#### 2.2.5 Standby Control Circuit

If the product requires low-power standby, it is recommended to use the RK809-5 power supply solution. The following introduces the standby PMIC SLEEP control circuit using RK809-5:

#### **RK3568 Hardware Design Guide**

When the RK3568 chip is in the normal working mode, the state pin PMIC\_SLEEP of the chip will maintain a low level output.

When the system enters the standby mode, the PMIC\_SLEEP pin will output a high-level sleep indicator signal. At this time, the PMIC is controlled by the signal to enter the standby state. According to the configuration of the software dts file, part of the power supplies will be turned off, and some of the power supplies will be lowered.

When the system is awakened from the standby mode, the PMIC\_SLEEP pin will output a low level for the first time. At this time, the PMIC will resume the working state before standby and restore the power output of each channel.

PMIC\_SLEEP is a special function signal, please do not change the usage at will.

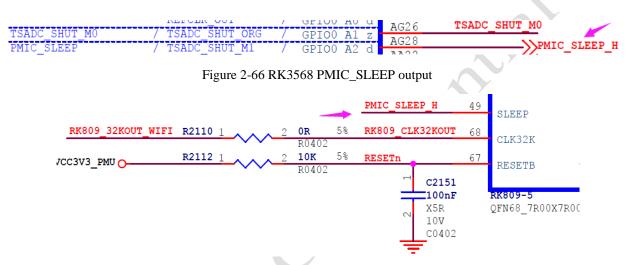


Figure 2-67 RK809-5 PMIC\_SLEEP input

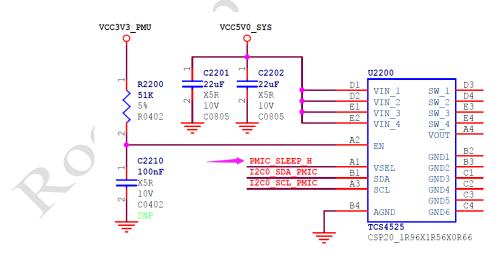


Figure 2-68 The PMIC\_SLEEP input of VDD\_CPU BUCK

#### 2.2.6 Power Peak Current Table

The following data is the peak current of each module, they are used for evaluating power supply solution and PCB Layout, and they are used for reference only.

Note: It cannot be simply added up as the peak current of SOC. Please evaluate the heat dissipation solution according to the average current of the actual scenes.

Power Name	Voltage (V)	Peak Current(mA)
PMUPLL_AVDD_0V9	0.9	10
PMUPLL_AVDD_1V8	1.8	9
SYSPLL_AVDD_0V9	0.9	30
SYSPLL_AVDD_1V8	1.8	18
PMU_VDD_LOGIC_0V9	0.9	50
VDD_CPU	DVFS	3000
VDD_GPU	DVFS	1200
VDD_NPU	DVFS	1000
VDD_LOGIC	0.9	1200
DDRPHY_VDDQ	1.1/1.2/1.35/1.5	TBD
DDRPHY_VDDQL	0.6/1.1/1.2/1.35/1.5	TBD
USB3_AVDD_0V9	0.9	5
USB3_AVDD_1V8	1.8	30
USB3_AVDD_3V3	3.3	10
USB2_AVDD_0V9	0.9	5
USB2_AVDD_1V8	1.8	30
USB2_AVDD_3V3	3.3	10
MULTI_PHY_AVDD_0V9	0.9	150
MULTI_PHY_AVDD_1V8	1.8	21
PCIE30_AVDD_0V9	0.9	160
PCIE30_AVDD_1V8	1.8	60
MIPI_CSI_RX_AVDD_0V9	0.9	10
MIPI_CSI_RX_AVDD_1V8	1.8	2.5
MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9	0.9	50
MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8	1.8	15
MIPI_DSI_TX1_AVDD_0V9	0.9	50
MIPI_DSI_TX1_AVDD_1V8	1.8	15
eDP_TX_AVDD_0V9	0.9	150
eDP_TX_AVDD_1V8	1.8	100
HDMI_TX_AVDD_0V9	0.9	25
HDMI_TX_AVDD_1V8	1.8	16
SARADC_AVDD_1V8	1.8	1.5
OTP_VCC18	1.8	59
PMUI00	1.8	TBD
PMUIO1	3.3	TBD
PMUIO2/VCCIO1/2/3/4/5/6/7/	1.8/3.3	TBD

Table 2–14 RK3568 peak current table

# 2.3 Functional Interface Circuit Design Guide

# 2.3.1 SDMMC0/1/2

The RK3568 integrates three SDMMC controllers, all of which support SD V3.01 and MMC V4.51 protocols. SDMMC0 and SDMMC1 support up to 200MHz, and SDMMC2 only support up to 150MHz.

# 2.3.1.1 SDMMC0 Interface

- SDMMC0 interface is multiplexed in the VCCIO3 power domain;
- Support System Boot, default allocation of SD card function;
- SDMMC0 is multiplexed with JTAG and other functions, functions selection is realized through the state of SDMMC0 DET by default. Please refer to the introduction in the section 2.1.5 for details;
- VCCIO3 power supply, need external 3.3V or 1.8V power supply,

When connecting an SD card: if it only supports SD2.0 mode: it can directly supply 3.3V power; If you want to support SD3.0 mode compatible with SD2.0 mode: default 3.3V power supply, after negotiating with SD card to run SD3.0 mode, the power supply voltage needs to be switched to 1.8V power supply, RK809-5 LDO5 supplies power to VCCIO3 alone, so this process can be achieved.

When connected a SDIO device: supply 1.8V or 3.3V according to the peripherals and the actual operating mode.

U1000J	
<b>VCCIO3 Domain</b> Operating Voltage=1.8V/3.3V	
SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1 / FWM8_M1 / GPI01_D5 SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1 / FWM9_M1 / GPI01_D6 SDMMC0_D2 / ARMJTAG_TCK / UART5_CTSn_M0 / GPI01_D7 SDMMC0_D3 / ARMJTAG_TMS / UART5_RTSn_M0 / GPI02_A0	и H26
SDMMC0_CMD / PWM10_M1 / UART5_RX_M0 / CAN0_TX_M1 / GPIO2_A1	H28
SDMMCO_CLK / TEST_CLKOUT / UART5_TX_M0 / CANO_RX_M1 / GPIO2_A2	<u>d</u>

BGA636 19R00X19R00X1R20

#### Figure 2-69 RK3568 SDMMC0 interface pin

- When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.
- When using SD card, pay attention to the following items:
  - The supply voltage of VDD pin of the SD card is 3.3V, and the decoupling capacitors are not allowed to be deleted. Place them close to the connector when layout.
  - SDMMC0\_D [3:0], SDMMC0\_CMD, SDMMC0\_CLK need to be connected to a 220hm resistor in

series, and SDMMC0\_DET to be connected to a 100ohm resistor in series;

You have to add ESD device when SDMMC0\_D [3:0], SDMMC0\_CMD, SDMMC0\_CLK, SDMMC0\_DET signals are close the SD card position. If it requires to support SD3.0 mode, the junction capacitance of the ESD device must be less than 1pF. And if it only requires to support SD2.0 mode, the junction capacitance of the ESD device can be extended to 9pF.

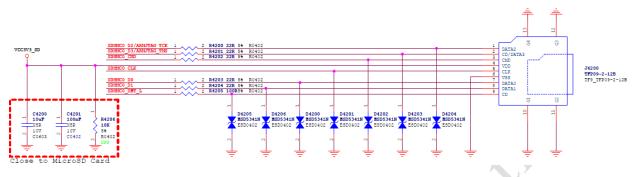


Figure 2-70 SD card interface circuit

 SDMMC0 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Signal	Internal pull-up and pull-down	Connection mode	Description (chipset)
SDMMC0_D[3:0]	pull up	connect a 220hm resistor in series, use the corresponding IO internal pull-up resistor	SD data send/receive
SDMMC0_CLK	pull down	connect a 220hm resistor in series	SD clock send
SDMMC0_CMD	pull up	connect a 220hm resistor in series, use the corresponding IO internal pull-up resistor	SD command send/receive
SDMMC0_DET	pull up	connect a 100ohm resistor in series, use the corresponding IO internal pull-up resistor	SD card insertion detection

Table 2-15 SDMMC0	interface design
-------------------	------------------

# 2.3.1.2 SDMMC1 Interface

- SDMMC1 interface is multiplexed in the VCCIO4 power domain;
- Does not support System Boot, default allocate to SDIO WIFI function;
- VCCIO4 power supply, supplies 1.8V or 3.3V according to the peripheral and the actual operating mode,

need to be consistent with the peripheral IO. For the SD card function, pay attention to the power domain voltage, the requirements same as SDMMC0;

DMMC1_D1			/ GPIO2 A3 u E28
	/ GMACO_RXD3	/ UART6 TX MO	/ GPIO2 A4 u p20
DMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0	/ GPIO2 A5 u C27
DMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0	/ GPIO2 A6 u
DMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0	/ GPIO2 A7 u C28
DMMC1 CLK	/ GMAC0 TXCLK	/ UART9 TX M0	/ GPIO2 B0 d D27
	***********************		D26
DMMC1_PWREN	/ I2C4 SDA M1	/ UART8 RTSn M0 / CAN2 RX M1	/ GPIO2 B1 d E25
DMMC1_DET	/ 12C4 SCL M1	/ UART8 CTSn M0 / CAN2 TX M1	/ GPIO2 B2 u
	GMAC0 TXD0	/ UART1 RX M0	/ GPIO2 B3 u F28
	GMACO TXD1	/ UART1 TX MO	GDT00 D4 - 627
	GMACO TXEN	/ UARTI RTSn M0 / SPI1 CLK M	G28
	GMACO RXD0	/ UART1 CTSn M0 / SPI1 CLK M	
2S2 SCLK RX M0	/ GMAC0 RXD1	/ UART6 RTSn M0 / SPI1 MOSI 1	M0 / GPIO2 B7 d H25
2S2 LRCK RX M0	/ GMACO RXDV CRS	/ UART6 CTSn M0 / SPII CS0 M	CDT02 CD 1 124
2S2_MCLK_M0	/ ETHO REFCLKO 25M	/ UART7_RTSn_M0 / SPI2_CLK_M	0 / GPI02 C0 d G23
			F25
2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0 / SPI2_MISO	H24
2S2_LRCK_TX_M0 2S2_SD0_M0	/ GMAC0_MDC	/ UART9_RTSn_M0 / SPI2_MOSI / UART9_CTSn_M0 / SPI2_CS0_M	M0 / GPIO2 C3 d H23
252_5D0_M0 252_5D1_M0	/ GMAC0_MDIO		0 / GPIO2 C4 d
2S2 SDI M0	/ GMACO RXER	/ UART8 TX M0 / SPI2 CS1 M	0 / GPIO2 C5 d
			E26

BGA636\_19R00X19R00X1R20

Figure 2-71 RK3568 SDMMC1 interface pin

SDMMC1 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Signal	Internal pull-up and pull-down	Connection mode	Description (chipset)
SDMMC1_D[3:0]	pull up	connect a 22ohm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor	SD data send/receive
SDMMC1_CLK	pull down	connect a 220hm resistor in series	SD clock send
SDMMC1_CMD	pull up	connection a 220hm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor	SD command send/receive

Table 2–16 SDMMC1 interface design

- When connecting SDIO WIFI, you need to consider a low-power standby solution, that is, when using VDD\_LOGIC standby and power-off solution, then the relevant control pins of SDIO WIFI need to be moved to the PMUIO1/2 power domain. After VDD\_LOGIC is powered off, the IO status of VCCIO1/2/3/4/5/6/7 power domain cannot be maintained.
- When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.

#### 2.3.1.3 SDMMC2 Interface

■ The SDMMC2 interface is multiplexed in two power domains, one is in the VCCIO5 power domain and

the other is in the VCCIO6 power domain. Only one of them can be used: either all using VCCIO5 power domain or all using VCCIO6 power domains; in other words, it is not supported that some using VCCIO5 power domain and the rest using VCCIO6 power domain;

- Does not support System Boot;
- Using VCCIO5 or VCCIO6 to supply 1.8V or 3.3V power according to the peripheral and the actual operating mode, and it should be consistent with the peripheral IO. For the SD card function, pay attention to the power domain voltage, please refer to SDMMC0 for detailed requirements;

CIF D0	orougo r.	8V/3.3V			
	/ EBC SDDO0	/ SDMMC2 D0 M0	/ 12s1 MCLK M1	/ VOP BT656 D0 M1 /	GPIO3 C6 d
CIF D1	/ EBC SDD01	/ SDMMC2 D1 M0	/ 12S1 SCLK TX M1	/ VOP BT656 D1 M1 /	GPI03 C7 d
CIF D2	/ EBC SDDO2	/ SDMMC2 D2 M0	/ I2S1 LRCK TX M1	/ VOP BT656 D2 M1 /	GPIO3 D0 d
CIF D3	/ EBC SDDO3	/ SEMMC2 D3 M0	/ 12S1 SDO0 M1	/ VOP BT656 D3 M1 /	GPIO3 D1 d
NIF D4	/ EBC SDDO4	/ SDMMC2 CMD M0	/ I2S1 SDI0 M1	/ VOP BT656 D4 M1 /	GPIO3 D2 d
IF D5	/ EBC SDD05	/ SDMMC2 CLK M0	/ I2S1 SDI1 M1	/ VOP BT656 D5 M1 /	GPIO3 D3 d
NIF D6	/ EBC SDDO6	/ SDMMC2 DET M0	/ I2S1 SDI2 M1	/ VOP BT656 D6 M1 /	GPIO3 D4 d
CIF D7	/ EBC SDD07	/ SDMMC2 FWREN M0	/ 12S1 SDI3 M1	/ VOP BT656 D7 M1 /	GPIO3 D5 d
SIF D8	/ EBC SDDO8	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLK0 M1 /	GPIO3 D6 d
CIF D9	/ EBC SDDO9	/ GMAC1 TXD3 M1	/ UART1 RX M1	/ PDM SDI0 M1 /	GPIO3 D7 d
SIF D10	/ EBC SDD010	/ GMAC1 TXCLK M1		/ PDM CLK1 M1 /	GPIO4 A0 d
CIF D11	/ EBC SDD011	/ GMAC1 RXD2 M1		/ PDM SDI1 M1 /	GPIO4 A1 d
CIF D12	/ EBC SDD012	/ GMAC1 RXD3 M1	/ UART7 TX M2	/ PDM SDI2 M1 /	GPIO4 A2 d
CIF D13	/ EBC SDD013	/ GMAC1 RXCLK M1	/ UART7 RX M2	/ PDM SDI3 M1 /	GPIO4 A3 d
CIF D14	/ EBC SDD014	/ GMAC1 TXD0 M1	/ UART9 TX M2	/ 1282 LRCK TX M1 /	GPIO4 A4 d
CIF D15	/ EBC SDD015	/ GMAC1 TXD1 M1	/ UART9 RX M2	/ 1282 LRCK RX M1 /	GPIO4 A5 d
ISP FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CS0 M0	/ 1251 SCLK RX M1 /	GPIO4 A6 d
	/ ====	( cup c1 . pyp0 . w1	( app2) do1 w0	/ T001 TD0T DV V1 /	CDT04 37 4
CAM CLKOUTO CAM CLKOUTI	/ EBC SDCE1 / EBC SDCE2	/ GMAC1 RXD0 M1 / GMAC1 RXD1 M1	/ SPI3 CS1 M0 / SPI3 MISO M0	/ 1281 LRCK RX M1 / / 1281 SD01 M1 /	GPIO4 A7 d GPIO4 B0 d
CAM CHROUIT	7 EBC SDCE2	/ GMACI KADI MI	/ 3F13 M130 M0	/ 1251 5001 MI /	GPI04 BU d
ISP PRELIGHT TRIG	/ EBC SDCE3	/ GMAC1 RXDV CRS M1		/ 1281 SDO2 M1 /	GPIO4 B1 d
12C4 SDA MO	/ EBC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI M0	/ 1282 SDI M1 /	GPIO4 B2 d
12C4 SCL M0	/ EBC GDOE	/ ETH1 REFCLKO 25M 1		/ 1282 SD1 M1 /	GP104 B2 d
1204 JOH M0	/ LDC GDOL	/ EIIII KEPCEKO ZOM I	11 / SF15 CBR NO	/ 1252 500 M1 /	0F104 55 G
12C2 SDA M1	/ EBC GDSP	/ CAN2 RX M0	/ ISP FLASH TRIGIN	/ VOP BT656 CLK M1/	GPIO4 B4 d
12C2 SCL M1	/ EBC SDSHR	/ CAN2 TX M0		/ 1281 SDO3 M1 /	GPIO4 B5 d
	/ EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ 1282 MCLK M1 /	GPIO4 B6 d
CIF HREF	/ EBC SDOE	/ GMAC1 MDIO M1		/ 1282 SCLK TX M1 /	GPIO4 B7 d
CIF HREF CIF VSYNC CIF CLKOUT	/ EBC GDCLK		/ PWM11 IR M1		GPIO4 C0 d
CIF VSYNC	/ EBC GDCLK		/ PWM11 IR M1	/	GPIO4 CO d

BGA636\_19R00X19R00X1R20

Figure 2-72 RK3568 SDMMC2 interface M0 functional pins

CDC D4	/ VOP BT656 D1 M0 / VOP BT656 D2 M0		/ PCIE20 CLKREQn M1 ,	/ 1281 MCLK M2 ,	/ GPIO2 D0 d
CDC D3 CDC D4	/ TOD DECEC DO NO	/ SPIO MOSI M1	/ PCIE20 WAKEn M1	/ 12S1 SCLK TX M2 ,	/ GPIO2 D1 d
CDC D3 CDC D4	/ VOP B1656 D2 M0	/ SPIO CSO M1	/ PCIE30X1 CLKREOn M1 /	/ 12S1 LRCK TX M2 ,	/ GPIO2 D2 d
	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ 12S1_SDI0_M2	/ GPIO2 D3 d
	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREOn M1 /	/ 1281 SDI1 M2 ,	/ GPIO2 D4 d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ 12S1_SD12_M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ 12S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2 ,	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UARTS RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D0	/ GMAC1 TXD2 M0		SDMMC2 D1 M1	GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0		SDMMC2 D2 M1	GP103 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ 1283 LRCK M0	SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ 1283 SDO M0	SDMMC2 CMD M1	GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ 1283 SDI M0	SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0		SDMMC2 DET M1 ,	GPIO3 A7 d
	/ VOP BT1120 D6	/ ETH1 REFCLKO 25M M0		SDMMC2 PWREN M1	GPIO3 B0 d
LCDC D15					6F105 B0 a
			/ IIAD#4 DV M1		
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0		/ PWMM8_MO	/ GPI03 B1 d
LCDC D16 LCDC D17	/ VOP BT1120 D7 / VOP BT1120 D8	/ GMAC1_RXD0_M0 / GMAC1_RXD1_M0	/ UART4 TX M1	/ PWM8_M0 / PWM9_M0	/ GPIO3 B1 d / GPIO3 B2 d
LCDC D16 LCDC D17 LCDC D18	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CRS M0	/ UART4 TX M1 / I2C5 SCL M0	/ PWM8 M0 / PWM9 M0 / PDM SDI0 M2	/ GPIO3 B1 d / GPIO3 B2 d / GPIO3 B3 d
LCDC D16 LCDC D17 LCDC D18 LCDC D19	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CRS M0 / GMAC1 RXDV CRS M0	/ UART4 TX M1 / I2C5 SCL M0 / I2C5 SDA M0	/ PWM8_M0 / PWM9_M0 / PDM_SDI0_M2 / PDM_SDI1_M2	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d / GPI03 B4 d
LCDC D16 LCDC D17 LCDC D18 LCDC D19 LCDC D20	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D11	/ GMACI RXD0 M0 / GMACI RXDI M0 / GMACI RXDV CRS M0 / GMACI RXDV CRS M0 / GMACI RXDV M0	/ UART4 TX M1 / I2C5 SCL M0 / I2C5 SDA M0 / I2C3 SCL M1	/ FWM8_M0 / FWM9_M0 / PDM_SDI0_M2 / FDM_SDI1_M2 / FDM_SDI1_M2 / FWM10_M0	/ GPIO3 B1 d GPIO3 B2 d / GPIO3 B3 d / GPIO3 B4 d / GPIO3 B5 d
LCDC D16 LCDC D17 LCDC D18 LCDC D19 LCDC D20 LCDC D21	/ VOF BT1120 D7 / VOF BT1120 D8 / VOF BT1120 D9 / VOF BT1120 D10 / VOF BT1120 D11 / VOF BT1120 D12	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CRS M0 / GMAC1 RXDV CRS M0	/ UART4 TX M1 / I2C5 SCL M0 / I2C5 SDA M0 / I2C3 SCL M1	/ FWM8 M0 / FWM9 M0 / FDM SDIO M2 / FDM SDII M2 / FVM10 M0 / FWM11 IR M0	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d / GPI03 B4 d
LEDC D15 LEDC D16 LEDC D17 LEDC D17 LEDC D19 LEDC D20 LEDC D21 LEDC D21 LEDC D22 LEDC D23	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D11	/ GNAC1 RKD0 M0 / GNAC1 RKD1 M0 / GNAC1 RKDV CRS M0 / GNAC1 RKER M0 / GNAC1 RKD0 M0 / GNAC1 TKD1 M0	/ UART4 TX M1 / I2C5 SCL M0 / I2C5 SDA M0 / I2C3 SCL M1 / I2C3 SDA M1 / UART3 TX M1	/ FWM8_M0 / FWM9_M0 / PDM_SDI0_M2 / FDM_SDI1_M2 / FDM_SDI1_M2 / FWM10_M0	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d / GPI03 B4 d / GPI03 B5 d / GPI03 B6 d
LCDC D16 LCDC D17 LCDC D18 LCDC D18 LCDC D19 LCDC D20 LCDC D21 LCDC D22 LCDC D23	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D10 / VOP BT1120 D11 / VOP BT1120 D12 / PWM12 M0	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CR8 M0 / GMAC1 RXDV CR8 M0 / GMAC1 TXD0 M0 / GMAC1 TXD0 M0 / GMAC1 TXD1 M0 / GMAC1 TXDN M0	/ UART4 TX M1 / 12C5 SCL M0 / 12C5 SDA M0 / 12C3 SCL M1 / 12C3 SCL M1 / 12C3 SDA M1 / UART3 TX M1 / UART3 TX M1	PWM8_M0 PDM SDIO M2 PDM SDIO M2 PWM10 M0 PWM10 M0 PWM11 IR M0 PDM SDI2 M2	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d / GPI03 B4 d / GPI03 B5 d / GPI03 B7 d / GPI03 B7 d / GPI03 C1 d
LCDC D16 LCDC D17 LCDC D18 LCDC D19 LCDC D20 LCDC D21 LCDC D22 LCDC D23 LCDC D23 LCDC HSYNC	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D10 / VOP BT1120 D11 / VOP BT1120 D12 / FMM12 M0 / FMM13 M0	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CR8 M0 / GMAC1 RXDV CR8 M0 / GMAC1 RXDF M0 / GMAC1 RXDF M0 / GMAC1 TXD1 M0 / GMAC1 TXD1 M0 / GMAC1 MCLKINOUT M0	/ UART4 TX M1 / 12C5 SCT M0 / 12C5 SDA M0 / 12C3 SDA M0 / 12C3 SDA M1 / UART3 TX M1 / UART3 TX M1 / UART3 RK M1 / PCIE20 PERSTA M1	/ FWNS MO / FWNS MO / FDM SDIO M2 / FDM SDII M2 / FWNI MO / FWNI MO / FWNI IR MO / FDM SDI2 M2 / FDM SDI3 M2	/ GPI03 B1 d GPI03 B2 d / GPI03 B3 d / GPI03 B4 d / GPI03 B5 d / GPI03 B5 d / GPI03 B7 d / GPI03 C0 d
LCDC D16 LCDC D17 LCDC D18 LCDC D18 LCDC D19 LCDC D20 LCDC D21 LCDC D22 LCDC D22 LCDC HSYNC LCDC HSYNC	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D11 / VOP BT1120 D11 / VOP BT1120 D12 / FWM13 M0 / VOP BT1120 D13	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CRS M0 / GMAC1 RXDR M0 / GMAC1 TXD0 M0 / GMAC1 TXD1 M0 / GMAC1 TXD1 M0 / GMAC1 TXEN M0 / GMAC1 MCLKINGUT M0 / SPI1 MOSI M1	/ UART4 TX M1 / 12C5 SCT M0 / 12C5 SDA M0 / 12C3 SDA M0 / 12C3 SDA M1 / UART3 TX M1 / UART3 TX M1 / UART3 RK M1 / PCIE20 PERSTA M1	/ FWN8 M0 / FPN9 M0 / FDM SDI0 M2 / FDM SDI1 M2 / FWN10 M0 / FPM SDI2 M2 / FDM SDI2 M2 / FDM SDI3 M2 / I2S1 SDO2 M2	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d / GPI03 B4 d / GPI03 B5 d / GPI03 B7 d / GPI03 B7 d / GPI03 C1 d
LCDC D16 LCDC D17 LCDC D18 LCDC D19 LCDC D20 LCDC D21 LCDC D21 LCDC D22	/ VOP BT1120 D7 / VOP BT1120 D8 / VOP BT1120 D9 / VOP BT1120 D10 / VOP BT1120 D10 / VOP BT1120 D12 / PWM12 M0 / PWM13 M0 / VOP BT1120 D13 / VOP BT1120 D14	/ GMAC1 RXD0 M0 / GMAC1 RXD1 M0 / GMAC1 RXDV CR8 M0 / GMAC1 RXER M0 / GMAC1 RXER M0 / GMAC1 TXD1 M0 / GMAC1 TXD1 M0 / GMAC1 MCLENNOT M0 / GMAC1 MCLENNOT M0 / SPI1 MISC M1	/ UART4 TX M1 / 12C5 SCI M0 / 12C5 SDA M0 / 12C3 SDA M0 / 12C3 SDA M1 / UART3 TX M1 / UART3 TX M1 / PCIE20 PERSTA M1 / UART5 TX M1 / UART5 TX M1	/ PWM8 M0 PWM5 M0 FDM SDIO M2 PDM SDII M2 PMM10 M0 PWM11 IR M0 PMM1 IR M0 PDM SDI2 M2 FDM SDI3 M2 (I281 SDO2 M2 I281 SDO3 M2	/ GPI03 B1 d / GPI03 B2 d / GPI03 B3 d GPI03 B4 d / GPI03 B5 d / GPI03 B5 d / GPI03 C0 d / GPI03 C0 d / GPI03 C1 d - GPI03 C2 d

BGA636\_19R00X19R00X1R20

Figure 2-73 RK3568 SDMMC2 interface M1 functional pins

• SDMMC2 interface pull-up and pull-down and matching design recommendations are shown in the Table:

Signal	Internal pull-up and pull-down	Connection mode	Description (chipset)
SDMMC2_D[3:0]	pull up	connect a 22ohm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor	SD data send/receive
SDMMC2_CLK	pull down	connect a 220hm resistor in series	SD clock send
SDMMC2_CMD	pull up	connect a 22ohm resistor in series which can be deleted when the trace is short; use the corresponding IO internal pull-up resistor	SD command send/receive

Table 2–17 SDMMC2 interface design

When the board-to-board connection is realized through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, as long as it can meet the SI test), and reserve TVS devices.

#### 2.3.1.4 Notice of SDIO WIFI Interface

Please ensure that the IO level of the module is consistent with the IO level of CPU, otherwise, level

matching processing is required.

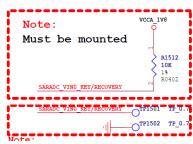
- The crystal load capacitance should be selected according to the CL capacitance value of the crystal actually used, and the frequency tolerance at room temperature should be controlled within 10ppm.
- The antenna reserves a  $\pi$ -type circuit for antenna matching adjustment.
- Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD.
- If you use a module that requires 32.768k clock input, please pay attention to the clock amplitude.
- The schematic design is compatible with multiple modes. In the process of SMT, you must select according to the actual used module, and do not do SMT at will.

#### 2.3.2 SARADC Circuit

- The RK3568 integrates a SARADC controller, which can provide 8 SARADC inputs.
- The SARADC\_VIN0 of the RK3568 chip is used as the key value input sampling port by default, and is multiplexed as the Recovery mode button (cannot be modified). SARADC\_VIN0 is pulled up to VCCA\_1V8 through a 10Kohm pull-up resistor, and the default voltage is high voltage (1.8V). Under the premise that there is no key action and the system has burned the firmware, power on and directly enter the system; if the Recovery mode button has been pressed when the system is started, that is, SARADC\_VIN0 is kept at low level (0V), RK3568 enters Loader flashing mode. When the PC recognizes the USB device, release the button to restore SARADC\_VIN0 to high level (1.8V) for flashing firmware. Therefore, when a product without buttons, if SARADC\_VIN0 is left hanged up, it will be unstable, which may affect booting. Therefore, the 10Kohm pull-up resistor of SARADC\_VIN0 must be reserved and cannot be deleted to ensure the default normal booting judgment. In addition, for the convenience of development, it is recommended to reserve keys or test points.

# RK3568\_O(SARADC/OTP)

J1000o									
SARADC	в27	SARADC_VIN0_KEY/RECOVERY	C1501 1	П	2	1nF	X5R	50V	h.
Recovery/ SARADC_VIN0	C26	SARADC VIN1 HW ID	c1502 1	1	2	C0402 1nF	X5R	50V	Ľ
SARADC_VIN1	D24	SARADC VIN2 HP HOOK	c1503 1		2	C0402 1nF	X5R	50V	Ľ
SARADC_VIN2	E23	SARADC VIN3 BOM ID	c1504 1		2	C0402 1nF	X5R	50V	Ľ
SARADC_VIN3				11	-	C0402			111



#### Figure 2-74 SARADC VIN0 interface

On RK3568, the SARADC sampling range is 0-1.8V, with 10 bits sampling accuracy. The key array is in parallel, and the input key value can be adjusted by increasing or decreasing the keys and adjusting the ratio of the voltage-dividing resistance, so as to realize multi-key input to meet requirements of different customer products. In the process of design, it is recommended that the sampling value of any two keys must be greater than +/-35, that is, the center voltage difference must be greater than 123mV.

RK3568 Hardware Design Guide

SARADC				
Recovery/ SARADC VIN0	в27	SARADC_VIN0_KEY/RECOVERY	C1501 1	2 1nF X5R 50V
SARADC VIN1	C26	SARADC_VIN1_HW_ID	<b>c1502</b> 1	C0402 2 <b>1nF</b> X5R 50V
SARADC VIN2	D24	SARADC_VIN2_HP_HOOK	<b>c1503</b> 1	C0402 2 <b>1nF</b> X5R 50V
SARADC VIN3	E23	SARADC_VIN3_BOM_ID	c1504 1	C0402 2 <b>1nF</b> X5R 50V
SARADC VIN4	G21	SARADC_VIN4	<b>c1505</b> 1	C0402 2 <b>1nF</b> X5R 50V
SARADC VIN5	F22	SARADC_VIN5	<b>c1506</b> 1	C0402 2 1nF X5R 50V C0402
SARADC VIN6	G20	SARADC_VIN6	<b>c1507</b> 1	2 1nF X5R 50V C0402
	F21	SARADC_VIN7	<b>c1508</b> 1	2 1nF X5R 50V
	H22	VCCA 1V8	I	C0402
	-			

Figure 2-75 RK3568 SARADC module

- Pay attention to the following items in RK3568 SARADC design:
  - The decoupling capacitors of the SARADC\_AVDD\_1V8 power supply must not be deleted, and they should be placed close to the RK3568 pin during layout.
  - When SARADC\_VIN [7:0] is used, a 1nF capacitor must be added close to the pin to eliminate jitter.
  - When it is used for button collection, ESD protection is required close to the button, and the button with 0 key value must be connected in series with a 100ohm resistor to strengthen the anti-static surge capability (if there is only one button, ESD components must be close to the button, first pass ESD components →100ohm resistor →1nF→ chip pin).

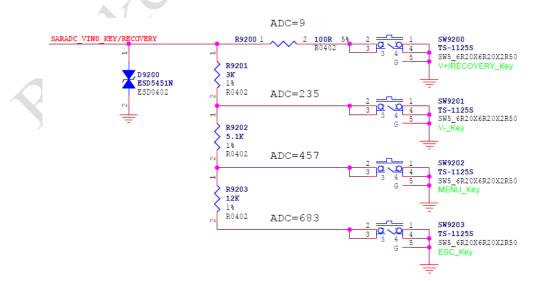
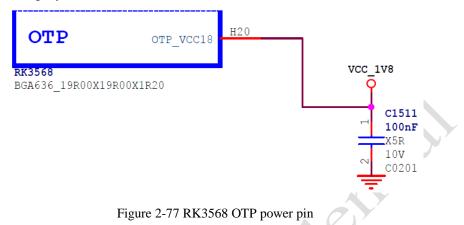


Figure 2-76 The button circuit using SARADC sampling

- The RK3568 integrates an 8Kbit OTP, 7Kbit can be used for security applications.
- Support write, read and idle mode, in these modes, OTP\_VCC18 pin must be powered.
- The decoupling capacitor of the OTP\_VCC18 power supply must not be deleted. Place it close to the RK3568 pin during layout.



# 2.3.4 USB2.0/USB3.0 Circuit

There are one USB3.0 OTG controller, one USB3.0 HOST controller, and two USB2.0 HOST controllers in RK3568, see the pink and green boxes as below:

- The USB SS signal of the USB3.0 OTG controller uses MULTI\_PHY0, and the USB LS/FS/HS signal uses USB2.0 OTG0 PHY.
- The USB SS signal of the USB3.0 HOST controller uses MULTI\_PHY1, and the USB LS/FS/HS signal uses USB2.0 HOST1 PHY.
- Two USB2.0 HOST controllers use USB2.0 HOST2 PHY and USB2.0 HOST3 PHY respectively.

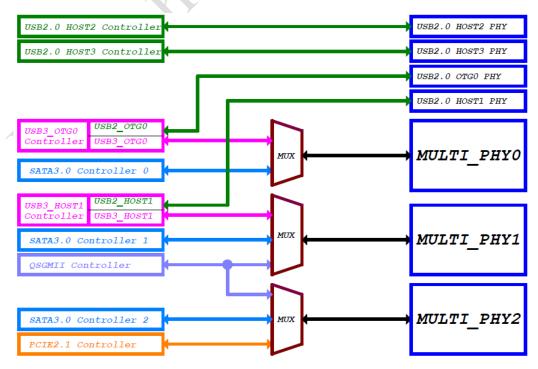


Figure 2-78 Multiplexing relationship between MULTI\_PHY0/1and USB3.0 controllers

In the USB3.0 OTG0 controller, the USB LS/FS/HS mode signal uses USB2.0 OTG0 PHY, and the USB SS mode signal uses MULTI\_PHY0 (multiplexed with the SATA0 controller). The signals in the box below form a complete USB3.0 OTG0 interface, other combinations are not supported; If you only need USB2.0 interface, just select the DP/DM signal, and MULTI\_PHY0 can be configured as SATA0 function.

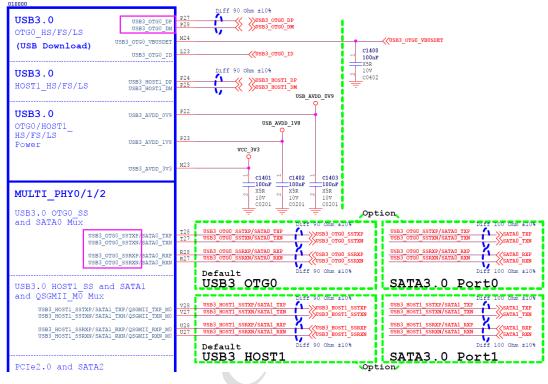


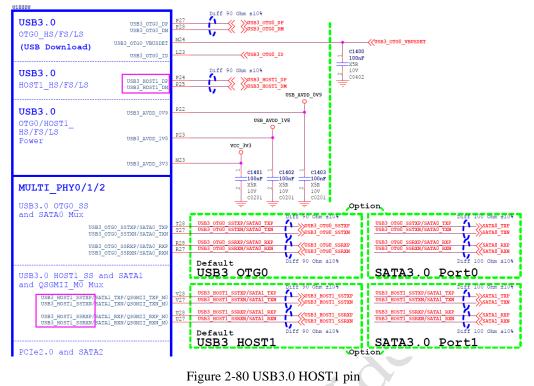
Figure 2-79 USB3.0 OTG0 pin

Note Note

Only USB3\_OTG0\_DP and USB3\_OTG0\_DM support downloading firmware. If a product does not use this interface, it must be reserved during debugging and production process. Note: USB3\_OTG0\_VBUSDET must also be connected.

In the USB3.0 HOST1 controller, the USB LS/FS/HS mode signal uses USB2.0 HOST1 PHY, and the USB SS mode signal uses MULTI\_PHY1 (multiplexed with the SATA1 controller and the QSGMII controller). The signals in the box below form a complete USB3.0 HOST1 interface, other combinations are not supported;

If you only need USB2.0 interface, just select the DP/DM signal, and MULTI\_PHY1 can be configured as SATA1 or QSGMII function.



The USB2.0 HOST2 controller uses USB2.0 HOST2 PHY, the signals in the box below form the USB2.0 HOST2 interface.

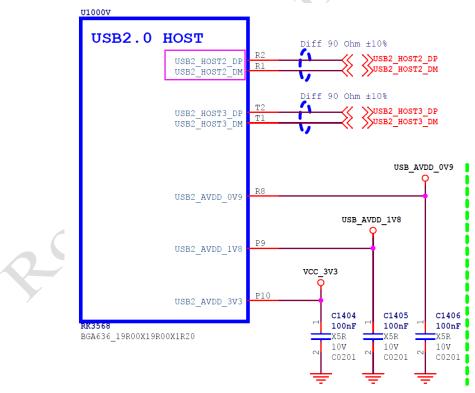


Figure 2-81 USB2.0 HOST2 pin

The USB2.0 HOST3 controller uses USB2.0 HOST3 PHY, the signals in the box below form the USB2.0 HOST3 interface.

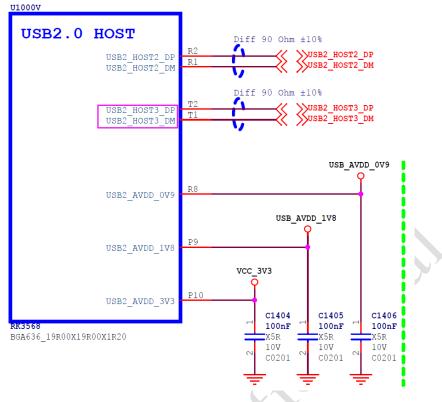


Figure 2-82 USB2.0 HOST3 pin

- Pay attention to the following items in USB2.0/USB3.0 design:
  - Only USB3\_OTG0\_DP/USB3\_OTG0\_DM is the system firmware flashing port. If a product does not use this port, this port must be reserved during the debugging and production process, otherwise, firmware flashing is disabled during debugging and production process.
  - There is an internal about 200Kohm resistor in USB3\_OTG0\_ID to pull up to USB3\_AVDD\_1V8;
  - USB3\_OTG0\_VBUSDET is the OTG and Device mode detection pin, high effective, 2.7-3.3V, TYP:

3.0V, it is recommended to place a 100nF capacitor on the pin.

OTG mode can be set to the following three modes:

• OTG mode: it can switch to device mode or HOST mode according to the status of the ID pin automatically. When ID pin is pulled high, it is device mode, and when ID pin is pulled low, it is HOST mode. When in device mode, it will also judge whether the VBUSDET pin is high. If it is high, DP will be pulled up and enumeration will start.

• Device mode: When set to this mode, ID pin is not needed, just judge whether the VBUSDET pin is high, if it is high, DP will be pulled up and enumeration will start.

• HOST mode: When set to this mode, there is no need to care about ID and VBUSDET status. (If the product only needs HOST mode, but only USB3\_OTG0\_DP/USB3\_OTG0\_DM is the system firmware flashing port, and this port is needed during debugging and production. So when flashing and adb debugging, it needs to be set to device mode, the USB3\_OTG0\_VBUSDET signal must also be connected).

• Before uboot is up, it is device mode by default. After entering uboot, you can configure these three modes according to actual needs.

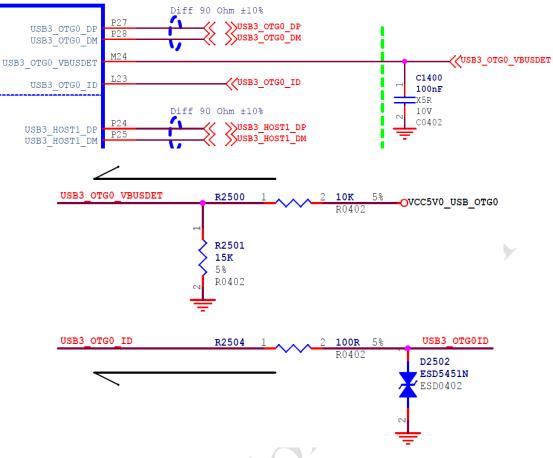


Figure 2-83 RK3568 VBUSDET and ID Circuit

USB3\_AVDD\_0V9, USB2\_AVDD\_0V9, USB3\_AVDD\_1V8, USB2\_AVDD\_1V8 power pins and VDDA\_0V9, VCCA\_1V8 are required to be isolated by magnetic beads, please refer to the reference diagram/ schematic design for the details;

al	<b>C2132</b> 2	1	1uF X5R	6.3V	VDDA_0V9	FB2100		2	120R-100MHz	OUSB AVDD	079
	<b>C2133</b> 2	1	C0402 <b>1uF</b> X5R	6.3V	VCCA_1V8 O	FB2101	0.030ohm	2	L0603 120R-100MHz	OUSB_AVDD	-
_'II			C0402				0.030ohm		L0603	OOSB_RVDD_	

Figure 2-84 USB2.0 PHY power supply magnetic bead isolation circuit

- In order to improve the USB performance, the decoupling capacitors of each power supply of the PHY must not be deleted. Please place them close to the pins during layout;
- In order to strengthen the anti-static and surge capability, ESD devices must be reserved on signal. The ESD parasitic capacitance of the USB2.0 signal cannot exceed 3pF. In addition, the DP/DM of the USB2.0 signal is connected in series with a 2.20hm resistor to strengthen the anti-static surge capability, it cannot be deleted. The following figure is an example of USB2\_HOST2\_DP/DM, other USB2.0 interfaces also need to be processed in the same way;

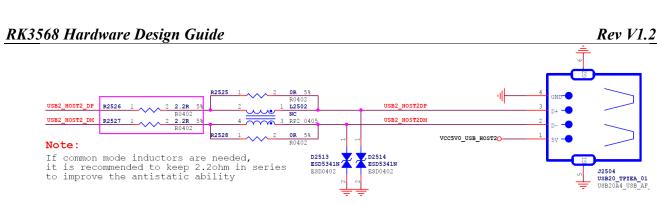


Figure 2-85 USB2.0 signal is connected in series with a 2.20hm resistor

In order to suppress electromagnetic radiation, you can consider to reserve a common mode choke on the signal line. In the debugging process, you can choose to use a resistor or a common mode choke according to the actual situation. The diagram below is an example of USB2 HOST2 DP/DM, other USB2.0 interfaces also need to be processed in the same way;

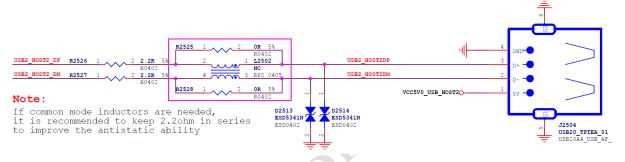
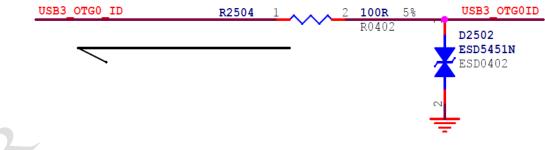


Figure 2-86 USB2.0 signal is connected in series with common mode choke circuit

If the USB3\_OTG0\_ID signal is used, in order to strengthen the anti-static and surge capability, ESD devices must be reserved on the signal, and a 100ohm resistor must be connected in series, which cannot be deleted. See the following diagram:





For the HOST function, it is recommended to add a current-limiting switch for the 5V power supply. The current-limiting size can be adjusted according to application needs. The current-limiting switch is controlled by GPIO, it is recommended to add more than 100µF and 100nF capacitor for the 5V power supply.

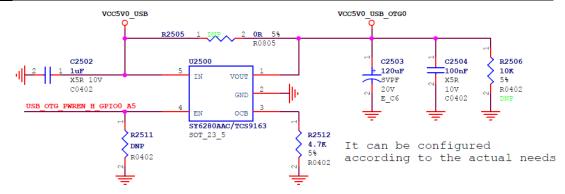


Figure 2-88 USB 5V current-limiting circuit

- It requires to add a 100nF AC coupling capacitor to the SSTXP/N line in the USB 3.0 protocol. The AC coupling capacitor is recommended to use 0201 package for lower ESR and ESL and fewer impedance changes on the line.
- All signals of the USB3 connector must be added with ESD devices which should be placed close to the USB connector. For SSTXP/N, SSRXP/N signals, the ESD parasitic capacitance must not exceed 0.4pF.

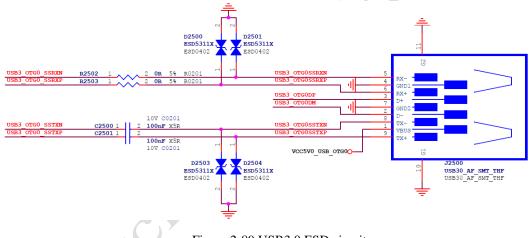


Figure 2-89 USB3.0 ESD circuit

MULTI\_PHY\_AVDD\_0V9/1V8 power supply pins should be placed 4.7µF and 100nF decoupling capacitors, which must not be deleted. Place them close to the RK3568 pin during layout.

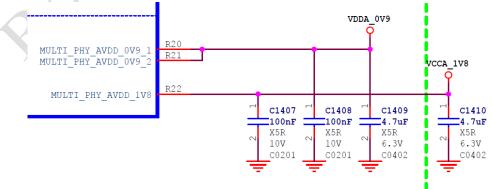


Figure 2-90 MULTI PHY power supply decoupling circuit

■ USB2.0/USB3.0 interface matching design recommendations are shown in the following Table.

# **RK3568 Hardware Design Guide**

	Table 2-18 RK3568 USB2.0/USB3.0 inter	face design
Signal	Connection mode	Description
USB3_OTG0_DP/DM	Connect 2.20hm resistor in series	data input and output in USB HS/FS/LS mode
USB3_OTG0_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package is recommended)	data output in USB SS mode
USB3_OTG0_SSRXP/SSRXN	Connect 0ohm resistor in series	data input in USB SS mode
USB3_OTG0_ID	Connect a 100ohm resistor in series (to strengthen the external power supply, the power supply needs to be connected to the same power supply as USB3_AVDD_1V8)	USB OTG ID recognition, required for Micro-USB interface
USB3_OTG0_VBUSDET	Resistance voltage-dividing detection	USB OTG insertion detection
USB3_HOST1_DP/DM	Connect 2.20hm resistor in series	data input and output in USB HS/FS/LS mode
USB3_HOST1_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package is recommended)	data output in USB SS mode
USB3_HOST1_SSRXP/SSRXN	Connect 0ohm resistor in series	data input in USB SS mode
USB3_HOST2_DP/DM	Connect 2.20hm resistor in series	data input and output in USB HS/FS/LS mode
USB3_HOST3_DP/DM	Connect 2.20hm resistor in series	data input and output in USB HS/FS/LS mode

# 2.3.5 SATA3.0 Circuit

There are three SATA3.0 controllers in RK3568, see the blue box below, using MULTI\_PHY0/1/2 respectively.

- Support SATA PM function, each port can support 5 devices.
- Support SATA 1.5Gb/s, SATA 3.0Gb/s, SATA 6.0Gb/s speeds.
- Support eSATA.

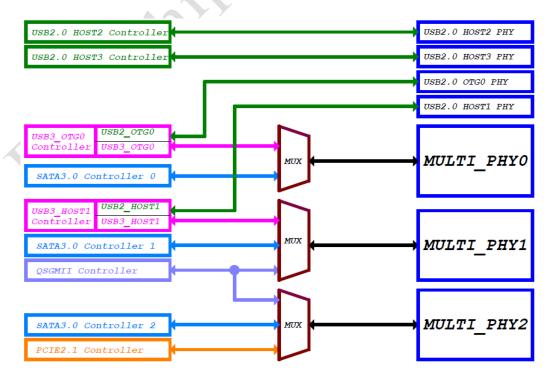
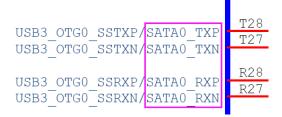
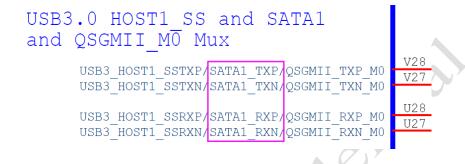


Figure 2-91 MULTI\_PHY0/1/2 and SATA3.0 controller multiplexing relationship

The SATA0 controller uses MULTI\_PHY0 (multiplexed with USB3.0 OTG0 controller).



■ The SATA1 controller uses MULTI\_PHY1 (multiplexed with USB3.0 HOST1 and QSGMII controller).



The SATA2 controller uses MULTI\_PHY2 (multiplexed with PCIe2.0 and QSGMII controller).

PCIE2.0 and SATA2 and QSGMII\_M1 Mux PCIE20\_TXP/SATA2\_TXP/QSGMII\_TXP\_M1 PCIE20\_TXN/SATA2\_TXN/QSGMII\_TXN\_M1 PCIE20\_RXP/SATA2\_RXP/QSGMII\_RXP\_M1 PCIE20\_RXN/SATA2\_RXN/QSGMII\_RXN\_M1 PCIE20\_REFCLKP PCIE20\_REFCLKP PCIE20\_REFCLKP

The related control IOs of SATA0/1/2 controller:

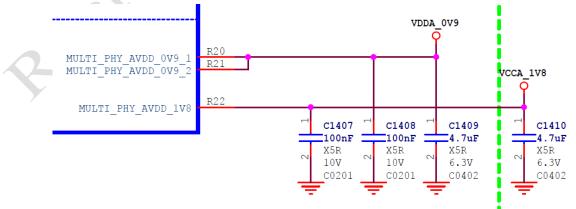
SATA0\_ACT\_LED: LED blinking control output when SATA0 interface has data transmission; SATA1\_ACT\_LED: LED blinking control output when SATA1 interface has data transmission; SATA2\_ACT\_LED: LED blinking control output when SATA2 interface has data transmission; SATA\_CP\_DET: Plug in and out detection input of SATA hot-plug device SATA\_MP\_SWITCH: Switch detection input of SATA hot-plug device SATA\_CP\_POD: Power switch output of SATA hot-plug device

SATA\_CP\_DET, SATA\_MP\_SWITCH, SATA\_CP\_POD are multiplexed with SATA0/1/2 interfaces, which can be configured by register to be SATA0, SATA1 or SATA2.

			1_RX_M1	/ PCIE30X2_CLKREQ		2S3_MCLK_M1	/	GPIO4 C2 d	
M15 IR M1	/ SPI3 MOSI N		1 TX M1	/ PCIE30X2 WAKEn		2S3 SCLK M1		GPIO4 C3 d	i A
P HPDIN MO M12 M1	/ SPDIF TX M2 / SPI3 MISO M		A2 ACT LED A1 ACT LED	/ PCIE30X2 PERSTr / UART9 TX M1		2S3 LRCK M1	·	GPIO4 C4 d	A .
M12_M1 M13_M1	/ SPI3 MISO M / SPI3 CSO M1		AU ACT LED AO ACT LED	/ UART9 RX M1		2S3 SDO M1 2S3 SDI M1	/	GPIO4 C5 d GPIO4 C6 d	
MITX SCL	/ 12C5 SCL M1	1					,	GPIO4 C7 u	A
MITX SDA	/ 12C5 SDA M							GPIO4 D0 u	A
MITX_CEC_M0	/ SPI3_CS1_M1	1					/	GPIO4 D1 u	
								GPIO4 D2 d	l A
68								VCCIO7	, <u>v</u>
<b>68</b> 36 19R00X19R00X	X1R20							VCCI07	, <u>v</u>
	X1R20				REFCLK		/ (	VCCIO7 GPIO0 A0 d	
	X1R20		TSADC PMIC	SHUT MO	/ TSADC	OUT SHUT_ORG SHUT_M1	/ (		d z
36 19R00X19R00>			PMIC	SLEEP	/ TSADC	SHUT ORG	/ (	GPIOO AO d GPIOO A1 z GPIOO A2 d GPIOO A3 u	
36 19R00X19R00> SDMMC0_DET	/ SATA_C		PMIC / PCIE3	SLEEP 0X1_CLKREQn_M0	/ TSADC	SHUT ORG		GPIO0 A0 d GPIO0 A1 z GPIO0 A2 d GPIO0 A3 u GPIO0 A4 u	
36 19R00X19R00> SDMMC0_DET SDMMC0_FWRE	/ SATA C N / SATA P	4P SWITCH	PMIC / PCIE3 / PCIE2	SLEEP 0X1 CLKREQn M0 0 CLKREQn M0	/ TSADC	SHUT ORG		GPIO0 A0 d GPIO0 A1 z GPIO0 A2 d GPIO0 A3 u GPIO0 A4 u GPIO0 A5 d	
36 19R00X19R00> SDMMC0_DET	/ SATA_C	4P SWITCH	PMIC / PCIE3 / PCIE2	SLEEP 0X1_CLKREQn_M0	/ TSADC	SHUT ORG		GPIO0 A0 d GPIO0 A1 z GPIO0 A2 d GPIO0 A3 u GPIO0 A4 u	
36 19R00X19R00> SDMMC0_DET SDMMC0_PWRE	/ SATA C N / SATA P	4P SWITCH	PMIC / PCIE3 / PCIE2	SLEEP 0X1 CLKREQn M0 0 CLKREQn M0	/ TSADC / TSADC	SHUT ORG		GPIO0 A0 d GPIO0 A1 z GPIO0 A2 d GPIO0 A3 u GPIO0 A4 u GPIO0 A5 d	

Figure 2-92 SATA0/1/2 related control IO pins

- Pay attention to the following items in SATA design:
  - When designing the slot, the peripheral circuit and power supply should meet the requirements of Spec.
  - MULTI\_PHY\_AVDD\_0V9/1V8 power supply pins should add 4.7µF and 100nF decoupling capacitors, which must not be deleted. Place them close to the RK3568 pin during layout.



- IOnF AC coupling capacitors connected in series on the TXP/N, RXP/N differential signals of SATA interface. The AC coupling capacitor is recommended to use 0201 package for lower ESR and ESL and fewer impedance changes on the line.
- ESD devices must be added to all signals of the eSATA interface connector, Place them close to the

connector during layout. The ESD parasitic capacitance cannot exceed 0.4pF.

SATA interface matching design recommendations are shown in the following Table.

Signal	Connection mode	Description
SATA0_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA0_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input
SATA1_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA1_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input
SATA2_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA2_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input

Table 2 10 PK 3568	SATA interface design
1able 2 - 19  KK 3368	SAIA interface design

# 2.3.6 QSGMII/SGMII Circuit

There is one QSGMII or SGMII interface in RK3568.

- SGMII (Serial Gigabit Media Independent Interface) converts the RGMII or RMII interface between gigabit MAC and gigabit PHY into a serial interface. Using a SGMII interface is to reduce the number of pins required for the RGMII interface, and the rate of SGMII interface is 1.25Gbps.
- QSGMII (Quad Serial Gigabit Media Independent Interface) is an extension of SGMII. QSGMII interface transfers data between a 4-port gigabit MAC and a 4-port gigabit PHY via a serial line running at a 5Gbps rate. Each Port can run at a 10/100/1000Mbps rate, but RK3568 has only two gigabit MACs inside, that is to say, it can only support 2 Port 10/100/1000Mbps interface via the QSGMII interface.
- QSGMII interface of RK3568 is compatible with SGMII.
- GMAC0/GMAC1 controller used by QSGMII/SGMII and RGMII/RMII interface from MUX to IO are multiplexed.
- QSGMI/SGMII PCS interface is multiplexed to two PHY interfaces: MULTI\_PHY1 and MULTI\_PHY2, but only one of the PHY interfaces can be used.

The paths of GMAC0, GMAC1, QSGMII/SGMII PCS and QSGMII/SGMII PHY are shown in the following diagram with green lines.

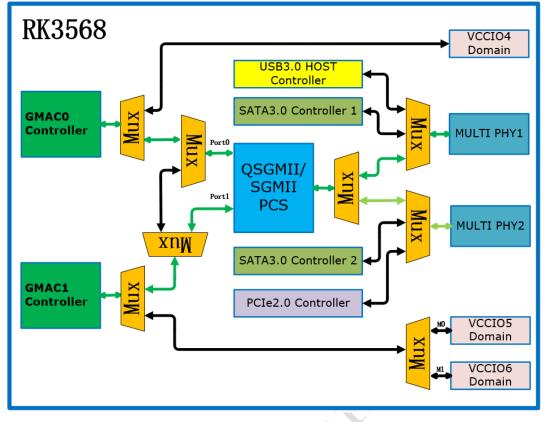


Figure 2-93 The paths of GMAC0, GMAC1, QSGMII/SGMII PCS and QSGMII/SGMII PHY

The application block diagram of QSGMII using MULTI\_PHY1 is as follows (green lines). In this case, the function of GMAC0 and GMAC1 controllers multiplexed to VCCIO4/5/6 is unavailable, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI\_PHY1 is unavailable either.

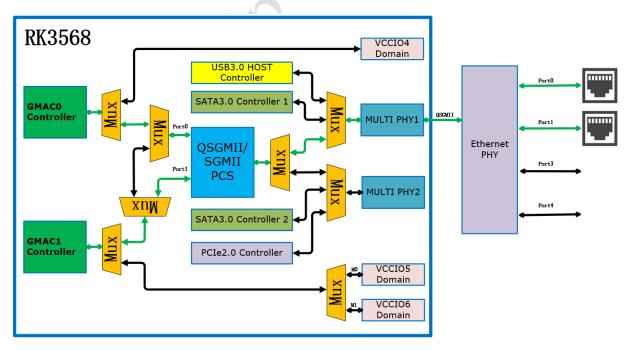


Figure 2-94 The application block diagram of QSGMII-MULTI\_PHY1Y1

■ The application block diagram of QSGMII using MULTI\_PHY2 is as follows (green lines). In this case, the function of GMAC0 and GMAC1 controllers multiplexed to VCCIO4/5/6 is unavailable, the function

of SATA2 and PCIe2.0 multiplexed by MULTI\_PHY2 is unavailable either.

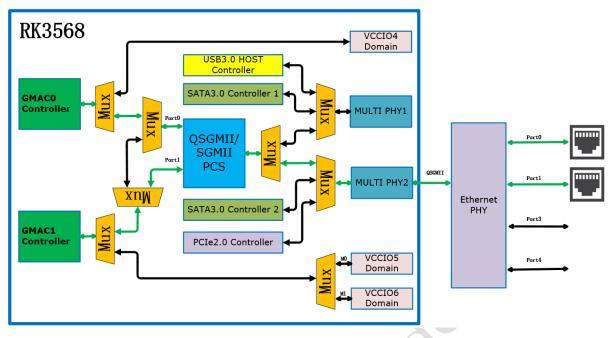
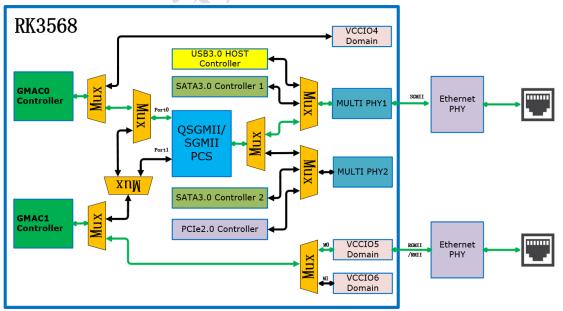


Figure 2-95 The application block diagram of QSGMII-MULTI\_PHY2

- The application block diagram of SGMII using MULTI\_PHY1 is as follows (green lines), GMAC0 controller or GMAC1 controller are optional.
  - When choosing GMAC0 controller for SGMII, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI\_PHY1 is unavailable, the function of GMAC0 multiplexed by VCCIO4 is unavailable either. One of GMAC1 controllers multiplexing to VCCIO5 or VCCIO6 can be selected to implement the second Ethernet port.



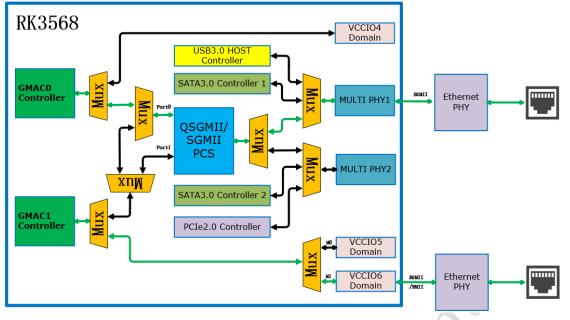


Figure 2-96 The application block diagram of GMAC0-SGMII-MULTI\_PHY1

When choosing GMAC1 controller for SGMII, the function of USB3.0 HOST1 and SATA1 multiplexed by MULTI\_PHY1 is unavailable, the function of GMAC1 multiplexed by VCCIO5 or VCCIO6 is unavailable either. GMAC0 controller multiplexing to VCCIO4 can implement the second Ethernet port. As shown in the following diagram (green lines).

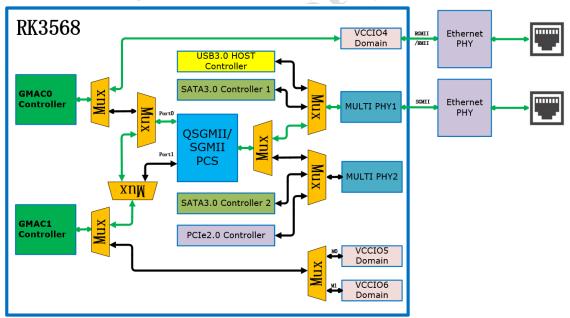


Figure 2-97 The application block diagram of GMAC1-SGMII-MULTI\_PHY1

- The application block diagram of SGMII using MULTI\_PHY2 is as follows (green lines), GMAC0 controller or GMAC1 controller can be used.
  - When choosing GMAC0 controller for SGMII, the function of SATA2 and PCIe2.0 multiplexed by MULTI\_PHY2 is unavailable, the function of GMAC0 multiplexed by VCCIO4 is unavailable either. One of GMAC1 controllers multiplexing to VCCIO5 or VCCIO6 can be selected to implement the second Ethernet port.

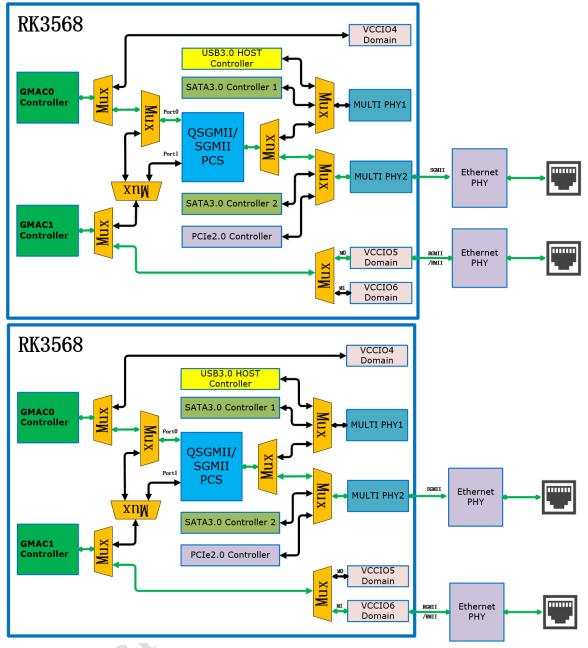


Figure 2-98 The application block diagram of GMAC0-SGMII-MULTI\_PHY2

When choosing GMAC1 controller for SGMII, the function of SATA2 and PCIe2.0 multiplexed by MULTI\_PHY2 is unavailable, the function of GMAC1 multiplexed by VCCIO5 or VCCIO6 is unavailable either. GMAC0 controller multiplexing to VCCIO4 can implement the second Ethernet port. As shown in the following diagram (green lines).

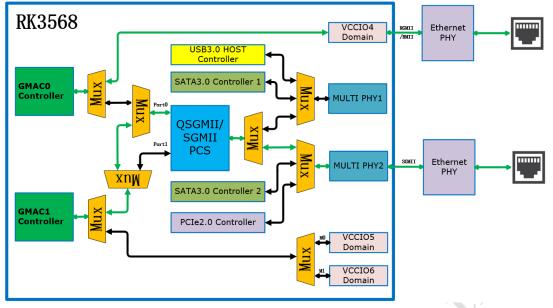


Figure 2-99 The application block diagram of GMAC1-SGMII-MULTI\_PHY2

When QSGMII/SGMII is multiplexed with USB3.0 HOST1 and SATA1 controllers by MULTI\_PHY1, the function of QSGMII multiplexed in MULTI\_PHY2 is unavailable.

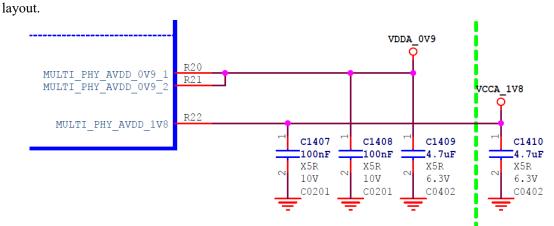
USB3.0 HOST1 SS and SATA1 and QSGMII MO Mux	
USB3_HOST1_SSTXP/SATA1_TXP/QSGMII_TXP_M0	V28
USB3_HOST1_SSTXN/SATA1_TXN/QSGMII_TXN_M0	V27
USB3_HOST1_SSRXP/SATA1_RXP/QSGMII_RXP_M0	U28
USB3_HOST1_SSRXN/SATA1_RXN/QSGMII_RXN_M0	U27

When QSGMII/SGMII is multiplexed with SATA2 and PCIe2.0 controllers by MULTI\_PHY2, the function of QSGMII multiplexed in MULTI\_PHY1 is unavailable.



- please notice the following items in QSGMII/SGMII design,:
  - Peripheral circuit and power supply of peripherals should meet the requirements of peripherals.
  - The power pins of MULTI\_PHY\_AVDD\_0V9/1V8 should be placed with 4.7uF and 100nF

decoupling capacitors, which cannot be deleted. Placed as close to RK3568 pins as possible when



- The 100nF AC coupling capacitor connected in series to TXP/N and RXP/N differential signals of QSGMII/SGMII interface is recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced.
- The matching design recommendations of QSGMII/SGMII interface are shown in the following Table.

Signal	Connection mode	Description
QSGMII_TXP/TXN_M0	Connect in series with a 100Nf capacitor (the 0201 package is recommended)	QSGMII is multiplexed in MULTI_PHY1 data output
QSGMII_RXP/RXN_M0	Connect in series with a 100Nf capacitor (the 0201 package is recommended)	QSGMII is multiplexed in MULTI_PHY1 data output
QSGMII_TXP/TXN_M1	Connect in series with a 100Nf capacitor (the 0201 package is recommended)	QSGMII is multiplexed in MULTI_PHY2 data output
QSGMII_RXP/RXN_M1	Connect in series with a 100Nf capacitor (the 0201 package is recommended)	QSGMII is multiplexed in MULTI_PHY2 data output

#### Table 2-20 RK3568 QSGMII/SGMII interface design

# 2.3.7 PCIe2.0 Circuit

RK3568 has a x1 Lane PCIe2.0 RC Mode controller, which supports RC (Root Complex) mode only.

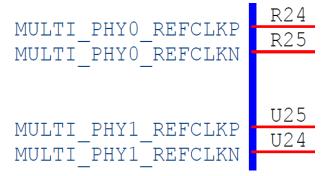
PCIe2.0 controller is multiplexed with SATA2 and QSGMII\_M1 controllers by MULTI\_PHY2.

PCIe2.0 and QSGM				
Г			VD COCMITE MVD M1	W27
			XP/QSGMII_TXP_M1	W28
	PCIE20_TXN/	SATA2_T	XN/QSGMII_TXN_M1	
	DCIE20 DVD	ים פאשאט	VD/OCCMIT DVD M1	Y27
			XP/QSGMII_RXP_M1	Y28
	PCIE20_RXN/	SATA2_R	XN/QSGMII_RXN_M1	
			PCIE20 REFCLKP	V24
			—	V25
			PCIE20_REFCLKN	

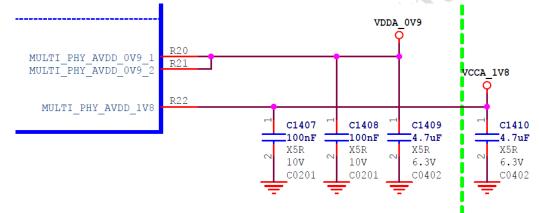
PCIE20\_REFCLKP/N supports both output and input, and output is provided to EP device by default.

# **RK3568 Hardware Design Guide**

■ MULTI PHY0/PHY1 has two pairs of REFCLKs, which are disabled for the moment and hung up.



- please notice the following items in PCIe2.0 design,:
  - When designing Slot, peripheral circuit and power supply should meet the requirements of Spec.
  - The power pins of MULTI\_PHY\_AVDD\_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted. And placed close to RK3568 pins when layout.



- The 100nF AC coupling capacitor connected in series to TXP/N differential signal of PCIe2.0 interface is recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced.
- The functional pin must be used by PCIE20\_CLKREQn and PCIE20\_WAKEn, and they cannot be replaced by GPIO. Please pay special attention to that: choose both\_M0 or \_M1 or \_M2, instead of one is \_M0 and the other is \_M1.
- PCIE20\_PERSTn can choose functional pin or be replaced by GPIO. If you choose functional pin, PCIE20\_PERSTn must be in the same \_Mx group as PCIE20\_CLKREQn and PCIE20\_WAKEn.
- Standard PCIe Slot: PCIE20\_CLKREQn, PCIE20\_WAKEn, PCIE20\_PERSTn are 3.3V level.
- It's suggested to add a 100NF capacitor in the Slot pin of PCIE20\_PERSTn to enhance the antistatic capability.
- You can use GPIO when PCIE20 PRSNT is 'Add In Card' which means inserting detection pins.
- The matching design recommendations of PCIe2.0 interface are shown in the following Table.

# **RK3568 Hardware Design Guide**

Signal	Connection mode	Description
PCIE20_TXP/TXN	Connect in series with a 100Nf capacitor (the 0201 package is recommended)	PCIe data output
PCIE20_RXP/RXN	Direct connection	PCIe data input
PCIE20_REFCLKP/CLKN	Direct connection	PCIe reference clock
PCIE20_CLKREQn	Connect in series with a 220hm resistor	PCIe reference clock request input (RC mode)
PCIE20_WAKEn	Connect in series with a 22ohm resistor	PCIe wake-up input(RC mode)
PCIE20_PERSTn	Connect in series with a 22ohm resistor	PCIe global reset output(RC mode)
PCIE20_PRSNT	Connect in series with a 22ohm resistor	'Add In Card'-insert test input (RC mode)

# 2.3.8 PCIe3.0 Circuit

RK3568 has built in a PCIe3.0 x2 Lane Dual Mode controller, a PCIe3.0 x1 Lane RC Mode controller and a PCIe3.0 x2 Lane PHY.

- Support PCIe3.0 x2 Lane RC mode and is compatible with PCIe3.0 x1 Lane RC mode.
- Support PCIe3.0 x2 Lane EP mode and is compatible with PCIe3.0 x1 Lane EP mode.
- Support PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode.
- Connect both PCIe3.0 x2 Lane Dual Mode controller and PCIe3.0 x1 Lane RC Mode controller to PCIe3.0 x2 Lane PHY.

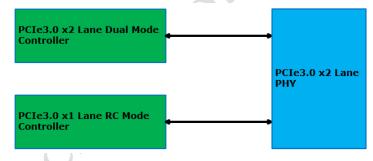


Figure 2-100 PCIe3.0 controller/PCIe3.0 PHY block diagram

- PCIe3.0 x2 Lane RC mode, which is compatible with PCIe3.0 x1 Lane RC mode: PCIe3.0 x2 Lane Dual Mode controller usage:
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x2 Lane RC mode, its corresponding signals are PCIE30\_TX0P、PCIE30\_TX0N、PCIE30\_RX0P、PCIE30\_RX0P、PCIE30\_TX1P、PCIE30\_TX1N、PCIE30\_RX1P、PCIE30\_RX1N.
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30\_TX0P、PCIE30\_TX0N、PCIE30\_RX0P、PCIE30\_RX0N.
- PCIe3.0 x2 Lane EP mode is compatible with PCIe3.0 x1 Lane EP mode: PCIe3.0 x2 Lane Dual Mode controller usage:
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x2 Lane EP mode, its corresponding signals are PCIE30\_TX0P、PCIE30\_TX0N、PCIE30\_RX0P、PCIE30\_RX0N、PCIE30\_TX1P、PCIE30\_TX1N、PCIE30\_RX1P、PCIE30\_RX1N.
  - When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane EP mode, its corresponding

signals are PCIE30\_TX0P、PCIE30\_TX0N、PCIE30\_RX0P、PCIE30\_RX0N.

■ PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode:

One uses PCIe3.0 x2 Lane Dual Mode controller, and the other one uses PCIe3.0 x1 Lane RC Mode controller.

- When PCIe3.0 x2 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30 TX0P、PCIE30 TX0N、PCIE30 RX0P、PCIE30 RX0N.
- When PCIe3.0 x1 Lane Dual Mode controller works in PCIe3.0 x1 Lane RC mode, its corresponding signals are PCIE30\_TX1P、PCIE30\_TX1N、PCIE30\_RX1P、PCIE30\_RX1N.
- PCIE30\_REFCLKP/N supports input only.
  - Require providing HCSL level clock input.
  - Must provide the clock which meets requirement of PCIe3.or above.
  - When you use RK3568 PCIe3.0 x2 Lane RC mode, which is compatible with PCIe3.0 x1 Lane RC mode, the reference clock paths are shown as follows:

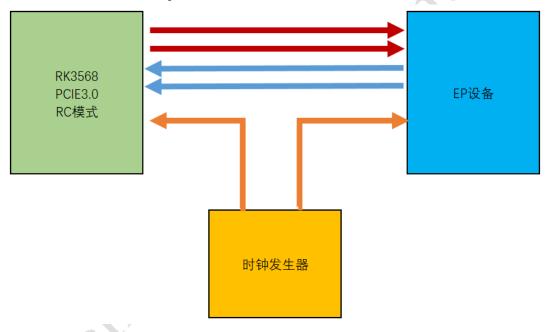


Figure 2-101 Reference clock paths in RK3568 PCIe3.0 x2 Lane RC mode

When in RK3568 PCIe3.0 x2 Lane EP mode, which is compatible with PCIe3.0 x1 Lane EP mode, the reference clock paths are shown as follows:

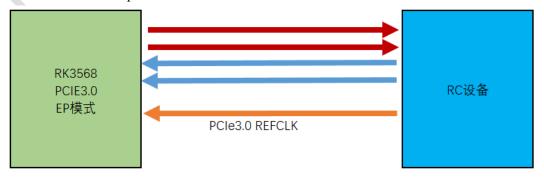


Figure 2-102 Reference clock paths in RK3568 PCIe3.0 x2 Lane EP mode

When in RK3568 PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode, the reference clock

# RK3568 Hardware Design Guide

paths are shown as follows:

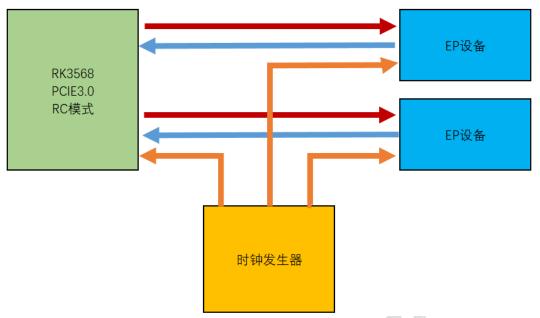


Figure 2-103 The reference clock paths in RK3568 PCIe3.0 x1 Lane RC mode + PCIe3.0 x1 Lane RC mode

- Please note the following items in PCIe3.0 design:
  - In the design of slot, peripheral circuit and power supply should meet the requirements of Spec.
  - The power pins of PCIE30\_AVDD\_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted. And Place them close to RK3568 pins when layout.

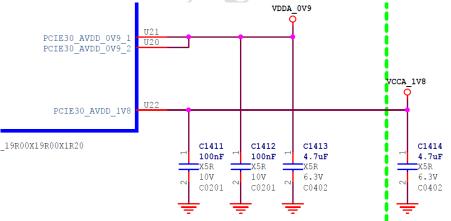


Figure 2–1 The decoupling capacitors of PCIe3.0 PHY power supply

Figure 2-104 PCIe3.0 PHY power decoupling capacitors

- The 220nF AC coupling capacitor connected in series to TX0P/N and TX1P/N differential signals of PCIe3.0 interface is recommended to use 0201package, if you use lower ESR and ESL, impedance changes on the line can also be reduced.
- PCIE\_RESREF is an external reference resistor pin of PCIe3.0 PHY, which externally connects a 200 Ω resistance to ground with accuracy of 1%. The value of the resistance cannot be changed and it should be placed close to RK3568 chip pins when layout.



Figure 2-105 PCIe3.0 PHY RESREF pin

# **RK3568 Hardware Design Guide**

- PCIE30X2\_CLKREQn, PCIE30X2\_WAKEn and PCIE30X2\_PERSTn are corresponding to Lane PCIe3.0 x2 Dual Mode controller.
- PCIE30X1\_CLKREQn, PCIE30X1\_WAKEn and PCIE30X1\_PERSTn are corresponding to Lane PCIe3.0 x1 RC Mode controller.

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
	PCIe3.0 x1Lane	PCIE30 REFCLK	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
-,	+ PCIe3.0 x1Lane	(RC:input)	PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

- PCIE30X2\_CLKREQn, PCIE30X1\_CLKREQn, PCIE30X2\_WAKEn and PCIE30X1\_WAKEn must be used as functional pins, and they cannot be replaced by GPIO. Note: select both \_M0 or \_M1 or \_M2 instead of one \_M0 and one \_M1.
- PCIE30X2\_PERSTn and PCIE30X1\_PERSTn can be used as functional pins or be replaced by GPIO. If you choose functional pins, PCIE30X2\_PERSTn and PCIE30X1\_PERSTn must be in the same \_Mx group as PCIE30X2\_CLKREQn、 PCIE30X2\_WAKEn and PCIE30X1\_CLKREQn、 PCIE30X1\_WAKEn.
- Standard PCIe Slot: PCIE30X2\_CLKREQn、PCIE30X1\_CLKREQn、PCIE30X2\_WAKEn、 PCIE30X1\_WAKEn、PCIE30X2\_PERSTn and PCIE30X1\_PERSTn are 3.3V level.
- It's suggested to add a 100nF capacitor in the Slot pin of PCIE30X2\_PERSTn and PCIE30X1\_PERSTn to enhance the antistatic capability.
- You can use GPIO when PCIE30\_PRSNT is 'Add In Card' which means inserting detection pins.
- The matching design recommendations of PCIe3.0 interface are shown in the following Table. Table 2–22 RK3568 PCIe3.0 interface design

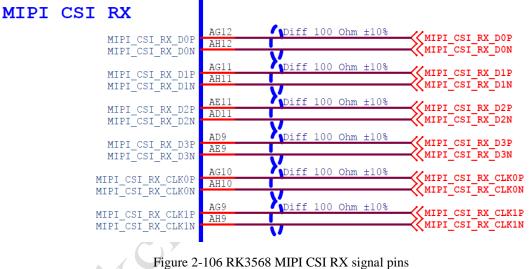
Signal	Connection mode	Description
PCIE30_TX0P/TX0N	Connect in series with a 220nF capacitor(the 0201 package is recommended)	PCIe data output
PCIE30_RX0P/RX0N	Direct connection	PCIe data input
PCIE30_TX1P/TX1N	Connect in series with a 220nF capacitor(the 0201 package is recommended)	PCIe data output
PCIE30_RX1P/RX1N	Direct connection	PCIe data input
PCIE30_REFCLKP_IN/ PCIE30_REFCLKN_IN	Direct connection	PCIe reference clock input
PCIE30_RESREF	Grounding with 200 $\Omega/1\%$ resistance	External reference resistor of PCIe3.0 PHY
PCIE30X2_CLKREQn	Connect in series with a 220hm resistor	PCIe reference clock request input (RC mode) PCIe reference clock request output (EP mode)
PCIE30X2_WAKEn	Connect in series with a 220hm resistor	PCIe wake-up input (RC mode) PCIe wake-up output (EP mode)

Signal	Connection mode	Description
PCIE30X2_PERSTn	Connect in series with a 22ohm resistor	PCIe global reset output (RC mode) PCIe global reset input (EP mode)
PCIE30X2_PRSNT	Connect in series with a 22ohm resistor	'Add In Card'-insert test input (RC mode)
PCIE30X1_CLKREQn	Connect in series with a 220hm resistor	PCIe reference clock request input (RC mode)
PCIE30X1_WAKEn	Connect in series with a 220hm resistor	PCIe wake-up input (RC mode)
PCIE30X1_PERSTn	Connect in series with a 220hm resistor	PCIe global reset output (RC mode)
PCIE30X1_PRSNT	Connect in series with a 220hm resistor	'Add In Card'-insert test input (RC mode)

# 2.3.9 Video Input Interface Circuit

### 2.3.9.1 MIPI CSI RX interface

RK3568 has built in a MIPI CSI RX PHY, which supports MIPI V1.2 with 4Lane in total and two pairs of clocks.



rigule 2-100 KK5500 Mil 1 C51 KA signal pilis

- Support x4Lane mode, refers to MIPI\_CSI\_RX\_CLK0 for MIPI\_CSI\_RX\_D[3:0] data.
- Support x2Lane+x2Lane mode,

MIPI\_CSI\_RX\_D[1:0] data refers to MIPI\_CSI\_RX\_CLK0,

MIPI\_CSI\_RX\_D[3:2] data refers to MIPI\_CSI\_RX\_CLK1.

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane +	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Figure 2-107 RK3568 MIPI CSI working mode and data, clock allocation

- Please pay attention to the design of MIPI CSI RX:
  - MIPI\_CSI\_RX\_AVDD\_0V9, MIPI\_CSI\_RX\_AVDD\_1V8 power pin and VDDA0V9\_IMAGE, VCCA1V8\_IMAGE are required to be isolated with magnetic beads. Please refer to the schematic design for details;

al	C2134 2	1 1uF X5R 6.3V VDDA0V9_IMAGE O	FB2102 1 2 120R-100MHz	MIPI AVDD 0V9
ןוי'		C0402 VCCA1V8 TMACE O	0.030ohm L0603	
- at	C2135 2	1 1uF X5R 6.3V -	FB2103 1 2 120R-100MHz	MIPI AVDD 1V8
I		C0402	0.030ohm L0603	<b>_</b>

Figure 2-108 MIPI CSI PHY power circuit isolated with magnetic beads

• To improve MIPI CSI RX performance, the decoupling capacitors of every PHY power supply cannot be deleted, and they should be placed close to power pins when layout.

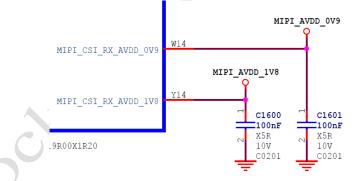


Figure 2-109 MIPI CSI RX PHY power decoupling capacitors

The matching design recommendations of MIPI CSI RX interface are shown in the following Table.

Signal	Connection mode	Description
MIPI_CSI_RX_D0P/D0N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke. Common mode inductor is reserved for EMI suppression	MIPI CSI data Lane0 input
MIPI_CSI_RX_D1P/D1N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke.	MIPI CSI data Lane1 input

Copyright © 2022 Rockchip Electronics Co., Ltd.

## **RK3568 Hardware Design Guide**

Signal	Connection mode	Description
MIPI_CSI_RX_D2P/D2N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke.	MIPI CSI data Lane2 input
MIPI_CSI_RX_D3P/D3N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke.	MIPI CSI data Lane3 input
MIPI_CSI_RX_CLK0P/CLK0N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke.	MIPI CSI clock0 input
MIPI_CSI_RX_CLK1P/CLK1N	Direct connection, to restrain electromagnetic radiation, and reserve common mode choke.	MIPI CSI clock1 input

### 2.3.9.2 CIF ( DVP ) Interface

CIF I/O domain supplies power to VCCIO6. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of product Camera (1.8V or 3.3V). Meanwhile, the pull-up level of I2C must be consistent with the power supply, otherwise it will cause abnormal or unable operation of the Camera. Please note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and may damage the IO.

	CIF D0 CIF D1 CIF D2		(			
CIF D2       / EEC SDD02       / SDBMC2 D2 M0       / IC31 LEOK TX M1       / VOP BT656 D2 M1       OPIO3 D0 4         CIF D3       / EBC SDD04       SDMMC2 CMD M0       / I231 SDD0 M1       / VOP BT656 D3 M1       GEIO3 D2 4         CIF D4       / EBC SDD04       SDMMC2 CMD M0       / I231 SD10 M1       / VOP BT656 D5 M1       GEIO3 D2 4         CIF D5       / EBC SDD05       / SDMMC2 CMN M0       / I231 SD11 M1       / VOP BT656 D5 M1       GEIO3 D3 4         CIF D6       / EBC SDD05       / SDMMC2 DET M0       / I231 SD13 M1       / VOP BT656 D5 M1       GEIO3 D5 4         CIF D7       / EBC SDD07       / SDMMC2 DET M0       / I231 SD13 M1       / VOP BT656 D7 M1       GEIO3 D6 4         CIF D7       / EBC SDD08       / GMAC1 TXD2 M1       / UART1 TX M1       / FDM CLK0 M1       GEIO3 D7 6         CIF D1       / EBC SDD01       / GMAC1 TXD1 M1       / UART1 TX M1       / FDM CLK0 M1       GEIO3 D7 4         CIF D10       / EBC SDD01       / GMAC1 TXD2 M1       / UART1 TX M2       / FDM SD1 M1       GEIO4 A1 A         CIF D11       / EBC SDD011       / GMAC1 TXD3 M1       / UART7 TX M2       / FDM SD1 M1       GEIO4 A1 A         CIF D12       / EBC SDD013       / GMAC1 TXD0 M1       / UART7 TX M2       / FDM SD1 M1       GEIO4 A3 A			/ SLMMC2 DU MU	/ 1281 MCLK M1	/ VOP BT656 D0 M1 /	GPIO3 C6 d
CIF D3       / EBC SDD03       / SDBMC2 D3 M0       / IZ31 SDD0 M1       / VOP BT656 D3 M1 / GP103 D1 d         CIF D5       / EBC SDD05       / SDBMC2 CMD M0       / IZ31 SD11 M1       / VOP BT656 D4 M1 / GP103 D2 d         CIF D5       / EBC SDD05       / SDBMC2 DE M0       / IZ31 SD11 M1       / VOP BT656 D5 M1 / GP103 D2 d         CIF D5       / EBC SDD05       / SDBMC2 DE M0       / IZ31 SD12 M1       / VOP BT656 D5 M1 / GP103 D5 d         CIF D7       / EBC SDD05       / SDBMC2 DE M0       / IZ31 SD13 M1       / VOP BT656 D7 M1 / GP103 D5 d         CIF D7       / EBC SDD09       / GMAC1 TXD2 M1       / UART1 TX M1       / FDM CLK0 M1       GP103 D7 d         CIF D1       / EBC SDD09       / GMAC1 TXD2 M1       / UART1 TX M1       / FDM CLK0 M1       GP103 D7 d         CIF D10       / EBC SDD01       / GMAC1 TXD2 M1       / UART1 TX M1       / FDM CLK1 M1       GP104 A0 d         CIF D12       / EBC SDD01       / GMAC1 TXD2 M1       / UART1 TX M2       / FDM SD13 M1       GP104 A1 d         CIF D12       / EBC SDD012       / GMAC1 TXD2 M1       / UART7 TX M2       / FDM SD12 M1       GP104 A2 d         CIF D13       / EBC SDD014       / GMAC1 TXD1 M1       / UART7 TX M2       / IZ32 LRCK RX M1 / GP104 A3 d         CIF D14       / EBC SDD015 <t< td=""><td>CIF D2</td><td>/ EBC SDDO1</td><td>/ SDMMC2 D1 M0</td><td>/ I2S1 SCLK TX M1</td><td>/ VOP BT656 D1 M1 /</td><td>GPI03 C7 d</td></t<>	CIF D2	/ EBC SDDO1	/ SDMMC2 D1 M0	/ I2S1 SCLK TX M1	/ VOP BT656 D1 M1 /	GPI03 C7 d
CHF P4         / ERC SDD04         / SDRMC2 CMD M0         / IASI SDIO M1         / VOF BIESS P4 M1         / GPI03 D2 G           CIF D5         / ERC SDD05         / SDRMC2 CHK M0         / IASI SDI1 M1         / VOF BIESS D5         M1 / GPI03 D2 G           CIF D6         / ERC SDD05         / SDRMC2 DET M0         / IASI SDI2 M1         / VOF BIESS D5         M1 / GPI03 D3 d4           CIF D7         / ERC SDD05         / SDRMC2 PWREN M0         / IASI SDI3 M1         / VOF BIESS D5         M1 / GPI03 D5 d           CIF D8         / ERC SDD05         / GMAC1 TXD2 M1         / UARTI TX M1         / FDM CLK0 M1         / GPI03 D5 d           CIF D8         / ERC SDD01         / GMAC1 TXD2 M1         / UARTI TX M1         / FDM SDI1 M1         / GPI03 D5 d           CIF D10         / ERC SDD010         / GMAC1 TXD2 M1         / UARTI TX M1         / FDM SDI1 M1         / GPI03 D7 d           CIF D11         / ERC SDD011         / GMAC1 TXD2 M1         / UARTI TX M2         / FDM SDI1 M1         / GPI04 A0 d           CIF D12         / ERC SDD013         / GMAC1 TXD2 M1         / UARTI TX M2         / FDM SDI3 M1         / GPI04 A2 d           CIF D13         / ERC SDD013         / GMAC1 TXD0 M1         / UARTI TX M2         / FDM SD13 M1         / GPI04 A3 d           CIF D14         <		/ EBC SDDO2	/ SDMMC2 D2 M0	/ I2S1 LRCK TX M1	/ VOP BT656 D2 M1 /	GPIO3 D0 d
CIF D5       / EBC SDDO5       / SDBMC2 CLK M0       / IZ81 SD11 M1       / VOP BT656 D5 M1 / GP103 D3 d1         CIF D6       / EBC SDDO6       / SDBMC2 DET M0       / IZ81 SD12 M1       / VOP BT656 D5 M1 / GP103 D4 d1         CIF D7       / EBC SDDO6       / SDBMC2 DET M0       / IZ81 SD13 M1       / VOP BT656 D7 M1 / GP103 D4 d1         CIF D7       / EBC SDD07       / SDMMC2 PWREN M0       / IZ81 SD13 M1       / VOP BT656 D7 M1 / GP103 D5 d1         CIF D7       / EBC SDD08       / GMAC1 TXD2 M1       / UART1 TX M1       / PDM CLK0 M1       / GP103 D6 d1         CIF D10       / EBC SDD010       / GMAC1 TXD3 M1       / UART1 TX M1       / FDM SD10 M1       GP103 D7 d1         CIF D11       / EBC SDD011       / GMAC1 TXD3 M1       / UART7 TX M2       / FDM SD11 M1       / GP104 A2 d1         CIF D11       / EBC SDD012       / GMAC1 TXD3 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A2 d1         CIF D12       / EBC SDD013       / GMAC1 TXD3 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A2 d1         CIF D14       / EBC SDD014       / GMAC1 TXD1 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A3 d1         CIF D14       / EBC SDD015       / GMAC1 TXD1 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A3 d1         <						
CHF P6         / ERC SDD05         / SDRMC2 DET M0         / IX31 SD12 M1         / VOP ER555 D5 M1         / GP103 D4 4           C1F D7         / ERC SDD07         STRMC2 PWEN M0         / IX31 SD13 M1         / VOP ER555 D5 M1         / GP103 D5 4           C1F D7         / ERC SDD07         STRMC2 PWEN M0         / IX31 SD13 M1         / VOP ER555 D7 M1         GP103 D5 4           C1F D8         / ERC SDD05         / GMAC1 TXD3 M1         / UART1 TX M1         / PDM SD10 M1         / GP103 D6 4           C1F D10         / ERC SDD010         / GMAC1 TXD3 M1         / UART1 TX M1         / FDM SD10 M1         / GP103 A0 4           C1F D10         / ERC SDD010         / GMAC1 TXD2 M1         / UART1 TX M2         / FDM SD10 M1         / GP104 A0 d           C1F D12         / ERC SDD013         / GMAC1 RXD3 M1         / UART7 TX M2         / FDM SD13 M1         / GP104 A2 d           C1F D13         / ERC SDD013         / GMAC1 RXD1 M1         / UART7 TX M2         / I282 LRCK TX M1 / GP104 A3 d           C1F D14         / EBC SDD014         / GMAC1 TXD1 M1         / UART7 TX M2         / I282 LRCK RX M1 / GP104 A6 d           C1FF D15         / ERC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I283 LRCK RX M1 / GP104 A6 d           C1FF D14         / EBC SDD014         / GMAC1 TXD1						
CHE D7         / EBC SDD07         / SDM4C2 FWREN M0         / I281 SDI3 M1         / VOP BT656 D7 M1         / GPI03 D5 d           CLF D8         / EBC SDD08         GMAC1 TXD2 M1         / UART1 TX M1         / FDM CLK0 M1         / GPI03 D5 d           CLF D8         / EBC SDD08         GMAC1 TXD2 M1         / UART1 TX M1         / FDM SDI0 M1         / GPI03 D5 d           CLF D10         / EBC SDD010         GMAC1 TXD2 M1         / UART1 RX M1         / FDM SDI0 M1         / GPI04 A0 d           CLF D11         / EBC SDD011         / GMAC1 RXDE M1         / UART7 TX M2         / FDM SDI1 M1         GPI04 A0 d           CLF D12         / EBC SDD013         / GMAC1 RXDE M1         / UART7 TX M2         / FDM SDI1 M1         GPI04 A3 d           CLF D13         / EBC SDD015         / GMAC1 TXD0 M1         / UART7 TX M2         / FDM SDI3 M1         GPI04 A3 d           CLF D14         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I282 LRCK RX M1         GPI04 A5 d           CLF D15         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I281 SCH RX M1         GPI04 A6 d           CLF D14         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I281 SCH RX M1         GPI04 A6 d           CLF D15         / EBC SDCE1 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						
CIF D8         / EBC SDD03         / GMAC1 TXD2 M1         / UART1 TX M1         / FDM CLK0 M1         / GP103 D6 d           CIF D5         / EBC SDD03         / GMAC1 TXD3 M1         / UART1 TX M1         / FDM SD10 M1         / GP103 D7 d           CIF D5         / EBC SDD01         / GMAC1 TXD3 M1         / UART1 TX M1         / FDM SD10 M1         / GP103 D7 d           CIF D1         / EBC SDD01         / GMAC1 TXD3 M1         / UART1 TX M2         / FDM SD11 M1         / GP104 A0 d           CIF D12         / EBC SDD012         / GMAC1 TXD3 M1         / UART7 TX M2         / FDM SD12 M1         / GP104 A2 d           CIF D13         / EBC SDD012         / GMAC1 TXD0 M1         / UART7 TX M2         / FDM SD12 M1         / GP104 A2 d           CIF D14         / EBC SDD014         / GMAC1 TXD0 M1         / UART7 TX M2         / FDM SD12 M1         / GP104 A3 d           CIF D15         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I282 LRCK TX M1         / GP104 A3 d           CIF D15         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I281 SDCK M1         / GP104 A3 d           CIF D15         / EBC SDD015         / GMAC1 TXD1 M1         / UART7 TX M2         / I281 SDCK X M1         / GP104 A3 d           CAM CLKOUT0         / EB						
CHE DS       / ERC SDD05       / GNACI TXD1 MI       / UARTI RX MI       / FDM SD10 MI       / GP103 D7 G         CHF D10       / ERC SDD010       / GHACI TXD1 MI       / UARTI RX MI       / FDM SD10 MI       / GP104 A0 G         CHF D11       / ERC SDD011       / GHACI RXD2 MI       / UARTI TX M2       / FDM SD11 MI       / GP104 A1 G         CHF D12       / ERC SDD013       / GHACI RXD2 MI       / UARTI RX M2       / FDM SD12 MI       / GP104 A2 G         CHF D13       / ERC SDD014       / GHACI RXDE MI       / UARTI RX M2       / FDM SD13 MI       / GP104 A2 G         CHF D14       / ERC SDD014       / GMACI RXDE MI       / UARTI RX M2       / FDM SD13 MI       / GP104 A3 G         CHF D14       / ERC SDD015       / GMACI TXD0 MI       / UARTI RX M2       / I282 LRCK RX MI / GP104 A5 G         CLF D15       / ERC SDD015       / GMACI TXD1 MI       / UARTI RX M2       / I281 SCLK RX MI / GP104 A5 G         IAR FLASHTRIGOUT       / ERC SDCE0       / GMACI TXEN M1       / SF13 CS0 M0       / I281 SCLK RX M1 / GP104 A5 G         IAR FLASHTRIGOUT       / ERC SDCE1       / GMACI RXD1 MI       / SF13 CS0 M0       / I281 SCLK RX M1 / GP104 A5 G         CAM CLKOUT0       / ERC SDCE3       / GMACI RXDV CRS MI       / I281 SCLK M1 / GP104 A5 G         IAR FLASHTRIGOUT	CIF D7	/ EBC SDD07	/ SDMMC2 PWREN MO	/ I2S1 SDI3 M1	/ VOP BT656 D7 M1 /	GPIO3 D5 d
CHE DS       / ERC SDD05       / GNACI TXD1 MI       / UARTI RX MI       / FDM SD10 MI       / GP103 D7 G         CHF D10       / ERC SDD010       / GHACI TXD1 MI       / UARTI RX MI       / FDM SD10 MI       / GP104 A0 G         CHF D11       / ERC SDD011       / GHACI RXD2 MI       / UARTI TX M2       / FDM SD11 MI       / GP104 A1 G         CHF D12       / ERC SDD013       / GHACI RXD2 MI       / UARTI RX M2       / FDM SD12 MI       / GP104 A2 G         CHF D13       / ERC SDD014       / GHACI RXDE MI       / UARTI RX M2       / FDM SD13 MI       / GP104 A2 G         CHF D14       / ERC SDD014       / GMACI RXDE MI       / UARTI RX M2       / FDM SD13 MI       / GP104 A3 G         CHF D14       / ERC SDD015       / GMACI TXD0 MI       / UARTI RX M2       / I282 LRCK RX MI / GP104 A5 G         CLF D15       / ERC SDD015       / GMACI TXD1 MI       / UARTI RX M2       / I281 SCLK RX MI / GP104 A5 G         IAR FLASHTRIGOUT       / ERC SDCE0       / GMACI TXEN M1       / SF13 CS0 M0       / I281 SCLK RX M1 / GP104 A5 G         IAR FLASHTRIGOUT       / ERC SDCE1       / GMACI RXD1 MI       / SF13 CS0 M0       / I281 SCLK RX M1 / GP104 A5 G         CAM CLKOUT0       / ERC SDCE3       / GMACI RXDV CRS MI       / I281 SCLK M1 / GP104 A5 G         IAR FLASHTRIGOUT	OTE DO	/ PRG SDDC0	( CMR.C1	/ TINDON1 MY M1	/ DDM CTEO M1 /	CD702 DC 1
CIF D10       / EBC SDD010       / GMAC1 TXCLK M1       / FDM CLK1 M1       / GP104 A0 d         CIF D11       / EBC SDD012       / GMAC1 FXD2 M1       / DART7 TX M2       / FDM SD11 M1       / GP104 A1 d         CIF D12       / EBC SDD012       / GMAC1 FXD3 M1       / UART7 TX M2       / FDM SD12 M1       / GP104 A2 d         CIF D13       / EBC SDD012       / GMAC1 FXD3 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A2 d         CIF D14       / EBC SDD014       / GMAC1 TXD0 M1       / UART7 TX M2       / FDM SD12 M1       / GP104 A3 d         CIF D14       / EBC SDD015       / GMAC1 TXD0 M1       / UART7 TX M2       / I282 LRCK RX M1       / GP104 A3 d         CIF D15       / EBC SDD015       / GMAC1 TXEN M1       / UART7 SX M2       / I281 SCLK RX M1       / GP104 A5 d         LIP D15       / EBC SDD01       / GMAC1 TXEN M1       / SP13 C80 M0       / I281 SCLK RX M1       / GP104 A6 d         CAM CLK0UT0       / EBC SDCE2       / GMAC1 RXD1 M1       / SP13 M150 M0       / I281 SD01 M1       / GP104 A7 d         ISP FRELIGHT TRIG / EBC SDCE3       / GMAC1 RXD2 KR M1       / SP13 M051 M0       / I281 SD02 M1       / GP104 B1 d         I2C4 SDA M0       / EBC SDCE3       / GMAC1 RXER M1       / SP13 M051 M0       / I282 SD1 M1       GP104 B3 d <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						
CHE DI1 / ERC SDD011 / GNACI FXD2 M1 / UARTY TX M2 / FDM SDT1 M1 / GP104 A1 G CIF D12 / ERC SDD012 / GMACI FXD3 M1 / UARTY TX M2 / FDM SDT3 M1 / GP104 A2 d CIF D13 / ERC SDD013 / GMACI FXD4 M1 / UARTY TX M2 / FDM SDT3 M1 / GP104 A3 d CIF D14 / ERC SDD014 / GMACI TXD0 M1 / UARTY TX M2 / I282 LRCK TX M1 / GP104 A3 d CIF D15 / ERC SDD015 / GMACI TXD0 M1 / UARTY TX M2 / I282 LRCK TX M1 / GP104 A3 d CIF D15 / ERC SDD015 / GMACI TXD1 M1 / UARTY TX M2 / I282 LRCK TX M1 / GP104 A3 d CIF D15 / ERC SDD015 / GMACI TXD1 M1 / UARTY TX M2 / I282 LRCK RX M1 / GP104 A5 d I8F FLASHTRIGOUT / ERC SDCE0 / GMACI TXD1 M1 / SF13 C80 M0 / I281 SCK RX M1 / GP104 A5 d CAM CLKOUT0 / ERC SDCE1 / GMACI TXD1 M1 / SF13 C81 M0 / I281 LRCK RX M1 / GP104 A6 d CAM CLKOUT1 / ERC SDCE1 / GMACI RXD0 M1 / SF13 M190 M0 / I281 SD01 M1 / GP104 A7 d CAM CLKOUT1 / ERC SDCE2 / GMACI RXD1 M1 / SF13 M190 M0 / I281 SD01 M1 / GP104 B1 d I204 SDA M0 / ERC SDCE3 / GMACI RXDV CRS M1 / SF13 M051 M0 / I282 SD1 M1 / GP104 B2 d I204 SDA M0 / ERC GDOE / ETH1 REFCLKO 25M M1 / SF13 M051 M0 / I282 SD1 M1 / GP104 B2 d I202 SDA M1 / ERC GDOE / ETH1 REFCLKO 25M M1 / SF13 M051 M0 / I282 SD1 M1 / GP104 B2 d I202 SDA M1 / ERC GDSE / CAM2 TX M0 / I281 SD03 M1 / GP104 B2 d I202 SDA M1 / ERC GDSE / CAM2 TX M0 / I281 SD03 M1 / GP104 B2 d I202 SDA M1 / ERC GDSE / CAM2 TX M0 / I282 SD1 M1 / GP104 B3 d I202 SDA M1 / ERC GDSE / CAM2 TX M0 / I281 SD03 M1 / GP104 B3 d I202 SDA M1 / ERC GDSE / GMAC1 RXCM 1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF CLKOUT / ERC GDCLK / FMAC1 MDC M1 / UART1 RTSA M1 / I282 NCLK M1 / GP104 B5 d CIF CLKOUT / EBC GDCLK / FMAC1 MDC M1 / UART1				/ UARTI RA MI		
CIF D12       / EBC SDD012 / GMAC1 RXD3 M1       / UART7 TX M2       / FDM SD12 M1       / GP104 A2 d         CIF D13       / EBC SDD014 / GMAC1 RXD1 M1       / UART7 TX M2       / FDM SD13 M1       / GP104 A3 d         CIF D14       / EBC SDD014 / GMAC1 TXD1 M1       / UART7 TX M2       / I282 LRCK TX M1 / GP104 A4 d         CIF D15       / EBC SDD015 / GMAC1 TXD1 M1       / UART9 TX M2       / I282 LRCK TX M1 / GP104 A4 d         ISP FLASHTRIGOUT / EBC SDCE0 / GMAC1 TXEN M1       / UART9 TX M2       / I281 SCLK RX M1 / GP104 A5 d         ISP FLASHTRIGOUT / EBC SDCE1 / GMAC1 TXEN M1       / SP13 C80 M0       / I281 SCLK RX M1 / GP104 A6 d         CAM CLKOUT0       / EBC SDCE1 / GMAC1 RXD0 M1       / SP13 C81 M0       / I281 SD01 M1 / GP104 A6 d         CAM CLKOUT0       / EBC SDCE2 / GMAC1 RXD0 M1       / SP13 M150 M0       / I281 SD01 M1 / GP104 A7 d         CAM CLKOUT0       / EBC SDCE3 / GMAC1 RXDV CRS M1       / I281 SD02 M1 / GP104 B1 d       / GP104 B1 d         I204 SDA M0       / EBC GDCE / ETR1 REFCLK0 25M M1 / SP13 CLK M0       / I282 SD1 M1 / GP104 B3 d       / GP104 B3 d         I202 SDA M1       / EBC GDSP / CAN2 RX M0       / I281 SD03 M1 / GP104 B3 d       / I281 SD03 M1 / GP104 B5 d       / I281 SD03 M1 / GP104 B5 d         CIF HREF       / EBC SDSHR / CAN2 RX M0       / I281 RT M1 / I282 SCLK M1 / GP104 B5 d       / I282 SCLK M1 / GP104 B7 d <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td></td<>						
CIF DI3       / EBC SDD013       / GNAC1 FXCLK M1       / UARTY RX M2       / FDM SDI3 M1       / GPI04 A3 G         CIF DI4       / EBC SDD014       / GNAC1 TXD1 M1       / UARTY RX M2       / I282 LRCK RX M1       / GPI04 A3 G         CIF DI5       / EBC SDD015       / GMAC1 TXD1 M1       / UARTY RX M2       / I282 LRCK RX M1       / GPI04 A3 G         ISP FLASHTRIGOUT       / EBC SDD015       / GMAC1 TXD1 M1       / UARTY RX M2       / I282 LRCK RX M1       GPI04 A5 d         ISP FLASHTRIGOUT       / EBC SDCE0       / GMAC1 TXEN M1       / SPI3 C80 M0       / I281 SCLK RX M1       GPI04 A6 d         CAM CLKOUT0       / EBC SDCE1       / GMAC1 RXD1 M1       / SPI3 C81 M0       / I281 SDO1 M1       GPI04 A7 d         CAM CLKOUT1       / EBC SDCE2       / GMAC1 RXD1 M1       / SPI3 MISO M0       / I281 SDO1 M1       GPI04 B1 d         ISP FRELIGHT TRIG       / EBC SDCE3       / GMAC1 RXD1 CR5 M1       / SPI3 MOSI M0       / I282 SDI M1       GPI04 B2 d         I204 SDL M0       / EBC SDCE4       / GMAC1 RXD1 CR5 M1       / SPI3 CLK M0       / I282 SDI M1       GPI04 B2 d         I204 SDL M0       / EBC SDCE3       / GMAC1 RXER M1       / SPI3 CLK M0       / I282 SDI M1       GPI04 B2 d         I204 SDL M0       / EBC SDCE4       / ENTH REFCLK0 25M M1       /				/ UART7 TX M2		
CIF D14       / EBC SDD014       / GNACI TXD0 MI       / UART5 TX M2       / I282 LECK TX MI / GP104 A4 d         CIF D15       / EBC SDD015       / GNACI TXD1 MI       / UART5 EX M2       / I282 LECK EX MI / GP104 A5 d         IAP FLASHTRIGOUT       / EBC SDCE0       / GNACI TXD1 MI       / UART5 EX M2       / I282 LECK EX MI / GP104 A5 d         IAP FLASHTRIGOUT       / EBC SDCE0       / GNACI EXD0 M1       / SPI3 CS0 M0       / I281 SCLK EX M1 / GP104 A6 d         CAM CLKOUT0       / EBC SDCE1       / GNACI EXD0 M1       / SPI3 CS1 M0       / I281 LECK EX M1 / GP104 A7 d         CAM CLKOUT1       / EBC SDCE2       GNACI EXD0 M1       / SPI3 MIS0 M0       / I281 SD01 M1       GP104 B0 d         ISP FRELIGHT TRIG       / EBC SDCE3       / GNACI EXDV CRS M1       / I281 SD02 M1       / GP104 B1 d         I204 SDA M0       / EBC COM       / GNACI EXER M1       / SPI3 MOSI M0       / I282 SDI M1       / GP104 B2 d         I204 SCA M0       / EBC GDGE       / ETH1 REFCLKO 25M M1       / SPI3 CLK M0       / I282 SDI M1       / GP104 B3 d         I202 SDA M1       / EBC GDSF       / CAN2 EX M0       / I38P FLASH TRIGIN       / VOP ET555 CLK M1/ GP104 B5 d         I202 SCL M1       / EBC SDDE       / GNACI MDC M1       / UART1 RT55 M1       / I282 M1       GP104 B5 d         CIF HRE						
CHF         D15         / EBC SDD015         / GMACL TXD1 ML         / UART9 RX M2         / I282 LRCK RX M1         / GP104 A5 d           IRP_FLASHTRIGOUT         / EBC SDCE0         / GMACL TXEN M1         / SPI3 C80 M0         / I281 SCLK RX M1         / GP104 A5 d           CAM_CLEOUTO         / EBC SDCE1         / GMACL RXD0 M1         / SPI3 C81 M0         / I281 LRCK RX M1         / GP104 A5 d           CAM_CLEOUTO         / EBC SDCE1         / GMACL RXD0 M1         / SPI3 MISO M0         / I281 LRCK RX M1         / GP104 A7 d           CAM_CLEOUTO         / EBC SDCE2         / GMACL RXD1 M1         / SPI3 MISO M0         / I281 SD02 M1         / GP104 B1 d           ISP_FRELIGHT_TRIG         / EBC SDCE3         / GMACL RXDV CRS M1         / SPI3 MOSI M0         / I282 SD1 M1         / GP104 B1 d           I204 SDL M0         / EBC SDCE3         / GMACL RXDV CRS M1         / SPI3 CLK M0         / I282 SD1 M1         / GP104 B2 d           I204 SDL M0         / EBC SDCE3         / GMACL RXDV CRS M1         / SPI3 CLK M0         / I282 SD1 M1         / GP104 B2 d           I204 SDL M0         / EBC SDCE3         / GMACL RXDV CRS M1         / SPI3 CLK M0         / I282 SD1 M1         / GP104 B2 d           I202 SDL M1         / EBC SDCE3         / GMACL RXDV CRS M1         SPI3 CLK M0         / I283 SD0 M1						
ISP FLASHTRIGOUT / ERC SDCE0 / GMAC1 TXEN M1 / SPI3 C80 M0 / I281 SCLK RX M1 / GPI04 A6 d CAM CLKOUT0 / ERC SDCE1 / GMAC1 RXD0 M1 / SPI3 C81 M0 / I281 SCLK RX M1 / GPI04 A7 d CAM CLKOUT1 / EBC SDCE2 / GMAC1 RXD1 M1 / SPI3 MISO M0 / I281 SD01 M1 / GPI04 B0 d ISP FRELIGHT TRIG / EBC SDCE3 / GMAC1 RXDV CRS M1 / SPI3 MOSI M0 / I282 SD1 M1 / GPI04 B1 d I204 SDA M0 / EBC VCOM / GMAC1 RXER M1 / SPI3 MOSI M0 / I282 SD1 M1 / GPI04 B2 d I204 SDA M0 / EBC GDCE / ETH1 REFCLKO 25M M1 / SPI3 CLK M0 / I282 SD1 M1 / GPI04 B2 d I202 SDA M1 / EBC GDSP / CAN2 RX M0 / I287 SDO M1 / GPI04 B3 d I202 SDA M1 / EBC GDSP / CAN2 RX M0 / I287 SDO M1 / GPI04 B5 d I202 SCL M1 / EBC SDRR / CAN2 TX M0 / I287 SLK M0 / I281 SDO3 M1 / GPI04 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RT9n M1 / I282 NCLK M1 / GPI04 B5 d CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RT9n M1 / I282 NCLK M1 / GPI04 B5 d CIF CLKOUT / EBC GDCLK / FWM11 IR M1 GPI04 D7 d CIF CLKOUT / EBC GDCLK / FWM11 IR M1 GPI04 C0 d						
CAM CLKOUTO / ERC SDCE1 / GMAC1 RXDO M1 / SPI3 C81 M0 / I281 LRCK RX M1 / GPI04 A7 d CAM CLKOUT1 / EBC SDCE2 / GMAC1 RXDI M1 / SPI3 MISO M0 / I281 SDO1 M1 / GPI04 B0 d I39 FRELIGHT TRIG / EBC SDCE3 / GMAC1 RXDV CRS M1 / SPI3 MOSI M0 / I281 SDO2 M1 / GPI04 B1 d I204 SDA M0 / EBC VCOM / GMAC1 RXEW CRS M1 / SPI3 MOSI M0 / I282 SDI M1 / GPI04 B2 d I204 SDA M0 / EBC VCOM / GMAC1 RXEW M1 / SPI3 MOSI M0 / I282 SDI M1 / GPI04 B2 d I204 SDA M0 / EBC GDCE / ETH1 REFCLKO 25M M1 / SPI3 CLK M0 / I282 SDI M1 / GPI04 B3 d I202 SDA M1 / EBC GDSP / CAN2 RX M0 / I38F FLASH TRIGIN / VOP B1656 CLK M1/ GPI04 B3 d I202 SCL M1 / EBC SDSHR / CAN2 TX M0 / I38F FLASH TRIGIN / VOP B1656 CLK M1/ GPI04 B5 d C1F HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 MCLK M1 / GPI04 B5 d C1F HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 MCLK M1 / GPI04 B7 d C1F CLKOUT / EBC GDCLK / FWM11 IR M1 GPI04 B7 d						
CAM_CLEGUT1         / EBC_SDCE2         GMAC1_RXD1_M1         / SF13_MISO_M0         / I281_SD01_M1         / GP104_B0_d           ISP_PRELIGHT_TRIG         EBC_SDCE3         GMAC1_RXDV_CRS_M1         / I281_SD02_M1         / GP104_B1_d           I204_SDA_M0         / EBC_SDCE3         GMAC1_RXEN_CRS_M1         / I281_SD02_M1         / GP104_B1_d           I204_SDA_M0         / EBC_SDCE2         / GMAC1_RXEN_M1         / SP13_NOSI_M0         / I282_SDI_M1         / GP104_B2_d           I204_SCL_M0         / EBC_SDCE         / ERTI_REFCLENO_25M_M1         / SP13_CLK_M0         / I282_SDD_M1         / GP104_B3_d           I202_SDA_M1         / EBC_SDSP         / CAN2_RX_M0         / ISP_FLASH_TRIGIN         / VOP_BT656_CLK_M1/_GP104_B4_d           I202_SCL_M1         / EBC_SDSHR         / CAN2_RX_M0         / ISP_FLASH_TRIGIN         / VOP_BT656_CLK_M1/_GP104_B5_d           I202_SCL_M1         / EBC_SDSHR         / CAN2_RX_M0         / I281_SD03_M1         / GP104_B6_d           I202_SCL_M1         / EBC_SDSHR         / GMAC1_MDC_M1         / UART1_RTSn_M1         / I282_MCLK_M1         / GP104_B6_d           C1F_HREF         / EBC_SDCE         / GMAC1_MDC_M1         / UART1_RTSn_M1         / I282_SCLK_TX_M1         / GP104_B7_d           C1F_HREF         / EBC_SDCE         / GMAC1_MDIO_M1         / UART1_RTSn_M	ISP FLASHTRIGOU	F / EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CSO MO	/ 1281 SCLK RX M1 /	GPIO4 A6 d
CAM_CLEGUT1         / EBC_SDCE2         GMAC1_RXD1_M1         / SF13_MISO_M0         / I281_SD01_M1         / GP104_B0_d           ISP_PRELIGHT_TRIG         EBC_SDCE3         GMAC1_RXDV_CRS_M1         / I281_SD02_M1         / GP104_B1_d           I204_SDA_M0         / EBC_SDCE3         GMAC1_RXEN_CRS_M1         / I281_SD02_M1         / GP104_B1_d           I204_SDA_M0         / EBC_SDCE2         / GMAC1_RXEN_M1         / SP13_NOSI_M0         / I282_SDI_M1         / GP104_B2_d           I204_SCL_M0         / EBC_SDCE         / ERTI_REFCLENO_25M_M1         / SP13_CLK_M0         / I282_SDD_M1         / GP104_B3_d           I202_SDA_M1         / EBC_SDSP         / CAN2_RX_M0         / ISP_FLASH_TRIGIN         / VOP_BT656_CLK_M1/_GP104_B4_d           I202_SCL_M1         / EBC_SDSHR         / CAN2_RX_M0         / ISP_FLASH_TRIGIN         / VOP_BT656_CLK_M1/_GP104_B5_d           I202_SCL_M1         / EBC_SDSHR         / CAN2_RX_M0         / I281_SD03_M1         / GP104_B6_d           I202_SCL_M1         / EBC_SDSHR         / GMAC1_MDC_M1         / UART1_RTSn_M1         / I282_MCLK_M1         / GP104_B6_d           C1F_HREF         / EBC_SDCE         / GMAC1_MDC_M1         / UART1_RTSn_M1         / I282_SCLK_TX_M1         / GP104_B7_d           C1F_HREF         / EBC_SDCE         / GMAC1_MDIO_M1         / UART1_RTSn_M	CAM CLEOURO	/ FRC SDOFT	/ CMAC1 PYD0 M1	/ SDI3 CS1 M0	/ T291 T.DOW DV M1 /	GPT04 37 d
ISP_PRELIGHT_TRIG / EBC_SDCE3 / GMAC1_RXDV_CRS_M1         / I281_SDO2_M1 / GPI04_B1_d           I204_SDA_M0         / EBC_SDCE3 / GMAC1_RXER_M1 / SPI3_MOSI_M0 / I282_SDI_M1 / GPI04_B2_d           I204_SCL_M0         / EBC_GDOE / ETH1_REFCLK0_25M_M1 / SPI3_CLK_M0 / I282_SDD_M1 / GPI04_B3_d           I202_SDA_M1         / EBC_GDDE / ETH1_REFCLK0_25M_M1 / SPI3_CLK_M0 / I282_SDD_M1 / GPI04_B3_d           I202_SDA_M1         / EBC_GDSP_ / CAN2_RX_M0 / ISP_FLASH_TRIGIN / VOP_BT656_CLK_M1 / GPI04_B4_d           I202_SCL_M1         / EBC_SDSHR / CAN2_TX_M0 / ISP_FLASH_TRIGIN / VOP_BT656_CLK_M1 / GPI04_B5_d           CIF_HREF         / EBC_SDLE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_MCLK_M1 / GPI04_B6_d           CIF_HREF         / EBC_SDDE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_NCLK_M1 / GPI04_B6_d           CIF_CLKOUT         / EBC_SDCE / GMAC1_MDI0_M1           CIF_CLKOUT         / EBC_GDCLK						
12C4 SDA M0         / EBC VCOM         / GMAC1 BXER M1         / SPI3 MOSI M0         / I282 SDI M1         / GPI04 B2 d           12C4 SCL M0         / EBC GDOE         / ETRI REFCLKO 25M M1         / SPI3 CLK M0         / I282 SDO M1         / GPI04 B3 d           12C2 SDA M1         / EBC GDSP         / CAN2 RX M0         / ISP FLASH TRIGIN         / VOP B1656 CLK M1         / GPI04 B3 d           12C2 SDA M1         / EBC SDSH         / CAN2 RX M0         / ISP FLASH TRIGIN         / VOP B1656 CLK M1         / GPI04 B4 d           12C2 SCL M1         / EBC SDSHR         / CAN2 RX M0         / ISP FLASH TRIGIN         / VOP B1656 CLK M1         / GPI04 B5 d           C1F HREF         / EBC SDLE         / GMAC1 MDC M1         / UART1 RTSn M1         / I282 MCLK M1         / GPI04 B6 d           C1F VSYNC         / EBC SDOE         / GMAC1 MDIO M1         / I282 SCLK TX M1         / GPI04 B7 d           C1F CLKOUT         / EBC GDCLK         / FWM11 IR M1         GPI04 C0 d         /						01101 20 4
I2C4         SCL         M0         /         ERC         GDOE         /         ETH1         REFCLKO         25M         M1         /         SF13         CLK         M0         /         I282         SDO         M1         /         GF104         B3         G           I2C2         SDA         M1         /         EBC         GDSP         /         CAN2         RX         M0         /         I38P         FLASH         TRIGIN         /         VOP         BT656         CLK         M1         GP104         B4         d           I2C2         SCL         M1         /         EBC         SDSHR         /         CAN2         TX         M0         /         I281         SDO3         M1         /         GP104         B5         d           C1F         HREF         /         EBC         SDDE         /         GMAC1         MDC         M1         /         U282         MCLK         M1         GP104         B6         d         CLF         VSTNC         /         EBC         SDOE         /         GMAC1         MDIO         M1         /         L282         SCLK         TX         M1         GP104         B7	ISP PRELIGHT TR	IG / EBC SDCE3	/ GMAC1 RXDV CRS M1		/ 1281 SDO2 M1 /	GPIO4 B1 d
I2C4         SCL         M0         /         ERC         GDOE         /         ETH1         REFCLKO         25M         M1         /         SF13         CLK         M0         /         I282         SDO         M1         /         GF104         B3         G           I2C2         SDA         M1         /         EBC         GDSP         /         CAN2         RX         M0         /         I38P         FLASH         TRIGIN         /         VOP         BT656         CLK         M1         GP104         B4         d           I2C2         SCL         M1         /         EBC         SDSHR         /         CAN2         TX         M0         /         I281         SDO3         M1         /         GP104         B5         d           C1F         HREF         /         EBC         SDDE         /         GMAC1         MDC         M1         /         U282         MCLK         M1         GP104         B6         d         CLF         VSTNC         /         EBC         SDOE         /         GMAC1         MDIO         M1         /         L282         SCLK         TX         M1         GP104         B7						
I2C2 SDA MI         / EBC GDSP         / CAN2 RX M0         / I3P FLASH TRIGIN         / VOP BT656 CLK MI/ GPI04 B4 d           I2C2 SCL MI         / EBC SDSHR         / CAN2 TX M0         / I3P FLASH TRIGIN         / VOP BT656 CLK MI/ GPI04 B5 d           CIF HREF         / EBC SDLE         / GMAC1 MDC M1         / UART1 RTSn M1         / I282 MCLK M1         / GPI04 B6 d           CIF HREF         / EBC SDLE         / GMAC1 MDC M1         / UART1 RTSn M1         / I282 MCLK M1         / GPI04 B6 d           CIF VSYNC         / EBC SDCE         / GMAC1 MDIO M1         / UART1 RTSn M1         / I282 SCLK TX M1 / GPI04 B7 d           CIF CLKOUT         / EBC GDCLK         / FWM11 IR M1         GPI04 C0 d	I2C4 SDA MO	/ EBC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI MO	/ 1282 SDI M1 /	GPIO4 B2 d
12C2 SCL M1         / EBC SDSHR         / CAN2 TX M0         / I2S1 SD03 M1         / GPI04 B5 d           CIF HREF         / EBC SDLE         / GMAC1 MDC M1         / UARTI RTSn M1         / I2S2 MCLK M1         / GPI04 B6 d           CIF VSYNC         / EBC SDDE         / GMAC1 MDIO M1         / UARTI RTSn M1         / I2S2 SCLK TX M1         / GPI04 B7 d           CIF VSYNC         / EBC SDDE         / GMAC1 MDIO M1         / I2S2 SCLK TX M1         / GPI04 B7 d           CIF CLKOUT         / EBC GDCLK         / PWM11 IR M1         GPI04 C0 d	I2C4 SCL MO	/ EBC GDOE	/ ETH1 REFCLKO 25M M1	/ SPI3 CLK M0	/ 1282 SDO M1 /	GPIO4 B3 d
12C2 SCL M1         / EBC SDSHR         / CAN2 TX M0         / I2S1 SD03 M1         / GPI04 B5 d           CIF HREF         / EBC SDLE         / GMAC1 MDC M1         / UARTI RTSn M1         / I2S2 MCLK M1         / GPI04 B6 d           CIF VSYNC         / EBC SDDE         / GMAC1 MDIO M1         / UARTI RTSn M1         / I2S2 SCLK TX M1         / GPI04 B7 d           CIF VSYNC         / EBC SDDE         / GMAC1 MDIO M1         / I2S2 SCLK TX M1         / GPI04 B7 d           CIF CLKOUT         / EBC GDCLK         / PWM11 IR M1         GPI04 C0 d						
CIF HREF / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 MCLK M1 / GPI04 B6 d CIF VSYNC / EBC SDOE / GMAC1 MDIO M1 / I282 SCLK TX M1 / GPI04 B7.d CIF CLKOUT / EBC GDCLK / FWM11 IR M1 GPI04 C0 d				/ ISP FLASH TRIGIN		
CIF VSYNC / EBC SDOE / GMAC1 MDIO M1 / I282 SCLK TX M1 / GPIO4 B7 d CIF CLKOUT / EBC GDCLK / PWM11 IR M1 GPIO4 C0 d /	I2C2 SCL M1	/ EBC SDSHR	/ CAN2 TX M0		/ I2S1 SDO3 M1 /	GPIO4 B5 d
CIF VSYNC / EBC SDOE / GMAC1 MDIO M1 / I282 SCLK TX M1 / GPIO4 B7 d CIF CLKOUT / EBC GDCLK / PWM11 IR M1 GPIO4 C0 d /		/	1	(	(	
CIF CLEOUT / EBC GDCLK / FWM11 IR M1 GP104 C0 d				/ UARTI RTSh MI		
/	CIF VSINC	7 EBC SDOE	7 GMACI MDIO MI		/ 1282 SCLK TX MI /	GP104 B/ d
/	OTE OTROUM	/ PRC CDCTF		/ DRM11 TD M1		CDTO4 CO d
CIF CLKIN / EBC SDCLK / GMAC1 MCLKINOUT M1 / UART1 CTSn M1 / 1282 SCLK RX M1 / GPI04 C1 d	CIF CHROOT	/ EBC GDCHK		/ FWMII IK MI	/	GF104 C0 a
	CIE CLEIN	/ EBC SDCLK	/ GMAC1 MCLEINOUT M1	/ HART1 CTSp M1	/ T282 SCLE RX M1 /	GPT04 C1 d
	our ourer	7 220 02020	/ Chatter House House	, one of the	/ 1862 CODK KA MI /	01101 01 0

RK3568 BGA636 19R00X19R00X1R20

Figure 2-110 RK3568 CIF functional pins

- CIF interface supports following formats:
  - Support BT601 YCbCr 422 8bit input
  - ♦ Support BT656 YCbCr 422 8bit input
  - Support RAW 8/10/12bit input

Copyright © 2022 Rockchip Electronics Co., Ltd.

- Support BT1120 YCbCr 422 8/16bit input, single/dual-edge sampling
- Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input
- Relationship between 8/10/12/16bit data of CIF[15:0] is shown as follows, with high-order aligned.

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0			
CIF_D1	D1			
CIF_D2	D2			
CIF_D3	D3			
CIF_D4	D4	D0		
CIF_D5	D5	D1		
CIF_D6	D6	D2	D0	
CIF_D7	D7	D3	Dl	
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Figure 2-111 RK3568 Relationship between data of CIF

Data relationship in BT1120 16bit mode is shown as follows, and supports YC Swap.

	Table 2–24 RK3568 Data relationship in B11120 16bit mode					
	Pin Name	Defau	lt mode	Swap is enabled		
	P III INallie	Pixel #0	Pixel #1	Pixel #0	Pixel #1	
	CIF_D0	<b>Y</b> 0[0]	Y1[0]	Cb0[0]	Cr0[0]	
	CIF_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	
	CIF_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	
	CIF_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	
	CIF_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	
	CIF_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	
	CIF_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	
	CIF_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	
/	CIF_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	
	CIF_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	
	CIF_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	
	CIF_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	
	CIF_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	
	CIF_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	
	CIF_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	
	CIF_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	

Table 2–24 RK3568	Data relationship in	n BT1120 16bit mode

The pull up/down and matching design recommendations of CIF interface are shown in the following Table.

Signal	Pull up/down Inside	Connection, Mode	Description (chip end)
CIF_D[15:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF data input
CIF_HREF	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF row synchronous input
CIF_VSYNC	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF field synchronous input
CIF_CLKIN	Pull-down	Connect 220hm resistor in series, close to the device	CIF clock input
CIF_CLKOUT	Pull-down	Connect 220hm resistor in series, close to the chip	CIF clock output, can provide MCLK work clock for device.

25 DV25(0 CIE: / C

- When the board-to-board connection is through connectors, it is recommended to connect a resistor with a certain resistance in series (between 22ohm and 100ohm, as long as it can meet the SI test), and reserve TVS devices
- Note when designing MIPI CSI RX/CIF:
  - DVDD power supply of Camera is 1.2V/1.5V/1.8V, etc. Please provide accurate power supply according to the specifications of Camera. The reference circuit is 1.2V by default;
  - DVDD current of some Cameras is relatively large, if the current is more than 100mA, it is suggested to use DCDC for power supply;
  - Several power supplies of Camera require the power on sequence, please adjust the power on sequence according to the specifications of Camera, the default power on sequence in the schematic design is 1.8V-->1.2V-->2.8V;
  - When using the Camera with CIF interface, you should pay attention that DOVDD (IO power supply) of Camera must use the same voltage as VCCIO6 power supply;
  - When using two Cameras, the power supply can be separated or combined according to the actual requirements. The power supply in schematic design is separated by default.
  - For cameras with AF function, VCC2V8\_AF needs to supply the power separately or shares supply with AVCC2V8 DVP which should be separated by magnetic beads;
  - The decoupling capacitors of all power supplies of Camera should not be deleted, they must be reserved and placed close to the connector;
  - PWDN signal of Camera must be controlled by GPIO, and GPIO level must match with Camera IO level;
  - Reset signal of Camera is suggested to be controlled by GPIO, and GPIO level must match with Camera IO level. The 100nF capacitors of Reset signal should not be deleted and placed near the connector to enhance anti ESD capability;
  - MCLK of Camera can be got from:

2:CAM\_CLKOUT1

3:CIF\_CLKOUT

4:REFCLK\_OUT

Note: clock level must match with Camera IO level, if not, level conversion or resistor divider must be performed to match the level

• If two Cameras are the same model, note that whether I2C addresses are the same or not. If the address are the same, then two I2C buses are required.

# 2.3.10 Video Output Interface Circuit

RK3568 has a built-in VOP controller, three output Ports, and supports HDMI2.0 TX/MIPI DSI TX0/MIPIO DSI TX1/LVDS TX/eDP TX/RGB/BT1120/BT656 video interface output.

Path diagram of VOP and video interface output:

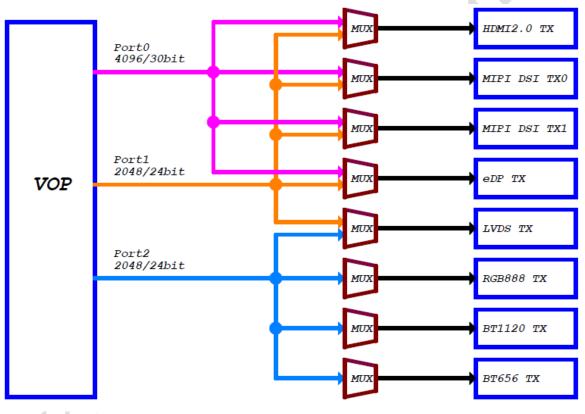


Figure 2-112 RK3568 the output path diagram of VOP and video interface

### 2.3.10.1 HDMI2.0 TX interface

RK3568 has a built-in HDMI2.0TX PHY with maximum output resolution up to 4096X2160@60Hz.

TMDS signal is shown in the following diagram, it is required to connect a 2.20hm resistor in series close to RK3568 end, the resistor cannot be deleted to improve the signal quality and strengthen anti ESD and surge capability.

		Diff 100 Ohm ±10% Diff 100 Ohm ±10%
HDMI2.0 TX	HDMI TX D2P	AG22 HDMI_TX2P R1702 1 2 2.2R 5% R0402 HDMI_TX2P_PORT
	HDMI_TX_D2N	
		AG21         HDMI_TX1P         R1700         2         2.2.R         5%         R0402         HDMI_TX1P         PORT           AH21         HDMI_TX1N         R1701         1         2         2.2.R         5%         R0402         HDMI_TX1P         HDMI_TX1N         HDMI_TX1N         HDMI_TX1N         PORT         HDMI_TX1N         HDMI_TX
	A	AG20 HDMI_TXOP R1704 1 2 2.2R 5% R0402 NHDMI TXOP PORT
	HDMI_TX_DOP A	AH20 HDMI_TXON R1705 1 2 2.2R 5% R0402 HDMI_TXON_PORT
		AH19 HDMI TXCLKP 2 2.2R 5% R0402
		AG19 HDMI_TXCLKN L1700 NC
	NDMI_IX_CLEN	Note: R1707 1 2 2.2R 59 R0402
		If common mode inductors are needed, it is recommended to keep 2.20hm in series to improve the antistatic abllity

Figure 2-113 RK3568 HDMI2.0 TX PHY TMDS pins

■ The power pins of HDMI\_TX\_AVDD\_0V9/1V8 should be placed with 4.7uF and 100nF decoupling capacitors, which cannot be deleted and be placed close to RK3568 pins when layout,

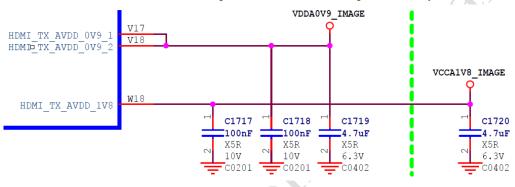


Figure 2-114 RK3568 HDMI2.0 TX PHY power supply decoupling capacitances

HDMI\_TX\_REXT is the external reference resistor pin of HDMI2.0TX PHY, connect a 1620Ω/1% resistor to ground, the value of resistance cannot be changed, and place the resistor close to RK3568 pins when layout.

HDMI\_TX\_HPDIN is a native function of HDMI2.0TX PHY. It supports 5V level, and the effective detection level is 2.4-5.3V. It is recommended to place a 100nF capacitor near the chip pin of RK3568 to eliminate jitter.



Figure 2-116 RK3568 HDMI2.0 TX PHY HPD pins

Near the end of HDMI connector, it needs to connect a 1Kohm resistor in series to strengthen anti ESD and surge capability., and you need reserve a 100Kohm resistor grounded.

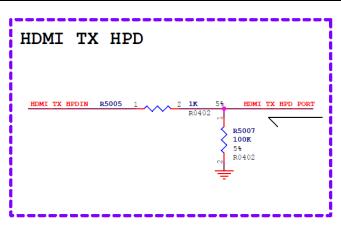


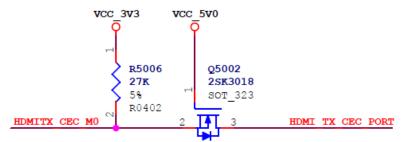
Figure 2-117 RK3568 HDMI2.0 TX PHY HPD circuit

HDMI\_TX\_CEC function is multiplexed in two locations, one is in the IO of VCCIO7 power domain, and the other is in the IO of PMUIO2 power domain; It is defined as 3.3V level in the CEC protocol, but the protocol requires that 3.3V voltage is added to the CEC pin by a 27K resistor and leakage current is not allowed to exceed 1.8uA.

Test ID 7-15: CEC Line Degradation				
Reference Requirement				
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be ≤1.8µA			

Figure 2-118 HDMI CEC protocol requirements

When RK3568 IO Domain is not powered on, if there is voltage on IO, it may cause electricity leakage. For example, RK3568 is power-off, and HDMI cable is still connected to Sink end (TV or monitor), at this time, CEC of Sink end is powered, and electricity will leak to RK3568 IO through HDMI cable, which will cause CEC leakage current of more than 1.8uA. Therefore, an isolation circuit needs to be added externally, and the resistance value of R5006 is not allowed to be modified at will. You need to use 27Kohm, and the default choice for Q5002 is 2SK3018. If you want to change to other models, the junction capacitance must be similar. If the junction capacitance is too large, it may not only influence working, but also fail the certification.





HDMI\_TX DDC\_SCL/DDC\_SDA is I2C/DDC bus of HDMI TX controller, its function multiplexes to the IO of VCCIO7 power domain. DDC\_SCL/DDC\_SDA is defined to 5V level in the protocol, while

RK3568 IO doesn't support 5V level, so the level conversion circuit must be added and cannot be deleted, Copyright © 2022 Rockchip Electronics Co., Ltd. 100

Using MOS tube for level conversion by default, and the MOS model is 2SK3018. If you want to change to other models, the junction capacitance must be similar. If the junction capacitance is too large, it may not only influence working, but also fail the certification.

It's recommend to use pull-up resistance with default value, and the value cannot be modified.

D5000 diode cannot be deleted to prevent electric leakage from Sink to VCC\_5V0.

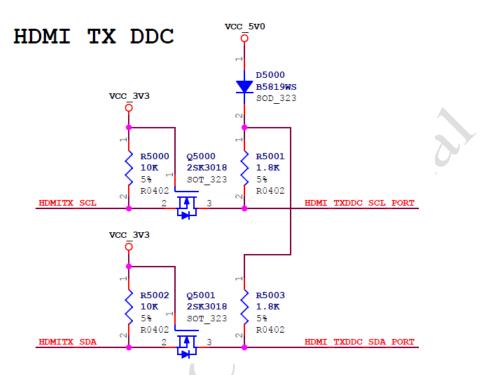


Figure 2-120 HDMI DDC level conversion circuit

- Make sure that Pin18 voltage of HDMI connector is between 4.8-5.3V, and the pin should be placed with 1uF decoupling capacitor, which cannot be deleted. The capacitor should be placed close to HDMI connector pins when layout.
- In order to enhance anti ESD capability, ESD devices must be reserved in signals, ESD parasitic capacitors of HDMI TMDS signal should not exceed 0.4pF, and ESD parasitic capacitors of other signals are recommended not to exceed 1pF.

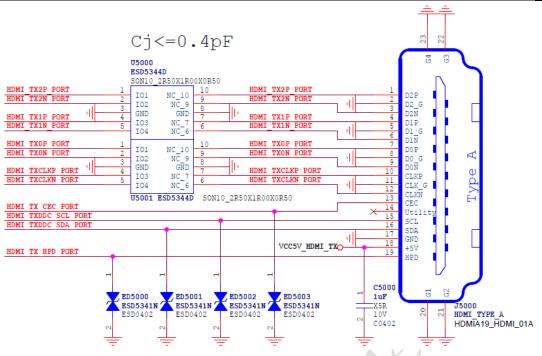


Figure 2-121 ESD circuit of HDMI connector

The matching design recommendations of HDMI2.0 TX interface are shown in the following Table.

Signal	Connection mode	Description		
HDMI_TX_D2P/D2N	Connect in series with a 2.20hm resistor	TMDS data Lane2 output		
HDMI_TX_D1P/D1N	Connect in series with a 2.20hm resistor	TMDS data Lane1 output		
HDMI_TX_D0P/D0N	Connect in series with a 2.20hm resistor	TMDS data Lane1 output		
HDMI_TX_CLKP/CLKNConnect in series with a 2.2ohm resistorCommon mode inductor is reserved for EMI suppression		TMDS clock output		
HDMI_TX_REXT	A 1620/1% ohm resistor grounded	A external reference resistor of HDMI2.0 TX PHY		
HDMI_TX_HPDIN	Connect in series with a 1000ohm resistor	HDMI IN test		
HDMITX_CEC	MOS isolation	HDMI CEC signal		
HDMITX_SCL	MOS level conversion	HDMI DDC clock		
HDMITX_SDA	MOS level conversion	HDMI DDC data input and output		

### Table 2-26 RK3568 HDMI2.0 TX interface design

## 2.3.10.2 MIPI DSI TX0/LVDS TX interface

RK3568 has a built-in MIPI DSI TX0 and a LVDS TX Combo PHY, it supports version MIPI V1.2 and has total 4Lane. The maximum output resolution of MIPI DSI TX0 is up to  $1920 \times 1080@60$ Hz, and the maximum output resolution of LVDS TX is up to  $1280 \times 800@60$ Hz.

MIPI	DSI	TX0/LVDS TX0	
			AH17
		MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	AG17
			AH16
		MIPI DSI TXO DIN/LVDS TXO DIN	AG16
			AH14
		MIPI_DSI_TX0_D2P/LVDS_TX0_D2P MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	AG14
			AH13
		MIPI_DSI_TX0_D3P/LVDS_TX0_D3P MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	AG13
			AH15
		MIPI DSI TX0 CLKP/LVDS TX0 CLKP	AG15

#### Figure 2-122 RK3568 MIPI DSI TX0/LVDS TX Combo PHY pins

Please note in the design of Mipi DSI tx0 and LVDS TX combo PHY

It's required to separate MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9,
 MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_1V8 power pins and VDDA0V9\_IMAGE, VCCA1V8\_IMAGE by magnetic beads. Please refer to schematic design for details;

at	C2134 2	1 1uF X5R 6.3V VDDA0V9_IMAGE O	FB2102 1 2 120R-100MHz	MIPI AVDD 0V9
_ ''I[		C0402 VCCA1V8 IMAGE	0.030ohm L0603	
l	C2135 2	1 1uF X5R 6.3V	FB2103 1 2 120R-100MHz	MIPI AVDD 1V8
L		C0402	0.030ohm L0603	

Figure 2-123 Magnetic bead isolation circuit of MIPI DSI PHY power supply

• To improve the performance of MIPI DSI TX0 and LVDS TX Combo PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

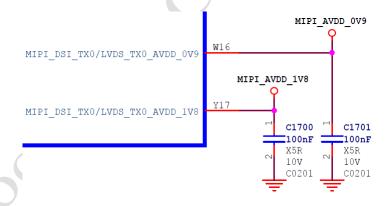


Figure 2-124 RK3568 MIPI DSI TX0/LVDS TX Combo PHY power decoupling capacitors

The matching design recommendations of MIPI DSI TX0 and LVDS TX Combo PHY interfaces are shown in the following Table.

#### Table 2-27 RK3568 MIPI DSI TX0 and LVDS TX Combo PHY interfaces design

Signal	Connection mode	Description
MIPI_DSI_TX0_D0P/LVDS_TX0_D0P MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	Connect directly Common mode inductor is reserved for EMI suppression	MIPI DSI data Lane0 output or LVDS data Lane0 output
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	Connect directly Common mode inductor is reserved for EMI suppression	MIPI DSI data Lane1 output or LVDS data Lane1 output
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	Connect directly Common mode inductor is reserved for EMI suppression	MIPI DSI data Lane2 output or LVDS data Lane2 output
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	Connect directly Common mode inductor is reserved for EMI suppression	MIPI DSI data Lane3 output or LVDS data Lane3 output
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	Connect directly Common mode inductor is reserved for EMI suppression	MIPI DSI clock output or LVDS clock output

#### 2.3.10.3 MIPI DSI TX1 interface

MIPI DSI TX1 PHY of RK3568 supports version MIPI V1.2 and has total 4Lane. The maximum output resolution of MIPI DSI TX1 is up to 1920X1080@60Hz;

MIPI DSI TX0+MIPI DSI TX1 can support Dual MIPI, and the maximum output resolution is up to 2048X1536@60Hz.

# MIPI DSI TX1

MIPI_DSI_TX1_D0P	AD18
MIPI_DSI_TX1_D0N	AE18
MIPI_DSI_TX1_D1P	AD17
MIPI_DSI_TX1_D1N	AC17
MIPI_DSI_TX1_D2P	AD14
MIPI_DSI_TX1_D2N	AC14
MIPI_DSI_TX1_D3P	AD12
MIPI_DSI_TX1_D3N	AE12
MIPI_DSI_TX1_CLKP	AD15
MIPI_DSI_TX1_CLKN	AE15

Figure 2-125 RK3568 MIPI DSI TX1 PHY pins

Please note the following items in MIPI DSI TX1 PHY design:

It's required to separate MIPI\_DSI\_TX1\_AVDD\_0V9, MIPI\_DSI\_TX1\_AVDD\_1V8 power pins and VDDA0V9\_IMAGE, VCCA1V8\_IMAGE by magnetic beads. Please refer to schematic design for details;

Figure 2-126 Magnetic bead isolation circuit of MIPI DSI TX1 PHY power supply

■ To improve the performance of MIPI DSI TX1 PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

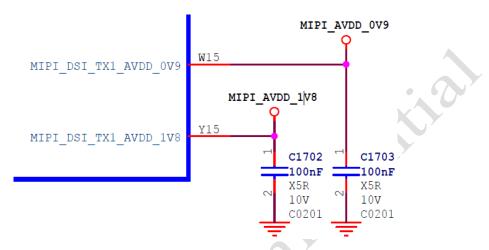


Figure 2-127 RK3568 MIPI DSI TX1 PHY power decoupling capacitors

The matching design recommendations of MIPI DSI TX1 PHY interfaces are shown in the following Table.

Signal	Connection mode	Note
	Connect directly	
MIPI_DSI_TX1_D0P/D0N	Common mode inductor is reserved for	MIPI DSI data Lane0 output
	EMI suppression	
	Connect directly	
MIPI_DSI_TX1_D1P/D1N	Common mode inductor is reserved for	MIPI DSI data Lane1 output
	EMI suppression	
	Connect directly	
MIPI DSI TX1 D2P/D2N	Common mode inductor is reserved for	MIPI DSI data Lane2 output
	EMI suppression	-
	Connect directly	
MIPI DSI TX1 D3P/D3N	Common mode inductor is reserved for	MIPI DSI data Lane3 output
	EMI suppression.	-
	Connect directly	
MIPI DSI TX1 CLKP/CLKN	Common mode inductor is reserved for	MIPI DSI clock output
	EMI suppression	-

Table 2–28 RK3568 MIPI DSI TX1 PHY interface design
---

# 2.3.10.4 eDP TX interface

The eDP TX PHY of RK3568 supports version eDP V1.3 and has total 4Lane. The maximum output resolution of eDP TX is up to 2560X1600@60Hz.

■ Each Lane rate can support to 1.62/2.7Gbps. *Copyright* © 2022 *Rockchip Electronics Co., Ltd.* 

- Support 1Lane or 2Lane or 4Lane mode.
- Support AUX channels with rate up to 1Mbps.

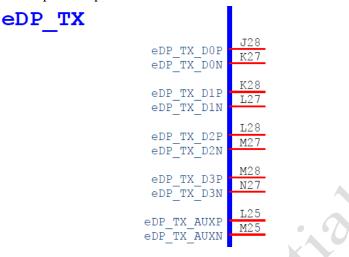


Figure 2-128 RK3568 eDP TX PHY pins

Please note the following items in eDP TX PHY design:

To improve the performance of eDP TX PHY, decoupling capacitors of each PHY power supplies cannot be deleted. Please place the capacitors near the pins when layout.

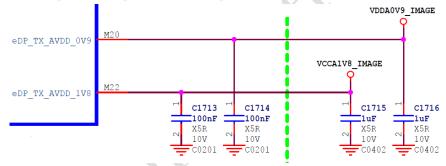


Figure 2-129 Figure 2-2 RK3568 eDP TX PHY power decoupling capacitors

 eDP\_TX\_D0P/DON, eDP\_TX\_D1P/D1N, eDP\_TX\_D2P/D2N and eDP\_TX\_D3P/D3N need to connect in series to 100nF AC coupling capacitor, and it's recommended to use 0201 package, if you use lower ESR and ESL, impedance changes on the line can be also reduced. The capacitor should be placed near RK3568 pins when layout.

			Diff 100 C	)hm ±10%			Dif	f 100 Ohm ±10%
- DD WV DOD	J28	EDP_TXD0P	C1704 1	2 100	<b>DnF</b> C0201	X5R 10V	5	->>EDP TX DOP
eDP_TX_DOP	K27	EDP_TXD0N	C1705 1	2 100	<b>)nF</b> C0201	X5R 10V		SEDP TX DON
eDP_TX_DON							5	WEDE IN DOM
- DD WW D1D	K28	EDP_TXD1P	C1706 1	2 100	<b>)nF</b> C0201	X5R 10V	5	->>EDP TX D1P
eDP_TX_D1P	L27	EDP_TXD1N	C1709 1	2 100	)nF C0201	X5R 10V		SEDP TX DIN
eDP_TX_D1N							1	
	L28	EDP_TXD2P	C1707 1	2 100	<b>nF</b> C0201	X5R 10V	5	->>EDP TX D2P
eDP_TX_D2P	M27	EDP TXD2N	C1708 1	2 100	)nF C0201	X5R 10V		SEDP TX D2N
eDP_TX_D2N								WEDP_IX_DZN
	M28	EDP TXD3P	C1710 1	2 100	<b>DnF</b> C0201	X5R 10V	5	
eDP_TX_D3P	N27	EDP TXD3N	C1711 1	2 100	)nF C0201	X5R 10V	1	EDP_TX_D3P
eDP_TX_D3N								->>EDP_TX_D3N
	L25			••			11	
eDP_TX_AUXP	M25						<b>-</b> //	EDP_TX_AUXP
eDP_TX_AUXN								Sedp_tx_auxn
			~ 🥒					

Figure 2-130 RK3568 eDP TX signal AC coupling capacitors

■ eDP\_TX\_AUXP/AUXN need to connect in series to the 100nF AC coupling capacitor near the interface

end. AUXP requires to reserve a 100K resistor grounded, and 100K resistor of AUXN is reserved and

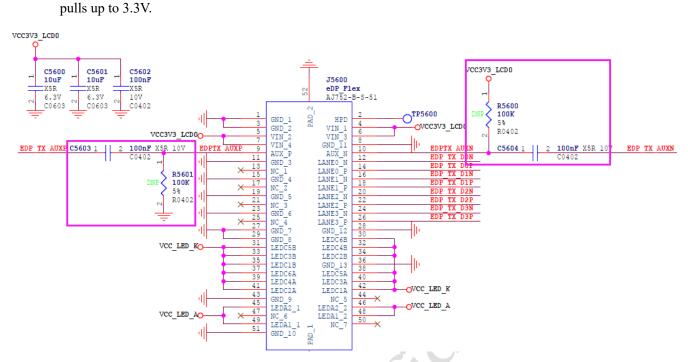


Figure 2-131 RK3568 eDP AUX signal AC coupling capacitors

The matching design recommendations of eDP TX PHY interface are shown in the following Table.

Signal	Connection mode	Description
eDP_TX_D0P/DON Connect in series with a 100nf capacitor (the 0201 package is recommended)		eDP data Lane0 output
eDP_TX_D1P/D1N Connect in series with a 100nf capacitor (the 0201 package is recommended)		eDP data Lane1 output
eDP_TX_D2P/D2N	Connect in series with a 100nf capacitor (the 0201 package is recommended)	eDP data Lane2 output
eDP_TX_D3P/D3N	Connect in series with a 100nf capacitor (the 0201 package is recommended)	eDP data Lane3 output
eDP_TX_AUXP/AUXN	Connect in series with a 100nf capacitor	eDP AUX channel

Table 2–29 KK3568 eDP TX PH Y Interface design	2-29 RK3568 eDP TX PHY inte	rface design
--	-----------------------------	--------------

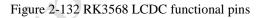
# 2.3.10.5 RGB TX interface

RK3568 supports parallel 24bit RGB output with maximum output resolution up to 1920X1080@60Hz; The parallel RGB interface supports the following formats:

	Table 2–30 RK3568	parallel RGB interface				
Interface	RGB888 format	RGB666 format	RGB565 format			
LCDC_CLK	LCDC_CLK	LCDC_CLK	LCDC_CLK			
LCDC_HSYNC	LCDC_HSYNC	LCDC_HSYNC	LCDC_HSYNC			
LCDC_VSYNC	LCDC_VSYNC	LCDC_VSYNC	LCDC_VSYNC			
LCDC_DEN	LCDC_DEN	LCDC_DEN	LCDC_DEN			
LCDC_D23	R7	R5	R4			
LCDC_D22	R6	R4	R3			
LCDC_D21	R5	R3	R2			
LCDC_D20	R4	R2	R1			
LCDC_D19	R3	R1	R0			
LCDC_D18	R2	R0	×			
LCDC_D17	R1	×	×			
LCDC_D16	R0	×	×			
LCDC_D15	G7	G5	G5			
LCDC_D14	G6	G4	G4			
LCDC_D13	G5	G3	G3			
LCDC_D12	G4	G2	G2			
LCDC_D11	G3	G1	G1			
LCDC_D10	G2	G0	G0			
LCDC_D9	G1	×	×			
LCDC_D8	G0	×	×			
LCDC_D7	В7	В5	B4			
LCDC_D6	B6	B4	В3			
LCDC_D5	В5	B3	B2			
LCDC_D4	B4	B2	B1			
LCDC_D3	В3	B1	B0			
LCDC_D2	B2	B0	×			
LCDC_D1	B1	×	×			
LCDC_D0	B0	×	×			

	/ VOP BT656 D0 M0	/ SPIO MISO M1	/ PCIE20 CLKREQn M1	/ 1281 MCLK M2 /	GPIO2 D0 d
CDC D1	/ VOP BT656 D1 M0	/ SPIO MOSI M1	/ PCIE20 WAKEn M1	/ 12S1 SCLK TX M2 /	GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPIO CSO M1	/ PCIE30X1 CLKREQn M1	/ 1281 LRCK TX M2 /	GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPIO CLK M1	/ PCIE30X1 WAKEn M1	/ 12s1 sdi0 m2 /	GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ 12S1 SDI1 M2 /	GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ 12S1 SDI2 M2 /	GPIO2 D5 d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1 ,	/ 12s1_sd13_M2 /	GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ 12S1 SDO0 M2 /	GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ 12S1 SDO1 M2 /	GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1 /	GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ 1283 MCLK M0	/ SDMMC2 D1 M1 /	GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ 1283 SCLK M0	/ SDMMC2 D2 M1 /	GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ 1283 LRCK M0	/ SDMMC2 D3 M1 /	GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1 /	GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ 1283 SDI M0	/ SDMMC2 CLK M1 /	GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1 /	GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLKO 25M M0		/ SDMMC2 PWREN M1 /	GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0 /	GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0 /	GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ 12C5 SCL M0	/ PDM SDIO M2 /	GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ 12C5 SDA M0	/ PDM SDI1 M2 /	GPI03 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ РWM10 M0 /	GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0 /	GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2 /	GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2 /	GPIO3 CO d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ 1281 SDO2 M2 /	GPI03 C1 d
LCDC VSYNC	/ VOP_BT1120_D14	/ SPI1 MISO M1	/ UART5_TX_M1	/ 12S1 SDO3 M2 /	GPI03 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ 1281 SCLK RX M2 /	GPIO3 C3 d
	(	/ GMAC1 MDC M0		/ PDM CLK1 M2 /	GPIO3 C4 d
PWM14 MO	/ VOP PWM M1 ) / SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ 1281 LRCK RX M2 /	GPIO3 C5 d

BGA636 19R00X19R00X1R20



Please note the following items in parallel RGB interface design:

- Parallel RGB I/O domain supplies power for VCCIO5. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripherals (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve parallel RGB interface performance, the decoupling capacitors of VCCIO5 power supply shouldn't be deleted. Please place them near the pin when layout.

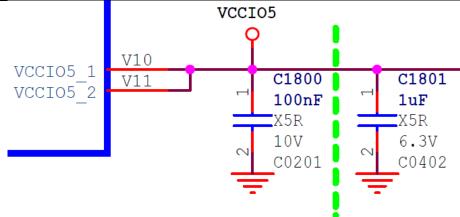


Figure 2-133 The decoupling capacitors of RK3568 VCCIO5 power supply

The pull up/down and matching design recommendations of parallel RGB interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
LCDC_D[23:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	LCDC data output
LCDC_HSYNC	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	LCDC row synchronous output
LCDC_VSYNC	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	LCDC field synchronous output
LCDC_DEN	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	LCDC data enabling output
LCDC_CLK	Pull-down	Connect a 220hm resistor in series near device end.	LCDC clock output

Table 2-31 RK3568 parallel RGB interface design

When board to board connection is realized through connectors, it is recommended to connect in series with resistors of certain value (between 220hm and 1000hm, as long as it can meet the SI test), as well as reserving TVS devices.

### 2.3.10.6 BT1120 TX interface

RK3568 supports 16bit BT1120 output interface with maximum output resolution up to 1920X1080@60Hz;

Corresponding relationship of BT1120 output interface data, and supports YC Swap.

Pin Name         Pixel #0         Pixel #1         Pixel #1           BT1120_D0         Y0[0]         Y1[0]         Cb0[0]         Cr0[0]           BT1120_D1         Y0[1]         Y1[1]         Cb0[1]         Cr0[1]           BT1120_D2         Y0[2]         Y1[2]         Cb0[2]         Cr0[2]           BT1120_D3         Y0[3]         Y1[3]         Cb0[3]         Cr0[3]           BT1120_D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[4]           BT1120_D5         Y0[5]         Y1[5]         Cb0[6]         Cr0[6]           BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[7]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120_D9         Cb0[0]         Cr0[0]         Y0[0]         Y1[0]           BT1120_D10         Cb0[2]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D11         Cb0[6]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D13         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D14         Cb0[6]         Cr0[6]	<b>D</b> '	NT	Delaul	t format	Swar	o open
BT1120_D1         Y0[1]         Y1[1]         Cb0[1]         Cr0[1]           BT1120_D2         Y0[2]         Y1[2]         Cb0[2]         Cr0[2]           BT1120_D3         Y0[3]         Y1[3]         Cb0[3]         Cr0[3]           BT1120_D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[4]           BT1120_D5         Y0[5]         Y1[5]         Cb0[6]         Cr0[6]           BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[6]           BT1120_D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[1]           BT1120_D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D11         Cb0[6]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D11         Cb0[6]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D13         Cb0[6]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[7]           BT1120_D13         Cb0[7]         Cr0[7	Pi	n Name	Pixel #0	Pixel #1		
BT1120 D1         Y0[1]         Y1[1]         Cb0[1]         Cr0[1]           BT1120 D2         Y0[2]         Y1[2]         Cb0[2]         Cr0[2]           BT1120 D3         Y0[3]         Y1[3]         Cb0[3]         Cr0[3]           BT1120 D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[4]           BT1120 D5         Y0[5]         Y1[5]         Cb0[6]         Cr0[6]           BT1120 D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120 D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120 D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[1]           BT1120 D1         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120 D1         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120 D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120 D11         Cb0[6]         Cr0[4]         Y0[4]         Y1[4]           BT1120 D13         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120 D13         Cb0[6]         Cr0[6]         Y0[7]         Y1[7]           D1         Cb0[6]         Cr0[7]	BT1	120 D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
BT1120_D2         Y0[2]         Y1[2]         Cb0[2]         Cr0[2]           BT1120_D3         Y0[3]         Y1[3]         Cb0[3]         Cr0[3]           BT1120_D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[3]           BT1120_D5         Y0[5]         Y1[5]         Cb0[6]         Cr0[4]           BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[7]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120_D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[0]           BT1120_D9         Cb0[1]         Cr0[1]         Y0[1]         Y1[1]           BT1120_D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D13         Cb0[7]         Cr0[3]         Y0[7]         Y1[7]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           ot         Cr0[6]         Y0[7]	BT1	120 D1				
BT1120_D3         Y0[3]         Y1[3]         Cb0[3]         Cr0[3]           BT1120_D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[4]           BT1120_D5         Y0[5]         Y1[5]         Cb0[6]         Cr0[5]           BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120_D8         Cb0[0]         Cr0[1]         Y0[1]         Y1[1]           BT1120_D9         Cb0[1]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D10         Cb0[2]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D11         Cb0[2]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D12         Cb0[4]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[7]           ot         CC105         Domain         Portion (Portion (Port	BT1	120 D2	L ]		E	Cr0[2]
BT1120         D4         Y0[4]         Y1[4]         Cb0[4]         Cr0[4]           BT1120         D5         Y0[5]         Y1[5]         Cb0[5]         Cr0[5]           BT1120         D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120         D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120         D8         Cb0[0]         Cr0[1]         Y0[0]         Y1[0]           BT1120         D9         Cb0[1]         Cr0[2]         Y0[2]         Y1[2]           BT1120         D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120         D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120         D13         Cb0[3]         Cr0[3]         Y0[3]         Y1[4]           BT1120         D13         Cb0[3]         Cr0[5]         Y0[6]         Y1[6]           BT1120         D14         Cb0[6]         Cr0[6]         Y0[7]         Y1[7]           ot         CC105         Domain         Pereting         Pereting         Pereting         Pereting         Pereting         Pereting         Pereting         Pereting         Pereting	BT1	120 D3	L 2	L J		L J
BT1120_D5         Y0[5]         Y1[5]         Cb0[5]         Cr0[5]           BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120_D8         Cb0[0]         Cr0[1]         Y0[7]         Y1[7]           BT1120_D9         Cb0[0]         Cr0[1]         Y0[1]         Y1[0]           BT1120_D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D11         Cb0[3]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[7]           ot         CCI05         Domain         Potesto         Y0[7]         Y1[7]           ot         CCI05         Domain         Potesto         Pot	BT1	120 D4	Y0[4]	Y1[4]	Cb0[4]	
BT1120_D6         Y0[6]         Y1[6]         Cb0[6]         Cr0[6]           BT1120_D7         Y0[7]         Y1[7]         Cb0[7]         Cr0[7]           BT1120_D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[0]           BT1120_D9         Cb0[1]         Cr0[1]         Y0[1]         Y1[1]           BT1120_D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D12         Cb0[4]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[6]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           ot         CC105         Domain         Portexton transport         Po	BT1	120 D5				
BT1120_D7         V0[7]         V1[7]         Cb0[7]         Cc0[7]           BT1120_D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[0]           BT1120_D9         Cb0[1]         Cr0[1]         Y0[1]         Y1[1]           BT1120_D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120_D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D12         Cb0[4]         Cr0[3]         Y0[3]         Y1[3]           BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           BT1120_D15         Cb0[6]         Cr0[7]         Y0[7]         Y1[7]           BT1120_D144         Cb0[6] <td< td=""><td></td><td>_</td><td></td><td></td><td></td><td></td></td<>		_				
BT1120         D8         Cb0[0]         Cr0[0]         Y0[0]         Y1[0]           BT1120         D9         Cb0[1]         Cr0[1]         Y0[1]         Y1[1]           BT1120         D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120         D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120         D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120         D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120         D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120         D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           BT1120         D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           ot         CCI05         Domain         Person         Person </td <td>BT1</td> <td> 120 D7</td> <td>L 2</td> <td></td> <td></td> <td></td>	BT1	 120 D7	L 2			
BT1120         D9         Cb0[1]         Cr0[1]         Y0[1]         Y1[1]           BT1120         D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120         D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120         D11         Cb0[3]         Cr0[4]         Y0[3]         Y1[3]           BT1120         D12         Cb0[4]         Cr0[4]         Y0[6]         Y1[5]           BT1120         D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120         D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120         D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           ot         CCI05         Domain         Perating         Voltage=1.8V/3.3V           pc         po         / vop Pr656 fb / voltage=1.8V/3.3V         Portei Name, nit         / 1281 McLe M2         / cercol po           pc         po         / vop Pr656 fb / voltage=1.8V/3.3V         Portei Name, nit         / 1281 McLe M2         / cercol po           pc         po         / vop Pr656 fb / voltage=1.8V/3.3V         Portei Name, nit         / 1281 McLe M2         / cercol po	BT1	120 D8				
BT1120         D10         Cb0[2]         Cr0[2]         Y0[2]         Y1[2]           BT1120         D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120         D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120         D13         Cb0[5]         Cr0[6]         Y0[6]         Y1[6]           BT1120         D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120         D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           or         CCI05         Domain         Perating         Y0[7]         Y1[7]           perating         Voltage=1.8V/3.3V         Perating         Y0[7]         Y1[7]         Y1[7]           perating         Voltage=1.8V/3.3V         Perating         Y0[7]         Y1[7]         Y1[7]           perating         Voltage=1.8V/3.3V         Perating         Y0[7]         Y1[7]         Y0[7]         Y1[7]           perating         Voltage=1.8V/3.3V         Perating         Y0[7]         Y1[7]         Y1[7]         Y1[7]           perating         Voltage=1.8V/3.3V         Perating         Y1[7]         Y1[7]         Y1[7]         Y1[7]			E 3			
BT1120         D11         Cb0[3]         Cr0[3]         Y0[3]         Y1[3]           BT1120         D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120         D13         Cb0[5]         Cr0[6]         Y0[5]         Y1[5]           BT1120         D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120         D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           or         CCI05         Domain         Perating         Voltage=1.8V/3.3V           Perating         Voltage=1.8V/3.3V         Perating         Voltage=1.8V/3.4V         Perating         Voltage=1.6V/7.9V         Perating         Voltage=1.6V/7.9V         Perating         Voltage=1.6V/7.9V         Perating         Voltage=1.6V/7.9V         Perating         Perating         Voltage=1.6V/7.9V         Perating         Perating<						
BT1120_D12         Cb0[4]         Cr0[4]         Y0[4]         Y1[4]           BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[6]         Y0[6]         Y1[7]           or         CC105         Domain         perating         Voltage=1.8V/3.3V           DCD0         / V0P B7656 D1 M0         / SP10 M160 M1         / PC1820 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DCD0         / V0P B7656 D1 M0         / SP10 M160 M1         / PC1820 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DCD0         / V0P B7656 D1 M0         / SP10 M160 M1         / PC1820 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DCD0         / V0P B7656 D1 M0         / SP10 CRE M1         / PC1820 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DCD0         / V0P B7656 D1 M0         / SP10 CRE M1         / PC1820 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DCD1         / V0P B7656 D1 M0         / SP12 CRE M1         / PO180 CLREBOD M1         / IS81 MCLE M2         / GP102 D1           DC15         / V0P B7656 D1 M0         / SP12 CRE M1 <t< td=""><td>BT1</td><td>120 D11</td><td></td><td>L 3</td><td></td><td></td></t<>	BT1	120 D11		L 3		
BT1120_D13         Cb0[5]         Cr0[5]         Y0[5]         Y1[5]           BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           or         CC105 Domain           perating Voltage=1.8V/3.3V           DCD0         / VOP_BT655_D1_M0         / SPI0_MISO_M1         / PC1E20_CLERED_M1         / T281_MCLE, M2 / GPI02_D1           DCD0         / VOP_BT655_D1_M0         / SPI0_MSD_M1         / PC1E20_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           DCD0         / VOP_BT655_D1_M0         / SPI0_MSD_M1         / PC1E30_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           DCD04         / VOP_BT655_D2_M0         / SPI0_CR6M_1         / PC1E30XI_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           DCD05         / VOP_BT655_D1         / SPI2_CR6M_1         / PC1E30XI_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           D2D54         / VOP_BT655_D1         / SPI2_CR6M_1         / F01230XI_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           D2D55         / VOP_BT655_D1         / SPI2_CR6M_1         / F01230XI_WAREE_M1         / T281_MCLE, M2 / GPI02_D2           D555         / VOP_BT655_D1         / SPI2_CR6M_1         / F01230XI_WAREE_M1         / T281_MCLE, M2 / GPI03_A0 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						
BT1120_D14         Cb0[6]         Cr0[6]         Y0[6]         Y1[6]           BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           or         CC105         Domain         perating         Voltage=1.8V/3.3V           DC 0         /vor press 0.000         / set0 M180 M1         / POIE20 CLEREON M1         / ISBI MCLE M2         / GPI02 D0           DC 0         /vor press 0.000         / set0 M180 M1         / POIE20 CLEREON M1         / ISBI MCLE M2         / GPI02 D1           DC 0         /vor press 0.000         / set0 M180 M1         / POIE20 CLEREON M1         / ISBI M2         / GPI02 D1           DC 0         /vor press 0.100         / set0 CLE M1         / POIE30X2 CLEREON M1         / ISBI M2         / GPI02 D1           DC 0         /vor press 0.100         / set0 CLE M1         / POIE30X2 CLEREON M1         / ISBI M2         / GPI02 D2           DC 04         /vor press 0.100         / set0 CLE M1         / POIE30X2 CLEREON M1         / ISBI M2         / GPI02 D2           DC 05         /vor press 0.100         / set12 M031 M1         / POIE30X2 CLEREON M1         / ISBI M2         / GPI02 D2           DC 05         /vor press 0.100         / set12 M031 M1         / POIE30X2 CLEREON M1         / ISBI M2         / GPI03 A0						
BT1120_D15         Cb0[7]         Cr0[7]         Y0[7]         Y1[7]           or         CCIO5 Domain         perating Voltage=1.8V/3.3V           DC p0         / V0P_B7656_D1M0         / BF10_M180_M1         / PC1E20_CLEREON_M1         / I381_MCLK_M2         / GF102_D0           DC p0         / V0P_B7656_D1M0         / BF10_M180_M1         / PC1E20_CLEREON_M1         / I381_MCLK_M2         / GF102_D0           DC p0         / V0P_B7656_D1M0         / BF10_M180_M1         / PC1E20_CLEREON_M1         / I381_MCLK_M2         / GF102_D0           DC p1         / V0P_B7656_D1M0         / BF10_CEN_M1         / PC1E20X1_CLEREON_M1         / I381_MCLK_M2         / GF102_D0           DC p4         / V0P_B7656_D1M0         / SF12_C80_M1         / PC1E30X2_CLEREON_M1         / I381_M012         / GF102_D1           DC p4         / V0P_B7656_D1M0         / SF12_C80_M1         / PC1E30X2_EREON_M1         / I381_M012         / GF102_D1           DC p5         / V0P_B7656_D1M0         / SF12_C80_M1         / UARKS_TX_M1         / I281_M012         / GF102_D1         / GF102_D1           DC p5         / V0P_B7656_G1M_0         / SF12_C80_M1         / UARKS_TX_M1         / I281_M012         / GF102_D1         / GF102_D1           DC D4         / V0P_B71120_D1         / SM42_CM1_M1         / UARKS_TX						-
OL         CCIO5 Domain           Departing Voltage=1.8V/3.3V           DC D0 / VOP_BT656_D1 M0 / SPI0_MISO_MI / PCIE20_CLEREON_MI / I281_BCLER M2 / OPI02_D0           DC D1 / VOP_BT656_D1 M0 / SPI0_MOST_MI / PCIE20_WAREN_MI / I281_BCLER M2 / OPI02_D1           DC D2 / VOP_BT656_D1 M0 / SPI0_CR0_MI / PCIE20_WAREN_MI / I281_BCLER M2 / OPI02_D1           DC D2 / VOP_BT656_D1 M0 / SPI0_CR0_MI / PCIE20_WAREN_MI / I281_BCLER M2 / OPI02_D1           DC D2 / VOP_BT656_D3 M0 / SPI0_CR0_MI / PCIE30XL_URAREN_MI / I281_BCLER M2 / OPI02_D2           DC D4 / VOP_BT656_D3 M0 / SPI2_CR0_MI / PCIE30XL_WAREN_MI / I281_BCLER M2 / OPI02_D1           DC D5 / VOP_BT656_D4 M0 / SPI2_CR0_MI / PCIE30XL_WAREN_MI / I281_BCLER / OPI02_D2           DC D5 / VOP_BT656_D5 M0 / SPI2_WAREN_MI / PCIE30XL_WAREN_MI / I281_BCLER / OPI02_D2           DC D5 / VOP_BT656_D5 M0 / SPI2_WAREN_MI / VARTE TX_MI / I281_BCLER / OPI02_D2           DC D5 / VOP_BT656_D5 M0 / SPI2_WAREN_MI / VARTE TX_MI / I281_BCLER / OPI02_D2           DC D5 / VOP_BT656_CLE M0 / SPI2_CLER MI / VARTE TX_MI / VARTE TX_MI / I281_BCLER / OPI02_D2           DC D5 / VOP_BT1120_D1 / SPI2_MISO_MI / PELSONI PERSTEN_MI / I281_BCLER / OPI03_A0           DC D5 / VOP_BT1120_D2 / GAACI_TXD5_M0 / I283_BCLE M0 / SUMMC2_D0 MI / GPI03_A1           DC D14 / VOP_BT1120_D1 / GAACI_RXD5_M0 / I283_BCLE M0 / SUMMC2_D1 MI / GPI03_A2           DC D15 / VOP_BT1120_D1 / GAACI_RXD5_M0 / I283_BCLE M0 / SUMMC2_D1 MI / GPI03_A3           DC D15 / VOP_BT1120_D1 / GAACI_RXD5_M0 / I283_BCLE M0 / SUMMC2_D1 MI / GPI03_A3						
DC D2 / VOP ET656 D2 M0 / SFID C80 M1 / PCIE30XI CLAREDN M1 / IC81 SDIO M2 / GFID2 D2 D5 D5 / VOP ET656 D4 M0 / SFID CLK M1 / PCIE30XI WAKEN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D4 M0 / SFIZ C80 M1 / PCIE30XI WAKEN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D5 M0 / SFIZ C80 M1 / PCIE30XZ CLKREDN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D5 M0 / SFIZ M30 M1 / PCIE30XZ PERSTN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D5 M0 / SFIZ M30 M1 / PCIE30XZ PERSTN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D5 M0 / SFIZ M30 M1 / PCIE30XZ PERSTN M1 / IC81 SDIO M2 / GFID2 D5 D5 / VOP ET656 D5 M0 / SFIZ M30 M1 / PCIE30XZ PERSTN M1 / IC81 SDIO M2 / GFID3 A0 / GFID3 A0 / GFID3 A0 / GFID3 A0 / GFID3 A1 / PCIE30XL PERSTN M1 / IC81 SDIO M2 / GFID3 A1 / GFID3 A1 / C0P ET1120 D1 / GAACI TXD2 M0 / IC83 MCLK M0 / SIMMC2 D0 M1 / GFID3 A1 / GFID3 A1 / C0P ET1120 D1 / GAACI TXD2 M0 / IC83 MCLK M0 / SIMMC2 D1 M1 / GFID3 A1 / GFID3 A2 / GFID3 A1 / C0P ET1120 D2 / GAACI TXD2 M0 / IC83 SCLK M0 / SIMMC2 D1 M1 / GFID3 A1 / GFID3 A1 / C0P ET1120 D4 / GAACI TXD2 M0 / IC83 SCLK M0 / SIMMC2 D3 M1 / GFID3 A2 / GFID3 A2 / GFID3 A1 / C0P ET1120 D5 / GAACI TXD2 M0 / IC83 SDIO M0 / SIMMC2 D3 M1 / GFID3 A2 / GFID3 A2 / GFID3 A1 / GFID3 A2 / GFID3 A2 / GFID3 A2 / GFID3 A1 / GFID3 A2 / GFID3 A1 / GFID3 A2 / GFID3 A1 / GFID3 A2 / GFID3 A2 / GFID3 A2 / GFID3 A1 / GFID3 A2 / GFID3 B2 / OP BT1120 D1 / GAACI TXDI M0 / UART4 TX M1 / F			=1.8V/3.3V			
DE D4         / VOP BT656 D4 M0         / SFI2 C61 M1         / PCTESOX2 CLRRED M1         / ICS1 SD11 M2         / GF102 D4           DC D5         / VOP BT656 D5 M0         SFI2 C63 M1         PCTESOX2 WARED M1         / ICS1 SD12 M2         / GF102 D5           DC D6         / VOP BT656 D5 M0         SFI2 M03T M1         PCTESOX2 FERSTM M1         / ICS1 SD12 M2         / GF102 D5           DC D6         / VOP BT656 C1K M0         SFI2 M130 M1         / UARTS TX M1         / ICS1 SD10 M2         / GF102 D7           DC CLK         / VOP BT656 CLK M0         / SFI2 CLK M1         / UARTS TX M1         / ICS1 SD10 M2         / GF103 A0           DC D8         / VOP BT120 D0         / SFI2 CLK M1         / UARTS TX M1         / ISS1 SD1 M2         / GF103 A1           DC D8         / VOP BT1120 D1         GMAC1 TXD2 M0         / IS33 MCLK M0         / SIMMC2 D1 M1         / GF103 A2           DC D10         / VOP BT1120 D2         / GMAC1 TXD2 M0         / IS33 BD1 M0         / SIMMC2 D3 M1         / GF103 A3           DC D11         / VOP BT1120 D5         / GMAC1 TXD2 M0         / IS33 BD1 M0         / SIMMC2 D3 M1         / GF103 A3           DC D12         / VOP BT1120 D5         / GMAC1 RXD2 M0         / IS33 BD1 M0         / SIMMC2 D3 M1         / GF103 A3           DC D13	peratin	IG Voltage= / VOP BI656 D0 M	0 / SPIO MISO M1	/ PCIE20 CL	RREQN_M1 / I2S1_MC	LK M2 / GPIO2 D0
DC DE         / VOP ET656 DE 400         / SFI2 MOST MI         / FCIE30X2 FERST. MI         / IZ81 SDI3 M2         / GPI02 DE           DC DF         / VOP ET656 DF 400         SFI2 MISO MI         / UARTS TX MI         / IZ81 SDI3 M2         / GPI02 DE           DC CLK         / VOP ET656 CLK M0         / SFI2 CLK MI         / UARTS TX MI         / IZ81 SDO1 M2         / GPI03 A0           DC CLK         / VOP ET120 DD         / SFI2 CLK MI         / UARTS TX MI         / IZ81 SDO1 M2         / GPI03 A0           DC D8         / VOP ET120 DD         / SFI2 CLK MI         / UARTS TX MI         / IZ83 MCLK M0         SDMMC2 DD MI         / GPI03 A1           DC D10         / VOP ET120 D2         / GMAC1 TXD3 M0         / IZ83 MCLK M0         SDMMC2 D2 MI         / GPI03 A1           DC D11         VOP ET1120 D3         / GMAC1 TXD3 M0         / IZ83 MCLK M0         SDMMC2 D3 MI         (GPI03 A1           DC D12         VOP ET1120 D4         / GMAC1 TXD3 M0         / IZ83 MD MO         / SDMMC2 D3 MI         (GPI03 A1           DC D14         VOP ET120 D5         / GMAC1 TXCLK M0         / IZ83 SDI M0         / SDMMC2 D14 MI         (GPI03 A1           DC D15         VOP ET120 D5         / GMAC1 TXCLK M0         / IZ83 SDI M0         / SDMMC2 CLK MI         (GPI03 A5           DC D15	peratin	IG Voltage= / VOP BT656 D0 M / VOP BT656 D1 M / VOP BT656 D2 M	0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0_CS0_M1	/ PCIE20 WA / PCIE30X1 (	KEn M1 / I2S1 SC CLKREQn M1 / I2S1 LF	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2
DC CLK         / VOP BT656 CLK M0         / SPI2 CLK M1         / UARTS FM M1         / I2S1 SD01 M2         / GPI03 A0           DC D8         / VOP BT1120 D0         / SPI1 CS0 M1         / PCIE30X1 PERSTR M1         / SIMMC2 D0 M1         / GPI03 A1           DC D9         VOP BT1120 D1         / GMAC1 TXD2 M0         / I2S3 MCLK M0         / SIMMC2 D1 M1         / GPI03 A3           DC D10         VOP BT1120 D2         / GMAC1 TXD3 M0         / I2S3 MCLK M0         / SIMMC2 D2 M1         / GPI03 A3           DC D11         VOP BT1120 D4         / GMAC1 TXD3 M0         / I2S3 SULK M0         / SIMMC2 D3 M1         / GPI03 A3           DC D12         VOP BT1120 D4         / GMAC1 TXD3 M0         / I2S3 SD0 M0         / SIMMC2 CMD M1         / GPI03 A5           DC D13         VOP BT1120 D4         / GMAC1 TXD1 M0         / I2S3 SD1 M0         / SIMMC2 CMF M1         / GPI03 A5           DC D14         VOP BT1120 D5         / GMAC1 TXD1 M0         / I2S3 SD1 M0         / SIMMC2 CMF M1         / GPI03 A5           DC D14         VOP BT1120 D7         / GMAC1 TXD1 M0         / UART4 FX M1         / PWM8 M0         GPI03 B1           DC D14         VOP BT1120 D7         / GMAC1 FXD1 M0         / UART4 FX M1         / PWM8 M0         / GPI03 B2           DC D15         VOP BT1120 D10 <td>peratin <u>DC D0 /</u> <u>DC D1 /</u> <u>DC D2 /</u> <u>DC D3 /</u> <u>DC D3 /</u></td> <td>ng Voltage= / vop br656 D0 M / vop br656 D1 M / vop br656 D2 M / vop br656 D3 M / vop br656 D3 M</td> <td>0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0 CSO M1 0 / SPI0 CLK M1 0 / SPI2 CS1 M1</td> <td>/ PCIE20 WA / PCIE30X1 / PCIE30X1 / PCIE30X1 / PCIE30X2</td> <td>KEN M1 / I2S1 SC CLKREQN M1 / I2S1 LF WAKEN M1 / I2S1 SI CLKREQN M1 / I2S1 SI</td> <td>LK TX M2 / GPI02 D1 CK TX M2 / GPI02 D2 I0 M2 / GPI02 D3 I1 M2 / GPI02 D4</td>	peratin <u>DC D0 /</u> <u>DC D1 /</u> <u>DC D2 /</u> <u>DC D3 /</u> <u>DC D3 /</u>	ng Voltage= / vop br656 D0 M / vop br656 D1 M / vop br656 D2 M / vop br656 D3 M / vop br656 D3 M	0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0 CSO M1 0 / SPI0 CLK M1 0 / SPI2 CS1 M1	/ PCIE20 WA / PCIE30X1 / PCIE30X1 / PCIE30X1 / PCIE30X2	KEN M1 / I2S1 SC CLKREQN M1 / I2S1 LF WAKEN M1 / I2S1 SI CLKREQN M1 / I2S1 SI	LK TX M2 / GPI02 D1 CK TX M2 / GPI02 D2 I0 M2 / GPI02 D3 I1 M2 / GPI02 D4
OC D9         VOP BTL100 D1         / GAACI TKU2 M0         / L233 BCLK M0         / SUMMC2 D1 M1         / GFT03 A2           OC D10         VOP BTL120 D2         (GAACI TKU2 M0         / L233 SUCK M0         / SUMMC2 D2 M1         (GFT03 A2           OC D11         VOP BTL120 D2         (GAACI TKU2 M0         / L233 SUCK M0         / SUMMC2 D2 M1         (GFT03 A2           OC D11         VOP BTL120 D3         (GAACI TKU2 M0         / L233 SUCK M0         / SUMMC2 D3 M1         (GFT03 A3           OC D13         VOP BTL120 D4         (GAACI TKU2 M0         / L233 SUC M0         / SUMMC2 D3 M1         (GFT03 A3           DC D15         VOP BTL120 D5         (GAACI TKULK M0         / L233 SDT M0         / SUMMC2 D1 M1         (GFT03 A1           DC D15         VOP BTL120 D5         (GAACI TKULK M0         / L335 SDT M0         / SUMMC2 D1 M1         (GFT03 A1           DC D15         VOP BTL120 D5         / GHACI TKUD M0         / L335 SDT M0         / SUMMC2 PWEN M1         (GFT03 B3           DC D15         VOP BTL120 D5         / GHACI TKUD M0         / UART4 TX M1         / PMM M0         (GFT03 B3           DC D15         VOP BTL120 D5         / GAACI TKUD M0         / L235 SDT M0         PTM SDT M2         (GFT03 B3           DC D10         VOP BTL120 D11         (GAAC	Deratin De D0 / De D1 / De D2 / De D3 / De D4 / De D5 / De D6 /	ng Voltage= / vop BT656 D0 M / vop BT656 D1 M / vop BT656 D2 M / vop BT656 D3 M / vop BT656 D4 M / vop BT656 D5 M / vop BT656 D5 M	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CS0 MI 0 / SPI0 CLK MI 0 / SPI2 CS1 MI 0 / SPI2 CS0 MI	/ PCIE20 WA / PCIE30X1 / PCIE30X1 / PCIE30X2 / PCIE30X2 / PCIE30X2	KEn M1 / 1281 SC CLKREQn M1 / 1281 LF WAKEn M1 / 1281 SI CLKREQn M1 / 1281 SI WAKEn M1 / 1281 SI	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2 10 M2 / GPIO2 D3 11 M2 / GPIO2 D3 12 M2 / GPIO2 D4
DC D9         VOP BT1120 D1         CBAR1 TXL2 M0         1283 MCLK M0         SUMMC2 D1 M1         CFT03 A2           DC D10         VOP BT1120 D2         C GARCI TXL2 M0         1283 SCLK M0         SIMMC2 D2 M1         CFT03 A2           DC D11         VOP BT1120 D2         C GARCI TXL2 M0         1283 SDCLK M0         SIMMC2 D2 M1         CFT03 A2           DC D11         VOP BT1120 D2         C GARCI TXD2 M0         1283 SDC M0         SIMMC2 D3 M1         CFT03 A3           DC D12         VOP BT1120 D4         C GMACI TXD2 M0         1283 SDC M0         SIMMC2 D3 M1         CFT03 A5           DC D15         VOP BT1120 D5         GRACI TXCLK M0         1293 SDT M0         SIMMC2 D1 M1         CFT03 A5           DC D15         VOP BT1120 D5         FIRI FEFCLKO 25M M0         SIMMC2 DFT M1         CFT03 A1           DC D15         VOP BT1120 D5         FIRI FEFCLKO 25M M0         SIMMC2 DFT M1         CFT03 B1           DC D15         VOP BT1120 D5         GRACI RXD1 M0         / UART4 RX M1         PMM M0         CFT03 B1           DC D15         VOP BT1120 D10         GARCI RXD1 M0         / UART4 RX M1         PMM M0         CFT03 B3           DC D15         VOP BT1120 D11         GARCI RXD1 M0         / IAC5 SCL M0         PIM SD1 M2         CFT03 B3	Deratin DC D0 // DC D1 // DC D2 // DC D3 // DC D4 // DC D5 // DC D5 // DC D5 // DC D5 //	Ig Voltage= / vop Br656 D0 M / vop Br656 D1 M / vop Br656 D2 M / vop Br656 D3 M / vop Br656 D4 M / vop Br656 D4 M / vop Br656 D5 M / vop Br656 D5 M	0 / SPI0 MISO MI 0 / SPI0 MOST MI 0 / SPI0 CSO MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSO MI 0 / SPI2 MOST MI 0 / SPI2 MISO MI	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX	KEn M1 / 1281 SC CLKREQn M1 / 1281 JE WAKEN M1 / 1281 SI CLKREQN M1 / 1281 SI WAKEN M1 / 1281 SI PERSTR M1 / 1281 SI M1 / 1281 SI	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2 10 M2 / GPIO2 D3 11 M2 / GPIO2 D4 12 M2 / GPIO2 D4 12 M2 / GPIO2 D5 13 M2 / GPIO2 D6 00 M2 / GPIO2 D7
DC D13 / VOP BT1120 D15 / GMAC1 TXCLK M0 / 123 8D1 M0 / SIMMAC2 CLK M1 / GPI03 A6 DC D14 / VOP BT1120 D5 / GMAC1 KXCLK M0 / SIMMAC2 DEF M1 / GPI03 B0 DC D15 / VOP BT1120 D5 / EFH1 PEFCIEO 25M M0 / JART4 FX M1 / PMM8 M0 / GPI03 B0 DC D16 / VOP BT1120 D7 / GMAC1 RXD1 M0 / JART4 FX M1 / PMM8 M0 / GPI03 B1 DC D17 / VOP BT1120 D8 / GMAC1 RXD1 M0 / JART4 FX M1 / PMM8 M0 / GPI03 B1 DC D17 / VOP BT1120 D9 / GMAC1 RXD1 M0 / JART4 FX M1 / PMM8 M0 / GPI03 B2 DC D18 / VOP BT1120 D9 / GMAC1 RXD1 M0 / JART4 FX M1 / PMM8 M0 / GPI03 B2 DC D19 / VOP BT1120 D9 / GMAC1 RXD1 M0 / J205 SDA M0 / PTM SD10 M2 / GPI03 B2 DC D21 / VOP BT1120 D10 / GMAC1 RXER M0 / I205 SDA M0 / PTM SD10 M2 / GPI03 B4 DC D20 / VOP BT1120 D11 / GMAC1 RXER M0 / J205 SDA M1 / PMM10 M0 / GPI03 B4 DC D20 / VOP BT1120 D11 / GMAC1 TXD0 M0 / J205 SDA M1 / PMM10 M0 / GPI03 B5 DC D21 / VOP BT1120 D12 / GMAC1 TXD1 M0 / J205 SDA M1 / PMM10 M0 / GPI03 B5 DC D22 / PMM12 M0 / GMAC1 TXEM M0 / UART3 FX M1 / PTM SD12 M2 / GPI03 B7 DC D23 / PMM12 M0 / GMAC1 CLKINOUT M0 / UART3 FX M1 / FTM SD12 M2 / GPI03 B7 DC SD23 / PMM12 M0 / GMAC1 CLKINOUT M0 / UART3 FX M1 / FTM SD12 M2 / GPI03 C1 DC M3YNC / VOP BT1120 D11 / SFI1 M051 M1 / PCH20 PERSTM 1 / I251 SD02 M2 / GPI03 C1 DC M3YNC / VOP BT1120 D13 / SFI1 M051 M1 / UART3 FX M1 / I251 SD02 M2 / GPI03 C1 DC M3YNC / VOP BT1120 D14 / SFI1 M30 M1 / UART3 FX M1 / I251 SD2 M2 / GPI03 C1 DC M3YNC / VOP BT1120 D15 / SFI1 GLK M1 / UART5 FX M1 / I251 SD2 M2 / GPI03 C3 M14 M0 / VOP FMM M1 / GMAC1 MDC M0 / UART7 TX M1 / I251 SCLF RK M2 / GPI03 C3	peratin DC D0 // DC D1 // DC D2 // DC D3 // DC D4 // DC D5 // DC D5 // DC D7 // DC D7 //	VOP BT556 D0 M VOP BT556 D1 M VOP BT556 D1 M VOP BT556 D1 M VOP BT556 D5 M VOP BT556 D5 M VOP BT556 D5 M VOP BT556 D6 M VOP BT556 D7 M VOP BT556 D7 M VOP BT556 D7 M	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 MISO MI 0 / SPI2 MISO MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX / UARTS TX / UARTS TX	KEn M1 / 1281 SC UKRECO M1 / 1281 IF WAKEN M1 / 1281 ST CLKRECO M1 / 1281 ST CLKRECO M1 / 1281 ST PERSTN M1 / 1281 ST M1 / 1281 ST M1 / 1281 ST	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2 IO M2 / GPIO2 D3 II M2 / GPIO2 D3 II M2 / GPIO2 D5 II M2 / GPIO2 D5 II M2 / GPIO2 D5 II M2 / GPIO2 D7 OO M2 / GPIO3 A0
DC D13         (VOP BT1120 CLK         (GMAC1 TXCLK M0         / I233 SDI M0         (SIMMAC2 CLK M1         GPIO3 A6           DC D14         (VOP BT1120 D5         (GMAC1 TXCLK M0         / SIMMAC2 DET M1         (GPIO3 A6           DC D15         (VOP BT1120 D5         (GMAC1 TXCLK M0         / SIMMAC2 DET M1         (GPIO3 A6           DC D15         (VOP BT1120 D5         (GMAC1 TXCLK M0         / SIMMAC2 DET M1         (GPIO3 B1           DC D16         (VOP BT1120 D7         (GMAC1 TXD1 M0         / UART4 FX M1         (PMM8 M0         (GPIO3 B1           DC D17         (VOP BT1120 D7         (GMAC1 TXD1 M0         / UART4 FX M1         (PMM9 M0         (GPIO3 B2           DC D18         (VOP BT1120 D7         (GMAC1 TXD1 M0         / UART4 TX M1         (PMM9 M0         (GPIO3 B2           DC D18         (VOP BT1120 D10         (GMAC1 TXD1 M0         / 1205 SDL M0         (PDM SD1 M2         (GPIO3 B2           DC D20         (VOP BT1120 D11         (GMAC1 TXD1 M0         / 1205 SDL M1         (PMM1 M0         (GPIO3 B5           DC D21         (VOP BT1120 D12         (GMAC1 TXD1 M0         / 1205 SDL M1         (PMM1 M0         (GPIO3 B5           DC D21         (VOP BT1120 D12         (GMAC1 TXD1 M0         / 1205 SDL M1         (PMM1 M0         (GPIO3 B5	Departin           DE D0         /           DE D1         /           DE D2         /           DE D3         /           DE D4         /           DE D5         /           DE D4         /           DE D5         /           DE D6         /           DE D7         /           DC D6         /           DC D6         /           DC D6         /           DC D6         /           DC D8         /           DC D9         /           D5 D10         /	VOP BT556 D0 M VOP BT556 D1 M VOP BT556 D1 M VOP BT556 D1 M VOP BT556 D5 M VOP BT556 D5 M VOP BT556 D5 M VOP BT556 D6 M VOP BT556 D7 M VOP BT556 D7 M VOP BT556 D7 M	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 MOSI MI 0 / SPI2 MOSI MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / SPI1 CSO MI 0 / GMACI TUDE M 0 / GMACI TUDE M	/ PCTE20 WA / PCTE30XI / PCTE30XI / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TXI / UARTS TXI	KEn M1 / 1281 SC UKRECO M1 / 1281 IF WAKEN M1 / 1281 ST CLKRECO M1 / 1281 ST CLKRECO M1 / 1281 ST PERSTN M1 / 1281 ST M1 / 1281 ST M1 / 1281 ST	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2 IO M2 / GPIO2 D3 II M2 / GPIO2 D3 II M2 / GPIO2 D5 II M2 / GPIO2 D5 II M2 / GPIO2 D5 II M2 / GPIO2 D7 OO M2 / GPIO3 A0
DC D15         VOP BT1120 D6         / ETH1 REFCLKO 25M M0         / SDMMC2 FWREN M1 / GFD3 B0           DC D16         VOP BT1120 D7         / GMAC1 RXD0 M0         / UART4 RX M1         / PWM6 M0         / GFD3 B1           DC D17         VOP BT1120 D5         / GMAC1 RXD0 M0         / UART4 RX M1         / PWM6 M0         / GFD3 B1           DC D17         VOP BT1120 D5         / GMAC1 RXD0 M0         / UART4 RX M1         / PWM9 M0         / GFD3 B2           DC D15         VOP BT1120 D5         / GMAC1 RXD0 RS M0         / I2C5 SCL M0         / PIM SD10 M2         / GFD3 B3           DC D15         VOP BT1120 D51         / GMAC1 RXD0 M0         / I2C5 SCL M0         / PIM SD11 M2         / GFD3 B3           DC D15         VOP BT1120 D51         / GMAC1 RXD0 M0         / I2C5 SCL M0         / PIM SD11 M2         / GFD3 B3           DC D21         VOP BT1120 D11         / GMAC1 RXD1 M0         / I2C5 SDA M1         / PWM11 RM 0         / GFD3 B5           DC D22         YMM12 M0         / GMAC1 RXD1 M0         / UART3 RX M1         / PWM11 RM 0         / GFD3 B7           DC D22         FMM12 M0         / GMAC1 RXD1 M0         / UART3 RX M1         / PIM SD1 M2         / GFD3 B7           DC D22         FWM13 M0         / GMAC1 RXD1 M0         / UART3 RX M1         / PIM	peratin <u>DC D0</u> // <u>DC D1</u> // <u>DC D3</u> // <u>DC D3</u> // <u>DC D5</u> // <u>DC D5</u> // <u>DC D6</u> // <u>DC D6</u> // <u>DC D6</u> // <u>DC D8</u> // <u>DC D8</u> // <u>DC D8 //</u> <u>DC D11 //</u> <u>DC D1 //</u> <u>DC D1 //</u> <u>DC D1 //</u> <u>DC D1 //</u> <u>DC D1 //</u>	VOP BT656 D0 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D3 M VOP BT656 D3 M VOP BT656 D4 M VOP BT656 D5 M VOP BT120 D0 VOP BT1120 D1 VOP BT1120 D1	0 / SPI0 MIBO M1 0 / SPI0 MOBI M1 0 / SPI0 CSN M1 0 / SPI2 CSN M1 0 / SPI2 CSN M1 0 / SPI2 CSN M1 0 / SPI2 MIBO M1 0 / SPI2 CLK M1 M0 / SPI2 CLK M1 / GMACI TXD2 M / GMACI TXD2 M / GMACI TXD2 M / GMACI TXD2 M	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS SX1 / DCTE30X1 0/ I233 SCIR 10/ I233 SCIR 10/ I233 SCIR 10/ I233 SCIR	KEn M1         / I2831 SC           CLKREGO, M1         IIS31 ST           WAKEN M1         IIS31 ST           WAKEN M1         IIS31 ST           PERSTN M1         IIS31 ST           M0         STMMC2	LK TX M2 / GPIO2 D1 CK TX M2 / GPIO2 D2 IO M2 / GPIO2 D3 II M2 / GPIO2 D3 II M2 / GPIO2 D5 II M2 / GPIO2 D5 II M2 / GPIO2 D5 O1 M2 / GPIO3 A0 D0 M1 / GPIO3 A0 D1 M1 / GPIO3 A3 D3 M1 / GPIO3 A5 D3 M1 / GPIO3 A5
DC D21 VOP BF1120 D12 / GRACI TXLI R0 / 1003 SLA RI / PMM11 R R0 / GP103 B6 DC D22 / PMM12 M0 / GRACI TXLEN M0 / UART3 TX M1 / PIM SD12 M2 (PIO3 B7 DC D23 / PMM13 M0 / GRACI MCLKINGUT M0 / UART3 RX M1 / PIM SD13 M2 / GP103 C1 DC HSYNC / VOP BT1120 D13 / SPI1 M0SI M1 / PC1E20 PERSTN M1 / I281 SD02 M2 / GP103 C1 DC VSYNC / VOP BT1120 D14 / SPI1 M1S0 M1 / UART5 TX M1 / I281 SD03 M2 / GP103 C2 DC DEN / VOP BT1120 D15 / SPI1 CLK M1 / UART5 RX M1 / I281 SCLK RX M2 / GP103 C3 M14 M0 / VOP FMM M1 / GRACI MDC M0 / UART7 TX M1 / PDM CLKI M2 / GP103 C4	peratin           Dc D0         /           Dc D1         /           Dc D2         /           Dc D3         /           Dc D4         /           Dc D5         /           Dc D5         /           Dc D5         /           Dc D5         /           Dc D6         /           Dc D7         /           DC D11         /           Dc D12         /           Dc D13         /	VOP BT656 D0 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D3 M VOP BT656 D3 M VOP BT656 D4 M VOP BT656 D4 M VOP BT656 D4 M VOP BT656 D5 M VOP BT120 D5 VOP BT120 D5	0 / SPI0 MISO M1 0 / SPI0 MOST M1 0 / SPI0 CSO M1 0 / SPI2 CSI M1 0 / SPI2 CSI M1 0 / SPI2 CSO M1 0 / SPI2 MOST M1 0 / SPI2 MOST M1 0 / SPI2 MOST M1 0 / SPI2 CLK M1 / GMAC1 TXD2 M / GMAC1 TXD2 M	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UART8 TX / UAR	KEn M1         / 1281 sc           CLKREQn M1         / 1281 sc           WAXEN M1         / 1281 sc           M0         / SDMMC2           M0         SDMMC2	LK TX M2 / GPI02 D1 CK TX M2 / GPI02 D2 IO M2 / GPI02 D2 II M2 / GPI02 D3 II M2 / GPI02 D5 IZ M2 / GPI02 D5 IZ M2 / GPI02 D5 O1 M2 / GPI03 A0 D0 M1 / GPI03 A0 D0 M1 / GPI03 A1 D1 M1 / GPI03 A3 D2 M1 / GPI03 A3 D3 M1 / GPI03 A3 CMD M1 / GPI03 A5 CMD M1 / GPI03 A5 C
DC D21 VOP BF1120 D12 / GRACI TXLI NO / 10C3 SIA NI / PINHI FK NO / GPIOS B6 DC D22 / PINHI 20 / GRACI TXLEN NO / UART3 TX MI / PINK SDIZ M2 / GPIOS B7 DC D23 / PINHI M0 / GRACI MCLKINOUT MO / UART3 FX MI / PINK SDIZ M2 / GPIO3 C0 DC HSYNC / VOP BT1120 D13 / SPII MOSI MI / PCIE20 PERSTE MI / I2SI SDO2 M2 / GPIO3 C1 DC VSYNC / VOP BT1120 D14 / SPII MISO MI / UART5 TX MI / I2SI SDO3 M2 / GPIO3 C2 DC DEN / VOP BT1120 D15 / SPII CLK MI / UART5 FX MI / I2SI SDO3 M2 / GPIO3 C3 MI4 M0 / VOP FWM MI / GRACI MDC M0 / UART7 TX MI / PINK CLKI M2 / GPIO3 C4	peratin           DC D0         /           DC D1         /           DC D2         /           DC D3         /           DC D5         /           DC D10         /           DC D12         /           DC D12         /           DC D12         /           DC D13         /           DC D14         /           DC D15         /	VOP BT656 D0 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D3 M VOP BT656 D3 M VOP BT656 D4 M VOP BT656 D4 M VOP BT656 D4 M VOP BT656 D5 M VOP BT120 D5 VOP BT120 D5	0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0 CSO M1 0 / SPI2 MOSI M1 0 / SPI2 MOSI M1 0 / SPI2 CLK M1 0 / SPI2 CLK M1 / GMACI TXD2 M / GMACI TXD3 M / GMACI TXD2 M / GMACI TXD3 M	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS SX / UAR	KEn M1 / I281 SC CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST M1 / I281 ST M0 / STMMC2 M0 / STMMC2 / STMMC2	LK TX M2 / GPI02 D1 CK TX M2 / GPI02 D2 IO M2 / GPI02 D2 II M2 / GPI02 D3 II M2 / GPI02 D5 IZ M2 / GPI02 D5 IZ M2 / GPI02 D5 O1 M2 / GPI03 A0 D0 M1 / GPI03 A0 D0 M1 / GPI03 A1 D1 M1 / GPI03 A3 D2 M1 / GPI03 A3 D3 M1 / GPI03 A3 CMD M1 / GPI03 A5 CMD M1 / GPI03 A5 C
DC D21 VOP BF1120 D12 / GRACI TXLI NO / 10C3 SIA NI / PINHI FK NO / GPIOS B6 DC D22 / PINHI 20 / GRACI TXLEN NO / UART3 TX MI / PINK SDIZ M2 / GPIOS B7 DC D23 / PINHI M0 / GRACI MCLKINOUT MO / UART3 FX MI / PINK SDIZ M2 / GPIO3 C0 DC HSYNC / VOP BT1120 D13 / SPII MOSI MI / PCIE20 PERSTE MI / I2SI SDO2 M2 / GPIO3 C1 DC VSYNC / VOP BT1120 D14 / SPII MISO MI / UART5 TX MI / I2SI SDO3 M2 / GPIO3 C2 DC DEN / VOP BT1120 D15 / SPII CLK MI / UART5 FX MI / I2SI SDO3 M2 / GPIO3 C3 MI4 M0 / VOP FWM MI / GRACI MDC M0 / UART7 TX MI / PINK CLKI M2 / GPIO3 C4	peratin           DC D1         /           DC D1         /           DC D2         /           DC D3         /           DC D5         /           DC D5         /           DC D5         /           DC D5         /           DC D6         /           DC D7         /           DC D8         /           DC D9         /           DC D10         /           DC D11         /           DC D12         /           DC D12         /           DC D12         /           DC D14         /           DC D14         /           DC D14         /	YOP BT656 D0 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D3 M VOP BT656 D3 M VOP BT656 D4 M VOP BT656 D5 M VOP BT656 D6 M VOP BT656 D5 M VOP BT656 D5 M VOP BT120 D1 VOP BT120 D1 VOP BT120 D2 VOP BT120 D5 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6	0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0 CSO M1 0 / SPI2 MOSI M1 0 / SPI2 MOSI M1 0 / SPI2 CLK M1 0 / SPI2 CLK M1 / GMACI TXD2 M / GMACI TXD3 M / GMACI TXD2 M / GMACI TXD3 M	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS SX / UAR	KEn M1 / I281 SC CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST M1 / I281 ST M0 / STMMC2 M0 / STMMC2 / STMMC2	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 C2 II M2 / GPIG2 D3 II M2 / GPIG2 D3 II M2 / GPIG2 D5 I3 M2 / GPIG2 D5 I3 M2 / GPIG2 D5 00 M2 / GPIG3 A0 D0 M1 / GPIG3 A0 D0 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D5 M1 / GPIG3 A3 D5 M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 A5
DC D21 VOP BF1120 D12 / GMAC1 TXLI B0 / 1003 SNA M1 / PMM11 FK M0 / GP103 B6 DC D22 / PMM12 M0 / GMAC1 TXLEM M0 / UART3 TX M1 / PDM SD13 M2 / GP103 B7 DC D23 / PMM13 M0 / GMAC1 MCLKINOUT M0 / UART3 FX M1 / PDM SD13 M2 / GP103 C0 DC HSYNC / VOP BT1120 D13 / SP11 M0SI M1 / PC1E20 PERSTA M1 / I281 SD02 M2 / GP103 C1 DC VSYNC / VOP BT1120 D14 / SP11 M1S0 M1 / UART5 TX M1 / I281 SD03 M2 / GP103 C2 DC DEN / VOP BT1120 D15 / SP11 CLK M1 / UART5 FX M1 / I281 SD03 M2 / GP103 C3 M14 M0 / VOP FMM M1 / GMAC1 MDC M0 / UART7 TX M1 / PIM CLK1 M2 / GP103 C4	peratin <u>DC D0</u> // DC D1 // DC D2 // DC D2 // DC D5 // DC D5 // DC D5 // DC D5 // DC D5 // DC D5 // DC D1 //	YOP BT656 D0 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D1 M VOP BT656 D3 M VOP BT656 D3 M VOP BT656 D4 M VOP BT656 D5 M VOP BT656 D6 M VOP BT656 D5 M VOP BT656 D5 M VOP BT120 D1 VOP BT120 D1 VOP BT120 D2 VOP BT120 D5 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6 VOP BT120 D6	0 / SPI0 MISO M1 0 / SPI0 MOSI M1 0 / SPI0 CSO M1 0 / SPI2 MOSI M1 0 / SPI2 MOSI M1 0 / SPI2 CLK M1 0 / SPI2 CLK M1 / GMACI TXD2 M / GMACI TXD3 M / GMACI TXD2 M / GMACI TXD3 M	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS TX / UARTS SX / UAR	KEn M1 / I281 SC CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST CUKREQn M1 / I281 ST M1 / I281 ST M0 / STMMC2 M0 / STMMC2 / STMMC2	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 D2 ID M2 / GPIG2 D3 II M2 / GPIG2 D3 II M2 / GPIG2 D3 II M2 / GPIG2 D5 I3 M2 / GPIG2 D5 I3 M2 / GPIG2 D7 N01 M2 / GPIG3 A0 D0 M1 / GPIG3 A1 D1 M1 / GPIG3 A3 D2 M1 / GPIG3 A3 D3 M1 / GPIG3 A4 CMD M1 / GPIG3 A5 DET M1 / GPIG3 B1 / GPIG3 B2
DC D23 / FWM13 M0 / GMAC1 MCLKINGUT M0 / UART3 RX M1 / FDM 5DI3 M2 / GFIG3 C0 DC HSYNC / VOP BT1120 D13 / SFI1 MOSI M1 / PCIE20 FERSTN M1 / I2S1 SDO2 M2 / GFIG3 C1 DC VSYNC / VOP BT1120 D14 / SFI1 MISO M1 / UART5 TX M1 / I2S1 SDO3 M2 / GFIG3 C2 DC DEN / VOP BT1120 D15 / SFI1 CLK M1 / UART5 RX M1 / I2S1 SOLK RX M2 / GFIG3 C3 M14 M0 / VOP FWM M1 / GMAC1 MDC M0 / UART7 TX M1 / FDM CLK1 M2 / GFIG3 C4	peratin <u>DC D0</u> / DC D1 / DC D2 / DC D2 / DC D3 / DC D3 / DC D5 / DC D5 / DC D5 / DC D7 / DC D7 / DC D7 / DC D1 / D	VOP BT656 D0 M           / VOP BT656 D1 M           VOP BT656 D1 M           / VOP BT656 D3 M           / VOP BT656 D3 M           / VOP BT656 D3 M           / VOP BT656 D4 M           / VOP BT656 D5 M           / VOP BT6120 D1           / VOP BT1120 D1           / VOP BT1120 D1           / VOP BT1120 D5	0 / SPI0 MISO MI 0 / SPI0 MOST MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CLK MI 0 / GMACI TKDS M 0 GMACI TKDS M 0 GMACI RKDS	/ PCTE20 WA / PCTE30X1 / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTE TX1 / UARTE TX1 / UARTE TX1 / UARTE RX1 / UARTE RX1 / UARTE X1 0 / I233 SDC NO / I233 SDC NO / I233 SDC NO / I233 SDC NO / UARTE RX1 NO / UARTE RX1 NO / UARTE RX1 NO / UARTE TX1 NO / UARTE TX1 // UARTE X1 // UARTE X	KEn M1         / I281 SC           CLKREGO M1         I281 SC           WAKEN M1         I281 SC           CLKREGO M1         I281 SC           WAKEN M1         I281 SC           WAKEN M1         I281 SC           WAKEN M1         I281 SC           WAKEN M1         I281 SC           WI         I281 SC           M1         I281 SC           M1         I281 SC           M0         SDMMC2           M1         FMMS MC           M0         SDMMC2           M1         FMMS MC           M1         FMMS MC           M0         FMMS MC           M1         FMMS MC	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 C2 ID M2 / GPIG2 D3 II M2 / GPIG2 D3 II M2 / GPIG2 D3 II M2 / GPIG2 D5 I3 M2 / GPIG2 D5 I3 M2 / GPIG2 D7 N01 M2 / GPIG3 A0 D0 M1 / GPIG3 A1 D1 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D3 M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 B3 / GPIG3 B2 / GPIG3 B3 0 M2 / GPIG3 B3 1 M2 / GPIG3 B5 / GPIG3 B3 0 M2 / GPIG3 B5 / GPIG3 B5 0 M2 / GPIG3 B5 / GPI
DC V9YNC / VOP BT1120 D14 / SP11 MISO M1 / UART5 TX M1 / I281 SD03 M2 / GPI03 C2 DC DEN / VOP BT1120 D15 / SP11 CLK M1 / UART5 RX M1 / I281 SCLK RX M2 / GPI03 C3 M14 M0 / VOP FWM M1 / GWAC1 MDC M0 / UART7 TX M1 / PIM CLK1 M2 / GPI03 C4	Deratin DC D0 // DC D1 // DC D2 // DC D2 // DC D5 // DC D10 // DC D12 // DC D12 // DC D14 // DC D15 // DC D14 // DC D15 // DC D14 // DC D15 // DC D14 // DC D15 // DC D15 // DC D15 // DC D15 // DC D17 // DC D16 // DC D16 // DC D19 // DC D19 // DC D16 // DC D19 // DC D16 // DC D19 // DC D19 // DC D19 // DC D19 // DC D16 // DC D19 // DC D16 // DC D19 // DC D19 //	Ig         Voltage=           / vop Br656 D0 M           / vop Br656 D1 M           / vop Br656 D1 M           / vop Br656 D2 M           / vop Br656 D2 M           / vop Br656 D3 M           / vop Br656 D4 M           / vop Br656 D5 M           / vop Br120 D1           / vop Br1120 D2           / vop Br1120 D3           / vop Br1120 D4           / vop Br1120 D5           / vop Br1120 D7	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 MOSI MI 0 / SPI2 MOSI MI 0 / SPI2 CLK MI 0	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS RX1 / UARTS RX1 / UARTS RX1 / UARTS RX1 / UARTS RX1 / T233 NCTE 00 / I233 NCTE 10 / UART4 RX1 10 / UART4 TX NO / UART4 TX NO / UART4 TX NO / I205 SCT 10 / I205 SCT 10 / I203 SCT 10	KEn MI         / I283 SC           CLKREGO, MI         / I281 SC           WAKEN MI         / I281 SC           WI         / I281 SC           WO         / SCMMC2           WO         / SCMMC2           WO         / SCMMC2           WO         SCMMC2           WI         / PMMS MG           WO         SCMMC2           WO         SCMMC2           WO         SCMMC2           WI         / PMMS MG           WO         FEW SC	LK TX M2 / GPI02 D1 CK TX M2 / GPI02 D2 IO M2 / GPI02 D2 II M2 / GPI02 D2 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI03 A0 D0 M1 / GPI03 A0 D0 M1 / GPI03 A2 D2 M1 / GPI03 A2 D2 M1 / GPI03 A2 D2 M1 / GPI03 A5 D2 M1 / GPI03 A5 DET M1 / GPI03 A5 DET M1 / GPI03 A5 I M2 / GPI03 B1 / GPI03 B1 / GPI03 B1 / GPI03 B1 / GPI03 B3 1 M2 / GPI03 B4 / GPI03 B5 / GPI03 B5
DC DEN / VOP BT1120 D15 / SF11 CLK M1 / UART5 FX M1 / I2S1 SCLK RX M2 / GF103 C3 M14 M0 / VOP FWM M1 / GWAC1 MDC M0 / UART7 TX M1 / FIM CLK1 M2 / GF103 C4	peratin pc p0 / / pc p1 / / pc p2 / / pc p3 / / pc p3 / / pc p5 / / pc p5 / / pc p6 / / pc p5 / / pc p6 / / pc p1 / /	Ig         Voltage=           / vop Br656 D0 M           / vop Br656 D1 M           / vop Br656 D1 M           / vop Br656 D2 M           / vop Br656 D2 M           / vop Br656 D3 M           / vop Br656 D4 M           / vop Br656 D5 M           / vop Br120 D1           / vop Br1120 D2           / vop Br1120 D3           / vop Br1120 D4           / vop Br1120 D5           / vop Br1120 D7	0 / SPI0 MISO MI 0 / SPI0 MOST MI 0 / SPI0 CSN MI 0 / SPI2 MOST MI 0 / SPI2 CSN MI 0 / SPI2 CLK MI M0 / SPI2 CLK MI / GMACI TKD3 M / GMACI TKD3 M / GMACI TKD3 M / GMACI TKD1 M / GMACI TKD0 M	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UAR	KEn MI         / I283 SC           CLKREGO, MI         / I281 SC           WAKEN MI         / I281 SC           WI         / I281 SC           WO         / SCMMC2           WO         / SCMMC2           WO         / SCMMC2           WO         SCMMC2           WI         / PMMS MG           WO         SCMMC2           WO         SCMMC2           WO         SCMMC2           WI         / PMMS MG           WO         FEW SC	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 D2 CK TX M2 / GPIG2 D2 TI M2 / GPIG2 D3 TI M2 / GPIG2 D5 T3 M2 / GPIG2 D5 T3 M2 / GPIG2 D5 T3 M2 / GPIG3 A0 D0 M1 / GPIG3 A1 D1 M1 / GPIG3 A1 D1 M1 / GPIG3 A3 D3 M1 / GPIG3 A3 D3 M1 / GPIG3 A5 CLK M1 / GPIG3 A5 CLK M1 / GPIG3 A5 CLK M1 / GPIG3 A5 CLK M1 / GPIG3 B5 CLK M1 / GPIG3 B5
M14 M0 / VOP FWM M1 / GMAC1 MDC M0 / UART7 TX M1 / FIM CLK1 M2 / GFIO3 C4	Deratin De D0 / DE D1 / DE D1 / DE D2 / DE D3 / DE D5 / DE D5 / DE D5 / DE D5 / DE D5 / DE D5 / DE D7 / DE D5 / DE D1 / DE D2	VOP BT656 D0 M           / VOP BT656 D1 M           VOP BT656 D1 M           VOP BT656 D3 M           VOP BT656 D3 M           VOP BT656 D4 M           VOP BT656 D5 M           VOP BT656 D5 M           VOP BT656 D7 M           VOP BT6120 D1           VOP BT1120 D1           VOP BT1120 D5           VOP BT1120 D1	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CM MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / SPI2 CLK MI 0 / GMACI TXD2 M 1 / GMACI TXD2 M 1 / GMACI TXD3 M 1 / GMACI TXD3 M 1 / GMACI TXD5 M 1 / GMACI TXD5 M 1 / GMACI TXD0 M 1 / GM	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTE FX / UAR	KEn M1         / I281 SC           CLKREGO M1         / I281 ST           WAKEN M1         / I281 ST           W1         / STMMC2           W0         / STMMC2           W0         / STMMC2           W1         / PWMS MC           W1         / PWMS MC           W1         / PWMS MC           W1         / PWMS MC           W1         / PWMS M11 T           W1         / PEN SDT	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 D2 CK TX M2 / GPIG2 D3 T1 M2 / GPIG2 D3 T1 M2 / GPIG2 D3 T1 M2 / GPIG2 D5 T3 M2 / GPIG2 D5 T3 M2 / GPIG2 D5 M2 / GPIG3 A6 D0 M1 / GPIG3 A0 D0 M1 / GPIG3 A3 D3 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 A5 DET M1 / GPIG3 B3 1 M2 / GPIG3 B3 1 M2 / GPIG3 B3 1 M2 / GPIG3 B5 C M2 / GPIG3 B5 1 M2 / GPIG3 B5 2 M2 / GPIG3 B5 R M0 / GPIG3
MI5 IR MO / SPDIF TX MI / GMAC1 MDIO MO / UART7 RX MI / I281 LRCK RX M2 / GPIO3 C5	peratin <u>pc p0</u> / pc p1 pc p2 pc p3 pc p3 pc p5 pc p4 pc p5 pc p5 pc p4 pc p5 pc p7 pc p6 pc p7 pc p1 pc	Ig         Voltage=           / vop Br656 D0 M           / vop Br656 D1 M           / vop Br656 D2 M           / vop Br656 D3 M           / vop Br656 D4 M           / vop Br656 D5 M           / vop Br656 D7 M           / vop Br656 C5 M           / vop Br656 C5 M           / vop Br656 C5 M           / vop Br120 D1           / vop Br1120 D2           / vop Br1120 D3           / vop Br1120 D4           / vop Br1120 D5           / vop Br1120 D5           / vop Br1120 D7           / vop Br1120 D14           / vop Br1120 D12           / vop Br1120 D14           / vop Br1120 D14           / vop Br1120 D14           / vop Br1120 D14	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CON MI 0 / SPI0 CSN MI 0 / SPI2 CSN MI 0 / SPI2 CSN MI 0 / SPI2 CSN MI 0 / SPI2 MOST MI 0 / SPI2 MOST MI 0 / SPI2 CLK MI 1 / GACI TXD3 M 1 / GACI TXD1 M 1 / SPI1 MOSI MI	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UAR	KEn MI         / I281 SC           CLKREGO, MI         / I281 ST           WAKEN, MI         / I281 ST           WI         / STMMC2           WO         STMMC2           WO         STMMC2           WI         STMMC2           WI         STMMC2           WI         FPMS MG           WI         FPMS ST           WI         FPMS ST </td <td>LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 D2 IO M2 / GPIG2 D2 II M2 / GPIG2 D3 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 O1 M2 / GPIG3 A0 D0 M1 / GPIG3 A2 D0 M1 / GPIG3 A2 D2 M1 / GPIG3 A5 D3 M1 / GPIG3 A5 D3 M1 / GPIG3 A5 CLK M1 / GPIG3 A5 CLK M1 / GPIG3 B1 / GPIG3 B2 / GPIG3 B1 / GPIG3 B1 / GPIG3 B3 / GPIG3 B1 / GPIG3 C1 / GPIG3 C1</td>	LK TX M2 / GPIG2 D1 CK TX M2 / GPIG2 D2 IO M2 / GPIG2 D2 II M2 / GPIG2 D3 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 O1 M2 / GPIG3 A0 D0 M1 / GPIG3 A2 D0 M1 / GPIG3 A2 D2 M1 / GPIG3 A5 D3 M1 / GPIG3 A5 D3 M1 / GPIG3 A5 CLK M1 / GPIG3 A5 CLK M1 / GPIG3 B1 / GPIG3 B2 / GPIG3 B1 / GPIG3 B1 / GPIG3 B3 / GPIG3 B1 / GPIG3 C1 / GPIG3 C1
	peratin <u>DC D0</u> // DC D1 // DC D2 // DC D3 // DC D5 // DC D5 // DC D5 // DC D6 // DC D6 // DC D10 // DC D10 // DC D10 // DC D11 // DC D11 // DC D12 // DC D13 // DC D15 //	VOP BT656 D0           / VOP BT656 D1           / VOP BT656 D1           VOP BT656 D3           / VOP BT656 D4           / VOP BT656 D5           / VOP BT656 D7           / VOP BT656 D7           / VOP BT656 D7           / VOP BT6120 D1           / VOP BT1120 D1           / VOP BT1120 D1           / VOP BT1120 D2           / VOP BT1120 D2           / VOP BT1120 D5           / VOP BT1120 D1	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 MOSI MI 0 / SPI2 CLK MI 0 / GMACI TKD2 M 1 / GMACI TKD1 M 1 / SPI1 MISO MI 1 / SPI1 CLK MI	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS TX / UARTS TX	KEn MI         / I281 SC           CLKREGO, MI         / I281 ST           WAKEN, MI         / I281 ST           WI         / I281 ST           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG	LK TX M2 / GPI02 D1 LK TX M2 / GPI02 D2 IO M2 / GPI02 D2 II M2 / GPI02 D2 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI03 D5 O1 M2 / GPI03 A0 D0 M1 / GPI03 A1 D1 M1 / GPI03 A1 D2 M1 / GPI03 A3 D3 M1 / GPI03 A5 CLK M1 / GPI03 A5 CLK M1 / GPI03 A5 CLK M1 / GPI03 A5 DET M1 / GPI03 A5 CLK M2 / GPI03 C1 M2 / GPI03 C1 M2 / GPI03 C1 M2 / GPI03 C1 M2 / GPI03 C1 LK RX M2 / GPI03 C1 LK RX M2 / GPI03 C1
	peratin           DC D0         /           DC D1         /           DC D1         /           DC D2         /           DC D3         /           DC D4         /           DC D5         /           DC D6         /           DC D6         /           DC D7         /           DC D6         /           DC D7         /           DC D8         /           DC D10         /           DC D11         /           DC D12         /           DC D12         /           DC D14         /           DC D14         /           DC D14         /           DC D15         /           D6 D16         /           D7         /           D6 D17         /           D6 D18         /           D6 D23         /           D6 D23         /           DC VSYNC         /           DC DEN         /	Ig         Voltage=           / vop Br556 D0 M           / vop Br556 D1 M           Vop Br556 D2 M           / vop Br556 D4 M           / vop Br556 D5 M           / vop Br556 D6 M           / vop Br556 D7 M           / vop Br5120 D1           / vop Br1120 D2           / vop Br1120 D2           / vop Br1120 D7           / vop Br1120 D1           / vop Br1120 D1<	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 MOSI MI 0 / SPI2 CLK MI 0 / GMACI TKD2 M 1 / GMACI TKD1 M 1 / SPI1 MISO MI 1 / SPI1 CLK MI	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS RX1 / UARTT RX1	KEn MI         / I281 SC           CLKREGO, MI         / I281 ST           WAKEN, MI         / I281 ST           WI         / I281 ST           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG	LK TX M2 / GPI02 D1 LK TX M2 / GPI02 D2 IO M2 / GPI02 D2 II M2 / GPI02 D2 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI02 D5 II M2 / GPI03 D5 O1 M2 / GPI03 A0 D0 M1 / GPI03 A1 D1 M1 / GPI03 A2 D2 M1 / GPI03 A3 D3 M1 / GPI03 A5 CLK M1 / GPI03 C1 / GPI03 B5 / GPI03 B1 / GPI03 C1 / GPI03 C1
VCCIO5 VCCIO5	Deratin De D0 / / DC D1 / / DC D2 / / DC D2 / / DC D5 / / DC D5 / / DC D5 / / DC D6 / / DC D6 / / DC D6 / / DC D1 / / / DC D1 / / / DC D1 / / / DC D1 / / / / DC D1 / / / / / / / / / / DC D2 / / / / / / / / / / / / / / / / / /	Ig         Voltage=           / vop Br556 D0 M           / vop Br556 D1 M           Vop Br556 D2 M           / vop Br556 D4 M           / vop Br556 D5 M           / vop Br556 D6 M           / vop Br556 D7 M           / vop Br5120 D1           / vop Br1120 D2           / vop Br1120 D2           / vop Br1120 D7           / vop Br1120 D1           / vop Br1120 D1<	0 / SPI0 MISO MI 0 / SPI0 MOSI MI 0 / SPI0 CSO MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 CSI MI 0 / SPI2 MOSI MI 0 / SPI2 CLK MI 0 / GMACI TKD2 M 1 / GMACI TKD1 M 1 / SPI1 MISO MI 1 / SPI1 CLK MI	/ PCTE20 WA / PCTE30X1 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / PCTE30X2 / UARTS RX1 / UARTT RX1	KEn MI         / I281 SC           CLKREGO, MI         / I281 ST           WAKEN, MI         / I281 ST           WI         / I281 ST           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG           WO         STMMC2           WI         PR08 MG	LK TX M2 / GPIG2 D1 LK TX M2 / GPIG2 D2 IG M2 / GPIG2 D3 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG2 D5 II M2 / GPIG3 D5 O1 M2 / GPIG3 A0 D0 M1 / GPIG3 A0 D0 M1 / GPIG3 A1 D1 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 D2 M1 / GPIG3 A5 CLK M1 / GPIG3 A5 DET M1 / GPIG3 A5 CLK M1 / GPIG3 B5 0 M2 / GPIG3 B5 0 M2 / GPIG3 B5 2 M2 / GPIG3 C5 I M2 / G



BGA636\_19R00X19R00X1R20

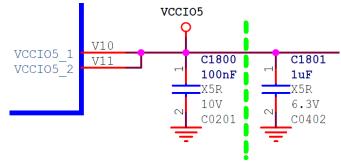
Figure 2-134 RK3568 VOP BT1120 functional pins

Please note the following items in BT1120 output interface design:

BT1120 output I/O domain supplies power for VCCIO5. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.

■ In order to improve BT1120 output interface performance, the decoupling capacitors of VCCIO5 power

supply should not be deleted. Please place them near the pin when layout.



The pull up/down and matching design recommendations of BT1120 output interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
VOP_BT1120_D[15:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	BT1120 data output
VOP_BT1120_CLK	Pull-down	Connect a 220hm resistor in series near device end.	BT1120 clock output

#### Table 2-33 RK3568 BT1120 output interface design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 220hm and 1000hm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.7 BT656 TX interface

RK3568 supports 8bit BT656 output interface and PAL and NTSC, VOP\_BT656 interface multiplexes to two power domains, \_M0 of VCCIO5 and \_M1 of VCCIO6. When selecting, the whole group \_M0 or the whole group M1 is selected, instead of mixing.

■ VOP BT656 multiplexes in the interface of VCCIO5 power domain.

LCDC D1 LCDC D2 LCDC D3 LCDC D4	/ VOP BT656 D1 M0	/ SPIO MISO M1	/ PCIE20 CLKREQn M1	/ 12S1 MCLK M2 /	GPIO2 D0 d
		7 SPIÖ MOSI M1	/ PCIE20 WAKEn M1	/ 12S1 SCLK TX M2 /	GPIO2 D1 d
LCDC D3 LCDC D4	/ VOP BT656 D2 M0	/ SPIO CSO M1	/ PCIE30X1 CLKREOn M1	/ 1251 LRCK TX M2 /	GPIO2 D2 d
LCDC D4	/ VOP BT656 D3 M0	/ SPIO CLK M1	/ PCIE30X1 WAKEn M1	/ 12S1 SDI0 M2 /	GPIO2 D3 d
	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ 12s1 sd11 M2 /	GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ 12S1 SD12 M2 /	GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ 12S1 SDI3 M2 /	GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ 12S1 SDO0 M2 /	GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2 /	GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1 /	GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ 1253 MCLK M0	/ SDMMC2 D1 M1 /	GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ 12S3 SCLK M0	/ SDMMC2 D2 M1 /	GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ 1253 LRCK M0	/ SDMMC2 D3 M1 /	GPIO3 A4 d
LCDC_D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ 1253 SDO M0	/ SDMMC2_CMD_M1 /	GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ 1253 SDI M0	/ SDMMC2 CLK M1 /	GPIO3 A6 d
LCDC_D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1 /	GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLKO 25M M	10	/ SDMMC2 PWREN M1 /	GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0 /	GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0 /	CDTO2 P2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2 /	CDT02 D2 -1
	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ 12C5 SDA M0	/ PDM SDI1 M2 /	CDTO2 R4 -1
LCDC D19			/ 12C3 SCL M1		CDIO2 DE J
		/ GMAC1 TXD0 M0		7 PWM10 M0 /	
LCDC D19 LCDC D20 LCDC D21	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ 12C3 SCL M1 / 12C3 SDA M1	/ PWM10 M0 /	CDIO2 R6 d
LCDC D20 LCDC D21	/ VOP BT1120 D11 / VOP BT1120 D12	/ GMAC1 TXD1 M0	/ 12C3 SDA M1	/ PWM11 IR M0 /	GPIO3 B6 d
	/ VOP BT1120 D11		/ I2C3 SDA M1 / UART3 TX M1		CDIO2 R6 d
LCDC D20 LCDC D21 LCDC D22 LCDC D23	/ VOP BT1120 D11 / VOP BT1120 D12 / PWM12 M0 / PWM13 M0	7 GMAC1 TXD1 M0 7 GMAC1 TXEN M0 7 GMAC1 MCLKINOUT M0	/ 12C3 SDA M1 / UART3 TX M1 / UART3 RX M1	/ PWM11 IR MO / / PDM SDI2 M2 / / PDM SDI3 M2 /	GPIO3 B6 d GPIO3 B7 d GPIO3 C0 d
LCDC D20 LCDC D21 LCDC D22 LCDC D23 LCDC HSYNC	/ VOP BT1120 D11 / VOP BT1120 D12 / FWM12 M0 / FWM13 M0 / VOP BT1120 D13	/ GMAC1 TXD1 M0 / GMAC1 TXEN M0 / GMAC1 MCLKINOUT M0 / SPI1 MOSI M1	/ I2C3 SDA MI / UART3 TX MI / UART3 RX MI / PCIE20 PERSTn M1	/ PWM11 IR M0 // / PDM SDI2 M2 // / PDM SDI3 M2 // / I2S1 SDO2 M2 /	GPI03 B6 d GPI03 B7 d GPI03 C0 d GPI03 C1 d
LEDE D20 LEDE D21 LEDE D22 LEDE D23 LEDE HSYNC LEDE VSYNC	/ VOP BT1120 D11 / VOP BT1120 D12 / FWM12 M0 / FWM13 M0 / VOP BT1120 D13 / VOP BT1120 D13	/ GMAC1 TXD1 M0 / GMAC1 TXEN M0 / GMAC1 MCLKINOUT M0 / SPI1 MOSI M1 / SPI1 MISO M1	/ 12C3 SDA MI / UART3 TX MI / UART3 RX MI / PCIE20 PERSTn M1 / UART5 TX MI	/ PMM11 IR M0 / PDM SDI2 M2 / / PDM SDI3 M2 / / I2S1 SD02 M2 / / I2S1 SD03 M2 /	GPI03 B6 d GPI03 B7 d GPI03 C0 d GPI03 C1 d GPI03 C2 d
LEDE D20 LEDE D21 LEDE D22 LEDE D23 LEDE HSYNC LEDE VSYNC	/ VOP BT1120 D11 / VOP BT1120 D12 / FWM12 M0 / FWM13 M0 / VOP BT1120 D13	/ GMAC1 TXD1 M0 / GMAC1 TXEN M0 / GMAC1 MCLKINOUT M0 / SPI1 MOSI M1	/ I2C3 SDA MI / UART3 TX MI / UART3 RX MI / PCIE20 PERSTn M1	/ PWM11 IR M0 // / PDM SDI2 M2 // / PDM SDI3 M2 // / I2S1 SDO2 M2 /	GPI03 B6 d GPI03 B7 d GPI03 C0 d GPI03 C1 d
LEDE D20 LEDE D21 LEDE D22 LEDE D23	/ VOP BT1120 D11 / VOP BT1120 D12 / PWM12 M0 / PWM13 M0 / VOP BT1120 D13 / VOP BT1120 D14 / VOP BT1120 D15 / VOP BT1120 D15	/ GMAC1 TXD1 M0 / GMAC1 TXEN M0 / GMAC1 MCLKINOUT M0 / SPI1 MOSI M1 / SPI1 MISO M1	/ 12C3 SDA MI / UART3 TX MI / UART3 RX MI / PCIE20 PERSTn M1 / UART5 TX MI	/ PMM11 IR M0 / PDM SDI2 M2 / / PDM SDI3 M2 / / I2S1 SD02 M2 / / I2S1 SD03 M2 /	GPI03 B6 d GPI03 B7 d GPI03 C0 d GPI03 C1 d GPI03 C2 d

BGA636\_19R00X19R00X1R20

2004



■ VOP BT656 multiplexes in the interface of VCCIO6 power domain.

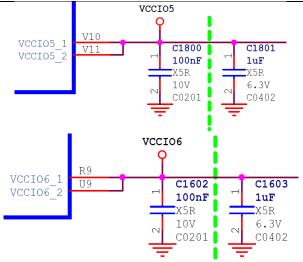
				(	
IF DO	/ EBC SDDO0	/ SDMMC2 D0 M0	/ 1281 MCLK M1	/ VOP BT656 D0 M1 /	GPIO3 C6 d
IF D1	/ EBC SDDO1	/ SDMMC2 D1 M0	/ 12S1 SCLK TX M1	/ VOP BT656 D1 M1 /	GPI03 C7 d
IF D2	/ EBC SDDO2	/ SDMMC2 D2 M0	/ I2S1 LRCK TX M1	/ VOP BT656 D2 M1 /	GPIO3 D0 d
IF D3	/ EBC SDDO3	/ SDMMC2 D3 M0	/ 12S1 SDO0 M1	/ VOP BT656 D3 M1 /	GPIO3 D1 d
IF D4	/ EBC SDD04	/ SDMMC2 CMD M0	/ 12S1 SDI0 M1	/ VOP BT656 D4 M1 /	GPIO3 D2 d
IF D5	/ EBC SDD05	/ SDMMC2 CLK M0	/ 12S1 SDI1 M1	/ VOP BT656 D5 M1 /	GPIO3 D3 d
IF D6	/ EBC SDDO6	/ SDMMC2 DET M0	/ 12S1 SD12 M1	/ VOP BT656 D6 M1 /	GPIO3 D4 d
IF D7	/ EBC SDD07	/ SDMMC2 PWREN M0	/ I2S1 SDI3 M1	/ VOP BT656 D7 M1 /	GPIO3 D5 d
IF D8	/ EBC SDDO8	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLK0 M1 /	GPIO3 D6 d
IF D9	/ EBC SDD00	/ GMAC1 TXD2 M1 / GMAC1 TXD3 M1	/ UART1 RX M1	/ PDM SDI0 M1 /	GPI03 D6 d GPI03 D7 d
IF D9 IF D10	/ EBC SDD09	/ GMAC1 TXD3 M1 / GMAC1 TXCLK M1	/ UARTI KA MI	/ PDM SDIO MI /	CD104 30 -1
IF D10	/ EBC SDD010	/ GMAC1 TACLA MI / GMAC1 RXD2 M1		/ PDM CDK1 M1 /	GPIO4 A0 d
IF D12	/ EBC SDD011 / EBC SDD012	/ GMAC1 RXD2 M1 / GMAC1 RXD3 M1	/ TTADE 7 EX M2	/ PDM SDI1 M1 /	GPIO4 A1 d
	/ EBC SDD012 / EBC SDD013	/ GMAC1 RXD3 M1 / GMAC1 RXCLK M1	/ UART7 TX M2 / UART7 RX M2	/ PDM SDI2 MI /	GPIO4 A2 d
IF D13	/ EBC SDD013 / EBC SDD014	*******			GPIO4 A3 d
IF D14 IF D15	/ EBC SDD014 / EBC SDD015	/ GMAC1 TXD0 M1 / GMAC1 TXD1 M1	/ UART9 TX M2 / UART9 RX M2	/ 1282 LRCK TX M1 / / 1282 LRCK RX M1 /	GPIO4 A4 d GPIO4 A5 d
AM CLKOUTO AM CLKOUTI	/ EBC SDCE1 / EBC SDCE2	/ GMAC1 RXD0 M1 / GMAC1 RXD1 M1	/ SPI3 CS1 M0 / SPI3 MISO M0	/ 1281 LRCK RX M1 / / 1281 SDO1 M1 /	GPIO4 A7 d GPIO4 B0 d
SP PRELIGHT TRIG	/ EBC SDCE3	/ GMAC1 RXDV CRS M1		/ 1231 SDO2 M1 /	GPI04 B1 d
2C4 SDA M0	/ EBC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI MO	/ I2S2 SDI M1 /	00704 00 1
2C4 SDA MO 2C4 SCL MO	/ EBC GDOE	/ ETH1 REFCLKO 25M M1			GPIO4 B2 d GPIO4 B3 d
204 BCL MU	/ LBC GDOL	/ ETHI REPUBRO 25M MI	/ SPIS CLK MU	/ 1282 SDO M1 /	GPIO4 BS d
2C2 SDA M1	/ EBC GDSP	/ CAN2 RX MO	/ ISP FLASH TRIGIN	/ VOP BT656 CLK M1	GPIO4 B4 d
2C2 SCL M1	/ EBC SDSHR	/ CAN2 TX M0		/ 1281 8D03 M1 /	GPIO4 B5 d
		1	1	1	
IF HREF	/ EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ 1282 MCLK M1 /	GPIO4 B6 d
IF VSYNC	/ EBC SDOE	/ GMAC1 MDIO M1		/ 1282 SCLK TX M1 /	GPIO4 B7 d
IF CLKOUT	/ EBC GDCLK		/ PWM11 IR M1		GPIO4 CO d
IF CLKIN	/ EBC SDCLK	/ GMAC1 MCLKINOUT M1	/ UART1 CTSn M1	/ 1282 SCLK RX M1 /	GPIO4 C1 d
					VCCIO6_1 -

BGA636\_19R00X19R00X1R20

### Figure 2-136 RK3568 VOP BT656 M1 functional pins

Please note the following items in BT656 output interface design:

- BT656 M0 output I/O domain supplies power for VCCIO5.In the actual design of products, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral(1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO5 power domain of the software is consistent with the power supply voltage of VCCIO5 power domain, otherwise the function will be abnormal and it may damage IO.
- BT656 M1 output I/O domain supplies power for VCCIO6. In the actual design of products, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve BT656 output interface performance, the decoupling capacitors of VCCIO5 or VCCIO6 power supply should not be deleted. Please place them near the pin when layout.



The pull up/down and matching design recommendations of BT656 output interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
VOP_BT656_D[7:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	BT656 data output
VOP_BT656_CLK	Pull-down	Connect a 220hm resistor in series near device end.	BT656 clock output

Table 2-34 RK3568 BT656 output interface design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

## 2.3.10.8 EBC TX interface

RK3568 has an EBC interface. EBC is a TCON module used to drive E-ink screen. It supports 8bit/16bit output and EBC interface multiplexes to VCCIO6 power domain.

U1000M

CIF         D1         / EI           CIF         D2         / EI           CIF         D3         / EI           CIF         D4         / EI           CIF         D5         / EI           CIF         D5         / EI           CIF         D6         / EI           CIF         D7         / EI	BC SDDO0 BC SDDO1 BC SDDO2 BC SDDO3 BC SDDO4 BC SDDO5 BC SDD06	/ SDMMC2 D0 M0 / SDMMC2 D1 M0 / SDMMC2 D2 M0 / SDMMC2 D3 M0 / SDMMC2 CMD M0 / SDMMC2 CLK M0	/ I281 MCLK M1 / I281 SCLK TX M1 / I281 LRCK TX M1 / I281 SD00 M1 / I281 SD10 M1	/ VOP BT656 D0 M1 / / VOP BT656 D1 M1 / / VOP BT656 D2 M1 / / VOP BT656 D3 M1 /	GPIO3 C6 d GPIO3 C7 d GPIO3 D0 d GPIO3 D1 d
LIF         D2         /         FL           CIF         D3         /         EI           CIF         D4         /         EI           CIF         D5         /         EI           CIF         D5         /         EI           CIF         D6         /         FI           CIF         D7         /         EI	BC SDDO2 BC SDDO3 BC SDDO4 BC SDDO5	/ SDMMC2 D2 M0 / SDMMC2 D3 M0 / SDMMC2 CMD M0	/ 1231 LRCK TX M1 / 1231 SD00 M1	/ VOP BT656 D2 M1 / / VOP BT656 D3 M1 /	GPIO3 D0 d
IF D3 / E1 IF P4 / E1 IF D5 / E1 IF D6 / E1 IF D7 / E1	BC SDDO3 BC SDDO4 BC SDDO5	/ SDMMC2 D3 M0 / SDMMC2 CMD M0	/ I2S1 SDO0 M1	/ VOP BT656 D3 M1 /	00703 01 1
IF D4 / E1 IF D5 / E1 IF D6 / E1 IF D7 / E1	BC SDDO4 BC SDDO5	/ SDMMC2 CMD M0			01100 01 0
IF D5 / E1 IF D6 / E1 IF D7 / E1	BC SDDO5			/ VOP BT656 D4 M1 /	CDT02 D2 -1
IF D6 / E1 IF D7 / E1	BC SDDOG	/ SUMMCZ CLR MU	/ 12S1 SDI1 M1	/ VOP BT656 D5 M1 /	CD102 D2 J
		/ SDMMC2 DET M0	/ I2S1 SDI2 M1	/ VOP BT656 D6 M1 /	GPI03 D3 d GPI03 D4 d
	BC SDD07	/ SDMMC2 PWREN M0	/ 12S1 SDI3 M1	/ VOP BT656 D7 M1 /	GPIO3 D5 d
IF D8 / EI	BC SDDO8	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLKO M1 /	GPIO3 D6 d
	BC SDDO9	/ GMAC1 TXD3 M1	/ UART1 RX M1	/ PDM SDIO M1 /	GPIO3 D7 d
	BC SDDO10	/ GMAC1 TXCLK M1		/ PDM CLK1 M1 /	GPIO4 A0 d
	BC SDD011	/ GMAC1 RXD2 M1		/ PDM SDI1 M1 /	GPIO4 A1 d
	BC SDD012	/ GMAC1 RXD3 M1	/ UART7 TX M2	/ PDM SDI2 M1 /	GPIO4 A2 d
IF D13 / EI	BC SDD013	/ GMAC1 RXCLK M1	/ UART7 RX M2	/ PDM SDI3 M1 /	GPIO4 A3 d
	BC SDD014	/ GMAC1 TXD0 M1	/ UART9 TX M2	/ 1282 LRCK TX M1 /	GPIO4 A4 d
IF D15 / EI	BC SDD015	/ GMAC1 TXD1 M1	/ UART9 RX M2	/ 1282 LRCK RX M1 /	GPIO4 A5 d
SP FLASHTRIGOUT / E	BC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CS0 M0	/ 1281 SCLK RX M1 /	
AM CLKOUTO / E	BC SDCE1	/ GMAC1 RXD0 M1	/ SPI3 CS1 M0	/ I2S1 LRCK RX M1 /	GPIO4 A7 d
	BC SDCE2	/ GMAC1 RXD1 M1	/ SPI3 MISO MO	/ I2S1 SD01 M1 /	GPIO4 A7 d
SP PRELIGHT TRIG / E	BC SDCE3	/ GMAC1 RXDV CRS M1		/ 12S1 SDO2 M1 /	GPIO4 B1 d
2C4 SDA M0 / EI	BC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI MO	/ I282 SDI M1 /	GPIO4 B2 d
2C4 SCL M0 / E	BC GDOE	/ ETH1 REFCLKO 25M M1	/ SPI3 CLK MO	/ 1282 SDO M1 /	GPIO4 B3 d
	BC GDSP	/ CAN2 RX M0	/ ISP FLASH TRIGIN	/ VOP BT656 CLK M1/	GPIO4 B4 d
2C2 SCL M1 / E	BC SDSHR	/ CAN2 TX M0		/ I2S1 SDO3 M1 /	GPIO4 B5 d
		1	(	(	
	BC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ 1282 MCLK M1 /	GPIO4 B6 d
IF VSYNC / E	BC SDOE	/ GMAC1 MDIO M1		/ 1282 SCLK TX M1 /	GPIO4 B7 d
IF CLKOUT / EI	BC GDCLK		/ PWM11 IR M1		GPIO4 C0 d
	BC SDCLK			/	

BGA636 19R00X19R00X1R20

Figure 2-137 RK3568 EBC functional pins

Please note the following items in EBC output interface design:

- EBC output interface domain supplies power for VCCIO6. In the actual product design, the corresponding power supply should be selected according to actual IO power supply requirements of peripheral (1.8V or 3.3V), and the power must be consistent with the requirements. Meanwhile, note that the drive voltage configuration of VCCIO6 power domain of the software is consistent with the power supply voltage of VCCIO6 power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve EBC output interface performance, the decoupling capacitors of VCCIO6 power supply should not be deleted. Please place it near the pin when layout.

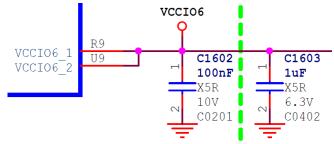


Figure 2-138 The decoupling capacitors of RK3568 VCCIO6 power supply Copyright © 2022 Rockchip Electronics Co., Ltd.

# RK3568 Hardware Design Guide

The pull up/down and matching design recommendations of EBC output interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)		
EBC_SDDO[15:0]	Pull-down	Direct connection	Source driver data output		
EBC_SDCE[3:0]	Pull-down	Direct connection	Source chip select/ Start pulse source driver		
EBC_VCOM	Pull-down	Direct connection	Com voltage control		
EBC_GDOE	Pull-down	Direct connection	Gate output enable		
EBC_GDSP	Pull-down	Direct connection	Gate start pulse		
EBC_SDSHR	Pull-down	Direct connection	Source driven shift register		
EBC_SDLE	Pull-down	Direct connection	Source data latch enable		
EBC_SDOE	Pull-down	Direct connection	Source data output enable		
EBC_GDCLK	Pull-down	Direct connection	Gate driver clock		
EBC_SDCLK	Pull-down	Direct connection	Source driver clock		

Table 2-35 RK3568 EBC output interface design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.10.9 Pay attention to the following items in LCD screen and touch screen design

- Please choose a resistor with 1% accuracy for FB end limiting resistor of LED backlight boost IC, and choose an appropriate package size according to power requirements.
- Please choose the GPIO pulled-down internal and connected to pull-down resistor external for EN/PWM pin of LED backlight boost IC, in order to avoid the flash screen when power on.
- Please choose a filter capacitor with appropriate rated voltage for the drive voltage output of LED backlight.
- Please choose an appropriate model according to working current for the schottky diode of LED backlight boost circuit, and pay attention to the reverse breakdown voltage of the diode, in order to avoid the reverse breakdown when there is no load.
- Please match the inductance, saturation current, DCR, etc. according to actual model for the inductance of LED backlight boost circuit.
- The signal level of screen and touch screen should match IO drive level of the chip, such as RST/ Stand by signal and so on.
- The power supply of screen must be controllable. It is not provided by default when power on.
- The decoupling capacitors of screen and touch screen shall not be deleted, but must be retained.
- I2C bus of TP must add 2.2K and pull up to VCC3V3\_TP power supply. It is recommended not to share the bus with other devices. If you must share the bus, pay attention to whether the pull-up power supply and the address conflict or not.

# **RK3568 Hardware Design Guide**

- For TP ICs with Charge pump, please note rated voltage of capacitors.
- For the screen, when it connects to the board by FPC, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.
- It is recommended to reserve common-mode inductance at the interface of serial interface screen.

#### 2.3.10.10 Please note the following items in VGA interface design

RK3568 itself doesn't support VGA OUT directly, it needs an external conversion chip, you can choose RGB888, HDMI, MIPI, eDP and other interfaces to change to VGA output. Here we mainly describe the related points of using RTD2166.

- The decoupling capacitors of each power supply pin shall not be deleted, and must be retained.
- Pay attention to the requirements of power on sequence.
- If there is a RESET signal in the conversion chip, then it must be controlled by RK3568 GPIO, and the level of RK3568 GPIO must match the IO level of conversion chip. The 100nF capacitor of RESET signal cannot be deleted. Place it near the pin of conversion chip to enhance anti ESD capability.
- RTD2166 Pin32 HPD, 100Kohm resistor grounded should not be deleted.
- RTD2166 peripheral circuit must refer to the reference design circuit directly.
- VGA\_HSYNC/VSYNC should support 5V level, and Pin17 must provide a 5V power supply.
- VGA\_R/G/B needs to pull down by a 750hm/1% resistor with 1% accuracy, which cannot be deleted.
- VGA R/G/B filter circuit needs to refer to the requirements of each conversion chip.
- All signals of VGA connector must be added TVS tubes, which should be placed as close as possible to the VGA connector.

### 2.3.11 Audio Interface Circuit

RK3568 has 4 I2S controllers,

- I2S0 controller:
  - Support 8 channels TX and 8 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - It is used by HDMI2.0TX PHY internally in the chip, and the part which isn't multiplexed to IO is used externally.
- I2S1 controller:
  - Support 8 channels TX and 8 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S, PCM and TDM modes.
  - ♦ I2S format supports normal, left-aligned and right-aligned formats.

×10

Set

- ♦
  - PCM format supports early, late1, late2, late3.
- TDM format supports normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift and right shift mode.
- I2S, PCM and TDM modes cannot be used at the same time.
- I2S2 controller:
  - Support 2 channels TX and 2 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S and PCM modes.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - PCM format supports early, late1, late2, late3.
  - I2S and PCM modes cannot be used at the same time.
- I2S3 controller:
  - Support 2 channels TX and 2 channels RX.
  - Bit rate is from 16bits to 32bits.
  - Maximum sampling rate is 192 kHz.
  - Support master or slave mode.
  - Support I2S and PCM modes.
  - I2S format supports normal, left-aligned and right-aligned formats.
  - PCM format supports early, late1, late2, late3.
  - I2S and PCM modes cannot be used at the same time.

RK3568 has 1 PDM controller.

- Support up to 8 channels.
- Bit rate is from 16bits to 24bits.
- Maximum sampling rate is 192 kHz.
- Support master receive mode.

RK3568 has 1 S/PDIF controller.

- Support two 16bit audio data which is saved in the location with 32-bit space.
- Support two phase format stereo audio data output.
- Support 16-bit to 31-bit audio data left-aligned or right-aligned in 32-bit sampled data buffers.
- Support 16-bit, 20-bit and 24-bit audio data transmission in linear PCM mode.
- Support nonlinear PCM transmission.

Connection diagram of I2S playback and record in Master and slave modes.

• RK3568 in Master mode:

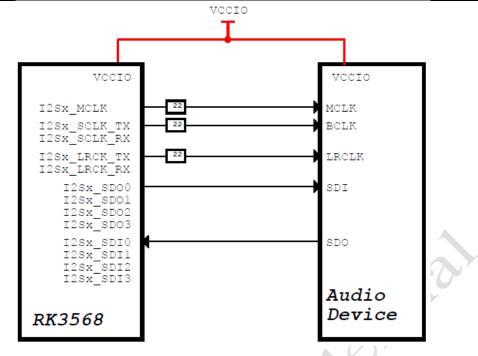


Figure 2-139 Connection diagram of RK3568 I2S in Master mode

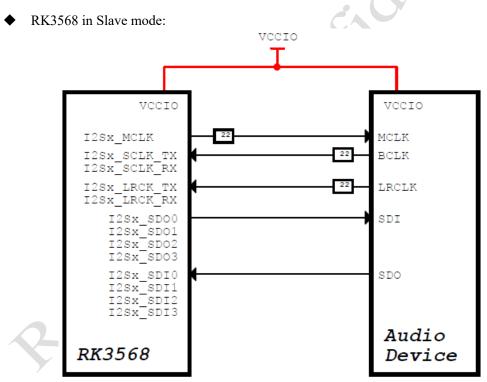


Figure 2-140 Connection diagram of RK3568 I2S in Slave mode

#### 2.3.11.1 I2S1 Interface

I2S1 interface contains independent 8-channel output and 8-channel input. In order to meet the requirements of asynchronous sampling rate of playback and record, two groups (SCLK\_TX\LRCK\_TX, SCLK\_RX\LRCK\_RX) of bit clock and frame clock are also provided correspondingly. Note that if SDOx and SDIx refer to only one group of bit/frame clock, SCLK\_TX\LRCK\_TX is preferred as their common clock.

I2S1 interface pins multiplex in three different power domains:

◆ I2S1\_M0 is multiplexed in the VCCIO1 power domain, the multiplexing relationship is optimized

according to the frequently used scene, in which three SD0x and SDIx signals are multiplexed

together and allocated according to the actual scene demand.

	SDA MO SCL MO		JART3 RX MO JART3 TX MO			/ CAN1 RX M / CAN1 TX M			/ AUDIOPWM LOU / AUDIOPWM LOU		C ADC DATA C ADC CLK		GPIO1 A0 u GPIO1 A1 u
251	MCLK M0	/ 1	JART3 RTSn MO	)		/ SCR CLK	/ PCIE30X	1 PERSTn M2				/	GPIO1 A2 d
251 251	SCLK TX MO		JART3 CTSn MO JART4 RX MÖ		DM CLK1 MO	/ SCR IO	/ PCIE30X	1 WAKEn M2	/ SPDIF TX MO	/ ACODE	C DAC CLK		GPIO1 A3 d GPIO1 A4 d
251 251	LRCK TX MO		JART4 RTSn MO JART4 TX MO	) / PI	DM CLKO MO	/ SCR RST	/ PCIE30X	1 CLKREQn M2	/ AUDIOPWM ROU	/ ACODEC	C DAC SYNC		GPIO1 A5 d GPIO1 A6 d
	SDO0 M0 SDO1 M0		JART4 CTSn MO	)	DM SDI3 MO	/ SCR DET	/ PCIE20	CLKREOn M2	/ AUDIOPWM ROU		C DAC DATAL C DAC DATAR		
251 251	SDO2 M0 SDO3 M0	71	2S1 SD12 M0 2S1 SD11 M0 2S1 SD10 M0	/ PI	DM SDI2 MO DM SDI1 MO DM SDI0 MO		/ PCIE20 / PCIE20	WAKEn M2 PERSTn M2		/ ACODE	C ADC SYNC	4	GPIO1 A7 d GPIO1 B0 d GPIO1 B1 d GPIO1 B2 d GPIO1 B3 d

Figure 2-141 RK3568 I2S1 M0 functional pins

 I2S1\_M1 is multiplexed in VCCIO6 power domain, and it can support the whole 8CH TX and 8CH RX.

EBC SDD00 EBC SDD01 EBC SDD02 EBC SDD03 EBC SDD04	/ SDMMC2 D0 M0 / SDMMC2 D1 M0 / SDMMC2 D2 M0	/ 1281 MCLK M1 / 1281 SCLK TX M1	/ VOP BT656 D0 M1 / / VOP BT656 D1 M1 /	
EBC SDDO2 EBC SDDO3		/ I2S1 SCLK TX M1	/ WOD DECEC D1 M1 /	
EBC SDDO3	/ SDMMC2 D2 M0			GPIO3 C7 d
		/ I2S1 LRCK TX M1	/ VOP BT656 D2 M1 /	GPIO3 D0 d
	/ SDMMC2 D3 M0	/ 1281 SDO0 M1	/ VOP BT656 D3 M1 /	GPIO3 D1 d
	/ SDMMC2 CMD M0	/ 1281 SDI0 M1	/ VOP BT656 D4 M1 /	GPIO3 D2 d
EBC SDD05	/ SDMMC2 CLK M0	/ 1281 SDI1 M1	/ VOP BT656 D5 M1 / / VOP BT656 D6 M1 /	GPIO3 D3 d
EBC SDD06 EBC SDD07	/ SDMMC2 DET M0 / SDMMC2 PWREN M0	/ 1281 SD12 M1 / 1281 SD13 M1	/ VOP BT656 D6 M1 / / VOP BT656 D7 M1 /	GPIO3 D4 d GPIO3 D5 d
EBC SDD07	7 SDMMCZ PWREN MO	/ 1251 5D15 M1	/ VOP B1636 D/ M1 /	GPIO3 D5 a
EBC SDDO8	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM_CLK0_M1 /	GPIO3 D6 d
				GPI03 D7 d
EBC SDD010	/ GMAC1 TXCLK M1			GPIO4 A0 d
EBC SDD011	/ GMAC1 RXD2 M1		/ PDM SDI1 M1 /	GPIO4 A1 d
EBC SDD012	/ GMAC1 RXD3 M1	/ UART7 TX M2	/ PDM SDI2 M1 /	GPIO4 A2 d
EBC SDD013	/ GMAC1 RXCLK M1	/ UART7 RX M2	/ PDM SDI3 M1 /	GPIO4 A3 d
EBC SDD014	/ GMAC1 TXD0 M1	/ UART9 TX M2	/ 1282 LRCK TX M1 /	GPIO4 A4 d
EBC SDD015	/ GMAC1 TXD1 M1	/ UART9 RX M2	/ 1232 LRCK RX M1 /	GPIO4 A5 d
EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CSO MO	/ 1281 SCLK RX M1 /	GPIO4 A6 d
EBC SDCE1	/ GMAC1 RXD0 M1	/ SPI3 CS1 M0	/ I2S1 LRCK RX M1 /	GPIO4 A7 d
EBC SDCE2	/ GMAC1 RXD1 M1	/ SPI3 MISO MO	/ I2S1 SD01 M1 /	GPIO4 B0 d
EBC SDCE3	/ GMAC1 RXDV CRS M1		/ 1251 SDO2 M1 /	GPIO4 B1 d
PRC MOOM	CMACL DVED MI	/ SDT2 MOST MO	( T292 SDT M1 /	CDT04 D2 J
				GPIO4 B2 d GPIO4 B3 d
BBC GDOE	/ EINI AECENCO ZOM MI	/ SFIS CBR MO	/ 1262 600 MI	01101 b5 d
EBC GDSP	/ CAN2 RX M0	/ ISP FLASH TRIGIN	/ VOP BT656 CLK M1/	GPIO4 B4 d
EBC SDSHR	/ CAN2 TX M0		/ I2S1 SDO3 M1 /	GPIO4 B5 d
EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ 1282 MCLK M1 /	GPIO4 B6 d
EBC SDOE	/ GMAC1 MDIO M1		/ 1282 SCLK ТХ М1 /	GPIO4 B7 d
EBC GDCLK		/ PWM11 IR M1		GPIO4 C0 d
EBC SDCLK	/ GMAC1 MCLKINOUT M1	/ UART1 CTSn M1	/ / 1282 sclk rx m1 /	GPIO4 C1 d
	ERC SDD011 ERC SDD012 ERC SDD013 ERC SDD014 ERC SDD014 ERC SDCE1 ERC SDCE1 ERC SDCE2 ERC SDCE2 ERC SDCE3 ERC GDC5 ERC GDC5 ERC GDC5 ERC SDLE ERC SDLE ERC SDLE ERC SDLE ERC SDLE	EEC SDDO9 / GNACI TXD3 M1 EEC SDD01 / GNACI TXD3 M1 EEC SDD011 / GNACI TXDK M1 EEC SDD012 / GNACI TXD2 M1 EEC SDD012 / GNACI FXD3 M1 EEC SDD013 / GNACI FXD3 M1 EEC SDD015 / GNACI TXD0 M1 EEC SDD015 / GNACI TXD0 M1 EEC SDC00 / GNACI TXD1 M1 EEC SDC00 / GNACI TXD1 M1 EEC SDC02 / GNACI FXD0 M1 EEC SDC02 / GNACI FXD0 M1 EEC SDC02 / GNACI FXD0 M1 EEC SDC02 / GNACI FXD1 M1 EEC SDC03 / GNACI FXD0 CRS M1 EEC SDC04 / GNACI FXD0 CRS M1 EEC GD05 / ETH1 FEFCLKO 25M M1 EEC SDC04 / GNACI FXD0 CRS M1 EEC SDC05 / GNACI FXD0 M1	EEC SDDO9 / GMACI TXD3 M1 / UART1 RX M1 EEC SDD010 / GMACI TXCKK M1 EEC SDD011 / GMACI TXCKK M1 EEC SDD011 / GMACI RXD2 M1 EEC SDD012 / GMACI RXD3 M1 / UART7 TX M2 EEC SDD013 / GMACI RXD3 M1 / UART7 RX M2 EEC SDD014 / GMACI TXDD M1 / UART9 TX M2 EEC SDD015 / GMACI TXD1 M1 / UART9 TX M2 EEC SDC01 / GMACI TXD1 M1 / UART9 RX M2 EEC SDC01 / GMACI TXD1 M1 / SFI3 CS1 M0 EEC SDC02 / GMACI RXD0 M1 / SFI3 CS1 M0 EEC SDC02 / GMACI RXD1 M1 / SFI3 CS1 M0 EEC SDC02 / GMACI RXDV CRS M1 EEC SDC03 / GMACI RXDV CRS M1 EEC GD05 / ETH1 REFCIKO 25M M1 / SFI3 CLK M0 EEC GD05 / ETH1 REFCIKO 25M M1 / SFI3 CLK M0 EEC SDC93 / GMACI RXDV CRS M1 / SFI3 CLK M0 EEC SDC9 / GMACI RXDV CR	ERC 3DD09         / GMAC1 TXD3 M1         / UART1 RX M1         / PIM 5DI0 M1           ERC 3DD010         (GMAC1 TXCLK M1         / PDM 5D11 M1         / PDM 5D11 M1           ERC 3DD011         (GMAC1 TXCLK M1         / PDM 5D11 M1         / PDM 5D11 M1           ERC 3DD012         (GMAC1 RXD2 M1         / UART7 TX M2         / PDM 5D12 M1           ERC 3DD013         (GMAC1 RXD3 M1         / UART7 TX M2         / PDM 5D13 M1           ERC 3DD014         (GMAC1 RXD3 M1         / UART7 RX M2         / PDM 5D13 M1           ERC 3DD015         (GMAC1 TXD0 M1         / UART9 RX M2         / I282 LRCK RX M1           ERC 3DD015         (GMAC1 TXD1 M1         / UART9 RX M2         / I282 LRCK RX M1           ERC 3DCE0         (GMAC1 TXEN M1         / SPI3 CS1 M0         / I281 SCLK RX M1           ERC 3DCE1         (GMAC1 RXD0 M1         / SPI3 CS1 M0         / I281 SD01 M1           ERC 3DCE2         (GMAC1 RXD1 M1         / SPI3 MISO M0         / I281 SD01 M1           ERC SDCE3         (GMAC1 RXDV CRS M1         / I281 SD02 M1         /           ERC GD0E         (ETH1 REFCLKO 25M M1 / SFI3 CLK M0         / I282 SDI M1         /           ERC GD0E         (ETH1 REFCLKO 25M M1 / SFI3 CLK M0         / I282 SDO M1         /           ERC GD0E         (ETH1

BGA636\_19R00X19R00X1R20

Figure 2-142 RK3568 I2S1 M1 functional pins

 I2S1\_M2 is multiplexed in VCCIO5 power domain, and it can support the whole 8CH TX and 8CH RX.

CDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	I2S1 MCLK M2	GPIO2 D0 d
CDC D1	7 VOP BT656 D1 M0	7 SPIO MOSI M1	/ PCIE20 WAKEn M1	I2S1 SCLK TX M2 /	CDTO2 D1 J
CDC D2	/ VOP BT656 D2 M0	/ SPIO CSO M1	/ PCIE30X1 CLKREOn M1	I2S1 LRCK TX M2 /	GPIO2 DI d GPIO2 D2 d
CDC D3	/ VOP BT656 D3 M0	/ SPIO CLK M1	/ PCIE30X1 WAKEn M1	/ 12S1 SDI0 M2 /	GPIO2 D3 d
CDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ 12S1 SDI1 M2 /	GPIO2 D4 d
CDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ 12S1 SDI2 M2 /	GPIO2 D5 d
CDC D6	/ VOP BT656 D6 M0	/ spi2 Mosi M1	/ PCIE30X2 PERSTn M1	/ 12S1 SDI3 M2 /	GPIO2 D6 d
CDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ 1251 SDO0 M2 /	GPIO2 D7 d
CDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ 12S1 SDO1 M2 /	GPIO3 A0 d
2DC D0	( WOD DE1120 DC	( CDT1 CC0 M1	/ DOTE2081 DEDCE: M1	/ cpan/c2 p0 x/1	( CDT02 31 1
CDC D8	/ VOP BT1120 D0	/ SPI1 CSO M1	/ PCIE30X1 PERSTn M1 , / I2S3 MCLK M0	/ SDMMC2 D0 M1 /	GPIO3 A1 d
CDC D9 CDC D10	/ VOP BT1120 D1 / VOP BT1120 D2	/ GMAC1 TXD2 M0 / GMAC1 TXD3 M0	/ 1253 MCLK M0 / 1253 SCLK M0	/ SDMMC2 D1 M1 / / SDMMC2 D2 M1 /	GPIO3 A2 d GPIO3 A3 d
CDC D10	/ VOP BT1120 D2	/ GMAC1 RXD2 M0	/ 1253 SCLK M0	/ SDMMC2 D2 M1 /	CDTO2 A4 d
CDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0 / GMAC1 RXD3 M0	/ 1253 BRCK M0	/ SDMMC2 CMD M1 /	CDTO2 35 d
CDC D13	/ VOP BT1120 CLK	7 GMAC1 TXCLK M0	/ 1253 SDI M0	SDMMC2 CLK M1 /	CPTO3 A6 d
CDC D14	7 VOP BT1120 D5	7 GMAC1 RXCLK M0	7 1200 001 110	/ SDMMC2 DET M1 /	CDTO2 37 d
CDC D15	/ VOP BT1120 D6	/ ETH1 REFCLKO 25M M0		/ SDMMC2 PWREN M1 /	GPIO3 B0 d
CDC D16 CDC D17	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0 /	GPIO3 B1 d
CDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ РWM9 M0 /	GPIO3 B2 d
CDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDIO M2 /	GPIO3 B3 d
CDC D19 CDC D20	/ VOP BT1120 D10 / VOP BT1120 D11	/ GMAC1 RXER M0 / GMAC1 TXD0 M0	/ 12C5 SDA M0 / 12C3 SCL M1	/ PDM SDI1 M2 / / PWM10 M0 /	GPIO3 B4 d GPIO3 B5 d
CDC D20	7 VOP BT1120 D11 7 VOP BT1120 D12	/ GMAC1 TXD0 M0 / GMAC1 TXD1 M0	/ 12C3 SDA M1	/ PWM10 M0 /	
CDC D21	/ PWM12 M0	/ GMAC1 TXD1 M0 / GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2 /	GPIO3 B6 d GPIO3 B7 d
CDC D22	7 PWM12 M0 7 PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UARTS IX MI	/ PDM SD12 M2 /	GPIO3 C0 d
					01100 00 0
CDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ 12S1 SDO2 M2	GPI03 C1 d
CDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ 12S1 SDO3 M2	GPIO3 C2 d
CDC DEN	/ VOP BT1120 D15	7 SPI1 CLK M1	/ UART5 RX M1	/ 12S1 SCLK RX M2	GPIO3 C3 d
WM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2 /	GPIO3 C4 d
	/ SPDIF TX M1	/ GMAC1 MDIO MU	/ UART / RX M1	1251 LRCK RX M2	GPIO3 C5 d
	/ SPDIF TX M1	7 GMAC1 MDIO M0	/ UART7 RX M1	I2S1 LRCK RX M2	GPIO3 C5 d

BGA636\_19R00X19R00X1R20

Figure 2-143 RK3568 I2S1 M2 functional pins

In I2S1 interface design, please note:

- I2S1\_M0, I2S1\_M1 and I2S1\_M2 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 or M2 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve I2S1 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S1 interface are shown in the following Table.

Table 2–36 RK3568 I2S1 interface design					
Signal	Pull up/down inside	Connection mode	Description (chip end)		
I2S1_MCLK	Pull-down	Connect a 220hm resistor in series	I2S system clock output		
I2S1_SCLK_TX	Pull-down	Connect a 220hm resistor in series	I2S continuous SCLK (TX, related AudioPlay)		
I2S1_LRCK_TX	Pull-down	Connect a 220hm resistor in series	I2S frame clock for channel selection (TX, related AudioPlay)		
I2S1_SDO[3:0]	Pull-down	Direct connection	I2S serial data		
I2S1_SCLK_RX	Pull-down	Connect a 220hm resistor in series	I2S continuous SCLK (RX, related AudioRecord)		
I2S1_LRCK_RX	Pull-down	Connect a 220hm resistor in series	I2S frame clock for channel selection (RX, related AudioRecord)		
I2S1_SDI[3:0]	Pull-down	Direct connection	I2S serial data		

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

### 2.3.11.2 I2S2 interface

I2S2 interface contains independent 2-channel output and 2-channel input. In order to meet the requirements of asynchronous sampling rate of playback and record, two groups (SCLK\_TX\LRCK\_TX, SCLK\_RX\LRCK\_RX) of bit clock and frame clock are also provided correspondingly. Note that if SDOx and SDIx refer to only one group of bit/frame clock, SCLK\_TX\LRCK\_TX is preferred as their common clock.

I2S2 interface pins multiplex in two different power domains:

• I2S2\_M0 is multiplexed in the VCCIO4 power domain.

SDMMC1 D0	/ GMAC0 RXD2	/ UART6 RX MO		/ GPIO2 A3 1	
SDMMC1 D1	/ GMAC0 RXD3	/ UART6 TX MO		/ GPIO2 A4 1	и в2
SDMMC1_D2	/ GMAC0 RXCLK	/ UART7 RX M0		/ GPIO2 A5 1	u C2
SDMMC1_D3	/ GMAC0 TXD2	/ UART7 TX MO		/ GPIO2 A6 1	u
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9 RX MO		/ GPIO2 A7	u C2
SDMMC1 CLK	/ GMAC0 TXCLK	/ UART9 TX M0		/ GPIO2 B0	d D2
SDMMC1 PWREN	/ I2C4 SDA M1	/ UART8 RTSn M0	/ CAN2 RX M1	/ GPIO2 B1	d D2
SDMMC1 DET	/ 12C4 SCL M1	/ UART8 CTSn M0	/ CAN2 TX M1	/ GPI02 B1	
	CM3 C0				F2
	GMAC0 TXD0 GMAC0 TXD1	/ UART1 RX M0 / UART1 TX M0		GPIO2 B3	GZ
	GMACO TXEN	/ UART1 RTSn M0	/ SPI1 CLK M0	/ GPIO2 B4 1 / GPIO2 B5 1	GZ
	GMAC0_RXD0	/ UART1_CTSn_M0	/ SPI1_MISO_MO	/ GPI02 B5	
12S2 SCLK RX M0	/ GMAC0 RXD1	/ UART6 RTSn M0	/ SPI1 MOSI M0	/ 00100 07	H2
1252 SCLK RX MO	/ GMACO RXDV CRS	/ UART6 CTSn M0	/ SPI1 CS0 M0	/ GPIO2 B7	- F24
1252 MCLK MO	/ ETHO REFCLKO 25M	/ UART7 RTSn M0	/ SPI1_CS0_M0	/ GPI02 C0 (	- ( <u>-</u> /.
	/	/	/	· · · · · · · · · · · · · · · · · · ·	F2
1282 SCLK TX M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0	/ SPI2 MISO M0	/ GPIO2 C2 (	
12S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0	/ SPI2 MOSI MO	/ GPIO2 C3 (	
I2S2_SDO_M0	/ GMACO MDIO	/ UART9_CTSn_M0 / UART8_TX_M0	/ SPI2_CS0_M0	/ GPIO2 C4	F21
1252_SDI_M0	/ GMACO_RXER	/ UART8_TX_MU	/ SPI2_CS1_M0	/ GPIO2 C5	
CLK32K_OUT1		/ UART8 RX MO	/ SPI1_CS1_M0	/ GPIO2 C6	d E2
CLK32K_OUT1		/ UART8 RX M0	/ SPI1_CS1_M0	/ GPIO2 C6	

E' 0.144 DW2560 1202 MO

Figure 2-144 RK3568 I2S2 M0 functional pins

• I2S2\_M1 is multiplexed in the VCCIO6 power domain.

EBC_SDD01         / SDMMC2 D1 M0         / I281 SCLK TX M1         / VOP BT556 D1 M1         / GPI03 C1 d           / EBC_SDD02         / SDMMC2 D2 M0         / I281 LECK TX M1         / VOP BT556 D2 M1         / GPI03 D0 d           / EBC_SDD03         / SDMMC2 D2 M0         / I281 LECK TX M1         / VOP BT556 D2 M1         / GPI03 D0 d           / EBC_SDD03         / SDMMC2 CMD M0         / I281 SDI0 M1         / VOP BT556 D3 M1         / GPI03 D1 d           / EBC_SDD05         / SDMMC2 CMD M0         / I281 SDI0 M1         / VOP BT556 D5 M1         / GPI03 D3 d           / EBC_SDD05         / SDMMC2 CLK M0         / I281 SDI1 M1         / VOP BT556 D5 M1         / GPI03 D3 d           / EBC_SDD05         / SDMMC2 DT M0         / I281 SDI3 M1         / VOP BT556 D5 M1         / GPI03 D5 d           / EBC_SDD05         / SDMMC2 DT M0         / I281 SDI3 M1         / VOP BT556 D7 M1         / GPI03 D5 d           / EBC_SDD05         / GMAC1 TXD2 M1         / UART1 TX M1         / PDM CLK0 M1         / GPI03 D6 d           / EBC_SDD010         / GMAC1 TXD3 M1         / UART1 TX M1         / PDM CLK0 M1         / GPI04 A1 d           / EBC_SDD011         / GMAC1 FXD3 M1         / UART7 TX M2         PDM CLK1 M1         / GPI04 A1 d           / EBC_SDD013         / GMAC1 FXD3 M1         / UART7 TX M2	CIF D0	/ EBC SDDO0	/ SDMMC2 D0 M0	/ 1281 MCLK M1	/ VOP BT656 D0 M1 /	GPIO3 C6 d
	CIF D1					
<pre>/ ERC SDD03 / SPMMC2 D3 M0 / L231 SD00 M1 / VOP BT656 D3 M1 / GFL03 D1 d</pre>	CIF D2					
ZERC_SDB04       / SDB052       CMD_N0       / I281_SDI0_M1       / YOP_BT556_D5_M1 / GPI03_D2_G         / ERC_SDD05       / SDM022_CLK_M0       / I281_SDI1_M1       / YOP_BT556_D5_M1 / GPI03_D4_G         / ERC_SDD05       / SDM022_CLK_M0       / I281_SDI3_M1       / YOP_BT556_D5_M1 / GPI03_D4_G         / ERC_SDD05       / SDM022_PWREN_M0       / I281_SDI3_M1       / YOP_BT556_D7_M1 / GPI03_D5_G         / ERC_SDD05       / GMAC1_TXD2_M1       / UART1_TX_M1       / PDM_CLE0_M1       / GPI03_D6_G         / ERC_SDD05       / GMAC1_TXD3_M1       / UART1_TX_M1       / PDM_CLE0_M1       / GPI03_D6_G         / ERC_SDD010       / GMAC1_TXD3_M1       / UART1_TX_M1       / PDM_CLE0_M1       / GPI04_D0_G         / ERC_SDD011       / GMAC1_TXD3_M1       / UART7_TX_M2       / PDM_CLE0_M1       / GPI04_A1_G         / ERC_SDD012       / GMAC1_TXD3_M1       / UART7_TX_M2       / PDM_SD13_M1       / GPI04_A2_G         / ERC_SDD013       / GMAC1_TXD1_M1       / UART7_TX_M2       / I282_LRCK_TX_M1       / GPI04_A2_G         / ERC_SDD014       / GMAC1_TXD1_M1       / UART7_TX_M2       / I282_LRCK_TX_M1       / GPI04_A2_G         / ERC_SDD015       / GMAC1_TXD1_M1       / UART7_TX_M2       / I282_LRCK_TX_M1       / GPI04_A2_G         / ERC_SDD014       / GMAC1_TXDN_M1       / UART	CIF D3	/ EBC SDDO2				
<pre>/ EBC SDD05 / SDMMC2 CIK N0 / I231 SDI1 M1 / VOP BF656 D5 M1 / GF103 D3 d / EBC SDD06 / SDMMC2 FWREN N0 / I231 SDI3 M1 / VOP BF656 D5 M1 / GF103 D4 d / EBC SDD07 / SDMMC2 FWREN N0 / I231 SDI3 M1 / VOP BF656 D5 M1 / GF103 D5 d / EBC SDD08 / GMAC1 TXD2 M1 / UART1 TX M1 / FDM CLKO M1 / GF103 D5 d / EBC SDD00 / GMAC1 TXD2 M1 / UART1 RX M1 / FDM CLKO M1 / GF103 D7 d / EBC SDD010 / GMAC1 TXD2 M1 / UART1 RX M1 / FDM CLKO M1 / GF103 D7 d / EBC SDD010 / GMAC1 TXD2 M1 / UART1 RX M1 / FDM CLKO M1 / GF104 A0 d / EBC SDD010 / GMAC1 TXD2 M1 / UART1 TX M2 / FDM SDI0 M1 / GF104 A0 d / EBC SDD010 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SDI1 M1 / GF104 A3 d / EBC SDD013 / GMAC1 FXD3 M1 / UART7 TX M2 / FDM SDI1 M1 / GF104 A3 d / EBC SDD014 / GMAC1 FXD3 M1 / UART7 TX M2 / FDM SDI1 M1 / GF104 A3 d / EBC SDD013 / GMAC1 TXD0 M1 / UART7 TX M2 / FDM SDI3 M1 / GF104 A3 d / EBC SDD014 / GMAC1 TXD0 M1 / UART7 TX M2 / FDM SDI3 M1 / GF104 A3 d / EBC SDD015 / GMAC1 TXD1 M1 / UART7 TX M2 / I232 LRCK TX M1 / GF104 A3 d / EBC SDD015 / GMAC1 TXD1 M1 / UART7 TX M2 / I232 LRCK RX M1 / GF104 A5 d / EBC SDD015 / GMAC1 TXD1 M1 / SF13 CS1 M0 / I231 SCIK RX M1 / GF104 A6 d / EBC SDCE2 / GMAC1 FXD1 M1 / SF13 M150 M0 / I231 SCIK RX M1 / GF104 A6 d / EBC SDCE2 / GMAC1 FXD1 M1 / SF13 M150 M0 / I231 SCIK RX M1 / GF104 A6 d / EBC SDCE2 / GMAC1 FXD1 M1 / SF13 M150 M0 / I231 SCIK RX M1 / GF104 A6 d / EBC SDCE2 / GMAC1 FXD1 M1 / SF13 M150 M0 / I231 SCIK RX M1 / GF104 B1 d / EBC SDCE2 / GMAC1 FXEN M1 / SF13 M150 M0 / I231 SCIM M1 / GF104 B1 d / EBC SDCE2 / GMAC1 FXEN M1 / SF13 M150 M0 / I231 SCOL M1 / GF104 B1 d / EBC SDCE3 / GMAC1 FXEN M1 / SF13 SCLK M0 / I231 SCOL M1 / GF104 B1 d / EBC SDCE2 / GMAC1 FXEN M1 / SF13 SCLK M0 / I231 SCOL M1 / GF104 B1 d / EBC SDCE2 / GMAC1 FXEN M1 / SF13 SCLK M0 / I232 SDI M1 / GF104 B1 d / EBC SDCE4 / ETHL FFECHC2 S5M M1 / SF13 SCLK M0 / I232 SDI M1 / GF104 B1 d / EBC SDEF / CAN2 FX M0 / I351 SCLK M0 / I231 SDO3 M1 / GF104 B1 d / EBC SDEF / GMAC1 MC0 M1 / UART1 RTSn M1 / I232 MCLK M1 / GF104 B1 d / EBC SDEF / GMAC1 MC0 M1 / UART</pre>	CIF D4					
Z EBC SDD06       / SDMMC2 DET M0       / I281 SDI3 M1       / VOE BE655 D6 M1 / GP103 D4 d         Z EBC SDD07       / SDMMC2 PRREN M0       / I281 SDI3 M1       / VOE BE656 D7 M1 / GP103 D5 d         / EBC SDD08       / GMAC1 TXD2 M1       / UART1 TX M1       / PDM CLK0 M1       / GP103 D7 d         / EBC SDD09       / GMAC1 TXD2 M1       / UART1 TX M1       / PDM CLK0 M1       / GP103 D7 d         / EBC SDD010       / GMAC1 TXD2 M1       / UART1 TX M1       / PDM CLK1 M1       / GP104 A0 d         / EBC SDD011       / GMAC1 FXD2 M1       / UART1 TX M2       / PDM CLK1 M1       / GP104 A0 d         / EBC SDD012       / GMAC1 FXD2 M1       / UART7 TX M2       / PDM SDI3 M1       / GP104 A2 d         / EBC SDD013       / GMAC1 FXD2 M1       / UART7 TX M2       / PDM SDI3 M1       / GP104 A3 d         / EBC SDD014       / GMAC1 FXD1 M1       / UART9 TX M2       / PDM SDI3 M1       / GP104 A3 d         / EBC SDD015       / GMAC1 FXD1 M1       / UART9 TX M2       / I282 LBCK TX M1       / GP104 A5 d         / EBC SDD014       / GMAC1 FXD1 M1       / UART9 TX M2       / I281 SDIA M1       / GP104 A5 d         / EBC SDD015       / GMAC1 FXD1 M1       / UART9 TX M2       / I281 SDIA M1       / GP104 A5 d         / EBC SDCE0       / GMAC1 FXD1 M1       / UAR	CIF D5	/ EBC SDD05		/ 1281 SD10 M1		
/ EBC SDD07       / SDMAC2 PWREN M0       / 1281 SD13 M1       / VOP_BT656 D7 M1 / GP103 D5 d         / EBC SDD08       / GMAC1 TXD2 M1       / UART1 TX M1       / PDM_CLK0 M1       / GP103 D6 d         / EBC SDD019       / GMAC1 TXD3 M1       / UART1 TX M1       / PDM_CLK0 M1       / GP103 D6 d         / EBC SDD019       / GMAC1 TXD3 M1       / UART1 RX M1       / PDM_CLK1 M1       / GP104 A0 d         / EBC SDD011       / GMAC1 FXD2 M1       / UART7 TX M2       / PDM_SD11 M1       / GP104 A0 d         / EBC SDD012       / GMAC1 FXD2 M1       / UART7 TX M2       / PDM_SD13 M1       / GP104 A2 d         / EBC SDD014       / GMAC1 FXD1 M1       / UART7 TX M2       / PDM_SD13 M1       / GP104 A2 d         / EBC SDD015       / GMAC1 FXD1 M1       / UART7 TX M2       / PDM_SD13 M1       / GP104 A2 d         / EBC SDD015       / GMAC1 FXD1 M1       / UART7 TX M2       / PDM_SD13 M1       / GP104 A3 d         / EBC SDD015       / GMAC1 FXD1 M1       / UART7 TX M2       / PDM_SD13 M1       / GP104 A5 d         / EBC SDC014       / GMAC1 FXD1 M1       / UART7 SX M2       / I281 SDC1 M1       / GP104 A6 d         / EBC SDC25       / GMAC1 FXDN M1       / SP13 CS1 M0       / I281 SD01 M1       / GP104 A7 d, d         / EBC SDC25       / GMAC1 FXDV CRS M1	CIF D6					
<pre>/ EBC SDD08 / GMAC1 TXD2 M1 / UART1 TX M1 / FDM CLK0 M1 / GF103 D6 d / EBC SDD09 / GMAC1 TXD2 M1 / UART1 RX M1 / FDM SD10 M1 / GF103 A0 d / EBC SDD010 / GMAC1 TXD1K M1 / UART7 RX M1 / FDM SD10 M1 / GF104 A0 d / EBC SDD011 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SD11 M1 / GF104 A0 d / EBC SDD012 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SD11 M1 / GF104 A0 d / EBC SDD013 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SD13 M1 / GF104 A0 d / EBC SDD014 / GMAC1 FXD0 M1 / UART7 TX M2 / FDM SD13 M1 / GF104 A0 d / EBC SDD014 / GMAC1 FXD0 M1 / UART7 TX M2 / FDM SD13 M1 / GF104 A0 d / EBC SDD014 / GMAC1 FXD0 M1 / UART7 TX M2 / FDM SD13 M1 / GF104 A0 d / EBC SDD014 / GMAC1 FXD0 M1 / UART7 FX M2 / IZ32 LECK FX M1 / GF104 A5 d / EBC SDD015 / GMAC1 FXDN M1 / SF13 CS0 M0 / IZ31 SCHK RX M1 / GF104 A5 d / EBC SDCE1 / GMAC1 FXDN M1 / SF13 MISC M0 / IZ31 SCHK RX M1 / GF104 A6 d / EBC SDCE2 / GMAC1 FXD1 M1 / SF13 MISC M0 / IZ31 SD01 M1 / GF104 B0 d / EBC SDCE3 / GMAC1 FXDN M1 / SF13 MOST M0 / IZ31 SD01 M1 / GF104 B0 d / EBC SDCE3 / GMAC1 FXDR M1 / SF13 MOST M0 / IZ31 SD02 M1 / GF104 B1 d / EBC SDCE3 / GMAC1 FXER M1 / SF13 MOST M0 / IZ31 SD00 M1 / GF104 B1 d / EBC SDCE3 / GMAC1 FXER M1 / SF13 MOST M0 / IZ31 SD00 M1 / GF104 B1 d / EBC SDCE3 / GMAC1 FXER M1 / SF13 MOST M0 / IZ31 SD00 M1 / GF104 B3 d / EBC SDCE4 / FTH1 FEFCLFO 25M M1 / SF13 CLK M0 / IZ31 SD00 M1 / GF104 B3 d / EBC SDCE5 / GMAC1 RXER M1 / SF13 MOST M0 / IZ31 SD00 M1 / GF104 B3 d / EBC SDCE5 / GMAC1 RXER M1 / SF13 MOST M0 / IZ31 SD00 M1 / GF104 B3 d / EBC SDCE5 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SD0 M1 / GF104 B3 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B3 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B3 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B5 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B5 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B7 d / EBC SDCE4 / GMAC1 MDC M1 / UART1 RTSN M1 / IZ32 SCHK TX M1 / GF104 B7 d / EBC SDCE4 / GMAC1 MDC M1 / UAR</pre>	CIF D7					
/ ERC SDD03 / GMAC1 TXD2 M1 / UART1 TX M1 / FDM SD10 M1 / GFL03 D5 d / ERC SDD03 / GMAC1 TXD2 M1 / UART1 RX M1 / FDM SD10 M1 / GFL03 D7 d / ERC SDD010 / GMAC1 TXD2 M1 / UART7 TX M2 / FDM SD11 M1 / GFL04 A0 d / ERC SDD011 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SD11 M1 / GFL04 A1 d / ERC SDD013 / GMAC1 FXD2 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A2 d / ERC SDD013 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A3 d / ERC SDD014 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A3 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A4 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A4 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A5 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A6 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A6 d / ERC SDD015 / GMAC1 FXD1 M1 / UART7 TX M2 / FDM SD13 M1 / GFL04 A6 d / ERC SDD015 / GMAC1 FXD1 M1 / SFL3 CSD M0 / FDS1 RCK RX M1 / GFL04 A6 d / ERC SDCE1 / GMAC1 FXDN M1 / SFL3 CSL M0 / FDS1 RCK RX M1 / GFL04 A6 d / ERC SDCE2 / GMAC1 FXDV CRS M1 / SFL3 CSL M0 / FDS1 RCK RX M1 / GFL04 R0 d / ERC SDCE3 / GMAC1 FXDV CRS M1 / SFL3 CLK M0 / FDS1 SD01 M1 / GFL04 R0 d / ERC SDCE3 / GMAC1 FXDV CRS M1 / SFL3 CLK M0 / FDS1 SD02 M1 / GFL04 R2 d / ERC SDCE3 / GMAC1 FXDV CRS M1 / SFL3 CLK M0 / FDS1 SD02 M1 / GFL04 R2 d / ERC SDCE3 / GMAC1 FXDV CRS M1 / SFL3 CLK M0 / FDS1 SD02 M1 / GFL04 R2 d / ERC SDCE4 / FTHL FEFCLK0 25M M1 / SFL3 CLK M0 / FDS2 SD0 M1 / GFL04 R3 d / ERC SDSF / CAN2 FX M0 / FDFL FASH TFNGIN / VOP BFC56 CLK M1 / GFL04 R3 d / ERC SDSF / CAN2 FX M0 / FDFL FASH TFNGIN / VOP BFC56 CLK M1 / GFL04 R5 d / ERC SDSF / GMAC1 MDC M1 / UART1 RTSn M1 / FDS2 SD0 M1 / GFL04 R5 d / ERC SDSF / GMAC1 MDC M1 / UART1 RTSn M1 / FDS2 SD2 M1 / GFL04 R5 d / ERC SDSF / GMAC1 MDC M1 / UART1 RTSn M1 / FDS2 SCRK TX M1 / GFL04 R5 d / ERC SDSF / GMAC1 MDC M1 / UART1 RTSn M1 / FDS2 SCRK TX M1 / GFL04 R5 d / ERC SDSF / GMAC1 MDC M1 / UART1 RTSn M1 / FDS2 SCRK TX M1 / GFL04 R5 d / ERC SDDCE	011 07	7 850 65507	/ DEMNCE FWICH NO	/ 1251 5515 MI	/ VOL BIGGO D/ HI /	GF103 D5 d
ERC_SDD09      GRACI_TXD3_M1      UART1_RX_M1      FDM_SDI0_M1      GF103_D7_d        ERC_SDD011      GMACI_TXCLK_M1      FDM_SDI0_M1      GF104_A0_d      GF104_A0_d        ERC_SDD011      GMACI_RXD2_M1      FDM_SDI1_M1      GF104_A0_d      GF104_A0_d        ERC_SDD011      GMACI_RXD2_M1      UART7_RX_M2      FDM_SDI1_M1      GF104_A2_d        ERC_SDD013      GMACI_RXD1_M1      UART7_RX_M2      FDM_SDI3_M1      GF104_A2_d        ERC_SDD014      GMACI_RXD1_M1      UART7_RX_M2      FDM_SDI3_M1      GF104_A2_d        ERC_SDD015      GMACI_RXD1_M1      UART7_RX_M2      IZ32_LRCR_RX_M1      GF104_A5_d        ERC_SDD015      GMACI_RXD1_M1      UART7_RX_M2      IZ32_LRCR_RX_M1      GF104_A5_d        ERC_SDD015      GMACI_RXD0_M1      UART7_RX_M2      IZ32_LRCR_RX_M1      GF104_A5_d        ERC_SDCE0      GMACI_RXD0_M1      SF13_CS1_M0      I231_LS0LR_RX_M1      GF104_A7_d	CIF D8	/ EBC SDDO8	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLK0 M1 /	GPTO3 D6 d
ERC_SDDD10/_GMAC1_TXCLK_M1      / FUN_CLKL_M1      / FUN_CLKL_M1       FUN_A0_d        ERC_SDD011/_GMAC1_TXCLK_M1       UART7_TX_M2       FUN_SD11_M1	CIF D9					
ZERC SDD011 / GNACL FXD2 ML       / FDM SDL1 ML       / GFL04 AL d         / ERC SDD012 / GNACL FXD2 ML       / UART7 TX M2       / FDM SDL3 ML       / GFL04 AL d         / ERC SDD013 / GNACL FXD2 ML       / UART7 TX M2       / FDM SDL3 ML       / GFL04 AL d         / ERC SDD014 / GNACL FXD2 ML       / UART7 TX M2       / FDM SDL3 ML       / GFL04 AL d         / ERC SDD014 / GNACL FXD2 ML       / UART7 TX M2       / FDM SDL3 ML       / GFL04 AL d         / ERC SDD015 / GNACL TXD1 ML       / UART7 TX M2       / IZ82 LRCK TX ML       GFL04 AL d         / ERC SDD014 / GNACL TXD1 ML       / UART7 TX M2       / IZ82 LRCK TX ML       GFL04 AL d         / ERC SDD015 / GNACL TXDN ML       / UART7 TX M2       / IZ81 SLCK RX ML       GFL04 AL d         / ERC SDCE0 / GNACL TXDN ML       / SFL3 CS1 M0       / IZ81 SLCK RX ML       GFL04 AL d         / ERC SDCE2 / GNACL FXDN ML       / SFL3 CS1 M0       / IZ81 SD01 ML       GFL04 AL d         / ERC SDCE3 / GNACL FXDN CRS ML       / SFL3 MOSL M0       / IZ81 SD02 ML       GFL04 BL d         / ERC SDCE3 / GNACL FXER ML       / SFL3 MOSL M0       / IZ81 SD02 ML       GFL04 BL d         / ERC SDCE3 / GNACL FXER ML       / SFL3 MOSL M0       / IZ82 SD0 ML       GFL04 BL d         / ERC SDCE3 / GNACL FXER ML       / SFL3 MOSL M0       / IZ82 SD0 ML       G	CIF D10					
ERC_SDD012      GRAC1_EXD3 M1      UART7 TX M2      EDM SD12 M1      GF104 A2_d        ERC_SDD013      GMAC1_EXCLR_M1      UART7 TX M2      PDM SD13 M1      GF104 A2_d        ERC_SDD014      GMAC1_EXCLR_M1      UART7 TX M2      PDM SD13 M1      GF104 A2_d        ERC_SDD014      GMAC1_EXCLR_M1      UART7 TX M2      PDM SD13 M1      GF104 A3_d        ERC_SDD015      GMAC1_EXCLM_M1      UART5 TX M2      I232 LRCFK_TX M1      GF104 A5_d        ERC_SDCE0      GMAC1_TXEN_M1      UART5 TX M2      I231 SCLK_TX M1      GF104 A6_d        ERC_SDCE0      GMAC1_TXEN_M1      SF13 CS0 M0      I231 SCLK_TX M1      GF104 A6_d	CIF D11					
./ ERC_SDE013 / GMAC1_PXCLK_M1 / UART7_RX_M2 / FEM_SDI3_M1 / GPI04_A3_d         ./ ERC_SDE013 / GMAC1_TXE0_M1 / UART5_TX_M2 / I282_LRCK_TX_M1 / GPI04_A4_d         ./ ERC_SDE015 / GMAC1_TXE1_M1 / UART5_RX_M2 / I282_LRCK_RX_M1 / GPI04_A5_d         ./ ERC_SDE00 / GMAC1_TXEN_M1 / UART5_RX_M2 / I282_LRCK_RX_M1 / GPI04_A5_d         ./ ERC_SDCE0 / GMAC1_TXEN_M1 / SF13_CS0_M0 / I231_SCLK_RX_M1 / GPI04_A6_d         ./ ERC_SDCE1 / GMAC1_FXE0_M1 / SF13_CS1_M0 / I231_SCLK_RX_M1 / GPI04_A6_d         ./ ERC_SDCE2 / GMAC1_RXD1_M1 / SF13_CS1_M0 / I231_SD01_M1 / GPI04_A6_d         ./ ERC_SDCE3 / GMAC1_RXD1_M1 / SF13_MISO_M0 / I231_SD01_M1 / GPI04_B1_d         ./ ERC_SDCE3 / GMAC1_RXD2_CRS_M1 / SF13_MOS1_M0 / I231_SD02_M1 / GPI04_B1_d         ./ ERC_GDCE / ETHL EFFCLK0_25M_M1 / SF13_CLK_M0 / I282_SD1_M1 / GPI04_B3_d         ./ ERC_GDSF_ / CANC1_RXEM_M1 / LSF13_CLK_M0 / I282_SD0_M1 / GPI04_B3_d         ./ ERC_SDSF_ / CANC1_RX_M0 / LSF1_SCLK_M0 / I282_SD0_M1 / GPI04_B3_d         ./ ERC_SDSF_ / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SD0_M1 / GPI04_B5_d         ./ ERC_SDSF_ / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SCLK_TX_M1 / GPI04_B6_d         ./ ERC_SDCE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SCLK_TX_M1 / GPI04_B6_d         ./ ERC_SDCE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SCLK_TX_M1 / GPI04_B6_d         ./ ERC_SDCE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SCLK_TX_M1 / GPI04_B6_d         ./ ERC_SDCE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I282_SCLK_TX_M1 / GPI04_B6_d         ./ ERC_SDCLK / GMAC1_MDC_M1 / FMM1_IR_M1	CIF D12			/ UART7 TX M2		
	CIF D13					
ERC_SDDD15/_GMAC1_TXD1_M1UART9_RX_M2I232_LRCK_RX_M1GP104_A5_d         FERC_SDCE0GMAC1_TXEN_M1SP13_CS0_M0I231_RCK_RX_M1_/_GP104_A6_d        ERC_SDCE1GMAC1_RXD0_M1SP13_CS1_M0I231_RCK_RX_M1_/_GP104_A6_d        ERC_SDCE2GMAC1_RXD1_M1SP13_MISO_M0I231_RCK_RX_M1_/_GP104_A6_d        ERC_SDCE3GMAC1_RXDV_CRS_M1SP13_MISO_M0I231_SD01_M1GP104_B1_d        ERC_GDCE3GMAC1_RXDV_CRS_M1SP13_MOSI_M0I232_SD1_M1GP104_B2_d        ERC_GDCEETHL_REFCLE0_25M_M1SP13_CLK_M0I232_SD1_M1GP104_B3_d        ERC_GDCEETHL_REFCLE0_25M_M1SP13_CLK_M0I232_SD0_M1GP104_B3_d        ERC_SDSHRCAN2_TX_M0ISP13_CLK_M0I232_SD0_M1GP104_B4_d        ERC_SDSHRCAN2_TX_M0ISP13_CLK_M1UCE1_SD03_M1GP104_B4_d        ERC_SDSHRCAN2_TX_M0IBF1ASH_TRIGINUCE1_SD03_M1GP104_B5_d        ERC_SDCE4GMAC1_MDC_M1UART1_RTSN_M1I232_SCLK_TX_M1GP104_B6_d        ERC_SDCE4GMAC1_MDIO_M1IRM11_IR_M1      GP104_C0_d	CIF D14					
F. / EBC SDCE0 / GMAC1 TXEN M1 / SF13 CS0 M0 / I281 SCLK RX M1 / GF104 A6 d         / EBC SDCE1 / GMAC1 RXD0 M1 / SF13 CS1 M0 / I281 SCLK RX M1 / GF104 A7 d         / EBC SDCE2 / GMAC1 RXD1 M1 / SF13 MISO M0 / I281 SD01 M1 / GF104 B0 d         IG / EBC SDCE3 / GMAC1 RXD1 M1 / SF13 MISO M0 / I281 SD02 M1 / GF104 B1 d         / EBC SDCE3 / GMAC1 RXD1 M1 / SF13 MOSI M0 / I281 SD02 M1 / GF104 B1 d         / EBC SDCE3 / GMAC1 RXDR M1 / SF13 MOSI M0 / I282 SD1 M1 / GF104 B3 d         / EBC GOSE / ETHL REFELKO 25M M1 / SF13 CLK M0 / I282 SD0 M1 / GF104 B3 d         / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BF656 CLK M1/ GF104 B3 d         / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BF656 CLK M1/ GF104 B5 d         / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 SDCK M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B5 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B7 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSn M1 / I282 SCLK TX M1 / GF104 B7 d         / EBC SDLE / GMAC1 MDTO M1 / UART1 RTSN M1 / I282 SCLK TX M1 / GF104 B7 d	CIF D15				/ T282 LRCK RX M1 /	
F		7 120 022010	/			01101 110 0
ERC SDCE1 (GMACI FXD0 MI / SFI3.C31.M0 / IA31 LRCK.RX.MI / GFI04.A7.d. / ERC SDCE2 / GMACI FXD1 MI / SFI3 MISO M0 / IA31 SDO1 MI / GFI04 B0 d / ERC SDCE3 / GMACI FXDV CRS MI / SFI3 MOSI M0 / IA31 SDO1 MI / GFI04 B1 d / ERC VCOM / GMACI FXER MI / SFI3 MOSI M0 / IA32 SDI MI / GFI04 B2 d / ERC GDCE / ETHI FEFCIKO 25M MI / SFI3 CLK M0 / IA32 SDO MI / GFI04 B3 d / ERC GDSF / CAN2 FX M0 / ISF FLASH TRIGIN / VOP BF656 CLK MI/ GFI04 B3 d / ERC SDSHR / CAN2 FX M0 / ISF FLASH TRIGIN / VOP BF656 CLK MI / GFI04 B3 d / ERC SDSHR / CAN2 FX M0 / ISF FLASH TRIGIN / VOP BF656 CLK MI / GFI04 B5 d / ERC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I232 SDLK M1 / GFI04 B5 d / ERC SDDE / GMAC1 MDC M1 / UART1 RTSn M1 / I232 SDLK M1 / GFI04 B5 d / ERC SDDE / GMAC1 MDC M1 / FMM11 IR M1 GFI04 B7 d	ISP FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CS0 M0	/ 1281 SCLK RX M1 /	GPIO4 A6 d
/ EBC SDCE2         / GMAC1 EXD1 M1         / SF13 MISO M0         / I281 SDO1 M1         / GF104 B0 d           IG / EBC SDCE3         / GMAC1 EXDV CRS M1         / I281 SDO2 M1         / GF104 B1 d           / EBC VCOM         / GMAC1 EXER M1         / SF13 MOSI M0         / I282 SDI M1         / GF104 B2 d           / EBC GDOE         / EFH1 EFFCLKO 25M M1         / SF13 CLK M0         / I282 SDI M1         / GF104 B2 d           / EBC GDOE         / EFH1 EFFCLKO 25M M1         / SF13 CLK M0         / I282 SDO M1         / GF104 B2 d           / EBC GDOE         / EFH1 EFFCLKO 25M M1         / SF13 CLK M0         / I282 SDO M1         / GF104 B2 d           / EBC GDOE         / EBC SDSH         / CAN2 FX M0         / I387 FLASH TRIGIN         / VOP BT656 CLK M1         GF104 B4 d           / EBC SDSH         / CAN2 FX M0         / I387 SDO3 M1         GF104 B5 d         / GF104 B5 d           / EBC SDLE         / GMAC1 MDC M1         / UART1 RTSh M1         / I282 NCLK M1         GF104 B7 d           / EBC SDOE         / GMAC1 MDC M1         / UART1 RTSh M1         / I282 SCLK TX M1         GF104 B7 d           / EBC SDOE         / GMAC1 MDO M1         / F70011 IR M1         / I282 SCLK TX M1         GF104 B7 d						
IG / EBC SDCE3 / GMAC1 RXDV CRS M1 / SP13 MOSI M0 / I2S1 SDO2 M1 / GP104 B1 d / EBC VCOM / GMAC1 RXER M1 / SP13 MOSI M0 / I2S2 SDI M1 / GP104 B2 d / EBC GDOE / ETHI REFCLEO 25M M1 / SP13 CLR M0 / I2S2 SDO M1 / GP104 B3 d / EBC GDSF / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BE556 CLK M1/ GP104 B3 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BE556 CLK M1/ GP104 B3 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BE556 CLK M1/ GP104 B3 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BE556 CLK M1/ GP104 B5 d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSN M1 / I2S2 MCLK M1 / GP104 B5 d / EBC SDDE / GMAC1 MDC M1 / UART1 RTSN M1 / I2S2 SCLK TX M1 / GP104 B7 d / EBC SDCE / GMAC1 MDIO M1 / FWM11 IR M1 / GP104 C0 d	CAM CLKOUT0					
IG         / EBC_SDCE3         / GMAC1_FXEV_CRS_M1         / I281_SD02_M1         / GF104_B1_d           / EBC_VCOM         / GMAC1_FXER_M1         / SF13_MOSI_M0         / I282_SDI_M1         / GF104_B2_d           / EBC_GDCE         / ETHL REFCIKO_25M_M1         / SF13_CLK_M0         / I282_SDO_M1         / GF104_B3_d           / EBC_GDSE         / CAN2_FX_M0         / ISP_FLASH_TRIGIN         / VOR_BT656_CLK_M1/         GF104_B3_d           / EBC_SDSHR         / CAN2_FX_M0         / ISP_FLASH_TRIGIN         / VOR_BT656_CLK_M1/         GF104_B5_d           / EBC_SDSHR         / CAN2_FX_M0         / ISP_FLASH_TRIGIN         / VOR_BT656_CLK_M1/         GF104_B5_d           / EBC_SDLE         / GMAC1_MDC_M1         / UART1_RT9n_M1         / I282_MCLK_M1         GF104_B5_d           / EBC_SDDE         / GMAC1_MDIO_M1         / UART1_RT9n_M1         / I282_SCLK_TX_M1         GF104_B7_d           / EBC_SDDE         / GMAC1_MDIO_M1         / FMM11_IR_M1         GF104_B7_d         / GF104_B7_d	CAM CLKOUT1	7 EBC SDCE2	/ GMACI RXDI MI	/ SPI3 MISO MU	/ 1281 SDOI MI /	GPIO4 BU d
/ EBC VCOM / GMAC1 RXER M1 / SPI3 MOSI M0 / I282 SDI M1 / GPI04 B2 d / EBC GDOE / ETHL REFCLKO 25M M1 / SPI3 CLK M0 / I282 SDO M1 / GPI04 B3 d / EBC GDSP / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1/ GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M1 / GPI04 B4 d / EBC SDSHR / CAN2 RX M0 / ISP FLASH TRIGIN / ISP FLASH TR	TOD DDDTTCUE EDTC	( EDG 000E2	( CMR C1		( T221 2D02 M1 (	00704 01 1
/ EBC VCOM / GMAC1 FXER M1 / SPI3 MOST M0 / [1322 SDI M1 / GF104 B2.d / EBC GDOE / ETHL REFCLEO 25M M1 / SPI3 CLK M0 / [1322 SDO M1 / GF104 B3.d / EBC GDSF / CAN2 FX M0 / ISP FLASH TRIGIN / VOF BT656 CLK M1/ GF104 B5.d / EBC SDSHR / CAN2 TX M0 / ISP FLASH TRIGIN / VOF BT656 CLK M1/ GF104 B5.d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSh M1 / [1232 MCLK M1 / GF104 B5.d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSh M1 / [1232 SCLK TX M1 / GF104 B5.d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSh M1 / [1232 SCLK TX M1 / GF104 B7.d / EBC SDCLK / GMAC1 MDIO M1 / FWM11 IR M1 / [1232 SCLK TX M1 / GF104 B7.d	15F FREDIGHT IRIG	7 EBC BDCES	7 GMACI RADV CR5 MI		/ 1251 5D02 MI /	GPI04 BI a
<pre>/ FRC GDOE / ETHL REFCLKO 25M MI / SFL3 CLK M0 / I282 SDO MI / GFL04 B3 d / ERC GDSP / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B4 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B5 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B5 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B5 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B5 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / VOP BT656 CLK MI/ GFL04 B5 d / ERC SDBR / CAN2 TX M0 / ISP FLASH TRIGIN / IZ81 SD03 M1 / GFL04 B5 d / ERC SDDE / GMAC1 MDC M1 / VART1 RTSn M1 / IZ82 NCLK TX M1 / GFL04 B7 d / ERC SDGE / GMAC1 MDIO M1 / FWM11 IR M1 / GFL04 C0 d / ERC GDCLK</pre>	I2C4 SDA MO	/ FRC VCOM	CMACI EVER MI	/ SDI3 MOST MO	/ T292 SDT M1 /	CDTO4 P2 d
/ EBC GDSP / CAN2 RX M0 / ISP FLASH TRIGIN / VOP BT656 CLK M/ GPI04 B4 d / EBC SDSHR / CAN2 TX M0 / I281 SD03 M1 / GPI04 B5 d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSN M1 / I282 MCLK M1 / GPI04 B6 d / EBC SDLE / GMAC1 MDC M1 / UART1 RTSN M1 / I282 MCLK M1 / GPI04 B7 d / EBC SDCE / GMAC1 MDIO M1 / UART1 RTSN M1 / I282 SCLK TX M1 / GPI04 B7 d / EBC SDCLK / FWM11 IR M1 / GPI04 C0 d	I2C4 SCL M0					
	1204 BCH M0	7 EBC GDOE	7 EIIII KEPCHKO 25M M	II / SFIS CHK MO	/ 1232 3D0 M1	0F104 D5 G
/ EBC_SDSHR / CAN2_TX_M0 / UART1_RTSn_M1 / I2S1_SD03_M1 / GPI04_B5_d / EBC_SDLE / GMAC1_MDC_M1 / UART1_RTSn_M1 / I2S2_MCLK_M1 / GPI04_B6_d / EBC_SD0E / GMAC1_MDI0_M1 / I2S2_SCLK_TX_M1 / GPI04_B7_d / EBC_SD0E / GMAC1_MDI0_M1 / FWM11_IR_M1 / GPI04_C0_d	I2C2 SDA M1	/ EBC GDSP	/ CAN2 BX MO	/ TSP FLASH TRIGIN	/ VOR BT656 CLK M1/	GPTO4 B4 d
/ EBC SDLE / GMAC1 MDC M1 / UART1 RTSh M1 / I2S2 MCLK M1 / GPI04 B6 d // EBC SDOE / GMAC1 MDIO M1 / I2S2 SCLK TX M1 / GPI04 B7 d // EBC GDCLK / FWM11 IR M1 / GPI04 C0 d	I2C2 SCL M1					
/ EBC SDLE / GMAC1 MDC M1 / UART1 RTSn M1 / I232 MCLK M1 / GFIQ4 B6 d / EBC SDDE / GMAC1 MDIO M1 / I232 SCLK TX M1 / GFIQ4 B7 d / EBC GDCLK / FWM11 IR M1 GFIQ4 C0 d	1200 000 111	/ 220 02011(	/ 01410 111 110		/ 1001 0000 111 /	01101 D5 d
/ ERC SDOE / GMACI MDIO M1 / I232 SCLK IX M1 / GPIO4 B7 d - / I232 SCLK IX M1 / GPIO4 B7 d - / ERC SDOLK / FWM11 IR M1 / GPIO4 C0 d -	CIF HREF	/ EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ T2S2 MCLK M1	GPTO4 B6 d
/ EBC GDCLK / FWM11 IR M1 GPI04 C0 d	CIF VSYNC					
/ EBC_GDCLK / FWM11_IR_M1 GPI04_C0_d	CIT VOINC	7 100 0000	/ ONNOT NDTO MI		/. 1202_0021(_1A_M1_/	01101 D7 u
	CIF CLEOUT	/ EBC GDCLK		/ PWM11 TR M1		GPTO4 C0 d
/ EBC SDCLK / GMAC1 MCLKINOUT M1 / UART1 CTSh M1 / 1232 SCLK RX M1 / GP104 C1 d		/ 100 000000				01101 00 0
	CIE CLEIN	/ EBC SDCLK	/ GMAC1 MCLEINOUT M1	/ UART1 CTSn M1	/ T282 SCLK BX M1	GPT04 C1 d
	CIF CLKOUT		/ GMAC1 MCLKINOUT M1		/ 1282 SCLK RX M1 /	

BGA636\_19R00X19R00X1R20

Figure 2-145 RK3568 I2S2 M1 functional pins

**RK3568 Hardware Design Guide** 

In I2S2 interface design, please note:

- I2S2\_M0 and I2S2\_M1 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve I2S2 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S2 interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
I2S2_MCLK	Pull-down	Connect a 220hm resistor in series	I2S system clock output
I2S2_SCLK_TX	Pull-down	Connect a 220hm resistor in series	I2S continuous SCLK (TX, related AudioPlay)
I2S2_LRCK_TX	Pull-down	Connect a 220hm resistor in series	I2S frame clock for channel selection (TX, related AudioPlay)
I2S2_SDO	Pull-down	Direct connection	I2S serial data
I2S2_SCLK_RX	Pull-down	Connect a 220hm resistor in series	I2S continuous SCLK (RX, related AudioRecord)
I2S2_LRCK_RX	Pull-down	Connect a 220hm resistor in series	I2S frame clock for channel selection (RX, related AudioRecord)
I2S2_SDI	Pull-down	Direct connection	I2S serial data

#### Table 2–37 RK3568 I2S2 interface design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 220hm and 1000hm, as long as it can meet the SI test), as well as reserving TVS devices.

### 2.3.11.3 I2S3 interface

I2S3 interface contains independent 2-channel output and 2-channel input. This group only supports the same sampling rate of playback and record.

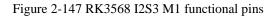
I2S3 interface pins multiplex in two different power domains:

• I2S3\_M0 is multiplexed in the VCCIO5 power domain.

LCDC D0	/ VOP BT656 D0 M0	/ SPIO MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2 /	GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPIÖ MOSI M1	/ PCIE20 WAKEn M1	/ 1251 SCLK TX M2 /	GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPIO CSO M1	/ PCIE30X1 CLKREQn M1 .	/ 12S1 LRCK TX M2 /	GPIO2 D2 d
LCDC D3 LCDC D4	/ VOP BT656 D3 M0	/ SPIO CLK M1	/ PCIE30X1 WAKEn M1	/ 12S1 SDI0 M2 /	GPIO2 D3 d
LCDC D4 LCDC D5	/ VOP BT656 D4 M0 / VOP BT656 D5 M0	/ SPI2 CS1 M1 / SPI2 CS0 M1	/ PCIE30X2 CLKREQn M1 . / PCIE30X2 WAKEn M1	/ 1251 SDI1 M2 / / 1251 SDI2 M2 /	GPIO2 D4 d GPIO2 D5 d
LCDC D6	/ VOP B1656 D5 M0 / VOP B1656 D6 M0	/ SPI2 CS0 MI / SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ 1251 5D12 M2 /	GPI02 D5 d GPI02 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ 12S1 SD00 M2 /	GPI02 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SD01 M2 /	GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1 ,	/ SDMMC2 D0 M1 /	GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1 /	GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ 12s3 sclk M0	/ SDMMC2 D2 M1 /	GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1 / / SDMMC2 CMD M1 /	GPIO3 A4 d
LCDC D12 LCDC D13	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1 / / SDMMC2 CLK M1 /	GPIO3 A5 d
LCDC D13 LCDC_D14	/ VOP BT1120 CLK / VOP BT1120 D5	/ GMAC1 TXCLK M0 / GMAC1 RXCLK M0	/ I2S3 SDI MO	/ SDMMC2 CLK M1 / / SDMMC2 CLK M1 / / SDMMC2 DET M1 /	GPIO3 A6 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLKO 25M M0		/ SDMMC2 PWREN M1 /	GPIO3 A7 d GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ РWM8 м0 /	GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ РWM9 M0 /	GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ 12C5 SCL M0	/ PDM SDIO M2 /	GPIO3 B3 d
LCDC D19 LCDC D20	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ 12C5 SDA M0 / 12C3 SCL M1	/ PDM SDI1 M2 /	GPIO3 B4 d
LCDC D20 LCDC D21	/ VOP BT1120 D11 / VOP BT1120 D12	/ GMAC1 TXD0 M0 / GMAC1 TXD1 M0	/ 12C3 SCL M1 / 12C3 SDA M1	/ PWM10 M0 /	GPIO3 B5 d
LCDC D21	/ PWM12 M0	/ GMACI TXDI MO / GMAC1 TXEN MO	/ UART3 TX M1	/ PWM11 IR M0 / / PDM SDI2 M2 /	GPIO3 B6 d GPIO3 B7 d
LCDC D23	/ PWM12 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2 /	GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2 /	GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2 /	GPI03 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ 1251 SCLK RX M2 /	GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0		/ PDM CLK1 M2 /	GPIO3 C4 d
PWM15 IR MO	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ 12S1 LRCK RX M2 /	GPIO3 C5 d
					VCCIO5_1 VCCIO5_2
3568					
A636_19R00X1	9R00X1R20				
			68 I2S3 M0 functio		

EDF         HPDIN         MO         / SPDIF         TX         M2         / SATA2         ACT         LED         / FCIE30X2         PERSTh         M2         / I2S3         LRCK         M1         / GPI04         C4           FWM12         M1         / SPI3         MISO         M1         / SATA1         ACT         LED         / UARTS         TX         M1         / I2S3         SDO         M1         / GPI04         C5           FWM13         M1         / SPI3         CSO         M1         / SATA0         ACT         LED         / UARTS         RX         M1         / I2S3         SDI         M1         / GPI04         C5           FWM13         M1         / SPI3         CSO         M1         / SATA0         ACT         LED         / UARTS         RX         M1         / I2S3         SDI         M1         / GPI04         C5           HDMITX_SCL         / I2C5         SCL         M1         / GPI04         C7	PWM14_M1	/ SPI3_CLK_M1	/ CAN1_RX_M1	/ PCIE30X2_CLKREQn_N		/ GPI04 C2 d
PWMI2 MI         / SPI3 MISO MI         / SATAI ACT LED         / UART9 TX MI         / I2S3 SDO MI         / GPI04 C5           PWMI3 MI         / SPI3 CS0 MI         / SATAO ACT LED         / UART9 AX MI         / I2S3 SDI MI         / GPI04 C5           HDMITX SCL         / I2C5 SCL MI         / GPI04 C6         / GPI04 C6         / GPI04 C6           HDMITX SCL         / I2C5 SCL MI         / GPI04 C7         / GPI04 C7         / GPI04 C7		/ SPI3 MOSI M1	/ CAN1 TX M1	/ PCIE30X2 WAKEn M2	/ I2S3 SCLK M1	/ GPIO4 C3 d
PWM13 MI         / SP13 CSO MI         / SATAO ACT LED / UART9 RX MI         / 1253 SDI MI         / GP104 C6           HDMITX SCL         / I2C5 SCL MI         / GP104 C7         / GP104 C7           HDMITX SDA         / I2C5 SDA MI         / GP104 D0         / GP104 D0						
HDMITX SDA / 12C5 SDA M1 / GPIO4 D0					/ 1253 SDO M1 / 1253 SDI M1	/ GPI04 C5 d
	HDMITX SDA	/ 12C5_SDA_M1				/ GPI04 C7 u / GPI04 D0 u / GPI04 D1 u
GPIO4 D2						GPIO4 D2 d

BGA636\_19R00X19R00X1R20



In I2S3 interface design, please note:

- I2S3\_M0 and I2S3\_M1 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to I2S peripheral IO level and

they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.

- In order to improve I2S3 interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of I2S3 interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
I2S3_MCLK	Pull-down	Connect a 220hm resistor in series	I2S system clock output
I2S3_SCLK	Pull-down	Connect a 220hm resistor in series	I2S continuous SCLK
I2S3_LRCK	Pull-down	Connect a 220hm resistor in series	I2S frame clock for channel selection
I2S3_SDO	Pull-down	Direct connection	I2S serial data
I2S3_SDI	Pull-down	Direct connection	I2S serial data

Tabla	2	38	DK3568	1253	interface	design
rable	2-	-30	KK2209	1233	interface	design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.4 PDM interface

RK3568 provides a group of PDM digital audio interface, and supports up to 8-channel PDM format audio input, the maximum sampling rate is 192kHz, and the bit rate is from 16bits to 32bits, in order to improve the effect caused by clock PCB routing. There are two PDM clocks of the same clock source and phase.

PDM interface pins multiplex in three different power domains:

• PDM\_M0 is multiplexed in the VCCIO1 power domain.

2C3 SDA M0 2C3 SCL M0	/ UART3 RX M0 / UART3 TX M0		/ CAN1 RX M0 / CAN1 TX M0		/ AUDIOPWM LOUT P / AUDIOPWM LOUT N	/ ACODEC ADC DATA / ACODEC ADC CLK	/ GPIO1 A0 u / GPIO1 A1 u
2s1 MCLK M0	/ UART3 RTSn M0		/ SCR CLK	/ PCIE30X1 PERSTn M2			/ GPIO1 A2 d
251 MCDK MO	/ OARIS RISH MO		/ SCR CHR	/ FCIESONI FERSIN M2			7 GP101 A2 d
2S1 SCLK TX M0	/ UART3 CTSn M0		/ SCR IO	/ PCIE30X1 WAKEn M2		/ ACODEC DAC CLK	/ GPIO1 A3 d
2S1 SCLK RX M0	/ UART4 RX M0 /	PDM CLK1 M0			/ SPDIF TX MÖ		/ GPIO1 A4 d
	/					,	
2S1 LRCK TX M0 2S1 LRCK RX M0	/ UART4 RTSn M0 / UART4 TX M0 /	PDM CLK0 M0	/ SCR RST	/ PCIE30X1 CLKREQn M2	/ AUDTOPWM ROUT P	/ ACODEC DAC SYNC	/ GPIO1 A5 d / GPIO1 A6 d
251 BRCK RA MU	/ UARIA IX MO /	FDM CLKO MO			/ AUDIOPWM ROUI P		/ GPIOI A6 d
12S1 SDO0 M0	/ UART4 CTSn M0		/ SCR DET		/ AUDIOPWM ROUT N	/ ACODEC DAC DATAL	/ GPIO1 A7 d
2S1 SD01 M0	/ I2S1 SDI3 M0 /	PDM SDI3 M0		/ PCIE20 CLKREQn M2		/ ACODEC DAC DATAR	/ GPIO1 A7 d / GPIO1 B0 d / GPIO1 B1 d
1251 SDO2 M0	/ I2S1 SDI2 M0 /	PDM SDI2 M0		/ PCIE20 WAKEn M2		/ ACODEC ADC SYNC	/ GPIO1 B1 d
1251 SDO3 M0	/ 12S1 SDI1 M0 /	PDM SDI1 M0		/ PCIE20 PERSTn M2			/ GPIO1 B2 d / GPIO1 B3 d
	I2S1 SDI0 M0 /	PDM SDIO MO					/ GPIO1 B3 d

Figure 2-148 RK3568 PDM M0 functional pins

• PDM\_M1 is multiplexed in the VCCIO6 power domain.

CIF D1	/ EBC SDDO0	/ SDMMC2 D0 M0	/ 12S1 MCLK M1	/ VOP BT656 D0 M1 /	GPIO3 C6 d
	/ EBC SDDO1	/ SDMMC2 D1 M0	/ I2S1 SCLK TX M1	/ VOP BT656 D1 M1 /	GPI03 C7 d
IF D2	/ EBC SDDO2	/ SDMMC2 D2 M0	/ I2S1 LRCK TX M1	/ VOP BT656 D2 M1 /	GPIO3 D0 d
IF D3	/ EBC SDDO3	/ SDMMC2 D3 M0	/ I2S1 SDO0 M1	/ VOP BT656 D3 M1 /	GPIO3 D1 d
IF D4	/ EBC SDDO4	/ SDMMC2 CMD M0	/ 12S1 SDI0 M1	/ VOP BT656 D4 M1 /	GPIO3 D2 d
IF D5	/ EBC SDDO5	/ SDMMC2 CLK M0	/ I2S1 SDI1 M1	/ VOP BT656 D5 M1 /	GPIO3 D3 d
IF D6	/ EBC SDDO6	/ SDMMC2 DET M0	/ I2S1 SDI2 M1	/ VOP BT656 D6 M1 /	GPIO3 D4 d
IF D7	/ EBC SDD07	/ SDMMC2 PWREN M0	/ 12S1 SDI3 M1	/ VOP BT656 D7 M1 /	GPIO3 D5 d
	(	( mm m1 mm 0 av1	(		
IF D8	/ EBC SDD08	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLKO M1 /	GPIO3 D6 d
IF D9	/ EBC SDD09	/ GMAC1 TXD3 M1	/ UART1 RX M1	/ PDM SDI0 M1 /	GPIO3 D7 d
IF D10	/ EBC SDD010	/ GMAC1 TXCLK M1		/ PDM CLK1 M1 /	GPIO4 A0 d
IF D11	/ EBC SDD011	/ GMAC1 RXD2 M1	/ TIND 07 00 MO	/ PDM SDI1 M1 /	GPIO4 A1 d
IF D12	/ EBC SDD012	/ GMAC1 RXD3 M1	/ UART7 TX M2	/ PDM SDI2 M1 /	GPIO4 A2 d
IF D13	/ EBC SDD013	/ GMAC1 RXCLK M1	/ UART7 RX M2	/ PDM SDI3 M1 /	GPIO4 A3 d
IF D14 IF D15	/ EBC SDD014 / EBC SDD015	/ GMAC1 TXD0 M1 / GMAC1 TXD1 M1	/ UART9 TX M2 / UART9 RX M2	/ 1282 LRCK TX M1 / / 1282 LRCK RX M1 /	GPIO4 A4 d GPIO4 A5 d
11 013	/ EBC SDD013	7 GMACI TADI MI	/ UARTS RA M2	/ 1252 BRCK RA MI /	GPI04 AJ d
SP FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CS0 M0	/ 1281 SCLK RX M1 /	GPIO4 A6 d
AM CLKOUTO	/ EBC SDCE1	/ GMAC1 RXD0 M1	/ SPI3 CS1 M0	/ 1281 LRCK RX M1 /	GPIO4 A7 d
AM CLKOUT1	/ EBC SDCE2	/ GMAC1 RXD1 M1	/ SPI3 MISO MO	/ I2S1 SDO1 M1 /	GPIO4 B0 d
SP PRELIGHT TRIG	( EDG (DOE)	/ GMAC1 RXDV CRS M1		/ 12s1 sdo2 m1 /	00704 01 1
SP PRELIGHT TRIG	/ LBC SDCES	7 GMACI RADV CR5 MI		/ 1251 5D02 MI /	GPIO4 B1 d
2C4 SDA M0	/ EBC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI MO	/ 1282 SDI M1 /	GPIO4 B2 d
2C4 SCL M0	/ EBC GDOE	/ ETH1 REFCLKO 25M M1	/ SPI3 CLK M0	/ I2S2 SDO M1 /	GPIO4 B3 d
	/ 220 0202		/	/ 2000 000 112	
2C2 SDA M1	/ EBC GDSP	/ CAN2 RX M0	/ ISP FLASH TRIGIN	/ VOP BT656 CLK M1/	GPIO4 B4 d
	/ ppg_gpgup	/ CAN2 TX M0		/ 12S1 SDO3 M1 /	GPIO4 B5 d
	/ EBC SDSHR				
2C2 SCL M1		(	( manual page 141	(	
2C2 SCL M1 IF HREF	/ EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ 1282 MCLK M1 /	GPIO4 B6 d
2C2 SCL M1		/ GMAC1 MDC M1 / GMAC1 MDIO M1	/ UART1 RTSn M1	/ 1282 MCLK M1 / / 1282 SCLK TX M1 /	GPI04 B6 d GPI04 B7 d
2C2 SCL M1 IF HREF	/ EBC SDLE		/ UART1 RTSn M1		

BGA636\_19R00X19R00X1R20

Figure 2-149 RK3568 PDM M1 functional pins

• PDM\_M2 is multiplexed in the VCCIO5 power domain.

M2 / GFIG2 D1 M2 / GFIG2 D2 / GFIG2 D3 / GFIG2 D3 / GFIG2 D5 / GFIG2 D5 / GFIG2 D5 / GFIG3 A0 / GFIG3 A1 / GFIG3 A3 / GFIG3 A3 / GFIG3 A5 / GFIG3 A5 / GFIG3 A5 / GFIG3 A5 / GFIG3 A6
/ GPIG2 D3 / GPIG2 D5 / GPIG2 D5 / GPIG2 D5 / GPIG2 D7 / GPIG3 A0 / GPIG3 A1 / GPIG3 A3 / GPIG3 A3 / GPIG3 A5 / GPIG3 A5 / GPIG3 A5
/ GPI02 D4 / GPI02 D5 / GPI02 D7 / GPI02 D7 / GPI03 A0 / GPI03 A1 / GPI03 A2 / GPI03 A4 / GPI03 A5 / GPI03 A5 / GPI03 A5
/ GFI02 D5 / GFI02 D6 / GFI02 D7 / GFI03 A0 / GFI03 A1 / GFI03 A2 / GFI03 A3 / GFI03 A5 / GFI03 A5 / GFI03 A5
/ GPI02 D6 / GPI03 D7 / GPI03 A0 / GPI03 A1 / GPI03 A2 / GPI03 A4 / GPI03 A5 / GPI03 A5 / GPI03 A5
/ GPI02 D7 / GPI03 A0 / GPI03 A1 / GPI03 A2 / GPI03 A3 / GPI03 A4 / GPI03 A5 / GPI03 A6
/ GPI03 A0 / GPI03 A1 / GPI03 A2 / GPI03 A3 / GPI03 A3 / GPI03 A5 / GPI03 A6 / GPI03 A6
/ GPI03 A1 / GPI03 A2 / GPI03 A3 / GPI03 A4 / GPI03 A5 / GPI03 A6 / GPI03 A6
/ GPI03 A2 / GPI03 A3 / GPI03 A4 / GPI03 A5 / GPI03 A6 / GPI03 A7
/ GPI03 A2 / GPI03 A3 / GPI03 A4 / GPI03 A5 / GPI03 A6 / GPI03 A7
/ GPI03 A3 / GPI03 A4 / GPI03 A5 / GPI03 A6 / GPI03 A7
/ GPIO3 A4 / GPIO3 A5 / GPIO3 A6 / GPIO3 A7
/ GPIO3 A5 / GPIO3 A6 / GPIO3 A7
/ GPIO3 A6 / GPIO3 A7
/ GPIO3 A7
/ GF103 R/
MI / GF105 D0
/ GPI03 B1
/ GPIO3 B2
/ GPIO3 B3
/ GPIO3 B4
/ GPIO3 B5
/ GPIO3 B6
/ GPI03 B7
/ GPIO3 CO
/ GPIO3 C1
/ GPI03 C2
M2 / GPIO3 C3
/ GPI03 C4
M2 / GPIO3 C5

BGA636\_19R00X19R00X1R20

Figure 2-150 RK3568 PDM M2 functional pins Copyright © 2022 Rockchip Electronics Co., Ltd.

In PDM interface design, please note:

- PDM\_M0, PDM\_M1 and PDM\_M2 cannot be used at the same time, and you can only choose one group of them each time. You cannot choose M0 for some signals, and M1 or M2 for the other signals, this function is not supported.
- The corresponding supply of power domain should be adjusted according to PDM peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- In order to improve PDM interface performance, the decoupling capacitors of VCCIOx power supply should not be deleted. Please place them near the pin when layout.
- The pull up/down and matching design recommendations of PDM interface are shown in the following Table.

Signal	Pull up/down inside	Connection mode	Description (chip end)
PDM_CLK0	Pull-down	Connect a 220hm resistor in series	PDM clock 0 output
PDM_CLK1	Pull-down	Connect a 220hm resistor in series	PDM clock 1 output
PDM_SDI[3:0]	Pull-down	Connect a 220hm resistor in series	PDM data input

### Table 2–39 RK3568 PDM interface design

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

### 2.3.11.5 SPDIF interface

RK3568 provides a SPDIF TX digital audio interface which supports up to 24bits resolution. SPDIF is the abbreviation of Sony/Philips Digital Interface Format. As for the transmission carrier, SPDIF is divided into coaxiality and optical fiber, which transmit the same signal depending on different carriers and have different interfaces and connection appearance. The communication rate of SPDIF is usually limited by the carrier, so it is necessary to consider the interface device specifications used in the hardware design. But the optical signal transmission needn't to consider the interface level and impedance problems, the interface is flexible and its anti-interference ability is stronger.

SPDIF interface pins multiplex in three different power domains, VCCIO4, VCCIO5 and VCCIO7.

- The corresponding supply of power domain should be adjusted according to SPDIF peripheral IO level and they should be matched. Meanwhile, you should also note that the drive voltage configuration of VCCIOx power domain of the software is consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it may damage IO.
- The pull up/down and matching design recommendations of optical fiber SPDIF interface are shown in the following Table.

	Table 2	2-40 RK3568 SPDIF interf	ace design
Signal	Pull up/down inside	Connection mode	Description (chip end)
SPDIF_TX	Pull-down	Connect a 220hm resistor in series	SPDIF signal output

When board to board connection is realized by connectors, it is recommended to connect in series with resistors of certain value (between 22ohm and 100ohm, as long as it can meet the SI test), as well as reserving TVS devices.

#### 2.3.11.6 Analog audio interface

If the codec function of RK809-5 is not used, Pin14, 15,16,17,19,40 of RK809-5 must be grounded, and Pin18, 36,37,38,35,39,41,34,32,43,42 can be floated, the pin circuits left must be reserved.

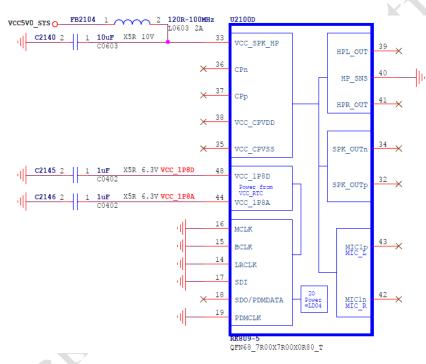


Figure 2-151 Process mode of related pins when RK809-5 Codec module is not used

When using RK809-5 power supply solution, the codec came with RK809-5 can achieve the headset output, 1.3W mono loudspeaker output and one-channel differential or two single-ended audio input functions.

RK3568 is connected to RK809-5 by I2S1 and PDM interfaces.

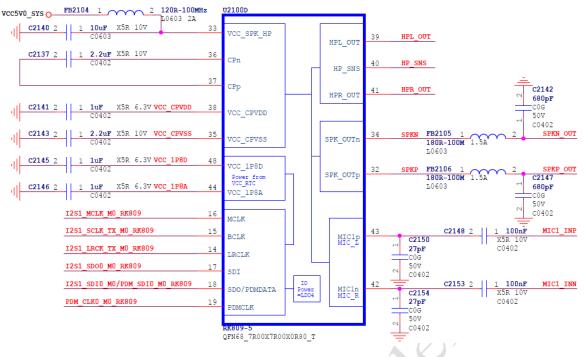
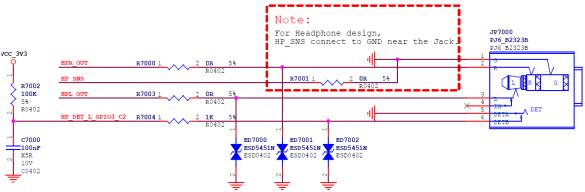


Figure 2-152 RK809-5 Codec module

- The IO level of I2S/PDM interface of RK809-5 is LDO4 output power supply of RK809-5, so I2S/PDM interface power domain level of RK3568 must match LDO4 output power supply voltage; Normally, LDO4 output of RK809-5 supplies power to I2S/PDM interface power domain of RK3568.
- HP\_SNS of RK809-5 Codec output is referenced as internal Offset, this pin needs to be connected to GND for reference externally. For the case HPOUT used as LINEOUT for connecting external power amplifier, HPSNS can be grounded near RK809-5. For the earphone output case, HPSNS shall be independently routed to the earphone connector and connected to GND to reduce the level difference between HPSNS and the earphone GND. During routing, it shall be accompanied routing in the middle of HPR/HPL to avoid interference from other signals. The trace is shown in the figure below.

In addition, ESD devices should be added to HPR\_OUT and HPL\_OUT to enhance anti ESD capability.



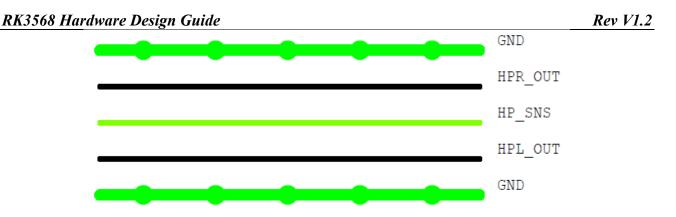


Figure 2-153 RK809 Codec output earphone circuit

- HP\_DET of the headset connects a 1K ohm resistor and a 100nF capacitor in series, you should reserve ESD devices to strengthen the ability of anti-static surge.
- RK809-5 Pin33 is not only a speaker power supply, but also an internal Charger pump power supply. The working voltage range is 2.7-5.5V. It is recommended that the LC circuit cannot be deleted, and it should be placed near RK809-5 when layout.

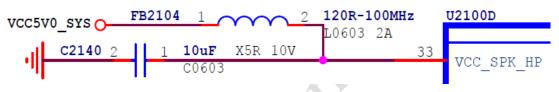


Figure 2-154 RK809-5 SPK/HP power supply pins

RK809-5 Codec built-in Mono filter-free speaker driver circuit, can provide 1.3W@80hm driving capacity. It is suitable for low power mono applications, and saves the cost of extra external power.
 Speaker output filter circuit is close to RK809-5, and ESD protection device is placed near the connector. Note the magnetic bead size in the following figure, the current is not less than 1.5A; if you need higher power or better output tone quality, it is recommended to expand the analog or digital power amplifier.

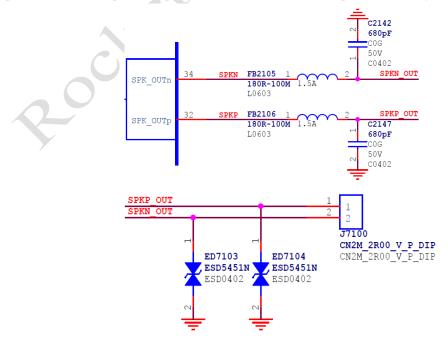


Figure 2-155 RK809-5 SPK output circuit

If RK809-5 built-in monophonic speaker drive circuit cannot meet the requirements of driving ability, or needs to achieve stereo function, you can attach independent analog/digital power amplifier.externally. When the analog power/Analog power amplifier is attached externally, HPOUT is used as LINEOUT for output; when the digital power/ power amplifier is attached externally, it can be connected to the I2S interface. You need to pay attention to the power supply design, when the power/ power supply is large, the supply mode should be noted.

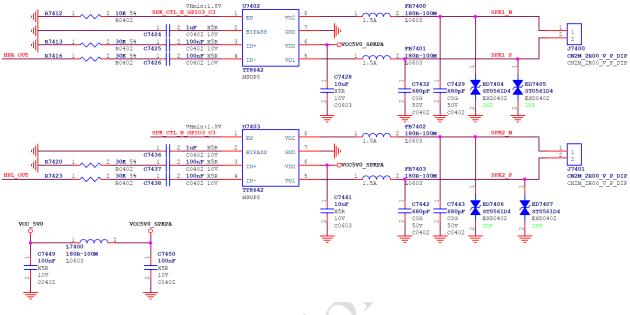


Figure 2-156 External SPK circuit

#### Single-MIC circuit

If using a three-segment headset, the local MIC can be configured as a differential input by using the analog ADC of RK809-5 (differential input provides better recording effect than single-ended input, and bias power supply requires a 68-1000hm resistor and a capacitor more than 1uF for RC filtering).

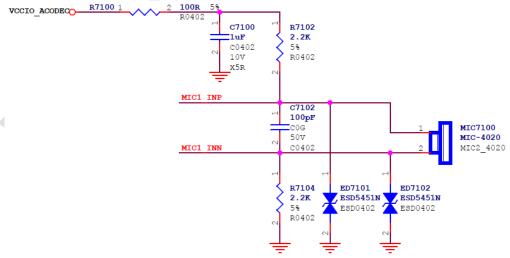
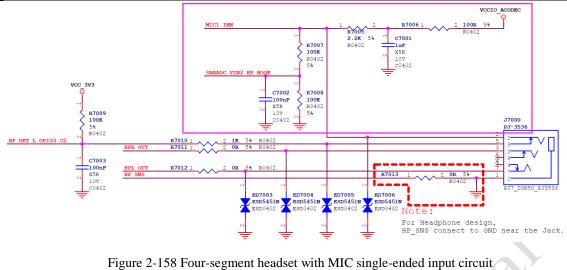


Figure 2-157 Electret MIC differential input circuit

If you use a four-segment headset + local MIC requirements, analog ADC configuration of RK809-5 is separated into two single-ended inputs.



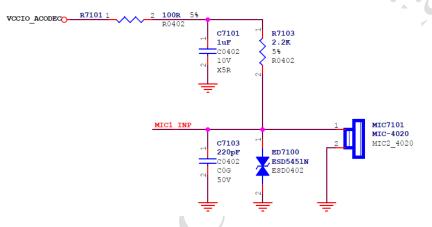


Figure 2-159 Electret MIC single-ended input circuit

Blocking capacitors of MIC shall not be deleted. And it should be placed close to RK809-5 when layout.

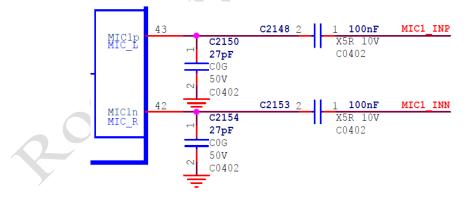


Figure 2-160 RK809-5 MIC input circuit pins

Array MIC circuit solution

In the reference design of RK3568, multi-scene audio input/output solutions and multi-microphone solutions are provided.

Briefly introduce as follows:

When the ADC integrated by RK809-5 can meet the input requirements, the ADC of RK809-5 is inputted firstly; When you need to use far-field sound pickup and recovery, it is not recommended to use single-ended ADC to connect, and the differential signals input is used by default. If the input interfaces are not enough,

you need to expand the ADC. By default, audio ADC of PDM interface is used in the current solution, and audio ADC of I2S interface can also be used.

	Application cases	Corresponding pages of circuit diagram
1	Three-segment headset	70.Audio-Headphone Port—Default circuit
L	+ Differential microphone	71.Audio-SingleMic+RK809_SPK—Default circuit
	+ Mono speaker output	71.Audio-SingleMic+RK809_SPK—SPK circuit
2	Four-segment headset	70.Audio-Headphone Port—Option circuit
2	+ Single-ended microphone	71.Audio-SingleMic+RK809_SPK— <b>Option circuit</b>
	+ Mono speaker output	71.Audio-SingleMic+RK809_SPK—SPK circuit
3	Three-segment headset	70.Audio-Headphone Port—Default circuit
3	+ Differential microphone	71.Audio-SingleMic+RK809_SPK—Default circuit
	+ Mono speaker output	72.Audio-MicArray+RK809_SPKRK809-5 SPK circuit
	+ Mono channel audio	72.Audio-MicArray+RK809 SPKOption1 circuit
	differential recovery	/2.Audio-MicAnay+KK809_SFKOption1 circuit
4	Three-segment headset	70.Audio-Headphone Port—Default circuit
4	+Two or four array mic	72.Audio-MicArray+RK809_SPK—MicArray circuit
	+ Mono speaker output	72.Audio-MicArray+RK809_SPKRK809-5 SPK circuit
	+ Mono channel audio	72.Audio-MicArray+RK809_SPKOption1 circuit
	differential recovery	(recommended)
		Or 72.Audio-MicArray+RK809_SPK— <b>Option2 circuit</b>
5	Four-segment headset	70.Audio-Headphone Port—Option circuit
5	+Two or four array mic	72.Audio-MicArray+RK809_SPK—MicArray circuit
	+ Mono speaker output	72.Audio-MicArray+RK809_SPKRK809-5 SPK circuit
	+ Mono channel audio	72.Audio-MicArray+RK809 SPKOption1 circuit
	differential recovery	72.Audio-MicAnay+RR809_51ROption1 circuit
6	Three or four-segment headset	70.Audio-Headphone Port—Default circuit or Option circuit
U	+Two or four array mic	74.Audio-MicArray+EXT Dual_SPK—MicArray circuit
	+ Stereo speaker output	74.Audio-MicArray+EXT Dual_SPKSpeaker Output circuit
	+Stereo differential recovery	74.Audio-MicArray+EXT Dual_SPK—Loopback circuit

Table 2–41 RK3568 matching relationship	hatwaan audia	annlightigns on	d the aircruit diagram
Table 2–41 KK5500 matching relationshi	b between audio	applications an	

Application case 4 I2S/PDM connection schematic diagram 1:

Speaker recovery of RK809-5 uses PDM\_CLK0+PDM\_D0 channel or PDM\_CLK1+PDM\_D3 (recommended),

Array microphone uses PDM\_CLK1+PDM\_D1/2 channel.

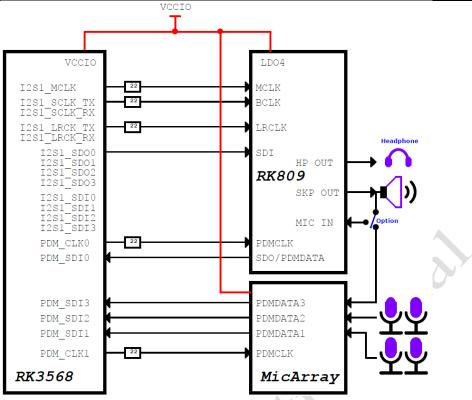


Figure 2-161 Array MIC solution I2S/PDM connection diagram 1

 Application case 6 I2S/PDM connection schematic diagram 2: Stereo speaker recovery uses PDM\_CLK1+PDM\_D3. Array microphone uses PDM\_CLK1+PDM\_D1/2 channel.

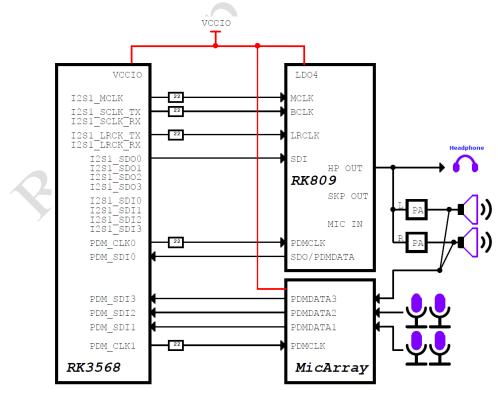


Figure 2-162 Array MIC solution I2S/PDM connection diagram 2

### *RK3568 Hardware Design Guide* 2.3.12 GMAC Interface Circuit

RK3568 has two GMAC controllers, which can provide RMII or RGMII interface to connect external Ethernet PHY, or can also connect external Ethernet PHY through QSGMII/SGMII PCS, QSGMII/SGMII interface, as described in 2.3.6 QSGMII/SGMII circuit.

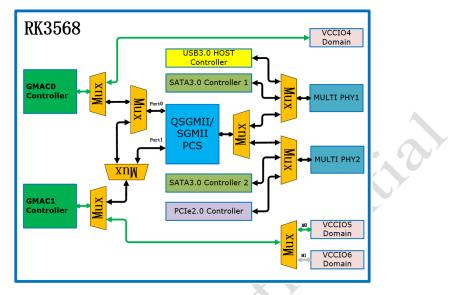


Figure 2-163 Path block diagram of RK3568 GMAC0, GMAC1 reused with IO

GMAC controller supports the following features:

- Support RGMII interface of 10/100/1000 Mbps data transmission rate
- Support RMII interface of 10/100 Mbps data transmission rate
- RGMII/RMII interface of GMAC0 is reused with VCCIO4 power domain

SDMMC1 D0	/ GMAC0 RXD2	/ UART6 RX M0		/ GPIO2 A3
SDMMC1 D1	/ GMAC0 RXD3	7 UART6 TX M0		/ GPIO2 A4
SDMMC1 D2	/ GMAC0 RXCLK	7 UART7 RX M0		/ GPIO2 A5
SDMMC1 D3	/ GMAC0 TXD2	/ UART7 TX M0		/ GPIO2 A6
SDMMC1 CMD	/ GMAC0 TXD3	/ UART9 RX MO		/ GPIO2 A7
SDMMC1 CLK	/ GMAC0 TXCLK	/ UART9 TX M0		/ GPIO2 B0
SDMMC1 PWREN	/ 12C4 SDA M1	/ UART8 RTSn M0	/ CAN2 RX M1	/ GPIO2 B1
SDMMC1 DET	/ 12C4 SCL M1	/ UART8 CTSn M0	/ CAN2 TX M1	/ GPIO2 B2
	CMA CO. (777.00)			/
	GMAC0 TXD0 GMAC0 TXD1	/ UART1 RX M0 / UART1 TX M0		/ GPIO2 B3
	GMACO TXDI GMACO TXEN	/ UART1 TX MU / UART1 RTSn M0	/ SPI1 CLK M0	/ GPIO2 B4
	GMACO TAEN GMACO RXDO	/ UART1 CTSn M0	/ SPII CLK MO	/ GPIO2 B5 / GPIO2 B6
	GIACO IGDO	/ UNICIT_CIDIT_HO	/ 5111_M150_M0	7 GP102 B0
12S2 SCLK RX M0	GMAC0 RXD1	/ UART6 RTSn M0	/ SPI1 MOSI M0	/ GPIO2 B7
12S2 LRCK RX M0	/ GMACO RXDV CRS	/ UART6 CTSn M0	/ SPI1 CS0 M0	/ GPIO2 CO
12S2 MCLK M0	/ ETHO_REFCLKO_25M	/ UART7_RTSn_M0	/ SPI2_CLK_M0	/ GPIO2 C1
12S2 SCLK TX M0	/ GMAC0 MCLKINOUT	/ UART7 CTSn M0	/ SPI2 MISO MO	/ GPIO2 C2
12S2 LRCK TX M0	/ GMAC0 MDC	/ UART9 RTSn M0	/ SPI2 MOSI MO	/ GPI02 C2
12S2 SD0 M0	/ GMAC0 MDIO	/ UART9 CTSn M0	/ SPI2 CS0 M0	/ GPI02 C4
I2S2_SDI_M0	/ GMACO_RXER	/ UART8 TX MO	/ SPI2_CS1_M0	/ GPIO2 C5
		/	/	/
CLK32K OUT1		/ UART8 RX M0	/ SPI1 CS1 M0	/ GPIO2 C6

BGA636\_19R00X19R00X1R20

• RGMII/RMII interface of GMAC0 is reused with VCCIO5 power domain or VCCIO6 power domain, using suffix \_M0/\_M1/ to distinguish different multiplexing positions. \_M0/\_M1/ cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for some others.

M0 reused with VCCIO5 power domain

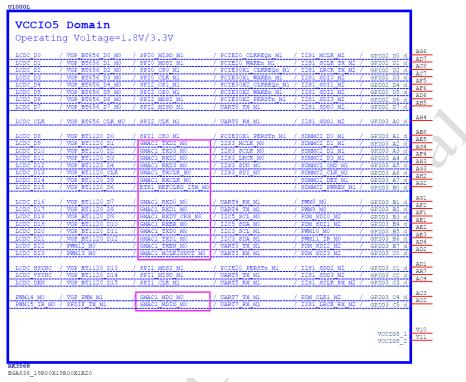
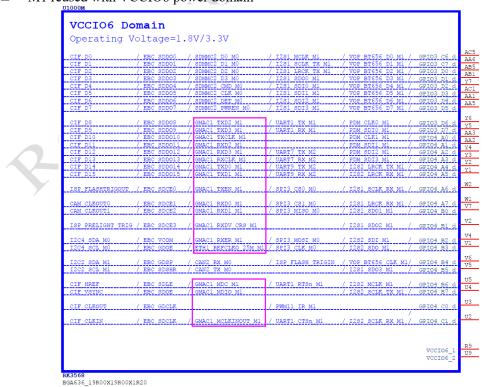


Figure 2-165 RK3568 GMAC1 M0 functional pins



M1 reused with VCCIO6 power domain

Figure 2-166 RK3568 GMAC1 M1 functional pins

Notices in the design of RGMII/RMII interface:

- The power of RGMII/RMII interface is supplied by VCCIOx. During actual product design, need to select the corresponding power supply according to the actual IO power supply requirement (1.8V or 3.3V) of the peripherals, which must be matched. Besides, have to make sure the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- Recommend to use 1.8V for RGMII/RMII if possible to get better signal quality.
- In order to improve RGMII/RMII interface performance, the decoupling capacitor of VCCIOx power domain cannot be deleted and it should be placed close to the pin.
- ETH0\_REFCLKO\_25M requires to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- ETH1\_REFCLKO\_25M requires to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- TXD0-TXD3,TXCLK,TXEN require to series connect 22 ohm resistor at RK3568 end to improve the signal quality.
- RXD0-RXD3,RXCLK,RXDV require to series connect 22 ohm resistor at PHY end to improve the signal quality.

	RGMII/RMII interface pull-up/down and matching design are recommended in the Table below.	
--	---	--

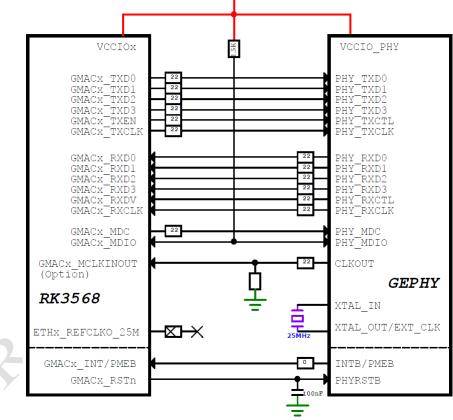
Signal	IO type(chipse t end)	Connection mode	RGMII interface	Signal description	RMII interface	Signal description
GMACx_TX D[3:0]	Output	Series connect 220hm resistor close to RK3568	RGMIIx_TXD[3:0]	Data sending	RMIIx_TXD[1:0]	Data sending
GMACx_TX CLK	Output	Series connect 220hm resistor close to RK3568	RGMIIx_TXCLK	Reference clock for data sending		
GMACx_TX EN	Output	Series connect 220hm resistor close to RK3568	RGMIIx_TXEN	Data sending enabled(rising edge) and data sending error (falling edge)	RMIIx_TXEN	The signal used for data sending
GMACx_RX D[3:0]	Input	Series connect 220hm resistor close to PHY end	RGMIIx_RXD[3:0]	Data receiving	RMIIx_RXD[1:0]	Data receiving
GMACx_RX CLK	Input	Seriesconnect22ohmresistorclose to PHY end	RGMIIx_RXCLK	Reference clock for data receiving		
GMACx_RX DV	Input	Series connect 220hm resistor close to PHY end	RGMIIx_RXDV	Data receiving valid (rising edge) and receiving error (falling edge)	RMIIx_RXDV_C RS	Data receiving valid and carrier sensing
GMACx_RX ER	Input	Series connect 220hm resistor close to PHY end			RMIIx_RXER	Error hint for data receiving
GMACx_MC LKINOUT	Input/ Output	Output mode:Seriesconnect22ohmresistorclose to RK3568Input mode:Seriesconnect22ohmresistorclose to PHY end	RGMIIx_MCLKIN _125M	PHY is sending 125MHz to MAC, optional	RMII_MCLKIN_ 50M or RMII_MCLKOU T_50M	Reference clock of RMII data sending and data receiving

Table 2-42 RK3568 RGMII/RMII interface design

Signal	IO type(chipse t end)	Connection mode	RGMII interface	Signal description	RMII interface	Signal description
ETHx_REFC LKO_25M	Output	Series connect 220hm resistor close to RK3568	ETHx_REFCLKO_ 25M	25MHz clock provided by RK3568 to replace PHY crystal	ETHx_REFCLK O_25M	25MHz clock provided by RK3568 to replace PHY crystal
GMACx_MD C	Output	Series connect 220hm resistor close to RK3568	RGMIIx_MDC	Manage data clock	RMIIx_MDC	Manage data clock
GMACx_MD IO	Input/Outpu t	Series connect 220hm resistor, external pull-up 1.5K-1.8Kohm resistor	RGMIIx_MDIO	Manage data output/input	RMIIx_MDIO	Manage data output/input

■ When board-to-board connection is realized by connector, recommend to series connect resistor with a certain value (220hm-1000hm, as long as it can meet the SI test), and reserved TVS component

RGMII connection example 1, please refer to the reference design for the details (GEPHY uses external 25MHz crystal as working clock).



VCCIO

Figure 2-167 RGMII connection example 1

RGMII connection example 2, please refer to the reference design for details (GEPHY uses the 25MHz provided by RK3568 as working clock).

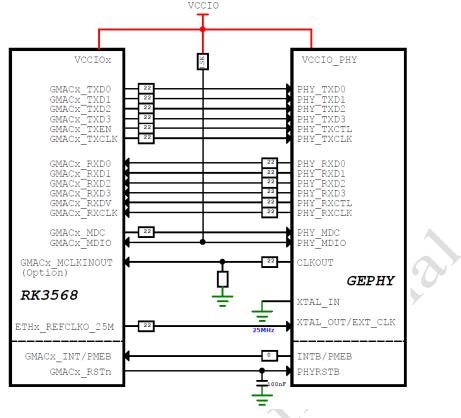


Figure 2-168 RGMII connection example 2

RMII connection example 1, please refer to the reference design for details (GMACx\_MCLKINOUT adopts output mode, that is, used as both FEPHY working clock and reference clock of RMII interface. Some FEPHY doesn't support this mode).

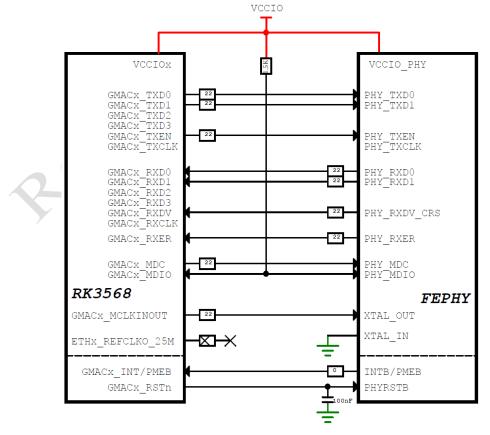


Figure 2-169 RMII connection example 1

RMII connection example 2, please refer to the reference design for details (25MHz crystal is used as FEPHYworking clock, GMACx\_MCLKINOUT adopts output mode which is used as the reference clock of RMII interface).

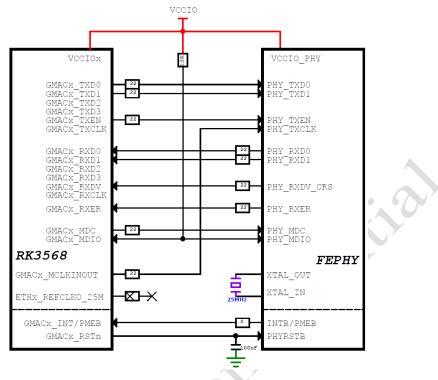


Figure 2-170 RMII connection example 2

RMII connection example 3, please refer to the reference design for details (using 25MHz provided by RK3568 to replace FEPHY crystal, GMACx\_MCLKINOUT adopts output mode which is used as the reference clock of RMII interface).

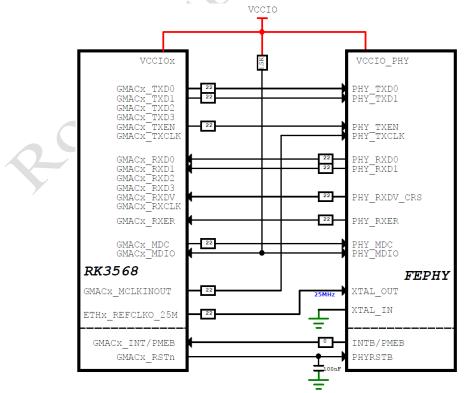


Figure 2-171 RMII connection example 3

RMII connection example 4, please refer to the reference design for details (FEPHY uses external 25MHz crystal as working clock, GMACx\_MCLKINOUT adopts input mode, and the reference clock of RMII interface is provided by FEPHY).

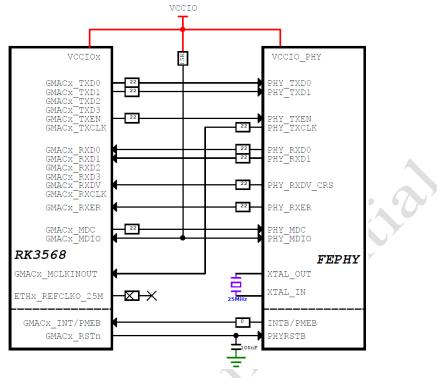


Figure 2-172 RMII connection example 4

RMII connection example 5, please refer to the reference design for details (using 25MHz provided by RK3568 to replace FEPHY crystal, GMACx\_MCLKINOUT adopts input mode and the reference clock of RMII interface is provided by FEPHY).

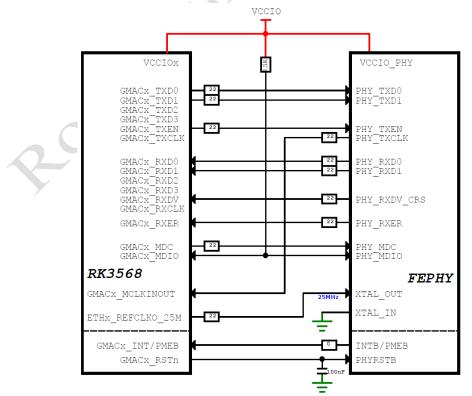


Figure 2-173 RMII connection example 5

- Reset signal of Ethernet PHY should be controlled by GPIO, and GPIO level must match with PHY IO level. 100nF capacitor should be added close to PHY pin to enhance anti-static ability. Note: RTL8211F/FI reset pin only supports 3.3V level.
- INTB/PMEB of RTL8211F/FI is open drain output. Must add external pull-up resistor. The reference design uses internal pull-up resistor of RK3568 IO by default.
- When PHY uses external crystal, please select the crystal capacitance according to the load capacitance value of the actually used crystal, and the frequency deviation should be controlled within +/-20ppm.
- The resistor externally connected to RSET pin of RTL8211F/FI is 2.49KΩ/1%, which cannot be modified at will.
- MDIO must add external pull-up resistor, with recommended value 1.5-1.8Kohm, and the pull-up power must be consistent with the power.
- The transformer central tap of RTL8211F/FI must be connected according to the reference design. If using other Ethernet PHY, the connection of the transformer central tap should follow the reference design of each Ethernet PHY vendor, because different PHY vendors have different connection methods.
- 1000pF isolation capacitor is recommended to use high-voltage safety capacitor, which has enough electrical clearance to ensure the security of lightning strike.
- The 75 ohm resistor at the high voltage side of the network transformer is recommended to use the package bigger than 0805.
- When the lightning protection level reaches 4KV or above, the lightning protection tube should be added, as ordinary isolation transformer can only meet 2KV grade requirement.
- If there is lightning differential test requirement, need to add TVS tube between MDI differential pair.
- Must confirm whether RJ45 package is consistent with the schematic or not. RJ45 has Tab down and Tab up two type, which signal sequence are just opposite. If using RTL8211F/FI, recommend to use Tab down, MDI sequence is in order.
- The initial hardware configuration of PHY must match with the actual requirement.

# 2.3.13 UART Interface Circuit

RK3568 has 10 UART controllers, which support the following functions:

- All include two 64-byte FIFO used for data receiving and sending.
- Support 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, and 4Mbps.
- Support programmable baud rate, support non-integer clock divider.
- Support interrupt or DMA based mode.
- Support 5-8bit width transmission.

Considering the application flexibility of different products, 10 UARTs are separately reused with several different power domains, using suffix \_M0/\_M1/\_M2 to identify different multiplexing locations. \_M0/\_M1/\_M2 cannot be used at the same time. You can only select one group of them. It doesn't support to select M0 for some signals, while selecting M1 or M2 for other signals.

■ RK3568 UART interface distribution.

UART No.	Reuse status	Reused power domain
UART0	None	PMUIO2
UART1	N40 N41	M0:VCCIO4
UARTI	M0,M1	M1:VCCIO6
UART2	M0,M1	M0:PMUIO2
UAR12	1110,111	M1:VCCIO3
UART3	M0,M1	M0:VCCIO1
UARIS	1110,111	M1:VCCIO5
UART4	M0,M1	M0:VCCIO1
UARI4	1410,1411	M1:VCCIO5
UART5	M0,M1	M0:VCCIO3
UARIS	1410,1411	M1:VCCI05
UART6	M0,M1	M0:VCCIO4
UARIO	1410,1411	M1:VCCIO3
		M0:VCCIO4
UART7	M0,M1,M2	M1:VCCIO5
		M2:VCCIO6
UART8	M0,M1,M2	M0:VCCIO4
0/11(10	1110,1111,1112	M1:VCCIO5
		M0:VCCIO4
UART9	M0,M1,M2	M1:VCCIO7
		M2:VCCIO6

- UART2 MO is Debug UART of RK3568 by default. Please refer to 2.1.6 JTAG and UART Debug circuit for notices.
- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of UART peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- UART interface pull-up/down and matching design are recommended as in the Table below.

Signal	Connection mode	Description (chipset end)
UARTx_RX	Direct connection	UART data input
UARTx_TX	Direct connection	UART data output
UARTx_CTSn	Direct connection	UART allowing to send signal
UARTx_RTSn	Direct connection	UART requesting to send signal

Table 2-44 RK3568 UART interface design

When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (220hm-1000hm, as long as it can meet the SI test), and reserve TVS component.

Besides above FSPI controllers, RK3568 lso has 4 generic SPI controllers, which support the following functions:

- Support master and slave two modes.
- Support 4, 8, 16bit serial data transmission.
- Support full duplex and half duplex mode transmission.

Considering the application flexibility of different products, 4 SPIs are separately reused with different power domains, using suffix \_M0/\_M1/ to identify different multiplexing locations. \_M0/\_M1/ cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

- RK3568 SPI interface distribution.
  - Table 2–45 RK3568 SPI interface distribution

SPI no.	Reused status	Reused power domain	
SPI0	M0 M1	M0:PMUIO2	
5810	M0,M1	M1:VCCIO5	
SPI1	MONT		M0:VCCIO4
511	M0,M1	M1:VCCIO5	
SDIC	M0,M1	SPI2 M0,M1	M0:VCCIO4
5F12			M1:VCCIO5
SPI3		M0:VCCIO6	
515	M0,M1	M1:VCCIO7	

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of SPI peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- SPI interface pull-up/down and matching design are recommended as in the Table below.

	-	
Signal	Connection mode	Description (chipset end)
SPIx CLK	Series connect 220hm resistor	SPI clock
SPIX_CLK	Series connect 220mm resistor	SPI clock
SPIx_MOSI	Direct connection	SPI data output(Master)
SPIx_MISO	Direct connection	SPI data input(Master)
SPIx_CS0	Direct connection	SPI chip selection 0
SPIx CS1	Direct connection	SPI chip selection 1

Table 2-46 RK3568 SPI interface design	n
--	---

When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (220hm-1000hm, as long as it can meet the SI test), and reserve TVS component.

### 2.3.15 CAN Interface Circuit

RK3568 has 3 CAN controllers, which support the following functions:

■ Support CAN 2.0B protocol.

■ Support 1Mbps, 8Mbps.

Considering the application flexibility of different products, 3 CANs are separately reused with different power domains, using suffix \_M0/\_M1 to identify different multiplexing locations. \_M0/\_M1 cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

■ RK3568 CAN interface distribution.

CAN no.	Reused status	Reused power domain
CAN0	M0,M1	M0:PMUIO2
CANO	1110,1111	M1:VCCIO3
CANI	M0 M1	M0:VCCIO1
CAN1	M0,M1	M1:VCCIO7
CAND	M0 M1	M0:VCCIO6
CAN2	M0,M1	M1:VCCIO4

Table	2 - 47	<b>RK3568</b>	CAN	interface	distribution
1 aoic	<u>~</u> +/	1113500		mornace	unsunoution

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of CAN peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- CAN interface pull-up/down and matching design are recommended as in the Table below.

Signal Connection mode		Description (chipset end)
CANx_RX	Direct connection	CAN data input
CANx_TX	Direct connection	CAN data output

Table 2–48 RK3568 CAN interface design

■ When using a connector to realize board-to-board connector, recommend to series connect resistor with certain value (220hm-1000hm, as long as it can meet the SI test), and reserve TVS component.

# 2.3.16 I2C Interface Circuit

RK3568 has 6 I2C controllers, which support the following functions:

- Support I2C bus main mode.
- Support software programmable clock and the transmission speed is up to 400Kbit/sec.
- Support 7bit and 10bit addressing mode.

Considering the application flexibility of different products, 6 I2Cs are separately reused with different power domains, using suffix \_M0/\_M1 to identify different multiplexing locations. \_M0/\_M1 cannot be used at the same time. You can only select one group of them while allocating. It doesn't support to select M0 for some signals while selecting M1 for other signals.

■ RK3568 I2C interface distribution.

I2C No.	Reuse status	Reused power domain
I2C0	None	PMUIO2
I2C1	None	PMUIO2
1202	M0 M1	M0:PMUIO2
I2C2	M0,M1	M1:VCCIO6
1202	N0 M1	M0:VCCIO1
I2C3	M0,M1	M1:VCCIO5
1204	N0 M1	M0:VCCIO6
I2C4	M0,M1	M1:VCCIO4
1205	N0 M1	M0:VCCIO5
I2C5	M0,M1	M1:VCCI07

Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of I2C peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.

- I2C0 is allocated to PMIC by default, which is convenient for software. Recommend not to change.
- I2C signal SCL, SDA require to connect external pull-up resistor. Select the resistors with different values according to different load of bus. Recommend to connect 2.2kΩ pull-up resistor.
- The addresses of the devices on I2C bus should not conflict. The pull-up power must be consistent with the power supply.
- I2C interface pull-up/down and matching design are recommended as in the Table below.

Signal	Connection mode	Description (chipset end)			
I2Cx_SCL	Direct connection	I2C clock			
I2Cx_SDA	Direct connection	I2C data output/input			

Table 2-50 RK3568 I2C interface design

When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (220hm-1000hm, as long as it can meet the SI test), and reserve TVS component.

# 2.3.17 PWM Interface Circuit

RK3568 has 4 independent PWM controllers, each controller has 4 channels, have up to 16 PWM channels at most, and support the following functions:

- Support capture mode.
- Support continuous mode or one-time mode.
- Optimized infrared application of PWM3, PWM7, PWM11 and PWM15.

Considering the application flexibility of different products, 16 PWMs are separately reused with different

power domains, using suffix M0/M1 to identify different multiplexing locations.

RK3568 PWM interface distribution.

Table 2–51 RK3568 PWM interface distribution							
PWM No.	Reused status	Reused power domain					
DWAMO	M0 M1	M0:PMUIO2					
PWM0	M0,M1	M1:PMUIO2					
DW/M1	M0 M1	M0:PMUIO2					
PWM1	M0,M1	M1:PMUIO2					
PWM2	M0 M1	M0:PMUIO2					
P W W12	M0,M1	M1:PMUIO2					
PWM3_IR	None	PMUIO2					
PWM4	None	PMUIO2					
PWM5	None	PMUIO2					
PWM6	None	PMUIO2					
PWM7_IR	None	PMUIO2					
PWM8	M0,M1	M0:VCCI05					
P W 1018	1910,1911	M1:VCCIO3					
PWM9	M0,M1	M0:VCCIO5					
1 WW	1910,1911	M1:VCCIO3					
PWM10	M0,M1	M0:VCCIO5					
1 WW10	1910,1911	M1:VCCIO3					
PWM11_IR	M0,M1	M0:VCCIO5					
	1910,1911	M1:VCCIO6					
PWM12	M0,M1	M0:VCCIO5					
1 WWW12	1910,1911	M1:VCCIO7					
PWM13	M0,M1	M0:VCCIO5					
1 WW115		M1:VCCIO7					
PWM14	M0,M1	M0:VCCIO5					
	1410,1411	M1:VCCIO7					
PWM15_IR	M0,M1	M0:VCCIO5					
	1410,1411	M1:VCCIO7					

- Adjust the power supply of the corresponding power domain to keep it consistent with the IO level of PWM peripheral. Besides, need to notice that the driver voltage configuration of VCCIOx power domain in software must be consistent with the power supply voltage of VCCIOx power domain, otherwise the function will be abnormal and it will probably damage IO.
- When using a connector to realize board-to-board connection, recommend to series connect resistor with certain value (220hm-1000hm, as long as it can meet the SI test), and reserve TVS component.
- When an IR receiver is used as input, pay attention to the following items:
- If IR receiver is required to support suspend/resume and low power consumption (that is, the VDD\_LOGIC power supply shutdown solution), it is recommended to use PWM3 as the input of IR receiver,

- The power supply of infrared receiver should use VCC3V3\_PMU power supply;
- The power supply of IR receiver requires 22-100ohm resistor and capacitor more than 10nF to do RC filtering.
- IR receiver uses 38KHz by default, and software requires fine tune accordingly if changed to other frequency.
- The output pin level of IR receiver must match with RK3568 IO level.
- The output pin of the infrared receiver is recommended to be connected to a 22 ohm resistor in series and a 1nF capacitor to the ground, and then connected to RK3568 to strengthen the anti-static surge capability.

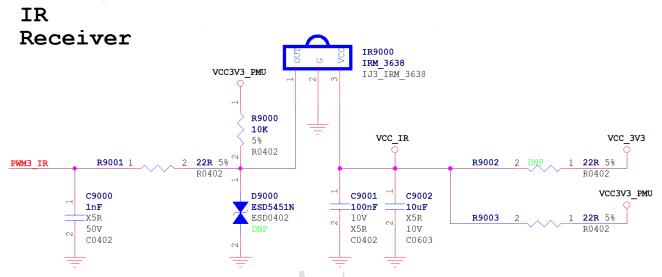


Figure 2-174 IR receiver circuit

- IR receiver layout should be far away from the wireless module antenna, such as WIFI antenna, to avoid the influence of wireless data transmission on the infrared signal receiving.
- IR receiver layout should avoid direct LED light source on the board to avoid the influence of LED flicker frequency on the infrared receiving.
- The whole process of IR signal is recommended to be surrounded by GND. If unable to be grounded, recommend to keep from other signals with the distance >=2 times of linewidth.

### 2.3.18 RK3568 Unused Modules Pins Processing

Please refer to the document of "RK3568\_Methods for Processing Unused Pins\_V10\_20201218\_CN.xlsx".

# **3 PCB Design recommendations**

## **3.1 PCB Layers Design**

In order to reduce the reflection phenomenon in the process of high-speed signal transmission, impedance matching must be maintained on the signal source, the receiving end and the transmission line. The impedance of a single-ended signal line depends on its line width and its relative position to the reference layer. The line width/line spacing between the differential pairs required for a specific impedance depends on the selected PCB stackup. Since the minimum line width and minimum line distance depend on the PCB type and cost requirements, due to this limitation, the selected PCB stackup must be able to achieve all impedance requirements on the board, including inner and outer layers, single-ended and differential lines, etc.

Layer design rules:

- The layers neighboring to the chip is a ground layer, which provides a reference layer for device layer for routing;
- All signal layers are as close as possible to the ground layer
- Try to avoid two signal layers neighboring directly
- The main power supply is as close to the related ground as possible
- A symmetrical structure design should be adopted in principle. The meaning of symmetry includes: the thickness and type of the media layer, the thickness of the copper foil, and the symmetry of the graphic distribution type (large copper foil layer, circuit layer)

PCB multilayer recommended solution: When designing a specific PCB layers, the above rules should be used flexibly, and the layer arrangement should be determined according to actual requirements instead of applying mechanically. The recommended solutions for frequently used layer arrangements are given below for reference only. In layers setting, if there are neighboring layers for routing, the interlayer crosstalk can be reduced by increasing the distance between neighboring layers. For the case of cross-segmentation, ensure that the key signal must have a relatively complete reference ground plane or provide necessary bridging measures.

6-layer PCB design is recommended for RK3568. The following multilayer structure is an example to help customers in the selection and evaluation of multilayer structure. If you choose another type of multilayer structure, please recalculate the impedance according to the specifications given by PCB manufacturers.

### 3.1.1 Six Layers PCB Design

In the 6-layer PCB design, the reference layer of the top-level signal L1 is L2, and the reference layer of the bottom-level signal L6 is L5. L3 and L5 are also used as reference layer for L4 high-speed signal routing, depending on layers conditions. It is recommended that the layer sequence is `refers to L5, and 1oZ is recommended. The following figure shows the 1.6mm thickness reference layer design. Please adjust Core thickness according to board thickness requirements.

Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M				18	0.71	+/-10	3.8
1	TOP	1		35	1.38	+/-10	
			PP 1080X1(RC64%)	80	3.15	+/-10	4.2
2	GND	1		30	1.18	+/-10	
			PP 2116X1(RC50%)	102	4.02	+/-10	4.2
3	POWER	1		30	1.18	+/-10	
			Core	1008	39.69	+/-10	4.2
4	SIGNAL	1		30	1.18	+/-10	
			PP 2116X1(RC50%)	102	4.02	+/-10	4.2
5	GND	1		30	1.18	+/-10	
			PP 1080X1(RC64%)	80	3.15	+/-10	4.2
6	BOTTOM	1		35	1.38	+/-10	
S/M				18	0.71	+/-10	3.8
			总计:	1598	62.91		

Figure 3-1 Six layers PCB design

## 3.1.2 Four Layers PCB Design

In 4-layer PCB design, the reference layer of the top signal L1 is L2, and the reference layer of the bottom signal L4 is L3. It depends on the layers conditions, and 1oZ is recommended. The following figure shows the reference layer of 1.6mm thickness. Please adjust Core thickness according to board thickness requirements.

Layer No.	sig/pln	Copper thk. before process (oz)	Construction				Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)	
S/M								18	0.71	+/-10	3.8
1	TOP	1						30	1.18	+/-10	
				PP 1080X	(1(RC68%)			80	3.15	+/-14	4.2
2	GND	1						30	1.18	+/-10	
				Co	ore			1265	49.80	+/-30	4.2
3	POWER	1						30	1.18	+/-10	
				PP 1080X	(1(RC68%)			82	3.23	+/-14	4.2
4	BOTTOM	1						30	1.18	+/-10	
S/M								18	0.71	+/-10	3.8
							总计:	1583	62.32		

### Figure 3-2 Four layers PCB design

### 3.1.3 RK3568 Fan-out Design

• Ball fan-out design of the outer two circles

For the outermost balls, you can go out from the TOP layer with a line width of 4mil; the signal of the second circle goes out from the middle of the two balls with a line width of 4mil. It is recommended to set a grid and go out from the middle of the two balls.

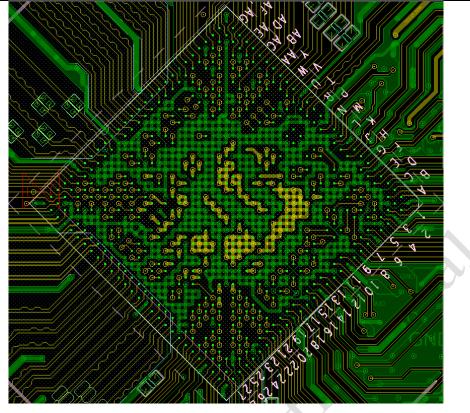


Figure 3-3 RK3568 Fan-out diagram 1

• Ball fan-out design in inner circles

If the signals of the first and second circles are useful, then starts from the third circle, if it needs to change to inner layers. Please make sure to follow the rules of layer changing vias, and it is recommended to place layer changing via at intervals of 2-4 rows, and leave an empty row not placing layer changing vias to keep as large a channel as possible for the ground layer and the power layer.

The ground layer copper covering situation shown in the figure below, there are multiple channels connected with the outside ground, which is good for SI/PI and heat dissipation

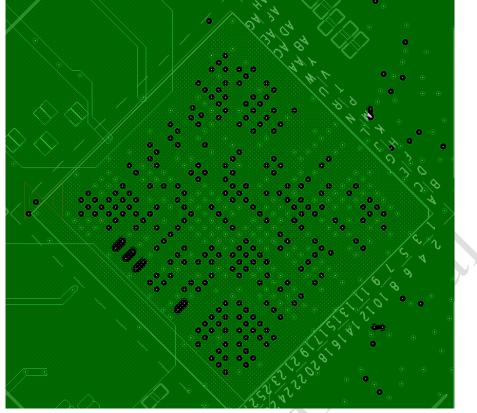


Figure 3-4 RK3568 Fan-out diagram 2

From the power layer copper covering situation shown in the figure below, we can see that, the regular placement of vias make various power sources having as much copper covering channels as possible, and improving the quality of power supply effectively.

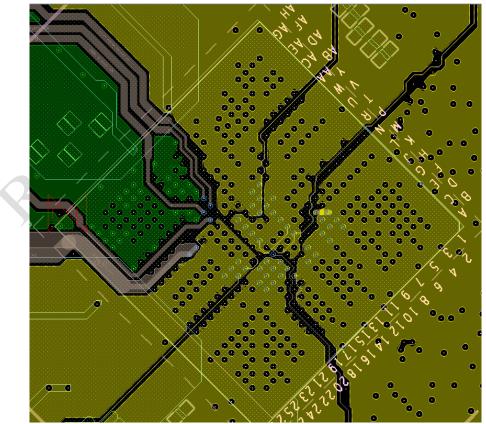


Figure 3-5 RK3568 Fan-out diagram 3

The trace of bottom layer (the trace of inner layer is similar) is shown in the figure below, the layer-changing vias are set according to the grid and placed in the middle of balls, and 3.5mil line width fanned out between two vias.

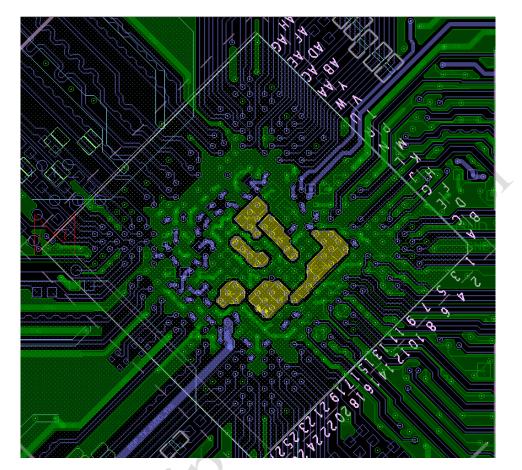


Figure 3-6 RK3568 Fan-out diagram 4

# **3.2 Interface PCB Design Recommendations**

For high-speed PCB design constraints, please refer to the introduction and the constraints of the general rules for high-speed PCB design in the "Rockchip\_RK3568\_High\_Speed\_PCB\_Design\_Guide" document

- The length of the trace controlling should include the length of package and the length of via
- Below is a diagram of space between signals

		(	
Spacing betv	veen signals		

Figure 3-7 A diagram of space between signals

Below is a diagram of equal length within and between differential pairs

Inter-Pair Skew
⊒

Figure 3-8 A diagram of equal length within and between differential pairs

When doing equal length inner the differential pair, normally, serpentine line is used to compensate for length differences. In order to reduce the impedance disconnection, the requirements for the serpentine line are as shown in the figure below. In addition, pay attention to that the serpentine line for compensation should be as close as possible to the change point when doing length compensation

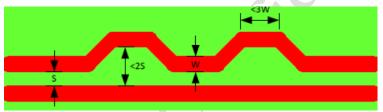


Figure 3-9 A diagram of differential pair length compensation requirements

When the signal reference plane changes, it should refer to the ground plane too, and the stitching vias should be close to the signal vias; for differential signals, it is recommended that the distance between the stitching vias and the signal vias should be less than 30mil

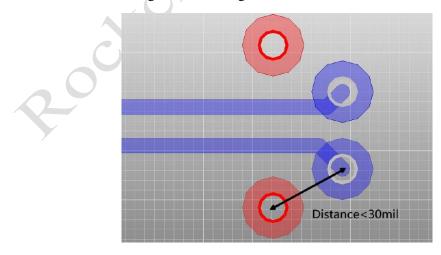


Figure 3-10 Stitching vias requirement diagram

Try to avoid routing high-speed signals on the edge of the reference plane, otherwise it will affect impedance. It is recommended that the distance from high-speed signal to the edge of the reference plane is greater than or equal to 40mil

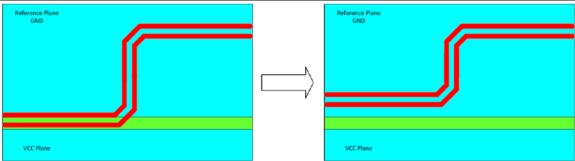
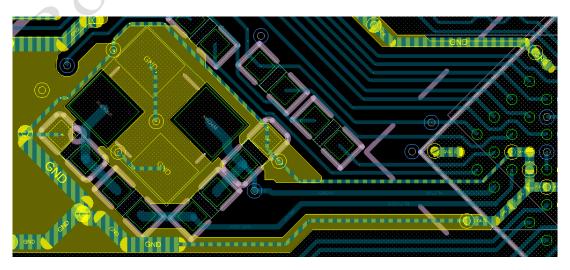


Figure 3-11 Edge requirement of signal reference plane diagram

 For other requirements, please refer to the description in the "Rockchip\_RK3568\_High\_Speed\_PCB\_Design\_Guide" document

### 3.2.1 Clock/Reset Circuit PCB Design

- Please pay attention to the following items in the PCB design of the clock circuit:
  - Give priority to the layout of the crystal circuit, which should be placed on the same layer as the chip and as close as possible to avoid drilling vias. The crystal trace should be as short as possible, away from interference sources, and as far as possible from the edge of the board;
  - The crystal and clock signal traces should be surrounded by ground throughout the whole process, and at least one GND via is added every 200-300mil for the surrounded ground line, and it is necessary to ensure the integrity of the ground reference plane of the neighboring layer;
  - If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground throughout the whole process, to avoid interference;
  - Clock traces Xin, Xout and the projection area under the crystal are prohibited from any traces to avoid noise coupling into the clock circuit;
  - A ground loop can be placed around the top layer under the crystal. The ground loop is connected to the neighboring ground layer through vias to isolate noise;
  - The second layer under the crystal maintains a complete ground reference plane to avoid any trace division, which helps to isolate noise and maintain the crystal output



**Rev V1.2** 

- The decoupling capacitor of the power supply must be placed on the back of the chip pin. Try to go through the capacitor pad and then to the chip pin when routing.
- Pay attention to the following items in the PCB design of the reset circuit:
  - During layout, the RESETn reset signal should be kept away from the edge of the board and metal connectors to prevent the reset module from crashing due to abnormalities caused by ESD.
  - The RESETn filter capacitors layout should be placed as close as possible to the chip pin. The signal must pass through the capacitors before entering the chip. Note that each ground pad of the filter capacitors must be with a 0402 ground via. It is recommended to place more than two grounding vias if space allowed.
  - The RESETn signal should be far away from strong interference signals such as DCDC and RF to prevent interference. If the trace is long, it is recommended to be surrounded by ground and add at least one GND vias every 400 mils.
  - The TVS protection diodes of the RESETn button should be placed as close as possible to the buttons. The signal topology is: button--->TVS--->100 ohm--->Capacitor (near CPU&PMIC) --->CPU&PMIC; when ESD occurs, The ESD current must be attenuated by the TVS components first.

### 3.2.2 PMIC/Power Circuit PCB Design

#### 3.2.2.1 RK809-5 power supply PCB design solution

- In the overall layout, from the perspective of power quality, RK809-5 should be placed as close as possible to RK3568 (when considering heat dissipation design, it needs to be placed properly, not too close or too far away. It is recommended that the interval is between 20mm-50mm, and try not to place it on the edge of the board to avoid bad heat dissipation). For placing direction, it is necessary to make the trace (copper covering) of RK809-5 BUCK output to RK3568 be smooth without crossing.
- RK809-5 BUCK1/BUCK2 PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor and VCC1/2 and GND should be as small as possible. The tracing of SW1/2 should be as short as possible to prevent interference to other modules; the tracing of VFB1/2 should be as close as possible to SW1/2. For places that need to place vias: VCC1/2 needs at least 4 pieces 0.5\*0.3mm vias, and VBUCK1/2 needs at least 5 pieces 0.5\*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

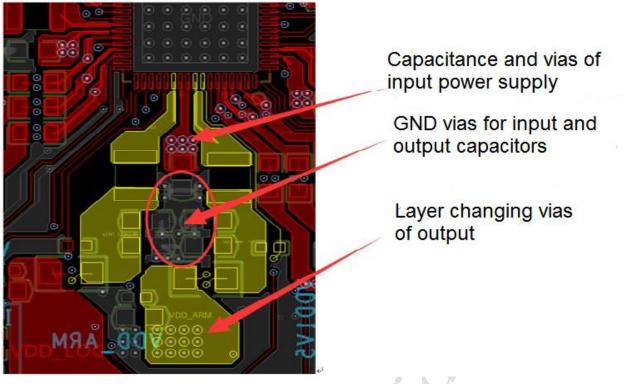


Figure 3-13 RK809-5 BUCK1/BUCK2 Layout and routing

■ K809-5 BUCK3 PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC3 and GND should be as small as possible. The tracing of SW3 should be as short as possible to prevent interference to other modules; the tracing of VFB3 should be as close as possible to SW3.

For places that need to drill vias, VCC3 needs at least three 0.5\*0.3mm vias, and VBUCK3 needs at least five 0.5\*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

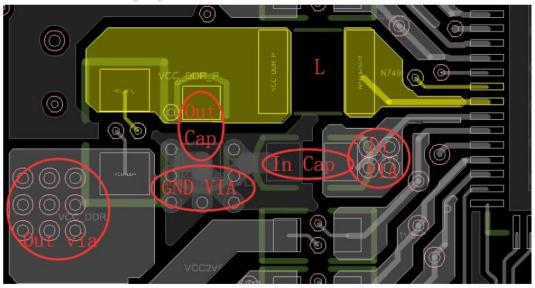


Figure 3-14 RK809-5 BUCK3 Layout and routing

■ RK809-5 BUCK4 PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC4 and GND should be as small as possible. The tracing of SW4 should be as short as possible to prevent interference to other modules; the tracing of VFB4 should be as close as possible to SW4.

For places that need to drill vias, VCC4 needs at least three 0.5\*0.3mm vias, and VBUCK4 needs at least five 0.5\*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

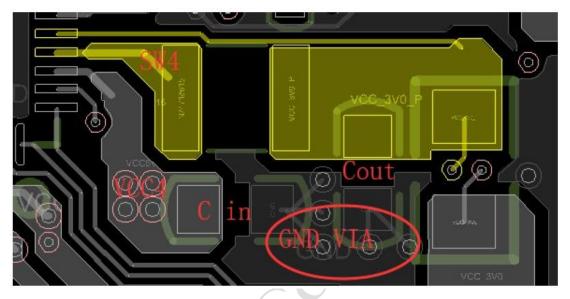


Figure 3-15 RK809-5 BUCK4 Layout and routing

#### RK809-5 BUCK5 PCB design requirements:

The input capacitors must be as close as possible to the chip, and the connection loop between the input capacitors, VCC9 and GND should be as small as possible. The tracing of SW5 should be as short as possible to prevent interference to other modules; the tracing of VFB5 should be as close as possible to SW5.

For places that need to drill vias, VCC9 needs at least three 0.5\*0.3mm vias, and VBUCK5 needs at least five 0.5\*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

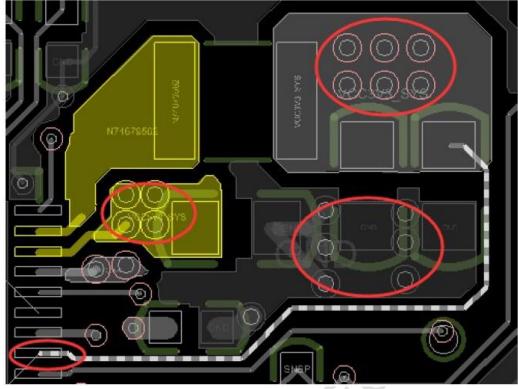


Figure 3-16 RK809-5 BUCK5 Layout and routing

■ RK809-5 LDO PCB design requirements:

The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor, VCC5/6/7/8 and GND should be as small as possible.

The output capacitor must be as close as possible to the chip, and the connection loop between the output capacitor, LDO1/2/3/4/5/6/7/8/9 and GND should be as small as possible.

- The XIN/XOUT signal traces of the 32.768KHz crystal of RK809-5 should be as short as possible, and the whole process should be surrounded by ground to ensure that there is a complete reference plane and no high-speed signals routing under the crystal circuit.
- The VREF capacitor of RK809-5 must be placed close to the pin and far away from other interference sources. The ground pad of the capacitor must be well grounded, that is, the path between the VREF capacitor ground pad and RK809-5 EPAD must be the shortest and must not be divided by other signals.
- 100nF capacitor of Pin 67 (RESETB) of RK809-5 must be close to RK809-5 pin
- It is recommended that the pins of RK809-5 should not be covered by copper. All pins are connected to the outside through tracing. The width of the tracing should not exceed the width of the pins to prevent the tin linking from pads becoming larger after the board is made.
- The EPAD ground pad of RK809-5 requires enough vias. It is recommended to ensure 5\*5 pieces of 0.5\*0.3mm or 6\*6 pieces of 0.4\*0.2mm vias to reduce ground impedance and enhance heat conduction.

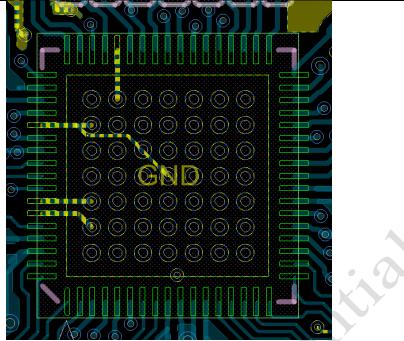


Figure 3-17 RK809-5 EPAD vias layout

## **3.2.2.2 DC-DC PCB design of discrete power supply**

The input capacitor CIN and output capacitor COUT are placed between VIN pin, VOUT pin and DC/DC GND, try to reduce the loop area between VIN, VOUT and DC/DC GND, so as to reduce the power ripple amplitude, Greatly improve the reliability of the chip, as shown below.

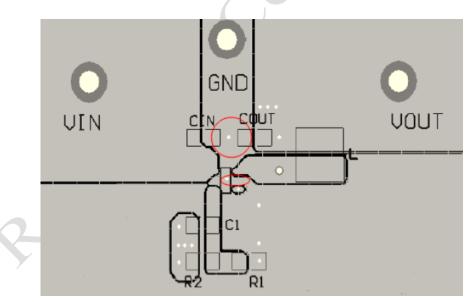


Figure 3-18 Discrete power supply DC/DC layout and routing

The input capacitor CIN, output capacitor COUT and DC/DC GND require as many vias as possible. It is recommended to have more than four 0503 vias. If the VIN and VOUT power supply have changed layers, it is recommended to place more vias. Four 0503 vias or more are recommended (it is related to the current, which will be described below). The inductance should be as close as possible to the DC/DC, the trace should be as thick and short as possible, and the resistance ground of the FB end should be as far away as possible from the interference source.

## 3.2.2.3 VDD\_CPU DC-DC Power PCB design

- The design of VDD\_CPU power supply is very important and directly affects the performance and stability of a product. Please design strictly according to RK's LAYOUT requirements.
- The VDD\_CPU power supply uses TCS4525 by default, and the overall layout should close to RK3568 as much as possible. The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor and VIN and GND should be as small as possible. The SW trace should be as short as possible to prevent interference to other modules; the VOUT trace should try to avoid being too close to SW. The connection loop between the output capacitor and GND should be as small as possible.

For places that need to drill vias, VIN needs at least five 0.5\*0.3mm vias, and Vbuck output needs at least twelve 0.5\*0.3mm vias.

Pay special attention to that the GND end of the input and output capacitors should be with the same number of vias as the positive end in order to achieve a better wave filtering effect.

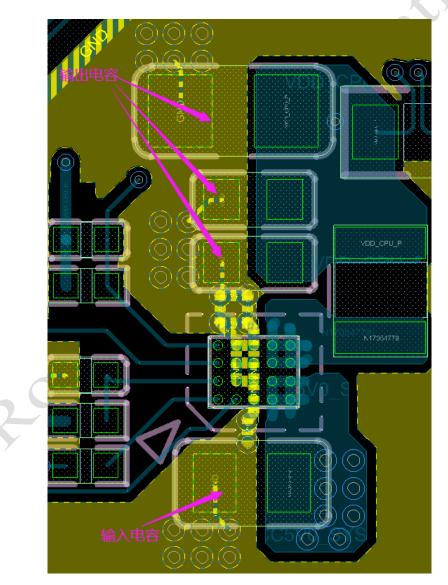


Figure 3-19 VDD\_CPU Power supply DC/DC layout and tracing

#### 3.2.2.4 VDD\_LOGIC,VDD\_GPU,VDD\_NPU,VDD\_CPU power supply DC-DC remote feedback design

■ The 1000hm feedback resistor should to be placed close to the output capacitor. One end of the resistor is

## **RK3568 Hardware Design Guide**

connected to the DC-DC output capacitor, the other end is connected to the FB feedback pin of the PMIC, and RK3568 power pin is connected to the most remote load of the same power network at the same time. The width of the feedback trace is 4mil, and it must be routed following the power supply copper to avoid interference; the feedback line is more than 6mil apart from other signals,

Such as the following diagram of VDD\_GPU power supply copper-covering and feedback line routing, other power supplies are similar.

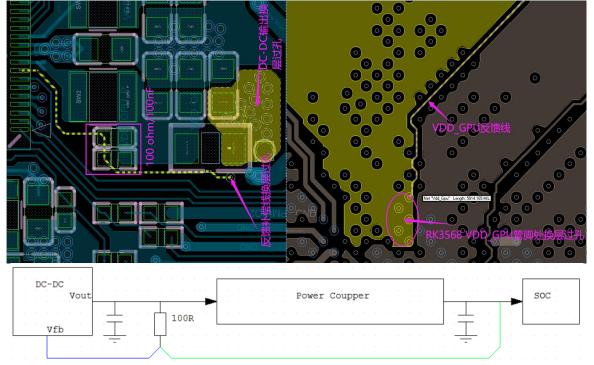


Figure 3-20 A diagram of DC/DC remote feedback design

#### 3.2.2.5 RK3568 VDD\_CPU Power PCB design

- The copper-covering width of VDD\_CPU should meet the current requirement of the chip. The copper-covering connected to the power pins of chip should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of CPU must be enough.
- When changing layer in peripheral, it is necessary for VDD\_CPU power supply to drill as many power vias as possible (more than twelve 0.5\*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For RK3568 chip VDD\_CPU power supply pin, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

## **RK3568 Hardware Design Guide**

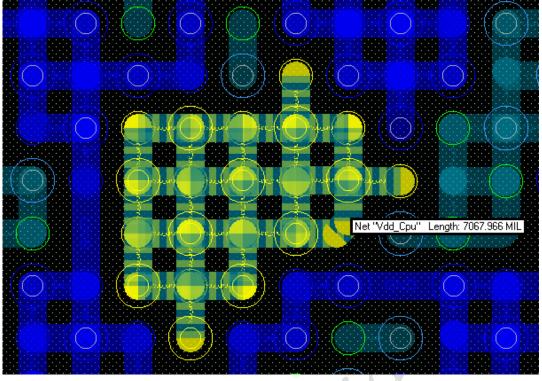


Figure 3-21 RK3568 VDD\_CPU Power pin routing and vias

On the schematic, the decoupling capacitors close to the VDD\_CPU power pin of RK3568 must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of decoupling capacitors should be placed as close as possible to RK3568.



Figure 3-22 Placement of decoupling capacitors on the back of RK3568 VDD\_CPU power pins

The trace width of the VDD\_CPU power supply in the CPU area should not be less than 90mil, and the trace width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the

voltage drop caused by the routing (please do not place layer change vias of other signal at will, they must be placed regularly, try to free up space for power supply and it is good for copper covering of ground)



Figure 3-23 Copper-covering on RK3568 VDD\_CPU power layer

#### 3.2.2.6 RK3568 VDD\_LOGIC Power PCB design

- The copper-covering width of VDD\_LOGIC should meet the current requirement of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough
- When changing layer in peripheral, it is necessary for VDD\_LOGIC power supply to drill as many power vias as possible (more than twelve 0.5\*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD\_LOGIC of RK3568, each ball requires a via, and they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

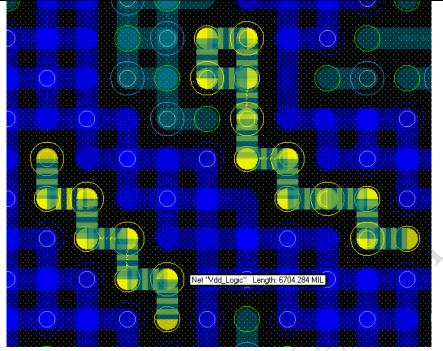


Figure 3-24 RK3568 VDD\_LOGIC power supply pin routing and vias

The decoupling capacitors close to the VDD\_LOGIC power pin of RK3568 in the schematic must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of decoupling capacitors should be placed as close as possible to RK3568.

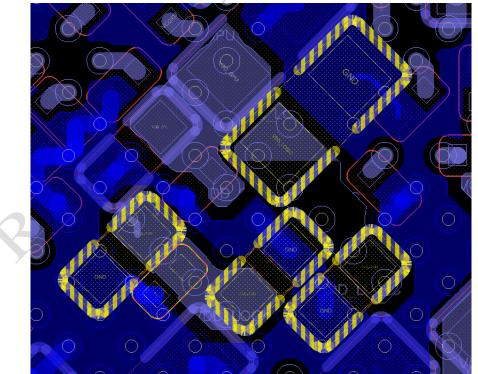


Figure 3-25 Placement of decoupling capacitors on the back of RK3568 VDD\_LOGIC power pins

The width of VDD\_LOGIC power supply in the CPU area should not be less than 60mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be

## **RK3568 Hardware Design Guide**

placed regularly, try to free up space for power supply and it is also good for copper covering of ground)

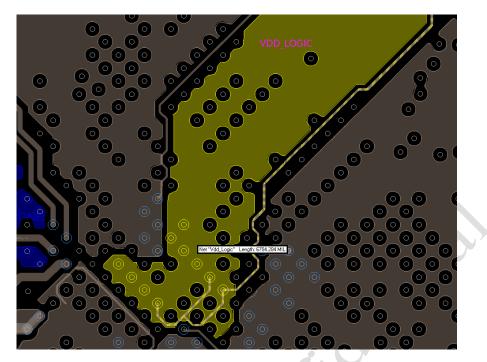


Figure 3-26 Copper-covering on RK3568 VDD\_LOGIC power layer

#### 3.2.2.7 RK3568 VDD\_GPU Power PCB design

- The copper-covering width of VDD\_GPU should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough
- When changing layer in peripheral, it is necessary for VDD\_GPU power supply to drill as many power vias as possible (more than five 0.5\*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD\_GPU of RK3568, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

## **RK3568 Hardware Design Guide**

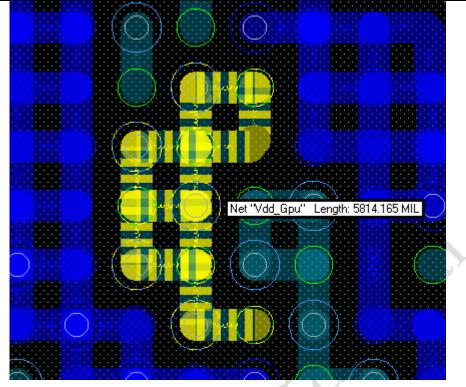


Figure 3-27 RK3568 VDD\_GPU Power pin traces and vias

The decoupling capacitors close to the VDD\_GPU power pin of RK3568 on the schematic, must be placed on the back of the corresponding power pin. The GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

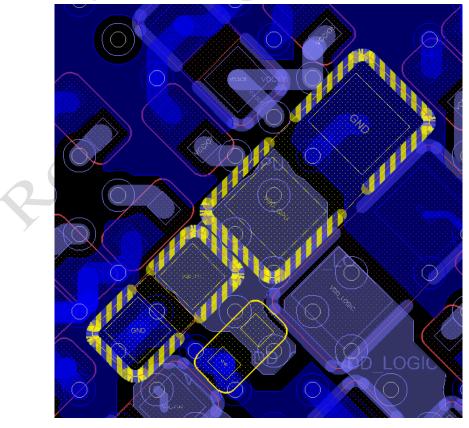


Figure 3-28 Placement of decoupling capacitors on the back of RK3568 VDD\_GPU power pins

The trace width of the VDD\_GPU power supply in the CPU area should not be less than 50mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground)



Figure 3-29 Copper covering on RK3568 VDD\_GPU power layer

#### 3.2.2.8 RK3568 VDD\_NPU Power PCB design

- The copper-covering width of VDD\_NPU should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough.
- When changing layer in peripheral, it is necessary for VDD\_NPU power supply to drill as many power vias as possible (more than five 0.5\*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VDD\_NPU of RK3568, each ball requires a via, they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

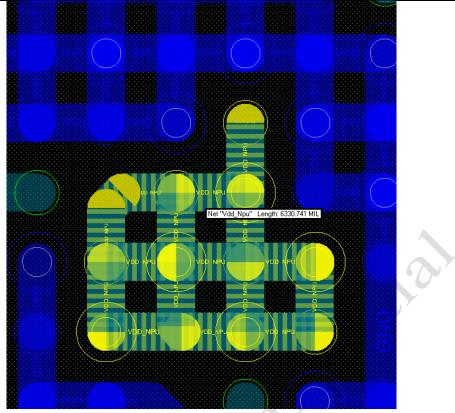


Figure 3-30 RK3568 VDD\_NPU Power pin routing and vias

The decoupling capacitor close to the VDD\_NPU power pin of RK3568 on the schematic, must be placed on the back of the corresponding power pin. The GND pad of the capacitor should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

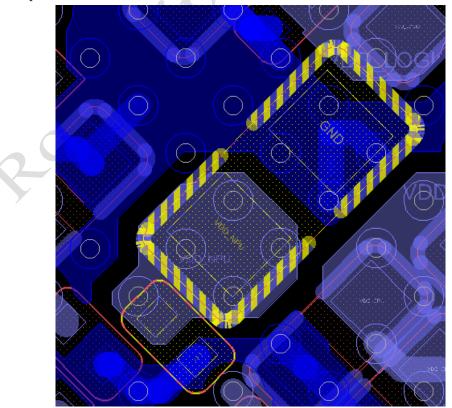


Figure 3-31 Placement of decoupling capacitors on the back of VDD\_NPU power Copyright © 2022 Rockchip Electronics Co., Ltd.

The trace width of the VDD\_NPU power supply in the CPU area should not be less than 50mil, and the trace width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by the routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground)

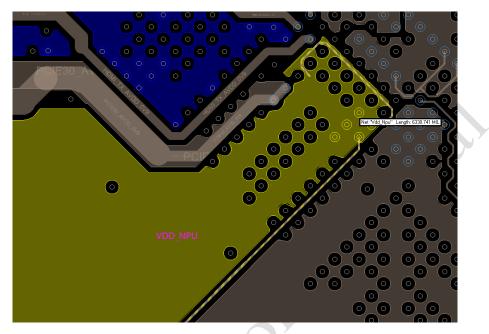


Figure 3-32 Copper covering on RK3568 VDD\_NPU power layer

#### 3.2.2.9 RK3568 VCC\_DDR Power PCB design

- The copper-covering width of VCC\_DDR should meet the current requirements of the chip. The copper-covering connected to the chip's power pins should be wide enough, and the path cannot be divided by vias, and calculated in effective line width, and make sure the path connected to each power pin of the CPU must be enough.
- When changing layer in peripheral, it is necessary for VCC\_DDR power supply to drill as many power vias as possible (more than eight 0.5\*0.3mm vias) to reduce the voltage drop caused by the layer change; the number of the GND vias of the decoupling capacitors should be the same with their power vias, otherwise capacitances effect will be greatly reduced.
- For the power supply pin VCC\_DDR of RK3568, each ball requires a via, and they are in a "井" shape on the top layer, cross-connected, and the recommended line width is 10mil

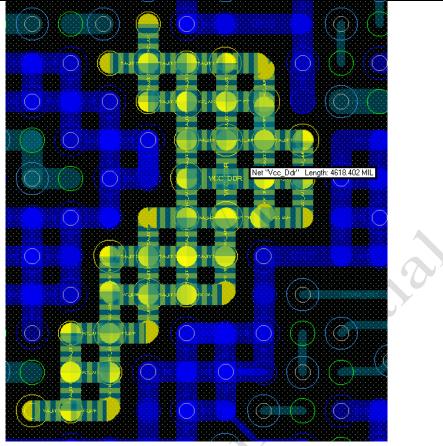


Figure 3-33 RK3568 VCC\_DDR power pin routing and vias



Figure 3-34 RK3568 VCC\_DDR/VCC0V6\_DDR Power pin routing and vias in LPDDR4x mode

The decoupling capacitor close to the VCC\_DDR power pin of RK3568 on the schematic, must be placed Copyright © 2022 Rockchip Electronics Co., Ltd.
173

When using LPDDR4x:

on the back of the corresponding power pin. The GND pad of the capacitor should be placed as close as possible to the GND Ball in the center of the chip. The rest of decoupling capacitors should be placed as close as possible to RK3568.

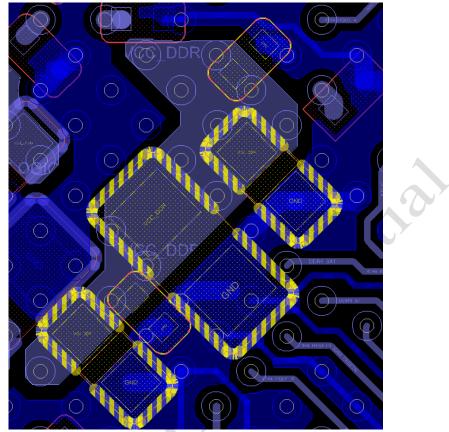


Figure 3-35 Placement of decoupling capacitor on the back of the power supply pin of RK3568 VCC\_DDR

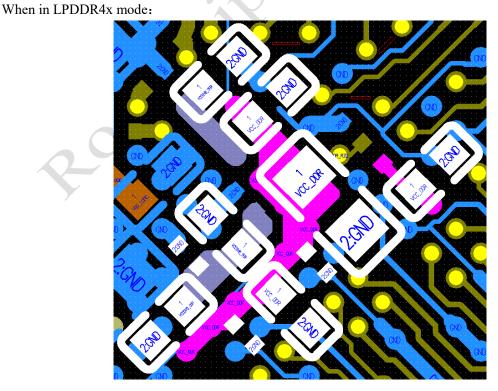


Figure 3-36 Placement of decoupling capacitors on the back of the power supply pins of VCC\_DDR/VCC0V6\_DDR of RK3568 in LPDDR4x mode

The trace width of VCC\_DDR power supply in the CPU area should not be less than 120mil, and the width of the peripheral area should not be less than 200mil. Try to use copper-covering to reduce the voltage drop caused by routing (please do not place layer change vias of other signal arbitrarily, they must be placed regularly, try to free up space for power supply and it is better for copper covering of ground) If it is a 4-layer board, the signal of the bottom layer has to take this plane as reference. Please refer to the description in the DRAM circuit PCB design for attentions.

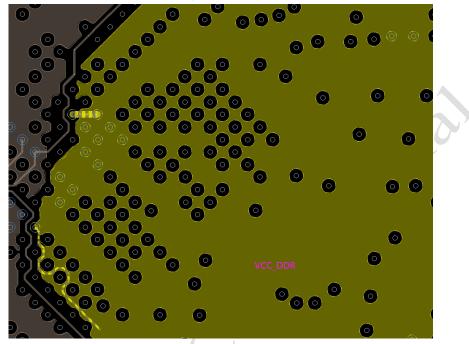


Figure 3-37 Copper covering on RK3568 VCC\_DDR power layer

#### 3.2.2.10 RK3568 GND pin PCB design

- For the GND pin of RK3568, ensure that every 1.5 ball correspond to a vias at least, and try to match a via to each ball, which provides better SI and PI conditions and is also helpful for heat dissipation.
- The neighboring layer of RK3568 chip must be a complete GND plane to ensure that the main reference ground is close to the Ball of CPU, to ensure the integrity of the power supply and enhance the heat dissipation of the PCB.
- The GND ball of the same network under RK3568 chip is in a "井" shape on the top layer, and is cross-connected. It is recommended that the trace width is 10mil.



Figure 3-38 RK3568 VSS pin routing and vias

The layer changing vias of each RK3568 signals should be place in the middle of the ball interval and regularly when layout, as shown in the figure, the ground in the middle of the rk3568 chip has a large area of copper connected with the outer ground copper. On the one hand, it is good for power supply and signal integrity, and on the other hand, it is good for heat dissipation of the chip.

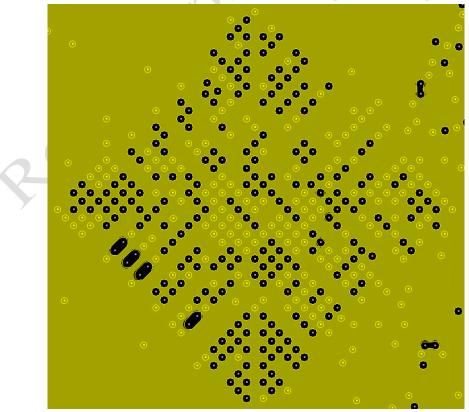


Figure 3-39 Ground copper-covering of RK3568

## **RK3568 Hardware Design Guide**

#### 3.2.2.11 PCB design of other RK3568 power supplies

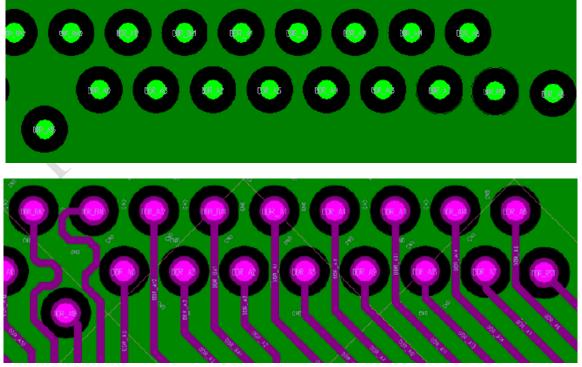
The decoupling capacitors of RK3568 other power supply must be placed on the back of the chip pin. When routing, try to go through the capacitor pad and then to the chip pin.

## 3.2.3 DRAM Circuit PCB design

Please apply the DDR reference template provided by Rockchip first.

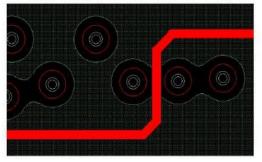
#### 3.2.3.1 Multilayer structure, impedance control, and other points of attention

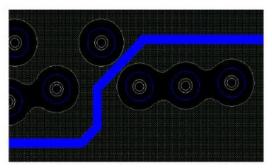
- When designing a 6-layer board: It is recommended to take the multilayer structure of TOP-GND-POWER-Signal-GND-Bottom (the structure where the L3 and L4 layers are relatively far apart), and the DDR signal should go on the TOP layer, Signal layer, and Bottom layer as far as possible, so that the return impedance of signals is the smallest. When signal changing layer, a stitching vias must be placed within 30 mils of the signal vias.
- **DDR** differential impedance is  $100\Omega \pm 10\%$
- **DDR** single-ended impedance is  $50\Omega \pm 10\%$
- The reference layer of DDR traces should be a complete ground plane to avoid continuous vias blocking the return path of the signal
- DDR signal traces should not go on the edge of the reference plane or the edge of PCB board, otherwise it will have a great impact of impedance. Ensure that the signal traces and the edge of the reference plane are greater than 40mil
- Optimize the position and spacing of layer changing vias, and do not damage the copper-covering of the power layer and the ground layer in a large area. If the copper-covering is divided by vias, it must be routed manually and then connected.



• Avoid that the return path is not connected, as shown in the figures below:

Bad





Good

- Keep integrity of VCC\_DDR power plane and do not route in the plane.
- Prohibit all DDR signals from crossing different planes
- Under 3200Mbps, the crosstalk between the DQ signals vias will increase, so the crosstalk of the vias must be minimized, please try not to change layers as much as possible. When layer changing is unavoidable, the number of layer changing vias side-by-side to DQ should not exceed two. Moreover, a stitching vias must be placed within 30 mils of the signal vias to provide a continuous return path and reduce crosstalk, and the number of signal layer-changing via must be controlled within two. The reference layer of the signal should be GND layer as much as possible. If it is converted into a power supply, then one stitching capacitor should be added corresponding to every 3 to 4 signal vias.
- VREF traces and other signals are guaranteed to be more than 3 times of line width. It is recommended that VREF be surrounded as much as possible, with the length of 15mil at least and the capacitor should be placed close to the DDR pins.
- The power decoupling capacitors must be placed on the back of the corresponding power pin, it is recommended to refer to the DDR template for placement.
- The decoupling capacitors of DDR VREF pin must be placed close to their respective pins
- Filter capacitor of RESET pin of DDR must be placed close to the pin
- The DDR circuit layout should be as close as possible to inner the board, away from the edge of the board and metal connectors to prevent the DDR module from crashing for abnormalities caused by ESD.

#### 3.2.3.2 DDR3/DDR3L PCB design

■ DDR3/DDR3L DQS/DQ/DM Signal routing topology

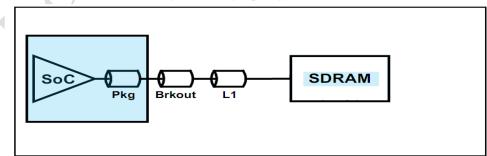


Figure 3-40 DDR3/DDR3L DQS/DQ/DM signal routing topology

Table 3–1 DDR3/DDR3L DQS/DQ/DM signal impedance and layout requirements			
Parameters	Requirement		
Single end impedance requirements	$50\Omega \pm 10\%$		
Differential impedance requirements	$100\Omega \pm 10\%$		
Length control requirement between DQ and DQS (within Byte)	The equal length between DQ and DQS don't need strictly controlled. It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible		
Length control requirement between DM and DQS (within Byte)	The equal length between DQ and DQS don't need strictly controlled. It is recommended to control it within 600mil, but make sure that the DM trace is as short as possible		
Equal length requirements between DQSP and DQSN	Less than 12mil		
Equal length requirements between DQS and CLK	Less than 1500mil		
Gap requirements between signals in DQ and DM groups	>=2 times the trace width		
Gap requirements between signals between DQ and DM groups	>=2 times the trace width		
Gap requirements between DQ/DM and DQS	>=3 times the trace width		
DQS routing requirements	If the trace is on the surface layer, DQS must be surrounded by ground all the way, and there must be ground vias within 200 mils of the ground trace		
DQ, DM routing requirements	If the trace is on the surface layer, in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be $\geq 2$ times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground wire interval, which can reduce crosstalk and signal impedance		

DDR3/DDR3L CLK signal routing topology

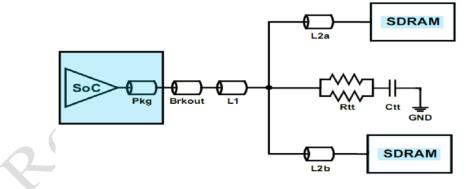


Figure 3-41 DDR3/DDR3L CLK signal routing topology

Clock signal matching method: RC circuit is placed at the branch point to improve the quality of the clock signal

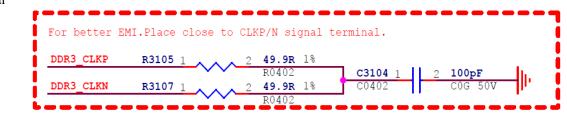


Figure 3-42 DDR3/DDR3L CLK signal RC circuit

# **RK3568 Hardware Design Guide** Table 3–2 DDR3/DDR3L CLK signal impedance

	CLK signal impedance and layout requirements		
Parameter	Requirements		
Differential impedance requirements	$100\Omega \pm 10\%$		
Equal length requirement between CLK and DQS	Less than 1500mil		
Equal length requirement between CLKP and CLKN	Less than 12mil		
Equal length requirement between L2a and L2b	Less than or equal to 20mil		
Length requirement of L2a, L2b	Less than 600mil, make sure the traces are as short as possible		
Length control requirements between CLK and CSn/CKE/ODT	Less than 30mil		
Length control requirements between CLK and other CA/CMD signals except CSn/CKE/ODT	Less than 600mil		
Gap requirements between CLK and other signals	>=3 times the line width		
CLK routing requirements	CLK must be surrounded by ground in the whole process, and there must be ground vias within 200mil of ground trace interval		

and largest no

~~~

#### DDR3/DDR3L CSn/CKE/ODT signal routing topology

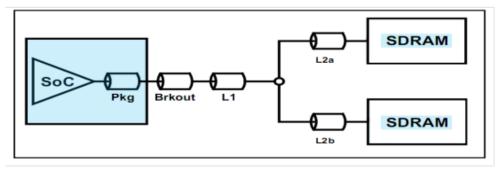


Figure 3-43 DDR3/DDR3L CSn/CKE/ODT signal layout topology

| Parameter                                              | Requirements                                                                                                     |
|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| Single ended impedance requirements                    | $50\Omega\pm10\%$                                                                                                |
| Equal length requirement between CSn/CKE/ODT and CLK   | Less than 30mil                                                                                                  |
| Gap requirements between CSn/CKE/ODT and other signals | >=2 times the trace width                                                                                        |
| Equal length requirements between L2a and L2b          | Less than or equal to 20mil                                                                                      |
| Length requirements of L2a, L2b trace                  | Less than 600mil, make sure the traces are as short as possible                                                  |
| Routing requirements of 4-layer board                  | The signal should follow in G-S-S-G way at bottom layer to provide a continuous return path and reduce crosstalk |

### Table 3-3 DDR3/DDR3L CSn/CKE/ODT signal impedance and layout requirements

-

Other CA/CMD signal of DDR3/DDR3L routing topologies except for CSn/CKE/ODT

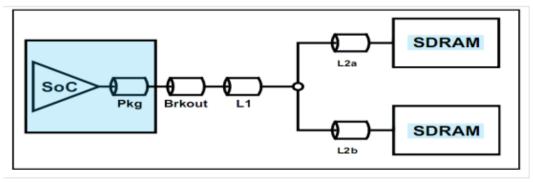


Figure 3-44 Other CA/CMD signal of DDR3/DDR3L layout topology except CSn/CKE/ODT

| parameter                                                                    | requirements                                                                                                     |  |  |
|------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|--|--|
| Single-ended impedance requirements                                          | $50\Omega \pm 10\%$                                                                                              |  |  |
| Equal length requirements of other CA/CMD signals and CLK except CSn/CKE/ODT | Less than 600mil                                                                                                 |  |  |
| Other signal gap requirements                                                | >=2 times the trace width                                                                                        |  |  |
| Equal length requirements between L2a and L2b                                | Less than or equal to 20mil                                                                                      |  |  |
| Length requirements of L2a, L2b trace                                        | Less than 600mil, make sure the traces are as short as possible                                                  |  |  |
| 4-layer board routing requirements                                           | The signal should follow in G-S-S-G way at bottom layer to provide a continuous return path and reduce crosstalk |  |  |

| Table 3-4 Other CA/CMD signal of DDR3/DDR3L layout topology except CSn/C | KE/ODT |
|--------------------------------------------------------------------------|--------|
|--------------------------------------------------------------------------|--------|

# 3.2.3.3 DDR3/DDR3L+ECC PCB design

■ DDR3/DDR3L+ECC DQS/DQ/DM signal routing topology

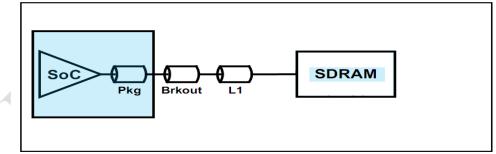


Figure 3-45 DDR3/DDR3L+ECC DQS/DQ/DM signal routing topology

| $T_11_2$ $T_2T_1$          |                        | · · · · · · · · · · · · · · · · · · · |                   |
|----------------------------|------------------------|---------------------------------------|-------------------|
| Table 3–5 DDR3/DDR3L+ECC D | JN/I JUJ/I JIVI SIONAL | impedance and ia                      | vour requirements |
|                            | ZO DQ DIN DIGNU        | impedance and la                      | your requirements |

| Parameter                                                   | Requirements                                                                                                                                                                                                                                                                                                                    |  |
|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| Single-ended impedance requirements                         | $50\Omega \pm 10\%$                                                                                                                                                                                                                                                                                                             |  |
| Differential impedance requirements                         | $100\Omega \pm 10\%$                                                                                                                                                                                                                                                                                                            |  |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need strictly controlled.<br>It is recommended to control it within 600mil, but make sure that the DQ trace is as short as possible                                                                                                                                                   |  |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need<br>strictly controlled.<br>It is recommended to control it within 600mil, but make<br>sure that the DM trace is as short as possible                                                                                                                                             |  |
| Equal length requirements between DQSP/DQSN                 | Less than 12mil                                                                                                                                                                                                                                                                                                                 |  |
| Equal length requirements between DQS and CLK               | Less than 1500mil                                                                                                                                                                                                                                                                                                               |  |
| Gap requirements between signals in DQ and DM groups        | >=2 times the trace width                                                                                                                                                                                                                                                                                                       |  |
| Gap requirements between signals between DQ and DM groups   | >=2 times the trace width                                                                                                                                                                                                                                                                                                       |  |
| Gap requirements between DQ/DM and DQS                      | >=3 times the trace width                                                                                                                                                                                                                                                                                                       |  |
| DQS routing requirements                                    | If the trace is on the surface layer, DQS must be<br>surrounded by ground all the way, and there must be<br>ground vias within 200 mils of the ground trace                                                                                                                                                                     |  |
| DQ, DM routing requirements                                 | If the trace is on the surface layer, in G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be $\geq 2$ times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |  |

■ DDR3/DDR3L+ECC CLK signal routing topology

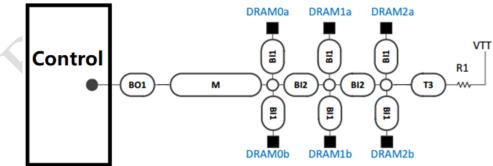


Figure 3-46 DDR3/DDR3L+ECC CLK signal layout topology

| Table 3–6 DDR3/DDR3L+E0                                                                   | CC CLK signal impedance and layout requirements                                                                                   |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Parameters                                                                                | Requirements                                                                                                                      |
| Differential impedance requirements                                                       | $100\Omega \pm 10\%$                                                                                                              |
| Equal length requirement between CLK and DQS                                              | Less than 1500mil                                                                                                                 |
| Equal length requirements between CLKP/CLKN                                               | Less than 12mil                                                                                                                   |
| Length control requirements between CLK and CSn/CKE/ODT                                   | Less than 60mil                                                                                                                   |
| Length control requirements between<br>CLK and other CA/CMD signals<br>except CSn/CKE/ODT | Less than 600mil                                                                                                                  |
| Gap requirements between CLK and other signals                                            | >=3 times the trace width                                                                                                         |
| CLK routing requirements                                                                  | CLK must be surrounded by ground in the whole<br>process, and there must be ground vias within 200mil<br>of ground trace interval |

A 2pF capacitor is connected in parallel between CLKP/N, and it should be as close as possible to RK3568 in

#### layout.

DDR3/DDR3L+ECC CSn/CKE/ODT signal routing topology 

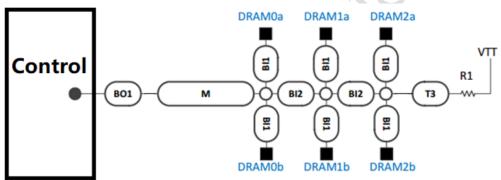


Figure 3-47 DDR3/DDR3L+ECC CSn/CKE/ODT signal routing topology

| Table 3-7 DDR3/DDR3L+ | -ECC CSn/CKE/ODT | signal impedance and la | vout requirements |
|-----------------------|------------------|-------------------------|-------------------|
|                       |                  |                         |                   |

| Parameters                                                | Requirements              |
|-----------------------------------------------------------|---------------------------|
| M-section trace impedance<br>requirements                 | $43\Omega \pm 10\%$       |
| Impedance requirements except for<br>M-segment trace      | $50\Omega \pm 10\%$       |
| Equal length requirement between CSn/CKE/ODT and CLK      | Less than 60mil           |
| Gap requirements between<br>CSn/CKE/ODT and other signals | >=2 times the trace width |

DDR3/DDR3L+ECC Other CA/CMD signal routing topology except CSn/CKE/ODT

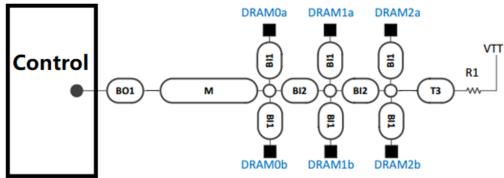


Figure 3-48 DDR3/DDR3L+ECC other CA/CMD signal layout topology except CSn/CKE/ODT

Table 3-8 DDR3/DDR3L+ECC other CA/CMD signal impedance and layout requirements except CSn/CKE/ODT

| Parameters                                           | Requirements              |  |  |
|------------------------------------------------------|---------------------------|--|--|
| M-section trace impedance requirements               | $50\Omega \pm 10\%$       |  |  |
| Impedance requirements except for<br>M-segment trace | $50\Omega \pm 10\%$       |  |  |
| Equal length requirement with CLK                    | Less than 600mil          |  |  |
| Gap requirements with other signals                  | >=2 times the trace width |  |  |

## 3.2.3.4 LPDDR3 PCB Design

| Table 3–9 LPDDR3 |            | 1           | 11        | •               |
|------------------|------------|-------------|-----------|-----------------|
|                  | cional im  | nadanca an  | nd lowout | raguiramanta    |
| 1au = 2 L D D D  | Signal III | Dettante an | iu iavoui | ICUUIICIIICIIIS |
|                  |            |             |           |                 |

| Parameters                                                     | Requirements                                                                                                                                                                          |
|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Single-ended impedance requirements                            | $50\Omega \pm 10\%$                                                                                                                                                                   |
| Differential impedance requirements                            | $100\Omega \pm 10\%$                                                                                                                                                                  |
| Length control requirement between DQ<br>and DQS (within Byte) | The equal length between DQ and DQS don't need be<br>strictly controlled<br>It is recommended to control it within 600mil, but make<br>sure that the DQ trace is as short as possible |
| Length control requirement between DM and DQS (within Byte)    | The equal length between DQ and DQS don't need be<br>strictly controlled<br>It is recommended to control it within 600mil, but make<br>sure that the DM trace is as short as possible |
| Equal length requirements between DQSP/DQSN                    | Less than 12mil                                                                                                                                                                       |
| Equal length requirements between<br>CLKP/CLKN之                | Less than 12mil                                                                                                                                                                       |
| Equal length requirements between DQS and CLK                  | Less than 1500mil                                                                                                                                                                     |
| Equal length requirements between CA/CMD and CLK               | Less than 30mil                                                                                                                                                                       |
| Gap requirements between signals in DQ and DM groups           | >=2 times the trace width                                                                                                                                                             |
| Gap requirements between signals between DQ and DM groups      | >=2 times the trace width                                                                                                                                                             |
| Gap requirements between DQ/DM and DQS                         | >=3 times the trace width                                                                                                                                                             |
| Gap requirements between CA/CMD and other signals              | >=2 times the trace width                                                                                                                                                             |
| Gap requirements between CLK and other signals                 | >=3 times the trace width                                                                                                                                                             |
| DQS routing requirements                                       | If the trace is on the surface layer, DQS must be<br>surrounded by ground all the way, and there must be<br>ground vias within 200 mils of the ground trace                           |

Copyright © 2022 Rockchip Electronics Co., Ltd.

| Parameters                                   | Requirements                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DQ, DM routing requirements                  | If the trace is on the surface layer, in G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be $\geq 2$ times the trace width and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |
| CA.CMD routing requirements of 4-layer board | The signal should follow in the G-S-S-G way at the<br>bottom layer to provide a continuous return path and<br>reduce crosstalk                                                                                                                                                                                                 |

#### 3.2.3.5 DDR4 PCB design

■ DDR4 DQS/DQ/DM signal routing topology

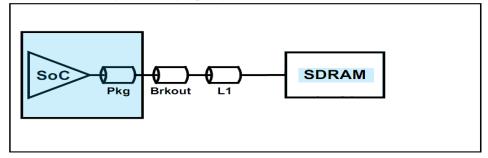


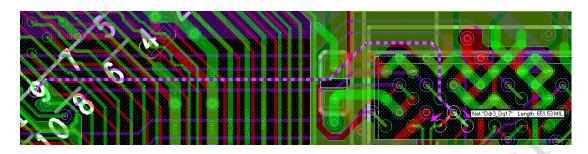
Figure 3-49 DDR4 DQS/DQ/DM signal layout topology

| Table 3–10 DDR4 DQS/DQ | Q/DM signal | impedance and | layout requirements |  |
|------------------------|-------------|---------------|---------------------|--|
|                        |             |               |                     |  |

| Parameters                                                  | Requirements                                                                                                                                                                                                                                                                                                                        |
|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Single-ended impedance requirements                         | $50\Omega \pm 10\%$                                                                                                                                                                                                                                                                                                                 |
| Differential impedance requirements                         | $100\Omega\pm10\%$                                                                                                                                                                                                                                                                                                                  |
| Length control requirement between DQ and DQS (within Byte) | The equal length between DQ and DQS don't need be<br>strictly controlled<br>It is recommended to control it within 600mil, but make<br>sure that the DQ trace is as short as possible                                                                                                                                               |
| Length control requirement between DM and DQS (within Byte) | The equal length between DQ and DQS don't need be<br>strictly controlled<br>It is recommended to control it within 600mil, but make<br>sure that the DM trace is as short as possible                                                                                                                                               |
| Equal length requirements between DQSP/DQSN                 | Less than 12mil                                                                                                                                                                                                                                                                                                                     |
| Equal length requirements between DQS and CLK               | Less than 1500mil                                                                                                                                                                                                                                                                                                                   |
| Gap requirements between signals in DQ and DM groups        | >=2 times the trace width                                                                                                                                                                                                                                                                                                           |
| Gap requirements between signals between DQ and DM groups   | >=2 times the trace width                                                                                                                                                                                                                                                                                                           |
| Gap requirements between DQ/DM and DQS                      | >=3 times the trace width                                                                                                                                                                                                                                                                                                           |
| DQS routing requirements                                    | If the trace is on the surface layer, DQS must be<br>surrounded by ground all the way, and there must be<br>ground vias within 200 mils of the ground trace                                                                                                                                                                         |
| DQ, DM routing requirements                                 | If the trace is on the surface layer, in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be $\geq 2$ times the trace width, and the gap between G-S is 1 time the trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

Note:

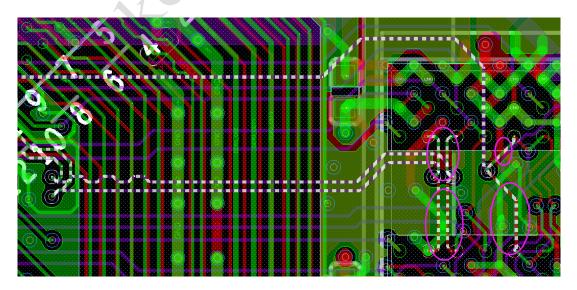
When using 4 pieces of 16bit DDR4, since the DQ/DM/DQS of cs0 and cs1 are shared, in order to get better signal quality, it is recommended to use symmetric placement, adjust the DQ order in the cs1 group to make the branch shortest, as shown in the figure below (see reference schematic for adjusted order)



DM/DQS does not support exchange, branches must be equal in length strictly, and the impact of layer-changing vias paths should be taken in consideration. For example, the controller signal trace is on the L4 layer, and the distance of switching to TOP layer through the via is farther than switching to Bottom layer.



When the branches are equal in length, this impact should be considered. As shown in the figure below, the branch traces of Top layer are short, and the branch traces of Bottom layer are long. This difference needs to be compensated.



DDR4 CLK signal routing topology

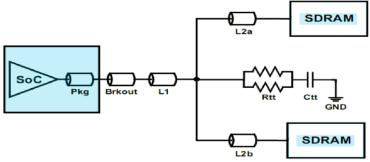


Figure 3-50 DDR4 CLK signal routing topology

Clock signal matching method: Place an RC circuit at the branch point, and it is also necessary to connect a series resistor to the DDR on the branch circuit. The series resistor must be placed at the branch point to improve the quality of the clock signal.

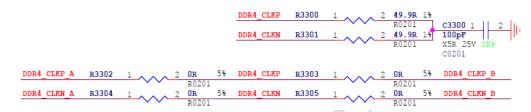


Figure 3-51 RC circuit for DDR4 CLK signal

| Parameters                                                                                | Requirements                                                                                                                      |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Differential impedance requirements                                                       | $100\Omega \pm 10\%$                                                                                                              |
| Equal length requirement between<br>CLK and DQS                                           | Less than 1500mil                                                                                                                 |
| Equal length requirements between<br>CLKP/CLKN                                            | Less than 12mil                                                                                                                   |
| Equal length requirements between L2a and L2b                                             | Less than or equal to 20mil                                                                                                       |
| Length requirements of L2a, L2b                                                           | Less than 600mil, make sure the traces are as short as possible                                                                   |
| Length control requirements between<br>CLK and CSn/CKE/ODT                                | Less than 30mil                                                                                                                   |
| Length control requirements between<br>CLK and other CA/CMD signals<br>except CSn/CKE/ODT | Less than 600mil                                                                                                                  |
| Gap requirements between CLK and other signals                                            | >=3 times the trace width                                                                                                         |
| CLK routing requirements                                                                  | CLK must be surrounded by ground in the whole<br>process, and there must be ground vias within 200mil<br>of ground trace interval |

Table 3–11 DDR4 CLK signal impedance and layout requirements

If it is a 4-layer board, DDR4 needs to rout through the Power layer, then the signal routed on the Power layer must follow in the G-S-S-G mode, as shown in the figure, the blue is the ground trace, and it is recommended to copy the reference PCB directly. Check from beginning to end that is it go with a complete ground trace, it is recommended to directly apply the template provided by RK.

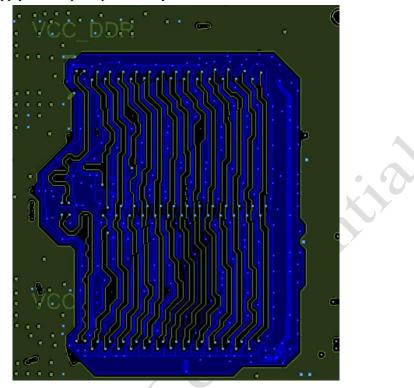


Figure 3-52 CLK/CA/CMD signal routing diagram on the L3 plane of DDR4 4-layer board

■ DDR4 CSn/CKE/ODT signal routing topology

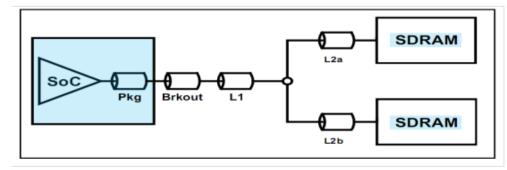


Figure 3-53 DDR4 CSn/CKE/ODT signal routing topology

| Parameters                            | Requirements                  |
|---------------------------------------|-------------------------------|
| Single-ended impedance requirements   | $50\Omega \pm 10\%$           |
| Equal length requirement between      | Less than 30mil               |
| CSn/CKE/ODT and CLK                   |                               |
| Gap requirements between              | >=2 times the trace width     |
| CSn/CKE/ODT and other signals         |                               |
| Equal length requirements between L2a | Loss there are equal to 20mil |
| and L2b                               | Less than or equal to 20mil   |

Table 3-12 DDR4 CSn/CKE/ODT signal impedance and layout requirements

| Parameters                             | Requirements                                         |
|----------------------------------------|------------------------------------------------------|
| Length requirements of L2a, L2b        | Less than 600mil, make sure the trace is as short as |
|                                        | possible                                             |
| Routing requirements for 4-layer board | The signal needs to take G-S-S-G way at the bottom   |
|                                        | layer to provide a continuous return path and reduce |
|                                        | crosstalk                                            |

• Other CA / CMD signal routing topologies except CSN / CKE / ODT when using DDR4

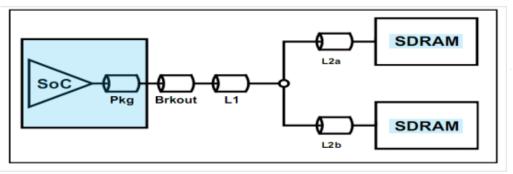


Figure 3-54 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4

| Table 3-13 Other CA /CMD signal routing topologies except CSN/CKE/ODT when using DDR4 |
|---------------------------------------------------------------------------------------|
|---------------------------------------------------------------------------------------|

| Parameters                                    | Requirements                                          |
|-----------------------------------------------|-------------------------------------------------------|
| Single-ended impedance requirements           | $50\Omega \pm 10\%$                                   |
| The equal length requirements between         |                                                       |
| CLK and other CA/CMD signals                  | Less than 600mil                                      |
| except CSn/CKE/ODT                            |                                                       |
| Other signal gap requirements                 | >=2 times the trace width                             |
| Equal length requirements between L2a and L2b | Less than or equal to 20mil                           |
| Length requirements of L2a, L2b               | Less than 600mil, make sure the trace is as short as  |
|                                               | possible                                              |
| Routing requirements for 4-layer board        | The signal is in G-S-S-G way at the bottom layer to   |
| Routing requirements for 4-rayer board        | provide a continuous return path and reduce crosstalk |

## 3.2.3.6 DDR4+ECC PCB design

■ DDR4+ECC DQS/DQ/DM signal routing topology

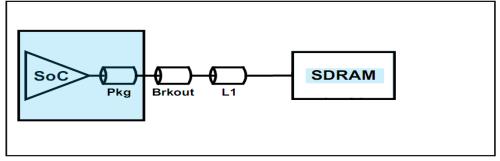


Figure 3-55 DDR4+ECC DQS/DQ/DM signal layout topology

| Parameters                                    | Requirements                                              |
|-----------------------------------------------|-----------------------------------------------------------|
| Single-ended impedance requirements           | $50\Omega \pm 10\%$                                       |
| Differential impedance requirements           | $100\Omega \pm 10\%$                                      |
|                                               | The equal length between DQ and DQS don't need b          |
| Length control requirement between            | strictly controlled.                                      |
| DQ and DQS (within Byte)                      | It is recommended to control it within 600mil, but make   |
|                                               | sure that the DQ trace is as short as possible            |
|                                               | The equal length between DQ and DQS don't need b          |
| Length control requirement between            | strictly controlled.                                      |
| DM and DQS (within Byte)                      | It is recommended to control it within 600mil, but make   |
| Divi and DQS (within Byte)                    | sure that the DM trace is as short as possible            |
| Equal length requirements between             | sure that the Divi trace is as short as possible          |
| DQSP/DQSN                                     | Less than 12mil                                           |
| Equal length requirements between DQS and CLK | Less than 1500mil                                         |
| Gap requirements between signals in           | >=2 times the trace width                                 |
| DQ and DM groups                              |                                                           |
| Gap requirements between signals              | >=2 times the trace width                                 |
| between DQ and DM groups                      |                                                           |
| Gap requirements between DQ/DM and DQS        | >=3 times the trace width                                 |
|                                               | If the trace is on the surface layer, DQS must b          |
| DQS routing requirements                      | surrounded by ground all the way, and there must b        |
|                                               | ground vias within 200 mils of the ground trace           |
| NL.                                           | If the trace is on the surface layer, in G-S-S-G way (G   |
|                                               | ground trace, S: signal trace), the gap between S-S mu    |
|                                               | be $\geq 2$ times the line width, and the gap between G-S |
| DQ, DM routing requirements                   | 1 time line width, there must be ground vias within 20    |
|                                               | mils of the ground trace interval, which can reduc        |
| <b>y</b>                                      | crosstalk and signal impedance                            |
| DDR4+ECC CLK signal routing topolog           |                                                           |
|                                               | DRAM0a DRAM1a DRAM2a                                      |
| Control                                       |                                                           |
| B01)-                                         |                                                           |
|                                               |                                                           |

Figure 3-56 DDR4+ECC CLK signal layout topology

| Table 3–15 DDR4+ECC CLK signal impedance and layout requirements                          |                                                                                                                                   |  |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|--|
| Parameters                                                                                | Requirements                                                                                                                      |  |
| Differential impedance requirements                                                       | $100\Omega \pm 10\%$                                                                                                              |  |
| Equal length requirement between CLK and DQS                                              | Less than 1500mil                                                                                                                 |  |
| Equal length requirements between CLKP/CLKN                                               | Less than 12mil                                                                                                                   |  |
| Length control requirements between<br>CLK and CSn/CKE/ODT                                | Less than 60mil                                                                                                                   |  |
| Length control requirements between<br>CLK and other CA/CMD signals<br>except CSn/CKE/ODT | Less than 600mil                                                                                                                  |  |
| Gap requirements between CLK and other signals                                            | >=3 times the trace width                                                                                                         |  |
| CLK routing requirements                                                                  | CLK must be surrounded by ground in the whole<br>process, and there must be ground vias within 200mil<br>of ground trace interval |  |

A 2pF capacitor is connected in parallel between CLKP/N, and its layout should be as close as possible to

## RK3568.

■ DDR4+ECC CSn/CKE/ODT signal routing topology

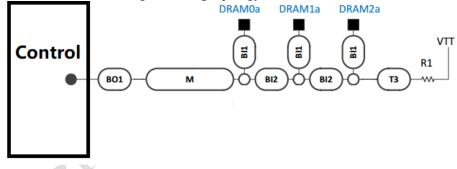


Figure 3-57 DDR4+ECC CSn/CKE/ODT signal routing topology

| Parameters                        | Requirements              |
|-----------------------------------|---------------------------|
| M-section trace impedance         | $43\Omega \pm 10\%$       |
| requirements                      | +322 ±1070                |
| Impedance requirements except for | $50\Omega \pm 10\%$       |
| M-segment trace                   | 5052 ±10 %                |
| Equal length requirement between  | Less than 60mil           |
| CSn/CKE/ODT and CLK               |                           |
| Gap requirements between          | >=2 times the trace width |
| CSn/CKE/ODT and other signals     | -2 unles the trace width  |

Table 3–16 DDR4+ECC CSn/CKE/ODT signal impedance and layout requirements

DDR4+ECC other CA/CMD signal routing topology except CSn/CKE/ODT

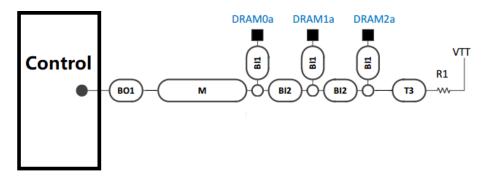


Figure 3-58 DDR4+ECC other CA/CMD signal layout topology except CSn/CKE/ODT

| Table 3-17 DDR4+ECC other CA/CMD signal impedance and layout requirements except     | CC /CVE/ODT    |
|--------------------------------------------------------------------------------------|----------------|
| Lable $3-1$ / DDR4+ECU other CA/CMD signal impedance and layout reduirements except  | (Nn/(KE/(DD))) |
| Tuble 5 17 DDT(1) DCC blief of bottin bight impedance and tayout requirements except |                |

| Parameters                                           | Requirements              |
|------------------------------------------------------|---------------------------|
| M-section trace impedance requirements               | $50\Omega \pm 10\%$       |
| Impedance requirements except for<br>M-segment trace | 50Ω ±10%                  |
| Equal length requirement with CLK                    | Less than 600mil          |
| Gap requirements with other signals                  | >=2 times the trace width |

#### 3.2.3.7 LPDDR4 PCB design

Table 3–18 LPDDR4 signal impedance and layout requirements

| Parameters                          | Requirements                                            |
|-------------------------------------|---------------------------------------------------------|
| Single-ended impedance requirements | $50\Omega \pm 10\%$                                     |
| Differential impedance requirements | $/100\Omega \pm 10\%$                                   |
|                                     | The equal length between DQ and DQS don't need be       |
| Length control requirement between  | strictly controlled.                                    |
| DQ and DQS (within Byte)            | It is recommended to control it within 600mil, but make |
|                                     | sure that the DQ trace is as short as possible          |
|                                     | The equal length between DQ and DQS don't need be       |
| Length control requirement between  | strictly controlled.                                    |
| DM and DQS (within Byte)            | It is recommended to control it within 600mil, but make |
| 7                                   | sure that the DM trace is as short as possible          |
| Equal length requirements between   | Less than 12mil                                         |
| DQSP/DQSN                           |                                                         |
| Equal length requirements between   | Less than 12mil                                         |
| CLKP/CLKN                           |                                                         |
| Equal length requirements between   | Less than 1200mil                                       |
| DQS and CLK                         |                                                         |
| Equal length requirements between   | Less than 500mil                                        |
| CA/CMD and CLK                      |                                                         |

| Parameters                                                   | Requirements                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Gap requirements between signals in DQ and DM groups         | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between signals<br>between DQ and DM groups | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between DQ/DM and DQS                       | >=3 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between CA/CMD<br>and other signals         | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between CLK and other signals               | >=3 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| DQS routing requirements                                     | If the trace is on the surface layer, DQS must be<br>surrounded by ground all the way, and there must be<br>ground vias within 200 mils of the ground trace                                                                                                                                                                              |
| DQ, DM routing requirements                                  | If the trace is on the surface layer in the GSSG way (G:<br>ground trace, S: signal trace), the gap between S-S must<br>be >=2 timesthe trace width, and the gap between G-S<br>is 1 time the trace width, there must be ground vias<br>within 200 mils of the ground trace interval, which can<br>reduce crosstalk and signal impedance |
| CA.CMD routing requirements for<br>4-layer boards            | The signal should follow in the G-S-S-G way at the<br>bottom layer to provide a continuous return path and<br>reduce crosstalk                                                                                                                                                                                                           |

# 3.2.3.8 LPDDR4x PCB design

Table 3–19 LPDDR4 signal impedance and layout requirements

| Parameters                          | Requirements                                            |
|-------------------------------------|---------------------------------------------------------|
| Single-ended impedance requirements | $50\Omega \pm 10\%$                                     |
| Differential impedance requirements | $100\Omega \pm 10\%$                                    |
|                                     | The equal length between DQ and DQS don't need be       |
| Length control requirement between  | strictly controlled.                                    |
| DQ and DQS (within Byte)            | It is recommended to control it within 600mil, but make |
|                                     | sure that the DQ trace is as short as possible          |
|                                     | The equal length between DQ and DQS don't need be       |
| Length control requirement between  | strictly controlled.                                    |
| DM and DQS (within Byte)            | It is recommended to control it within 600mil, but make |
|                                     | sure that the DM trace is as short as possible          |
| Equal length requirements between   | Less then 12mil                                         |
| DQSP/DQSN                           | Less than 12mil                                         |

| Parameters                                                | Requirements                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Equal length requirements between CLKP/CLKN               | Less than 12mil                                                                                                                                                                                                                                                                                                                          |
| Equal length requirements between DQS and CLK             | Less than 1200mil                                                                                                                                                                                                                                                                                                                        |
| Equal length requirements between CA/CMD and CLK          | Less than 500mil                                                                                                                                                                                                                                                                                                                         |
| Gap requirements between signals in DQ and DM groups      | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between signals between DQ and DM groups | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between DQ/DM and DQS                    | >=3 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between CA/CMD and other signals         | >=2 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| Gap requirements between CLK and other signals            | >=3 timesthe trace width                                                                                                                                                                                                                                                                                                                 |
| DQS routing requirements                                  | If the trace is on the surface layer, DQS must be<br>surrounded by ground all the way, and there must be<br>ground vias within 200 mils of the ground trace                                                                                                                                                                              |
| DQ, DM routing requirements                               | If the trace is on the surface layer, follow in the G-S-S-G way (G: ground trace, S: signal trace), the gap between S-S must be $\geq 2$ timesthe trace width, and the gap between G-S is 1 timethe trace width, there must be ground vias within 200 mils of the ground trace interval, which can reduce crosstalk and signal impedance |

# 3.2.4 Flash Circuit PCB design

## 3.2.4.1 eMMC PCB design

| Parameters                                            | Requirements              |
|-------------------------------------------------------|---------------------------|
| Single-ended impedance requirements                   | $50\Omega \pm 10\%$       |
| Equal length requirements between DATA/CMD and CLK/DS | Less than 120mil          |
| Total length requirement of PCB trace                 | Less than 4000mil         |
| Gap requirements between eMMC signals                 | >=2 times the trace width |
| Gap requirements between eMMC                         | >=3 times the trace width |

Table 3-20 eMMC signal impedance and layout requirements

Copyright © 2022 Rockchip Electronics Co., Ltd.

| Parameters                             | Requirements                                                                                                                              |
|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| signal and other signals               |                                                                                                                                           |
| Layer change vias                      | If they are less than 4, symmetrical stitching vias<br>should be placed close to the signal layer changing vias                           |
| Routing requirements of eMMC<br>CLK/DS | They must be surrounded by ground in the whole<br>process, and there must be ground vias within 300 mils<br>of the ground trace interval. |

Other points for attention:

- In the overall layout, place eMMC as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all eMMC signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The 22ohm series matching resistor of eMMC\_CLKOUT should be close to CPU (source end), and the trace between CPU pin and the resistor must be controlled within 300mil.
- The 0ohm series matching resistor of eMMC\_DATA\_STROBE should be close to eMMC, and the trace between the eMMC pin and the resistor must be controlled within 300mil.
- The width of the eMMC power trace should meet the current requirements of VCCIO2 power domain and the corresponding eMMC. It is recommended that the VCCIO2 power domain trace should be more than 12mil, and the power trace of the eMMC should be more than 25mil.
- The decoupling capacitors of eMMC and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- The external capacitor of the VDDi pin of eMMC must be placed close to the corresponding pin, and the trace should be as short and thick as possible
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the eMMC D0 signal, and do not generate additional branches

#### 3.2.4.2 FSPI PCB design

| Parameters                                        | Requirements                                                                                       |
|---------------------------------------------------|----------------------------------------------------------------------------------------------------|
| Single-ended impedance requirements               | $50\Omega \pm 10\%$                                                                                |
| Equal length requirement between DATA and CLK     | Less than 200mil                                                                                   |
| Total length requirement of PCB trace             | Less than 4000mil                                                                                  |
| Gap requirements between FSPI signals             | >=2 times the trace width                                                                          |
| The gap between the FSPI signal and other signals | >=3 times the trace width                                                                          |
| Layer change via                                  | If it is less than 4, symmetrical stitching vias should be<br>placed close to the layer change via |

Table 3–21 FSPI signal impedance and layout requirements

## **RK3568 Hardware Design Guide**

| Parameters                    | Requirements                                          |
|-------------------------------|-------------------------------------------------------|
|                               | It must be surrounded by ground in the whole process, |
| FSPI CLK routing requirements | and there must be ground vias within 300 mils of the  |
|                               | ground trace interval.                                |

Other points for attention:

- In the overall layout, try to place FSPI as close to RK3568 to shorten the trace as much as possible.
- The reference layer of all FSPI signals should be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The 22ohm series matching resistor of FSPI\_CLK is close to the CPU (source end), and the trace between CPU pin and the resistor must be controlled within 300mil.
- The width of the FSPI Flash power trace should meet the current requirements of VCCIO2 power domain and the corresponding FSPI. It is recommended that the width of VCCIO2 power domain traces be more than 12mil, and the FSPI power traces should be more than 25mil.
- The decoupling capacitors of FSPI Flash and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the FSPI CLK signal, and do not generate additional branches

## 3.2.4.3 Nand Flash PCB design

| Table 5 22 Nand Flash signal impedance and layout requirements | Table 3–22 Nand Flash signal | impedance and | layout requirements |
|----------------------------------------------------------------|------------------------------|---------------|---------------------|
|----------------------------------------------------------------|------------------------------|---------------|---------------------|

| Parameters                                                   | Requirements                                               |
|--------------------------------------------------------------|------------------------------------------------------------|
| Single-ended impedance requirements                          | $50\Omega \pm 10\%$                                        |
| Equal length requirements between the whole group of signals | Less than 200mil                                           |
| Total length requirement of PCB trace                        | Less than 4000mil                                          |
| Gap requirements between Nand Flash signals                  | >=2 times the trace width                                  |
| Gap requirements Nand Flash signal and other signals         | >=3 times the trace width                                  |
| Layer change via                                             | If it is less than 4, symmetrical stitching vias should be |
| Layer change via                                             | placed close to the signal layer change via                |
|                                                              | It must be surrounded by ground in the whole process,      |
| Nand Flash DQS routing requirements                          | and there must be ground vias within 300 mils of the       |
|                                                              | ground trace interval.                                     |

#### Other points for attention:

- In the overall layout, place Nand Flash as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all Nand Flash signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.

- The 0ohm series matching resistor of Nand Flash\_DQS is close to the end of the Nand Flash, and the trace between the Nand pin and the resistor must be controlled within 300mil.
- The width of the Nand Flash power line should meet the current requirements of the VCCIO2 power domain and the corresponding Nand Flash. It is recommended that the width of VCCIO2 power domain traces be more than 12mil, and Nand Flash power traces should be more than 25mil.
- The decoupling capacitors of Nand Flash and RK3568 VCCIO2 must be placed on the back of the corresponding power pins.
- It is recommended to use Daisy-chain for PCB routing at the reserved test point of the Nand D0 signal, and do not generate additional branches

#### 3.2.4.4 Note of eMMC and Nand Flash compatible design PCB

When dual layout is required for eMMC and Nand Flash compatible design, you need to pay attention to avoid long branches routing, causing abnormal functions. R4003, R4000, R4001 and R4100, R4101, R4102 must be placed on each signal branch point (please refer to RK3568\_AIoT\_REF\_SCH for the tag number)



Figure 3-59 Branch resistances of eMMC and Nand Flash compatible design

As shown in the figure below, R4000 and R4100 are placed on the branch point. When using eMMC, only R4000 is connected instead of R4100 to minimized the influence as much as possible

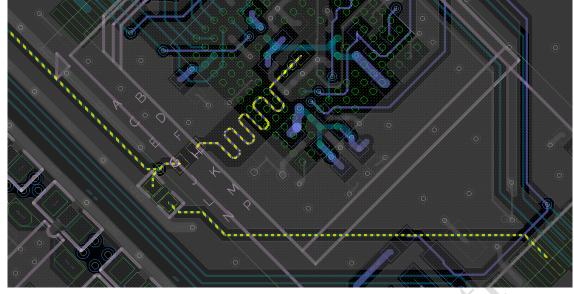


Figure 3-60 Branch resistor layout and routing of eMMC and NAND flash compatible design

When dual layout is required for compatible design of eMMC and Nand Flash, D0-D7 signals are recommended to use Daisy-chain. The routing must pass through the Nand pins and then connect to the eMMC pins. The eMMC pins should be as close as possible to the Nand pins. If compatible design is not necessary, it is recommended to keep only eMMC instead of Nand Flash to improve the stability of eMMC.

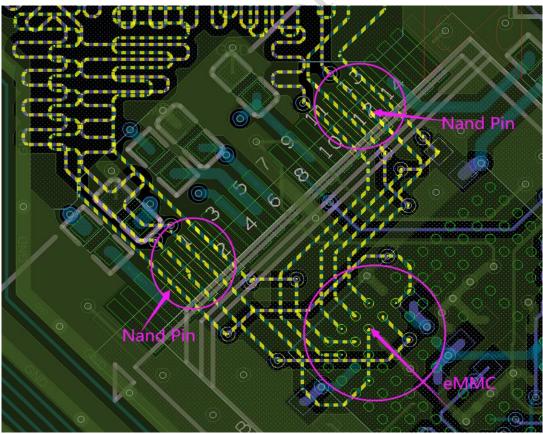


Figure 3-61Figure 3-1 DATA routing of eMMC and Nand Flash compatible design

# **RK3568 Hardware Design Guide**

## 3.2.5 SDMMC0/1/2 Interface Crcuit PCB Design

| Parameters                                               | Requirements                                               |  |
|----------------------------------------------------------|------------------------------------------------------------|--|
| Single-ended impedance requirements                      | $50\Omega \pm 10\%$                                        |  |
| Equal length requirements between DATA/CMD and CLK       | Less than 120mil                                           |  |
|                                                          | When CLK is less than or equal to 50MHz, less than         |  |
| Total length requirement of PCB trace                    | 6000mil;When CLK is greater than 50MHz, less than          |  |
|                                                          | 4000mil                                                    |  |
| Gap requirements between SDMMCx signals                  | >=2 times the trace width                                  |  |
| Gap requirements between SDMMCx signal and other signals | >=3 times the trace width                                  |  |
| Layer change vias                                        | If it is less than 4, symmetrical stitching vias should be |  |
|                                                          | placed close to the signal layer change via                |  |
| SDMMCx CLK routing requirements                          | It must be surrounded by ground in the whole process,      |  |
|                                                          | and there must be ground vias within 300 mils of the       |  |
|                                                          | ground trace interval.                                     |  |

 $T_{1} = 2 22 \text{ SDND} (C_{0}/1/2)$ 

Other points for attention:

- In the overall layout, place SDMMC as close to RK3568 as possible to shorten the trace as much as possible.
- The reference layer of all SDMMCx signals needs to be a complete ground plane to avoid continuous vias blocking the return path of signals.
- The SDMMCx CLK series matching resistor is close to CPU, and the trace between CPU pin and the resistor must be controlled within 400mil.
- The VCCIOx power domain where SDMMCx is located is 12mil or more, and the decoupling capacitor must be placed on the back of the corresponding power pin.
- When a card is used, the power capacitor of the card socket must be placed at the power pin of the card socket, and the trace must pass through the capacitor first and then go to the card socket pin. The power trace of the card socket must be 40mil or more; the TVS protection diode of the Micro-SD should be placed as close as possible to the card socket. The signal topology is: Micro-SD card socket --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device first; There should not be stubs on the TVS device trace; the ground pins of TVS are recommended to add ground vias as much as possible, and at least two 0.4\*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capacity; try to avoid routing in the area under the Micro-SD card socket to avoid coupling when ESD phenomenon occurs.

#### 3.2.6 SARADC/OTP Interface Circuit PCB Design

- The 1nF capacitors of SARADC\_VIN0/1/2/3/4/5/6/7 are jitter elimination capacitors, which should be placed as close to the pins of chipset as possible during layout.
- The decoupling capacitor of SARADC\_AVDD\_1V8 must be placed on the back of the corresponding power pin.
- Keep SARADC\_VIN0/1/2/3/4/5/6/7 signals away from digital signals such as LCD and DRAM. Do not rout on the neighboring layers of high-speed signal; do not placing layer change vias near high-speed signals; do not rout through the inductive area.
- If there are buttons, the TVS tube must be placed close to the button. The signal topology is: button --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be stubs on the TVS device trace
- It is recommended to increase ground vias as much as possible for the ground pins of TVS, at least two 0.4\*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

#### 3.2.7 USB2.0 Interface Circuit PCB Design

| Parameters                            | Requirements                                          |  |
|---------------------------------------|-------------------------------------------------------|--|
| Differential trace impedance          | $90\Omega \pm 10\%$                                   |  |
| requirements                          | 9022-1070                                             |  |
| Equal length requirements between     | Less than 20mil                                       |  |
| DP/DM                                 |                                                       |  |
| Total length requirement of PCB trace | Less than 6000mil                                     |  |
|                                       | If they are less than 4, symmetrical stitching vias   |  |
| Layer change vias                     | should be placed close to the signal layer change via |  |

Table 3-24 USB2.0 signal impedance and layout requirements

- In the overall layout, place the USB connector as close to RK3568 as possible to shorten the trace as much as possible.
- The USB3\_AVDD\_0V9/1V8/3V3 power supply and USB2\_AVDD\_0V9/1V8/3V3 decoupling capacitors must be placed on the back of the corresponding power supply pins.
- When the USB differential signal traces need to change layers, ensure that the number of vias on the traces is less than 4(6 at most), and place symmetrical stitching vias close to the signal layer change vias, and ensure that the center distance between the stitching vias and the signal vias should not exceed 30mil
- As far as possible, the reference layer of the USB differential pair should be a complete ground plane. If it is impossible to avoid routing across different planes, it must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval.

#### 3.2.8 USB3.0 Interface Circuit PCB Design

| Parameters                            | Requirements                                           |
|---------------------------------------|--------------------------------------------------------|
| Differential trace impedance          | $90\Omega \pm 10\%$                                    |
| requirements                          | 9052 ±1070                                             |
| Equal length requirements between     | Less than 12mil                                        |
| SSTXP/SSTXN                           |                                                        |
| Equal length requirements between     | Less than 12mil                                        |
| SSRXP/SSRXN                           |                                                        |
| Equal length requirements between     | Less than 6000mil                                      |
| SSTXP/N and SSRXP/N                   |                                                        |
| Total length requirement of PCB trace | Less than 6000mil                                      |
| Gap requirements between SSTX and     | >=4 times the trace width                              |
| SSRX signals                          | >-4 times the trace width                              |
| SSTX, SSRX signal and other signal    | >=4 times the trace width                              |
| gap requirements                      | -4 unies the trace width                               |
| Layer change vias                     | If they are less than 2, symmetrical stitching vias    |
|                                       | should be placed close to the signal layer change vias |

Table 3-25 USB3.0 signal impedance and layout requirements

- In the overall layout, place the USB connector as close to RK3568 as possible to shorten the trace as much as possible.
- The decoupling capacitor of MULTI\_PHY\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout SSTXP/N and SSRXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of SSTXP/N and SSRXP/N signals should be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the USB connector
- An empty space must be reserved below the USB3 connector pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty space should not be less than the size of the package pad.

## **RK3568 Hardware Design Guide**

Figure 3-62 Schematic diagram of empty space below the pad of USB3 connector and the pad of AC coupling capacitor

If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure below. 

| U X      | e                                                                   |  |
|----------|---------------------------------------------------------------------|--|
| D+<br>D- | High & <sub>r</sub> (over glass)<br>Low & <sub>r</sub> (over epoxy) |  |
| D+<br>D- | High & <sub>r</sub> (over glass)<br>Low & <sub>r</sub> (over epoxy) |  |

Figure 3-63 PCB fiberweave effect to improve routing way

## 3.2.9 SATA3.0 Interface Circuit PCB Design

| Parameters                                                | Requirements                                                                             |  |
|-----------------------------------------------------------|------------------------------------------------------------------------------------------|--|
| Differential trace impedance requirements                 | $100\Omega\pm10\%$                                                                       |  |
| Equal length requirements between TXP/TXN                 | Less than 12mil                                                                          |  |
| Equal length requirements between RXP/RXN                 | Less than 12mil                                                                          |  |
| Total length requirement of PCB trace                     | Less than 6000mil                                                                        |  |
| Gap requirements between TX and RX signals                | >=4 times the trace width                                                                |  |
| Gap requirements between TX, RX signals and other signals | >=4 times the trace width                                                                |  |
| Layer change vias                                         | If they are less than 2, symmetrical stitching vias should be placed close to the signal |  |
|                                                           | layer change via                                                                         |  |

- In the overall layout, the SATA connector should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The decoupling capacitor of MULTI\_PHY\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N and RXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N and RXP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the SATA connector
- An empty space must be reserved below the SATA connector pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

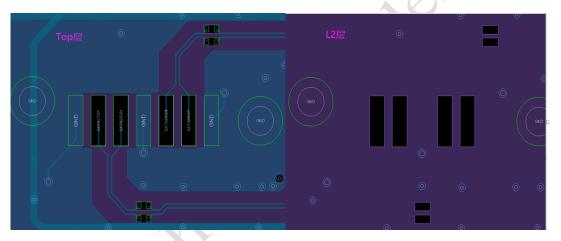


Figure 3-64 Schematic diagram of empty space below the pad of SATA connector and the pad of AC coupling capacitor

If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure3–63.

## 3.2.10 QSGMII/SGMII Interface Circuit PCB Design

| Parameters                        | Requirements         |
|-----------------------------------|----------------------|
| Differential trace impedance      | $100\Omega \pm 10\%$ |
| requirements                      | 10052 ±10 %          |
| Equal length requirements between | Less than 12mil      |
| TXP/TXN                           | Less than 12mi       |
| Equal length requirements between | Less than 12mil      |
| RXP/RXN                           | Less than 12mm       |

## Table 3-27 QSGMII/SGMII signal impedance and layout requirements

#### **RK3568 Hardware Design Guide**

| Parameters                            | Requirements                                           |  |
|---------------------------------------|--------------------------------------------------------|--|
| Total length requirement of PCB trace | Less than 6000mil                                      |  |
| Gap requirements between TX and RX    | >=4 times the trace width                              |  |
| signals                               | -4 times the trace width                               |  |
| Gap requirements between TX, RX       | >=4 times the trace width                              |  |
| signals and other signals             | >-4 times the trace width                              |  |
| I and the second second               | If they are less than 2, symmetrical stitching vias    |  |
| Layer change vias                     | should be placed close to the signal layer change vias |  |

- In the overall layout, the QSGMII/SGMII PHY connectors should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of MULTI\_PHY\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N and RXP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N and RXP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the PHY chip.
- An empty layer must be reserved below the QSGMII/SGMII PHY signal pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.
- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure3–63.

## 3.2.11 PCIe2.0 Interface Circuit PCB Design

| Parameters                                      | Requirements       |
|-------------------------------------------------|--------------------|
| Date differential trace impedance requirements  | $85\Omega\pm10\%$  |
| Clock differential trace impedance requirements | $100\Omega\pm10\%$ |
| Equal length requirements between TXP/TXN       | Less than 12mil    |
| Equal length requirements between RXP/RXN       | Less than 12mil    |
| Equal length requirements between REFCLKP/CLKN  | Less than 12mil    |

Table 3–28 PCIe2.0 signal impedance and layout requirements

| Parameters                                            | Requirements                                                                                                                            |
|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Total length requirement of PCB trace                 | Less than 6000mil                                                                                                                       |
| Equal length requirements between TX<br>and RX traces | Less than 6000mil                                                                                                                       |
| Gap requirements between TX and RX signals            | >=4 times the trace width                                                                                                               |
| Gap requirements between TX and RX signals            | >=4 times the trace width                                                                                                               |
| REFCLKP/N differential routing requirements           | It must be surrounded by ground in the whole process,<br>and there must be ground vias within 300 mils of the<br>ground trace interval. |
| Layer change via                                      | If it is less than 2, symmetrical stitching vias should be<br>placed close to the signal layer change via                               |

- In the overall layout, the PCIe Slot should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of MULTI\_PHY\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N, RXP/N, REFCLKP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, Try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N, RXP/N, REFCLKP/N signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- Please place AC coupling capacitors symmetrically and close to the PCIe Slot.
- An empty space must be reserved below the Slot pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

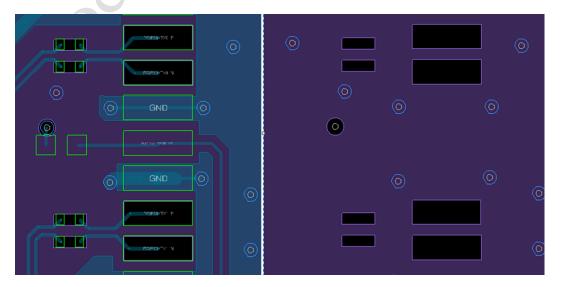


Figure 3-65 Schematic diagram of empty space below the pad of PCIe Slot and the pad of AC coupling capacitorCopyright © 2022 Rockchip Electronics Co., Ltd.205

#### **RK3568 Hardware Design Guide**

If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure 3–63.

#### 3.2.12 PCIe3.0 Interface Crcuit PCB Design

| Parameters                                            | Requirements                                                                                                                            |
|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Date differential trace impedance requirements        | $85\Omega\pm10\%$                                                                                                                       |
| Clock differential trace impedance requirements       | $100\Omega \pm 10\%$                                                                                                                    |
| Equal length requirements between TXP/TXN             | Less than 12mil                                                                                                                         |
| Equal length requirements between RXP/RXN             | Less than 12mil                                                                                                                         |
| Equal length requirements between<br>REFCLKP/CLKN     | Less than 12mil                                                                                                                         |
| Total length requirement of PCB trace                 | Less than 6000mil                                                                                                                       |
| Equal length requirements between TX<br>and RX traces | Less than 6000mil                                                                                                                       |
| Gap requirements between TX and RX signals            | >=5 times trace width                                                                                                                   |
| Gap requirements between TX and RX signals            | >=5 times trace width                                                                                                                   |
| REFCLKP/N differential routing requirements           | It must be surrounded by ground in the whole process,<br>and there must be ground vias within 300 mils of the<br>ground trace interval. |
| Layer change vias                                     | If they are less than 2, symmetrical stitching vias<br>should be placed close to the signal layer change via                            |

| Table 3–29 PCIe3.0       | signal | imnedance and   | lavout rec | uirements |
|--------------------------|--------|-----------------|------------|-----------|
| $14010 \ 3-271 \ 0103.0$ | Signal | information and | layout Icc | uncincins |

- In the overall layout, the PCIe Slot should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible
- The decoupling capacitor of PCIE30\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Try to rout TXP/N, RXP/N, REFCLKP/N on the TOP layer. When changing layers is needed, no more than 2 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30mil, try to use arcs or obtuse angles for routing corners instead of right angles or acute angles.
- The reference layer of TXP/N, RXP/N, REFCLKP/N signals needs to be a complete ground plane to

avoid continuous vias blocking the return path of the signal.

- Please place AC coupling capacitors symmetrically and close to the PCIe Slot.
- An empty layer must reserve below the Slot pad and the AC coupling capacitor pad to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad as shown in the figure 3–56
- If there is a long-distance trace, it is recommended to consider the PCB fiberweave effect. Try to avoid long-distance trace in one direction as far as possible. It is recommended to change to a 10 degree rotating trace, as shown in the figure 3–63.

#### 3.2.13 MIPI CSI RX Interface Circuit PCB Design

| Parameters                            | Requirements                                           |  |
|---------------------------------------|--------------------------------------------------------|--|
| Differential trace impedance          | $100\Omega \pm 10\%$                                   |  |
| requirements                          | 10022 ±10%                                             |  |
| Equal length requirements within a    | Less than 12mil                                        |  |
| differential pair                     |                                                        |  |
| Equal length requirements between     | Less than 36mil                                        |  |
| differential pairs                    |                                                        |  |
| Total length requirement of PCB trace | Less than 6000mil                                      |  |
| Gap requirements between MIPI         | >=3 times the trace width                              |  |
| signals                               |                                                        |  |
| Gap requirements between MIPI         | >=3 times the trace width                              |  |
| signals and other signals             |                                                        |  |
|                                       | If they are less than 4, symmetrical stitching vias    |  |
| Layer change vias                     | should be placed close to the signal layer change vias |  |

Table 3–30 MIPI CSI RX signal impedance and layout requirements

- In the overall layout, the MIPI CSI device should be placed as close as possible to RK3568, and the trace should be shortened as much as possible.
- The decoupling capacitor of MIPI\_CSI\_RX\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimize the layer-changing vias. When layer-changing is needed, no more than 4 vias, and place symmetrical stitching vias close to the signal vias. The center distance between stitching vias and signal vias should not exceed 30 mils.
- The reference layer of the MIPI CSI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

| Parameters                                                         | Requirements                                                                                                                            |
|--------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Single-ended trace impedance requirements                          | $50\Omega \pm 10\%$                                                                                                                     |
| Equal length requirements between all<br>CIF signals and CIF CLKIN | Less than 180mil                                                                                                                        |
| Total length requirement of PCB trace                              | Less than 5000mil                                                                                                                       |
| Gap requirements between CIF signals                               | >=2 times the trace width                                                                                                               |
| Gap requirements between CIF signal and other signals              | >=3 times the trace width                                                                                                               |
| CIF CLKIN Routing requirements                                     | It must be surrounded by ground in the whole process,<br>and there must be ground vias within 300 mils of the<br>ground trace interval. |

Table 3-31 CIF signal impedance and layout requirements

- In the overall layout, the CIF device should be placed as close as possible to RK3568, and the trace should be shortened as much as possible.
- The reference layer of all CIF signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The 22ohm series matching resistor of CIF CLKIN is close to the device, and the trace between the pin and resistor of the device end must be controlled within 400mil
- The decoupling capacitor of VCCIO6 must be placed on the back of the corresponding power pin.

## 3.2.15 MIPI DSI TX Interface Circuit PCB Design

Table 3-32 MIPI DSI TX signal impedance and layout requirements

| Parameters                                              | Requirements                                                                                                  |  |
|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--|
| Differential trace impedance requirements               | $100\Omega \pm 10\%$                                                                                          |  |
| Equal length requirements within the differential pair  | Less than 12mil                                                                                               |  |
| Equal length requirements between differential pairs    | Less than 36mil                                                                                               |  |
| Total length requirement of PCB trace                   | Less than 6000mil                                                                                             |  |
| Gap requirements between MIPI signals                   | >=3 times the trace width                                                                                     |  |
| Gap requirements between MIPI signals and other signals | >=3 times the trace width                                                                                     |  |
| Layer change vias                                       | If they are less than 4, symmetrical stitching vias<br>should be placed close to the signal layer change vias |  |

In the overall layout, the MIPI DSI device should be placed as close to RK3568 as possible, and the trace Copyright © 2022 Rockchip Electronics Co., Ltd.

should be shortened as much as possible.

- The decoupling capacitor of MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- The decoupling capacitor of MIPI\_DSI\_TX1\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of the MIPI differential pair. When layer-changing is needed, no more than 4 vias, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the MIPI DSI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

## 3.2.16 LVDS TX Interface Circuit PCB Design

| Parameters                                             | Requirements                                                                                                  |
|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| Differential trace impedance requirements              | $100\Omega \pm 10\%$                                                                                          |
| Equal length requirements within the differential pair | Less than 20mil                                                                                               |
| Equal length requirements between differential pairs   | Less than 60mil                                                                                               |
| Total length requirement of PCB trace                  | Less than 6000mil                                                                                             |
| Gap requirements between LVDS signals                  | >=3 times the trace width                                                                                     |
| Gap requirements between LVDS signal and other signal  | >=3 times the trace width                                                                                     |
| Layer change vias                                      | If they are less than 4, symmetrical stitching vias<br>should be placed close to the signal layer change vias |

Table 3–33 LVDS TX signal impedance and layout requirements

- In the overall layout, place the LVDS device as close as possible to RK3568 to shorten the trace as much as possible.
- The decoupling capacitor of MIPI\_DSI\_TX0/LVDS\_TX0\_AVDD\_0V9/1V8 power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of LVDS differential pair. When layer-changing is needed, no more than 4 vias and 6 at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the LVDS differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal.

| Parameters                                             | Requirements                                                                                                  |
|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|
| Differential trace impedance requirements              | $100\Omega \pm 10\%$                                                                                          |
| Equal length requirements within the differential pair | Less than 12mil                                                                                               |
| Total length requirement of PCB trace                  | Less than 6000mil                                                                                             |
| Gap requirements between eDP signals                   | >=4 times the trace width                                                                                     |
| Gap requirements between eDP signal and other signals  | >=4 times the trace width                                                                                     |
| Layer change vias                                      | If they are less than 4, symmetrical stitching vias<br>should be placed close to the signal layer change vias |

Table 3-34 eDP TX signal impedance and layout requirements

- In the overall layout, place the eDP device as close as possible to RK3568 to shorten the trace as much as possible.
- The decoupling capacitor of eDP\_TX\_AVDD\_0V9/1.8V power supply must be placed on the back of the corresponding power supply pin.
- Minimizes the layer-changing vias of LVDS differential pair. When layer-changing is needed, no more than 4 vias and 6 at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30mil
- The reference layer of the eDP\_TX differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

# 3.2.18 HDMI TX Interface Circuit PCB Design

Table 3–35 HDMI TX signal impedance and layout requirements

| Parameters                                             | Requirements                                                                                               |
|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| Differential trace impedance requirements              | $100\Omega \pm 10\%$                                                                                       |
| Equal length requirements within the differential pair | Less than 12mil                                                                                            |
| Equal length requirements between clock and data       | Less than 480mil                                                                                           |
| Total length requirement of PCB trace                  | Less than 6000mil                                                                                          |
| Gap requirements between HDMI data signals             | >=4 times the trace width                                                                                  |
| Gap requirements between HDMI data and HDMI clock      | >=5 times the trace width                                                                                  |
| Layer change vias                                      | If they are less than 2, symmetrical stitching vias should be placed close to the signal layer change vias |

■ In the overall layout, the HDMI socket should be placed as close as possible to RK3568, and the trace

should be shortened as much as possible.

- HDMI TX AVDD 0V9/1V8 power decoupling capacitors must be placed on the back of the corresponding power pins.
- The trace should be on the top layer as much as possible. When layer changing is needed, drill 2 vias at most, and symmetrical stitching vias should be placed close to the signal vias. The center distance between the stitching vias and the signal vias should not exceed 30 mils. Try to use arcs or obtuse angles, instead of right angles or acute angles.
- The whole group of differential traces are routed in parallel and surrounded by ground and the gap between the ground trace and the signal is greater than or equal to 4 times the line width, and there must be ground vias within 300 mils of the ground trace interval.
- The reference layer of all signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- An empty layer should be reserved below the pad of the HDMI socket and the pad of the TVS tube to ensure the continuity of impedance. The size of the empty layer should not be less than the size of the package pad.

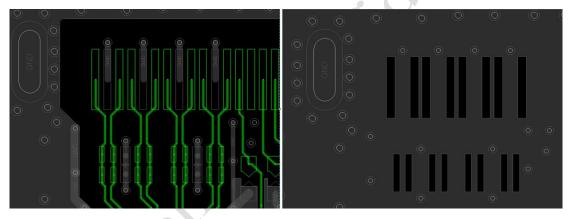


Figure 3-66 Schematic diagram of empty space below the pad of HDMI connector and the pad of TVS diode

The HDMI TVS tube should be placed as close as possible to the connector. The signal topology is: HDMI connector --->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be Stub on the TVS device trace. It is recommended to increase the ground vias as much as possible for the ground pins of TVS, at least two 0.4\*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

## **3.2.19 RGB TX Interface Circuit PCB Design**

| Parameters                            | Requirements      |  |
|---------------------------------------|-------------------|--|
| Single-ended trace impedance          | $50\Omega\pm10\%$ |  |
| requirements                          | 5052 ± 10 / 0     |  |
| Equal length requirements between all | Less than 180mil  |  |
| LCDC signals and LCDC CLK             |                   |  |
| Total length requirement of PCB trace | Less than 5000mil |  |

| Gap requirements between LCDC signals                  | >=2 times the trace width                                                                                                               |  |
|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|--|
| Gap requirements between LCDC signal and other signals | >=3 times the trace width                                                                                                               |  |
| LCDC CLK routing requirements                          | It must be surrounded by ground in the whole process,<br>and there must be ground vias within 300 mils of the<br>ground trace interval. |  |

- In the overall layout, the LCDC device should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The 220hm series matching resistor of LCDC clk is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil
- The reference layer of all LCDC signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The decoupling capacitor of VCCIO5 must be placed on the back of the corresponding power pin.

## 3.2.20 BT1120 TX Interface Circuit PCB Design

| Parameters                            | Requirements                                          |
|---------------------------------------|-------------------------------------------------------|
| Single-ended trace impedance          | $50\Omega \pm 10\%$                                   |
| requirements                          | 3052 ±10%                                             |
| Equal length requirements between all | Less than 180mil                                      |
| BT1120 signals and BT1120 CLK         |                                                       |
| Total length requirement of PCB trace | Less than 5000mil                                     |
| Gap requirements between BT1120       | >=2 times the trace width                             |
| signals                               |                                                       |
| Gap requirements between BT1120       | >=3 times the trace width                             |
| signal and other signals              |                                                       |
|                                       | It must be surrounded by ground in the whole process, |
| BT1120 CLK routing requirements       | and there must be ground vias within 300 mils of the  |
|                                       | ground trace interval.                                |

Table 3–37 BT1120 TX signal impedance and layout requirements

- In the overall layout, the BT1120 TX device should be placed as close to RK3568 as possible, and the trace should be shortened as much as possible.
- The 22ohm series matching resistor of BT1120 CLK is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil
- The reference layer of all BT1120 signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- The decoupling capacitor of VCCIO5 must be placed on the back of the corresponding power pin.

# 3.2.21 Audio Interface Circuit PCB Design

- The LC device of RK809-5 SPK is placed close to RK809
- The VCC\_SPK\_HP trace of RK809-5 is greater than 50mil.
- SPKP/SPKN follow the differential routing and surrounded by ground in the whole group, with 20mil trace width, and the trace should be shortened as much as possible.
- The left and right channels of HP\_L/HP\_R should be surrounded by ground separately. If they are not differential lines, they cannot be close together. Otherwise it will reduce the isolation of the left and right channels. It is recommended that the line width be greater than 10mil.
- The HP\_SNS network series resistor must be connected to the ground at the pin of the headphone socket to compensate the input and improve the isolation between the left and right channels

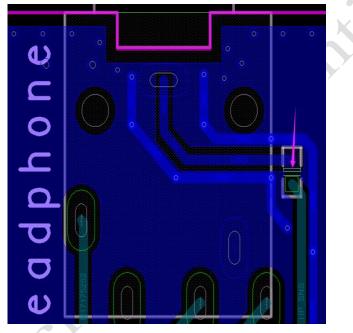


Figure 3-67 RK809-5 HP\_SNS resistor layout and routing

HP\_SNS is used as the accompanying ground of HPL/HPR, routing in groups and surrounded by ground in parallel, the trace width of HPL/HPR should not exceed 10mil



Figure 3-68 RK809-5 HPL/HPR/HP\_SNS routing

- When MIC single-ended connection, MIC1/MIC2 routing separately and are surrounded by ground separately.
- When MIC is differential connection, the MCP/MICN should follow differential routing and the whole group is surrounded by ground.
- MIC trace width is recommended to be more than 8mil
- Keep all audio signals away from high-speed signal lines such as LCD and DRAM. It is forbidden to rout on neighboring layers of high-speed signal traces, and the neighboring layers must be ground planes; it is forbidden to drill layer change vias near high-speed signal traces; do not pass through inductance areas and keep away from RF signals and devices.
- All neighboring layers of audio signals must not be power planes or traces.
- The TVS protection diode of the earphone socket/microphone should be placed as close as possible to the connection socket. The signal topology is: earphone socket/microphone--->TVS--->CPU; when ESD occurs, the ESD current must be attenuated by the TVS device; there should not be stubs on the TVS device traces. It is recommended to increase the ground vias as much as possible for the ground pins of TVS, and at least two 0.4\*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capacity.
- S/PDIF signal is recommended to be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the trace interval of the ground.

## 3.2.22 GMAC Interface Circuit PCB Design

#### 3.2.22.1 RGMII interface

| Parameters                                                                 | Requirements                                                                                                                            |
|----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Single-ended trace impedance requirements                                  | $50\Omega \pm 10\%$                                                                                                                     |
| Equal length requirements between<br>TXD0,TXD1,TXD2,TXD3,TXEN<br>and TXCLK | Less than 120mil                                                                                                                        |
| Equal length requirements between RXD0,RXD1,RXD2,RXD3,RXDV and RXCLK       | Less than 120mil                                                                                                                        |
| Total length requirement of PCB trace                                      | Less than 5000mil                                                                                                                       |
| Gap requirements between RGMII signals                                     | >=2 times the trace width                                                                                                               |
| Gap requirements between RGMII signal and other signals                    | >=3 times the trace width                                                                                                               |
| TXCLK and RXCLK routing requirements                                       | It must be surrounded by ground in the whole process,<br>and there must be ground vias within 300 mils of the<br>ground trace interval. |

#### Table 3–38 RGMII signal impedance and layout requirements

Copyright © 2022 Rockchip Electronics Co., Ltd.

214

| Table 3–39 RMII signal | impedance and | layout requirements |
|------------------------|---------------|---------------------|
|                        | 1             | 2 1                 |

| Parameters                                | Requirements                                  |  |
|-------------------------------------------|-----------------------------------------------|--|
| Single-ended trace impedance requirements | $50\Omega\pm10\%$                             |  |
| Equal length requirements between TXD0,   |                                               |  |
| TXD1, TXEN, RXD0, RXD1, RXDV, RXER        | Less than 300mil                              |  |
| and MCLKINOUT                             |                                               |  |
| Total length requirement of PCB trace     | Less than 5000mil                             |  |
| Gap requirements between RGMII signals    | >=2 times the trace width                     |  |
| Gap requirements between RGMII signal and | >=3 times the trace width                     |  |
| other signals                             |                                               |  |
|                                           | It must be surrounded by ground in the whole  |  |
| MCLKINOUT routing requirements            | process, and there must be ground vias within |  |
|                                           | 300 mils of the ground trace interval.        |  |

- In the overall layout, place GEPHY or FEPHY as close to RK3568 as possible to shorten the trace as much as possible.
- The 22ohm series matching resistance of TXD0-TXD3, TXCLK, TXEN is close to the CPU (source end), and the trace between CPU pin and the resistor must be controlled within 400mil.
- The 22ohm series matching resistors of RXD0-RXD3, RXCLK, and RXDV are close to the PHY end, and the trace between the PHY pin and the resistor must be controlled within 400mil.
- The 22ohm series matching resistor of ETH0\_REFCLKO\_25M and ETH1\_REFCLKO\_25M is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil.
- ETH0\_REFCLKO\_25M, ETH1\_REFCLKO\_25MIt must be surrounded by ground in the whole process, and there must be ground vias within 300 mils of the ground trace interval.
- RMII MCLKINOUT output mode: The 22ohm series matching resistor is close to the CPU (source end), and the trace between the CPU pin and the resistor must be controlled within 400mil.
- RMII MCLKINOUT input mode: The 22ohm series matching resistor is close to the PHY end, and the trace between the PHY pin and the resistor must be controlled within 400mil.
- The reference layer of all RGMII/RMII signals needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal

Take RTL8211F/FI as an example, the following items are attentions on the PHY side:

- Give priority to the layout of the crystal circuit, which should be on the same layer as the chip and placed as close as possible to avoid drilling vias. The crystal traces should be as short as possible, away from interference sources, and away from the edge of the board as far as possible.
- The crystal and clock signals need to be surrounded by ground throughout the whole process. At least one GND via is added to the ground trace every 100 mils, and the ground reference plane of the neighboring layer must be complete.
- Be sure to confirm whether the RJ45 package is consistent with the schematic. RJ45 has tab down and tab

up two types, and the signal sequence is just the opposite. If you use RTL8211F/FI, it is recommended to use Tab down, and the MDI sequence is direct.

- The network transformer should be as close to the RJ45 connector as possible, and the MDI trace should not exceed 4.5 inches
- The RSET resistor must be close to the pins of RTL8211F/FI, and the trace must not exceed 800mil, far away from other interference signals.
- The differential impedance of MDI differential signal from PHY to the network transformer is  $100\Omega \pm 10\%$ .
- For the differential signals from PHY to the network transformer: MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-, their length deviation in the differential pair is controlled within ±5mil, and the MDI differential pair strictly follows the differential rules for routing. For example, keep the same length, the same width, the same layer and fixed trace spacing, and keep as symmetrical as possible
- The trace length delay between MDI differential pairs is controlled within 800 mils.
- Gap between MDI0/1/2/3: >=3 times the line width
- Gap between MDI0/1/2/3 and other signals:  $\geq$ =4 times the line width.
- Minimizes layer-changing vias on MDI. When layer-changing is unavoidable, two vias at most, and symmetrical ground stitching vias are placed near the signal vias.
- The reference layer of the MDI differential pair needs to be a complete ground plane to avoid continuous vias blocking the return path of the signal
- For the MDI differential pair on the high-voltage side of the network transformer, the trace width is recommended to be as thick as possible, and 8mil is recommended
- It is recommended that the 75 ohm resistor trace on the high voltage side of the network transformer be more than 25 mil.
- The center filter capacitor of the network transformer must be close to the corresponding pin of the network transformer
- The decoupling capacitors of PHY chip power supply should be placed as close as possible to the pins of PHY chip. When routing, try to pass the capacitor pads first, and then to the chip pins. The length of the trace between the pins and the capacitor should not exceed 100mil
- For the internal DCDC of RTL8211F/FI, the inductor must be close to the chip pins. The LX trace should be as short and thick as possible, the width should not be less than 60mil, and the length should not exceed 200mil. The output capacitor must be close to the inductor, the trace must pass through the output capacitor first and then to the latter stage. PiN21 and Pin3, 8, 38 must be routed separately in a star shape, and the width of the trace should be more than 30mil
- If the PHY IO is 3.3V, the VCCIO\_PHY and VCC3V3\_PHY power supply lines must be star-shaped, and the line width should be more than 30mil
- The center pad of PHY chip must be well grounded, and the vias must be placed at least 5X5 piece of 0.5\*0.3mm vias
- The grounding of the anti-lightning diode must be well grounded. It is recommended that no less than 3X3 piece of 0.5\*0.3mm vias are provided, otherwise the effect of the anti-lightning diode will be

reduced

- Related components on the high-voltage side of the network transformer must be far away from the main ground of the PCB board
- The RJ45 interface and the high-voltage side of the network transformer belong to the high-voltage area, and copper-covering is forbidden. It is recommended to be separated from the low-voltage area by at least 4mm

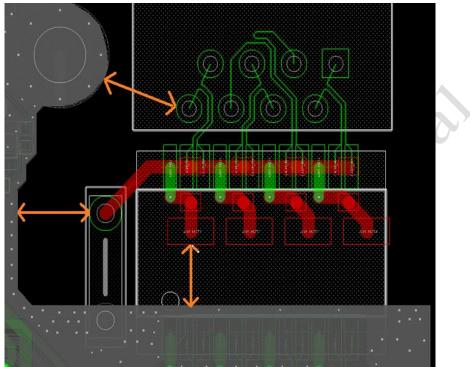


Figure 3-69 Schematic diagram of prohibited routing area for RJ45 interface and network transformer

If possible, it is recommended to open a creepage of more than 1mm under the network transformer to strengthen the anti-surge capability.

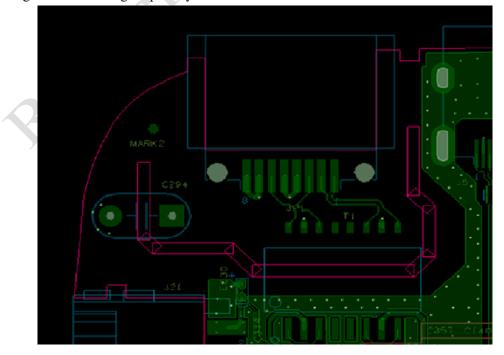


Figure 3-70 Schematic diagram of RJ45 interface and network transformer slotting

#### *RK3568 Hardware Design Guide* 3.2.23 WIFI/BT PCB Design

- In the overall layout, the WIFI module should be properly placed, and the module should be far away from DDR, HDMI, USB, LCD circuits, speakers and other easily interfered modules or connectors.
- No trace is allowed on the TOP layer below the module. Make sure that the reference plane is a complete ground plane. It is recommended that SDIO/PCIe/UART/PCM signal trace bypass the projection area of the module and connect to the module pins.
- Give priority to the crystal circuit layout which should be on the same layer as the chip and placed as close as possible to avoid vias. The crystal traces should be as short as possible, away from interference sources and antenna area as far as possible.
- The crystal and clock signals need to be surrounded by ground throughout the whole process. At least one GND via is added to the ground trace every 100 mils, and the ground reference plane of the neighboring layer must be complete.
- If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground all the way to avoid interference.
- 32.768k is routed separately and surrounded by ground, and at least one GND via is added every 400 mil for the ground trace
- For SDIO WIFI, please refer to chapter 3.2.5 requirements for PCB design requirements of SDIO signal
- For PCIe WIFI, please refer to chapter 3.2.11 or 3.2.12 for PCIe signal PCB design requirements
- When layout the inductance of the module, please note that after the trace comes out through the inductance, it passes through the capacitor first, and then enters the module power pin

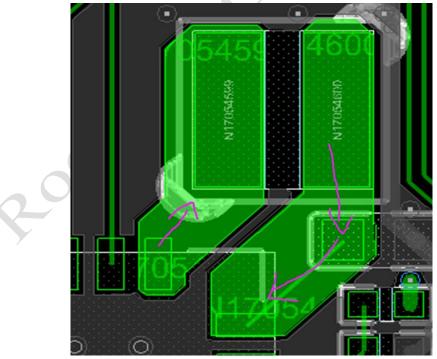


Figure 3-71 Schematic diagram of inductance and capacitance of the WIFI module routing

- The power decoupling capacitor of the module must be close to the power pin of the module
- The width of the VBAT pin trace of the module must be greater than 40mil
- The longer the antenna trace, the greater the energy loss. Therefore, in the design, the antenna path should

be as short as possible. There should be no branches, and try not to change layers.

The antenna matching circuit must be close to the antenna connector, and the antenna trace must be 50 ohms to ensure that the reference ground is complete, the impedance does not change suddenly, and no other signal traces or power sources are allowed below; the accompanying ground of the trace needs to be connected to the main ground reference plane by ground wall.

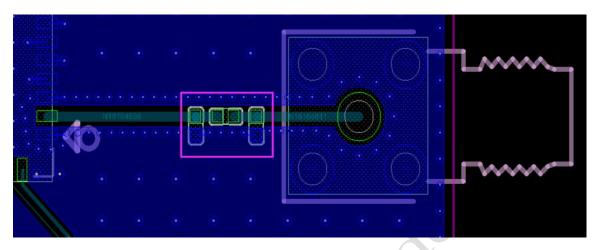


Figure 3-72 Schematic diagram of WIFI module antenna routing

- The antenna of the module and all layers below the antenna routing area are not allowed to other signal traces or power sources
- If it is a 2X2 MIMO antenna interface, the exit direction between the two antenna ports has to consider the location of the two antennas where should be as far away as possible to avoid interference, and vertical placement is recommended to avoid mutual interference

#### 3.2.24 VGA OUT PCB Design

- In the overall layout, the VGA connector should be placed as close to the conversion chip as possible, and the VGA analog signal trace should be shortened as much as possible.
- The decoupling capacitors for the power supply of the conversion chip should be placed as close as possible to the power supply pins of the conversion chip.
- The VGA\_R/G/B trace width should be as thick as possible, and it is recommended to be more than 12mil.
- The length difference between VGA R/G/B must not exceed 200mil
- VGA\_R/G/B 750hm resistor must be placed close to the chip
- The VGA\_R/G/B filter circuit must be placed close to the VGA connector
- VGA\_R/G/B signals are required to be surrounded by ground separately in the whole process, and there must be ground vias within 300 mils of the ground traces.
- The neighboring layer of VGA\_R/G/B signal must be ground plane instead of power plane
- Keep VGA\_R/G/B signals away from high-speed signal lines such as LCD, DRAM, etc. It is forbidden to route on the neighboring layers of high-speed signal trace; it is forbidden to drill vias to change layers near high-speed signal traces; do not route through inductance areas; keep away from RF signals and devices.

- The RC filter of VGA\_HSYNC/VSYNC must be placed close to VGA connector, and the trace must not exceed 6 inches
- All signal TVS diode of VGA connector should be placed as close as possible to the connector. The signal topology is: VGA socket--->TVS--->chip pins; when an ESD phenomenon occurs, the ESD current must be attenuated by the TVS device first; There should not be stubs on the TVS device trace.
- It is recommended to increase the ground vias as much as possible for the ground pins of TVS, at least two 0.4\*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

#### 3.2.25 LCD Screen and Touch Screen PCB Design

- Please place the current limiting resistor on the FB side of the LED backlight IC close to the screen connector instead of DC-DC.
- For backlight boost circuit, please pay attention to capacitor placement and power supply trace to ensure that the power supply's charging and discharging loop is minimized.
- If there are reserved test points for the screen and touch screen connectors, they should be close to the connector and the stub on the trace should be as short as possible.

#### 3.2.26 Camera PCB Design

- When the camera is with a connector: when the MIPI differential signal passes through the connector, the GND pin must be used for isolation between neighboring differential signal pairs.
- For CIF/MIPI and other signals, if there is a board-to-board connection is realized through the connector, it is recommended that all signals be connected in series with a certain resistance (between 2.2ohm-10ohm as long as it can meet the SI test), and reserved TVS device.
- If the camera connector has reserved test points, it should be close to the connector and the stub on the trace should be as short as possible
- The decoupling capacitors of the AVDD/DOVDD/DVDD power supply of the connector should be placed as close to the camera connector as possible.
- The camera layout needs to be far away from high-power radiating devices, such as GSM antennas.
- Please refer to section 3.2.13 for MIPI CSI RX signal PCB design requirements
- Please refer to section 3.2.14 For CIF signal PCB design requirements

## **4 Thermal Design Suggestion**

Good thermal design is especially important for the improvement of RK3568 product performance, system stability, and product safety

## 4.1 Thermal Simulation Result

Aiming at RK3568 FCBGA636\_19x19mm\_Pitch 0.65mm package, the EVB which is based on 4 layer PCB and Finite Element Modeling (FEM) to obtain a thermal resistance simulation report. The report is based on JEDEC JESD51-2 standard. The system design and application environment may be different from JEDEC jesd51-2 standard, which needs to be analyzed according to actual application conditions.

# M Note

Thermal resistance is the reference value when there is no radiator on PCB. The detailed temperature is related to the board's size, thickness, material and other physical factors.

#### 4.1.1 Result Overview

Thermal resistance simulation results are as follows:

| Table 4-1 RK3568 thermal resistance | e simulation report results |
|-------------------------------------|-----------------------------|
|-------------------------------------|-----------------------------|

| Package<br>(EHS-FCBGA) | $	heta_{JA}(^{\circ}\mathbb{C}/W)$ | $	heta_{JB}(^{\circ}\mathbb{C}/W)$ | $\theta_{JC}(^{\circ}C/W)$ |
|------------------------|------------------------------------|------------------------------------|----------------------------|
| JEDEC PCB              | 15.925                             | 10.813                             | 0.487                      |

Note: The simulated data is only used for reference only.

#### 4.1.2 PCB Description

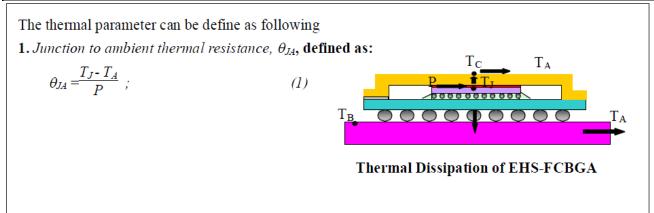
The PCB structure used for thermal resistance simulation is as follows:

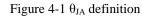
|         | PCB Dimension (L x W) | 114.3 x 101.6mm |  |
|---------|-----------------------|-----------------|--|
| EVB PCB | PCB Thickness         | 1.6mm           |  |
|         | Number of Cu Layer    | 4-layers        |  |

#### 4.1.3 Terms Interpretation

Terms in this chapter are explained below:

- TJ: The maximum junction temperature;
- T<sub>A</sub>: The ambient or environment temperature;
- T<sub>c</sub>: The maximum compound surface temperature;
- T<sub>B</sub>: The maximum surface temperature of PCB bottom;
- P: Total input power





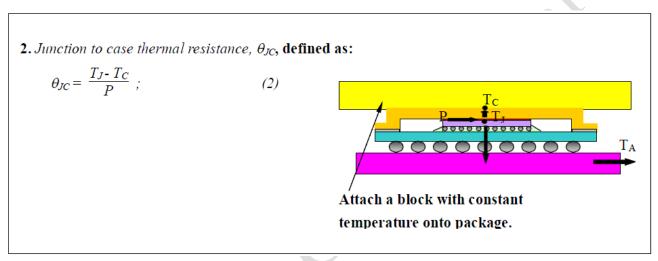


Figure 4-2  $\theta_{JC}$  definition

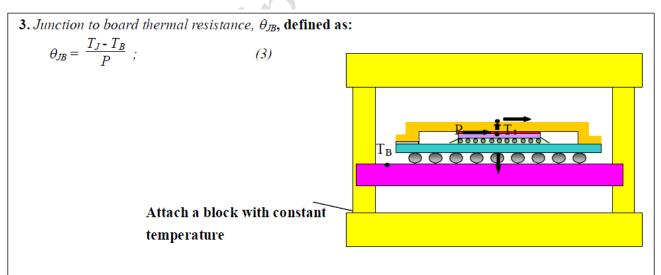


Figure 4-3  $\theta_{JB}$  definition

## 4.2 Thermal Control Method inside the Chip

#### 4.2.1 Thermal Control Strategy

In Linux kernel, it defines one thermal control frame called Linux Generic Thermal System Drivers, which can

control system temperature through different strategies. Currently below 3 strategies are commonly used:

- Power\_allocator: Introduce PID (percentage-integral-differential) control to dynamically allocate power for cooling device according to current temperature, when the temperature is low, the power that can be allocated is larger, that is, the frequency that can be operated is higher. As the temperature rises, the power that can be allocated is gradually reduced, and the frequency that can be operated is gradually reduced, so as to achieve the effect of limiting frequency according to temperature.
- Step\_wise: Limit frequency step by step according to current temperature.
- Fair share: The cooling devices with more frequency gears will give priority to frequency reduction
- Userspace: Do not limit frequency.

There is a T-sensor inside the RK3568 to detect the on-chip temperature, and the Power\_allocator strategy is used by default

#### 4.2.2 Temperature Control Configuration

RK3568 SDK can provide temperature control strategies for CPU and GPU separately, please refer to the document for detailed configurations: "Rockchip\_Developer\_Guide\_Thermal\_CN.pdf".

#### **4.3 Thermal Design Reference**

#### 4.3.1 Circuit Schematic Thermal Design Reference

- Under the condition of stability, provide overall power efficiency, such as using as less as high-voltage LDOs, and reduce the heat generated by the power supply itself during the power conversion process
- According to actual products, try not to supply power to the modules that are not used by the chip or do power down processing by software
- Choose a material with a large thermal conductivity, and re-estimate the size of the radiator to be used according to the "Calculation of Radiator Size" according to the product definition, usage environment and other conditions. It is recommended to use a larger radiator as much as possible

## 4.3.2 PCB Thermal Design Reference

For RK3568 products, RK3568 chip is the device that generates the most heat, so all heat dissipation treatments should be based on the chip.

Except RK3568, other main heating devices include: PMIC, charging IC and related inductors, backlight IC and related inductors.

- Reasonable structural design can ensure that there is a heat exchange path between the internal machine and air.
- In the overall layout, the components with high power consumption or heat generation should be uniformly distributed to avoid local overheating. It is recommended RK3568 and RK809-5 should be placed appropriately, not too close or too far away. It is recommended that the distance between the two is 20mm-50mm. Avoid to place them on the edge of the board, for bad heat dissipation.
- It is recommended to use a 6-layer board or more to increase the copper of the board as much as possible.

It is recommended to use a copper thickness of loz, and try to use much ground layers as possible. Other layers should follow the power and signal routing rules, and try to place as much ground copper as possible, with the help of a large area of copper for dissipates heat.

- RK3568 VDD LOGIC, VDD GPU, VDD NPU, VDD CPU, VCC DDR have relatively large currents, the routing or copper must meet the current-carrying capacity, otherwise it may increase the temperature rise
- For chips with EPAD, drill as many vias as possible on the EPAD, the neighboring layer must be a ground layer, and the copper on the back side should be as complete as possible. It is recommended that the copper on the back should be bare copper, which is good for heat dissipation.
- The GND pins of RK3568 chip is routed in "#" shape on the top layer and are cross-connected. It is recommended that the trace width is 10mil, which is beneficial to the heat dissipation of the chip.
- For the GND pin of RK3568 chip, it is recommended to try to ensure that each ball has a corresponding ground via. At least ensure that every 1.5 ball corresponds to one via to increase the heat conduction path. The neighboring layer must be a ground layer, which is good for heat dissipation of the chip.
- For decoupling capacitor ground pad on the back of RK3568 chip, it is recommended to use full copper covering, do not use flower holes to connect, try to make the ground copper as complete as possible to improve heat dissipation
- In empty areas, without damaging the power layer, try to increase ground vias and increase heat conduction paths to improve heat dissipation

# **5 ESD/EMI Protection Design**

## 5.1 Overview

This chapter provides ESD/EMI protection design suggestion for RK3568 product design to help customers to improve anti-static and anti-electromagnetic interference ability of product.

## **5.2 Terms Interpretation**

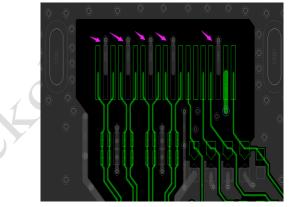
Terms of this chapter are explained as below:

- ESD: Electro-Static discharge;
- EMI: Electromagnetic Interference, including conduction interference and radiation interference

## **5.3 ESD Protection**

- Ensure reasonable mold design, retract connectors in the shell as much as possible, so that the distance from static electricity to the internal circuit becomes longer and the energy becomes weaker. The test standard changes from contact discharge conditions to air discharge, etc.
- Protect and isolate sensitive components in PCB layout.
- Try best to put the RK3568 and core components in the center of PCB layout. If it may not be able to put them in the center, ensure that the shielding cover has 2mm distance at least from the board edge and is connected to GND safely
- PCB layout is based on function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the parts that are easy to produce interference;
- Place ESD components reasonably. Generally place then near the source, that is, place ESD components in the junction or where electrostatic discharge.
- The layout of the components should be far away from the edge of the board and a certain distance from the connector
- The PCB surface should have a good GND loop, and each connector should be with good GND connection loop on the surface. If there is a shielding cover, it should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area;
- Do not go through the edge of surface layer and make as many ground vias as possible.
- Isolate signal from ground if necessary.
- Expose GND copper of PCB as much as possible, in order to strengthen the electrostatic discharge effect, or to facilitate to add foam and other remedial measures
- If there is a board-to-board connection through the connector, it is recommended that all signals be connected in series with a certain resistance (between 2.2ohm-10ohm, as long as it can meet the SI test), and reserved TVS devices, which can improve antistatic surge capacity

- The 100nF capacitor of the nPOR pin of RK3568 must be placed close to the pin, and the ground pad of the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.
- The distance between key signals such as Reset, clock, interrupt and other sensitive signals from the edge of the board should not be less than 5mm
- If other peripheral chips have Reset pins, it is recommended to add a 100nF capacitor close to the pin. The ground pad of the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.
- When the whole device is designed as a ground-floated device, it is recommended not to design each interface with separate ground.
- When the device casing is metal, with a three holes power, and the metal casing must be well connected to the ground.
- Reserve the shielding cover position. The shielding cover should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area.
- Isolate from PCB, so that static electricity can only be released in some areas, such as the ground pin of the connector is connected with the inner layer through a separate vias, keep out the surface PCB, and keep the surface ground copper and pins as far away as possible, that is, keep sensitive signals away from electrostatic discharge areas (surface copper), etc., as shown in the figure, isolate the distance between HDMI signal and GND on the surface.



# **5.4 EMI Protection**

- Electromagnetic interference has three factors: interference sources, coupling channels and sensitive devices. We have no way to deal with sensitive devices, so EMI problem can only start with interference sources and coupling channels. The best way to resolve EMI issues is to eliminate interference source. If it cannot eliminate, try to cut off coupling channels or avoid antenna effect.
- It is difficult to eliminate interference source on PCB. We can take actions such as filtering, grounding, balancing, resistance controlling, improving signal quality (e.g. termination connection) etc. Generally several methods will be applied together, but the basic requirement is good grounding.

• The commonly used EMI materials include shielding cover, special filter, resistor, capacitor, inductor, Copyright © 2022 Rockchip Electronics Co., Ltd. 226

magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread frequency device etc.

- The rules to select filters: if the load (receiver) is high resistance (regular single ended signal interface is high resistance, such as SDIO, RBG, CIF etc.), select capacitive filter components and parallel connect to circuit; if the load (receiver) is low resistance (such as power output interface), select inductive filter component and serial connect to circuit. After using the filter device, the signal quality cannot exceed its SI permission. Differential interface usually uses common mode choke to suppress EMI.
- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should comply with relevant technical standards.
- RK3568 spread spectrum function is divided into modules. The degree of spreading depends on the signal requirements of the relevant part. See RK3568 spreading instructions for detailed measures;
- Please don't delete the RC circuit between DDR3\_CLKP/N, DDR4\_CLKP/N, LPDDR3\_CLKP/N, which can improve EMI
- It is recommended to keep the matching resistance of all clocks connected in series, which will provide matching impedance, and improve the improvement measures of signal quality
- At the DC power input, the common mode inductance or EMI filter of the power supply can be reserved if possible
- Add reserved common mode inductance or filter circuit at USB, HDMI, VGA, screen connector and other interfaces
- When a radiator is added, it should be noted that the radiator may also couple EMI energy and generate radiation. When selecting a radiator, in addition to meeting the thermal design requirements, it should also meet the EMI test requirements. Grounding conditions should be reserved for the radiator. When grounding is required, the radiator should be grounded. It is not easy to clarify the number of grounding points and how to choose the grounding point. It needs to be adjusted according to the actual test of the first version of hardware in the laboratory.
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add the following requirements:
  - Try best to ensure the integrity of the signal;
  - Differential line should in equal length and be tight coupling to ensure the symmetry of the differential signal, minimize the misplacement of differential signals to avoid EMI problems caused by phase mismatch;
  - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from shell to other signal lines.
  - The matching resistors of all clocks connected in series should be placed close to CPU (source end), and traces between CPU pins and the resistors must be controlled within 400 mils.
  - If the PCB exceeds 4 layers, it is recommended that all clock signals go to the inner layer as much as possible
  - To prevent power radiation, the copper of the power supply layer must be retracted, with one H (the

#### **RK3568 Hardware Design Guide**

thickness of the medium between the power supply and ground) as the unit, and it is recommended to indented by 20H

contraction

## **6** Soldering Process

## 6.1 Overview

RK3568 are ROHS certified products, that is, they are all Lead-free products. This chapter regulates basic temperature settings of each period when customers use the chipset to SMT. It mainly introduces process control when using RK3568 chipset to do reflow soldering: lead-free process and mixed process.

## **6.2 Terms Interpretation**

Terms in this chapter are explained below:

- Lead-free: Lead-free process;
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and the lead-free solder paste are used in the pure lead-free process;
- Reflow profile: reflow soldering
- Restriction of Hazardous Substances (ROHS): instructions for restricting use of certain hazardous components in electrical and electronic equipment;
- Surface Mount Technology(SMT);
- Sn-Pb: Sn-Pb mixing process refers to using lead solder paste and a mixed soldering process with both lead-free BGA and lead IC;

## **6.3 Reflow Soldering Requirements**

#### 6.3.1 Solder Paste Composition Requirements

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10°C, it should be returned to normal temperature before use, and the return time should be 3~4 hours and the time should be recorded.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes. After stirring, it will flow naturally.

## 6.3.2 SMT Profile

Since RK3568 chipset are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020D process requirements, and customers need to adjust according to actual production conditions.

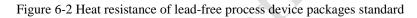
#### **RK3568 Hardware Design Guide**

| Profile Feature                                                                                                                                                    | Sn-Pb Eutectic Assembly              | Pb-Free Assembly                     |  |  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------------------------|--|--|
| Preheat & Soak<br>Temperature min (T <sub>smin</sub> )<br>Temperature max (T <sub>smax</sub> )<br>Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> ) | 100 °C<br>150 °C<br>60-120 seconds   | 150 °C<br>200 °C<br>60-120 seconds   |  |  |
| Average ramp-up rate<br>(T <sub>smax</sub> to T <sub>p</sub> )                                                                                                     | 3 °C/second max.                     | 3 °C/second max.                     |  |  |
| Liquidous temperature $(T_L)$<br>Time at liquidous $(t_L)$                                                                                                         | 183 °C<br>60-150 seconds             | 217 °C<br>60-150 seconds             |  |  |
| Peak package body temperature (T <sub>p</sub> )*                                                                                                                   | See classification temp in Table 4.1 | See classification temp in Table 4.2 |  |  |
| Time $(t_p)^{**}$ within 5 °C of the specified classification temperature $(T_c)$                                                                                  | 20** seconds                         | 30** seconds                         |  |  |
| Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )                                                                                                      | 6 °C/second max.                     | 6 °C/second max.                     |  |  |
| Time 25 °C to peak temperature                                                                                                                                     | 6 minutes max.                       | 8 minutes max.                       |  |  |
| * Tolerance for peak profile temperature (T <sub>p</sub> ) is defined as a supplier minimum and a user maximum.                                                    |                                      |                                      |  |  |

\*\* Tolerance for time at peak profile temperature (t<sub>p</sub>) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow soldering profile classification

| Package<br>Thickness | Volume mm <sup>3</sup><br><350 | Volume mm <sup>3</sup><br>350 - 2000 | Volume mm <sup>3</sup><br>>2000 |
|----------------------|--------------------------------|--------------------------------------|---------------------------------|
| <1.6 mm              | 260 °C                         | 260 °C                               | 260 °C                          |
| 1.6 mm - 2.5 mm      | 260 °C                         | 250 °C                               | 245 °C                          |
| >2.5 mm              | 250 °C                         | 245 °C                               | 245 °C                          |



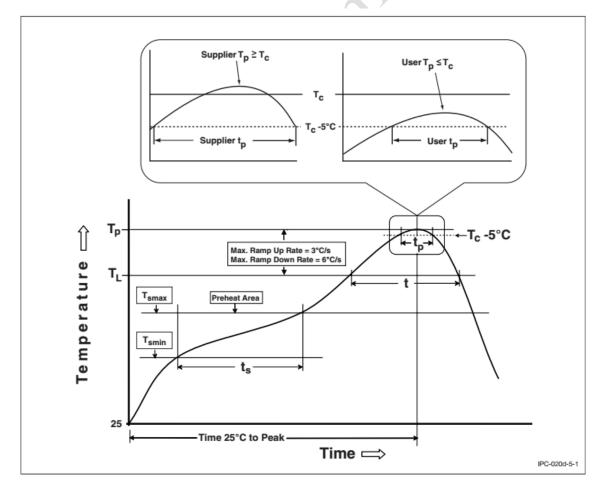


Figure 6-3 Lead-free reflow profile

## 6.3.3 SMT Recommendation Profile

The SMT profile recommended by RK is shown in Figure 6-4:

| Step 1<br>Board Preheat                                       | Step 2<br>Soak Time                                                                                            | Step 3<br>Peak Reflow & Time Above 220 °C                                                                                    | Step 4<br>Cool Down<br>Substrate MAX Temperature<br>≤260°C<br>Die Peak Temperature ≤300°C                                                                                                                                                                          |  |
|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| Start with solder joint temp <u>&lt;</u><br>40°C              | After nozzle is lowered<br>prior to peak reflow<br>(Soak Time: Paste dependant; consult<br>paste manufacturer) | Solder Joint Temp 230 – 250°C<br>Above ≥217°C 60 – 90 sec<br>Max delta-t of solder joint temperature at peak<br>reflow ≤10°C |                                                                                                                                                                                                                                                                    |  |
| Rising<br>Ramp Rate<br>0.5 – 2.5° C/ Sec.                     | Solder Joint Temp:<br>200 to 220°C                                                                             |                                                                                                                              | Cooling Ramp Rate<br>-0.5 to - 2.0°C/sec                                                                                                                                                                                                                           |  |
| Board Preheat Solder Joint<br>Temp:<br>125 – 150°C            | Critical Ramp Rate (205 to 215°C):<br>0.35 – 0.75°C/sec.                                                       | Peak Temp Range,<br>and Time Above ≥217°C spec's met.                                                                        | PCB land/pad temperature<br>needs to be at 100 – 130°C<br>±5°C when removing board<br>from rework machine bottom<br>heater at end of component<br>removal operation or ≤80°C<br>when using stand alone PCB<br>Pre-Heater for PCB land/pad<br>site dress operation. |  |
| Preheat with<br>bottom heater,<br>before nozzle<br>is lowered | Nozzle has lowered to reflow<br>component                                                                      | Nozzle is down during<br>peak reflow                                                                                         | Nozzle raises to home<br>position when solder joint<br>reaches peak temp range                                                                                                                                                                                     |  |

Figure 6-4 Lead-free reflow soldering process recommended profile parameters

# 7 Packages and Storage Conditions

## 7.1 Overview

This chapter introduces the storage and directions for RK3568 usage to ensure the safety and correct usage of products.

# 7.2 Terms Interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking • moisture barrier bag to reflow soldering; shider
- HIC: Humidity Indicator Card
- MSL: Moisture Sensitivity Level •
- MBB: Moisture Barrier Bag •
- Rebake: to bake again
- Solder Reflow
- Shell Life
- Storage environment

# 7.3 Moisture Packages

The dry vacuum package material of product is shown as follows:

- Desiccant;
- Six-point humidity card; •
- Moisture barrier bag: aluminum foil, silver opaque, with a mark of moisture sensitivity level;



Figure 7-1 Chipset dry vacuum package

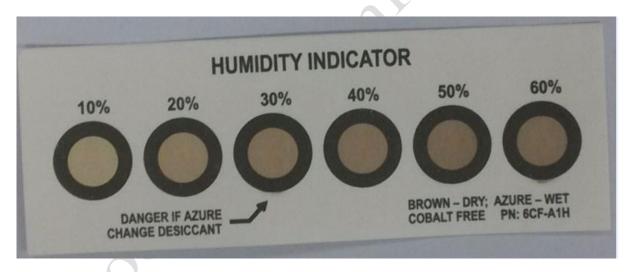


Figure 7-2 Six-point humidity card

# 7.4 Product Storage

#### 7.4.1 Storage Environment

The product is stored in vacuum packaging, and the storage time can reach 12 months when the temperature is  $\leq 40^{\circ}$ C and the relative humidity is <90%.

#### 7.4.2 Exposure Time

For environmental conditions:  $<30^{\circ}$ C and humidity 60%, please refer to Table 7-1 below.

The MSL level of RK3568 chipset is 3 and is very sensitive to humidity. If package is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of *Copyright* © 2022 *Rockchip Electronics Co., Ltd.* 233

#### **RK3568 Hardware Design Guide**

chip failure.

| MSL Level | Exposure time                                                                                |
|-----------|----------------------------------------------------------------------------------------------|
|           | Factory environmental conditions:≦30℃ /60%RH                                                 |
| 1         | Unlimited at $\leq 300$ °C/85%RH                                                             |
| 2         | 1 year                                                                                       |
| 2a        | 4 weeks                                                                                      |
| 3         | 168 hours                                                                                    |
| 4         | 72 hours                                                                                     |
| 5         | 48 hours                                                                                     |
| 5a        | 24 hours                                                                                     |
| 6         | Mandatory bake before use, and must be reflowed within the time limit specified on the label |

## 7.5 Usage of Moisture Sensitive Products

. .

After RK3568 packages are opened, it must meet the following conditions before reflow soldering:

- Continuous or cumulative exposure time is within 168 hours, and factory environment is ≤30°C/60% RH;
- Stored in <10% RH environment;
- Chips must be baked to remove internal moisture under the following conditions to avoid layered or popcorn problems during reflow:
- When humidity indicator card is at 23±5°C, >10% points have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 7-2 below for the time for chip re-baking:

| Table 7–2 KK5508 Ke-bake reference table |                |                                     |                                    |                                     |                                     |                                     |                                     |  |
|------------------------------------------|----------------|-------------------------------------|------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--|
| Package<br>Body                          | MSL Exc<br>Flo | <b>U</b>                            | High Temp Bake @125℃<br>+10/-0℃    |                                     | Medium Temp Bake<br>@90℃+8/-0℃      |                                     | Low Temp Bake @40℃<br>+5/-0℃        |  |
|                                          |                | Exceeding<br>Floor Life<br>by > 72h | Exceeding<br>Floor Life by<br>≤72h | Exceeding<br>Floor Life<br>by > 72h | Exceeding<br>Floor Life<br>by ≤ 72h | Exceeding<br>Floor Life<br>by > 72h | Exceeding<br>Floor Life<br>by ≤ 72h |  |
| Thickness<br>≤1.4mm                      | 3              | 9 hours                             | 7 hours                            | 33 hours                            | 23 hours                            | 13 days                             | 9 days                              |  |

#### Table 7–2 RK3568 Re-bake reference table



The Table shows the minimum baking time necessary after damp.

Low temperature baking is preferred.