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RK3568 EVB
User Guide

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Preface

Overview

This document is intended to introduce the basic functions and hardware characteristics, multi-function hardware configurations and software debug methods of RK3568 EVB, aiming to help developers to get start with RK3568 EVB and solution more quickly and correctly.

Product version

The corresponding product version of the document is as below:

Product name	Product version
RK3568 EVB	RK_EVB1_RK3568_DDR4P216SD6_V10_20200908

Intended Audience

This document (this guide) is mainly intended for：

- Technical support engineers
- Single board hardware development engineers
- Embedded software development engineers
- Test engineers

Revision History

This revision history recorded description of each version.

Revision Date	Version No.	Author	Revision History
2021-02-05	V1.0	WHB	Initial Release
2021-06-24	V1.1	WHB	Detailed description of optimization
2021-09-07	V1.2	WHB	Detailed description of optimization

Acronyms

These Acronyms includes the abbreviations of commonly used phrases in this document.

Acronym	Description in English	Description in Chinese
CPU	Central Processing Unit	中央处理器
NPU	Neural Network Processing Unit	神经网络处理器
VPU	Video Processing Unit	视频处理器
DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
eDP	Embedded Display Port	嵌入式数码音视讯传输接口
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
I2S	Inter-IC Sound	集成电路内置音频总线
PMIC	Power Management IC	电源管理芯片
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
DCDC	Direct Current to Direct Current	直流电转直流电
CAN	Controller Area Network	控制器局域网络
SARADC	Successive Approximation Register Analog to Digital Converter	逐次逼近寄存器型模数转换器
UART	Universal Asynchronous Receiver/ Transmitter	通用异步收发传输器
JTAG	Joint Test Action Group	联合测试行为组织
PWM	Pulse Width Modulation	脉冲宽度调制
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
LVDS	Low-Voltage Differential Signaling	低电压差分信号
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
RK/Rockchip	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
USB	Universal Serial Bus	通用串行总线
SATA	Serial Advanced Technology Attachment	串行高级技术附件
PCIe	Peripheral Component Interconnect Express	外围组件快速互连
RGB	Red,Green,Blue；RGB color mode is a color standard in industry	红绿蓝，RGB色彩模式，是工业界的一种颜色标准
VGA	Video Graphics Array	电脑显示视频Figure像标准接口
ADB	Android Debug Bridge	安卓调试桥
IR	Infrared Radiation	红外线
SPDIF	Sony/Philips Digital Interface	索尼/飞利浦数字音频接口
RTC	Real-time clock	实时时钟
RGMII	Reduced Gigabit Media Independent Interface	精简吉比特介质独立接口
WIFI	Wireless Fidelity	无线保真
CIF	Camera Interface	摄像头接口

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1 Overview

1.1 RK3568 Introduction

RK3568 is a quad-core ARM Cortex-A55 low-power and high-performance processor designed for personal mobile Internet devices and AIoT devices.

It provides many powerful embedded hardware engines to optimize the performance of advanced applications. The H.264 video decoder in RK3568 supports 4K@60fps, H.265 video decoder in RK3568 supports 4K@60fps, H.264/H.265 encoder supports 1080p@60fps, and high-quality JPEG codec. RK3568 embedded 3D GPU is fully compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1; the special 2D hardware engine maximizes the display performance and runs smoothly at the same time. The built-in NPU supports INT8/INT16 mixed operation. Due to strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

There are high-performance external memory interfaces in RK3568 to ensure high-capacity and high-stability system operating memory bandwidth, and it supports multiple memory models such as DDR3, DDR3L, LPDDR3, DDR4, LPDDR4, LPDDR4X, etc.

1.2 RK3568 Block Diagram

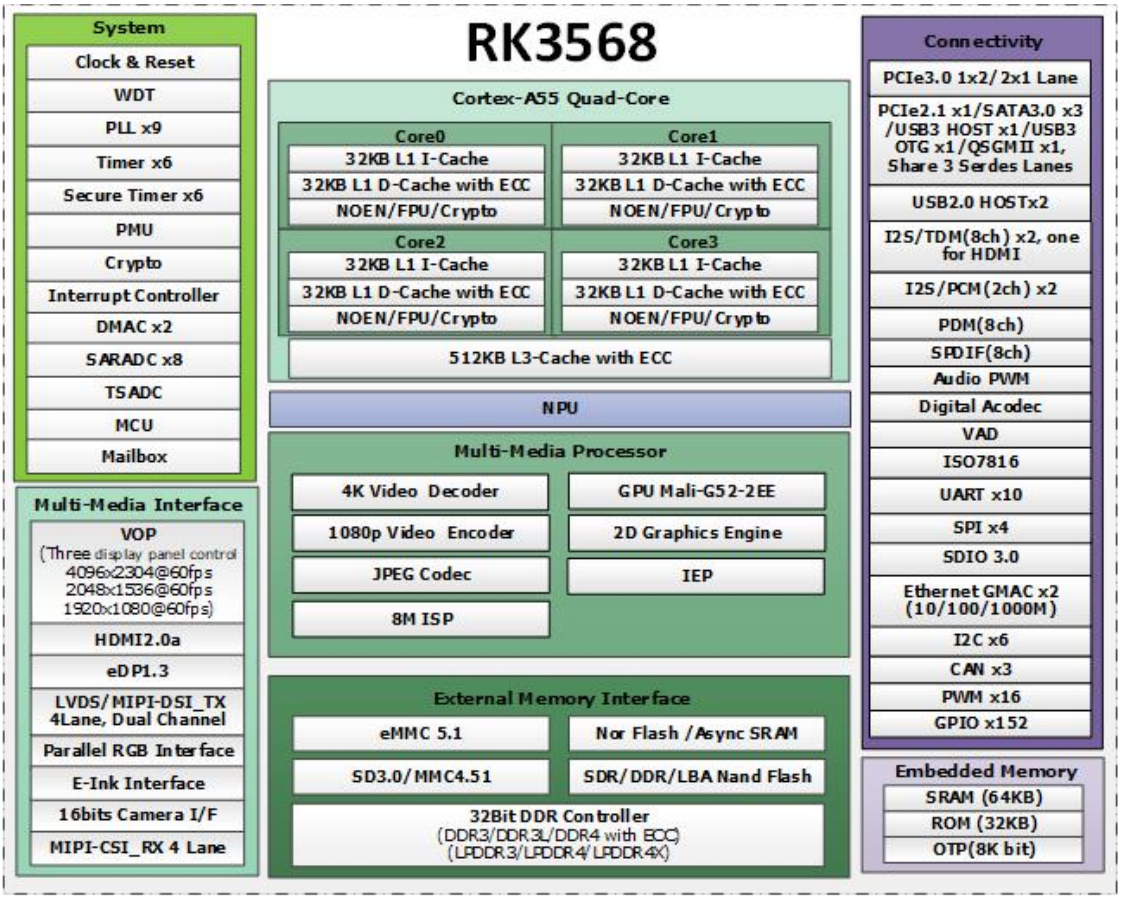


Figure 1-1 RK3568 Block Diagram

1.3 System Introduction

1.3.1 System Diagram

RK3568 EVB system takes RK3568 as a core chip, with PMIC RK809-5 power management chip，peripheral BUCK and LDO power chips, DDR4, eMMC and SATA/PCIe and other functional external device interfaces, integrating a stable and mass produced solution. The detailed system block diagram is as follows:

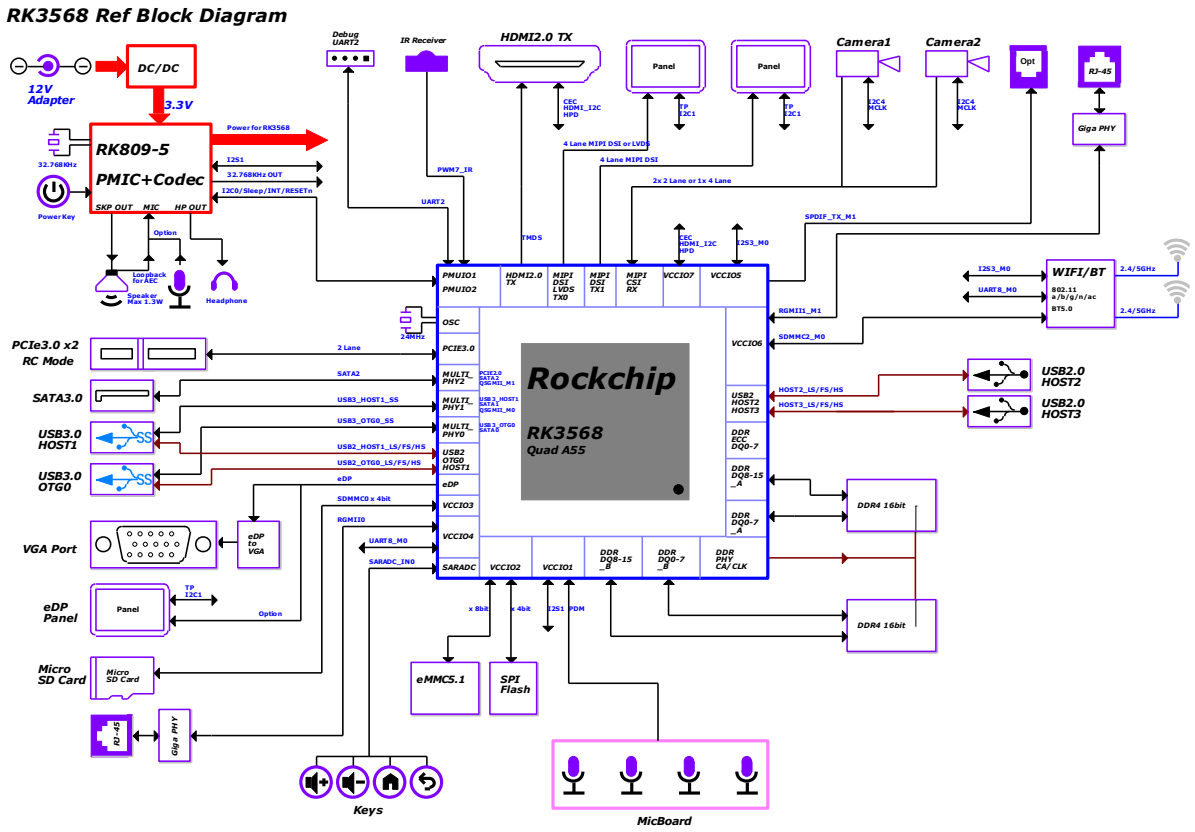


Figure 1-2 RK3568 EVB System Diagram

1.3.2 Functions Overview

RK3568 EVB includes the following functions:

- DC Power: DC 12V adapter power supply interface;
- USB3.0 OTG: one USB3.0 standard-A interface, dual layout USB2.0 micro interface, system firmware upgrade interface;
- USB3.0 HOST1: One USB3.0 standard-A interface, which can be connected to mouse, U disk, USB HUB and other devices;
- USB2.0 HOST2/3: Two USB2.0 standard-A interfaces, which can be connected to mouse, U disk, USB HUB and other devices;
- TF Card: You can connect an TF card to extend the system storage capacity ;
- CIF/EBC/RGMII/VOPBT656 Interface: Reserved CIF/EBC/RGMII/BT656 extension interfaces;
- MIPI CSI: Support two 2lane or one 4lane MIPI signal input, connected via FPC line;
- HDMI2.0 OUT: Support up to 4K@60Hz output;
- MIPI DSI/LVDS TX0: Support 4lane MIPI or LVDS signal output, connected via FPC line;

- MIPI DSI TX1: Support 4lane MIPI signal output, connected via FPC line;
- LCM eDP OUT: External eDP display screen with touch, connected via FPC line;
- VGA OUT: Convert eDP signal to VGA output;
- SDIO Wifi(2x2 Wifi&BT5.0): Wifi model is AP6398S, external SMA antenna, supports wireless Internet access function;
- Ethernet: Support 2 RGMII 10/100/1000M Ethernet;
- Audio Interface: Supports speaker or headphone audio output, single MIC recording, digital audio output interface and MIC array interface;
- SATA3.0 Interface: One 7pin SATA interface, one 4pin SATA power interface;
- PCIe3.0 Interface: One 2Lane PCIe, supports users to extend and debug PCIe devices;
- IR Receive: IR remote control input;
- Sensor: Gyroscope+G-Sensor devices;
- UART Debug: Debug and check LOG information;
- JTAG: System JTAG debug interface;
- System Key: Including Reset, MASKROM, POWERON, V+/Recover, V-, MENU, ESC keys;
- SARADC: 5-channel ADC 2.54mm standard male pin;
- UART: Support external 3 UART + 2 UART (Option) function devices;
- CAN: Support one CAN bus;
- SPDIF: Support digital audio interface

1.3.3 Functional Interfaces

Table 1-1 PCB Functional Interfaces Introduction

Functions	Usable or not
DDR4(512x16bit, total capacity is2GB)	YES
eMMC (total capacity 32GB)	YES
nand Flash	Choose one of the three types of flash, it is NC by default
SPI Flash	Choose one of the three types of flash, it is NC by default
DC 12V Input	YES
USB3.0 OTG	YES
USB3.0 Host(1 Port)	YES
USB2.0 Host(2 Port)	YES
TF Card	YES
CIF/EBC/RGMII/VOPBT656 Interface	Need jumper resistances, please refer to section 3.19
MIPI CSI	YES
HDMI2.0 OUT	YES
MIPI DSI/LVDS TX0(4lane)	YES
MIPI DSI TX1(4lane)	YES
LCM eDP OUT	Need jumper capacitances, please refer to section 3.16
VGA OUT	YES
SDIO Wifi(2x2 Wifi&BT5.0)	YES
RGMII 10M/100M/1000M（2 Port）	YES
Audio(SPK、MIC、Headphone)	YES
SATA3.0 Interface	YES
PCIe3.0 Interface	YES
IR Receive	YES
Gyroscope+G-Sensor	YES
UART Debug	YES
UART（5 Port）	YES
JTAG Interface	YES
System Key	YES
SARADC（5 Port）	YES
CAN	YES
SPDIF	YES

1.3.4 Functional Modules Layout

EVB functional interfaces layout are showed as follows：

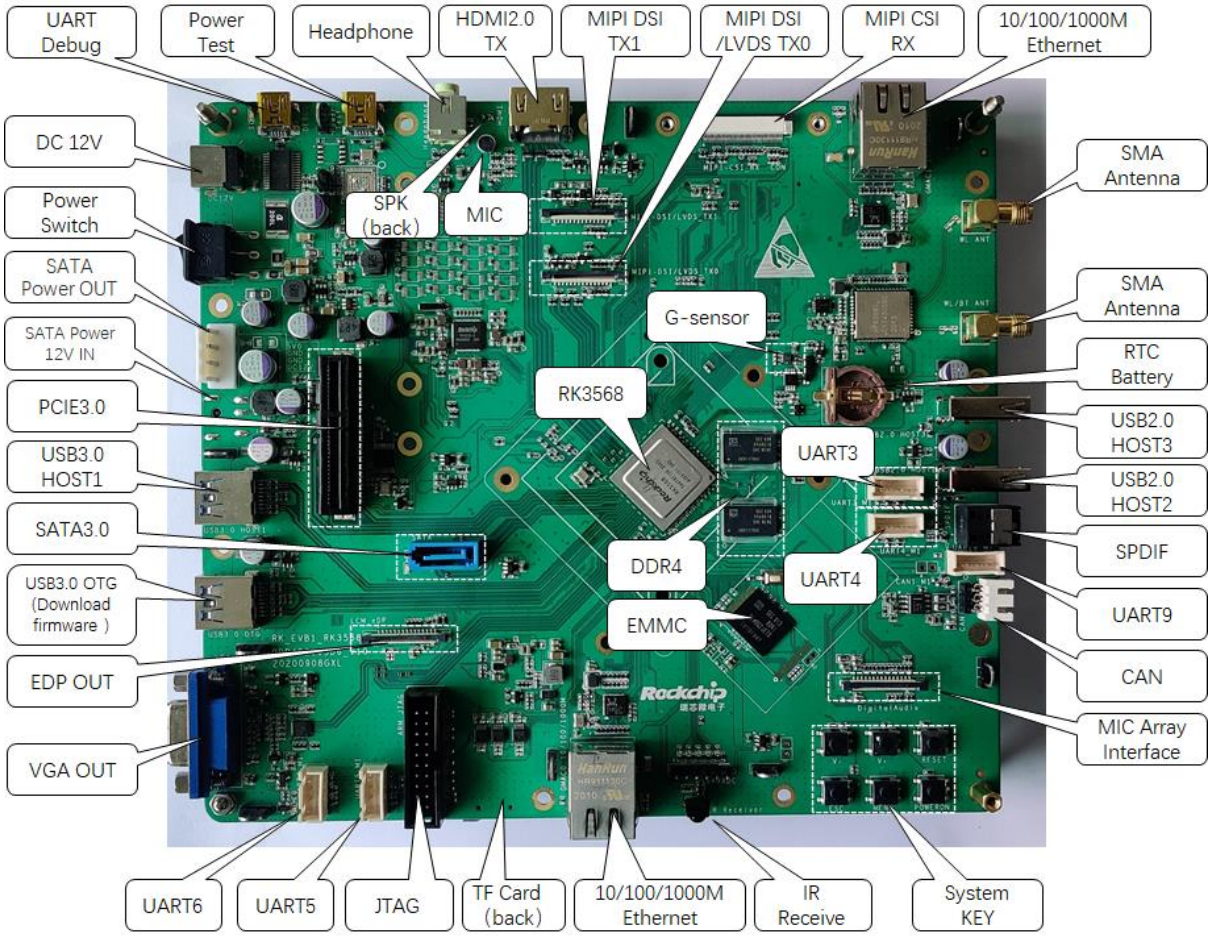


Figure 1-3 EVB TOP Surface

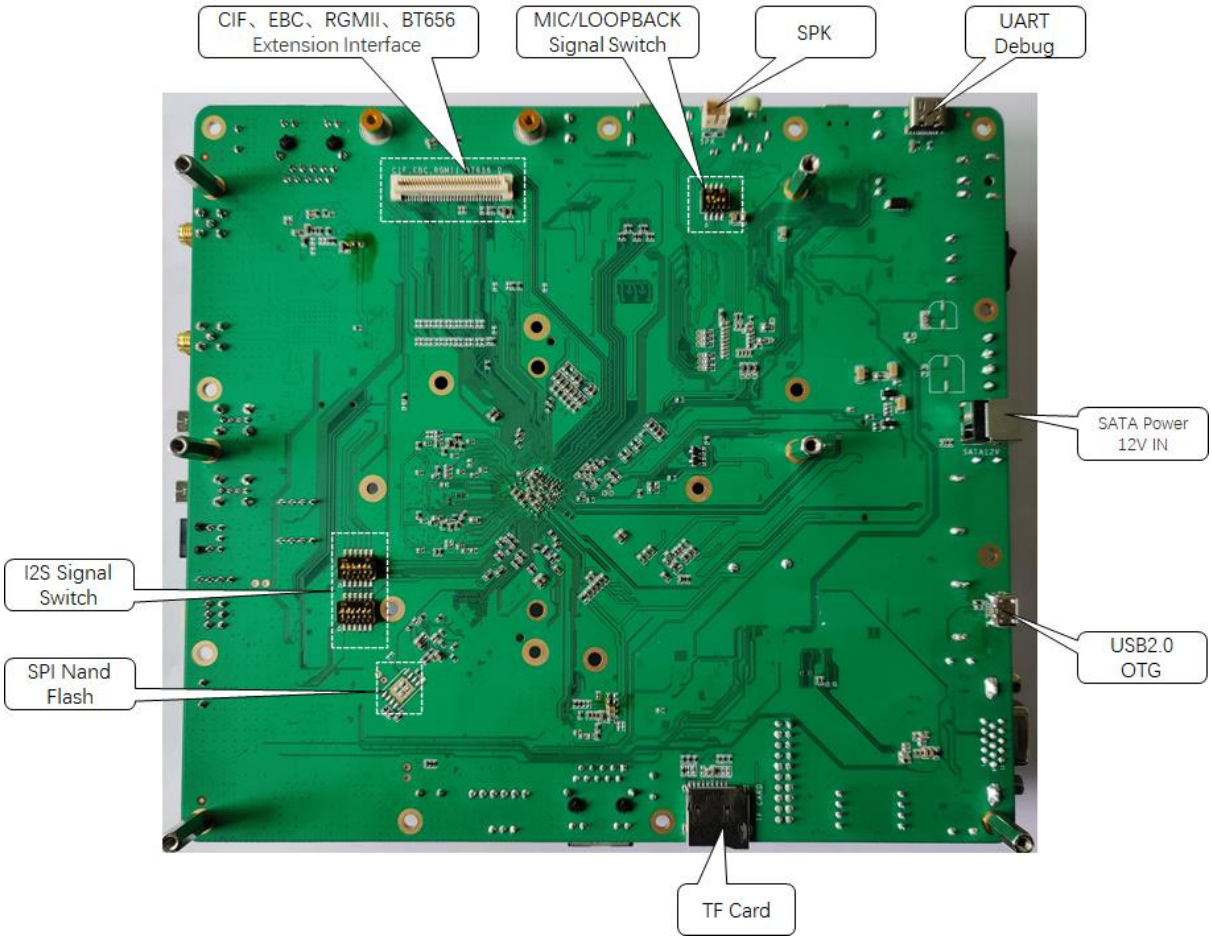


Figure 1-4 EVB Bottom Surface

1.4 Components

RK3568 EVB package includes the following components:

- One RK3568 EVB
- One DC adapter: input 100V AC~240V AC, 50Hz, output DC12V/2A
- Screen: 5.5 inch MIPI screen with 1920*1080 resolution
- Two 2.4G/5G dual band SMA male interface antennas

1.5 Power on, power off and Standby

The way to power on and off the EVB, let the EVB go to standby mode are introduced as follows:

- Power on: Connect DC 12v power supply and turn on the power switch to start the EVB.
- Power off: Press and hold the power button for 6 seconds to power off the system.
- Standby: Press the power button, the system will enter the first-level standby state. When there is no USB OTG connection, no other operations (such as key operation), and the software without Wake_Lock source. After about 3 seconds, it will switch from the first-level standby state to the second-level standby state.

1.6 Firmware Upgrade

1.6.1 USB Driver Installation

It has to install the driver before upgrading the EVB driver, the tool is located in:

SDK\RKTools\windows\Release_DriverAssitant, open "DriverInstall.exe", click "Driver Installation", to install the driver. If the previous version driver has been installed, please click "Driver Uninstall" and reinstall the driver.

The driver file almost covers all current operating systems which can be supported.

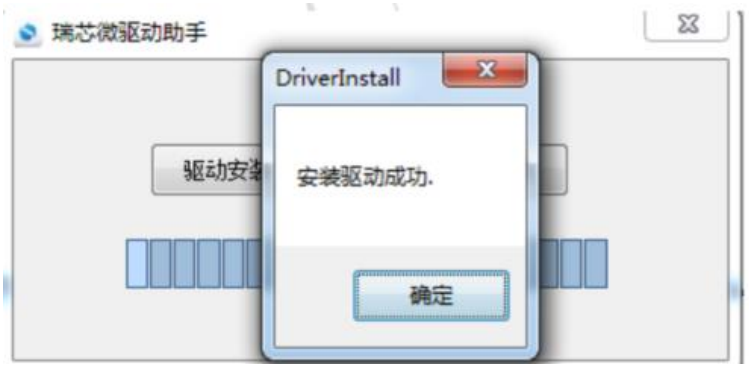


Figure 1-5 Driver Installed Successfully

1.6.2 Firmware Upgrade

There are two ways to upgrade RK3568 EVB firmware:

- Enter Loader upgrade mode:

Ensure that SARADC_VIN0 is low before the system is powered on, and the system will enter the Loader state.

Detailed steps are as follows:

1. Connect the USB3.0 OTG port to a PC, press and hold RECOVER key of the EVB.
2. EVB is powered by 12v. If it has been powered on, press the reset key.
3. After the flashing tool shows that a Loader device is found, release the RECOVER key.
4. Select Loader, Parameter, Uboot, Recovery and other files on the flashing tool.
5. Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

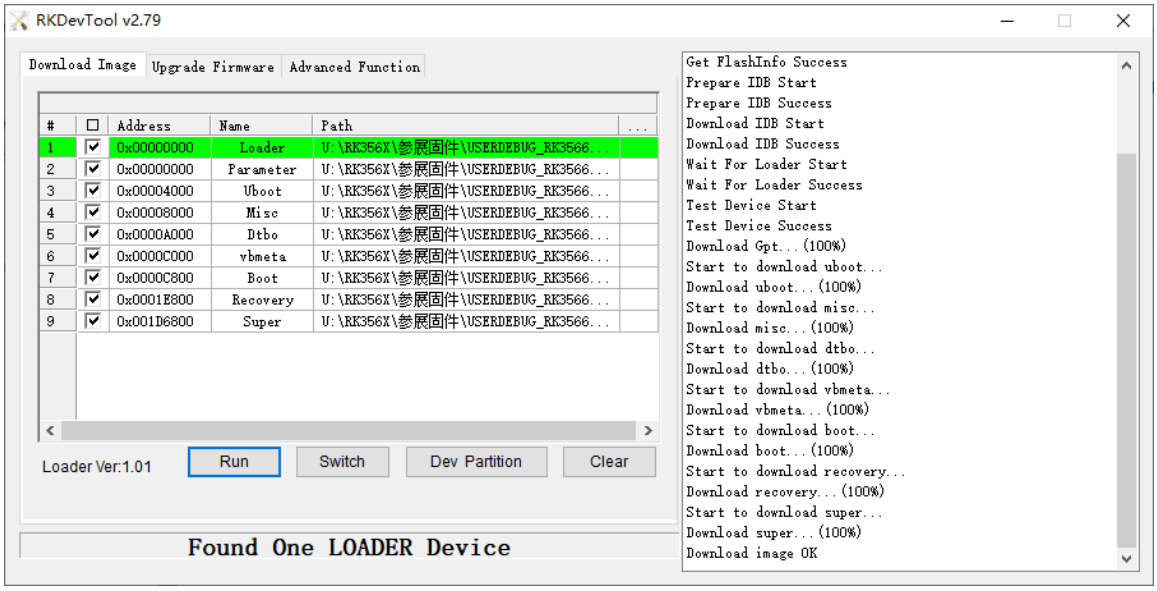


Figure 1-6 Loader Flashing Mode

- Maskrom upgrade mode:

Before the system is powered on, eMMC_D0 is connected to ground, causing eMMC to fail to boot and enter the Maskrom state.

Detailed steps are as follows:

1. Connect the USB3.0 OTG port to a PC, press and hold MASKROM button on the EVB.

2. The EVB is powered by 12V. If it has been powered on, press the reset button.

3. After the flashing tool shows that a Maskrom device is found, release the MASKROM button. Note that in the Maskrom state, you need to select the corresponding Loader options to finish the upgrading.

4. Select Loader, Parameter, Uboot, Recovery and other files on the flashing tool.

5. Click Execute to enter the upgrade state. The right side of the tool is the progress display bar, which displays the download progress and verification status.

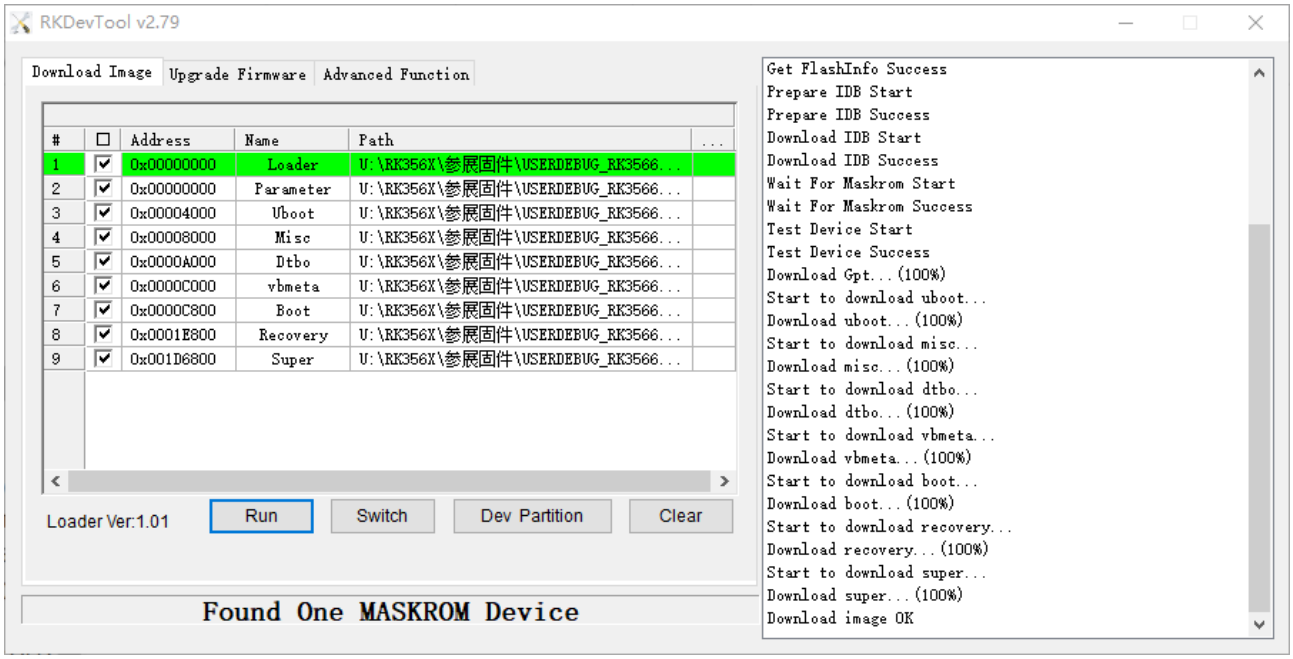


Figure 1-7 Maskrom Flashing Mode Serial

1.7 Port Debugging

1.7.1 Serial Port Debugging Tool

Connect the USB Debug interface of the EVB to a PC, and get the current COM number in the PC device manager.

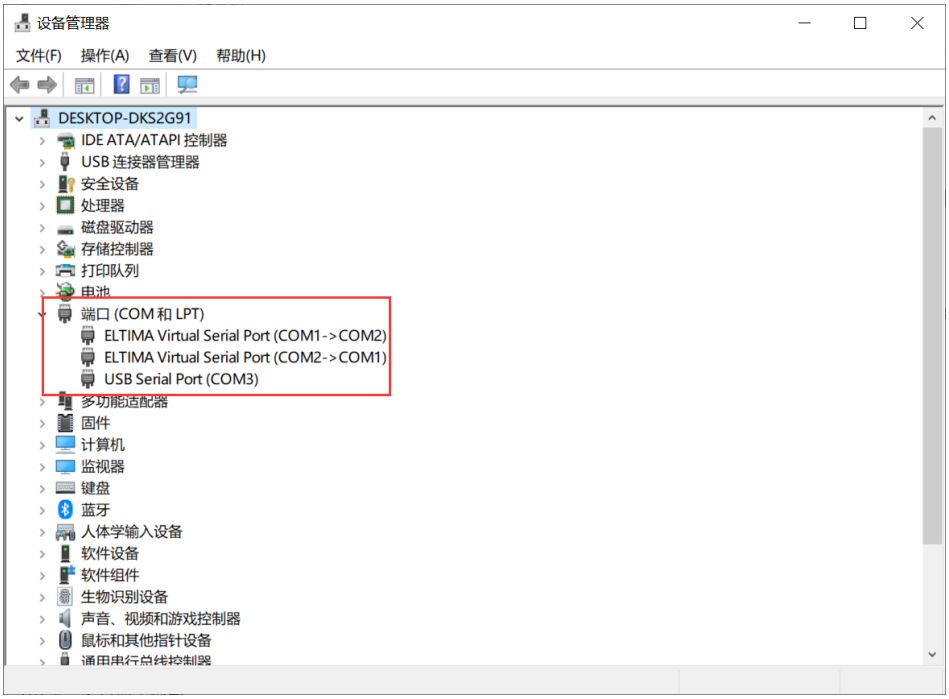


Figure 1-8 Current COM Number

Open the serial port debug tool. Firstly, enter Session interface; Secondly select “Serial” under Connection type; thirdly, select the corresponding serial port number and change the baud rate to 1.5M (RK3568 supports 1.5M baud rate by default), and finally click the "open" button to enter the serial debugging interface.

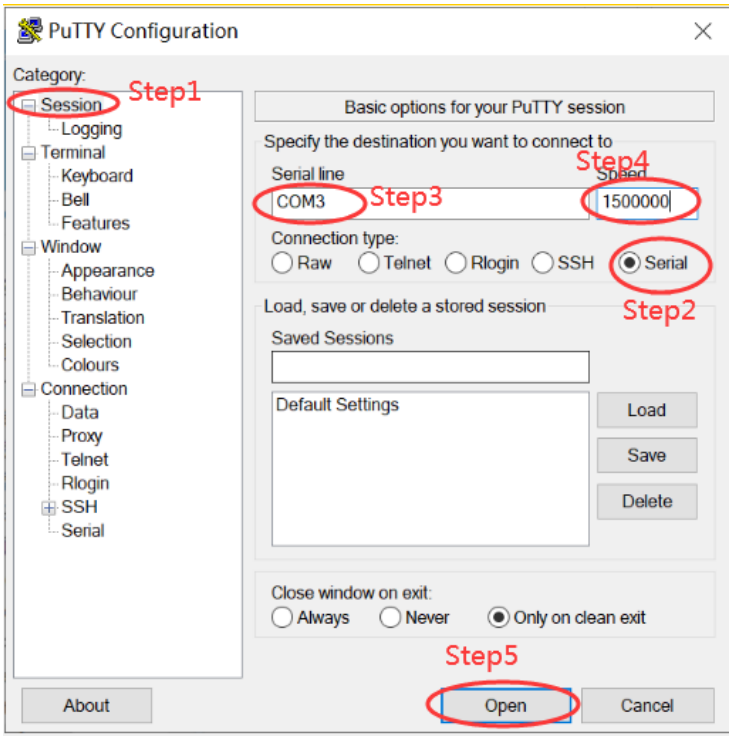


Figure 1-9 Serial Port Tool Configuration Interface

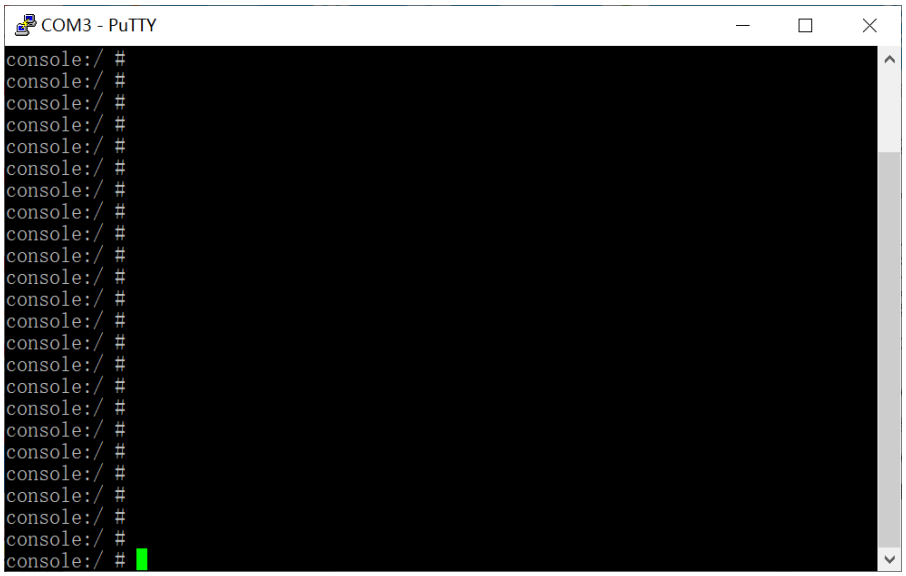


Figure 1-10 Serial Port Tool Debugging Interface

1.7.2 ADB Debug

1. Ensure that the driver is installed successfully, and the PC is connected to the USB3.0 OTG port of the EVB;

2. Power on the EVB and boot into the system;

3. On the PC, Click start ---run ---cmd, enter the directory where the adb.exe tool is located, and input "adb devices" if the connected device is searched, indicating that the connection is successful;

4. Input "adb shell" to enter ADB debug.

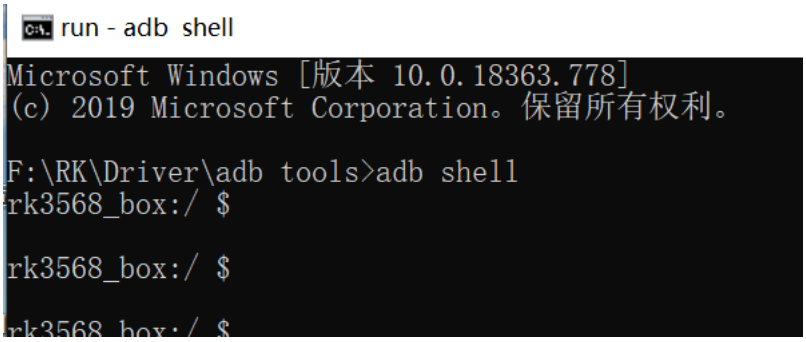


Figure 1-11 ADB Connected Successfully

2 Hardware Introduction

2.1 EVB Picture

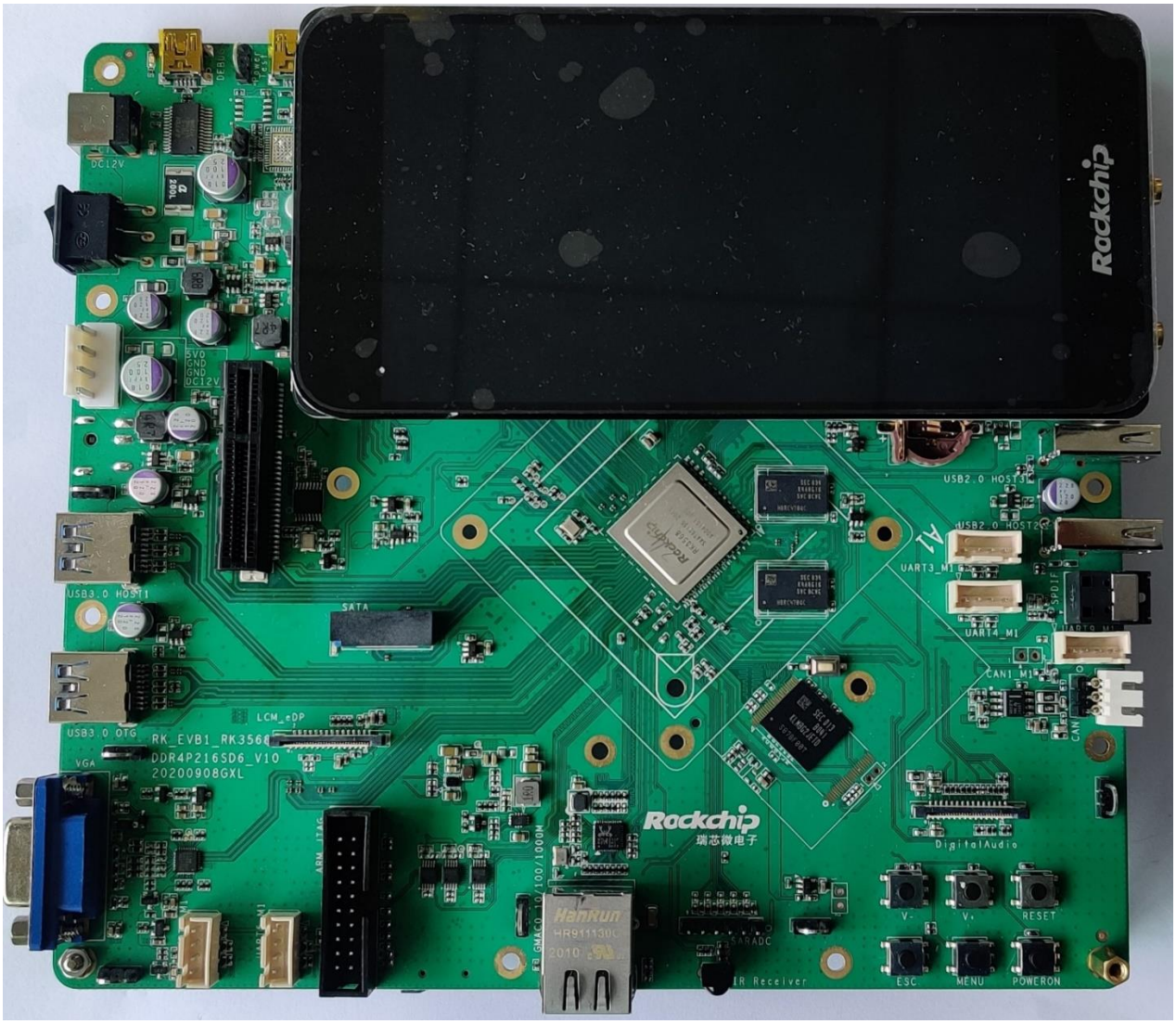


Figure 2-1 EVB Picture

2.2 Power Diagram

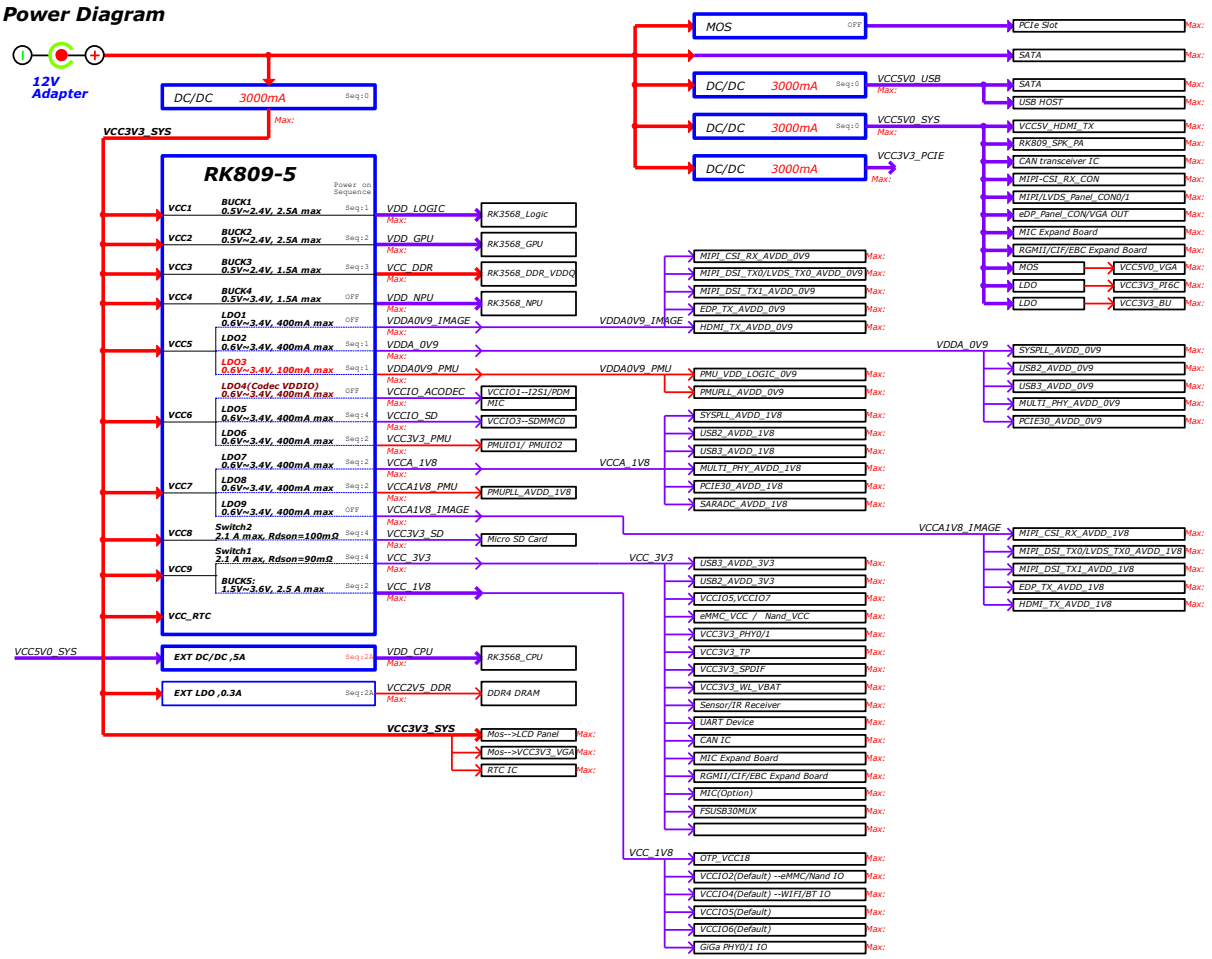


Figure 2-2 RK3568 EVB Power Diagram

2.3 I2C Address

The EVB reserves a reach peripheral interfaces. I2C peripherals debugging is relate to I2C channel multiplexing. Table 2-1 shows the match relation between I2C address of the EVB and voltage level, to avoid address conflicts and mismatched.

Table 2-1 Match Relation Between I2C Address and IO Voltage Level

I2C Channel	Devices	I2C address	Power domain
I2C0	RK809-5（PMIC）	0X20	3.3V
I2C0	TCS4525（DCDC）	0X1C	3.3V
I2C1	eDP TX	TBD	3.3V
I2C1	MIPI DSI/LVDS TX0	TBD	3.3V
I2C1	MIPI DSI TX1	TBD	3.3V
I2C1	CIF/EBC/VOPBT656	TBD	3.3V
I2C2	CIF/EBC/VOPBT656	TBD	3.3V
I2C3	CIF/EBC/VOPBT656	TBD	3.3V
I2C3	MIC Array Interface	TBD	3.3V
I2C4	Camera MIPI CSI	TBD	1.8V
I2C4	CIF/EBC/VOPBT656	TBD	1.8V
I2C5	RTD2166(VGA)		3.3V
I2C5	HYM8563TS（RTC）	Read：0XA3 Write：0XA2	3.3V
I2C5	G-sensor(MXC6655XA)	0X15	3.3V

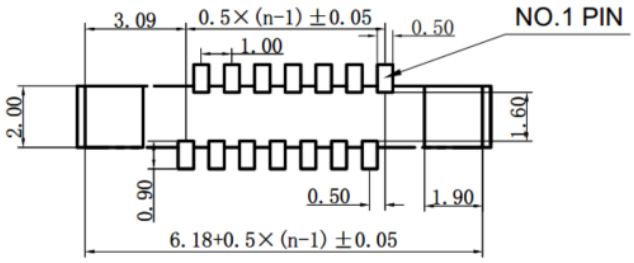
Note: when using an extension board, please ensure that the I2C address of the extension board does not conflict with the I2C address of the EVB.

2.4 Extension Connectors

Users may use extension boards in practical use. There are several types of connectors for development boards:

J5200, J5400, J5600, JP7700 are vertical double-row 30pins with 0.5mm pins and 1mm pitch (corresponding to the FPC cable with 0.5mm pitch, 30pin), the dimensions are as follows:

P数	A	B	C	D	P数	A	B	C	D
4	1.500	2.570	8.400	4.650	35	17.000	18.070	23.900	5.150
5	2.000	3.070	8.900	4.650	36	17.500	18.570	24.400	5.150
6	2.500	3.570	9.400	4.650	37	18.000	19.070	24.900	5.150
7	3.000	4.070	9.900	4.650	38	18.500	19.570	25.400	5.150
8	3.500	4.570	10.400	4.650	39	19.000	20.070	25.900	5.150
9	4.000	5.070	10.900	4.650	40	19.500	20.570	26.400	5.150
10	4.500	5.570	11.400	4.650	41	20.000	21.070	26.900	5.150
11	5.000	6.070	11.900	4.650	42	20.500	21.570	27.400	5.150
12	5.500	6.570	12.400	4.650	43	21.000	22.070	27.900	5.150
13	6.000	7.070	12.900	4.650	44	21.500	22.570	28.400	5.150
14	6.500	7.570	13.400	4.650	45	22.000	23.070	28.900	5.150
15	7.000	8.070	13.900	4.650	46	22.500	23.570	29.400	5.150
16	7.500	8.570	14.400	4.650	47	23.000	24.070	29.900	5.150
17	8.000	9.070	14.900	4.650	48	23.500	24.570	30.400	5.150
18	8.500	9.570	15.400	4.650	49	24.000	25.070	30.900	5.150
19	9.000	10.070	15.900	4.650	50	24.500	25.570	31.400	5.150
20	9.500	10.570	16.400	4.650	51	25.000	26.070	31.900	5.150
21	10.000	11.070	16.900	4.650	52	25.500	26.570	32.400	5.150
22	10.500	11.570	17.400	4.650	53	26.000	27.070	32.900	5.150
23	11.000	12.070	17.900	4.650	54	26.500	27.570	33.400	5.150
24	11.500	12.570	18.400	4.650	55	27.000	28.070	33.900	5.150
25	12.000	13.070	18.900	4.650	56	27.500	28.570	34.400	5.150
26	12.500	13.570	19.400	4.650	57	28.000	29.070	34.900	5.150
27	13.000	14.070	19.900	4.650	58	28.500	29.570	35.400	5.150
28	13.500	14.570	20.400	4.650	59	29.000	30.070	35.900	5.150
29	14.000	15.070	20.900	4.650	60	29.500	30.570	36.400	5.150
30	14.500	15.570	21.400	5.150	61	30.000	31.070	36.900	5.150
31	15.000	16.070	21.900	5.150	62	30.500	31.570	37.400	5.150
32	15.500	16.570	22.400	5.150	63	31.000	32.070	37.900	5.150
33	16.000	17.070	22.900	5.150	64	31.500	32.570	38.400	5.150
34	16.500	17.570	23.400	5.150					



PC BOARD LAYOUT

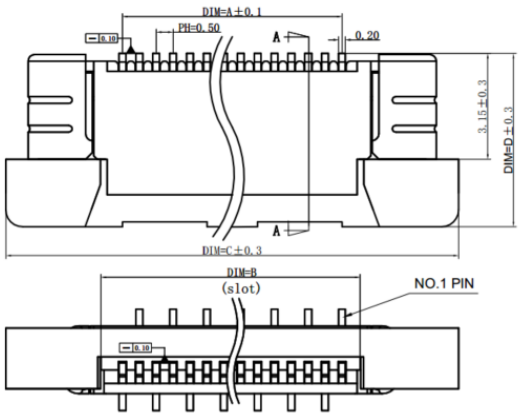
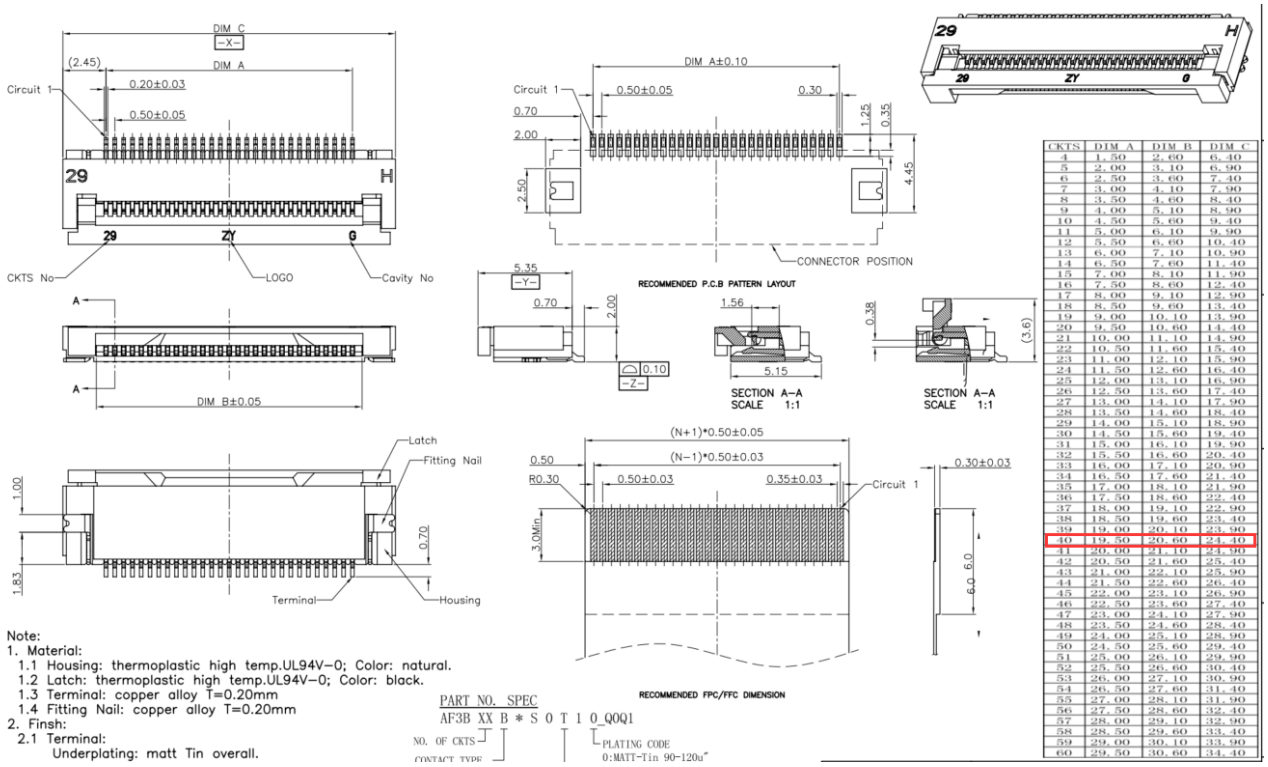


Figure 2-3Vertical Double Row 30 PIN PCB Package with 1mm Pitch

J4700 is a flip 40 PIN FPC Connectors, with 0.2mm pins and 0.5mm pitch (corresponding to FPC cable pitch 0.5mm, 40pin), the dimensions are as follows:



CKTS	DIM A	DIM B	DIM C
4	1.50	2.60	6.40
5	2.00	3.10	6.90
6	2.50	3.60	7.40
7	3.00	4.10	7.90
8	3.50	4.60	8.40
9	4.00	5.10	8.90
10	4.50	5.60	9.40
11	5.00	6.10	9.90
12	5.50	6.60	10.40
13	6.00	7.10	10.90
14	6.50	7.60	11.40
15	7.00	8.10	11.90
16	7.50	8.60	12.40
17	8.00	9.10	12.90
18	8.50	9.60	13.40
19	9.00	10.10	13.90
20	9.50	10.60	14.40
21	10.00	11.10	14.90
22	10.50	11.60	15.40
23	11.00	12.10	15.90
24	11.50	12.60	16.40
25	12.00	13.10	16.90
26	12.50	13.60	17.40
27	13.00	14.10	17.90
28	13.50	14.60	18.40
29	14.00	15.10	18.90
30	14.50	15.60	19.40
31	15.00	16.10	19.90
32	15.50	16.60	20.40
33	16.00	17.10	20.90
34	16.50	17.60	21.40
35	17.00	18.10	21.90
36	17.50	18.60	22.40
37	18.00	19.10	22.90
38	18.50	19.60	23.40
39	19.00	20.10	23.90
40	19.50	20.60	24.40
41	20.00	21.10	24.90
42	20.50	21.60	25.40
43	21.00	22.10	25.90
44	21.50	22.60	26.40
45	22.00	23.10	26.90
46	22.50	23.60	27.40
47	23.00	24.10	27.90
48	23.50	24.60	28.40
49	24.00	25.10	28.90
50	24.50	25.60	29.40
51	25.00	26.10	29.90
52	25.50	26.60	30.40
53	26.00	27.10	30.90
54	26.50	27.60	31.40
55	27.00	28.10	31.90
56	27.50	28.60	32.40
57	28.00	29.10	32.90
58	28.50	29.60	33.40
59	29.00	30.10	33.90
60	29.50	30.60	34.40

Figure 2-4 Flip and 0.5mm Pitch and 40 PIN FPC PCB Package

2.5 Reference Materials

The reference diagram and PCB version information of the EVB are as follows:

- RK_EVB1_RK3568_DDR4P216SD6_V10_20200908.DSN
- RK_EVB1_RK3568_DDR4P216SD6_V10_20200908GXL.brd

3 EVB Modules Introduction

3.1 Power Input

The power adapter inputs 12V/2A power, after going through the front-end step-down converter (buck) power, will get the system power VCC5V0_SYS and VCC3V3_SYS which will provide to PMIC power management chip, multiple discrete DCDC, LDO and FET switch, and output different voltages for system.

Power adapter input port, front-end Buck converter and PMIC chip are showed as follows:

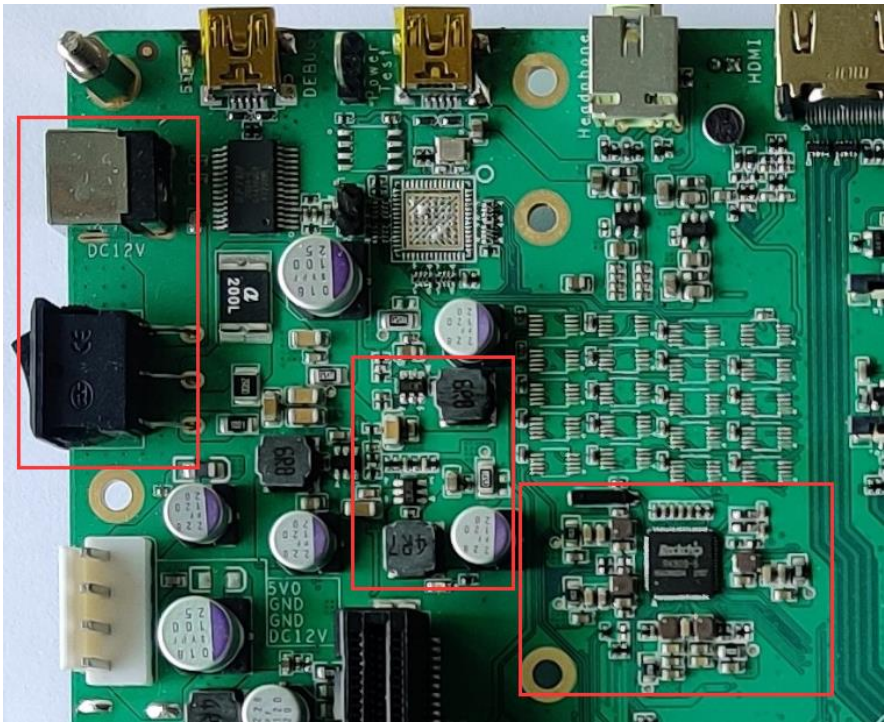


Figure 3-1 DC12V Input, Front-end Buck Converter and PMIC Chip

3.2 Memory

- eMMC
  - The memory on the EVB is eMMC FLASH with the capacity of 32GB by default
  - There is a Maskrom key reserved on the EVB for access to Maskrom to upgrade firmware easily
- SPI/NAND Flash
  - The EVB reserves SPI/ NAND Flash location
- DDR
  - The DDR on the EVB is two 512Mx16bit DDR4, with a total capacity of 2GB

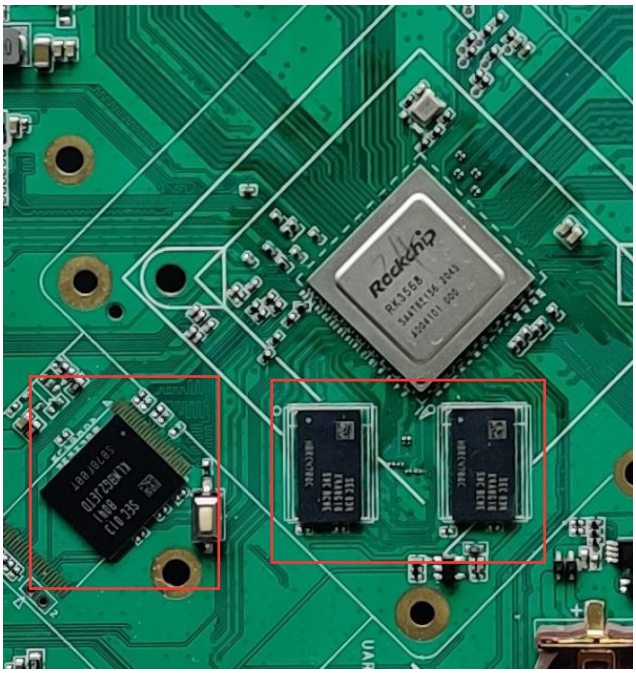


Figure 3-2 DDR4, eMMC and Reserved NAND Flash Location

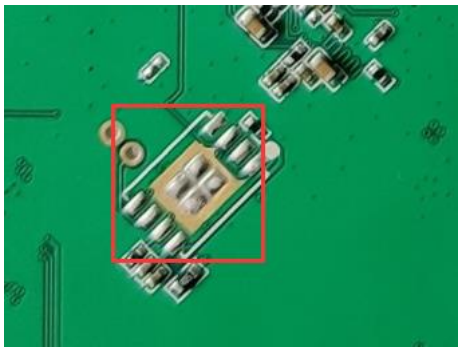


Figure 3-3 Reserved SPI Flash Location

The key Location of EVB for entering Maskrom flashing mode:

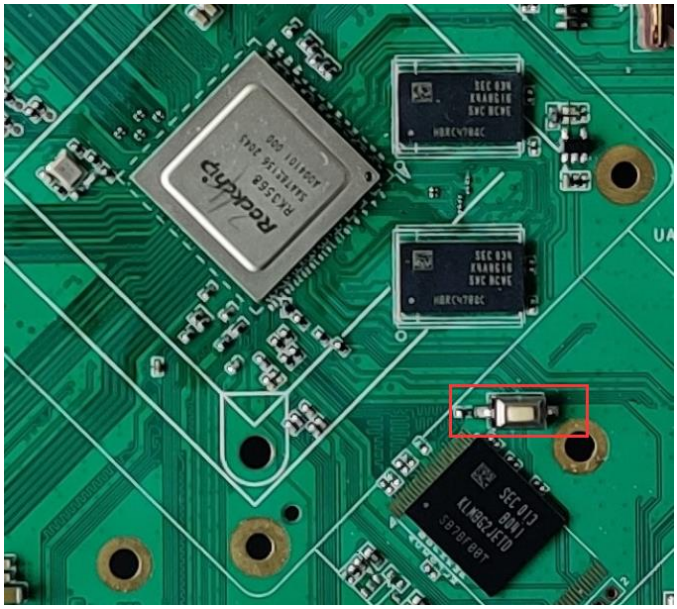


Figure 3-4 The Key Location for Entering Maskrom Flashing Mode

3.3 RTC Circuit

The RTC circuit is based on HYM8563TS chip, which can be powered by the development board or built-in button battery. It can keep providing accurate time even when the board is powered off, and communicate with the controller through I2C signal.

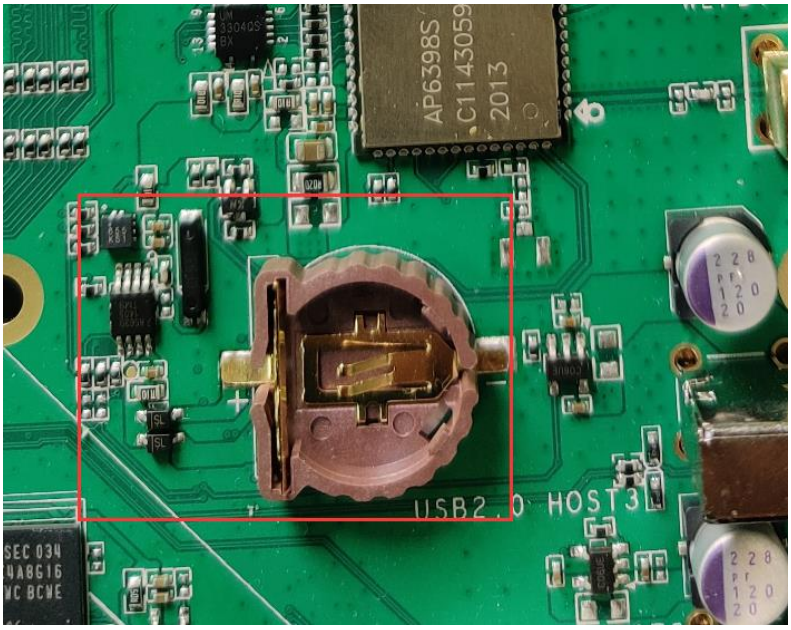


Figure 3-5 RTC Circuit

3.4 Keys Input

The EVB takes SARADC_VIN0 as RECOVER detection port, supports 10-bit resolution, and it will go to loader flashing mode by the RECOVER key on the EVB; in addition, there is also a RESET key on the board, which is convenient for resetting and restarting the device through hardware; and several other commonly used keys: V+, V-, ESC, MENU, POWERON.

Their location are as follows:

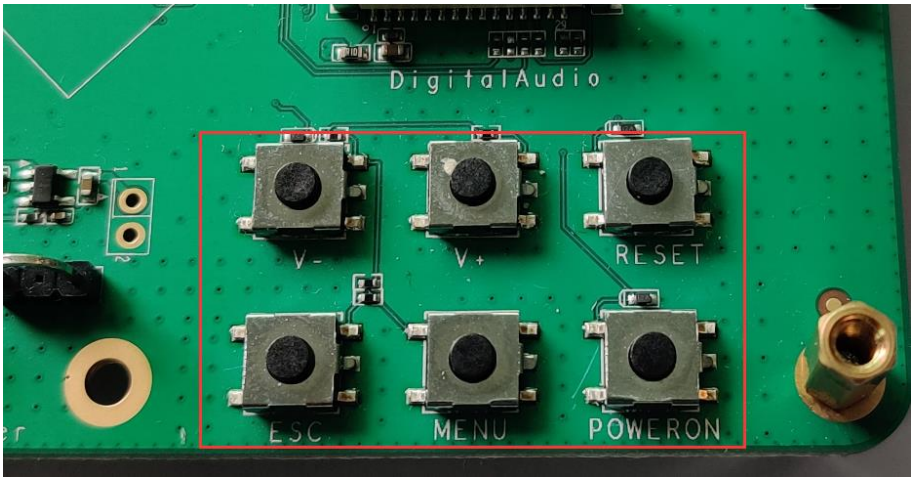


Figure 3-6 EVB Keys

3.5 Infrared Receiver

The small infrared receiver on the development board is general model IRM3638, with a center frequency of 38KHz.

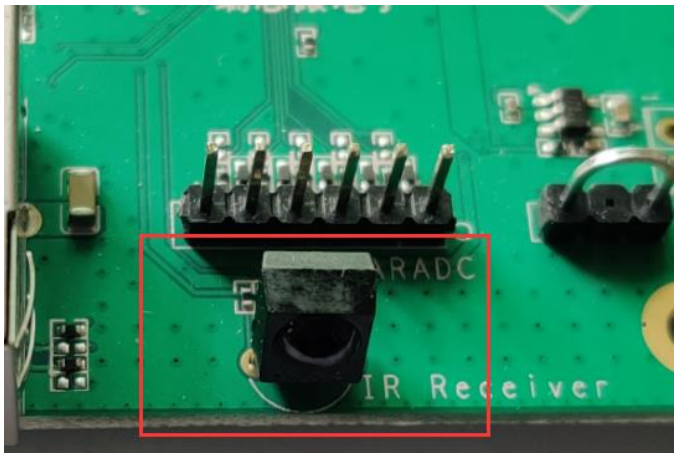


Figure 3-7 Receiver

3.6 Gyroscope Sensor

The EVB supports gyroscope sensors, and uses MXC6655XA chip to communicate with the controller through I2C.

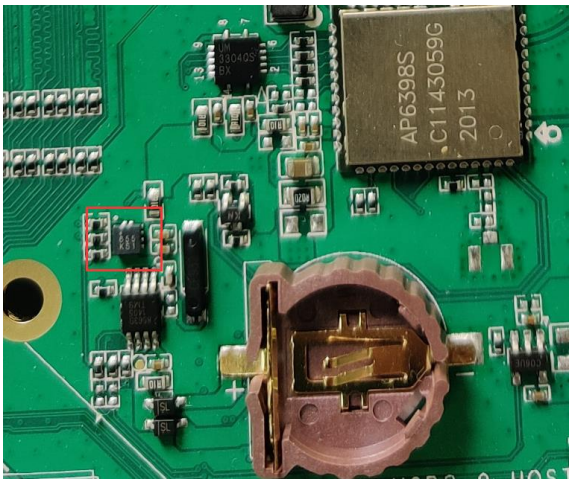


Figure 3-8 Gyroscope Sensor

3.7 UART Interface

The EVB reserves 5 UART interfaces, which communicate with the controller through UART3, UART4, UART5, UART6, and UART9 serial ports. The external standard 4 PINS 2.54mm male socket is convenient for UART peripheral debugging.

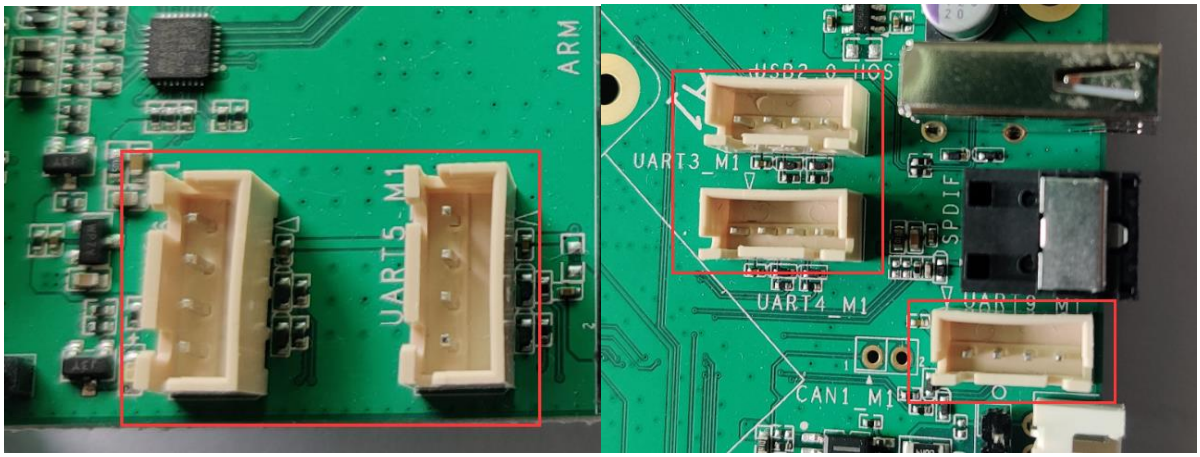


Figure 3-9 UART Interface

3.8 UART Debug Interface

The development board provides a serial port for debugging, it is UART2 by default, use FT232RL chip to covert UART to USB, with the baud rate of 1.5M.

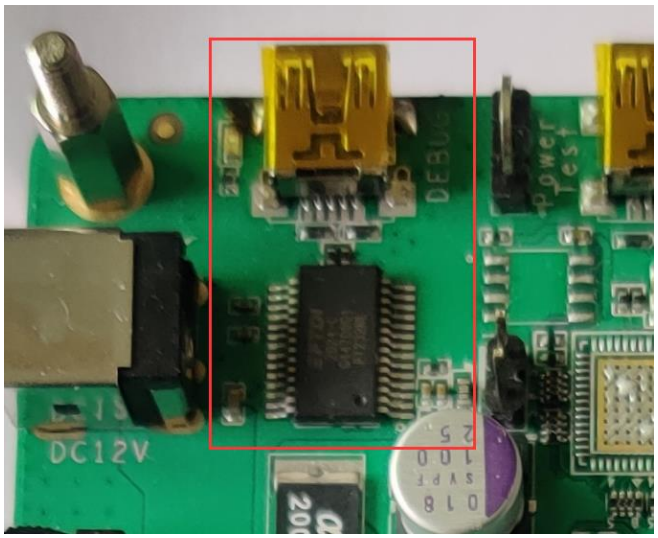


Figure 3-10 UART Debug Interface

3.9 CAN Bus Interface

The CAN bus of the development board takes TCAN1044V driver chip, which is used to convert logic level and signal level, and supports 1.7V-5.5V

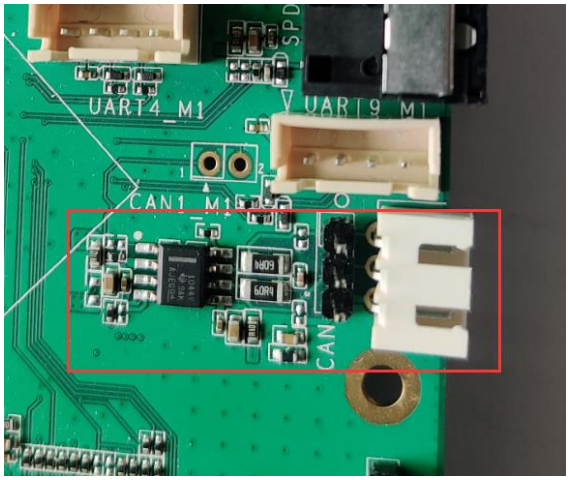


Figure 3-11CAN Bus Interface

3.10 JTAG Debug Interface

There is a standard 20pin JTAG debugging interface on the EVB, which is convenient for customers to debug through JTAG.

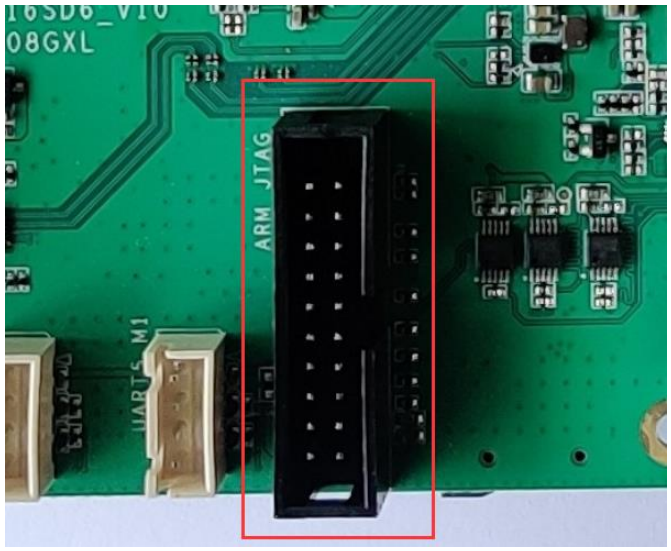


Figure 3-12 JTAG Debug Interface

3.11 SPDIF Audio Interface

The development board supports SONY and PHILIPS digital audio interface output, and the transmission hardware interface is fiber mode.

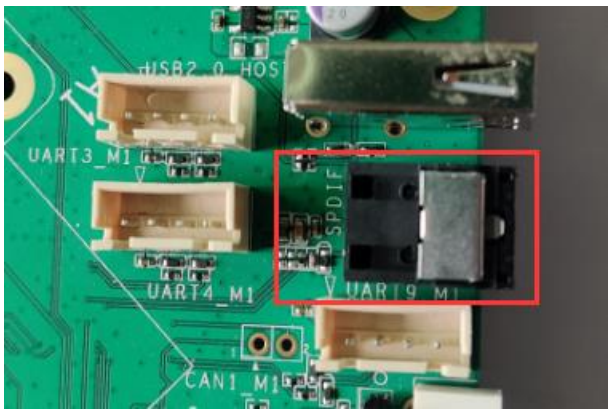


Figure 3-13 SPDIF Audio Interface

3.12 TF Card Interface

TF Card is SDMMC0 interface, which is used to extend the system storage capacity, the data bus width is 4bits, and supports SDMMC3.0 protocol.

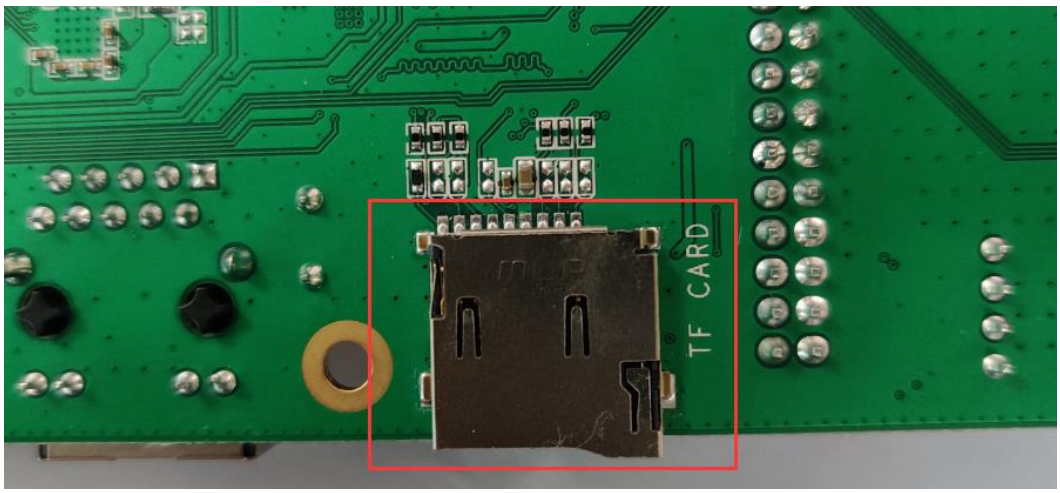


Figure 3-14 TF Card Interface (bottom surface)

3.13 MIPI Input Interface

The MIPI video input interface connected a horizontal connector with a pitch of 0.5mm.

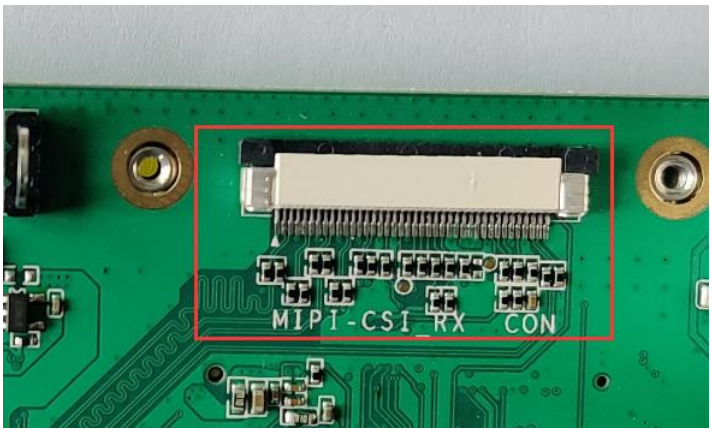


Figure 3-15 MIPI CSI_RX Video Input Interface

The MIPI CSI_RX interface signal sequence is as follows:

Table 3-1 MIPI CSI_RX Signal Definition:

1	GND
2	MIPI_CSI_RX_D0N_CON
3	MIPI_CSI_RX_D0P_CON
4	GND
5	MIPI_CSI_RX_D1N_CON
6	MIPI_CSI_RX_D1P_CON
7	GND
8	MIPI_CSI_RX_CLK0N_CON
9	MIPI_CSI_RX_CLK0P_CON
10	GND
11	MIPI_CSI_RX_D2N_CON
12	MIPI_CSI_RX_D2P_CON
13	GND
14	MIPI_CSI_RX_D3N_CON
15	MIPI_CSI_RX_D3P_CON
16	GND
17	MIPI_MCLK0
18	GND
19	NC
20	MIPI_RST0
21	CAMERA0_PDN
22	DVP_PWERN0
23	I2C4_SCL_M0_CAM
24	I2C4_SDA_M0_CAM
25	PWM14_M0
26	GND
27	GND
28	VCC5V0_MIPICON
29	VCC5V0_MIPICON
30	VCC5V0_MIPICON
31	GND
32	NC
33	CAMERA1_PDN
34	MIPI_RST1
35	GND
36	MIPI_MCLK1
37	GND
38	MIPI_CSI_RX_CLK1N_CON
39	MIPI_CSI_RX_CLK1P_CON
40	GND

3.14 MIPI/LVDS Output Interface

The MIPI/LVDS video output interface connected a vertical connector with a pitch of 1mm, and MIPI DSI/LVDS_TX0 is the default display interface.

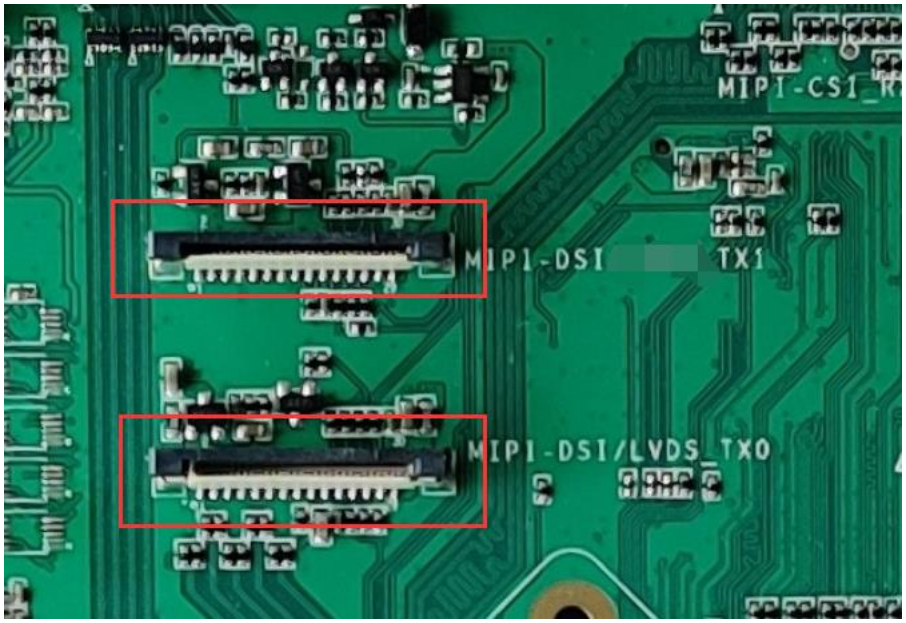


Figure 3-16 MIPI DSI/LVDS_TX0 and MIPI DSI _TX1 Video Input Interface

The MIPI DSI/LVDS_TX0 interface signal sequence is as follows:

Table 3-2 MIPI DSI/LVDS_TX0 Signal Definition

1	GND	
2		MIPI_DSI_TX0_D0N
3	MIPI_DSI_TX0_D0P	
4		GND
5	MIPI_DSI_TX0_D1N	
6		MIPI_DSI_TX0_D1P
7	GND	
8		MIPI_DSI_TX0_CLKN
9	MIPI_DSI_TX0_CLKP	
10		GND
11	MIPI_DSI_TX0_D2N	
12		MIPI_DSI_TX0_D2P
13	GND	
14		MIPI_DSI_TX0_D3N
15	MIPI_DSI_TX0_D3P	
16		GND
17	LCD0_BL	
18		NC
19	VCC3V3_LCD0	
20		LCD0_RST
21	LCD0_ID	
22		LCD0_PWREN_H

23	I2C_SCL_TP0	
24		ISC_SDA_TP0
25	TP_INT	
26		TP_RST
27	GND	
28		VCC5V0_LCD_0
29	VCC5V0_LCD_0	
30		VCC5V0_LCD_0

The MIPI DSI_TX1 interface signal sequence is as follows:

Table 3-3 MIPI DSI _TX1 Signal Definition

1	GND	
2		MIPI_DSI_TX1_D0N
3	MIPI_DSI_TX1_D0P	
4		GND
5	MIPI_DSI_TX1_D1N	
6		MIPI_DSI_TX1_D1P
7	GND	
8		MIPI_DSI_TX1_CLKN
9	MIPI_DSI_TX1_CLKP	
10		GND
11	MIPI_DSI_TX1_D2N	
12		MIPI_DSI_TX1_D2P
13	GND	
14		MIPI_DSI_TX1_D3N
15	MIPI_DSI_TX1_D3P	
16		GND
17	LCD1_BL_PWM	
18		NC
19	VCC3V3_LCD1	
20		LCD1_RST
21	LCD1_ID	
22		LCD1_PWREN_H
23	I2C_SCL_TP1	
24		ISC_SDA_TP1
25	TP1_INT	
26		TP1_RST
27	GND	
28		VCC5V0_LCD_1
29	VCC5V0_LCD_1	
30		VCC5V0_LCD_1

3.15 HDMI Output Interface

The development board supports HDMI output with HDMI2.0 protocol, supports up to 4K@60Hz, and HDMI A type output interface.

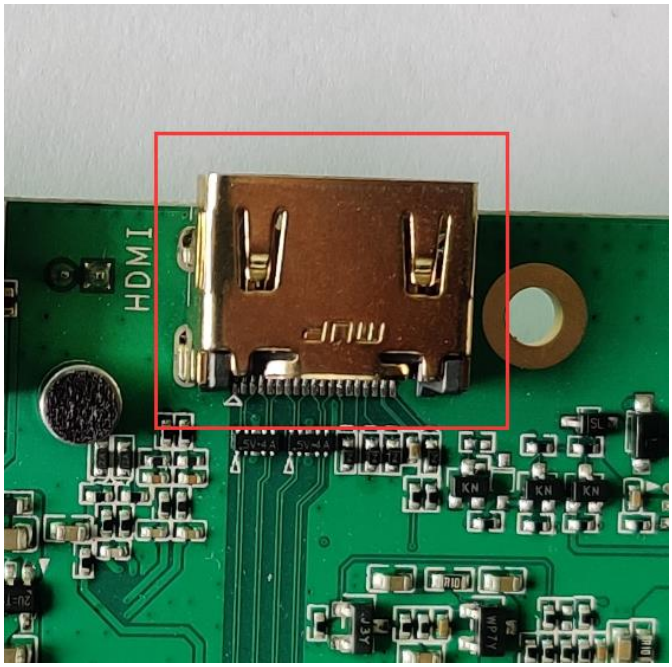


Figure 3-17 HDMI Output Interface

3.16 eDP Output Interface

The eDP signal is converted to VGA signal output by default. If eDP output is needed, jumper resistors and capacitors are needed. Remove resistors R5909, R5910, R5911, R5912 and capacitors C5905, C5908, and add resistors R5606, R5607, R5609, R5610 and capacitors C5600, C5601.

The eDP output interface uses a vertical connector with a pitch of 1mm.

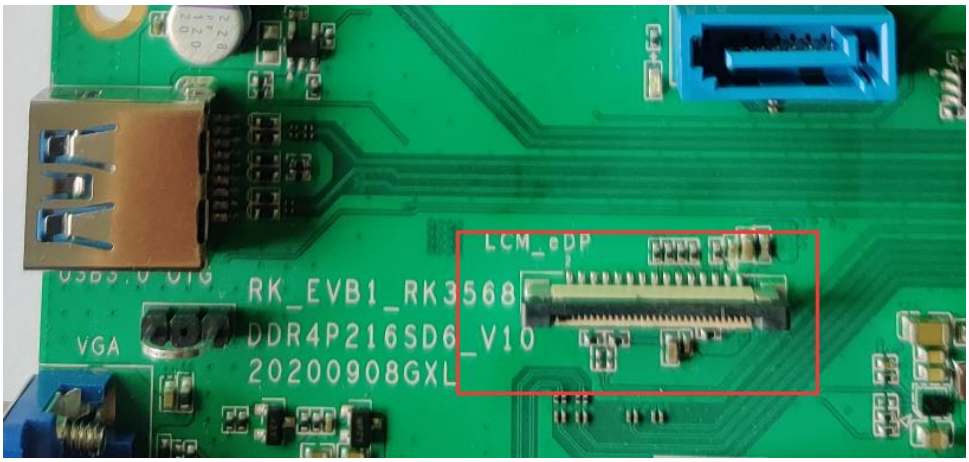


Figure 3-18 EDP Video Output Interface

The signal sequence of the eDP video output interface is as follows:

Table 3-4 eDP Video Signal Definition

1	GND	
2		eDP_TX_D0N_CON
3	eDP_TX_D0P_CON	
4		GND
5	eDP_TX_D1N_CON	
6		eDP_TX_D1P_CON
7	GND	
8		eDP_TX_AUXN_CON
9	eDP_TX_AUXP_CON	
10		GND
11	eDP_TX_D2N_CON	
12		eDP_TX_D2P_CON
13	GND	
14		eDP_TX_D3N_CON
15	eDP_TX_D3P_CON	
16		GND
17	LCD0_BL	
18		NC
19	VCC3V3_LCD0	
20		LCD0_RST
21	SARADC_VIN2_LCD_ID	
22		LCD0_PWREN_H
23	I2C1_SCL_TP_CON	
24		I2C1_SDA_TP_CON
25	TP_INT_L_GPIO0_B5_CON	
26		TP_RST_L_GPIO0_B6_CON
27	GND	
28		VCC5V0_LCDeDP
29	VCC5V0_LCDeDP	
30		VCC5V0_LCDeDP

3.17 VGA Output Interface

The eDP signal is converted to VGA signal through RTD2166 chip, and external standard VGA socket is convenient to connect VGA monitor

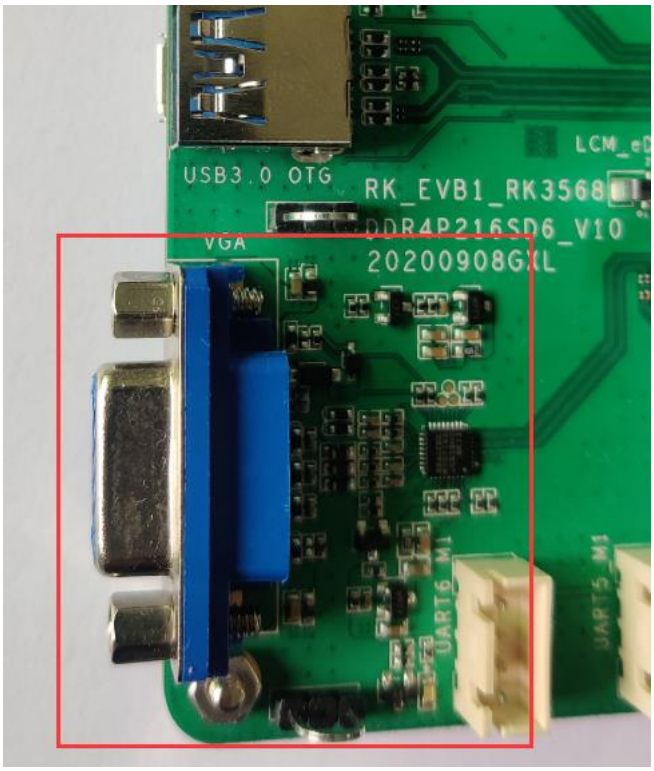


Figure 3-19 VGA Output Interface

3.18 Audio Input and Output Interface

The development board supports Headphone, SPK (8ohm/1.3W) and MIC functions; the digital MIC array interface is reserved to debug external MIC devices, and supports up to 8 channels.

The MIC output of RK809 is connected to MIC device by default. DIP switch S7000: 1-8, 2-7 are set to ON, 3-6, 4-5, are set to OFF; if RK809's SPK is needed for output recovery function, the MIC signal has to be connected to the SPK output signal, the DIP switch S7000: 1-8, 2-7 are set to OFF, 3-6, 4-5 are switch to ON

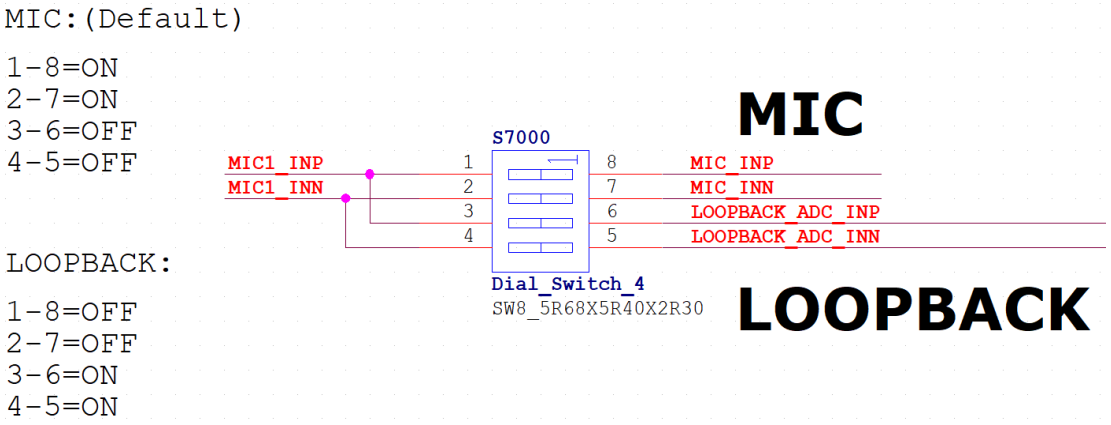


Figure 3-20 MIC and Loopback DIP Switch Selection Circuit

The MIC array interface uses RK809+PDM by default, the DIP switch S1900 is set to ON and S1901 is set to OFF; if it has to connect the I2S signal of RK3568 to the extension interface, set the DIP switch S1900 to OFF and S1901 to ON.

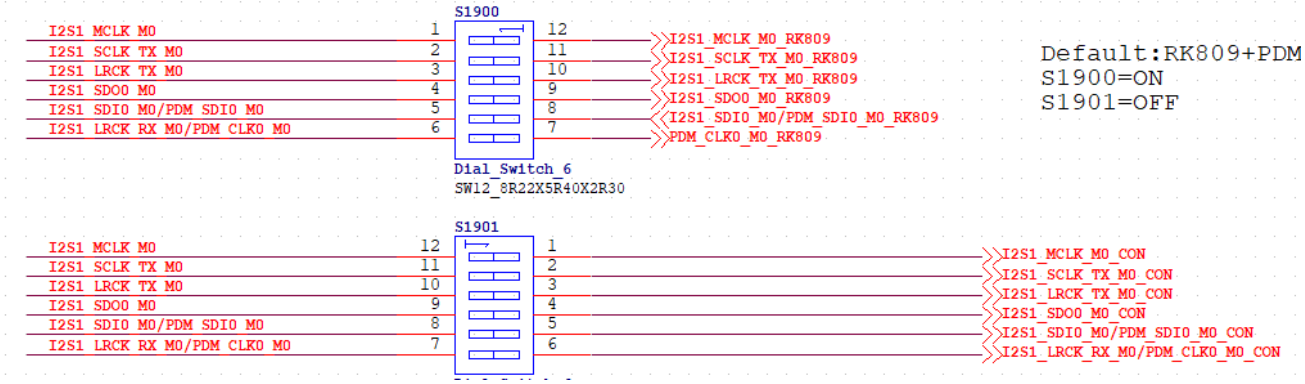


Figure 3-21 DIP Switch Selection Circuit of I2S1 Channel

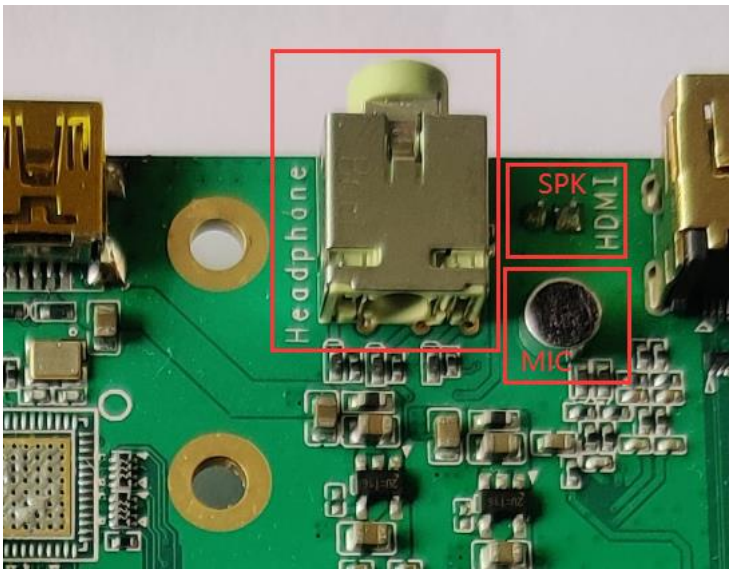


Figure 3-22 Headphone, SPK and MIC Interface

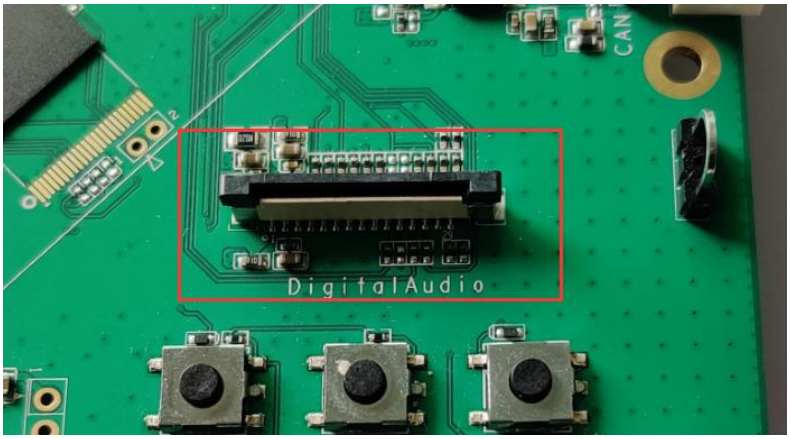


Figure 3-23 Audio MIC Array Interface

The audio MIC array interface signal sequence is as follows:

Table 3-5 Audio MIC Array Signal Definition

1	VCC5V0_SYS	
2		VCC5V0_SYS
3	VCCIO1	
4		GND
5	GND	
6		VCC_3V3
7	GND	
8		HP_DET_L_GPIO3_C2
9	GND	
10		I2S1_MCLK_M0_CON
11	GND	
12		I2S1_SCLK_RX_M0/PDM_CLK1_M0_CON
13	GND	
14		I2S1_SCLK_TX_M0_CON
15	GND	
16		I2S1_LRCK_RX_M0/PDM_CLK0_M0_CON
17	GND	
18		I2S1_LRCK_TX_M0_CON
19	I2S1_SDO0_M0_CON	
20		I2S1_SDO1_M0/I2S1_SDI3_M0 /PDM_SDI3_M0_CON
21	I2S1_SDO2_M0/I2S1_SDI2_M0 /PDM_SDI2_M0_CON	
22		I2S1_SDO3_M0/I2S1_SDI1_M0 /PDM_SDI1_M0_CON
23	I2S1_SDI0_M0/PDM_SDI0_M0_CON	
24		I2S1_SDO3_M0/I2S1_SDI1_M0 /PDM_SDI1_M0_CON
25	I2S1_SDO2_M0/I2S1_SDI2_M0 /PDM_SDI2_M0_CON	
26		I2S1_SDO1_M0/I2S1_SDI3_M0 /PDM_SDI3_M0_CON
27	GND	
28		PA_EN_H_GPIO3_C3
29	I2C3_SDA_M0	
30		I2C3_SCL_M0

3.19 CIF/EBC/RGMII/BT656 Extension Interfaces

The development board reserves CIF, EBC, RGMII, BT656 and other signal extension interfaces to facilitate users to debug the corresponding peripherals. If you need to change the extension interface, jumper resistors are needed, and you need to add the resistors corresponding to the signal, and remove the resistors accordingly. Due to the large number of networks, it will not go into much details here.

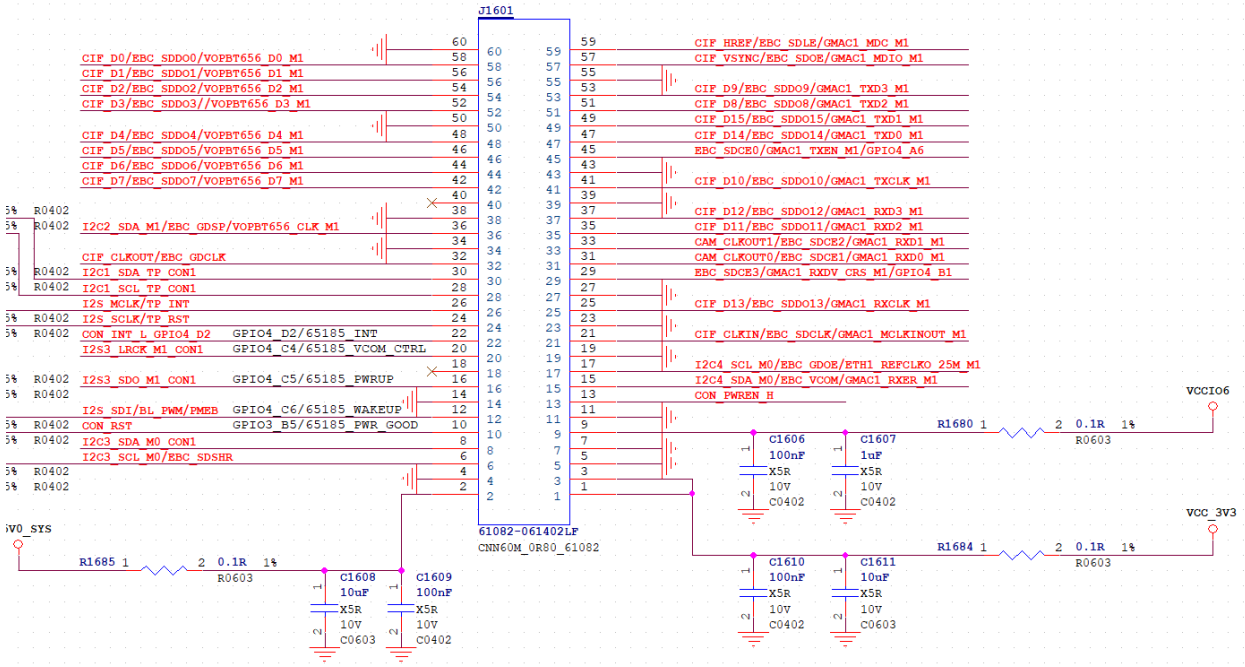


Figure 3-24 CIF, EBC, RGMII, BT656 Extension Interfaces

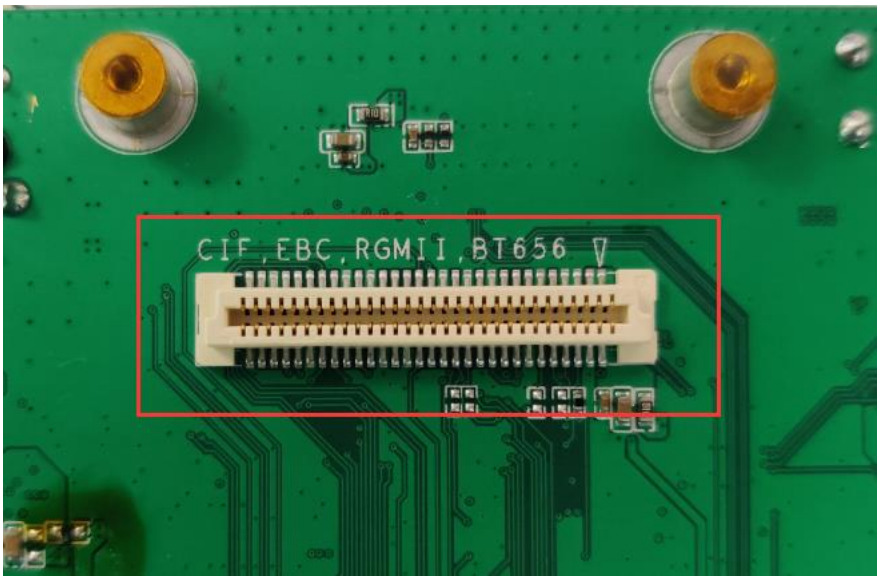


Figure 3-25 CIF, EBC, RGMII, BT656 Extension Interfaces (bottom surface)

CIF、EBC、RGMII、BT656 extension interfaces signal sequence is as follows:

Table 3-6 CIF, EBC, RGMII, BT656 Extension Interfaces Signal Definition

1	VCC_3V3	2	VCC5V0_SYS
3	VCC_3V3	4	GND
5	GND	6	I2C3_SCL_M0/EBC_SDSHR
7	GND	8	I2C3_SDA_M0_CON1
9	VCCIO6	10	CON_RST
11	GND	12	I2S_SDI/BL_PWM/PMEB
13	CON_PWREN_H	14	GND
15	I2C4_SDA_M0/EBC_VCOM/GMAC1_RXER_M1	16	I2S3_SDO_M1_CON1
17	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1	18	NC
19	GND	20	I2S3_LRCK_M1_CON1
21	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1	22	CON_INT_L_GPIO4_D2
23	GND	24	I2S_SCLK/TP_RST
25	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1	26	I2S_MCLK/TP_INT
27	GND	28	I2C1_SCL_TP_CON1
29	EBC_SDCE3/GMAC1_RXDV_CRS_M1/GPIO4_B1	30	I2C1_SDA_TP_CON1
31	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1	32	CIF_CLKOUT/EBC_GDCLK
33	CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1	34	GND
35	CIF_D11/EBC_SDDO11/GMAC1_RXD2_M1	36	I2C2_SDA_M1/EBC_GDSP/VOPBT656_CLK_M1
37	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1	38	GND
39	GND	40	NC
41	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1	42	CIF_D7/EBC_SDDO7/VOPBT656_D7_M1
43	GND	44	CIF_D6/EBC_SDDO6/VOPBT656_D6_M1
45	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1	46	CIF_D5/EBC_SDDO5/VOPBT656_D5_M1
47	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1	48	CIF_D4/EBC_SDDO4/VOPBT656_D4_M1
49	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1	50	GND
51	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1	52	CIF_D3/EBC_SDDO3//VOPBT656_D3_M1
53	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M1	54	CIF_D3/EBC_SDDO3//VOPBT656_D3_M1
55	GND	56	CIF_D1/EBC_SDDO1/VOPBT656_D1_M1
57	CIF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1	58	CIF_D0/EBC_SDDO0/VOPBT656_D0_M1
59	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1	60	GND

3.20 USB OTG/HOST Interface

The Development board with USB OTG and USB HOST interface:

- USB3.0 OTG consists of 2 USB3.0 high-speed signal lines and one OTG signal line, and is connected to USB3.0 standard-A type interface, and reserves standard micro USB2.0 interface which is backward compatible with USB 2.0 specifications. Therefore, this interface can be used to download and upgrade firmware, or as a USB3.0 HOST.

- USB3.0 HOST1 uses USB3.0 Standard-A interface and is backward compatible with USB 2.0 specification.

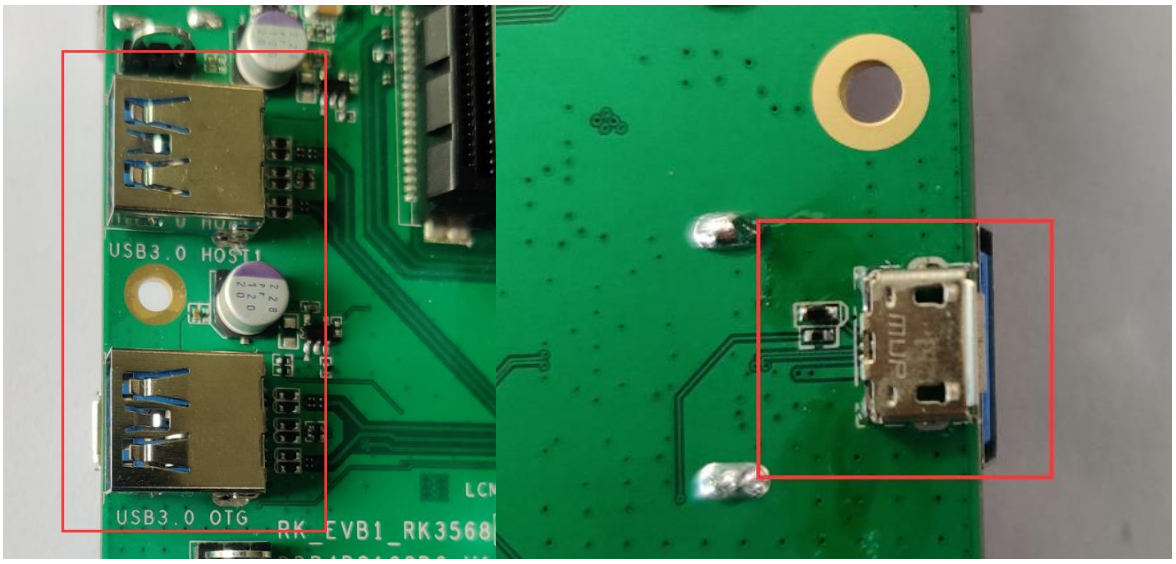


Figure 3-26 USB3.0 OTG, micro USB2.0 OTG and USB3.0 HOST1 Interface

- USB2.0 HOST2/3 takes USB2.0 Standard-A type interface, which is convenient to connect USB2.0 peripherals such as U disk and mouse directly.

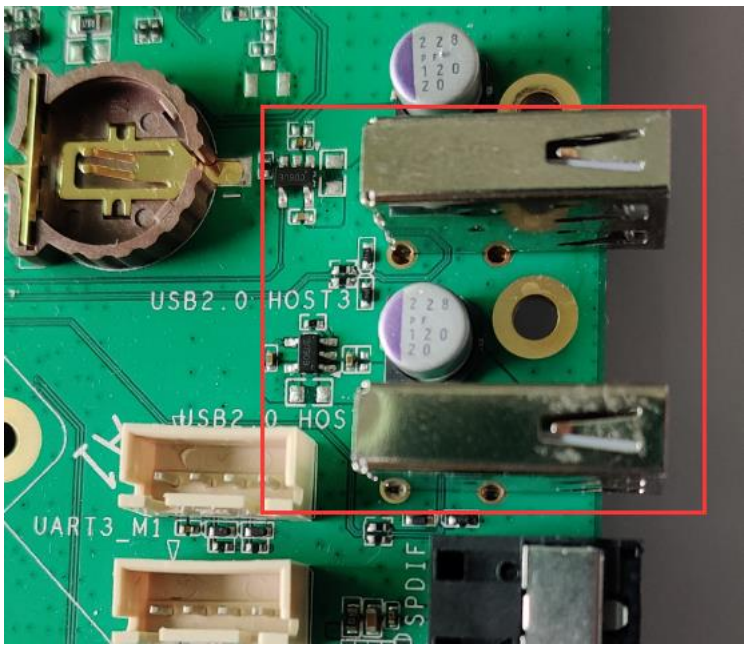


Figure 3-27 USB2.0 HOST2/3 Interface

3.21 Ethernet Interface

The development board supports two RJ45 interfaces and provide dual Gigabit Ethernet connections. Both channels use the Gigabit Ethernet MAC integrated inside RK3568 and are connected to an external PHY chip with the model of RTL8211F-CG, and the features are as follows:

- Compatible with IEEE802.3 standard, support full-duplex and half-duplex operation, support cross detection and self-adaptation.

- Support 10/100/1000M data rate.
- The interface uses RJ45 interface units with isolation transformer and indicator light

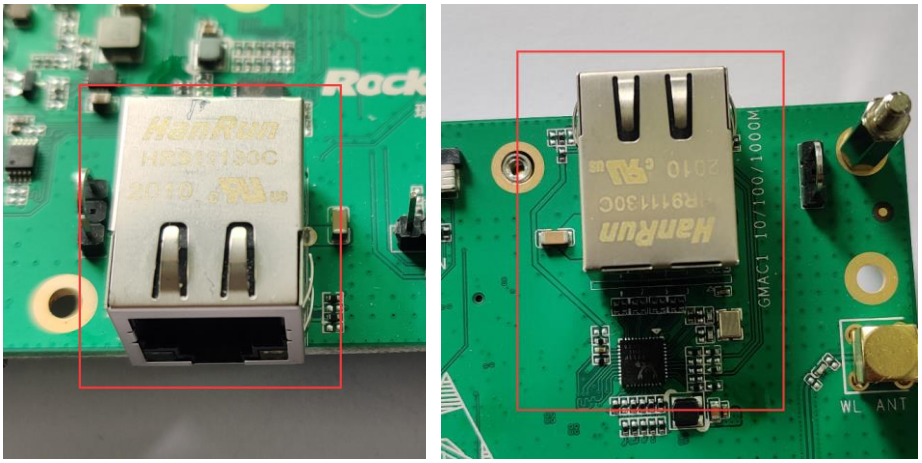


Figure 3-28 RJ45 Interface

3.22 PCIe Interface

The development board uses a standard PCIe3.0 connector, and an external PCIe board can be installed for communication.

- Working mode: Root Complex (RC).
- Supports 2 lane data interface.
- The 100MHz clock is provided by an external clock chip.

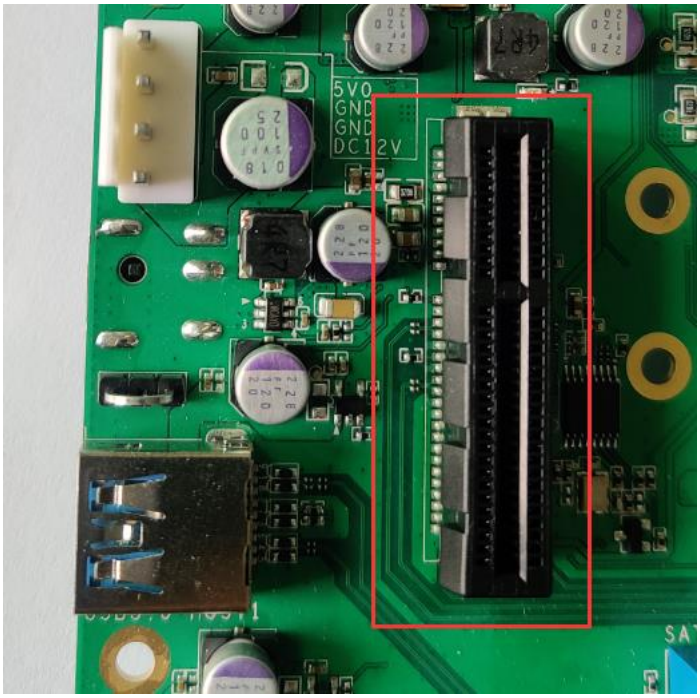


Figure 3-29 PCIe3.0 Connector

3.23 SATA Interface

The development board supports SATA3.0, and the connector is standard SATA interface. SATA 12V power

supply needs another adapter for power supply. There is a channel reserved for system 12V to directly supply power to SATA hard disk. It is not turned on by default. If necessary, you need to add the magnetic bead FB8301 (or a 0R resistance).

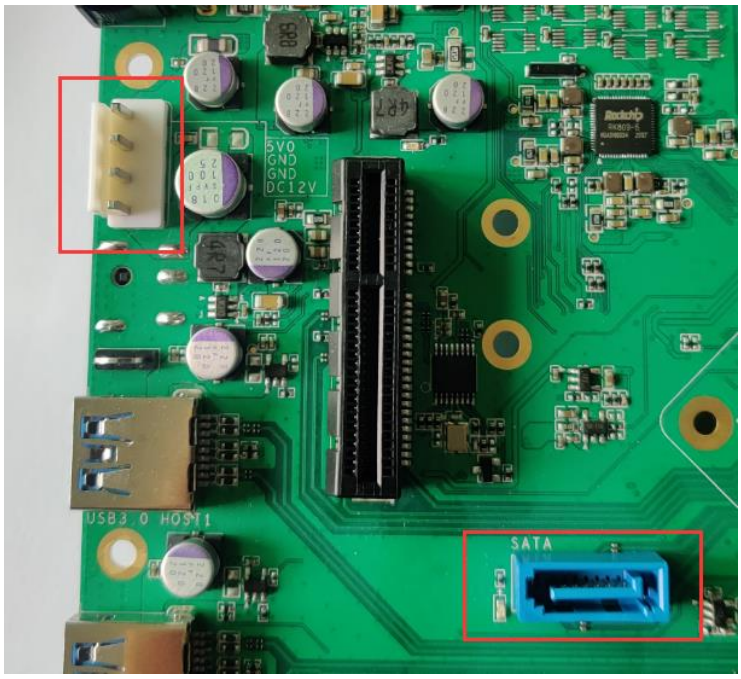


Figure 3-30 SATA Signal and Power Interface

3.24 WIFI

The WIFI+BT module on the development board uses Taiwan AMPAK AP6398S, with the following features:

- Support 2x2 WIFI (2.4G and 5G, 802.11 a/b/g/n/ac), BT5.0 function, 2 external SMA interface antennas.
- BT data communication in UART mode.
- BT audio is connected to the PCM interface of the controller.
- WIFI data uses 4bits SDIO data bus.

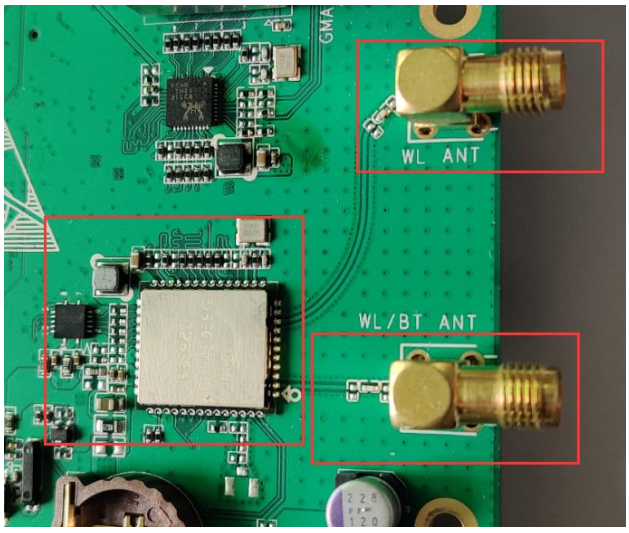


Figure 3-31 WIFI Module and SMA Antenna InterfaceNotice

4 Notice

RK3568 EVB is suitable for lab or project environment. Please read the following notices before operation:

- It is not allow to hot-plug the screen interface and extension board of the EVB anyway.
- Before unpacking and installing the EVB, please take the necessary anti-static measures to avoid the damage to the hardware of the EVB caused by ESD;
- Please hold the edge of the EVB, and do not touch the exposed metal part of the EVB so as to avoid the electrostatic damage to the components of the EVB;
- Please place the EVB on a dry plane to keep them away from heat source, electromagnetic interference source and radiation source, electromagnetic radiation sensitive equipment (such as medical equipment) and so on.