Secure Grade： Top-secret(　　) Secret(　　) Privacy(　　) Public(√)

RK3566 Hardware Design Guide

（Hardware Department）

Status： [　] Draft [　] Modifying [√] Released	**Version：**	1.1.0
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	Date：	2022-02-06
	Approver：	Reviewer
	Date：	2022-02-06

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Revision History

The revision history accumulates instructions for each update of the document and the latest version includes updates of all previous versions.

Version	Author	Revision Date	Revision Description
V1.0.0	Daniel. J	2021.06.03	1st Released Version
V1.1.0	Daniel. J	2022.02.06	Modified some descriptions

Preface

Overview

This document mainly describes the key points of hardware design and notices for RK3566 processor, aiming to help RK customers shorten the product design cycle, improving the product design stability and reducing the failure rate. Please refer to the requirements in this guide to do the hardware design, and suggest to use the relevant core templates released by Rockchip. If you need to make changes for specific reasons, please adhere to the design rules of high-speed-digital-circuit and RK Schematic & PCB checklist requirements.

Chip Type

This document is suitable for ：**RK3566**

Applicable Object

This document is mainly suitable for below:

- Product Hardware Development Engineers
- Field Application Engineers
- Test Engineers

Related Reference Documents

- RK3566_PinOut: Pin list, Ball map, GPIO information, Pin delay, Usage of unused pins;
- Rockchip_RK3566_High_Speed_PCB_Design_Guide: Design guide of high speed signals, Layout requirements and suggestions;
- RK356X Power Consumption Test Report： Reference data about power consumption；
- Rockchip_RK3566_IO_Power_Domain_Checklist： Checklist of THE IO power domain；
- Rockchip_RK3566_Schematic_and_PCB_Review_Checklist： schematic diagram、 PCB check table；
- Rockchip_RK3566_Hardware_Design_Guide： Hardware Design Guide；

Abbreviation

Acronym includes the abbreviations of commonly used phrases in this document:

Abbreviation	English Interpretation	Chinese Interpretation
ARM/CPU	ARM based Central Processing Unit	基于 ARM 的中央处理器
Acodec	Audio Codec	音频编解码器
CEC	Consumer Electronics Control	消费电子控制
CIF	Camera Input Format	相机并行接口
CSI	Camera Serial Interface	相机串行接口
DC/DC	Direct Current-Direct Current Convertor	直流/直流转换器
DDR	Double Data Rate	双倍速率同步动态随机存储器
DP	Display Port	显示接口
DSI	Display Serial Interface	显示串行接口
EBC	E-book Controller	电子书控制器
eDP	Embedded Display Port	嵌入式数码音视频传输接口
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
ESD	Electro-Static Discharge	静电释放
ESR	Equivalent Series Resistance	等效电阻
FSPI	Flexible Serial Peripheral Interface	灵活串行外设接口
GPU	Graphics Processing Unit	图形处理器
GMAC	Gigabit Media Access Controller	千兆媒体访问控制器
HDMI	High-Definition Multimedia Interface	高清晰度多媒体（接口）
I^2C/I2C	Inter-Integrated Circuit	内部整合电路(线式串行通讯总线）
I2S	Inter-IC Sound	集成电路内置音频总线
ISP	Image Signal Processing	图像信号处理
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1 兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LVDS	Low-Voltage Differential Signaling	低电压差分信号（接口）
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器（接口）
NPU	Netural-network Processing Unit	神经网络处理器
PCIe	Peripheral Component Interconnect Express	外设组件互联标准
PDM	Pulse Density Modulation	脉冲密度调制（接口）
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
PWM	Pulse Width Modulation	脉冲宽度调制

Rockchip	Rockchip Electronics Co., Ltd.	瑞芯微电子股份有限公司
RGMII	Reduced Gigabit Media Independent Interface	简化千兆媒体独立接口
RMII	Reduced Media Independent Interface	简化媒体独立接口
SARADC	Successive Approximation Register Analog to Digital Converter	逐次逼近寄存器型模数转换器
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output Card	安全数字输入/输出卡
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPI/FSPI	(Flexible)Serial Peripheral Interface	（灵活）串行外设（接口）
SPDIF	Sony/Philips Digital Interface Format	索尼/飞利浦数字音频接口
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
TSADC	Temperature Sensing Analog to Digital Converter	温度感应模数转换器
VOP	Video Output Processor	视频输出处理器
VPU	Video Processing Unit	视频处理器
UART	Universal Asynchronous Receiver/Transmitter	通用异步收发传输器
USB	Universal Serial Bus	通用串行总线

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1 Introduction

1.1 Overview

RK3566 is a high-performance, low-power, quad-core application processor chip, designed for personal mobile Internet devices and AIoT devices. It can be widely used in Android /Linux applications such as tablets, education tablets, speakers with screen, dictionary pens, cloud terminals, video conferencing systems. It can also be applied to consumer-grade or lightweight AI application scenarios with screens.

Many embedded powerful hardware engines are provided to optimize performance for highend application. RK3566 supports almost full-format H.264 decoder by 4K@60fps, H.265 decoder by 4K@60fps, also support H.264/H.265 encoder by 1080p@60fps, high-quality JPEG encoder/decoder.

RK3566 has an embedded 3D GPU, which is fully compatible with OpenGL ES1.1/2.0/3.2、OpenCL 2.0 and Vulkan 1.0. The special MMU 2D hardware engine can maximize the display performance and provide smooth operation.

The embedded NPU supports INT8/INT16 hybrid operations. In addition, with its strong compatibility, you can easily transform network models based on frameworks such as TensorFlow/MXNet/PyTorch/Caffe.

RK3566 has a high-performance memory interface (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X) to provide the memory bandwidth required in high-performance scenarios.

1.2 Block Diagram

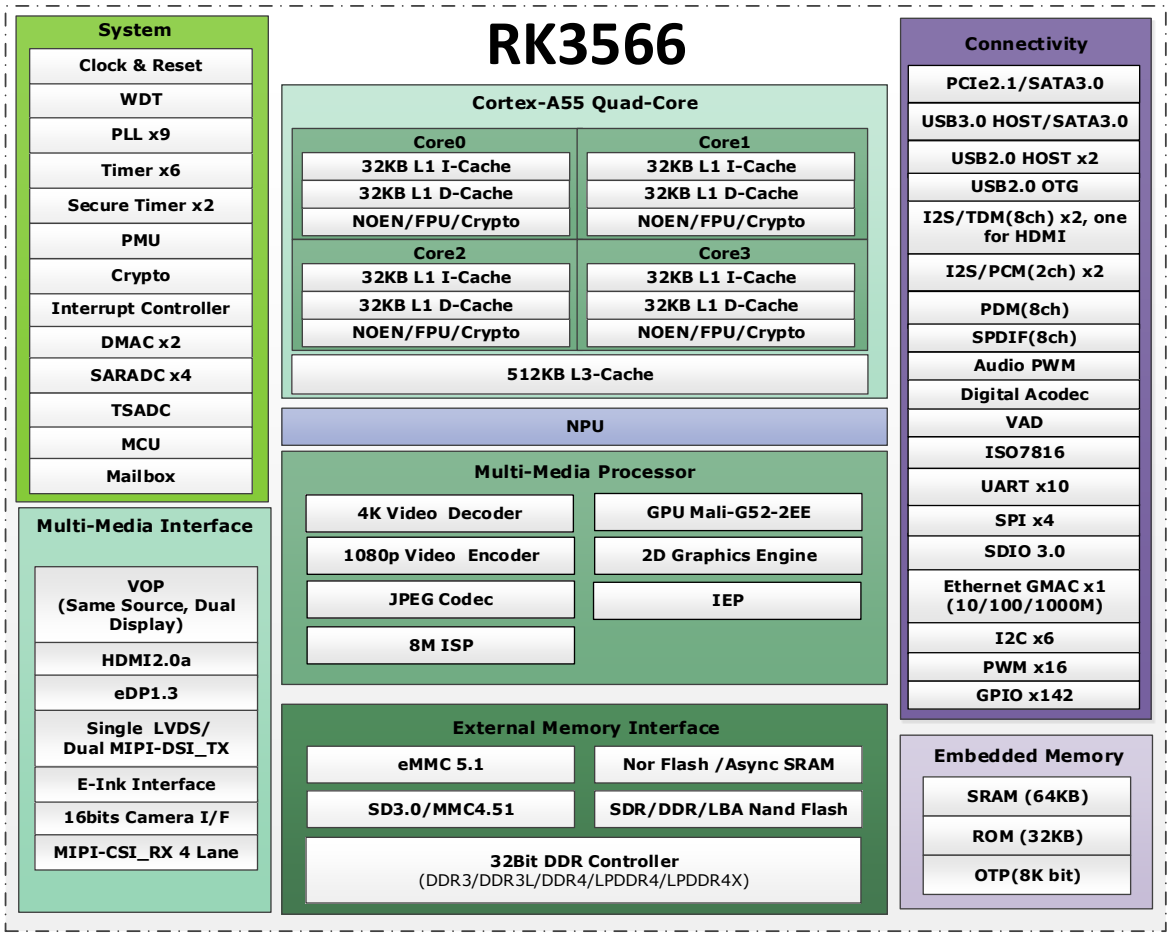


Figure 1-1 RK3566 Block Diagram

1.3 Application Block Diagram

1.3.1 RK817-5 Application Block Diagram

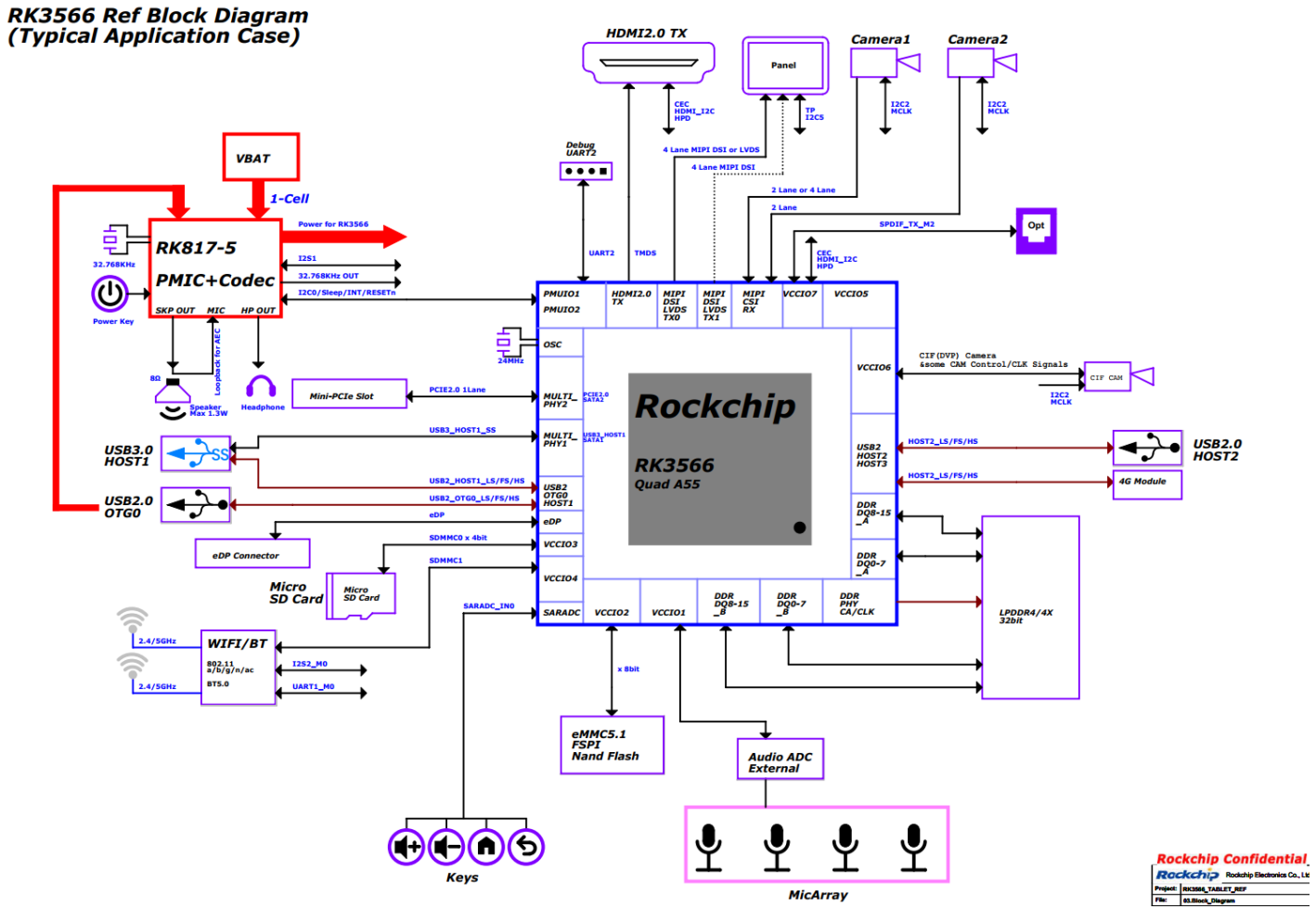


Figure 1-2 RK3566 RK817-5 Application Block Diagram

1.3.2 RK809-5 Application Block Diagram

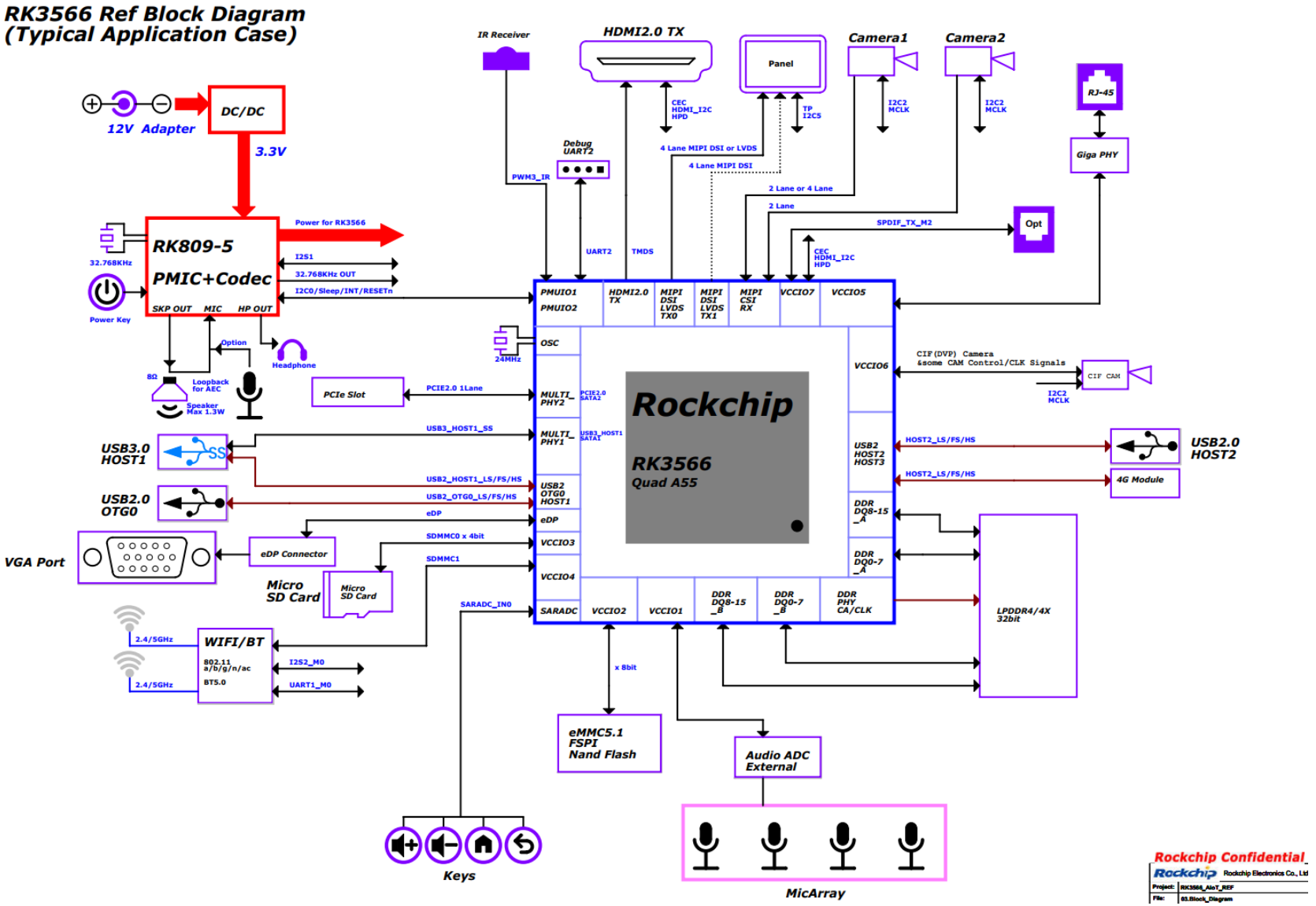


Figure 1-3 RK3566 RK809-5 Application Block Diagram

2 Hardware Design Recommendation

2.1 Minimum System Design

2.1.1 Clock Circuit

RK3566 internal oscillator circuit and the external 24MHz crystal together constitute the system clock circuit. The recommended crystal connection mode and device parameters are shown in Figure 2-1. The 22ohm resistor connected in series in XOUT24M network must be retained to limit the current and prevent overdrive. Do not change the 1M resistor between XOUT24M and XIN24M networks.

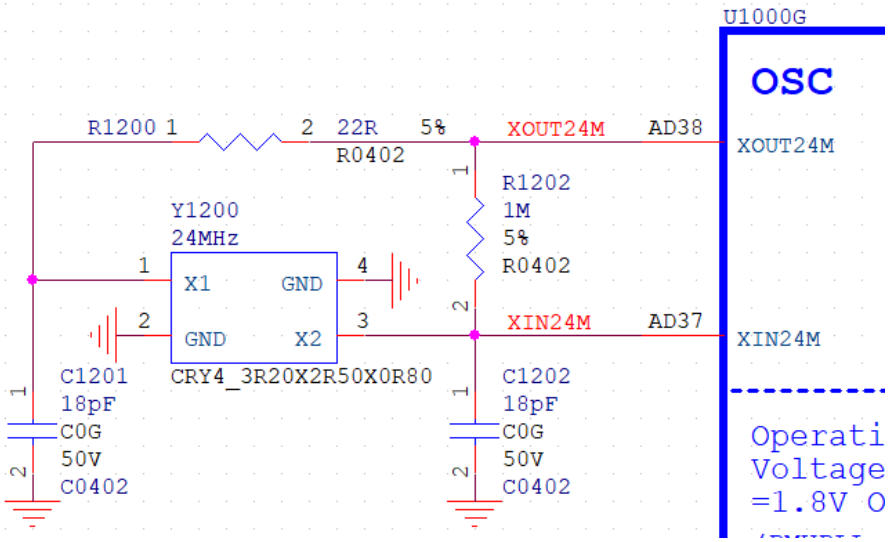


Figure 2-1 RK3566 Crystal Implementation

Note

The selected capacitor needs to match the crystal load capacitor, and the material is recommended to be NPO/COG. It is recommended to use 4-Pin SMT crystals, in which two GND pins are fully connected to the ground to enhance the anti-ESD interference ability of the system clock. 18pF is the capacitance value of crystal used by RK, not a general value.

The system clock can also be generated by an external oscillator circuit with a clock amplitude of 1.8V. The clock is input through the XIN24M pin, and the XOUT24M pin is left floating. The clock parameters are shown in the following table 2-1:

Table 2-1 RK3566 24mhz Digital Clock Source

Parameter	Spec.			Description
	Min.	Max.	Unit	
Frequency	24.000000		MHz	
Frequency Tolerance	+/-20		ppm	frequency tolerance range
Clock Amplitude	1.8		V	Peak-to-Peak value
Operating Temperature	-20	80	℃	
ESR	/	40	Ohm	

In standby state, RK3566 can reduce the system power consumption by reducing the system clock frequency. At this time, you can use the PVTM (Process Voltage Temperature Monitor) module inside the chip PMU to provide 32.768k clock, or the external input 32.768k clock can be used. In the case of extreme power consumption requirements for deep sleep, you should choose to use an external clock, which is input from the CLK32K_IN pin.

In the standby state, it supports IO interrupt wake-up in the power domains of PMUIO0, PMUIO1 and PMUIO2. If the required wake-up source is related to the 24MHz clock, the 24MHz clock cannot be turned off.

The external 32.768KHz RTC clock parameters are shown as below table:

Table 2-2 RK3566 32.768khz Clock Requirement

Parameter	Spec.			Description
	Min.	Max.	Unit	
Frequency	32.768000		kHz	
Frequency Tolerance	+/-30		ppm	frequency tolerance range
Clock Amplitude	0.65*VDD	VDD+0.3	V	VDD indicates the power voltage of the PMUIO2 power domain
Operating Temperature	-20	80	℃	
Duty Ratio	50		%	

2.1.2 Reset Circuit

The hardware reset of the RK3566 is input by the nPOR (RESET) pin, and the low level is active. In order to ensure the stability and normal operation of the chip, the minimum reset time required is 100 cycles of the 24MHz main clock, that is, which means at least 4us or more.

The reset signal needs to be connected in parallel with a 100nF capacitor close to the pin to eliminate jitter on the reset signal, enhance anti-interference ability, and prevent abnormal system reset caused by false trigger. The pull up level of the RESET pin should be consistent with the IO power domain (PMUIO1) where the nPOR pin is located.

Refer to the PMIC RK809-5 or RK817-5 power supply solution. After each power supply of the default output of the PMIC is powered on, the RESET pin will change the output level from low to high to complete the RESET action after a delay(ensure the power is all ready). When the PMIC is in working or SLEEP mode, if the RESET pin level is pulled low, the PMIC will restart. The power-on sequence of this restart is the same as the default.

If the matching PMIC is not used in the design and the power supply is realized by discrete devices, an

independent reset IC should be selected for RK3566 or the reset signal should be obtained from other chips.

Related circuits are shown in the figure. During layout, keep away from interference signals, interference devices, metal connectors, and edges of the PCB board. Make a ground guard for signals, and drill vias in the ground path with a interval distance of no more than 300mil.

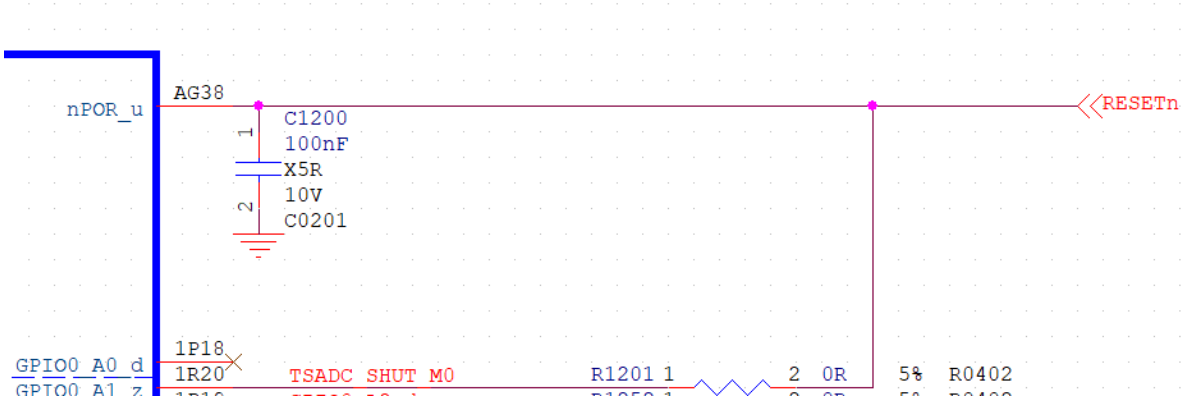


Figure 2-2 RK3566 Reset Input

2.1.3 Watchdog/TSADC Circuit

RK3566 integrates a Watchdog Timer. When a reset signal is generated, a low level will output from TSADC_SHUT_M0 or TSADC_SHUT_M1 pin, and resets RK3566 by hardware.

RK3566 integrates two TSADC(Temperature-sensor ADC) modules. When the internal temperature of the chip exceeds the threshold, the internal TSHUT signal can be sent to the CRU module to reset the RK3566. It can also output low level through TSADC_SHUT_M0 or TSADC_SHUT_M1 pin to reset RK3566 by hardware.

As shown in the figure 2-2, the TSADC_SHUT_M0 is connected to the RESETn network.

2.1.4 PMU Circuit

In order to meet the requirement of low power consumption products, RK3566 has designed a power management unit (PMU) to control and manage the internal power supply of the chip.

It should be noted that some functions or modules cannot work in the sleep state. For a detailed list of divisions, please refer to the description of the voltage domain (VD), power domain (PD) and related descriptions in the PMU chapter of the TRM document.

2.1.5 System Boot Sequence

RK3566 supports multiple booting ways. After the system is reset, the embedded boot code will automatically boot in the following order. The priority from high to low as below:

- Serial Nor Flash (FSPI)
- Serial Nand Flash (FSPI)
- Nand Flash
- eMMC Flash
- SDMMC Card

If there is no firmware in the memory medium, when connecting to the PC through the USB OTG0 interface, a Maskrom device will be found in the burning tool (the corresponding driver needs to be installed), and the firmware

can be burned at this time

2.1.6 System Initialization Configuration Signal

There are two important signals in RK3566 that will affect the system boot configuration, which need to be configured and kept stable before power-on. They are:

- Level configuration pin FLASH_VOL_SEL for VCCIO2 (FLASH) power domain;
- JTAG/SDMMC multiplexing function control pin SDMMC0_DET;

After the system reset, the chip will configure the default power-on function of the corresponding module according to the input level of the two pins.

The I/O level mode of the RK3566 VCCIO2 power domain requires hardware configuration. Because the power domain belongs to the FLASH power domain, which affects the system boot. When the system power on, the default level mode must be specified by hardware configuration and cannot be adjusted by register operation. The following figure shows the configuration.

- When the I/O level of VCCIO2 and the flash interface is 1.8V, the FLASH_VOL_SEL pin must be kept high level during the reset;
- When the I/O level of VCCIO2 and the flash interface is 3.3V, the FLASH_VOL_SEL pin must be kept low level during the reset;

The pin configuration must match the actual IO power supply of the external memory interface to prevent system stability or damage

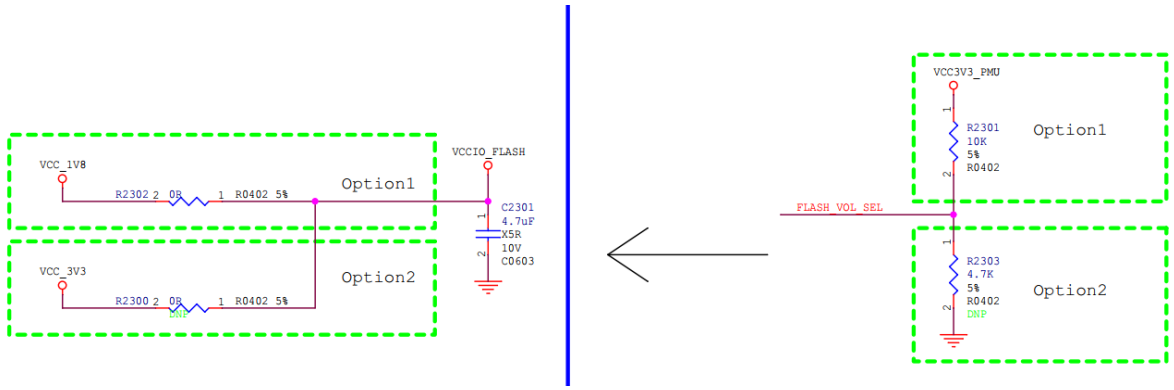


Figure 2-3 Correspondence Between RK3566 FLASH_VOL_SEL Pin Level And VCCIO2 Status

RK3566 reuses JTAG function and SDMMC function together to reduce IO pin count and take into account the convenience of the complete machine debugging. The SDMMC0_DET pin is used to switch the output function. Therefore, this pin must be configured before power-on. Otherwise, the debugging during the boot period will be affected if JTAG has no output, and SDMMC0 has no output will affects SDMMC boot.

- SDMMC0_DET pin detects that the level is high, the IO switches to the JTAG function;
- SDMMC0_DET detects that the level is low (normal state of SD card insertion, and the PIN is pulled down by SD card slot), the IO function is switched to SDMMC;

The pin is shown as below:

Figure 2-4 RK3566 SDMMC0/JTAG Reused Control Pin

The two pins configurations are shown in below table:

Table 2-3 RK3566 System Initialization Configuration Signal Description

Signal Name	Internal Pull Up/Down	Description
FLASH_VOL_SEL	pull up	FLASH (VCCIO2) power domain IO supply configuration pin: 0: IO level mode is 3.3V; 1: IO level mode is 1.8V;
SDMMC0_DET	pull up	JTAG function selection pin: 0: recognized as sd card insertion, SDMMC/JTAG/UART pin reused as SDMMC function. 1: recognized as SD card not insertion, SDMMC/JTAG/UART pin reused as JTAG/UART function (default).

2.1.7 JTAG Debug Circuit

The ARM_JTAG interface of RK3566 conforms to the IEEE1149.1 standard. PC can connect to the DSTREAM emulator through SWD mode (two-line mode) to debug ARM Core inside the chip. At the beginning of the design, it is recommended to reserve test points for these two signals.

Before connecting the emulator, ensure that the SDMMC0_DET pin is at a high level, otherwise the JTAG debugging mode cannot be entered. The configuration of this pin is described in the previous section. The ARM_JTAG interface description is as follows:

Table 2-4 RK3568 JTAG debug interface signal

Signal name	Description
ARM_JTAG_TCK	JTAG clock input in SWD mode
ARM_JTAG_TMS	JTAG data input and output in SWD mode

The connection method of JTAG and the definition of standard connector pins are shown in the figure below. Generally, only need to reserve test points according to the reference schematic for the first version. There is no need to reserve for the stable version.

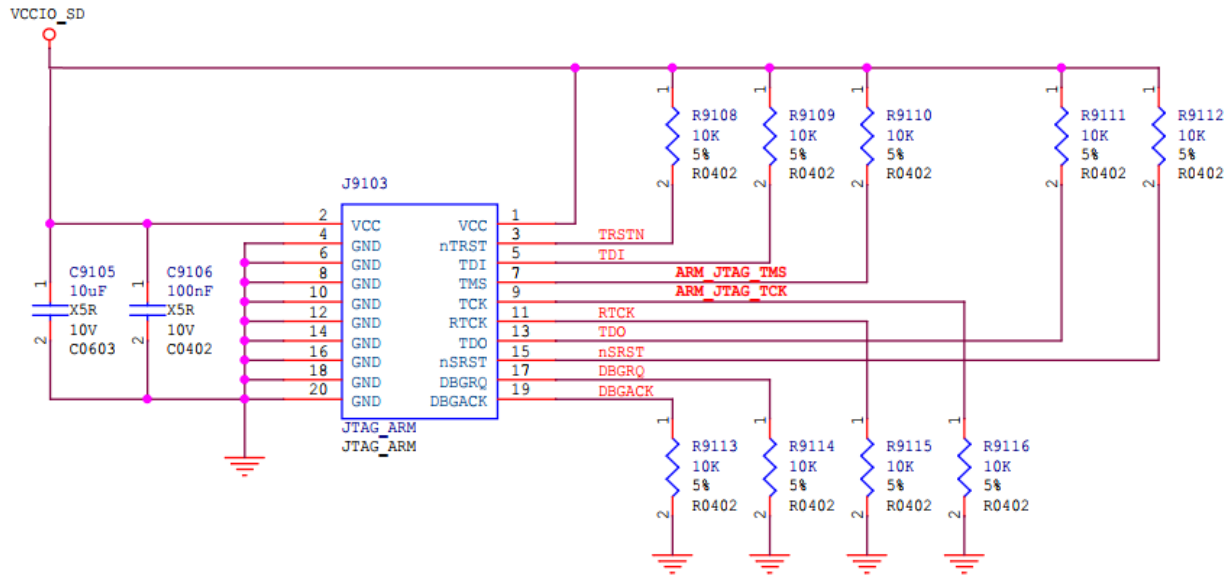


Figure 2-5 RK3566 JTAG Connection Circuit In SWD Mode

The MCU_JTAG module of RK3566 is temporarily closed to the public and no special treatment is required.

2.1.8 UART Debug Circuit

For details about this section, see section “Debugging UART Circuits”

2.1.9 DDR Circuit

2.1.9.1 DDR Controller Introduction

RK3566 DDR controller interface supports JEDEC SDRAM standard interface, the controller has the following features

- Support DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X standards;
- In DDR3/DDR3L/DDR4 interface mode, supports a 32-bit data bus width, 2 ranks (chip selection), and a maximum address of 8GB;
- In LPDDR3/LPDDR4/LPDDR4X interface mode, it supports a 32-bit data bus width, 4 ranks (chip selection), and a maximum address of 8GB;
- Support low power consumption modes such as Power Down and Self Refresh;

2.1.9.2 DDR Topology and Connection Guide

In order to simplify user design of DDR and ensure system reliability, the official layout template is provided for mainstream DDR chip and types, which users can refer to. The reference to the schematic and template must be strictly consistent, including power decoupling capacitors.

Taking LPDDR3 as an example, the SDRAM topology of RK3566 is shown in the following figure, and the topology of other DDR particles refer to the specific schematic diagram.

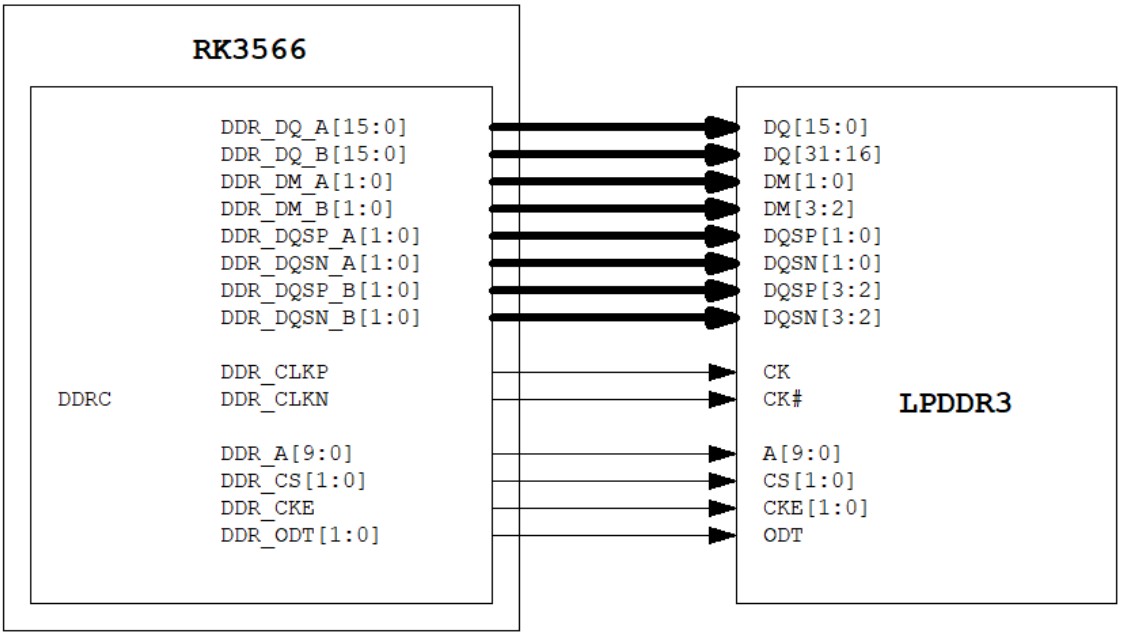


Figure 2-6 RK3566 LPDDR3 Topological Structure

For customers who need to do DDR Layout by themselves, the following limitations should be noted:

- DDR3/DDR3L:
  - Support the whole group swap between Byte. Support DQ swap within a Byte group.
  - The CA order cannot be swapped and must be assigned according to the reference schematic.
  - If you want to support templates compatible with 16bit/32bit, you must use the template provided by RK, and changes are not allowed.
- LPDDR3
  - It is necessary to maintain the one-to-one correspondence between D0-D7 of the DDR terminal and D0-D7 of the RK3566 LPDDR3 controller, and ensure the one-to-one correspondence between the associated DQS and DM, this Byte group does not support adjustment.
  - Other Byte support whole group exchange.
  - DQ in other bytes support swap.
  - The CA order can not interchangeable and must be assigned according to the reference schematic.
- DDR4
  - Support the whole group swap between Byte groups.
  - Support DQ swap within a Byte group.
  - The CA order cannot be swapped and must be assigned according to the reference schematic.
  - If you want to support templates compatible with 16bit/32bit, you must use the template provided by RK, and changes are not allowed.
- LPDDR4/LPDDR4X
  - The DQ and CA order cannot be swap and must be assigned according to the reference schematic.

2.1.9.3 Description of DQ Connection of LPDDR3

As mentioned in the previous section, the D[7:0] Byte of LPDDR3 does not support adjustment. Please keep the corresponding relationship between the D[7:0] of DDR and the DQ of RK3566, as well as the corresponding

relationship between the associated DQS, as shown in the figure below. Do not change.

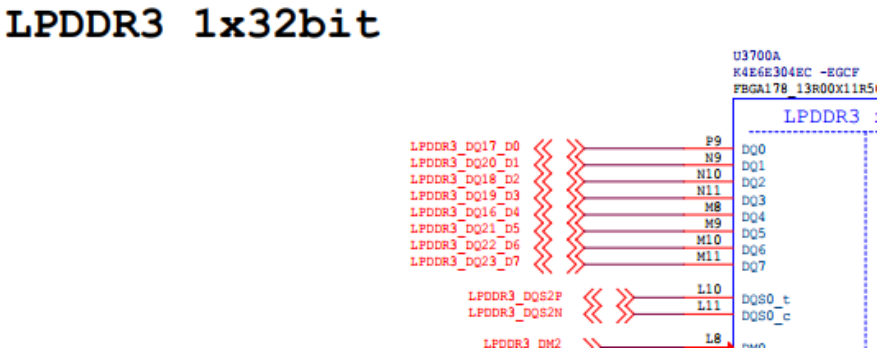


Figure 2-7 DQ[7:0] connection description of LPDDR3 particle

2.1.9.4 DDR Power Up Sequence Requirement

For DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 type memory, RK3566 DDR controller has only one set of power supply: DDR_VDDQ, DDR_VDDQ is used for DDR controller's Core power supply interface I/O power supply and output buffer power supply

For LPDDR4X type memory, RK3566 DDR controller needs two sets of power supplies: DDR_VDDQ and DDR_VDDQL, the latter is the power supply for the output buffer.

The supply voltage of VDDQ/VDDQL corresponding to different particles is shown in the figure:

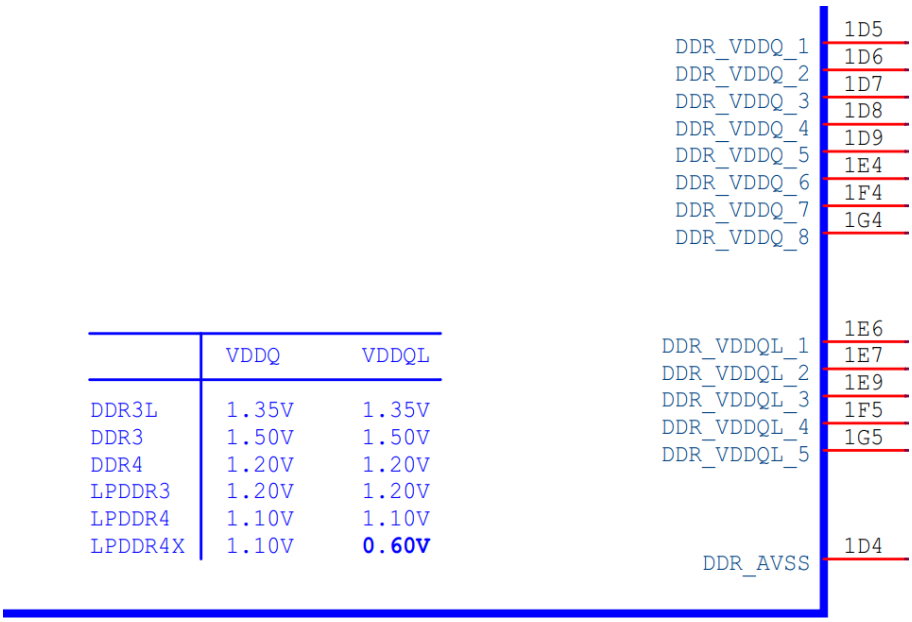


Figure 2-8 Different DDR particles correspond to VDDQ/VDDQL supply voltage

SDRAM usually include two sets of power supplies. Please refer to the JEDEC standard of the respective SDRAM chip for the power-on sequence. A brief introduction is as follows:

The power-on sequence of DDR3/DDR3L SDRAM is shown in the figure below:

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2-9 DDR3 SDRAM's power-on sequence

The power-on sequence of LPDDR3 SDRAM is shown in the figure below:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{Ref} must always be less than all other supply voltages

Figure 2-10 LPDDR3 SDRAM's power-on sequence

The power-on sequence of DDR4 SDRAM is shown in the figure below:

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD}-V_{DDQ}) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to TBDV max once power ramp is finished, AND
   - VrefCA tracks TBD.

   or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

Figure 2-11 DDR4 SDRAM's power-on sequence

The power-on sequence of LPDDR4 SDRAM is shown in the figure below:

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x V_{DD2}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

Table 5 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

NOTE 1 Ta is the point when any power supply first reaches 300 mV.
NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.
NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not excess 100 mV.

Figure 2-12 LPDDR4 SDRAM's Power-on Sequence

2.1.9.5 DDR RZQ Signal Processing

Noted that the connection method of DDR_RZQ is different due to the type of DDR chip:

When using DDR3/DDR3L/DDR4/LPDDR3, DDR_RZQ needs to be pulled down through a 1% precision 120ohm resistor;

When using LPDDR4/LPDDR4X, DDR_RZQ should be pulled up to the VCC_DDR power supply through a 1% precision 120ohm resistor.

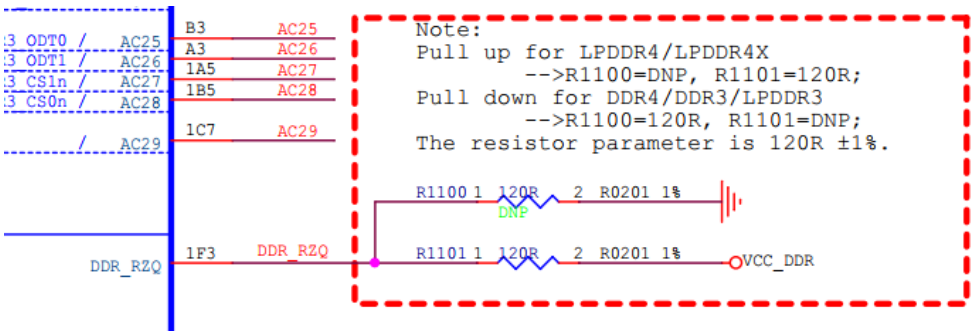


Figure 2-13 Description of DDR RZQ Connection

2.1.9.6 DDR VREFOUT Voltage Output Connection Usage

DDR PHY of RK3566 can provide voltage to the VREFDQ or VREFCA of the SDRAM chip. The specific connection usage for different SDRAM are as follows:

- DDR3/DDR3L: provide VREFDQ for DDR3/DDR3L, the default voltage is 0.75/0.675V, the output voltage value can be adjusted through registers; VREFCA of DDR3/DDR3L is still obtained through voltage divider circuit of VCC_DDR;
- LPDDR3: provide VREFDQ for LPDDR3, the voltage is related to ODT configuration, the output voltage value can be adjusted through registers; VREFCA of LPDDR3 is still obtained through voltage divider circuit of VCC_DDR;
- DDR4: provide VREFCA for DDR4, the default voltage is 0.6V, and the voltage value can be adjusted through the register;
- LPDDR4/LPDDR4X: No need to use.

2.1.9.7 DDR Support List

The maximum working frequency of RK3566 DDR is greatly affected by layout. Most of the official templates can support the maximum working frequency up to 1056MHz. For the specific rate, please refer to the relevant instructions of the DDR template file in the release information.

It is recommended that customers select the official DDR template for design to ensure the reliability and stability of the system. If you have to design by yourself, please consult RK for more detailed layout restrictions.

For the DDR chip Support List, please refer to the RK DDR Support List, which can be downloaded on the Redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.10 eMMC Circuit

2.1.10.1 eMMC Controller Introduction

The features of RK3566 eMMC controller are as follows:

- Compatible with standard iNAND interface;
- Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
- Support three data bus widths of 1-bit, 4-bit and 8-bit;
- Support HS200 mode;
- Support CMD Queue;

2.1.10.2 eMMC Topology and Connection Guide

Recommended pull up/down and the matching design of eMMC interface are as Table 2-5. The pull-up resistance of D0 and CMD signals must be reserved, and the pull-down resistance of DATA_STROBE signal is recommended to be reserved.

The capacitance of the VDDi pin of the eMMC chip must be 2.2uF, or a larger capacitance value as required by the specific particle specification.

Table 2-5 RK3566 eMMC Interface Design

Signal	Internal pull up/down	Connection method	Description (chip side)
eMMC_DQ[7:0]	pull up	Direct connection, D0 pull-up with a external 10K ohm resistor, other data use the inside pull-up resistor	eMMC data send/receive
eMMC_CLK	pull down	connect 22ohm resistor in series with RK3566 output end.	eMMC clock output
eMMC_DATA_STROBE	pull down	Direct connection; Reserve pull-down resistors	eMMC clock input
eMMC_CMD	pull up	Direct connection; Pull with external 10K resistance	eMMC command send/receive

2.1.10.3 eMMC Power Up Sequence Requirement

The eMMC controller of RK3566 belongs to VCCIO2 power domain, with only one group of power supply, so it is no timing sequence requirements. But it should be noted that the level of the power supply needs to match the FLASH_VOL_SEL state configuration mentioned above.

The eMMC has two sets of power supplies, refer to JEDEC standard for power-on sequence:

- VCC and VCCQ have no sequential requirements on the power-on sequence;
- VCC and VCCQ must be powered on and maintain a stable working voltage before the CMD command is generated;
- After the chip enters sleep mode, RK3566 can turn off the VCC power to reduce power consumption;
- Before the chip is awakened from sleep mode, the VCC power supply must be powered on and maintain a stable operating voltage;

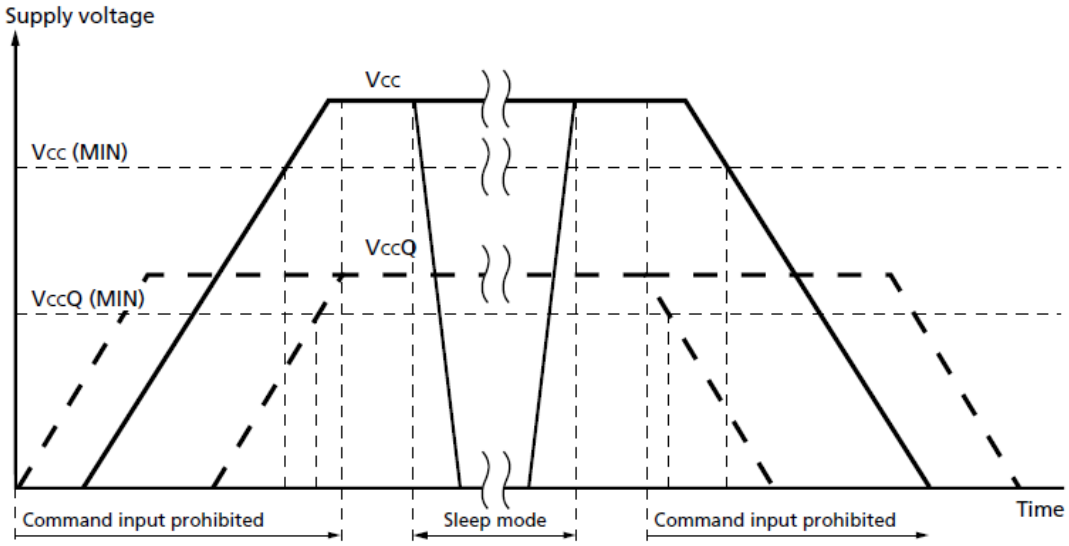


Figure 2-14 eMMC power up/down sequence

2.1.10.4 MASKROM Download Test Point Description

Please reserve the test point of eMMC D0/CLK in the development process to avoid the failure of entering the Maskrom download mode while the firmware fails. Refer to the reference schematic for the reservation method. The branch of the test point and signal routing should be strictly shortened during layout.

2.1.10.5 eMMC Support List

RK3566 eMMC support list please refer to *RK eMMC Support List* released by Rockchip. The document can be downloaded from redmine through below link:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.11 Nand Flash Circuit Design

2.1.11.1 Nand Flash Controller Introduction

- RK3568 Nand Flash controller has the following features:
- Supports SLC, MLC, TLC Nand Flash;
- Supports asynchronous flash memory interface with 8-bit data width;
- Supports ONFI synchronous flash memory interface with 8-bit data width;
- Supports Toggle flash memory interface with 8-bit data width;
- Support 16-bit BCH/ECC.

2.1.11.2 Nand Flash Topology and Matching Design

Recommended pull up/down and the matching design of Nand Flash interface are as follows, the pull-up resistors of FLASH_RDY/FLASH_CS0n/FLASH_CS1n must be reserved:

Table 2-6 RK3566 Nand Flash interface design

Signal	Internal pull up/down	Connection Method	Description (chip side)
FLASH_D[7:0]	pull up	direct connection	Nand Flash data send/receive
FLASH _WRn	pull up	direct connection	Nand Flash Writing enable
FLASH _DQS	pull down	direct connection	Nand Flash data strobe
FLASH _CLE	pull down	direct connection	Nand Flash Command latch enabled
FLASH _WPn	pull down	direct connection	Nand Flash write protected
FLASH _ALE	pull down	direct connection	Nand Flash address latch enabled
FLASH _RDY	pull up	direct connection, external pull-up with a 4.7K ohm resistor	Nand Flash Ready/busy state
FLASH _RDn	pull up	direct connection	Nand Flash read enable
FLASH _CS0n	pull up	direct connection; external pull-up with a 4.7K ohm resistor	Nand Flash Chip select 0
FLASH _CS1n	pull up	direct connection; external pull-up with a 4.7K ohm resistor	Nand Flash Chip select 1

2.1.11.3 Nand Flash Power up Sequence Requirement

The Nand Flash controller of RK3566 chip belongs to the VCCIO2 power domain, only one power supply, so there is no sequence requirements. But it should be noted that the level of the power supply needs to match the FLASH_VOL_SEL state configuration mentioned above.

Nand Flash chip has two sets of power supplies, please refer to JEDEC standard for power-on sequence.

Once V_{CC} and VccQ reach the V_{CC} minimum and VccQ minimum values, respectively, listed in Table 5 and power is stable, the R/B_n signal shall be valid after RB_valid_Vcc and shall be set to one (Ready) within RB_device_ready, as listed in Table 16. R/B_n is undefined until 50 µs has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Parameter	Raw NAND	EZ NAND
RB_valid_Vcc	10 µs	250 µs
RB_device_ready	1 ms	2 ms

Table 16 R/B_n Power-on Requirements

During power-on, VccQ shall be less than or equal to Vcc at all times. Figure 19 shows VccQ ramping after Vcc, however, they may ramp at the same time.

Figure 2-15 Nand Flash power-on/down sequence

2.1.11.4 Nand Flash Download Test Point Description

Please reserve the test point of FLASH D0/CLK in the development process to avoid the failure of entering the Maskrom download mode while the firmware fails. Refer to the reference schematic for the reservation method. The branch of the test point and signal routing should be strictly shortened during layout.

2.1.11.5 Nand Flash Support List

For RK3566 Nand Flash support list, please refer to the document "RK Nand Flash Support List", which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.12 FSPI Flash Circuit

2.1.12.1 FSPI Controller Introduction

FSPI is a flexible serial interface controller. There is a FSPI controller in RK3566, which can be used to connect FSPI devices.

The features of RK3566 FSPI controller are as follows:

- Support serial NOR and NAND FLASH;
- Support SDR mode; support single/dual/four-line mode;
- Support two chip select

2.1.12.2 FSPI Topology and Connection Guide

Recommended pull up/down and the matching design of FSPI Flash interface are as shown in Table2-7, where the external pull-up resistors of the FSPI_D2/FSPI_D3 pins must be reserved:

Table 2-7 RK3566 FSPI Interface Design

Signal	Internal pull up/down	Connection Method	Description (chip side)
FSPI_D[3:0]	D2 pull down D0/D1/D3 pull up	Direct connection	SPI data send/receive
FSPI0_CLK	Pull down	Series connect 22ohm resistor	SPI clock output
FSPI0_CS0n	Pull up	Direct connection	SPI chip select signal 0
FSPI0_CS1n	Pull down	Direct connection	SPI chip select signal 1

2.1.12.3 FSPI Support List

The FSPI Flash controller of RK3566 chip belongs to the VCCIO2 power domain, only one power supply, so there is no sequence requirements. But it should be noted that the level of the power supply needs to match the FLASH_VOL_SEL state configuration mentioned above.

SPI FLASH chip only has one set of power supplies, so there is no timing requirement.

2.1.12.4 FSPI Download Test Point Description

Please reserve the test point of FSPI D0/CLK in the development process to avoid the failure of entering the Maskrom download mode while the firmware fails. Refer to the reference schematic for the reservation method. The branch of the test point and signal routing should be strictly shortened during layout.

2.1.12.5 SPI Support List

RK3566 SPI support list, please refer to the document *RK SpiNor and SLC Nand Support List*, which can be downloaded from Rockchip redmine platform:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

Note

FSPI_CS1n is multiplexed with the DATA STROBE pin of eMMC, while other pins of FSPI have no multiplexing relationship with eMMC. Therefore, when FSPI only uses one chip select, eMMC can be used at the same time. For example, use FSPI as boot and eMMC as large capacity storage.

2.1.13 GPIO Circuit

There are 10 independent IO power domains in RK3566, which are PMUIO[0:2] and VCCIO[1:7]. Among them:

- PMUIO0 and PMUIO1 are fixed level power supply domain and cannot be configured;
- PMUIO2 and VCCIO1, VCCIO[3:7] power supply domains require that the hardware power supply voltage

match the configuration of the software:

- When the hardware IO level is connected to 1.8V, the software voltage should be configured to 1.8V;
- When the hardware IO level is connected to 3.3V, the software voltage should be configured to 3.3V;

- VCCIO2 Power domain does not need a software configuration, but the hardware power supply voltage must match the FLASH_VOL_SEL status:
  - When the VCCIO2 power supply is 1.8V, the FLASH_VOL_SEL pin must remain high level;
  - When the VCCIO2 power supply is 3.3V, the FLASH_VOL_SEL pin must be kept low level;

Otherwise, there will be the following risks:

- Software configuration is 1.8V while hardware power supply is 3.3V, which will make the IO in an overvoltage state, and the IO will be damaged if it works for a long time;
- Software configuration is 3.3V while hardware power supply is 1.8V, IO function will be abnormal;

If the power domain is changed in the customer project, voltage configurations must be updated. All kinds of documents from RK have emphasized this note. Please ask the customer's software and hardware engineer to review the correctness of the voltage configuration of their respective projects.

Reference documents:

1） DTS configuration notes： https://redmine.rock-chips.com/documents/106

2） Checklist： Rockchip_RK3566_IO_Power_Domain_Checklist_V1.0_CN.xlsx

2.1.13.1 GPIO Pins Description

Take the pin GPIO2_A3_u as an example, where _u indicates that the default reset state of this IO is internal pull-up; similarly, _d indicates that the default state is internal pull-down, and _z indicates that the default state is high-impedance state.

Except for the boot-related GPIO mentioned above, the default state of other IOs are all inputs after reset.

For function pins name with the suffix _M0/_M1/_M2, it means that the same function pin is multiplexed on different IOs, and only one of them can be used at the same time. And it should be noted that the same group of function pins can only be used in combination with the same suffix. For example, when selecting the UART2 function, you can choose the combination of UART2_TX_M0 and UART2_RX_M0, or the combination of UART2_TX_M1 and UART2_RX_M1. Different multiplexing suffix IO cannot be selected for combination.

2.1.13.2 GPIO Driving Capability

In RK3566, GPIO provides multiple levels of adjustable drive strength, which are Level 0-5. Some GPIOs can achieve Level 0-11 adjustment levels. For details, please refer to the *RK3566_PinOut* document. In addition, depending on the different type of GPIO, the initial default drive strength is different. Please refer to the chip TRM for configuration modification. You can also refer to the "Support Drive Strength" and "Default IO Drive Strength" columns in Table 5 in the *RK3566_PinOut* document.

2.1.13.3 GPIO Power

The power pin of GPIO power domain is described as below:

Table 2-8 RK3566 GPIO power pin description

Power domain	GPIO Type	Pin Name	Description
PMUIO0	Fixed 1.8V	PMUPLL_AVDD_1V8	1.8V Only IO supply for this GPIO domain (group).
PMUIO1	Fixed 3.3V	PMUIO1	3.3V Only IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO7	1.8V/3.3V	VCCIO7	1.8V or 3.3V IO supply for this GPIO domain (group).

PMUIO0 and PMUIO1 are fixed-level power domains and cannot be configured. Other IO domains can be configured.

The power supply ripple of the GPIO power domain is required to be within ±5%, and at least one 100nF decoupling capacitor should be placed nearby for each power supply pin. See the reference schematic for the detailed design.

If all IOs in one power domain are not used, then the power domain do not need a power supply, and the corresponding pins can be left floating.

2.2 Power Design

2.2.1 Minimum System Power Introduction

2.2.1.1 Power Requirement

Table 2-9 RK3566 power requirement

Module	Power Pin	Description
PMU PLL	PMUPLL_AVDD_0V9、 PMUPLL_AVDD_1V8	PMU PLL power
SYSTEM PLL	SYSPLL_AVDD_0V9、 SYSPLL_AVDD_1V8	System PLL power
CPU	VDD_CPU	CPU/ARM Core power
GPU	VDD_GPU	GPU power
NPU	VDD_NPU	NPU power
LOGIC	VDD_LOG	SOC logic power
PMU LOGIC	PMU_VDD_LOGIC_0V9	PMU logic power
DDR	VCC_DDR	DDR PHY power
GPIO	PMUIO0、PMUIO1、PMUIO2、 VCCIO1、VCCIO2、VCCIO3、 VCCIO4、VCCIO5、VCCIO6、VCCIO7	IO Domain power
SARADC	SARADC_AVDD_1V8	SARADC power
OTP	OTP_VCC18	OTP power
USB2.0 PHY	USB_AVDD1_0V9、USB_AVDD1_1V8、 USB_AVDD1_3V3、USB_AVDD2_0V9、 USB_AVDD2_1V8、USB_AVDD2_3V3	USB2.0 PHY power
MULTI PHY	MULTI_PHY_AVDD_0V9、 MULTI_PHY_AVDD_1V8	MULTI PHY power（include: USB3.0、SATA、PCIe）
MIPI CSI PHY	MIPI_CSI_RX_AVDD_0V9、 MIPI_CSI_RX_AVDD_1V8、	MIPI CSI RX PHY power
MIPI DSI/LVDS PHY	MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9、 MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8、 MIPI_DSI_TX1_AVDD_0V9、 MIPI_DSI_TX1_AVDD_1V8	MIPI DSI TX PHY/LVDS PHY power
eDP PHY	EDP_TX_AVDD_0V9、 EDP_TX_AVDD_1V8	eDP PHY power
HDMI PHY	HDMI_TX_AVDD_0V9、 HDMI_TX_AVDD_1V8	HDMI TX PHY power

2.2.1.2 Power on Sequence

Theoretically, follow the power-on principle of "the same module is powered on low voltage first, and power on high voltage later", "equal voltage in same module is powered on at the same time", and "no timing requirements between different modules". The RESETn should release not be less than 10ms after the last power is stable.

The recommended power-on sequence of the RK3566 is as follows:

VDDA0V9_PMU/VDDA_0V9/VDD_LOGIC→ VCCA1V8_PMU/VCC_1V8/VCC3V3_PMU/VDD_GPU → VDD_CPU → VCC_DDR → VCC_3V3 → RESETn

2.2.1.3 Power off Sequence

When the power supply voltage of the PMUIO1 power domain drops below 2.93V, RESETn must be pulled down first, and other power supplies will be powered off.

2.2.2 Power Design Recommendation

2.2.2.1 Standby Circuit Solution

RK3566 system uses the standby solution and the system consists of constant power supply area and power-off in standby area. The two parts are independently powered, as shown in the figure below:

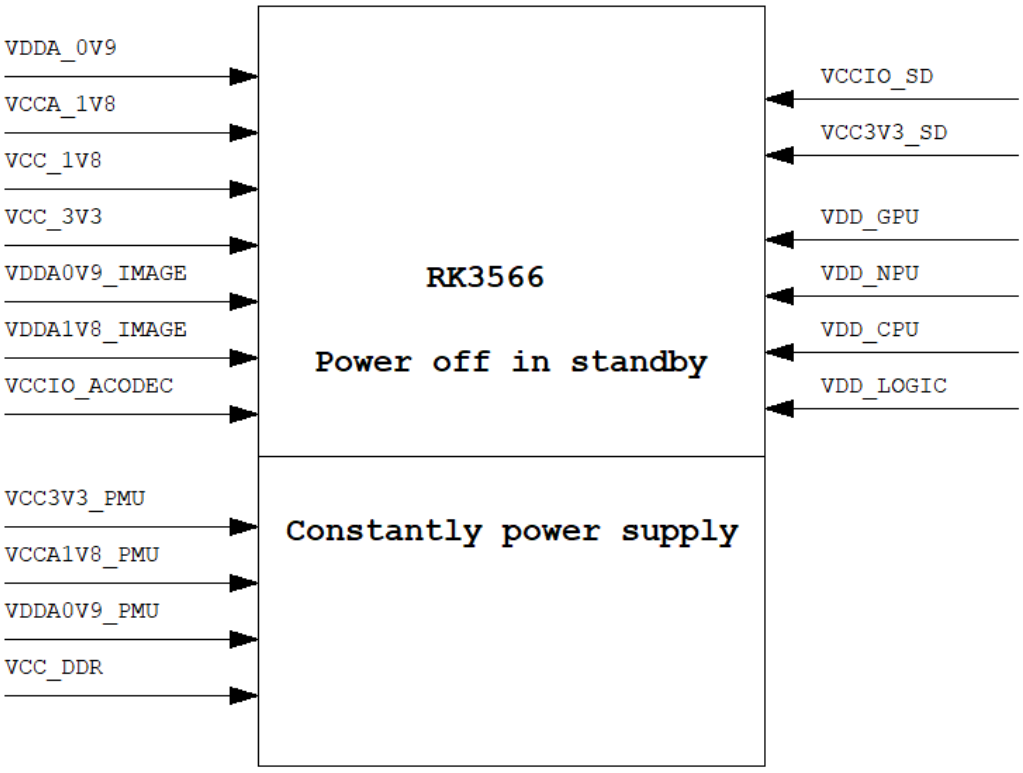


Figure 2-16 RK3566 Standby Circuit Solution

The standby power-down area power supply controls the PMIC to turn off each independent power supply in the standby state through the PMIC_SLEEP_H signal.

The power of the constant power supply area is directly provided by the power chip. In the standby state, at least four sets of power supplies should be kept power-up, as shown below:

- VCC_DDR: Power for DDR self-refresh.
- VDDA0V9_PMU: Provide power for Logic of PMUIO0 & PMUIO1 & PMUIO2 power domain. Provide power for PMUPLL and CPU OSC to work.
- VCCA1V8_PMU：Provide IO power for PMUIO1 & PMUIO2 power domain to maintain output status and interrupt response; Provide power for PMUPLL to work.
- VCC3V3_PMU：Provide IO power for PMUIO1 & PMUIO2 power domain to maintain output status and interrupt response.

The above standby solution can only support IO interrupt wake-up of PMUIO0, PMUIO1 and PMUIO2, and the IO of the other IO Domains will be invalid.

In standby, if you need to support USB HID device wake-up, the USB PHY power supply needs to be retained.

In standby, if you need to support IO interrupt wake-up in VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, VCCIO7, then the power supply of VDD_LOGIC and the corresponding IO Domain needs to be retained.

2.2.2.2 PLL Power

There are 9 PLLs in the RK3566, which are allocated as follows:

Table 2-10 RK3566 internal PLL Introduction

Classify	Quantity	Power	Standby State
PMU/OSC	2	PMUPLL_AVDD_0V9、 PMUPLL_AVDD_1V8	Can't turn off the power
Modules in the chip	7	SYSPLL_AVDD_0V9， SYSPLL_AVDD_1V8	Can turn off the power

Recommend to use LDO as a separate power supply for PLL, especially when DDR operating frequency is relatively high, the stable PLL power is helpful for improving the stability. The decoupling capacitor should be placed close to the pin. Please refer to the schematic for the specific number and capacity of capacitors, please do not change.

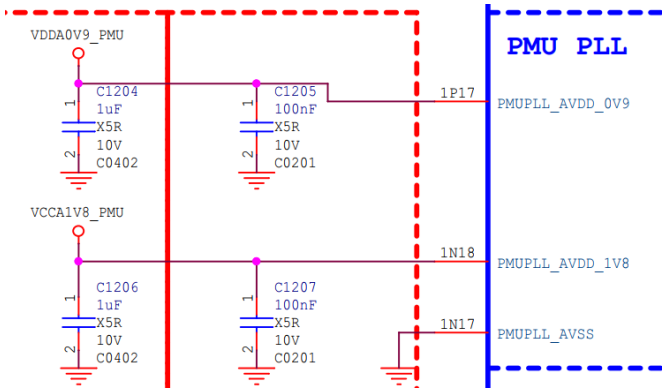


Figure 2-17 RK3566 PMU PLL power

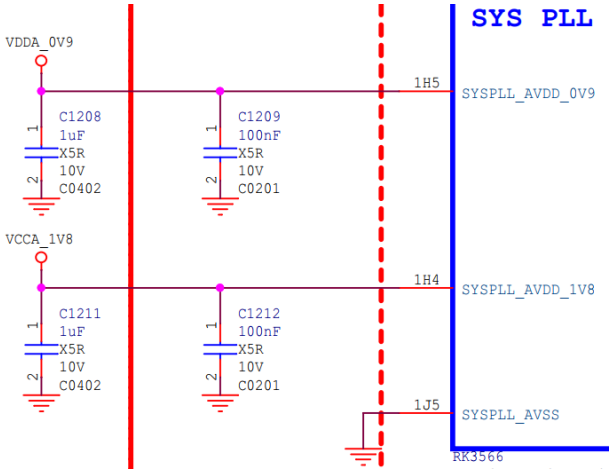


Figure 2-18 RK3566 SYS PLL power

2.2.2.3 CPU Power

RK3566 uses CPU independent power domain for power supply. As shown in the figure below, the VDD_CPU supplies power for the ARM Cortex-A55 core. The power supply uses an external DCDC power supply independently and supports dynamic frequency and voltage regulation. For related peak current, refer to *RK356X Power Consumption Test Report*. Do not delete the capacitor in the RK3566 reference design schematic.

For Layout, place the large capacitor on the back of RK3566 chip (please place it close to the chip for single layer SMT design) to ensure that the power ripple is less than 60mV and avoid system abnormalities caused by large power ripple under heavy load. The capacitor is shown in the figure below.

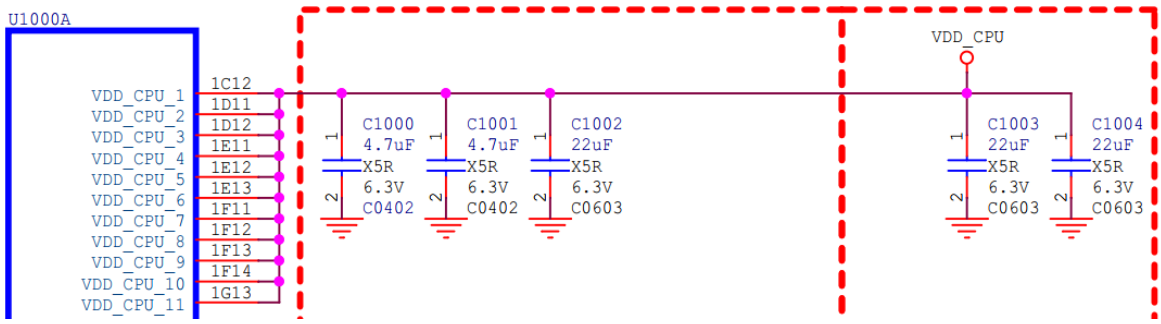


Figure 2-19 RK3566 VDD_CPU Power and Decoupling

On the Layout, power feedback is required. A separate feedback line from the bottom of the chip is connected to the FB terminal of the DC/DC power supply, which can effectively improve the voltage drop caused by PCB wiring and improve the timeliness of dynamic power adjustment. Detailed explain in the following subsections.

2.2.2.4 LOGIC Power

The LOGIC power of RK3566 uses PMIC to supply power and supports dynamic frequency and voltage regulation. Please refer to section 2.2.3 for the related peak current, please do not delete the capacitor in the RK3566 chip reference design schematic diagram.

For Layout, place the large capacitor on the back of RK3566 chip (please place it close to the chip for single layer SMT design) to ensure that the power ripple is less than 60mV and avoid system abnormalities caused by large

power ripple under heavy load. The capacitor is shown in the figure below.

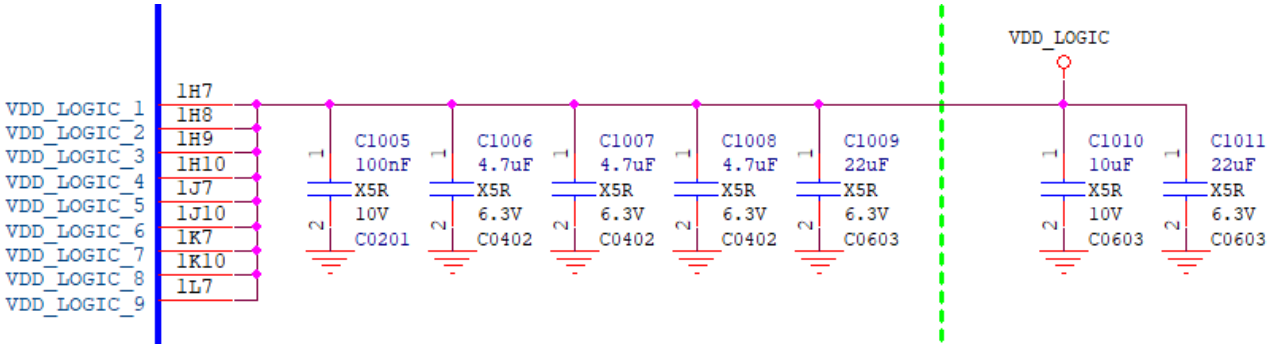


Figure 2-20 RK3566 LOGIC Power and Decoupling

Similarly, power feedback is required.

2.2.2.5 GPU & NPU Power

The GPU and NPU power of RK3566 uses PMIC to supply power and supports dynamic frequency and voltage regulation. Please refer to section 2.2.3 for the related peak current, please do not delete the capacitor in the RK3566 chip reference design schematic.

In the RK809-5 solution, the two power supplies are independent. NPU power supply can be turned on after startup.

In the RK817-5 solution, for cost considerations, the GPU and NPU power supply are combined. See the reference schematic for details.

For Layout, place the large capacitor on the back of RK3566 chip (please place it close to the chip for single layer SMT design) to ensure that the power ripple is less than 60mV and avoid system abnormalities caused by large power ripple under heavy load. The capacitor is shown in the figure below.

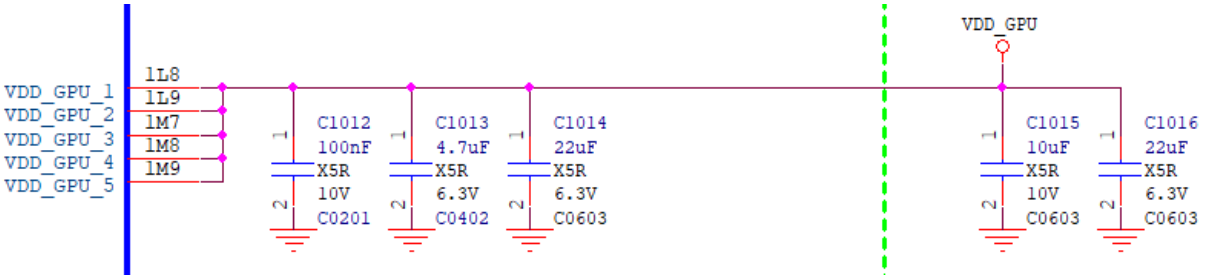


Figure 2-21 RK3566 VDD_GPU power and decoupling

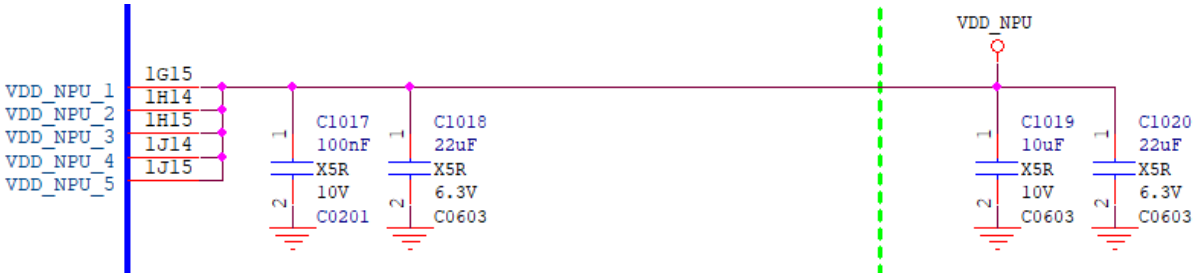


Figure 2-22 RK3566 VDD_NPU power and decoupling

Similarly, power feedback is required.

2.2.2.6 Remote Feedback Compensation of Power

The above mentioned VDD_CPU/VDD_LOGIC/VDD_GPU/VDD_NPU power supply DC-DC adopts remote feedback compensation design to compensate the voltage loss of the circuit and improve the timeliness of dynamic power supply adjustment. As shown in the figure:

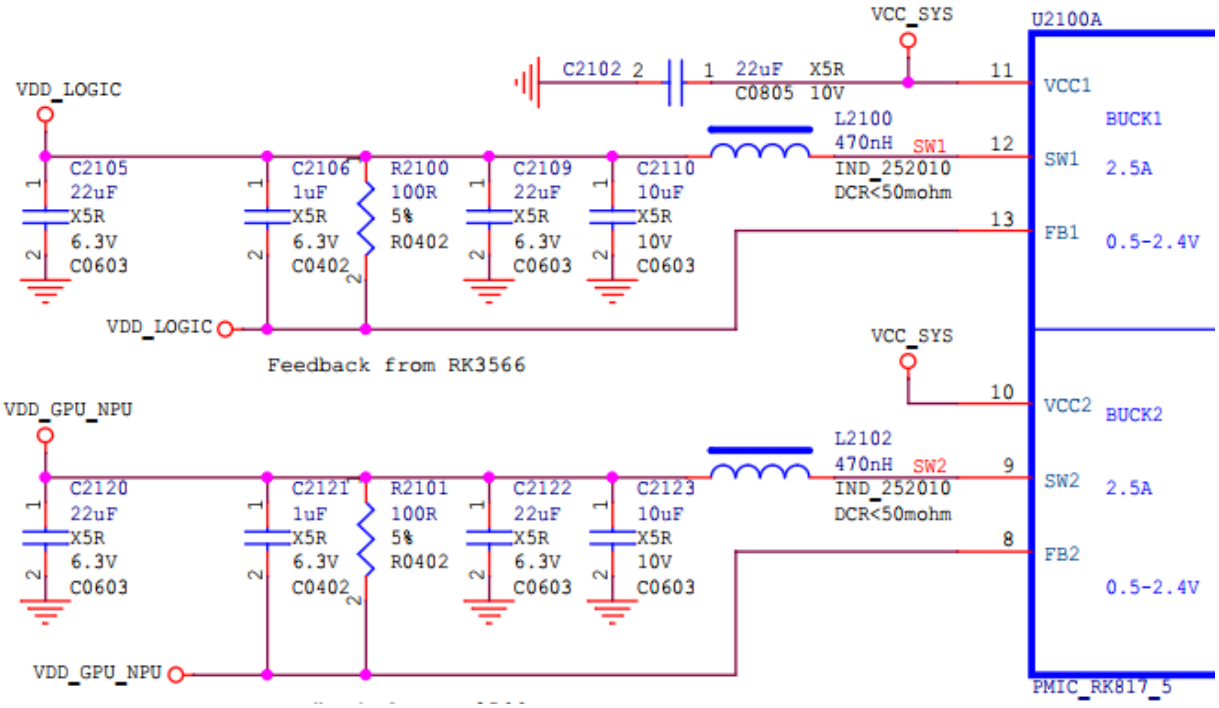


Figure 2-23 RK3566 power's remote feedback compensation

In order to avoid an open circuit of the remote feedback node during actual production or use, it is required to add a 100ohm resistor on the DC-DC side. This resistor can keep the output voltage stable even when the feedback node is open, and avoid abnormal output caused by the open circuit of the feedback node.

In addition, in some designs, the loop between the feedback compensation circuit and the power circuit may induce noise to affect DC-DC, and this resistance can reduce this effect. At the same time, in order to improve the transient response, a 1uF capacitor is connected in parallel near the 100ohm resistor. Attention, the 100ohm resistor and 1uF capacitor cannot be deleted at will.

2.2.2.7 DDR Power

The DDR controller interface of the RK3566 supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X level standards. When designing the product, please configure it according to the SDRAM chip usage and confirm it meets the design requirements.

The power supply difference between LPDDR4 and LPDDR4X is described in DDR section. You need to select the power supply on the corresponding DDR schematic diagram page. Select VCC_DDR for power supply when LPDDR4 are used, and VCC0V6_DDR for LPDDR4X.

In the case of using PMIC, the voltage of VCC_DDR is determined by the voltage divider resistance value to ensure the accuracy of the output voltage. The relevant divider voltage value can refer to the figure below:

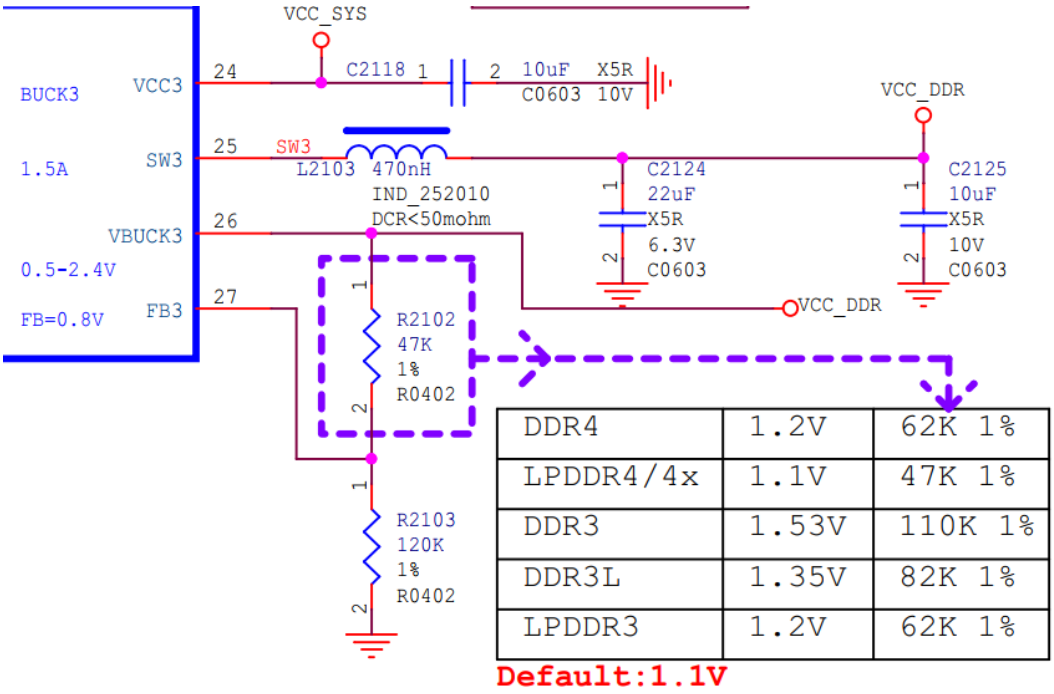


Figure 2-24 RK3566 VCC_DDR power

Similarly, please do not delete the capacitor in the RK3566 chip reference design schematic. For layout, place the large capacitor on the back of RK3566 chip (please place it close to the chip for single layer SMT design) to ensure that the power ripple is less than 60mV and avoid system abnormalities caused by large power ripple under heavy load. The capacitor is shown in the figure below.

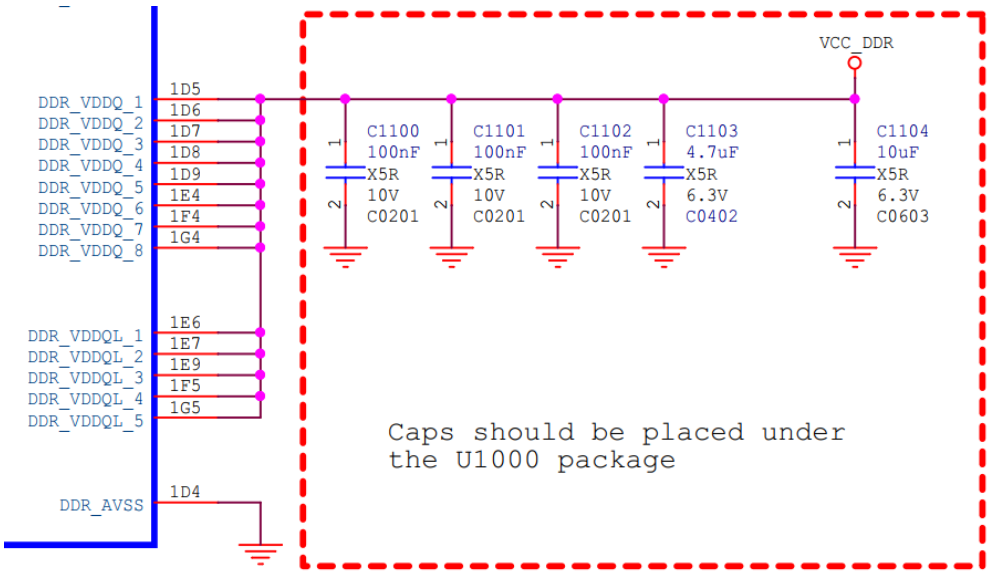


Figure 2-25 RK3566 DDR power and decoupling in DDR3/DDR3L/DDR4/LPDDR3/LPDDR4

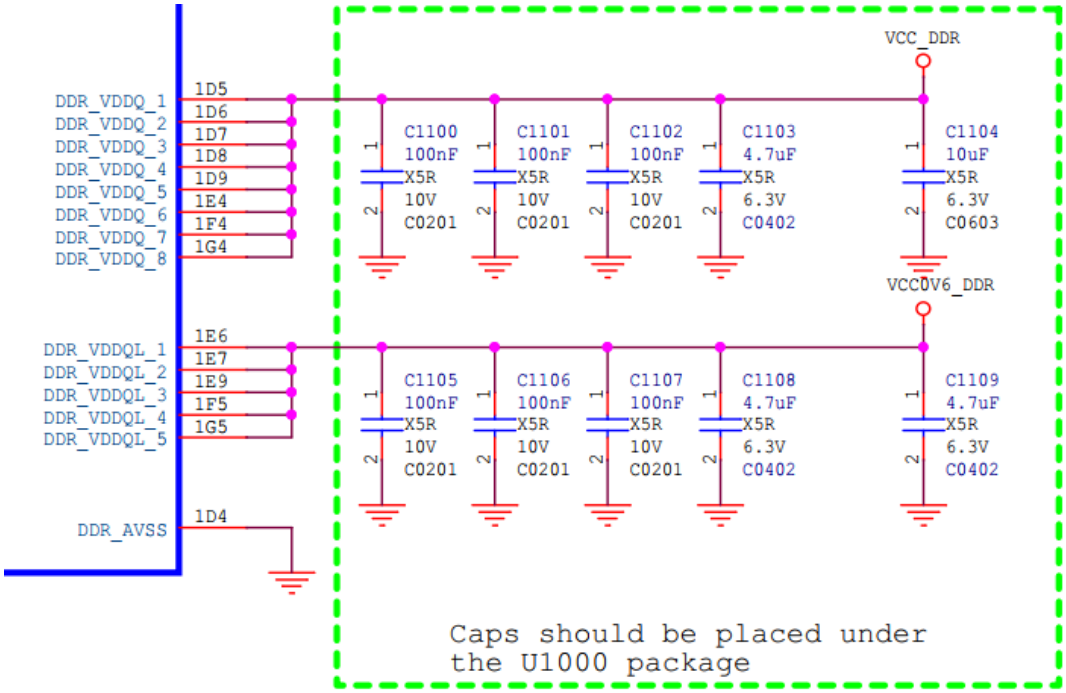


Figure 2-26 RK3566 DDR power and decoupling in LPDDR4X

2.2.2.8 VDDA_0V9/VDDA0V9_IMAGE Power Design

For the power supply of VDDA_0V9/VDDA0V9_IMAGE, there are two circuits provided for customers according to the power quality and power consumption in the supporting design of RK817-5, which can be selected according to the actual situation:

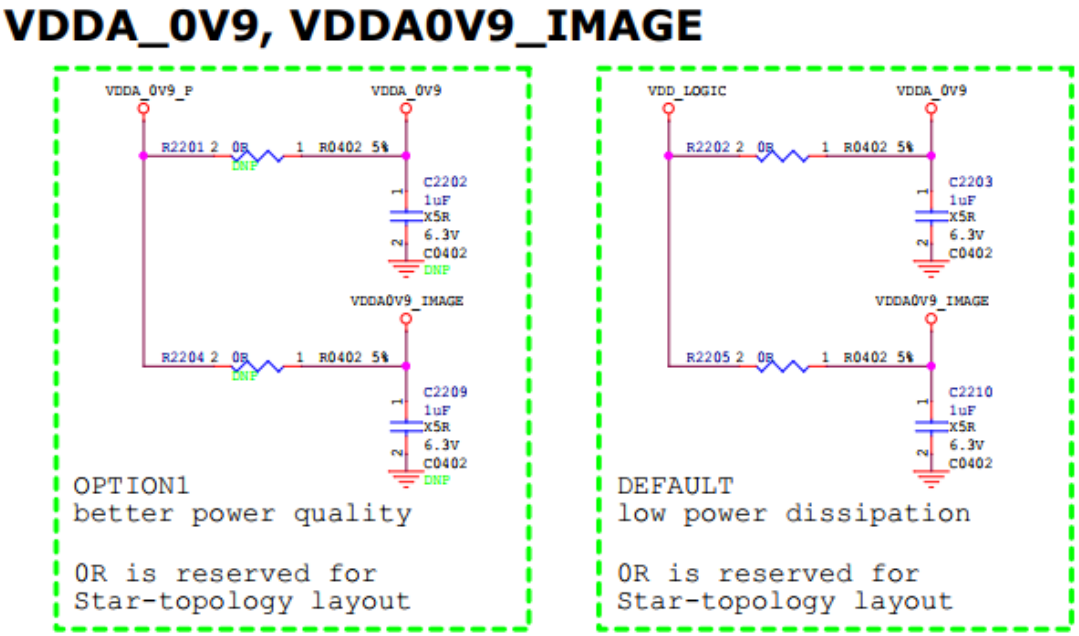


Figure 2-27 RK3566 0.9V related power supply design

2.2.2.9 VCC_1V8/VCCA_1V8/VCCA1V8_IMAGE Power Design

For the power supply of VCC_1V8/VCCA_1V8/VCCA1V8_IMAGE, there are two circuits provided for customers according to the cost and power consumption in the supporting design of RK817-5, which can be selected according to the actual situation:

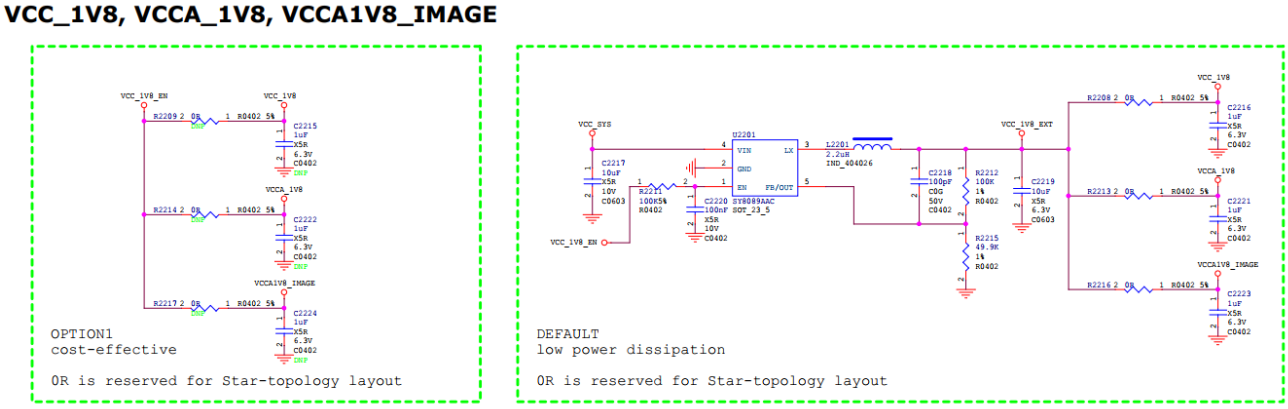


Figure 2-28 RK3566 7.8V related power supply design

2.2.2.10 GPIO Power

GPIO power supply refer to section 2.1.10. It is recommended to place a 100nF decoupling capacitor close each power supply pin. For detailed design, please refer to RK3566 chip reference design schematic.

2.2.2.11 Power Supply for Each Function Module

The power supply of each functional module part is designed according to the reference schematic. For detailed description, please refer to the corresponding module chapter of this article.

When some modules are not powered on, the kernel initialization may be stuck. Therefore, it needs software to disable the corresponding controller node in the DTS.

2.2.3 Power peak Ammeter

The *RK356X Power Consumption Test Report* document is provided in the release package for reference. Please pay attention to the limitation and description of the relevant test conditions.

2.2.4 RK817-5 Scheme Introduction

2.2.4.1 RK817-5 Block Diagram

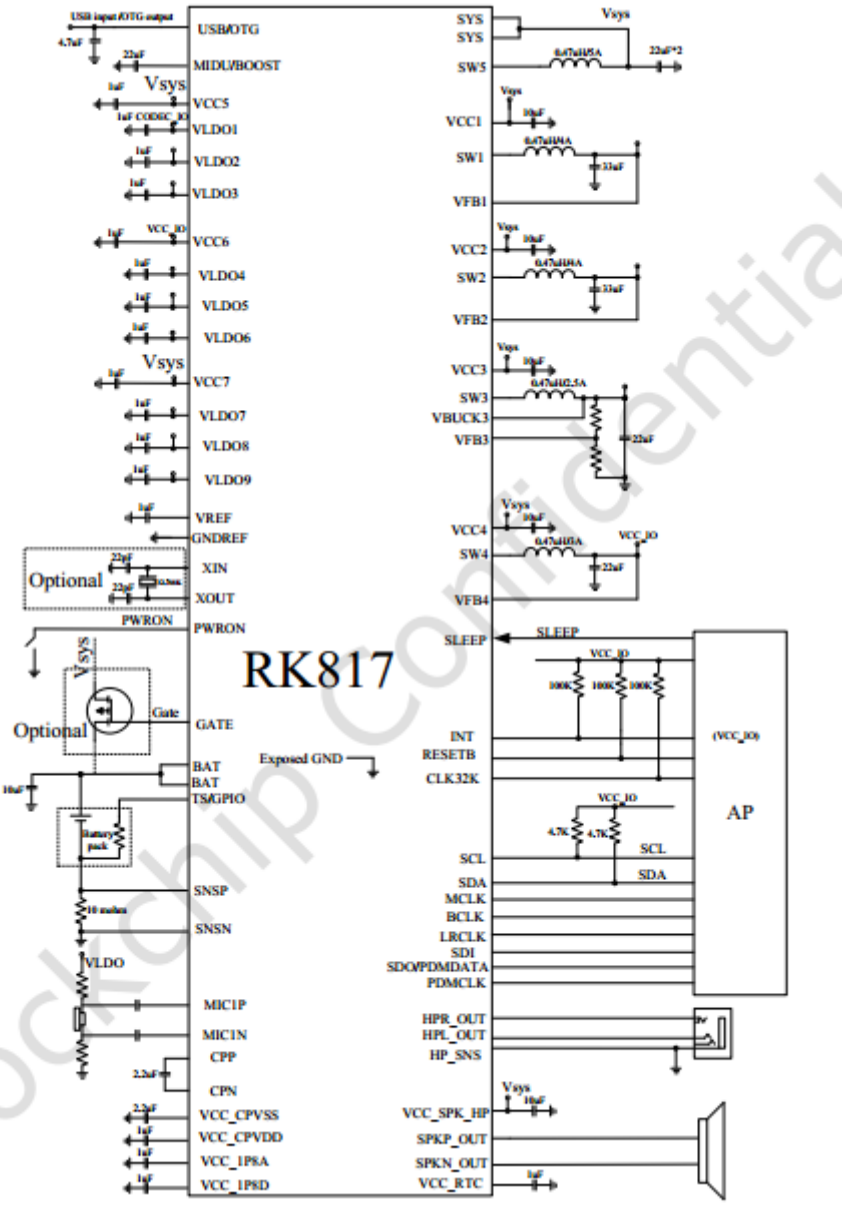


Figure 2-29 RK817-5 block diagram

2.2.4.2 RK817-5 Characteristic

- Input range: USB input is 3.8V-5.5V; BAT input is 2.7V-5.5V
- Li-ion battery switching charger with a maximum charging current of 3.5A
- Maximum 4A automatic power path management
- Built-in accurate voltameter
- Built-in real-time clock (RTC)
- Very low standby current of 16uA (under 32KHz clock frequency)
- True-ground headphone amp driver

- 1.3W filter free Class D power amplifier (drive 8ohm speaker)
- Fixed and programmable selectable power start sequence control
- Built-in high-performance audio codec
  - Built-in independent PLL
  - Support microphone input
  - Both DAC and ADC support I2S digital interface
  - Support ALC, limiter and noise gate
  - Support programmable digital and analog gain
  - Support 16bits-32bits bit rate
  - Sampling rate up to 192kHz
  - The software supports two working mode configurations: master and slave
  - Support 3 kinds of I2S formats (standard, left-justified, right-justified)
  - Support PDM mode (external input PCLK)
- Power Channel:
  - BUCK1: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK2: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK3: Synchronous step-down DC-DC converter, 1.5A max
  - BUCK4: Synchronous step-down DC-DC converter, 1.5A max
  - BOOST: Synchronous step-up DC-DC converter, 1.5A max (cannot be used with charging function at the same time)
  - LDO1-LDO2, LDO4-LDO9: low dropout linear regulator, 400mA max
  - LDO3: Low-noise, high-power rejection ratio low-dropout linear regulator, 100mA max
  - OTG: OTG switch, 1.5A max (cannot be used with charging function at the same time)
- Package: 7mmx7mm QFN68

2.2.4.3 RK3566+RK817-5 Typical Application Power Tree

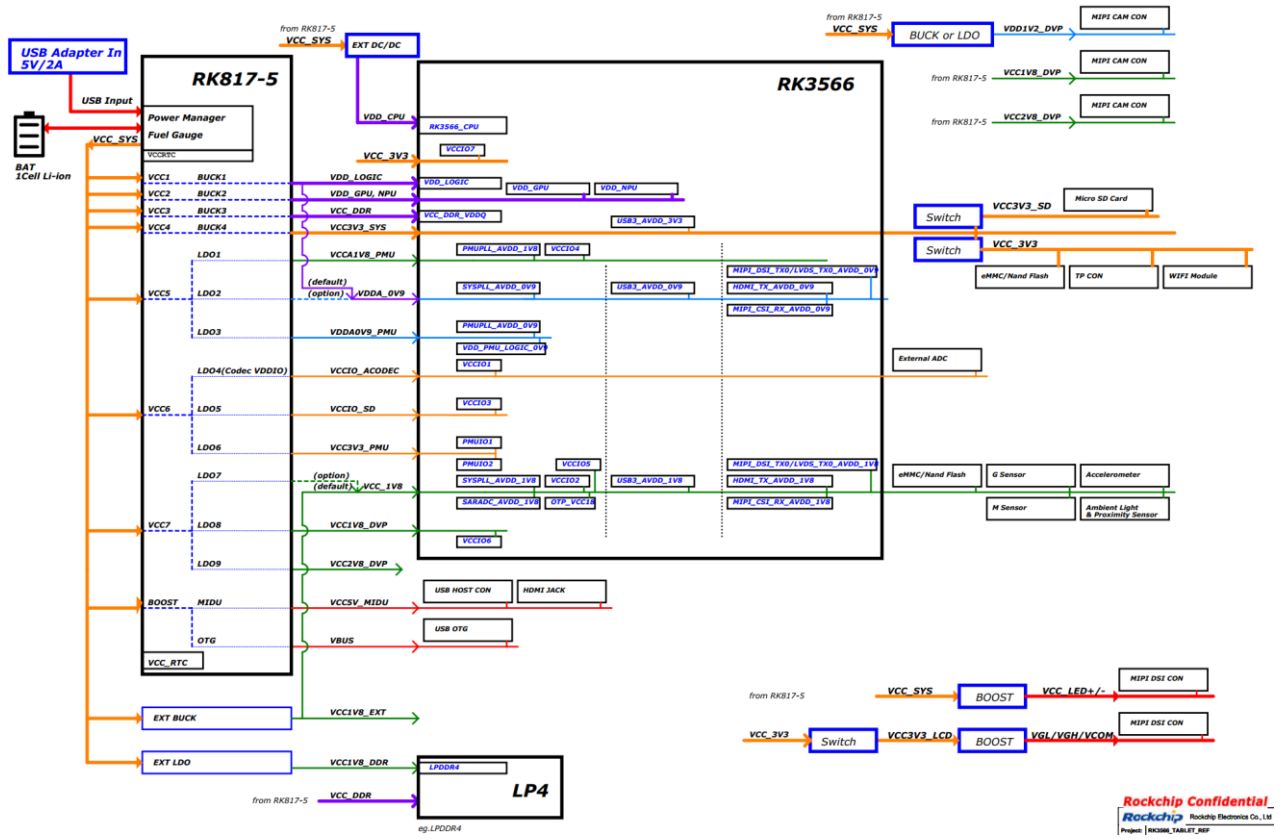


Figure 2-30 RK3566+RK817-5 Typical application power tree

2.2.4.4 Tips for RK817-5

The recommended value for the matching capacitance of the 32.768 crystal is 22pF, which can be fine-tuned according to the specific specifications of the crystal used.

NOTE

In order to lower power consumption, the drive strength of PMIC RTC oscillator is low. The oscillation signal can not be measured with an ordinary oscilloscope on the XOUT or XIN pin, or it will stop vibration when the oscilloscope probe touches it. It can measure the CLK32K pin to replace the test of XOUT/XIN.

The output capacitance of BUCK1 and BUCK2 must be greater than 30uF to ensure a better decoupling effect. Especially, in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased;

RK817-5 comes with USB OTG power supply function, short circuit protection function, and can be configured with 1.0-1.5A output current limit.

The switch logic controlled by the buttons is as follows: PWRON pin has a built-in pull-up resistor, which is pulled up to VCCRTC. When the low level time is detected for more than 500ms, it will power on; after power on, if

the PWRON pin is pulled down for more than 6s, it will be forced to power off (Usually used for forced shutdown and restart of the system after a system crash); during sleep and wake-up operations, the low level of the PWRON pin needs to be maintained for more than 20ms.

Basic conditions for RK817-5 to work:

- VBAT is greater than 3.3V or VUSB is greater than 4.4V;
- Detecting one of the following three conditions, RK817-5 automatically turns on: PWRON pin is low and maintains 500ms; USB is inserted; internal RTC Alarm is turned on and the time is up.
- Start the power-on process, each time sequence interval is 2ms, the next power will up utill the previous one is power ok. When all power supplies are ready, then release RESET, and the power-on process complete;

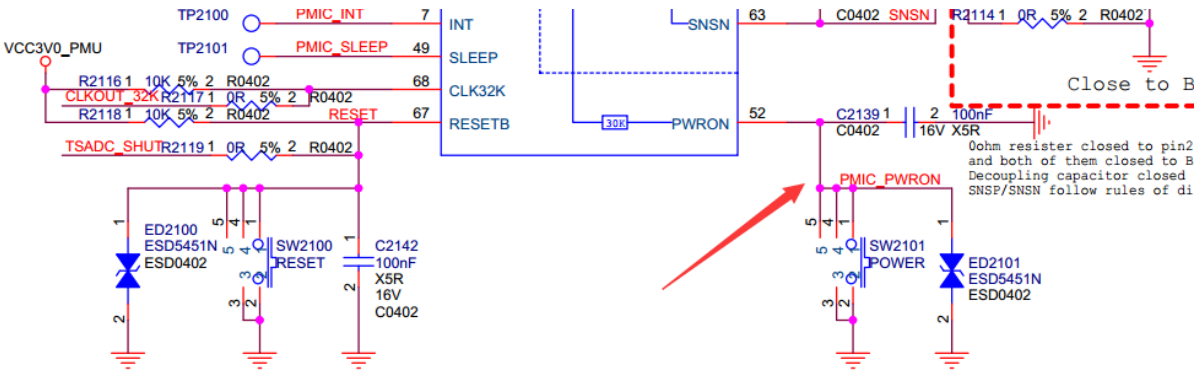


Figure 2-31 RK817-5 PWRON pin

RK817-5 will automatically shut down when it detects one of the following conditions:

- I2C write DEVICE_OFF=1;
- PWRON pin pull low over 6s;

After RK817-5 starts the power-off process, it pulls down the reset after one RTC clock cycle (about 30.5us later), and then turns off all the power outputs 2ms later, and finally complete the power-off process.

When a single-cell lithium battery is discharge at high current, the battery voltage will collapse due to excessive instantaneous current. The PMIC will enter the shutdown process after voltameter detects that the battery voltage is lower than the shutdown voltage threshold, resulting in the remaining battery capacity cannot be used, and shorting the product's battery life. In this case, it is necessary to minimize the internal resistance of the power supply loop and the battery. The internal resistance of the power circuit is shown by the red arrow in the figure below. Try to use short and thick traces or copper connections when routing the PCB. When the trace is changed layer, you need to drill more vias. And the internal resistance of the battery needs to be low. And use a lower on-resistance protection board and power cable to reduce the battery internal resistance.

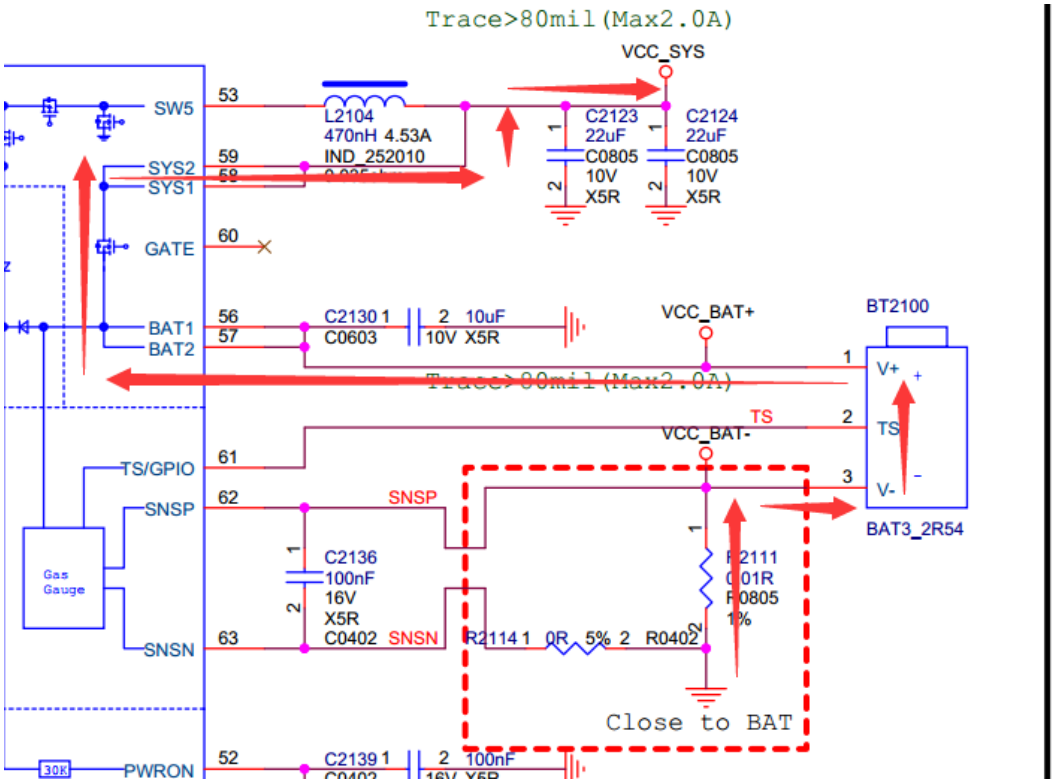


Figure 2-32 Rk817-5 Battery discharge path

2.2.4.5 RK817-5 Design Description

For details design instructions of RK817-5, please refer to the RK PMIC related design document *RK817 Application Guide*.

2.2.5 RK809-5 Scheme Introduction

2.2.5.1 RK809-5 Block Diagram

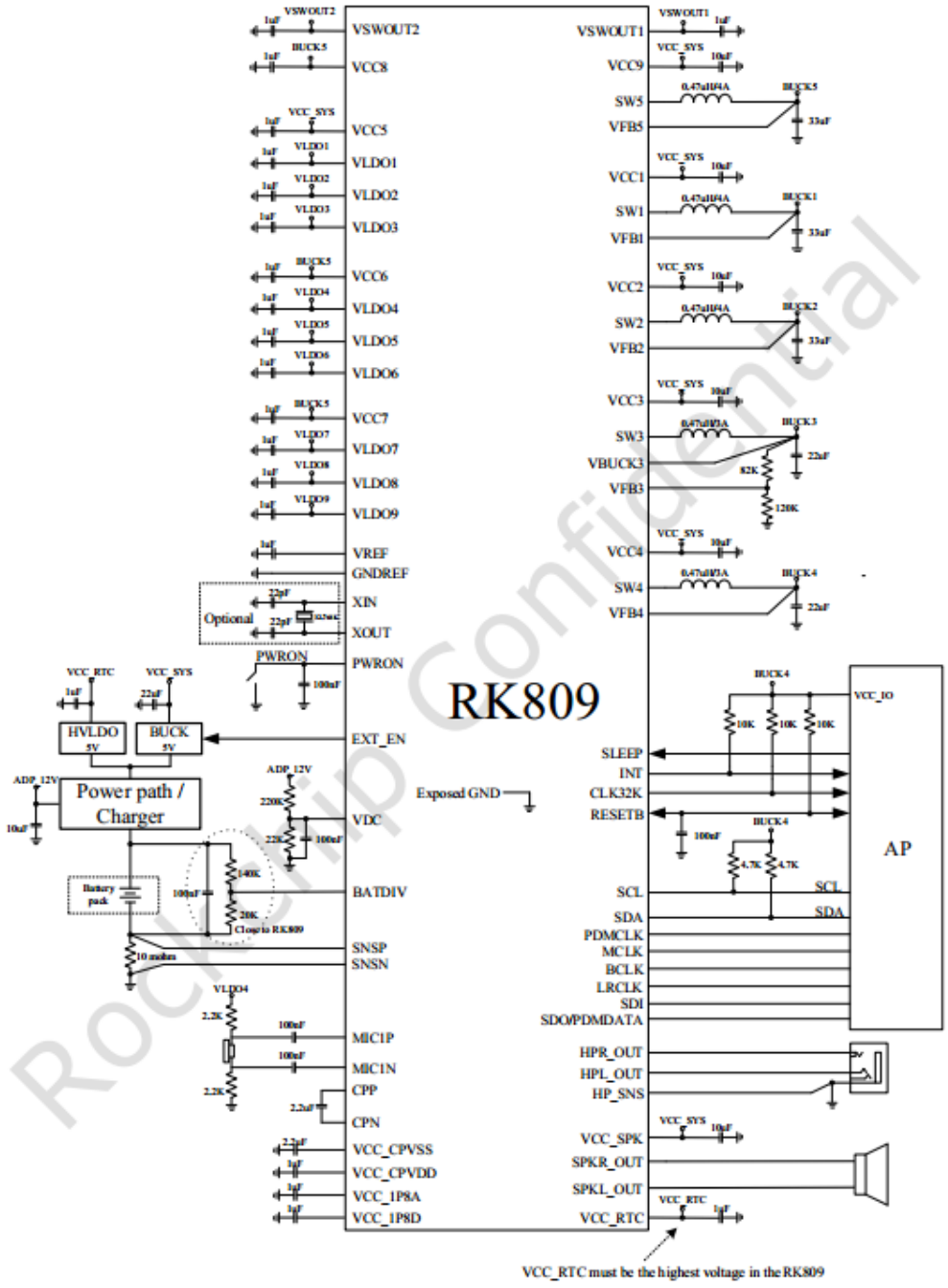


Figure 2-33 RK809-5 block diagram

2.2.5.2 RK809-5 Characteristic

- Power input range: 2.7V-5.5V
- Accurate voltameter with two ADCs of separate battery voltage and current
- Built-in real-time clock (RTC)
- Very low standby current of 16uA (under 32KHz clock frequency)
- True-ground headphone driver

- 1.3W filter free Class D power amplifier (drive 8ohm speaker)
- Fixed and programmable selectable power start sequence control
- Built-in high-performance audio codec
  - Built-in independent PLL
  - Support microphone input
  - Both DAC and ADC support I2S digital interface
  - Support ALC, limiter and noise gate
  - Support programmable digital and analog gain
  - Support 16bits-32bits bit rate
  - Sampling rate up to 192kHz
  - The software supports two working mode configurations of master and slave
  - Support 3 kinds of I2S formats (standard, left-justified, right-justified)
  - Support PDM mode (external input PCLK)
- Power Channel:
  - BUCK1: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK2: Synchronous step-down DC-DC converter, 2.5A max
  - BUCK3: Synchronous step-down DC-DC converter, 1.5A max
  - BUCK4: Synchronous step-down DC-DC converter, 1.5A max
  - BUCK5: Synchronous step-down DC-DC converter, 2.5A max
  - LDO1-LDO2, LDO4-LDO9: low dropout linear regulator, 400mA max
  - LDO3: Low-noise, high-power rejection ratio low-dropout linear regulator, 100mA max
  - Switch1: switch, 2.1A max, Rdson = 90mOhm
  - Switch2: switch, 2.1A max, Rdson = 100mOhm
- Package: 7mmx7mm QFN68

2.2.5.3 RK3566+RK809-5 Typical Application Power Tree

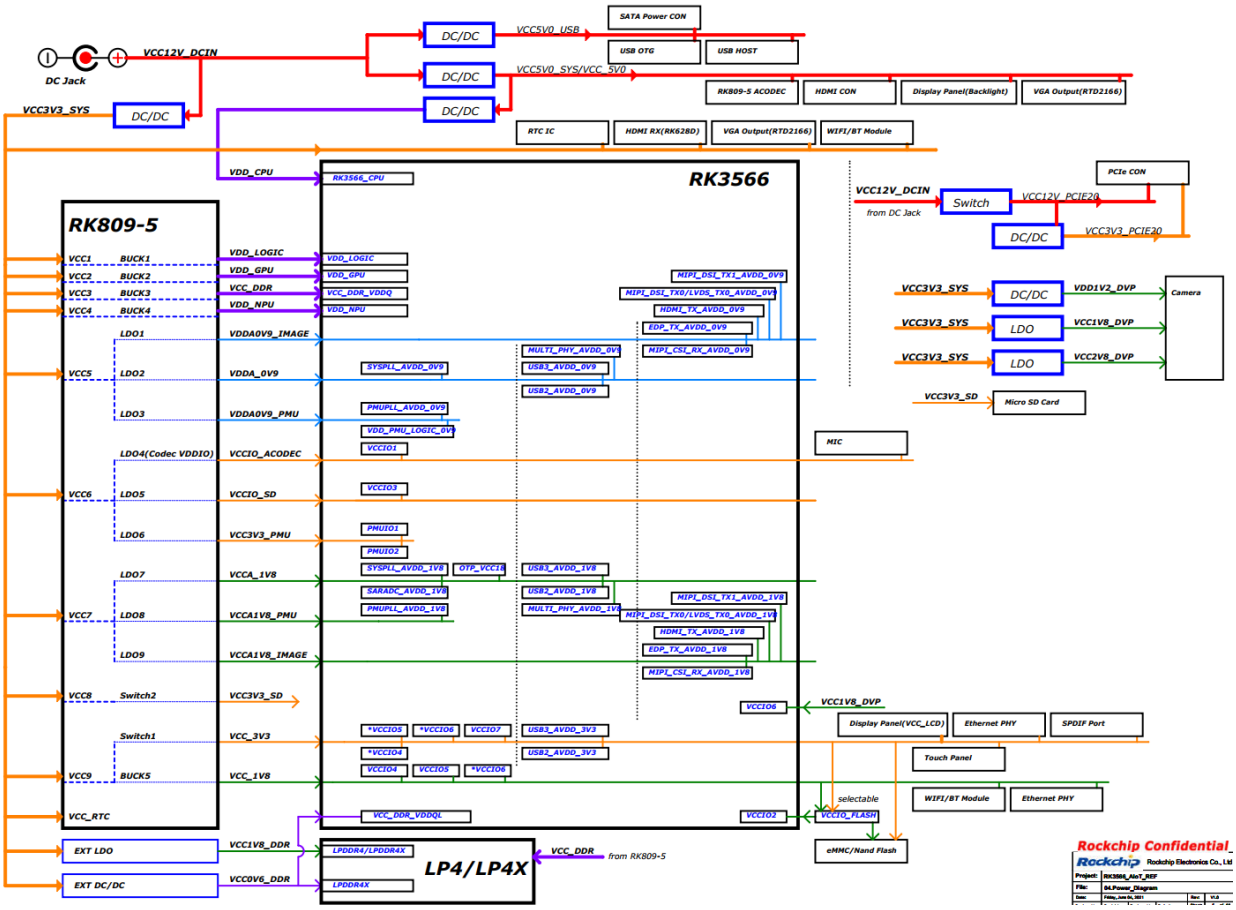


Figure 2-34 RK3566+RK809-5 Typical application power tree

2.2.5.4 Rk809-5 Precautions

The recommended value for the matching capacitance of the 32.768 crystal is 22pF, which can be fine-tuned according to the specific specifications of the crystal used.

NOTE

In order to lower power consumption, the drive strength of PMIC RTC oscillator is low. The oscillation signal can not be measured with an ordinary oscilloscope on the XOUT or XIN pin, or it will stop vibration when the oscilloscope probe touches it. It can measure the CLK32K pin to replace the test of XOUT/XIN.

VCC_RTC must be the first powered, and its voltage value must be the highest input power supply to RK809-5 (except for VCC_SPK_HP). It is recommended be connected to the same power supply with VCC9.

The output capacitance of BUCK1 and BUCK2 must be greater than 30uF to ensure a better decoupling effect. Especially, in the case of high current and high dynamic load, the output decoupling capacitor can be appropriately increased.

The boot logic directly controlled by the input power supply is as follows: when there is power input, the primary

DCDC step-down output VCC5V0_SYS and VCC_RTC, the VDC (generated by a voltage divider circuit from external power supply) is greater than 0.55V, then the PMIC starts to work and output power.

The switch logic controlled by the buttons is as follows: PWRON pin has a built-in pull-up resistor, which is pulled up to VCCRTC. When the low level time is detected for more than 500ms, it will power on; after power on, if the PWRON pin is pulled down for more than 6s, it will be forced to power off (Usually used for forced shutdown and restart of the system after a system crash); during sleep and wake-up operations, the low level of the PWRON pin needs to be maintained for more than 20ms.

Basic conditions for RK 809-5 to work

- VCC_RTC power supply;
- VCC5V50_SYS power supply
- Detecting one of the following three conditions, RK809-5 automatically turns on: PWRON pin is low and maintains 500mS; the VDC level exceeds 0.55V; internal RTC Alarm is turned on and the time is up.
- Start the power-on process, each time sequence interval is 2ms, the next power will up utill the previous one is power ok. When all power supplies are ready, then release RESET, and the power-on process complete;

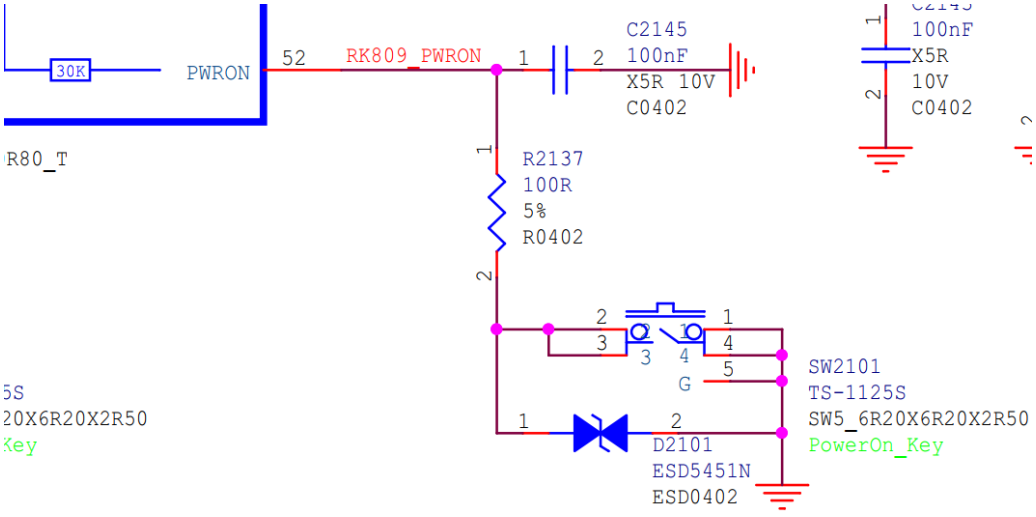


Figure 2-35 RK809-5 PWRON pin

RK809-5 will automatically shut down when it detects one of the following conditions:

- I2C write DEVICE_OFF=1;
- PWRON pin pull low over 6s;

After RK809-5 starts the power-off process, it pulls down the reset after one RTC clock cycle (about 30.5us later), and then turns off all the power outputs 2ms later, and finally complete the power-off process.

2.2.5.5 RK809-5 Design Description

For details design instructions of RK809-5, please refer to the RK PMIC related design document *RK809 Application Guide*.

2.2.6 Over Temperature Protection Circuit

When RK3566 occurs over-temperature or crash, the TSADC_SHUT pin of the chip will output low level to reset RK817-5 or RK809-5, trigger power off and restart, and reset the whole system with the registers cleared.

TSADC_SHUT is a specific function signal, please do not change the usage.

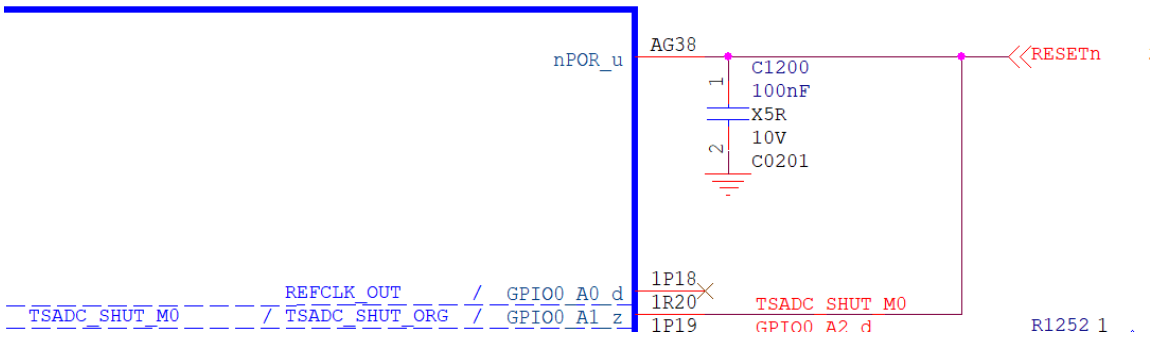


Figure 2-36 RK3566 TSADC_SHUT Over-temperature protection output

2.2.7 PMIC SLEEP Standby Control Circuit

When RK3566 is in work mode, the status pin PMIC_SLEEP of the chip will keep low level.

When the system enters standby mode, the PMIC_SLEEP pin will output sleep indicating signal with high level, and then PMIC will enter sleep status controlled by the signal. According to the configuration of software dts file, some power supply will turn off, and some power supply will lower down the voltage.

When the system is resumed from standby mode, the PMIC_SLEEP pin will output low level at the first time, and the PMIC and all the power supply will recover to normal work state.

PMIC_SLEEP is a specific function signal, please do not change the usage.

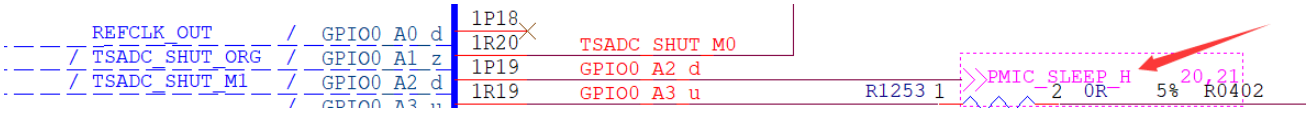


Figure 2-37 RK3566 PMIC_SLEEP output

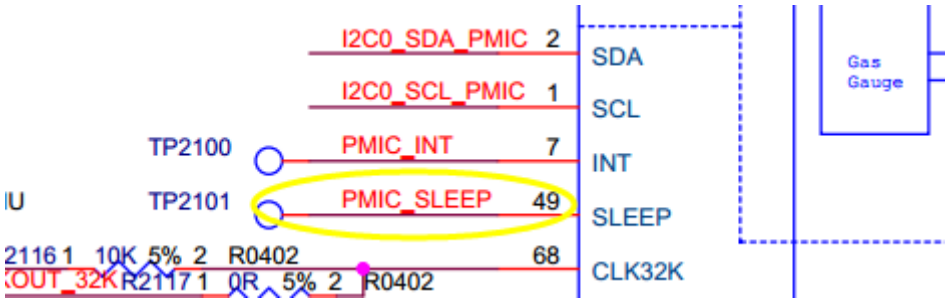


Figure 2-38 RK3566 PMIC_SLEEP input

2.3 Function Interface Circuit Design

2.3.1 SDMMC Memory Card Circuit

RK3566 integrates three SDMMC interface controllers, all of which can support SD V3.01 and MMC V4.51 protocols. SDMMC0 is shown in the figure:

- SDMMC0 controller has an independent power domain;
- SDMMC0 is multiplexed with JTAG and other functions, and functions are selected through SDMMC0_DET. For details, refer to the description in the JTAG section;
- VCCIO3 is the IO power supply, which requires an external 3.3V power supply (SD V2.0 mode) or 3.3V/1.8V adjustable power supply (SD V3.0 mode);
- SDMMC0_DATA, SDMMC0_CMD, SDMMC0_CLK need to be connected in series with 22ohm resistor, and SDMMC0_DET need to be connected in series with 100ohm resistor;
- When the signal is close to the SD card slot, an ESD device should be placed. In order to reduce the impact on the signal, it is recommended to choose a junction capacitance of less than 1pF (if only SD2.0 mode is required, the junction capacitance of the ESD device can be relaxed to less than 9pF);
- The decoupling capacitor for SD card power supply should be placed close to the card slot.

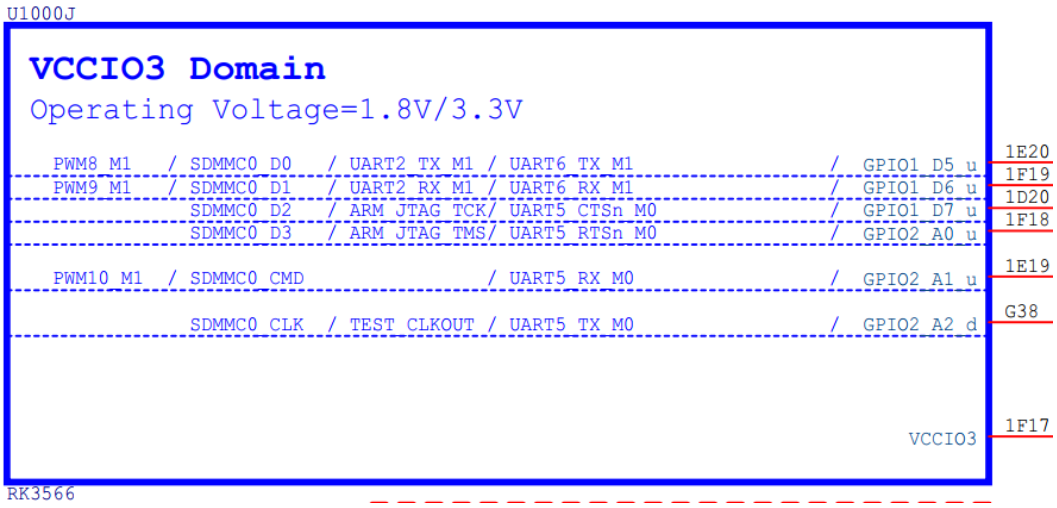


Figure 2-39 RK3566 SDMMC0 module

The pull-up/down and matching design of the SDMMC interface are recommended as shown in the table below.

Table 2-11 RK3566 SDMMC Interface Design

Signal	Internal pull up/down	Connection method (SDR104 high-speed mode)	Description(chip side)
SDMMC0_DQ[3:0]	Pull up	Series connect 22ohm resistor	SD data output/input
SDMMC0_CLK	Pull down	Series connect 22ohm resistor Place near the RK3566 end	SD clock output
SDMMC0_CMD	Pull up	Series connect 22ohm resistor	SD command output/input
SDMMC0_DET	Pull up	Series connect 100ohm resistor	SD card insertion detection

When you need to use an SD card for system memory, it is recommended to use SDMMC0 (if you need to use SDMMC1 or SDMMC2 for system memory, you need to consider the relevant power supply). The DET pin of SDMMC0 is located in the PMUIO power domain and can support card hot-plug wake-up.

The other two controllers SDMMC1 and SDMMC2 can also be used for SD card connection, but these two interfaces are more often used as SDIO interfaces to connect to WIFI, or their corresponding GPIOs are occupied by other multiplexed functions and cannot be used as SDMMC function.

The following is an explanation for WIFI connection, where SDMMC1 is used as SDIO and connected to the WIFI module, the corresponding VCCIO4 power domain is consistent with WIFI IO, and powered with VCCIO_WL. When SDIO3.0 is supported, VCCIO_WL is required to be 1.8V; when SDIO2.0 is supported, VCCIO_WL is 3.3V.

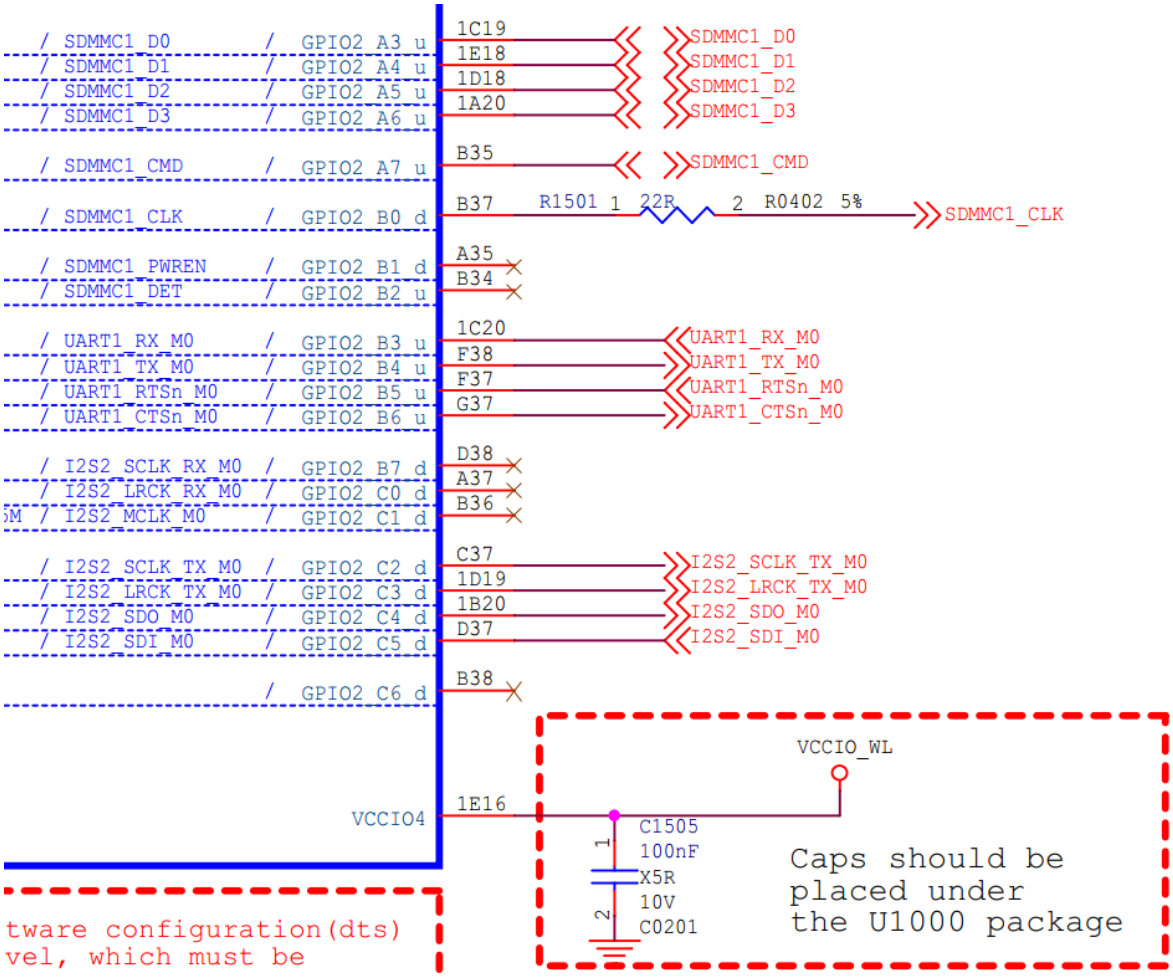


Figure 2-40 RK3566 WIFI/BT connection diagram

For low-power design considerations (if there is no special requirement for power consumption, you are free from this restriction by modifying the software), RK3566 will turn off the LOGIC power supply by default in the secondary standby state. At this time, only PMUIO logic remains powered, and the corresponding GPIO can be controlled. Therefore, if you need to support the WIFI/BT sleep wake-up function in this case, the corresponding WIFI/BT control signal should be connected to the GPIO of the PMUIO power domain. As shown in the figure below:

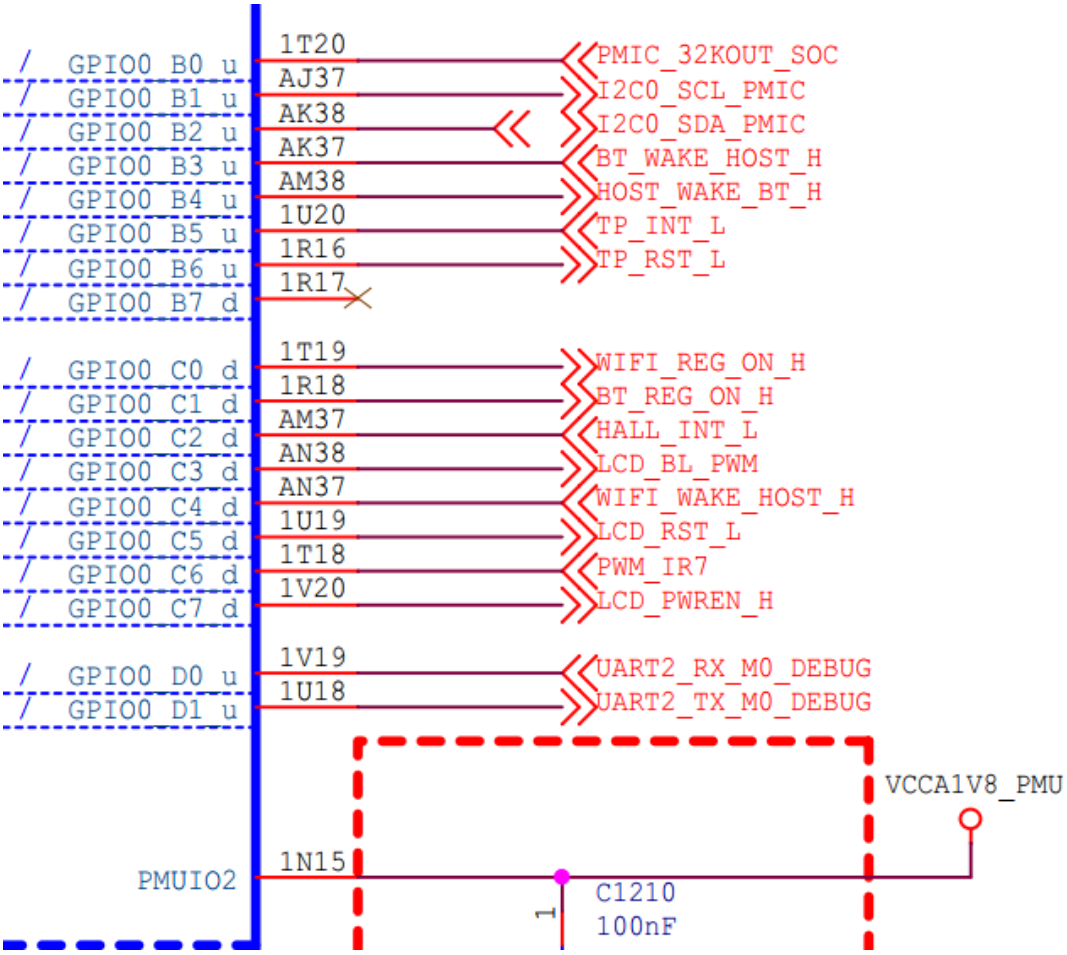


Figure 2-41 RK3566 WIFI/BT control signal connection diagram

The SDIO interface pull up/down and matching design recommendations are as follows:

Table 2-12 RK3566 SDIO interface design

Signal	Internal pull up/down	Connection method (SDR104 high-speed mode)	Description(chip side)
SDIO_DQ[3:0]	Pull up	direct connection	SDIO data send/receive
SDIO_CLK	Pull down	Series connect 22ohm resistor	SDIO clock output
SDIO_CMD	Pull up	direct connection	SDIO command send/receive

Design attention:

- The serial resistor of the SDIO CLK must be close to the RK3566; the wiring must be guarded with ground path and ground vias, and the interval between ground vias shall not be greater than 300mil;
- The length of all SDIO signal traces must be less than 4 inches, and the delay between SDIO CLK and DATA/CMD must be controlled within 120 mils;
- The reference layer of all SDIO signals needs to be a complete ground plane to avoid continuous vias blocking the signal return path;
- All SDIO signals must control the PCB impedance, and the single-ended signal impedance is 50ohm±10%;

2.3.2 USB Circuit

The RK3566 chip has one USB2.0 OTG ports, three USB2.0 HOST ports, and one USB3.0 HOST ports (one USB2.0 hosts will be occupied when the full USB3.0 HOST is used).

NOTE

1, The USB OTG port is the system firmware burning port by default, and must be reserved for debugging and production process.

2, When the USB 2.0 controller and the USB 3.0 controller are used together, the collocation principle of USB2.0 PHY1 and USB 3.0 PHY1 should be followed.

2.3.2.1 USB2.0 Introduction

The USB2.0 OTG and USB3.0 HOST1 interface are shown in the figure below. The USB_OTG0_ID pin has a internal pull-up resistor (about 200KOhm) to USB_AVDD_1V8, so the OTG interface is in Device mode by default. When an OTG device is inserted, this pin will be pulled low to enter the HOST mode.

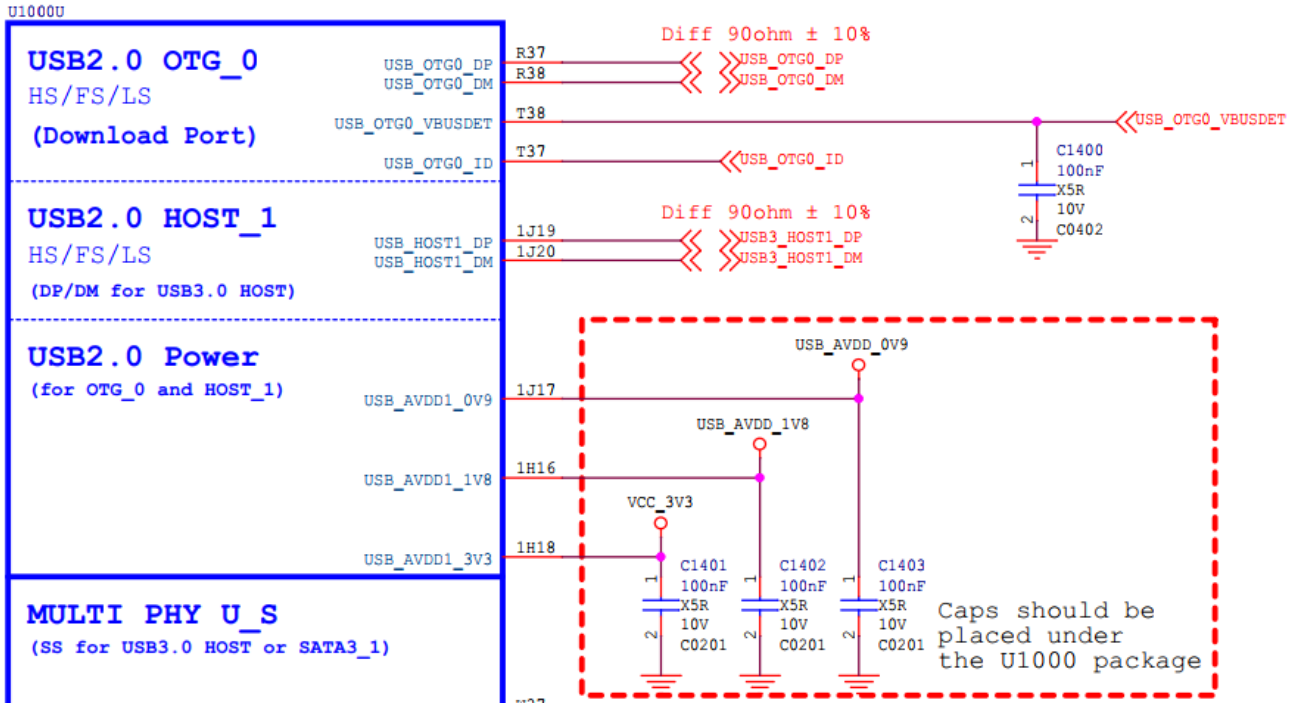


Figure 2-42 RK3566 USB2.0 OTG/HOST1 module

The USB_OTG0_VBUSDET pin is connected to the voltage divider circuit. When a high level is detected (2.7V-3.3V is judged to be high), it indicates that a USB is inserted. This pin should be connected whether it is used as an OTG port or used for firmware downloading.

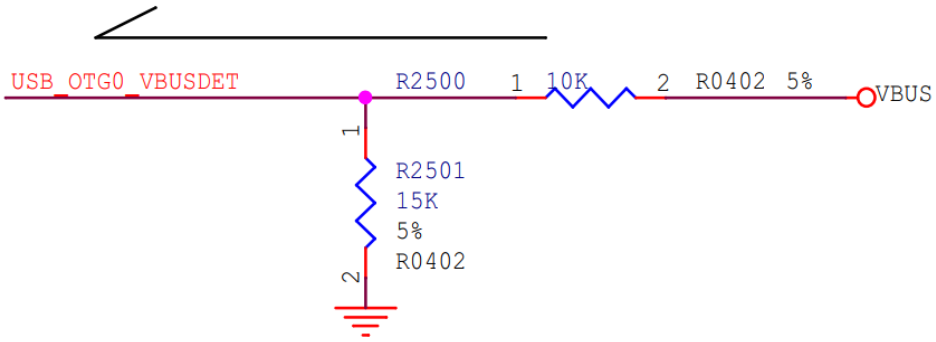


Figure 2-43 RK3566 USB2.0 OTG VBUSDET voltage divider circuit

To suppress electromagnetic radiation, common mode inductance is reserved on the signal line. In addition, to improve the ESD resistance of the interface, connect a 2.2R resistor in series and use ESD protection measures. The parasitic capacitance of the ESD device must be less than 1pF, and the ESD device should be placed close to the USB port. As shown in the figure below:

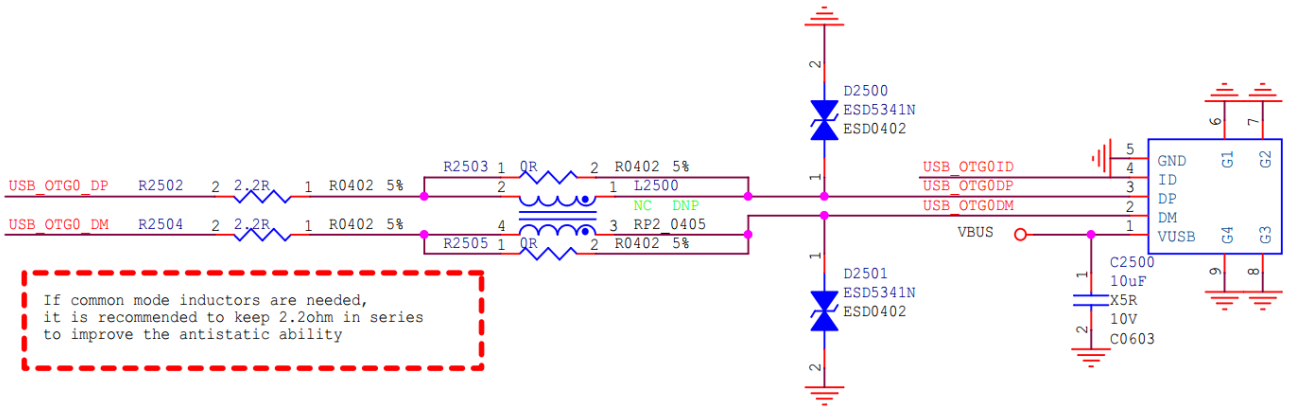


Figure 2-44 RK3566 USB2.0 OTG signal circuit protection

The reference diagram of RK817-5(tablet version), provides a reference for the TypeC(transfer OTG signals only) interface. It is necessary to add an OVP protection chip, and the OVP voltage is set at 5.5V. If you need to support analog headset and digital headset functions at the same time, a external switch circuit is needed. If you don't need analog headset function, just connect the USB signal directly to the interface.

The remaining USB2.0 HOST interfaces are shown in the figure below. For the protection design of the USB2.0 HOST interface, refer to the USB2.0 OTG interface. For details refer to the reference schematic diagram.

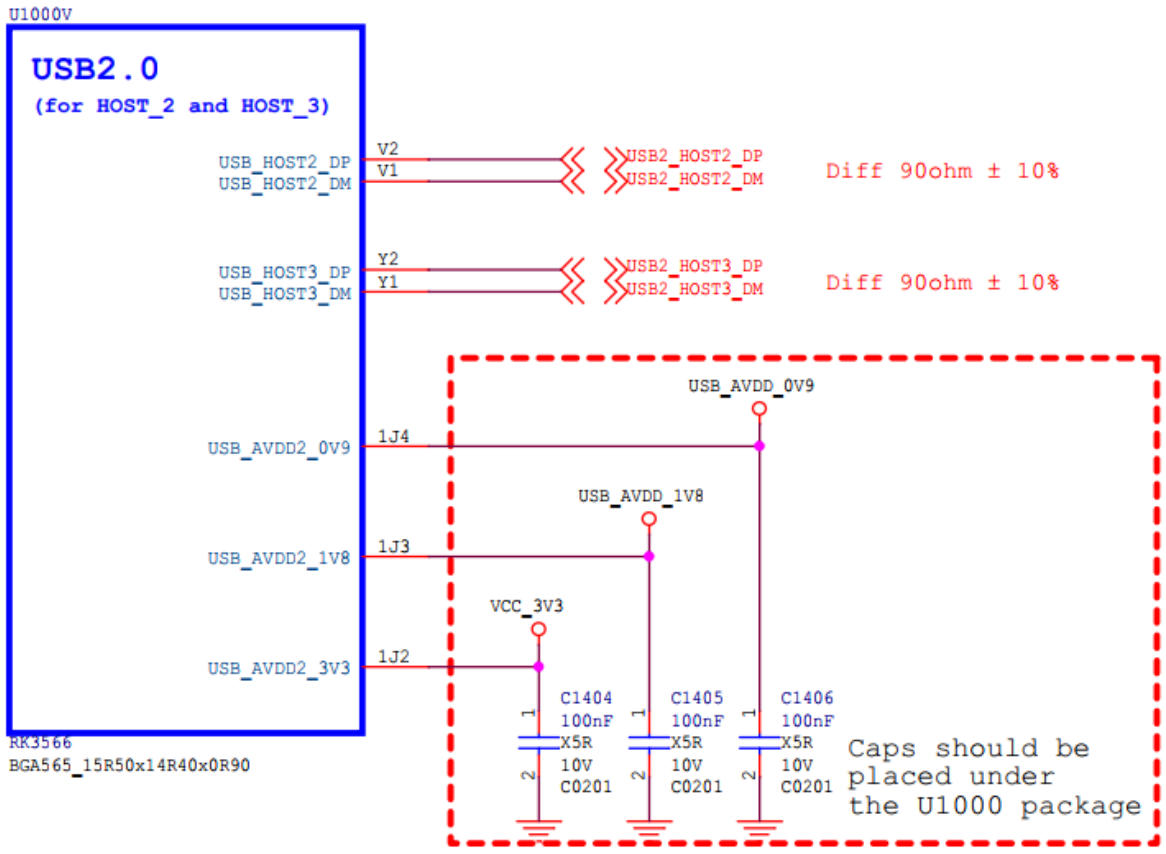


Figure 2-45 RK3566 USB2.0 HOST2/HOST3 module

2.3.2.2 USB3.2 Introduction

The high-speed differential signal part of RK3566 USB3.0 is integrated in MULTI PHY. For detailed multiplexing, please refer to the description of MULTI PHY chapter. It should be noted that the complete USB3.0 signal is composed of USB3.0 high-speed differential pair and USB2.0 HOST1. The corresponding relationship is fixed and cannot be adjusted at will.

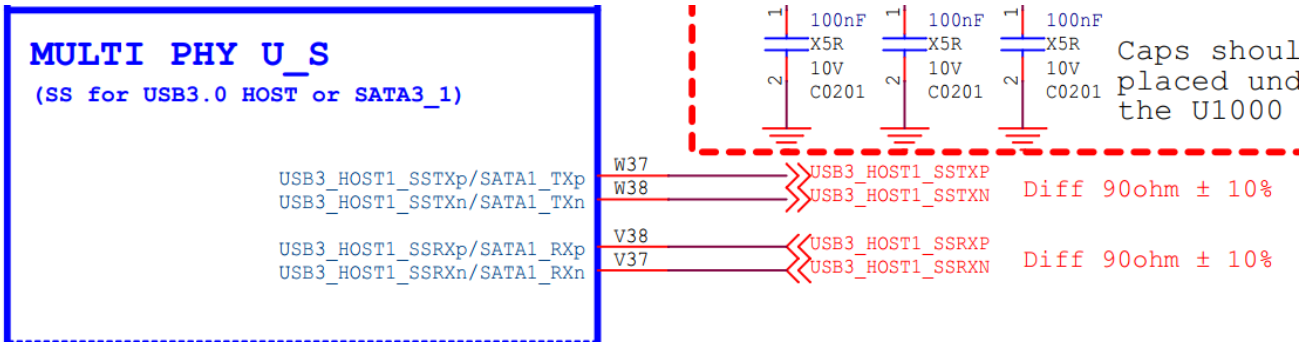


Figure 2-46 RK3566 USB3.0 module

For the USB2.0 HOST1 in the USB3.0 interface, the design points are described in the previous section. For the differential pair of USB3.0, the parasitic capacitance of the ESD device is required to be less than 0.4pF, and the location of the ESD device needs to be close to the USB interface. As shown below:

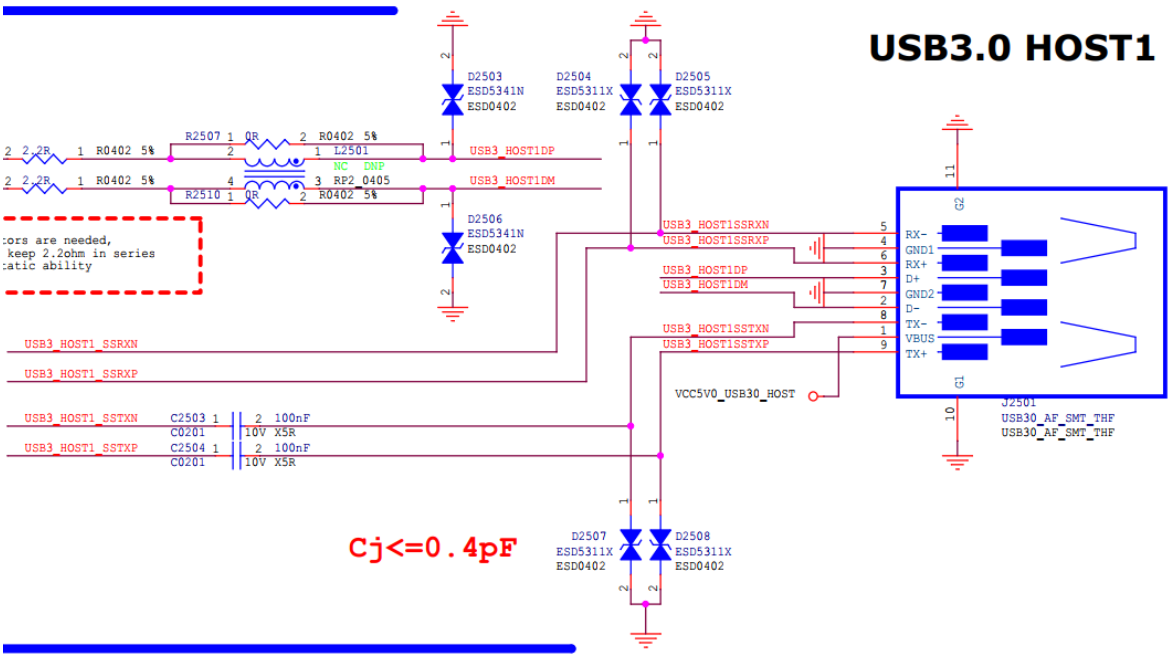


Figure 2-47 RK3566 USB3.0 signal circuit protection

2.3.2.3 USB Power Design

In order to ensure the quality of the USB power supply, the 0.9V/1.8V power supply of the controller needs to be connected in series with magnetic beads; at the same time, the decoupling capacitor of the USB controller power supply should be placed close to the pins.

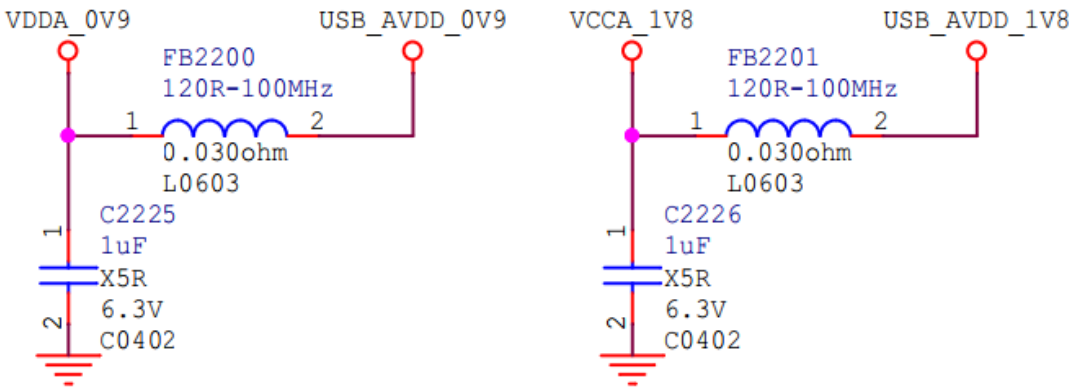


Figure 2-48 RK3566 USB controller power supply design

The USB interface pull up/down and matching design recommendations are as follows:

Table 2-13 RK3566 USB2.0 interface design

Signal	Connection method	Description
USB_OTG0_DP/DM	Series connect 2.2ohm resistor	USB OTG input/output
USB_OTG0_ID	Series connect 100ohm resistor (with internal 1.8V pull up)	USB OTG ID recognition, need to use for Micro-B interface
USB_OTG0_VBUSDET	Resistor voltage divider detection	USB OTG insertion detection
USB_HOST1_DP/DM	Series connect 2.2ohm resistor	USB HOST1 input/output
USB3_HOST1_SSTXP/SSTXN	Series connect 100nF capacitor	USB SS TX differential pair, impedance 90ohm±10%
USB3_HOST1_SSRXP/SSRXN	Direct connection or series connection 0ohm resistor(The specification requires that the peripheral TX is connected in series with a 100nF capacitor)	USB SS RX differential pair, impedance 90ohm±10%
USB3_HOST2_DP/DM	Series connect 2.2ohm resistor	USB HOST2 input/output
USB3_HOST3_DP/DM	Series connect 2.2ohm resistor	USB HOST3 input/output

2.3.3 SARADC Circuit

RK3566 integrates a SARADC controller, which can provide four SARADC inputs.

The RK3566 chip uses SARADC_VIN0 of SARADC as the key value input sampling port, and is multiplexed as a Recovery mode button (supported by the LOADER as default). SARADC_VIN0 is pulled up to VCCA_1V8 through a 10k pull-up resistor, and the default is high (1.8V). Under the premise that there is no key action and the system has been burned with firmware, the system will directly enter the system after power-on. If the Recovery mode button is pressed and SARADC_VIN0 remains at low level (0V) when the system starts, RK3566 will enter Rockusb Recovery download mode. When the PC recognizes the USB device, release the button to restore SARADC_VIN0 to a high level (1.8V), and the firmware can be downloaded. Therefore, when the Recovery mode button /SARADC_VIN0 is not used, it is still recommended to keep the 10k pull-up resistor of SARADC_VIN0 to ensure the default normal startup judgment.

On RK3566, the SARADC sampling range is 0-1.8V, and the sampling accuracy is 10bits. The key array adopts the parallel type, and the input key value can be adjusted by adding or subtracting keys and adjusting the voltage divider resistance ratio to achieve multi-key input to meet customer product requirements. It is recommended in the design that difference of any two key value must be greater than +/-35, that is, the center voltage difference must be greater than 123mV.

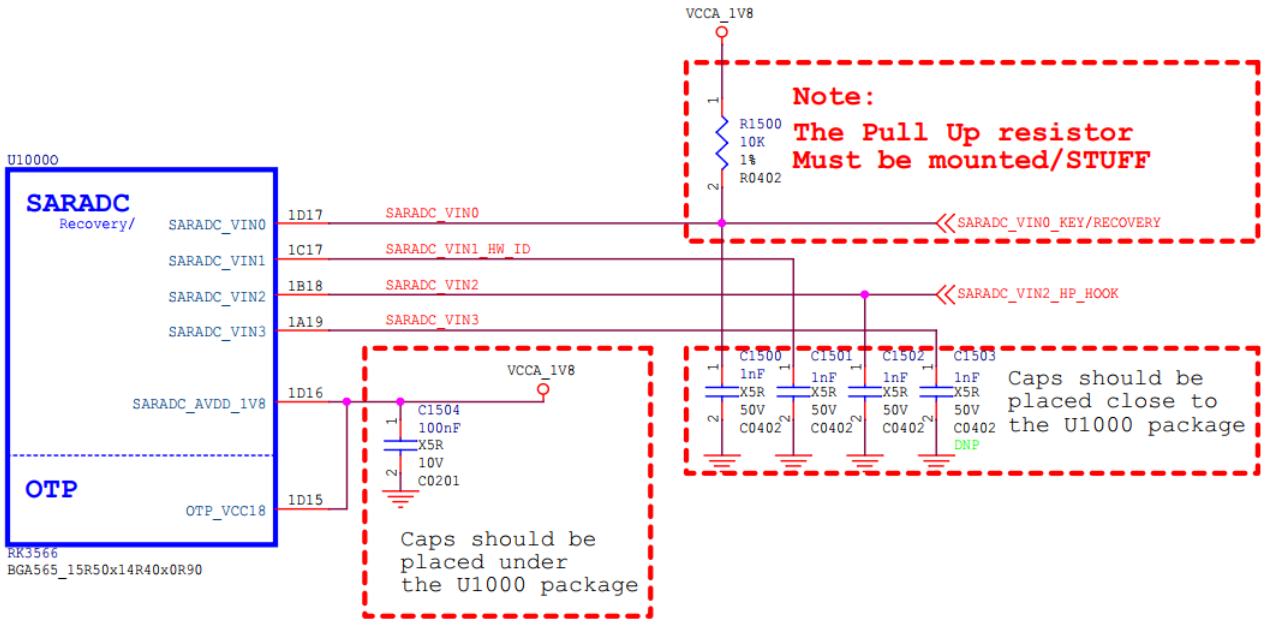


Figure 2-49 RK3566 SAR-ADC module

It should be noted in the design that the decoupling capacitor of the SARADC controller power supply should be placed close to the pin. The SARADC input is an analog signal, so it is necessary to protect the wiring, and try to maintain a wiring distance of more than 3W from other signals. If possible, it can be guarded with ground. In addition, when SARADC is used for button sample, ESD protection is required near the button, and anti-shake measures should be taken for the button signal input. See the reference schematic for the detailed circuit.

The SARADC interface design recommendations are as follows:

Table 2-14 RK3566 SARADC interface design

Signal	Connection method	Description(chip side)
SARADC_VIN0	Externally pull up to VCCA_1V8 through 10K, direct connection, connect a 1nF capacitor close to the pin	It is usually used for key sample and recovery mode status judgment.
SARADC_VIN[3:1]	Direct connection, connect a 1nF capacitor close to the pin	It can be flexibly used for all kinds of analog signal sample

2.3.4 OTP Circuit

RK3566 integrates 8Kbit OTP, of which 7Kbit can be used for security applications. OTP supports write, read and idle modes. In these modes, the OTP_VCC18 pin must be powered, and the power decoupling capacitor must be reserved and placed close to the RK3566 pin.

2.3.5 UART and Debug UART Circuit

2.3.5.1 UART Resource Introduction

RK3566 integrates 10 groups of UART interfaces, similar to other interfaces. Considering the diversity of interface applications of the product, the UART controller is multiplexed. In the schematic diagram, the suffix

"_M0/M1/M2" indicates the number of the corresponding function. During the design, need to allocate resources to avoid conflicts.

Table 2-15 RK3566 UART interface distribution

UART Number	UART Multiplexed	Power Domain
UART0	none	PMUIO2
UART1	M0,M1	M0:VCCIO4 M1:VCCIO6
UART2	M0,M1	M0:PMUIO2 M1:VCCIO3
UART3	M0,M1	M0:VCCIO1 M1:VCCIO5
UART4	M0,M1	M0:VCCIO1 M1:VCCIO5
UART5	M0,M1	M0:VCCIO3 M1:VCCIO5
UART6	M0,M1	M0:VCCIO4 M1:VCCIO3
UART7	M0,M1,M2	M0:VCCIO4 M1:VCCIO5 M2:VCCIO6
UART8	M0	M0:VCCIO4
UART9	M0,M1,M2	M0:VCCIO4 M1:VCCIO7 M2:VCCIO6

The UART controller supports the following functions:

- Supports 10 independent UART controllers, each of which contains two 64-byte FIFOs for data reception and transmission;
- In addition to supporting 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps, all support automatic flow control;
- Support programmable baud rate, support non-integer clock divider;
- Support interrupt-based mode or DMA-based mode;
- Support 5-8 bit width transmission.

2.3.5.2 Debug UART Circuit

The debugging UART of RK3566 uses UART2_RX_M0 by default, which belongs to the PMUIO2 power domain. When debugging is needed, an external UART to USB adapter board can be connected for debugging. Therefore, it is strongly recommended to reserve TP points for debugging serial port signals or reserve test headers in the customer's design.

It should be noted that the IO level of UART2_RX_M0 depends on the actual power supply of PMUIO2, the default is 1.8V in the tablet reference design, and the default is 3.3V in the AIoT reference design. According to the

actual level and the situation of the conversion chip, decide whether to carry out voltage division or level conversion processing.

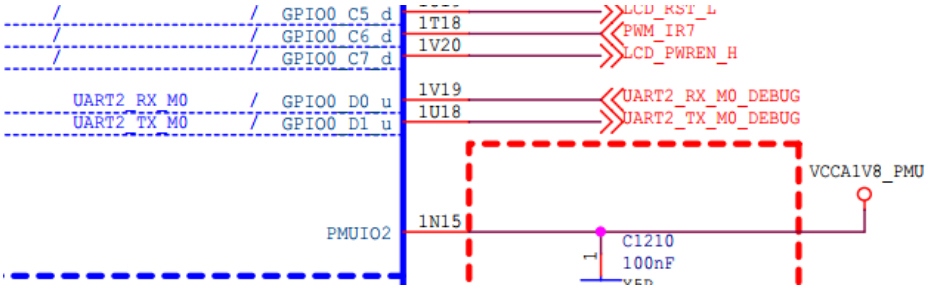


Figure 2-50 RK3566 UART2 debug points

In the debugging and production stage, you need to pay attention to the protection of the Debug UART2 interface. Refer to the following:

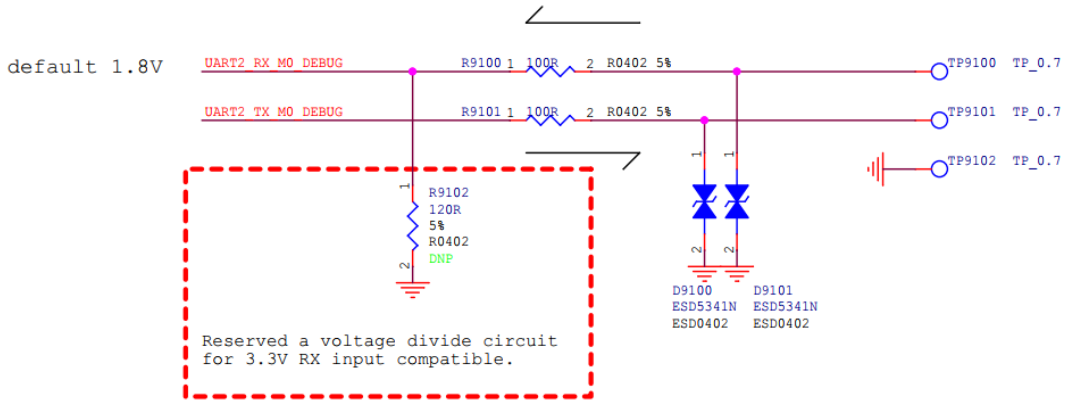


Figure 2-51 RK3566 UART2 interface protection circuit

The port number selects the port number of the PC connected to the development board, the baud rate is 1.5M, and the flow control RTS/CTS does not need to be checked(no flow control). If the built-in DB-9 port on the PC does not support high-speed mode, please use a UART to USB adapter.

Figure 2-52 RK3566 serial port configuration

2.3.6 I2C Circuit

I2C is a two-wire bidirectional serial bus. The I2C controller of RK3566 supports the following functions:

- Support 7 independent I2C;
- Support I2S bus master mode;
- Software programmable clock frequency and transmission rate up to 400Kbit/s;
- Support 7-bit/10-bit addressing mode;

I2C also supports multiplexing. The suffix with "_M0/M1" in the schematic diagram is the description of the multiplexing number of the corresponding function. It is necessary to allocate resources well to avoid conflicts during designing. As I2C is more likely to encounter conflicts, it is particularly emphasized. At the same time, it should be noted that the addresses of the peripherals on the I2C bus do not conflict, the pull-up power supply is consistent, and the peripherals have no risk of leakage or backflow.

Table 2-16 RK3566 I2C interface distribution

I2C Number	I2C Multiplexed	Power Domain
I2C0	None	PMUIO2
I2C1	None	PMUIO2
I2C2	M0,M1	M0:PMUIO2; M1:VCCIO6
I2C3	M0,M1	M0:VCCIO1; M1:VCCIO5
I2C4	M0,M1	M0:VCCIO6; M1:VCCIO4
I2C5	M0,M1	M0:VCCIO5; M1:VCCIO7
I2C_HDMI	None	VCCIO7

Among them, I2C0 belongs to the PMUIO2 power domain and is used to connect to the PMIC by default. It is recommended to keep this group of connections to reduce software changes. The remaining I2C can be flexibly allocated according to the actual situations such as level and peripherals.

In addition, it needs to be specially stated that HDMITX_SCL/HDMITX_SDA is an I2C/DDC bus dedicated for the HDMI TX controller, and do not used for other purposes.

2.3.7 PWM Circuit

Pulse width modulation (PWM) technology is widely used in product design, and is often used in applications such as controlling servo motors or backlight voltage regulation. RK3566 integrates 4 independent PWM controllers, each controller has 4 channels, so there can be up to 16 PWM channels.

The PWM of K3566 has the following characteristics:

- Support capture mode;
- Support continuous mode or single shot mode;
- Support secondary frequency division;
- Support low power consumption mode, reduce power consumption when the channel is inactive;

Among them, PWM3, PWM7, PWM11, PWM15 can be used for infrared receiving and decoding applications. Through the dedicated hardware decoder integrated inside the chip, the infrared signal decoding efficiency can be improved. When infrared receiver wake-up is required, need to use PWM3_IR;

The multiplexing of PWM signals is shown in the following table. The suffix with "_M0/M1" in the schematic diagram are the descriptions of the multiplexing numbers of the corresponding functions. Resource allocation should be done during design to avoid conflicts.

Table 2-17 RK3566 PWM interface distribution

PWM Number	PWM Multiplexed	Power Domain
PWM0	M0,M1	M0:PMUIO2 M1:PMUIO2
PWM1	M0,M1	M0:PMUIO2 M1:PMUIO2
PWM2	M0,M1	M0:PMUIO2 M1:PMUIO2
PWM3_IR	none	PMUIO2
PWM4	none	PMUIO2
PWM5	none	PMUIO2
PWM6	none	PMUIO2
PWM7_IR	none	PMUIO2
PWM8	M0,M1	M0:VCCIO5 M1:VCCIO3
PWM9	M0,M1	M0:VCCIO5 M1:VCCIO3
PWM10	M0,M1	M0:VCCIO5 M1:VCCIO3

PWM Number	PWM Multiplexed	Power Domain
PWM11_IR	M0,M1	M0:VCCIO5 M1:VCCIO6
PWM12	M0,M1	M0:VCCIO5 M1:VCCIO7
PWM13	M0,M1	M0:VCCIO5 M1:VCCIO7
PWM14	M0,M1	M0:VCCIO5 M1:VCCIO7
PWM15_IR	M0,M1	M0:VCCIO5 M1:VCCIO7

2.3.8 SPI Circuit

In addition to the FSPI controller, RK3566 also integrates 4 general-purpose SPI controllers, all of which support master and slave modes. The SPI controller also supports multiplexing. The suffix with "_M0/M1" in the schematic diagram is the description of the multiplexing number of the corresponding function. Resource allocation should be done during design to avoid conflicts.

Table 2-18 RK3566 SPI interface distribution

SPI Number	SPI Multiplexed	Power Domain
SPI0	M0	PMUIO2
SPI1	M0,M1	M0:VCCIO4 M1:VCCIO5
SPI2	M0	M0:VCCIO4
SPI3	M0,M1	M0:VCCIO6 M1:VCCIO7

2.3.9 Ethernet Interface

RK3566 has a built-in GMAC controller, provides RMII interface and RGMII interface, and is compatible with the complete Ethernet interface 10/100/1000M Ethernet controller of the Ethernet physical layer.:

- RGMII interface supporting 10/100/1000Mbps data transmission rate;
- RMII interface supporting 10/100Mbps data transmission rate;
- Support full-duplex and half-duplex operation;
- Support TCP segmentation offload (TSO) and UDP fragmentation offload (UFO) network acceleration.

The RGMII function pins are multiplexed in two power domains. The power domain of RGMII_M0 is VCCIO5, and the power domain of RGMII_M1 is VCCIO6. Only one set of interfaces can be used at a time. GMAC's power supply VCCIO5 or VCCIO6 can use 1.8V or 3.3V power supply, and it must be consistent with the IO level of the PHY.

The definition of RGMII and RMII interface are one-to-one correspondence. For example, when configured as 100MPHY, RGMII_CLK can be used as RMII_CLK, and so on.

Some considerations for signal design:

- In RGMII interface transceiver signal line, TX_CLK and RX_CLK are 125MHz, in order to achieve the transmission rate of 1000Mbps, TX data and RX data signal lines are sampled on both edge of the clock, the data enable signal (RGMII_TXEN, RGMII_RXDV) must be valid before the data is send.
- Reset: RGMII uses GPIO to control the reset method of PHY, or RC hardware reset circuit. It should be noted that if RC hardware reset circuit is used, the power of PHY must be controllable. By default, GPIO is used to control.
- The transmission of control and status information between the MAC layer and the PHY is the MDIO interface, the clock MDC signal and the data MDIO signal. It should be noted that the MDIO signal needs to be pulled up.
- The principle and connection of 10/100M are similar to 1000M, except that RGMII_CLK=50M; it should be noted that PHY_CRS_DV of 10/100M is connected to RGMII_RXDV.
- The RGMII interface can be connected to different Ethernet PHY to realize 100M/1000M network functions. Please refer to the original design documents of the PHY for the specific design.

2.3.9.1 RGMII Interface and 1000M PHY Design

RGMII can provide the following clock schemes, as shown in the figure below:

- The first type: The external crystal oscillator provides a 25MHz clock signal to the XTAL pin of the Ethernet PHY, and then the PHY converts it into a 125MHz clock signal internally. This clock signal can be output through the CLKOUT pin of the PHY and connected to the RGMII_CLK pin of the RK3566. Note that the PHY and GAMC controller are at the same voltage level.
- The second type: the external crystal oscillator provides a 25MHz clock signal to the XTAL pin of the Ethernet PHY, but does not need to return the CLK signal from the PHY (the RGMII_CLK pin of the RK3566 does not need to be used at this time), RK3566 output a 125MHz CLOCK signal from the RGMII_TXCLK pin and connect to the TXC pin of the PHY.
- The third type: EHT1_REFCLKO_25M pin provides a 25MHz clock signal to the Ethernet PHY, and then the PHY converts it into a 125MHz clock signal internally. This clock signal can be output from the CLKOUT pin of the PHY and connected to the RGMII_CLK pin of the RK3566. Note that the PHY and GAMC controller are at the same voltage level.
- The fourth type: The EHT1_REFCLKO_25M pin provides a 25MHz clock signal to the Ethernet PHY, but does not need to return the CLK signal from the PHY (the RGMII_CLK pin of the RK3566 is not needed at this time), RK3566 output a 125MHz CLOCK signal from the RGMII_TXCLK pin of the master and connect to the TXC pin of the PHY.

The 1st method is currently used by default.

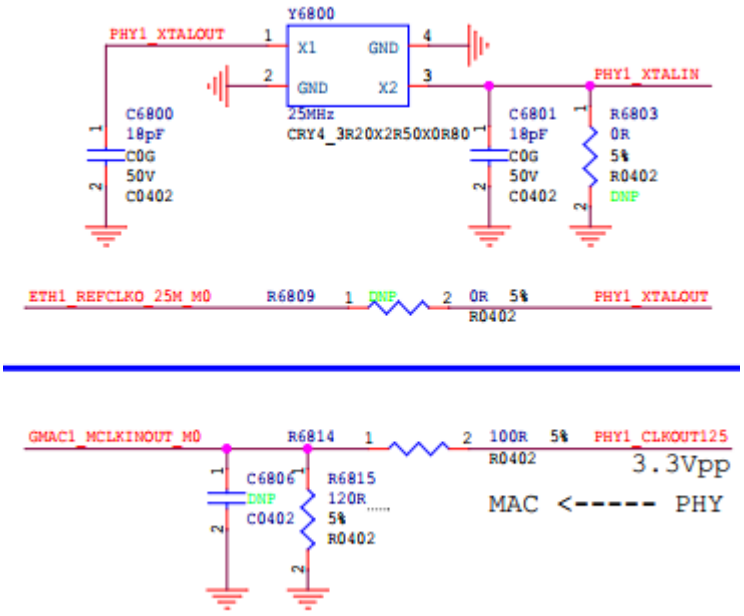


Figure 2-53 RK3566 GMAC Clock circuit

RGMII interface pull-up/down and matching design recommendations are as follows, the power domain of RGMII_M0 is VCCIO5, and the power domain of RGMII_M1 is VCCIO6, which are all multiplexed by the entire group. Do not repeat it here.

Table 2-19 RK3566 RGMII/GMII interface design

RGMII Signal	RMII Signal	Internal Pull up/down	Connection Method	Description
EHT1_REFCLKO_25M		pull down	Series connect 22ohm resistor	Output reference clock to PHY
GMAC_MCLKINOUT	RMII_CLK	pull down	Series connect 22ohm resistor	GMAC clock output or input
GMAC_MDIO	RMII_MDIO	pull down	Series connect 22ohm resistor	MDIO data
GMAC_MDC	RMII_MDC	pull down	Series connect 22ohm resistor	MDIO clock
GMAC_RXDV_CRS	RMII_RXDV	pull down	Series connect 22ohm resistor	CRS: Physical CRS signal, not necessary RXDV: RMII's RX data has message and carrier detection
GMAC_COL		pull down	Series connect 22ohm resistor	Detect physical collision, not necessary
GMAC_RXER	RMII_RXER	pull down	Series connect 22ohm resistor	MAC receiving error, not required
GMAC_RXCLK		pull down	Series connect 22ohm resistor	GMAC receive clock
GMAC_RXD[3:0]	RMII_RXD	pull down	Series connect	GMAC receive data

RGMII Signal	RMII Signal	Internal Pull up/down	Connection Method	Description
	[1:0]		22ohm resistor	
GMAC_TXD[3:0]	RMII_TXD [1:0]	pull down	Series connect 22ohm resistor	GMAC send data
GMAC_TXEN	RMII_TXEN	pull down	Series connect 22ohm resistor	GMAC sends data valid signal
GMAC_TXCLK		pull down	Series connect 22ohm resistor	GMAC send clock

Design attention:

- The circuit design of Ethernet PHY is detailed in the reference schematic diagram;
- The series resistance of the ETH1_REFCLKO_25M clock is close to the main control; the wiring must be guarded with ground and ground vias, and the interval of ground vias should not be greater than 300mil;
- The series resistance of RXD, RXDV, and RXCLK are close to the PHY;
- The series resistance of TXD, TXEN, TXCLK is close to the RK3566;
- The delay between TXCLK and TXD,TXEN must be controlled within 120mil;
- The delay between RXCLK and RXD, RXDV must be controlled within 120mil;
- TXCLK and RXCLK must be guarded with ground and ground vias, and the interval of ground vias should not be greater than 300mil;
- The reference layer of all RGMII signals needs to be a complete ground plane to avoid continuous vias blocking the signal return path;
- RGMII signal needs to control the impedance, single-ended impedance is 50ohm±10%; RGMII signal wiring does not exceed 5inch;

2.3.9.2 Correspondence between RMII Interface and 100M PHY Signal

The multiplexing relationship of related signals is as shown in the figure below. Pay attention to the TX/RX direction:

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------>	PHYx_TXD0	GMACx_TXD0	------>	PHYx_TXD0
GMACx_TXD1	------>	PHYx_TXD1	GMACx_TXD1	------>	PHYx_TXD1
GMACx_TXD2	------>	PHYx_TXD2			
GMACx_TXD3	------>	PHYx_TXD3			
GMACx_TXEN	------>	PHYx_TXEN	GMACx_TXEN	------>	PHYx_TXEN
GMACx_TXCLK	------>	PHYx_TXCLK			
GMACx_RXD0	<------	PHYx_RXD0	GMACx_RXD0	<------	PHYx_RXD0
GMACx_RXD1	<------	PHYx_RXD1	GMACx_RXD1	<------	PHYx_RXD1
GMACx_RXD2	<------	PHYx_RXD2			
GMACx_RXD3	<------	PHYx_RXD3			
GMACx_RXDV	<------	PHYx_RXDV	GMACx_RXDV	<------	PHYx_CRS_DV
GMACx_RXCLK	<------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<------	PHYx_RXER
GMACx_MDC	------>	PHYx_MDC	GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<----->	PHYx_MDIO	GMACx_MDIO	<----->	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx_XTALIN			
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125 (Option)	GMACx_MCLKINOUT	------>	PHYx_XTALIN/REFCLK
GPIO	------>	PHYx_RSTn	GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB	GPIO	<------	PHYx_INT/PMEB

Figure 2-54 RK3566 RGMII RMII signal correspondence

2.4 Audio related Circuit Design

RK3566 provides three groups of standard I2S interface, all supporting master or slave mode, the highest sampling rate up to 192 kHz, and bit rate from 16 bits to 32 bits.

In addition, one 8 channel PDM input interface and a SPDIF TX are also provided.

2.4.1 I2S1 Digital Audio Interface

I2S0 interface contains independent 8 channels output and 8 channels input. In order to meet the asynchronous sampling rate requirement of audio recording and playing, it provides two groups of bit clock and frame clock (SCLKTX\LRCKTX, SCLKRX\LRCKRX) accordingly. Need to pay attention to that, if SDOx and SDIx only refer to one group of bit/frame clock, use SCLKTX\LRCKTX as their common clock by default.

I2S1 interface supports master-slave working mode, software configurable; supports 3 kinds of I2S formats (normal, left-justified, right-justified); supports 4 kinds of PCM formats (early, late1, late2, late3).

This group of I2S pins are multiplexed in two different power domains, I2S1_M0 is multiplexed in VCCIO1, of which three SDOx and SDIx signals have multiplexing conflicts; I2S1_M1 is multiplexed in VCCIO6, which can completely lead out all signals. I2S1_M0 and I2S1_M1 cannot be used at the same time, only one of them can be used at a time. It is necessary to adjust the power supply of the corresponding power domain according to the IO level of the I2S peripheral to make it match.

In the case of using the PMIC power supply solution, I2S1_M0 is usually used as the audio communication interface of the PMIC integrated Codec, so this group of VCCIO power supply can directly use the PMIC's VCCIO_ACODEC power supply.

I2S0 interface pull-up/down and matching design recommendations are shown in the table.

Table 2-20 RK3566 I2S1 interface design

Signal	Internal pull up/down	Connection Method	Description (chip side)
I2S1_8CH_MCLK	pull down	Series connect 22ohm resistor	I2S system clock output for slave
I2S1_8CH_SCLK_TX	pull down	Series connect 22ohm resistor	I2S bit clock (TX, related with Audio Play)
I2S1_8CH_LRCK_TX	pull down	Series connect 22ohm resistor	I2S frame clock for channel selection (TX, related with Audio Play)
I2S1_8CH_SDO0	pull down	direct connection	I2S serial data 0 output
I2S1_8CH_SDO1	pull down	direct connection	I2S serial data 1 output
I2S1_8CH_SDO2	pull down	direct connection	I2S serial data 2 output
I2S1_8CH_SDO3	pull down	direct connection	I2S serial data 3 output
I2S1_8CH_SCLKRX	pull down	Series connect 22ohm resistor	I2S bit clock (RX, related with Audio Record)
I2S1_8CH_LRCKRX	pull down	Series connect 22ohm resistor	I2S frame clock for channel selection (RX, related with Audio Record)
I2S1_8CH_SDI0	pull down	direct connection	I2S serial data 0 input
I2S1_8CH_SDI1	pull down	direct connection	I2S serial data 1 input
I2S1_8CH_SDI2	pull down	direct connection	I2S serial data 2 input
I2S1_8CH_SDI3	pull down	direct connection	I2S serial data 3 input

2.4.2 I2S2 Digital Audio Interface

The I2S2 interface includes independent 2-channel output and 2-channel input. In order to meet the needs of asynchronous sampling rates for playback and recording, two sets of bit clock and frame clock (SCLKTX\LRCKTX, SCLKRX\LRCKRX) are also provided correspondingly. Need to pay attention to that, if SDOx and SDIx only refer to one group of bit/frame clock, use SCLKTX\LRCKTX as their common clock by default.

The I2S2 interface supports master-slave working mode, software configurable; supports 3 kinds of I2S formats (normal, left-justified, right-justified); supports 4 kinds of PCM formats (early, late1, late2, late3).

This group of I2S pins are multiplexed in two different power domains, I2S2_M0 is multiplexed in VCCIO4, and I2S2_M1 is multiplexed in VCCIO6, all signals can be fully derived. I2S2_M0 and I2S2_M1 cannot be used at the same time, only one of them can be used at a time. It is necessary to adjust the power supply of the corresponding power domain according to the IO level of the I2S peripheral to make it match.

In a design with Bluetooth function, I2S2 uses M0 multiplexing by default as PCM function to connect with Bluetooth peripherals. In the design, it is necessary to check the corresponding connection relationship between the interface and the receiving and sending signals of the Bluetooth peripheral.

I2S2 interface pull-up/down and matching design recommendations are shown in the table.

Table 2-21 RK3566 I2S2 interface design

Signal	Internal pull up/down	Connection Method	Description (chip side)
I2S2_MCLK	pull down	Series connect 22ohm resistor	I2S system clock output
I2S2_SCLK_TX	pull down	Series connect 22ohm resistor	I2S continuous serial clock (TX, related with Audio Play)
I2S2_LRCK_TX	pull down	Series connect 22ohm resistor	I2S frame clock for channel selection (TX, related with Audio Play)
I2S2_SDO0	pull down	direct connection	I2S serial data 0 output
I2S2_SCLKRX	pull down	Series connect 22ohm resistor	I2S continuous serial clock (TX, related with Audio Play)
I2S2_LRCKRX	pull down	Series connect 22ohm resistor	I2S frame clock for channel selection (TX, related with Audio record)
I2S2_SDI0	pull down	direct connection	I2S serial data 0 input

2.4.3 I2S3 Digital Audio Interface

The I2S3 interface supports 2-channel output and 2-channel input, and the sampling rate must be coincident.

The I2S3 interface supports master-slave working mode, software configurable; supports 3 kinds of I2S formats (normal, left-justified, right-justified); supports 4 kinds of PCM formats (early, late1, late2, late3).

This group of I2S pins are multiplexed in two different power domains, I2S3_M0 is multiplexed in VCCIO5, and I2S3_M1 is multiplexed in VCCIO7, all signals can be fully derived. I2S3_M0 and I2S3_M1 cannot be used at the same time, only one of them can be used at a time. It is necessary to adjust the power supply of the corresponding power domain according to the IO level of the I2S peripheral to make it match.

I2S3 interface pull-up/down and matching design recommendations are shown in the table.

Table 2-22 RK3566 I2S3 interface design

Signal	Internal pull up/down	Connection Method	Description (chip side)
I2S3_MCLK	pull down	Series connect 22ohm resistor	I2S system clock output
I2S3_SCLK	pull down	Series connect 22ohm resistor	I2S continuous serial clock (TX, related with Audio Play)
I2S3_LRCK	pull down	Series connect 22ohm resistor	I2S frame clock for channel selection (TX, related with Audio Play)
I2S3_SDO0	pull down	direct connection	I2S serial data 0 output
I2S3_SDI0	pull down	direct connection	I2S serial data 0 input

2.4.4 PDM Digital Audio Interface

RK3566 provides one PDM digital audio interface, supports up to 8 channels of PDM format audio input (Each PDM_SDI is time-shared sampling on rising/falling edges, so two channels of audio data can be transfer through one data line), the maximum sampling rate is up to 192kHz, the bit rate is from 16bits to 32bits.

This group of PDM pins are multiplexed in three different power domains, PDM_M0 is multiplexed in VCCIO1, PDM1_M1 is multiplexed in VCCIO6, and PDM_M2 is multiplexed in VCCIO5. The three multiplexing cannot be

used at the same time, only one of them can be used at a time. It is necessary to adjust the power supply of the corresponding power domain according to the IO level of the PDM peripheral to make it match.

PDM interface pull-up/down and matching design recommendations are shown in the table. In order to weaken the impact of PCB traces on the clock, two PDM clocks of the same origin and phase are provided: PDM_CLK0 and PDM_CLK1.

Table 2-23 RK3566 PDM interface design

Signal	Internal pull up/down	Connection Method	Description (chip side)
PDM_CLK0	pull down	Series connect 22ohm resistor	PDM clock 0
PDM_CLK1	pull down	Series connect 22ohm resistor	PDM clock 1
PDM_SDI[3:0]	pull down	direct connection	PDM data input 0、1、2、3

2.4.5 SPDIF Digital Audio Interface

RK3566 provides a SPDIF TX digital audio interface, which supports a maximum resolution of 24bits. The full name of SPDIF is Sony/Philips Digital Interface Format, which is short for SONY and PHILIPS digital audio interface. As far as the transmission carrier is concerned, SPDIF is divided into two types: coaxial and optical fiber. The signals transmitted by the two are the same, the transmission relies on different carriers, and the appearance of interfaces and connections are also different. The communication rate of SPDIF is usually limited by the carrier, so Need to consider the interface device specification used when designing the hardware. However, optical signal transmission does not need to consider interface level and impedance issues, and the interface is flexible and has stronger anti-interference ability.

The following figure is the reference schematic of the optical fiber SPDIF interface. It is recommended to make a ground guard when routing:

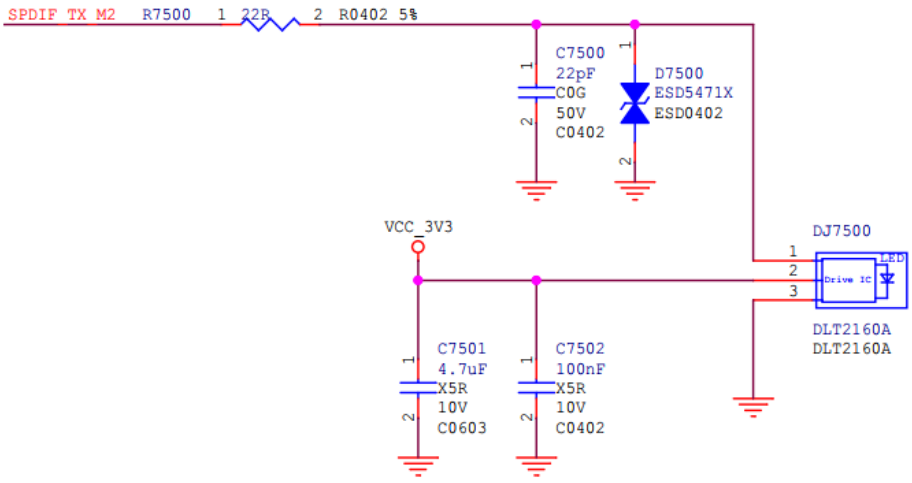


Figure 2-55 RK3566 SPDIF optical fiber interface circuit

SPDIF interface pull-up and pull-down and matching design recommendations are shown in the table.

SPDIF signal traces are recommended to be covered with ground in the whole process, and ground vias should be punched in the ground path, and the spacing between ground vias should not be greater than 300mil.

Table 2-24 RK3566 SPDIF interface design

Signal and Multiplexing Situation	Internal pull up/down	Connection Method	Power Domain
SPDIF_TX_M0	Pull down	Series connect 22ohm resistor	VCCIO1
SPDIF_TX_M1	Pull down	Series connect 22ohm resistor	VCCIO5
SPDIF_TX_M2	Pull down	Series connect 22ohm resistor	VCCIO7

2.4.6 Codec and Analog Audio Interface

In the case of using PMIC power supply solution, RK817-5/RK809-5's own Codec can realize the functions of headphone output, low-power mono speakers, one differential or two single-ended audio inputs. The two circuits are the same, the following uses RK817-5 as a guide to introduce:

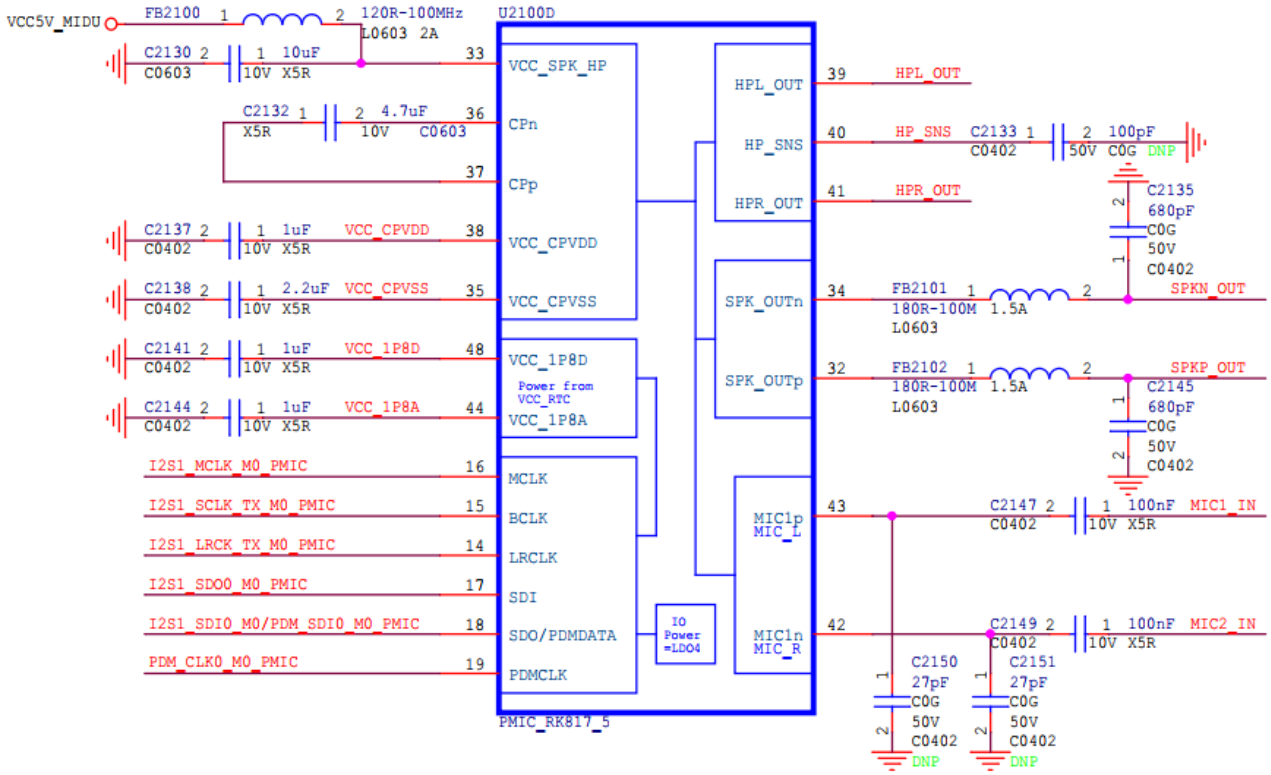


Figure 2-56 RK817-5 Codec circuit

NOTE

If the Codec function of RK817-5/RK809-5 is not used, the related pins MCLK/BCLK/LRCLK/SDI/PDMCLK/HP_SNS must be connected to ground, and the remaining SDO/PDMDATA/CPn/CPp/VCC_CPVDD/VCC_CPVSS/HPL_OUT/HPR_OUT/ SPK_OUTn/SPK_OUTp/MIC1p/MIC1n pins can be left floating.

The HPSNS input by Codec is used as the internal Offset reference, and this pin needs to be connected to GND externally for reference. For the case where HPOUT is used as LINEOUT to connect to an external power amplifier, HPSNS can be grounded near the PMIC. For headphone output scenarios, HPSNS needs to be routed separately to the headphone socket and connected to GND pin of the audio jack to reduce the level difference with

the headphone ground. When routing, it should be routed in the middle of HPR/HPL to avoid interference from other signals. The circuit is shown in the figure below. The HP_DET of the headphone jack is connected in series with a 1KOhm resistor, and a 100nF filter capacitor and ESD device are reserved to enhance the anti-static surge capability. HP_DET can use the internal pull-up of GPIO. At this time, the external 100KOhm pull-up resistor does not need to be stuffed.

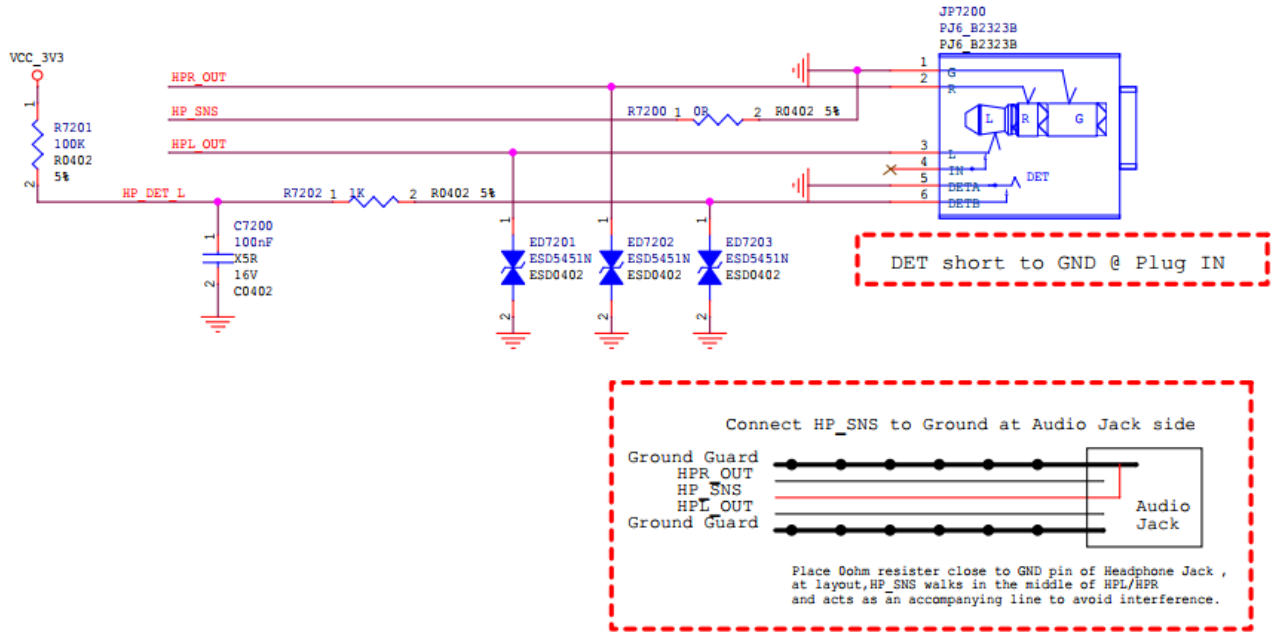


Figure 2-57 RK817-5 Headphone circuit

Codec has a built-in mono filter-free speaker driver circuit, which can provide 1.3W@8ohm driving capability, which can meet the application scenarios of low-power mono output and save the cost of additional external power amplifiers. The filter circuit of the speaker output should be placed close to RK817-5, and the ESD protection device is placed close to the connector.

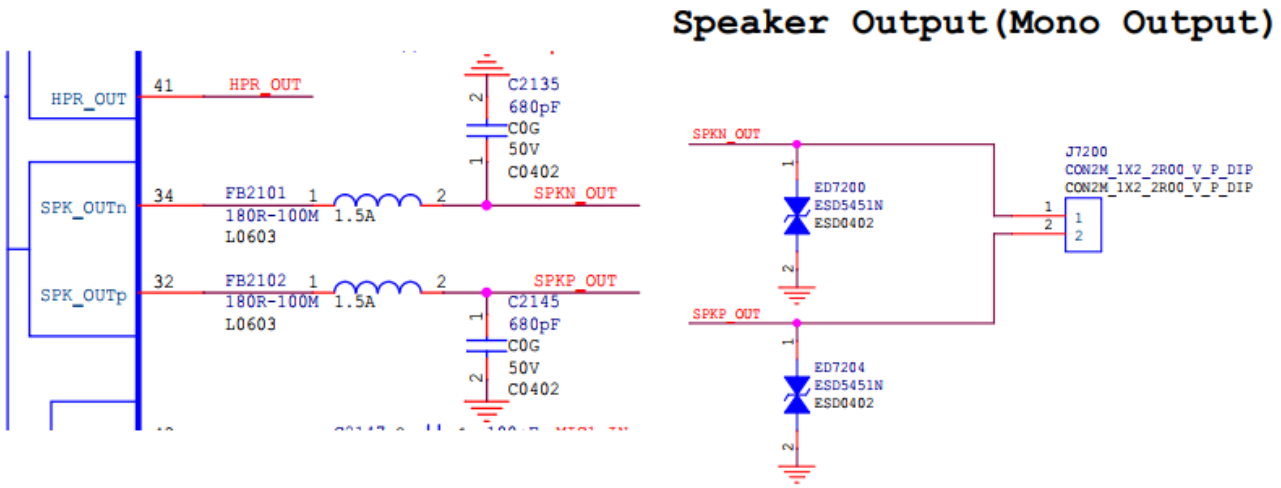


Figure 2-58 RK817-5 Speaker circuit

If Codec's built-in mono speaker drive circuit cannot meet the requirements for drive capability, or need to achieve stereo function or pursue higher sound quality, need to use the independent analog/digital power amplifier. When an analog power amplifier is adopted, use HPOUT as LINEOUT for output; when a digital power amplifier is used, connect it to the I2S interface.

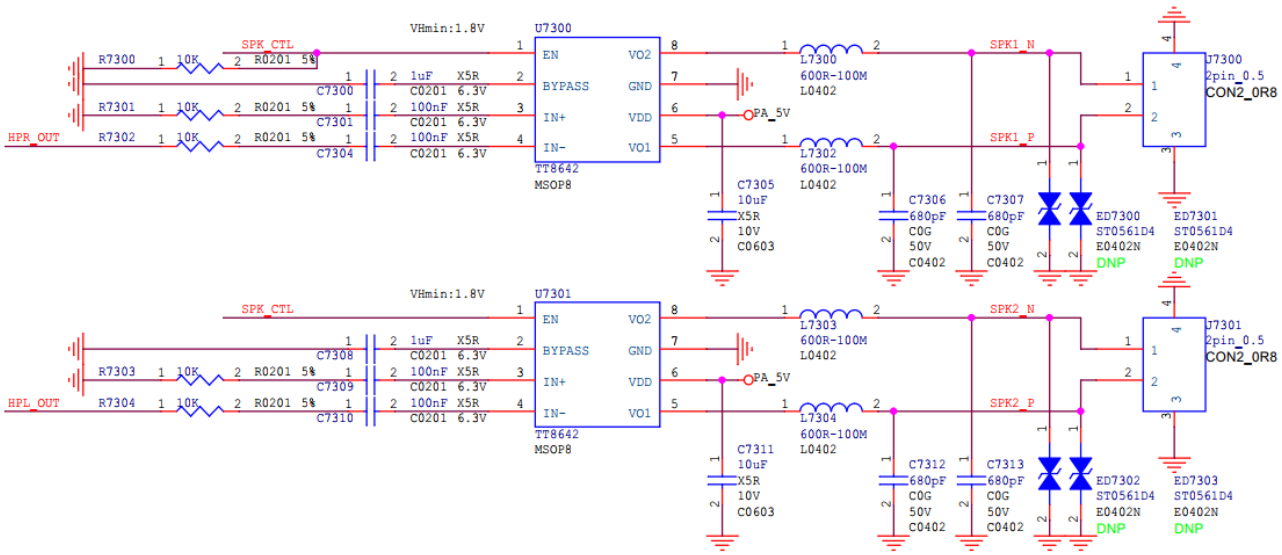


Figure 2-59 RK817-5 external analog power amplifier diagram

It should be noted that when the output power of the power amplifier is too large, the VCC5V_MIDU of RK817-5 may not be able to meet the power supply requirements. At this time, a boost power circuit need to use, and boosting power can be directly taken from VBAT to meet the load requirements.

2.4.6.1 MIC

The MIC circuit is shown in the figure below. When four-segment headphones are used, the analog ADC of RK817-5 can be split into two single-ended inputs. When three-segment headphones are used, the analog ADC of RK817-5 can be configured as a differential input. Compared with single-ended input, differential input has better recording effect and lower noise. For single-ended connection, MIC1/MIC2 are routed separately and grounded for each; for differential connection, MCP/MICN is routed according to differential coupling and grounded for the entire group.

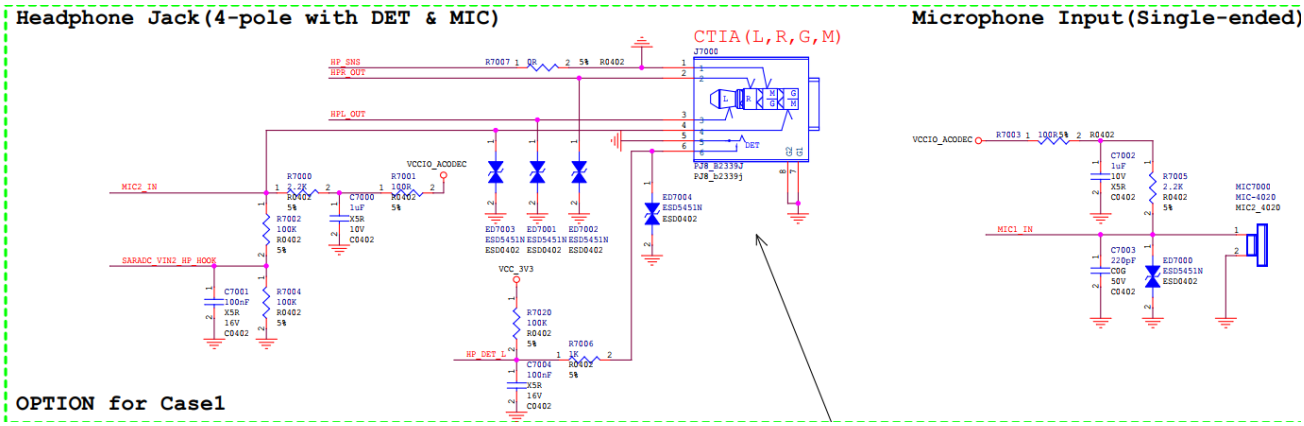


Figure 2-60 RK817-5 external four-segment earphone and single-ended microphone schematic diagram

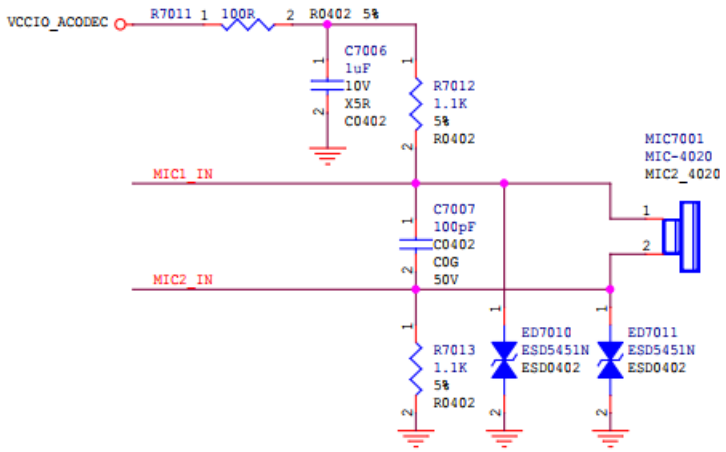


Figure 2-61 RK817-5 external differential microphone schematic diagram

2.4.6.2 Audio Input/Output and Multi-microphone Solution

In the reference design of RK3566, a multi-scene audio input and output solution and a multi-microphone solution are provided. A brief introduction is as follows:

When the integrated ADC of RK817-5 can meet the input requirements, the ADC input of RK817-5 can be used first; when far-field record and loopback are needed, please do not use single-ended ADC connection. The differential input is used by default. If the input interface is insufficient, an external ADC is needed. The current solution uses the audio ADC with the PDM interface as default, or the audio ADC with the I2S interface can also use.

When mono low-power class D power amplifier integrated in RK817-5 can meet the requirements, it can be used first. If you need high power or better output sound quality, it is recommended to expand the analog power amplifier or digital power amplifier. The analog power amplifier can use the HPOUT of RK817-5 as the audio source, and the digital power amplifier can use the I2S interface for external expansion. What needs attention is the power supply design of the power amplifier, when the power is too large, it is recommended to directly boost the power supply from VBAT.

In order to simplify the software design, the audio application scenarios listed in the following table are recommended:

Table 2-25 Correspondence between RK3566 audio application scenarios and drawings

Application scenario	Corresponding to the reference drawing page
Four-segment headset + single-ended microphone + mono small speaker output	70. Case 1 of Audio-HP/1MIC/1SPK
Three-segment earphone + differential microphone + mono small speaker output	70. Case 2 of Audio-HP/1MIC/1SPK
Three-segment headset + differential microphone + mono small speaker output + mono audio loopback	71. Case 3 of Audio-HP/1MIC/1SPK/1LOOP
Three-segment headset + two array microphones + mono small speaker output + mono audio loopback	72. Case 4 of Audio-HP/2MIC/1SPK/1LOOP
Multiple array microphones (up to 6) + stereo analog speaker output + stereo loopback	73.Audio-2SPK/2LOOP(option) and 74.Audio-MicArray(option)
More audio input or output requirements	Contact RK Consulting

2.5 Video Output Interface Design

RK3566 has a built-in VOP video controller, which has three video ports, supports MIPI DSI/eDP/-HDMI/BT656TX/BT1120TX video output modes, and supports up to dual-screen simultaneous display of different/or multiple interfaces.

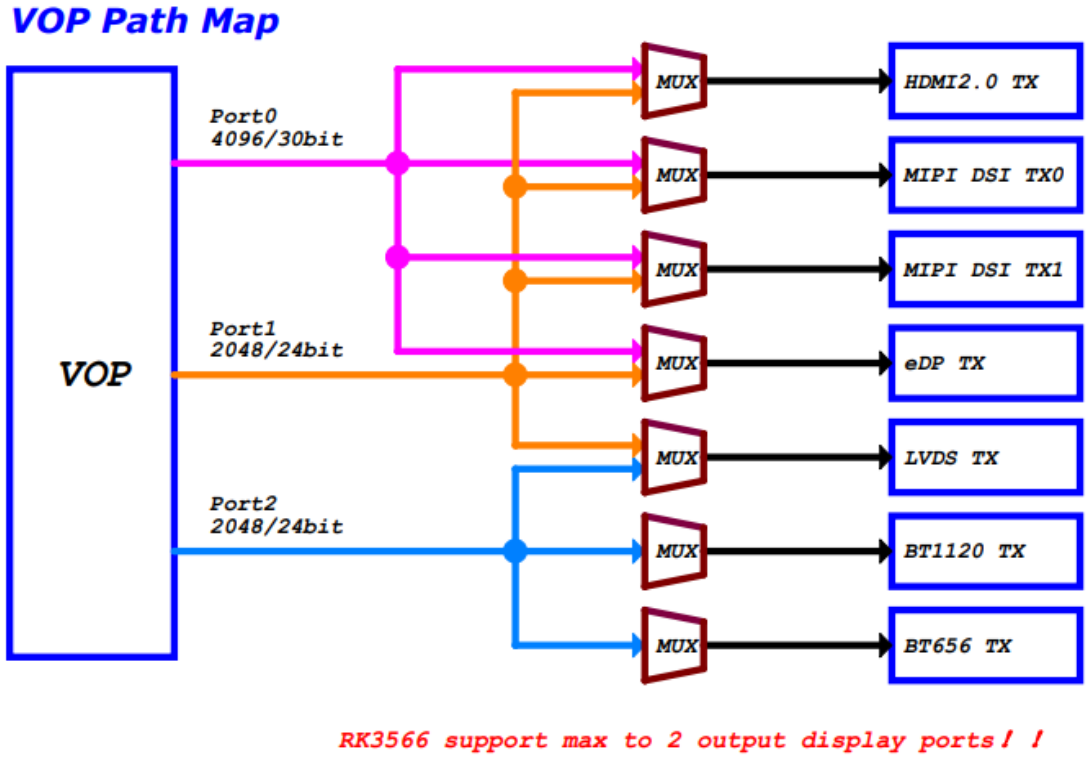


Figure 2-62 RK3566 video output interface path schematic diagram

It should be noted that the RK3566 screen with HDMI dual display has the following limitations:

- HDMI does not support interlaced resolution;
- HDMI will filter out resolutions below 60 frames;
- The direction of the main and secondary screens should be the same, preferably the same ratio; if HDMI is used as a secondary screen, the main screen needs to be horizontal, otherwise HDMI will be severely stretch;
- For more information, refer to the document：*Rockchip Developer Guide HDMI Based on DRM Frame*

2.5.1 MIPI-DSI Output

RK3566 integrates two MIPI-DSI controllers, both with 4lane interface, the rate can reach 2.5Gbps/lane, and the maximum output resolution can reach 1920x1080@60Hz. The relevant signals are shown in the figure:

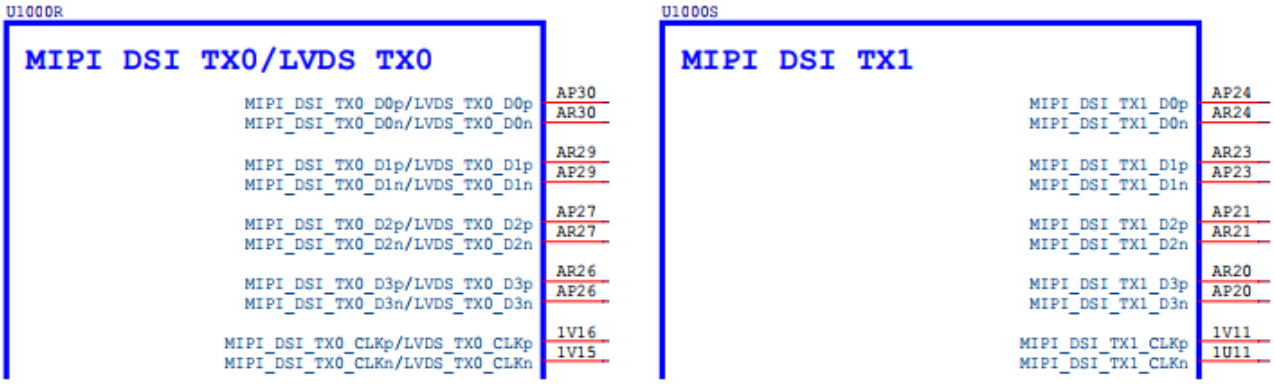


Figure 2-63 RK3566 MIPI-DSI0/DSI1 and LVDS0 interface

In order to improve the performance of MIPI-DSI, please place the decoupling capacitor of the controller power supply close to the pins. The 0.9V/1.8V power supply of the controller needs to be connected in series with magnetic beads.

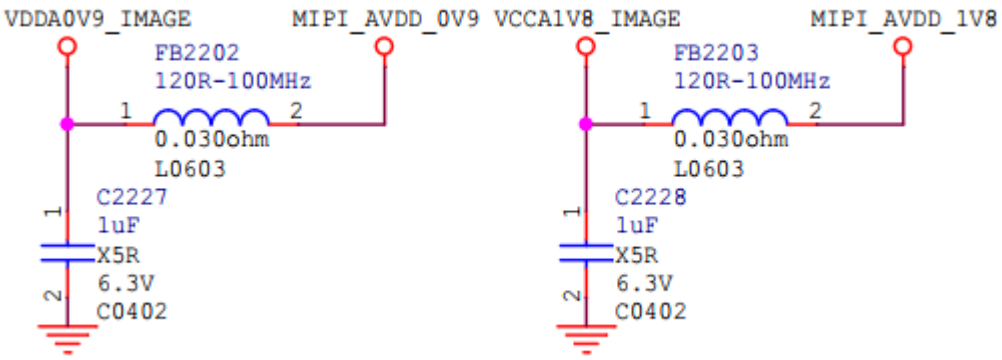


Figure 2-64 RK3566 MIPI-CSI power supply connected with magnetic beads in series

The MIPI-DSI interface impedance and description are as follows:

Table 2-26 RK3566 MIPI-DSI interface design

Signal	Impedance	Description
MIPI_DSI_TX0_DP/DN[3:0]	100ohm±10%	MIPI DSI0 data send
MIPI_DSI_TX0_CLKP/CLKN	100ohm±10%	MIPI DSI0 clock send
MIPI_DSI_TX1_DP/DN[3:0]	100ohm±10%	MIPI DSI1 data send
MIPI_DSI_TX1_CLKP/CLKN	100ohm±10%	MIPI DSI1 clock send

2.5.2 LVDS Output

The MIPI-DSI0 interface mentioned above also multiplexes a group of LVDS signals. RK3566 integrates an LVDS controller, the maximum output resolution can reach 1280x800@60Hz, and it needs to be switched to the corresponding function through software configuration.

Refer to MIPI-DSI section for related filtering processing of power supply pins.

LVDS interface impedance and description are as follows:

Table 2-27 RK3566 LVDS interface design

Signal	Impedance	Description
LVDS_TX0_DP/DN[3:0]	100ohm±10%	LVDS TX0 data send
LVDS_TX0_CLKP/CLKN	100ohm±10%	LVDS TX0 clock send

2.5.3 eDP Output

RK3566 integrates an eDP V1.3 controller that supports rates of 1.62Gbps/lane and 2.7Gbps/lane, supports 1lane, 2lane and 4lane modes, and the maximum output resolution can reach 2560x1600@60Hz. Support AUX channel, the rate can reach 1Mbps.

The 100nF coupling capacitor series connected to the differential signal pair must be placed close to the transmitting end. It is recommended to use the 0201 package to reduce ESR and ESL, and at the same time reduce the impedance mutation of the line.

The relevant signals are shown in the figure:

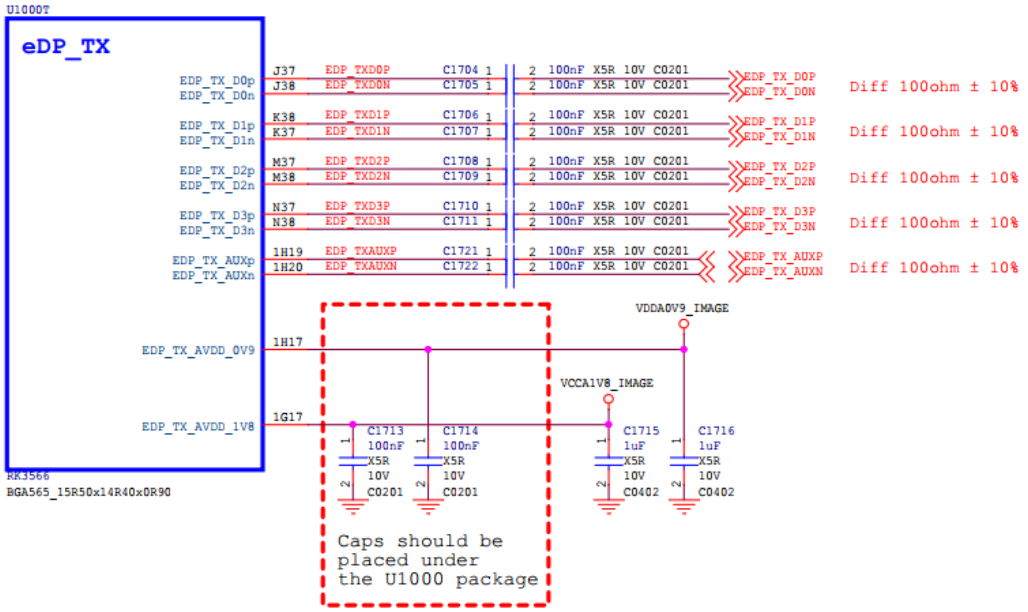


Figure 2-65 RK3566 eDP interface

The impedance and description of the eDP interface are as follows:

Table 2-28 RK3566 eDP interface design

Signal	Impedance	Description
eDP_TX_DP/DN[3:0]	100ohm±10%	eDP TX data transmission, series connected with 100nF capacitor
eDP_TX_AUXP/N	100ohm±10%	eDP TX auxiliary channel, series connected with 100nF capacitor At the socket end of the eDP screen, AUXP reserves 100k pull-down resistor, and AUXN reserves 100k pull-up resistor
eDP_HPDIN	none	eDP TX insertion detection

2.5.4 HDMI2.0 TX Output

RK3566 provides an HDMI output interface, the maximum output resolution can reach 4096x2160@60Hz. The relevant signals are shown in the figure. In design, the differential pair is connected in series with a 2.2ohm resistor to enhance the anti-static surge capability; the common mode inductor is reserved on the CLK signal as a possible measure to deal with EMI:

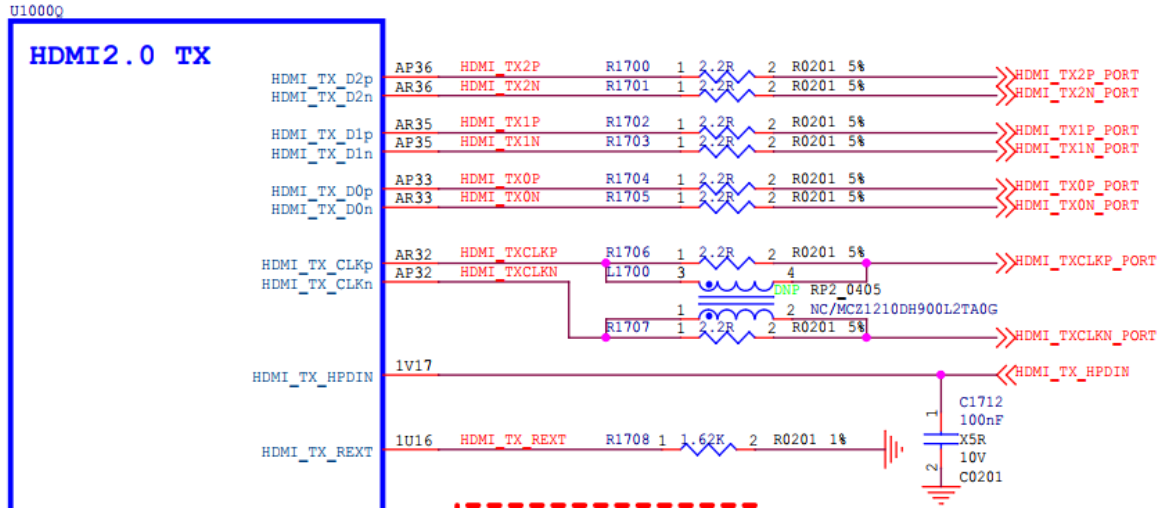


Figure 2-66 RK3566 HDMI interface

Please choose a 1.62k resistor with 1% accuracy as the reference resistor R1708 of the HDMI controller. This resistor will affect the quality of the signal eye diagram. Customers should not change it randomly. The layout must be placed close to RK3566.

HDMI_TX_HPDIN is a built-in function of PHY. It supports 5V level, and the detection effective level range is 2.4-5.3V. It is recommended to place a debounce capacitor on the network near the RK3566 pin. And near the socket side, you need to connect a 1KOhm resistor in series to strengthen the anti-static surge capability, and reserve 100KOhm resistance to ground.

In addition, the CEC circuit of the HDMI interface should pay attention to the anti-backflow isolation design, and the DDC (I2C) circuit should pay attention to the level conversion (the HDMI I2C of RK3566 does not support the 5V level, and the 2SK3018 MOS tube conversion circuit is used by default. The junction capacitance is equivalent), refer to the following picture:

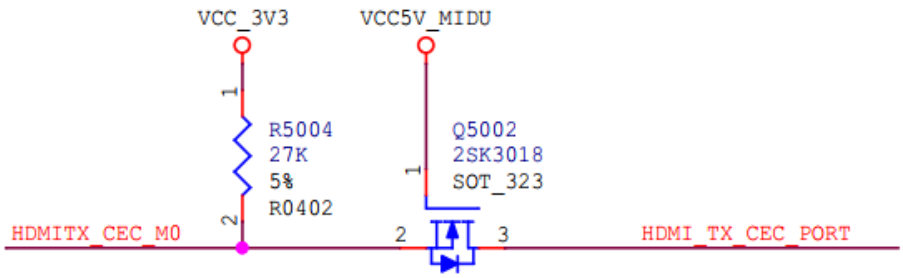


Figure 2-67 RK3566 HDMI CEC anti-backflow circuit

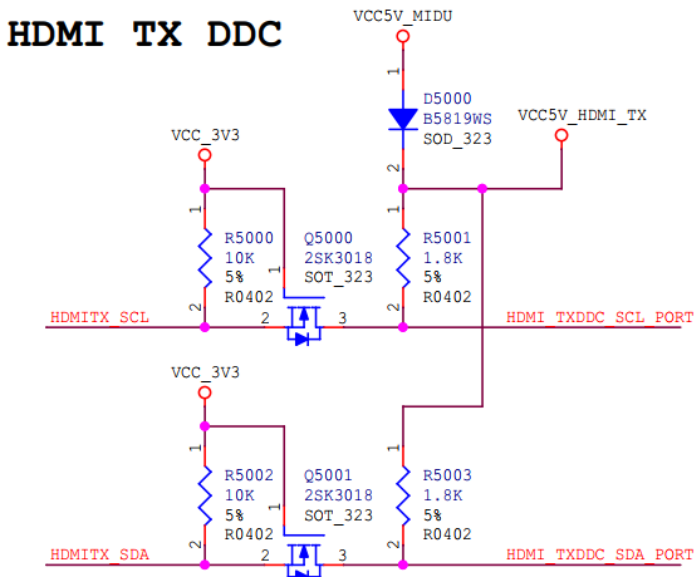


Figure 2-68 RK3566 HDMI I2C level conversion circuit

Both HDMI differential signals and low-speed control signals should be ESD protected. ESD devices should be placed close to the HDMI interface. The recommended capacitance should not exceed 0.4pF (low-speed control signal requirements can be reduced). Considering the cost and other reasons, I2C_SCL, I2C_SDA, CEC, and HPD can also use 4in1 ESD devices.

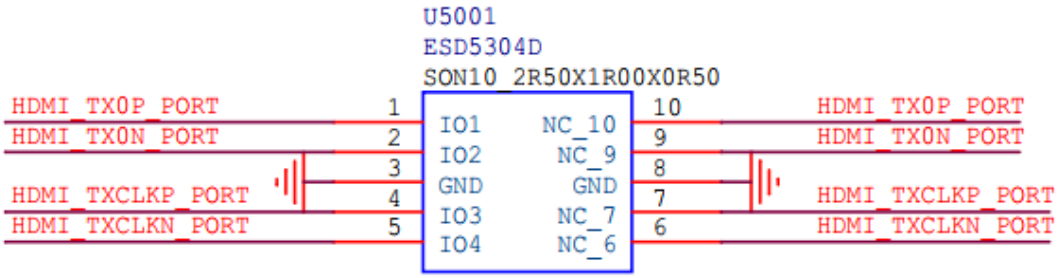


Figure 2-69 RK3566 HDMI signal ESD protection

HDMI interface impedance and description are as follows:

Table 2-29 RK3566 HDMI interface design

Signal	Impedance	Description
HDMI_TX_DP/DN[2:0]	100ohm±10%	HDMI TX data send
HDMI_TX_CLKP/CLKN	100ohm±10%	HDMI TX clock send
HDMI_TX_HPDIN	None	HDMI TX Insertion detection
HDMI_TX_REXT	None	HDMI reference resistor connection pin, default use 1% accuracy 1.62k resistor
HDMITX_SCL/SDA	None	HDMI data communication channel
HDMITX_CEC	None	HDMI consumer electronics control pin

2.5.5 BT1120 Output

RK3566 supports BT1120 format output, and the maximum output resolution can reach 1920x1080@60Hz. The corresponding pin belongs to the VCCIO5 power domain, and the signal description is as follows.

Table 2-30 RK3566 BT1120 output signal description

Signal	Internal pull up/down	Connection Method	Description (chip side)
VOP_BT1120_D[15:0]	pull down	Direct connection	BT1120 data output
VOP_BT1120_CLK	pull down	Series connect 22ohm resistor	BT1120 clock output

2.5.6 BT656 Output

RK3566 supports BT656 format output, and the corresponding pin belongs to the VCCIO6 power domain. The signal description is as follows.

Table 2-31 RK3566 BT656 output signal description

Signal	Internal pull up/down	Connection Method	Description (chip side)
VOP_BT656_D[7:0]	pull down	Direct connection	BT656 data output
VOP_BT656_CLK	pull down	Series connect 22ohm resistor	BT656 clock output

2.5.7 EBC Output

RK3566 supports EBC output and can drive electronic ink screens. The corresponding pins belong to the VCCIO6 power domain. The signal descriptions are as follows.

For e-paper and ink e-book products, refer to the special reference diagram *RK3566_EINK_REF* released by RK.

Table 2-32 RK3566 EBC output signal description

Signal	Internal Pull up/down	Connection Method	Description (chip side)
EBC_SDDO[15:0]	pull down	Direct connection	Source driver data
EBC_SDCE[3:0]	pull down	Direct connection	Source start pulse
EBC_VCOM	pull down	Direct connection	VCOM power enable
EBC_GDOE	pull down	Direct connection	Gate start pulse
EBC_GDSP	pull down	Direct connection	Gate output enable
EBC_SDSHR	pull down	Direct connection	Source drive shift register
EBC_SDLE	pull down	Direct connection	Source latch enable
EBC_SDOE	pull down	Direct connection	Source output enable
EBC_GDCLK	pull down	Direct connection	Gate drive clock
EBC_SDCLK	pull down	Direct connection	Source drive clock

2.5.8 Design Attention to LCD Screen and Touch Screen

- Please choose a resistor with 1% accuracy for FB end limiting resistor of LED backlight boost IC, and choose an appropriate package size according to power requirements.
- For the EN/PWM pin of LED backlight boost IC, select the internal pull-down GPIO, and an external

pull-down resistor to avoid flickering when powering on.

- For LED backlight drive voltage output, please select a filter capacitor with a suitable rated voltage.
- For the Schottky diode of the LED backlight boost circuit, please select the appropriate model according to the working current, and pay attention to the reverse breakdown voltage of the diode to avoid reverse breakdown when there is no load.
- Please match the inductance, saturation current, DCR, etc. of the LED backlight boost circuit according to the actual model.
- The signal level of the screen and touch screen must match the IO drive level of the chip, such as RST/Stand by signals.
- The power supply of the screen must be controllable, and it is not provided by default when it is powered on.
- The decoupling capacitance of the screen and touch screen shall not be deleted and must be retained.
- The I2C bus pull-up of TP needs to consider the leakage problem. It is recommended not to share the bus with other devices. If it must be shared, pay attention to whether the pull-up power supply and address conflicts.
- For TP IC with charge pump, please pay attention to the rated voltage of the capacitor.
- For the screen, when connecting to the board through FPC, it is recommended to connect a resistor in series (between 22ohm-100ohm, the specific can meet the SI test shall prevail), and reserve TVS devices.
- It is recommended to reserve a common mode inductor at the interface of the serial interface screen.

2.6 Video Input Interface Design

2.6.1 MIPI-CSI Interface

RK3566 has a built-in ISP processor, two sets of MIPI-CSI inputs, supports MIPI V1.2 version, a total of 4 lanes, and two pairs of clocks.

The differential interface inputs two sets of differential clock signals and four sets of differential data signals, and supports 2lane MIPI RX and 4lane MIPI RX input modes. The relevant signals are shown in the figure:

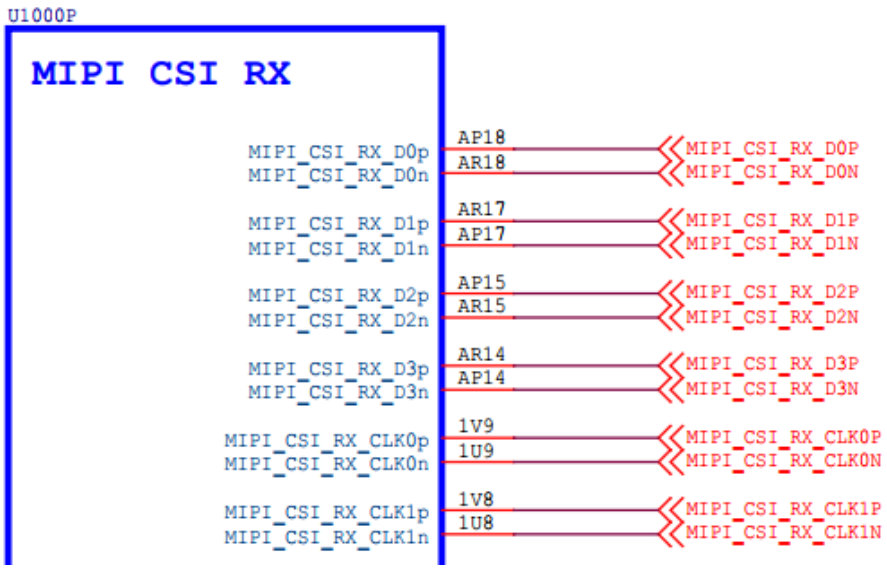


Figure 2-70 RK3566 MIPI-CSI module

The configuration of 2lane or 4lane mode is as follows. When 4lane mode is used, MIPI_CSI_RX_D[3:0] data signal refers to CLK0 clock; when 2lane mode is used, supports two camera inputs, and MIPI_CSI_RX_D[1:0] data signal refers to CLK0 Clock, MIPI_CSI_RX_D[3:2] data signal refers to CLK1 clock.

The camera's MCLK can be obtained from the following clock outputs of RK3566: CAM_CLKOUT0, CAM_CLKOUT1, CIF_CLKOUT, REFCLK_OUT. Need to pay attention to whether the corresponding IO level is consistent with the camera IO.

When two cameras are used, the power supply of the cameras can be separated or combined according to the actual situation. In addition, you should also check whether the I2C addresses are different. If the addresses are the same, you should also connect to two independent I2C controllers.

Usage of MIPI CSI Dx&CLKs		
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Figure 2-71 RK3566 MIPI-CSI working mode and data/clock distribution

In order to improve the performance of MIPI-CSI, please place the decoupling capacitor of the controller power supply close to the pins. The 0.9V/1.8V power supply of the controller needs to be connected in series with magnetic beads.

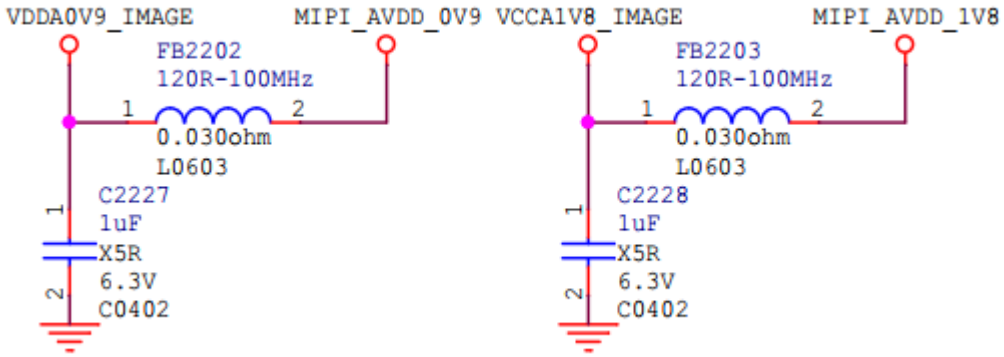


Figure 2-72 RK3566 MIPI-CSI power supply connected with magnetic beads in series

The reference design also provides a dual-camera solution that uses MIPI switches. This solution supports 4lane+2lane connections, that is, meet the high-resolution and medium(low)-resolution camera combination. It should be noted that, in order to ensure that the delays of all data signals and clocks are consistent, each group of signals should be input through the switch.

MIPI-CSI interface impedance and description are as follows:

Table 2-33 RK3566 MIPI-CSI interface design

Signal	Impedance	Description
MIPI_CSI_RX_DP/DN[3:0]	100ohm±10%	MIPI CSI0 data receive
MIPI_CSI_RX_CLK0P/N	100ohm±10%	MIPI 4lane mode clock Or 2lane mode clock 0
MIPI_CSI_RX_CLK1P/N	100ohm±10%	MIPI 2lane mode clock 1

2.6.2 DVP (CIF) Parallel Port Camera Input

There is a group of VICAP controller in RK3566, and the function pins of VICAP controller are named CIF_D[15:0], CIF_HSYNC, CIF_VSYNC, CIF_CLKOUT, CIF_CLKIN.

The VICAP pin is multiplexed in the VCCIO6 power domain. In the actual product design, you need to select the corresponding power supply according to the actual IO power supply requirements (1.8V or 3.3V) of the Camera. At the same time, the I2C pull-up level must be consistent with it, otherwise it will Cause the Camera to work abnormally or fail.

The parallel port VICAP controller interface supports the following formats:

- BT601RX YCbYr 422 8bit；
- BT656RX YCbYr 422 8bit；
- RAW Data 8/10/12bit；
- BT1120RX YCbCr 422 8/16bit，single/dual-edge sampling；
- 2/4 mixed BT656/BT1120 YCbCr 422 8bit；

The interface rate can reach 148.5MHz. Note:

- When the connected signal is in RAWData format, the connection should be aligned from the high bit of VICAP, such as 12bit RAWData corresponding to CIF_D[15:4] from the high position;
- When the connected signal is BT1120 RX, the low 8bit data is connected to Y by default, and the high 8bit data is connected to UV. Only internal synchronization is supported. Or use YC SWAP mode, as shown in the figure below;
- When the connected signal is BT656 or BT601, connect in order from the high bit of VICAP;
- CIF_CLKOUT outputs the Clock signal to the peripheral;
- CIF_CLKIN receives the Clock signal from the peripheral;
- The DVDD current needs of some cameras are relatively large, and it is recommended to use DC/DC power supply;

Corresponding relationships are organized as follows:

Usage of CIF Interface				
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Figure 2-73 RK3566 DVP (CIF) parallel port camera signal correspondence table

DVP (CIF) interface pull-up/down and matching design recommendations are shown in the table:

Table 2-34 RK3566 DVP (CIF) interface design

Signal	Internal Pull up/down	Connection Method	Description (chip side)
CIF_D[15:0]	pull down	Direct connection	DVP data input
CIF_HREF	pull down	Direct connection	DVP line sync signal
CIF_VSYNC	pull down	Direct connection	DVP field sync signal
CIF_CLKOUT	pull down	connect 22ohm resistor in series place close RK3566	DVP clock output
CIF_CLKIN	pull down	connect 22ohm resistor in series	DVP clock input

2.7 Combined High-Speed Interface Design（MULTI PHY）

RK3566 provides two sets of MULTI PHY, which can configured as USB3.0, SATA3.0, PCIE2.0 interfaces, the path diagram is as follows, the possible combinations are:

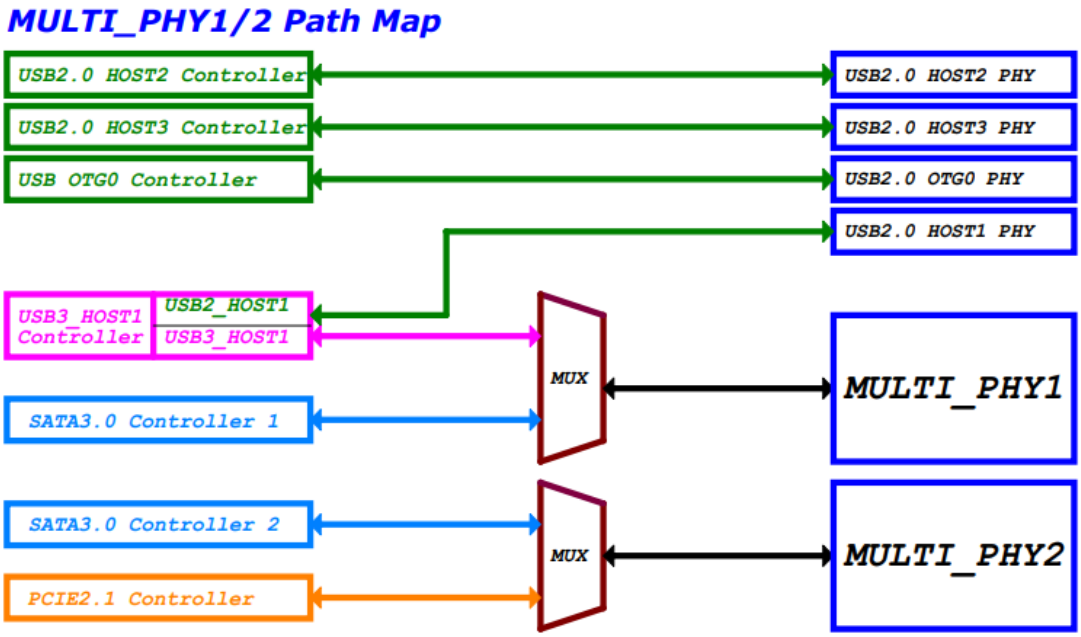


Figure 2-74 RK3566 MULTI PHY path topology diagram

Table 2-35 RK3566 MULTI PHY configuration table

Scenes	MULTI PHY U_S	MULTI PHY P_S
1	USB3.0	PCIE2.0
2	USB3.0	SATA3.0_2
3	SATA3.0_1	PCIE2.0
4	SATA3.0_1	SATA3.0_2

The MULTI_PHY controller of RK3566 has two sets of power supplies, which are analog power MULTI_PHY_AVDD_0V9 and MULTI_PHY_AVDD_1V8; the recommended power-on sequence is MULTI_PHY_AVDD_0V9 first.

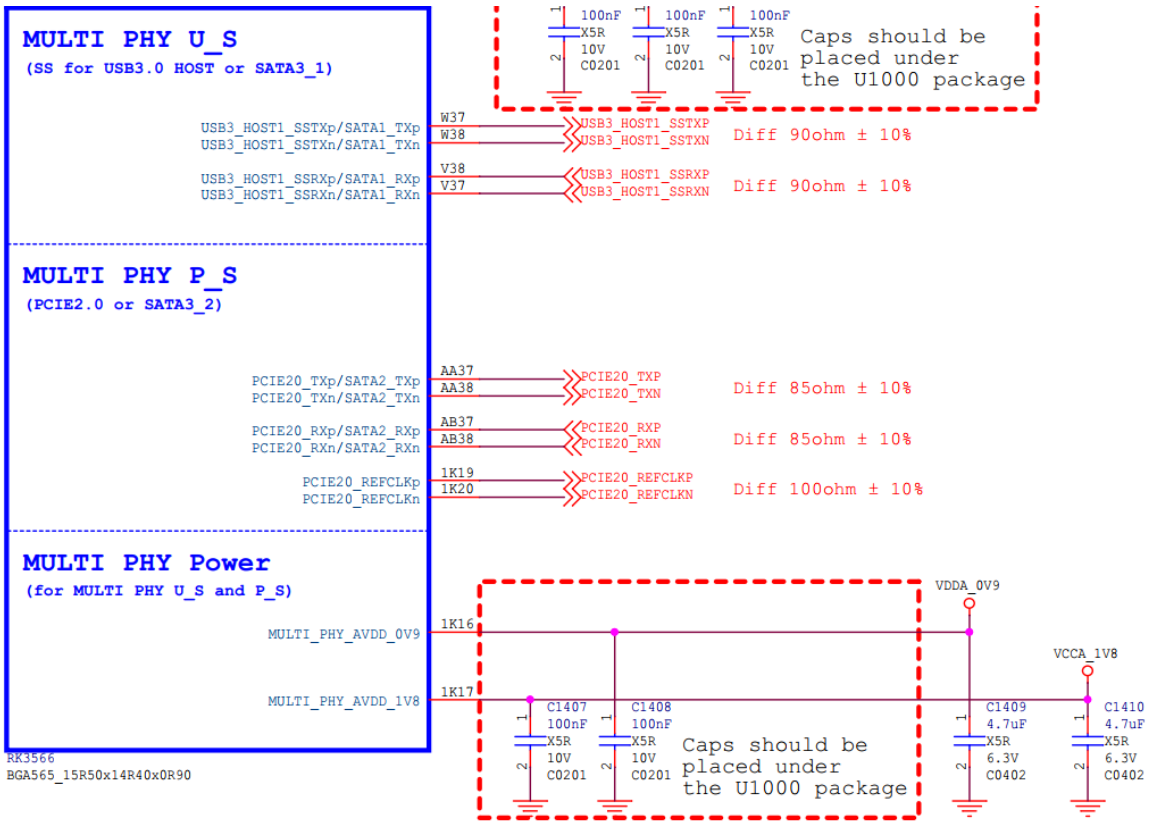


Figure 2-75 RK3566 MULTI PHY signal and power

The USB3.0 high-speed interface has been described above, and only SATA3.0 and PCIE2.0 high-speed interfaces are introduced here.

2.7.1 SATA3.0 High Speed Interface

SATA is the abbreviation of Serial Advanced Technology Attachment, which is a serial communication hard disk interface. RK3566 supports SATA V3.0 protocol and has the following features:

- Compatible with Gen1/Gen2/Gen3;
- A single data channel can support a maximum signal transmission rate of 6GT/s;
- Support OOB;
- Support SATA PM function, can be connected with external expansion chip;
- Support spread spectrum function;

SATA interface impedance and description are as follows:

Table 2-36 RK3566 SATA interface design

Signal	Impedance	Description
SATAx_TXP/N	90ohm±10%	SATA data send, place the coupling capacitor 10nF closed to the mainboard connector
SATAx_RXP/N	90ohm±10%	SATA data receive, place the coupling capacitor 10nF closed to the mainboard connector

2.7.2 PCIe 2.0 High Speed Interface

PCIe is the abbreviation of PCI-Express. RK3566 supports PCIe V2.1 protocol and has the following features:

- Compatible with Gen1/Gen2;
- Only supports Root Complex (RC) working mode;
- Support x1 mode, with 1 pair of TX/RX differential signal pair;
- A single data channel can support a maximum signal transmission rate of 5GT/s, and use 8b/10b encoding;
- Full duplex mode;
- Support spread spectrum function;

The PCIe interface impedance and description are as follows:

Table 2-37 RK3566 PCIe interface design

Signal	Impedance	Description
PCIe20_TXP/N	85ohm±10%	PCIe2.0 data send, place the coupling capacitor 100nF closed to the sending end or the mainboard connector
PCIe20_RXP/N	85ohm±10%	PCIe2.0 data reception, the coupling capacitor is located on the device side
PCIe20_REFCLKP/N	100ohm±10%	The reference clock of PCIe2.0, supports input and output. The default is output to provide clock for EP devices

In the design of PCIe 2.0, need to pay attention to:

- Note the power supply requirements of PCIe peripherals, especially in the slot design, fully consider the possible peripheral conditions;
- For the 100nF AC coupling capacitor connected with PCIe TX/RX differential signal in series, it is recommended to use 0201 package to reduce ESR and ESL, at the same time reduce the impedance mutation of the circuit;
- PCIE20_CLKREQn and PCIE20_WAKEn must use specific function pins and cannot be replaced by other IO; and they must be in the same group of MUX, that is, the same _Mx suffix;
- PCIE20_PERSTn can use function pins or GPIO. When selecting function pins, they must be in the same group of MUX as PCIE20_CLKREQn and PCIE20_WAKEn, that is, the same _Mx suffix;
- For standard PCIe Slot, PCIE20_PERSTn, PCIE20_CLKREQn and PCIE20_WAKEn are all 3.3V levels;
- PCIE20_PRSNT is the insertion detection pin of Add In Card, which can be realized by GPIO;

3 Thermal Design Recommendation

3.1 Thermal Simulation Result

For the RK3566 FCCSP 565ball package, based on the 4-layer PCB using Finite Element Modeling (FEM), a simulation report of thermal resistance can be obtained. The report is based on the JEDEC JESD51-2 standard. The system design and environment during application may be different from the JEDEC JESD51-2 standard, and it needs to be analyzed according to the application conditions.

Note

Thermal resistance is the reference value which is get under the condition that the PCB has no heat removal measures. The specific temperature is related to the board design, size, thickness, material and other physical factors.

3.1.1 Result Summaries

The thermal resistance simulation results are shown as below, these properties are typical values, and the terminology is explained in section 3.1.3:

Table 3-1 RK3566 thermal resistance simulation results

Package	$\boldsymbol{\theta}_{JA}$(℃/W)	$\boldsymbol{\theta}_{JB}$(℃/W)	$\boldsymbol{\theta}_{JC}$(℃/W)
FCCSP 565ball	20.728	17.74	1.544

3.1.2 PCB Information

The PCB structure for thermal resistance simulation is as follows:

Table 3-2 PCB structure of RK3566 thermal resistance simulation

Dimension（L x W）	PCB Thickness	Number of Cu Layer
114.3 x 101.6mm	1.6mm	4-layers

3.1.3 Terminology

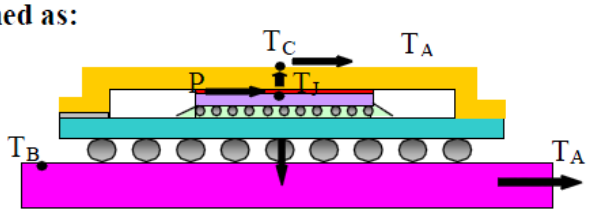
The terminologies in this chapter are explained as below:

- T_J: Average junction temperature (℃);
- T_A: The ambient or environment temperature (℃);
- T_C: The compound surface temperature (℃);
- T_B: The surface temperature of PCB (℃);
- P: Total input power (W);
- $\boldsymbol{\theta}_{JA}$: The thermal resistance from junction to ambient (℃/W);
- $\boldsymbol{\theta}_{JC}$: The thermal resistance from junction to case (℃/W);
- $\boldsymbol{\theta}_{JB}$: The thermal resistance from junction to PCB board (℃/W);

The thermal parameter can be define as following

1. *Junction to ambient thermal resistance,* θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$

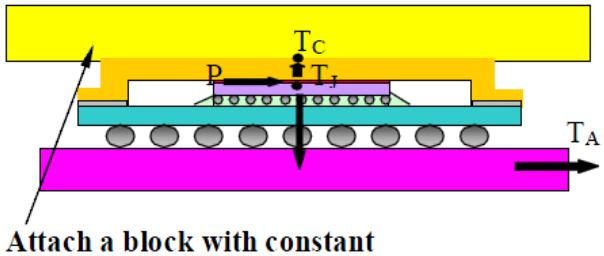


Thermal Dissipation of EHS-FCBGA

Figure 3-1 Definition of $\boldsymbol{\theta}_{JA}$

2. *Junction to case thermal resistance,* θ_{JC}**, defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad ; \qquad (2)$$

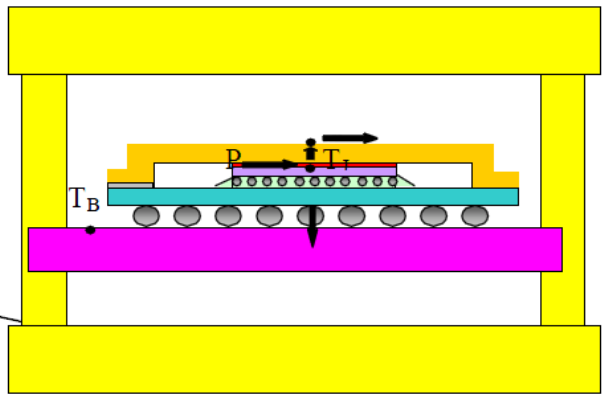


Attach a block with constant temperature onto package.

Figure 3-2 Definition of $\boldsymbol{\theta}_{JC}$

3. *Junction to board thermal resistance,* θ_{JB}**, defined as:**

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad ; \qquad (3)$$



Attach a block with constant temperature

Figure 3-3 Definition of $\boldsymbol{\theta}_{JB}$

3.2 Inner SOC Thermal Control Method

3.2.1 Thermal Control Strategy

In the Linux kernel, a set of temperature control framework “Linux Generic Thermal System Drivers” is defined, which can adjust the system temperature via different strategies. Below are 3 common strategies:

- Power_allocator: use the PID (proportional, integral, differential) control method, dynamically allocate power for modules according to current temperature, and convert power into frequency parameters, so as to achieve the effect of limiting the frequency according to the temperature;
- Step_wise: limit the frequency step by step according to current temperature;
- Userspace: not to limit the frequency;

There is a T-sensor inside the RK3566 to detect the on-chip temperature, and the Power_allocator strategy is used by default. The working status is divided into the following situations:

- When the temperature exceeds the setting value:
  - Reduce the maximum allowed frequency if the trend of temperature is upward;
  - Raise the maximum allowed frequency if the trend of temperature is downward;
- When the temperature is below the setting value:
  - The maximum allowed frequency is setting value(default value), not be controlled by the thermal strategy;
- After frequency reduction, if the chip is still overheated (such as poor heat dissipation) , then the software will trigger a restart if it exceeds a certain temperature (settable). If the restart fails due to deadlock or other factors, and the chip exceeds the set shutdown protection temperature line (settable), it will trigger the inner TSADC_SHUT action to directly shut down the PMIC.

Note

The temperature trend is obtained by comparing the sequentially sampled two temperatures. When the device temperature does not exceed the threshold, the temperature is sampled every 1 second; when the device temperature exceeds the threshold, the temperature is sampled every 20ms and the frequency is limited.

3.2.2 Thermal Control Configuration

RK3566 SDK provides temperature control strategies for CPU, GPU and NPU respectively. Please refer to *Rockchip Thermal Development Guide* for specific configuration.

3.3 Suggestions for Thermal Design of Circuits and PCB Layout

- Reasonable device layout to avoid local overheating: For example, make a reasonable placement of RK3566 and RK PMIC, balance power supply and heat dissipation constraints. It is recommended to place them at an interval of 20mm-50mm to ensure the quality of power supply and heat dissipation.
- In an open area, add as many vias as possible without damaging the integrity of the power supply plane to increase the heat dissipation path.
- Pay attention to the input and output voltage difference of the LDO. Improve the overall efficiency of the power supply and reduce the heat caused by its own dissipation.
- When the circuit module is not in use, it can be powered off or configured to enter low power consumption modes such as power mode.
- For the traces/copper with high current power supply, the current-carrying capacity should be considered to avoid excessive temperature rise caused by too small trace width.

- If conditions permit, it is recommended to use a multi-layer board design, increase the copper content of the board (for example, use a copper thickness of 1oz), increase the number and area of the ground plane, and use a large area of copper for heat dissipation.
- Chips with E-PAD or P-PAD usually dissipate high power, and it is necessary to fill the PAD with via holes, and the adjacent layer is treated as a complete ground plane, and the back copper is kept intact and exposed to bare copper to ensure the heat dissipation effect.
- The GND pins of the RK3566 are cross-connected in a "#" shape on the top layer, and the line width is 10 mils to ensure the heat dissipation capacity of the chip.
- For the GND pin of the RK3566, ensure that each pin has a corresponding ground via (in the worst case, ensure that each 1.5 ball share a via), and the adjacent layer is treated as a ground plane to ensure sufficient heat conduction path .
- Avoid using flower hole connections for the decoupling capacitor ground pads on the bottom side of the RK3566. Try to use full copper to ensure the integrity of the copper and improve the heat dissipation capacity.
- Carry out reasonable structural design, consider the reasonable heat exchange path between the inside and outside of the product; when using heat sinks, pay attention to the direction of the fins in line with the structural air duct, use sufficient size heat sinks and heat dissipation materials with high thermal conductivity .

4 ESD/EMI Protection Design

4.1 Overview

This chapter gives suggestions on the ESD/EMI protection in the RK3566 product design to help customers improve the product's anti-static and anti-electromagnetic interference level.

4.2 Terminology Explain

The terms in this chapter are explained as follows:

- ESD (Electro-Static discharge): electrostatic discharge;
- EMI (Electromagnetic Interference): electromagnetic interference, including conducted interference and radiated interference;

4.3 Suggestions for ESD Protection

- It is recommended to use a surface-mounted 4-Pin crystal, and the two GND pins must be well connected to the ground plane of the PCB board to enhance the anti-interference ability of the system clock.
- The distance between key signals (such as RESET, clock, interrupt, etc.), sensitive signals, etc., and the edge of the board shall not be less than 5mm.
- For RK3566, RK PMIC and other chips with reset input pins, a 100nF capacitor must be placed close to the RESET (or NPOR) pin, and the ground pad of the capacitor must have a 0402 ground via or more, to ensure a good grounding.
- If the signal passes through the board-level connector, it is recommended to connect a certain resistance resistor (between 2.2ohm-22ohm, which can meet the signal integrity test) in series, and reserve TVS devices to improve anti-static and surge capabilities.
- TVS devices must be reserved for interfaces, ports, and connectors and placed reasonably. Generally, they are required to be placed at the source, that is, TVS devices are placed closed to the interfaces or where the electrostatic discharge path is located. When routing, the signal must not change layers, and there must be no routing branches. The possible static electricity path must first pass through the TVS pin pads and then connect to the subsequent devices. The ground pad of the TVS tube should have at least two 0402 ground vias to ensure a good discharge path.
- For PCB layout, there are the following suggestions:
  - Protect and isolate sensitive components during PCB layout. For example, the minimum system (such as the main chip, DDR), key components and other circuit parts are far away from the metal interface.
  - Place the main chip and core components in the middle of the PCB as much as possible during the layout. If they cannot be placed in the middle of the PCB, ensure that the shielding cover is at least 2mm away from the edge of the board, and the shielding cover must be reliably grounded.
  - Layout the PCB according to functional modules and signal flow. It is best to isolate the part that is easy to produce interference, make each sensitive part independent of each other, and keep sensitive signals away from electrostatic discharge areas (surface copper). For example, the interface ground pin is connected to the inner layer ground through the ground vias alone, and make surface layout layer a "keepout" to keep the surface copper far away from the pin.

- The component layout is far away from the edge of the board and a certain distance from the metal connector.
- When designing the PCB, ensure a good internal and external ground loop to ensure the smoothness of the electrostatic loop, and avoid the large difference of potential when static electricity enters and cause system control abnormalities.

- The PCB surface layer must have a good GND plane to ensure that the connectors have a good GND loop on the surface layer. Make more ground vias around the interface device to enhance the effect of electrostatic discharge; copper can be appropriately exposed around the interface device to facilitate improvement measures such as adding foam.
- Reserve the shielding cover position. The shielding cover should be well connected to the surface ground, and more ground vias should be drilled at the welding place of the shielding cover.
- Do not run wires on the edge of the surface board and punch more ground vias.
- If necessary, isolate the signal from the ground.
- To ensure a reasonable mold design, the connector should be retracted into the shell as much as possible, so that the distance between the static electricity to the internal circuit is long enough and the energy is weakened.
- Use the absorption capacity of the components, such as connecting the heat sink to the main ground, and using a large area of metal to absorb part of the ESD energy, and protect the chip by changing the ESD transmission path.
- When designing the whole machine, consider the reasonable copper opening of the PCB board, and connect to conductive structural parts to enhance the effect of electrostatic discharge.
- When the whole machine is designed as a floating device, it is recommended not to separate the ground for each interface to avoid deterioration of ESD protection. Unless there is sufficient argumentation and testing.
- When the whole machine is a metal casing, the casing must be well connected to the ground.
- During the production process, avoid direct human contact with any components or circuits in the PCB board, and do not plug or unplug the interface when powered.

4.4 Suggestions for EMI Protection

- Three elements of electromagnetic interference: interference source, coupling channel and sensitive equipment. Among them, the elements that can be processed are the interference source and the coupling channel. The best way to solve the EMI problem is to eliminate the interference source. If it can't be eliminated, try to cut off the coupling channel or avoid the antenna effect.
- The interference sources on the PCB can be dealt with by filtering, grounding, balancing, impedance control, and improving signal quality (such as termination). Various methods are generally used comprehensively, but good grounding is the most basic requirement.
  - The RC circuit between DDR3/DDR4/LPDDR3 CLKP/N must not be deleted, which can be used as a measure to improve EMI;
  - Common mode inductors or filter circuits are reserved at the ports of USB, HDMI, VGA, and screen connector;
  - The matching resistors of all clocks connected in series must be close to the CPU side(source side), and the wiring between the CPU pins and the resistor must be controlled within 400mil;

- If the PCB exceeds 4 layers, try to route all clock signals in the inner layers;
- At the input of DC power supply, a power supply common mode inductor or EMI filter can be reserved;
- To prevent power source radiation, the copper layer on the power supply layer must be indented, with a unit of H (H is the thickness of the medium between the power layer and the ground layer), and it is recommended to indent by 20H;
- Filter selection principle: If the load (receiver) is high impedance (generally single-ended signal interfaces are high impedance, such as SDIO, RGB, CIF, etc.), then select a capacitive filter in parallel; if the load (receiver) is low impedance (such as power output interface), select an inductive filter in serial. After using the filter device, the signal quality cannot exceed its SI (signal integrity) allowable range. Differential interfaces generally use common mode inductors to suppress EMI.

- Commonly used materials to deal with EMI include shielding covers, special filters, resistors, capacitors, inductors, magnetic beads, common-mode inductors/magnetic rings, wave-absorbing materials, frequency-spreading devices, etc.
- The shielding measures on the PCB must be well grounded, otherwise it may cause radiation leakage or the shielding measures may form an antenna effect, and the shielding of the connector must comply with relevant technical standards. Key areas such as RK3566, DDR, etc. need to reserve the position of the shielding cover, and ensure a good grounding.
- The use of the spread spectrum function of the core device and the degree of spread spectrum shall be determined according to the signal requirements of the relevant parts. If the requirements are met, and the frequency and source of the radiated interference can be determined, the radiated energy can be reduced by spreading the relevant clock. From the perspective of signal quality, the smaller the spread, the better.
- EMI and ESD have a high degree of consistency in the LAYOUT requirements. Most of the aforementioned ESD LAYOUT requirements are suitable for EMI protection. In addition, add the following requirements;
  - Try to ensure signal integrity and power integrity;
  - Differential lines should be equal in length and tightly coupled to ensure the symmetry of the differential signal to minimize the misalignment of the differential signal and the clock and avoid EMI problems caused by phase mismatch;
  - Components with metal shell devices such as plug-in electrolytic capacitors should avoid coupling interference signals and radiate it out. It is also necessary to prevent the interference signal of the device from coupling to other signal lines from the metal shell.
- For designs with radiators, attention should be paid to the possibility of radiators coupling EMI energy and generating radiation. Therefore, thermal design requirements must be met when selecting radiators, and EMI requirements should also be considered. The radiator can reserve grounding conditions and deal with it according to the actual test of the first version.

5 Welding Process

5.1 Overview

RK3566 are RoHS directive certified products, that is, they are all lead-free products. This chapter regulates the basic temperature settings for each time period when using RK3566 SMT (Surface Mounted Technology), and introduces the process control when using RK3566 SMT reflow soldering: mainly lead-free process and mixed process.

5.2 Terminology Explain

The terms in this chapter are explained as follows:

- Lead-free: Lead-free process;
- Pb-free: Pure Lead-free process, all devices (mainboard, all ICs, resistors and capacitors, etc.) are lead-free devices, and using lead-free solder paste;
- Reflow Profile: reflow soldering;
- Restriction of Hazardous Substances (RoHS): Directives on restricting the use of certain hazardous components in electronic and electrical equipment;
- Sn-Pb: tin-lead mixing process, refers to the process of using leaded solder paste to mix lead-containing IC and lead-free IC;

5.3 Reflow Solder Requirement

5.3.1 Solder Paste Composition and Operation Requirement

The proportion of Solder alloy to flux is 90%: 10%; the volume ratio is 50%: 50%. The solder paste refrigeration temperature is 2~10℃. Before use, it should be warmed up at room temperature, and the warming time should be 3~4 hours and record the time.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes, after stirring, it becomes a natural vertical flow.

5.3.2 SMT Re-flow Profile

Since RK3566 chips are made of environmentally friendly materials, it is recommended to use Pb-Free technology.

The reflow curve in the figure below is only the recommended value for JEDEC J-STD-020D process requirements, and the client needs to adjust it according to the actual production situation.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Figure 5-1 Classification of Reflow Soldering Curves

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 5-2 Heat Resistance Standard of Lead-free Process Device Package

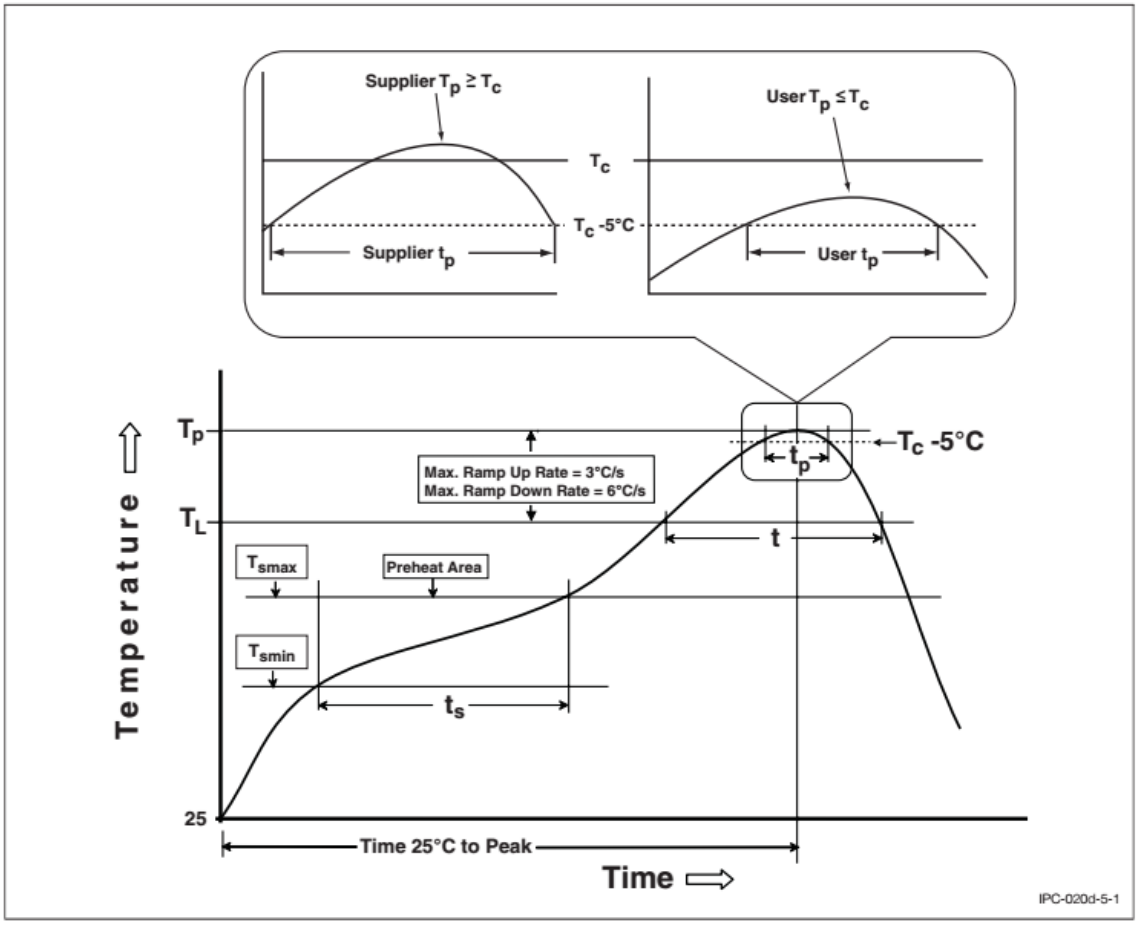


Figure 5-3 Lead-free Reflow Soldering Process Curve

5.3.3 Recommended SMT Re-flow Profile

The recommended SMT curve parameters are shown in the following table, refer to the solder paste SAC305, customers can adjust according to the actual situation:

Table 5-1 SMT Curve Parameters

Item	Time（s）	Temperature（℃）
Temperature Rise Slope		≤ 3℃/s
Constant Temperature（150-180℃）	60-90	
Reflow (time above 220℃)	60-70	
Peak Temperature		245±5℃
Peak Time	15-30	
Cooling Slope		≤ 3℃/s

6 Packaging and Storage Condition

6.1 Overview

This chapter stipulates the storage and use specifications of RK3566, to ensure the safe and correct use of the product.

6.2 Terminology Explain

The terms in this chapter are explained as follows:

- Desiccant: A material used to absorb moisture;
- Floor Life: Workshop time, which refers to the maximum time the product is allowed to be exposed to the environment (from unpacking the moisture-proof package to reflow soldering);
- HIC: Humidity Indicator Card;
- MSL: Moisture Sensitivity Level;
- MBB: Moisture Barrier Bag;
- Shell Life: storage period;

6.3 Dry Vacuum Packaging

The dry vacuum packaging materials of the product are as follows:

- Desiccant;
- Six-point humidity card;
- Moisture-proof bag, aluminum foil, silver opaque with moisture sensitivity level logo;

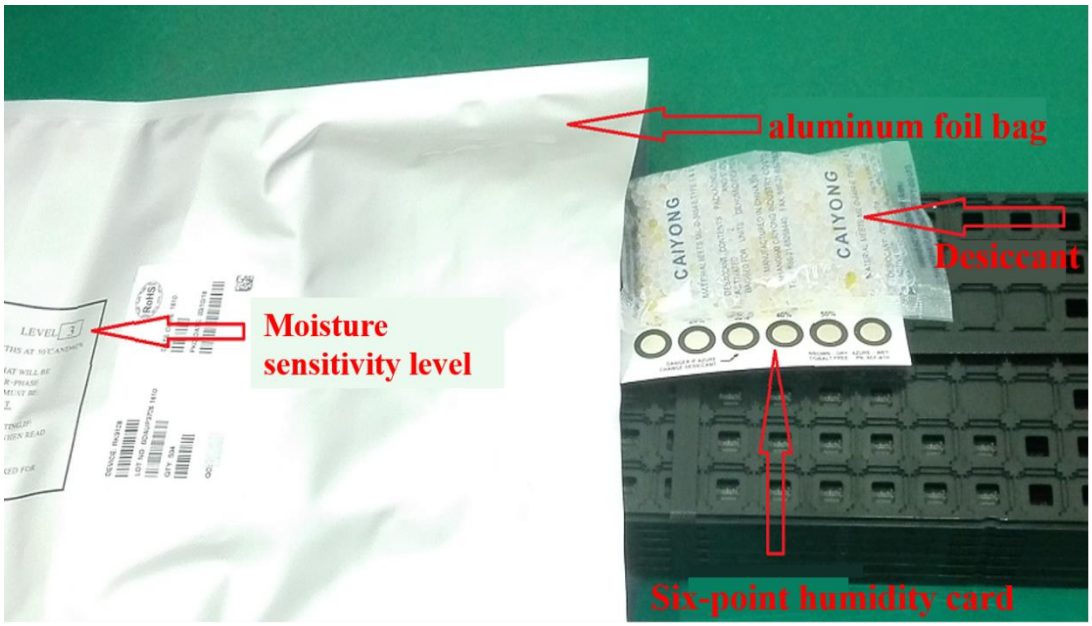


Figure 6-1 Dry Vacuum Packaging for Chip

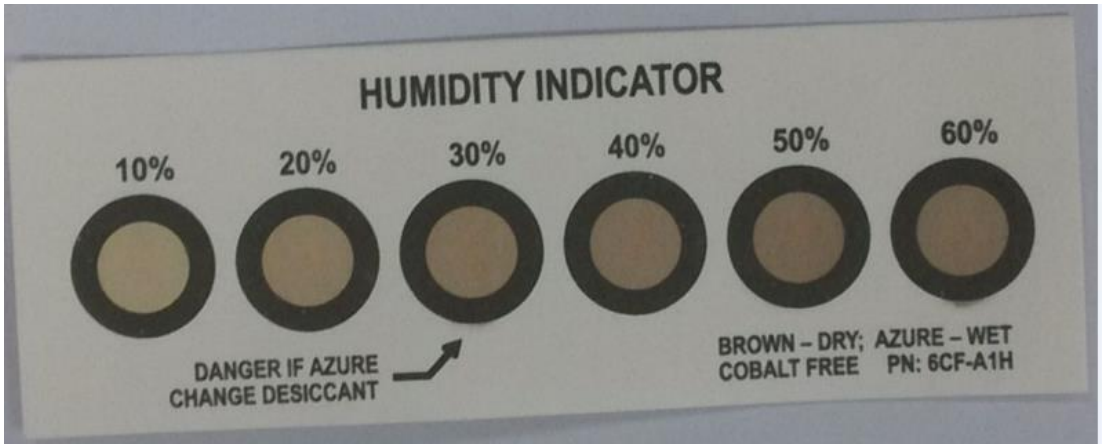


Figure 6-2 Six-point Humidity Card

6.4 Storage of Product

6.4.1 Storage Environment

The product is stored in vacuum packaging, and the shelf life can be up to 12 months when the temperature is less than 40°C and the relative humidity is less than 90%.

6.4.2 Exposure Time

Under ambient temperature <30℃ and humidity <60%, please refer to the following table 6-1.

The MSL level of RK3566 is 3, which is very sensitive to humidity. If it is not used in time after unpacking, and the chip is not baked after being placed for a long time, there will be a high probability of chip failure.

Table 6-1 Reference Table of Exposure Time (MSL)

MSL level	Exposure time Factory environmental conditions: ≦30 ℃ /60 ％RH
1	There is no restriction under the condition of ≤30 ℃/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	It must be baked before use and soldered within the time limit specified on the label

6.5 Usage of Moisture Sensitive Product

After the RK3566 chip is opened, the chip must meet the following conditions before reflow soldering:

- The continuous or cumulative exposure time is within 168 hours, and the factory environment is ≦30℃ /60% RH;
- Stored in <10% RH environment;

In the following cases, the chip must be baked to remove internal moisture to avoid delamination or popcorn

problems during reflow soldering:

- When the humidity indicator card is at 23±5℃, > 10% points have changed color. (Please refer to the label on the humidity indicator card for color changes);
- Does not meet the specifications of 2 or 2a;

Table 6-2 RK3566 Re-bake Reference Table

Package Thickness	MSL Level	High Temp Bake @125℃+10/-0℃		Medium Temp Bake @90℃+8/-0℃		Low Temp Bake @40℃+5/-0℃	
		Exceeding Floor Life > 72h	Exceeding Floor Life ≤ 72h	Exceeding Floor Life > 72h	Exceeding Floor Life ≤ 72h	Exceeding Floor Life > 72h	Exceeding Floor Life ≤ 72h
≤1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Note

The table shows the minimum baking time requirement after damp.

Preferred to use low-temperature baking.